Chapter 3

Reliability Improvements of Low Temperature Poly-Si Thin-Film Transistors with CF_4 Plasma Treatment

3.1 Introduction

The electrical characteristics of low-temperature poly-Si TFTs have been shown to be deeply influenced by grain-boundary and intragranular defects existed in poly-Si films [1-3]. To obtain high performance poly-Si TFTs, it is necessary to reduce the trap-states of the poly-Si films. It is well known that the hydrogenation process tends to tie up the grain-boundary dangling bonds and intragranular strain bonds with hydrogen, thereby remarkably improve the characteristics of the poly-Si TFTs [4-7]. However, it has been observed that the poly-Si TFTs with hydrogenation suffer from low hot-carrier endurance and thermal stability problems [8-9]. Recently, the research of the reliability issue in poly-Si TFTs is becoming a very important topic due to the great device performance instability of poly-Si TFTs under a long-term electrical stress. Several comprehensive studies have proposed that the degradation of poly-Si TFTs was mainly resulted from the conduction of a large amount of carriers, which induced the creation of metastable states within the poly-Si channel [8-10]. The hot-carrier and self-heating effect were also investigated in poly-Si TFTs [11-12] and were found to be accompanied well as that in MOSFETs.

Wu *et al*. attributed the degradation mechanism of hydrogenated poly-Si TFTs to the state creation in the channel caused by the breaking of weak Si-H bonds or Si-Si bonds, while the degradation rate increased with stressing bias voltage [10]. Moreover, self-heating has also been reported to be another degradation mechanism when poly-Si TFTs were fabricated on poor thermal conducting substrates, particularly for wide-channel TFTs and/or small-size TFTs [13-15]. The hot-carrier degradation phenomenon originating from a high drain electric field has also been widely discussed in many papers [16-18].

In this chapter, we first demonstrate that the significant performance improvements of the poly-Si TFTs by using CF_4 plasma treatment due to the passivation effect of the fluorine atoms. In this chapter, the stress immunity of the poly-Si TFTs with CF_4 plasma treatment was investigated in detail with two stress condition including hot-carrier mode self-heating mode.

3.2 Experimental details

The samples used in this experiment were the hydrogenated ELA poly-Si TFTs mentioned in the chapter 2, including the conventional TFTs and CF_4 plasma treated TFTs. The fabrication flows were described in Fig. 2-1.

The HP4156 precise semiconductor parameter analyzer was used to perform stress measurement on the TFTs and extract the transfer characteristics after application of bias stress.

3.3 Results and Discussion

The stress conditions were divided into two modes including hot-carrier stress (HCS) and self-heating stress (SHS). We use these two stress modes to examine the stress resistance of the hydrogenated LTPS TFTs. The applying stress bias for each stress modes was illustrated in Fig. 3-1. The stress bias of the hot-carrier mode was that $V_{G,stress}$ = 10V, $V_{D,stress}$ = 25V and source electrode was grounded. The stress bias of the self-heating mode was that $V_{G,stress}$ = 25V, $V_{D,stress}$ = 20V and source electrode was grounded.

3.3.1 Characteristics of poly-Si TFTs after hot-carrier stress

Fig. 3-2 and 3-3 show the transfer characteristics of the TFTs with and without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress. It can be seen that on-current and subthreshold-swing of the conventional TFTs were degraded significantly. However, less degradation was found of the TFTs with CF_4 plasma treatment. In this case, hot carriers were generated by impact ionization and induce the degradation of TFTs [17]. Therefore, the result of the transfer characteristics after stress indicates that the TFTs with CF_4 plasma treatment show higher stress immunity against the hot carrier degradation.

Fig. 3-4 and 3-5 show the output characteristics of the TFTs with and without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress. The driving current of the conventional TFTs after hot-carrier stress was reduced greatly compared with that of CF_4 plasma treated. Fig. 3-6 and 3-7 are the enlarged plots of Fig. 3-3 and 3-5. The driving current of the conventional TFTs after 1000sec hot-carrier stress shows enormous degradation at V_D = 0~2V. We deduce that the drain junction of the conventional TFTs might be damaged seriously by hot carriers during the impact ionization and lots of damages caused the resistance raised near the drain junction. On the contrary, the TFTs with CF_4 plasma treatment show small dagradation on driving current due to less damage near the drain junction.

Fig. 3-8 and 3-9 show the field effect mobility, On-current and subthreshold-swing degradation with stress time. It can be seen that the mobility and on-current degradation rate of the conventional TFTs is almost twice of the TFTs with CF_4 plasma treatment. The subthreshold-swing degradation rate of the conventional TFTs is thirteen times of the TFTs with CF_4 plasma treatment at the stress time of 1000sec.

3.3.2 Characteristics of poly-Si TFTs after self-heating stress

Fig. 3-10 and 3-12 show the transfer characteristics of the TFTs before and after 50sec and 1000sec self-heating stress. It can also be seen that on-current was more seriously degraded in conventional TFTs. Moreover, the subthreshold region of the conventional TFTs exhibits a hump phenomenon after self-heating stress. However, the subthreshold region of the TFTs with CF_4 plasma treatment is almost unchanged. In this case, TFTs are fabricated on buffer thermal oxide layers, which reduce the heat dissipation to the substrate. For this reason, TFTs can reach a very high temperature (over 300℃) during operation [17]. Such a high temperature will enhance the breaking of Si-H bonds and the generation of dangling bonds in the SiO_2/poly-Si interface, thus degrade the performance of the poly-Si TFTs. Therefore, the result of the transfer characteristics after stress indicates that the TFTs with CF_4 plasma treatment show higher stress immunity against the self-heating degradation.

Fig. 3-11 and 3-13 show the output characteristics of the TFTs before and after 50sec and 1000sec hot-carrier stress. The driving current of the conventional TFTs after self-heating stress was greatly reduced due to the generation of dangling bonds under a high temperature environment caused by device operation.

Fig.3-14 shows the field effect mobility and ON-current degradation with stress time. It can be seen that the mobility and on-current degradation rate of the conventional TFTs is almost triple of that for the TFTs with CF_4 plasma treatment.

3.3.3 Device degradation mechanisms and fluorine passivation effect

Fig.3-15 shows the degradation of mobility defined as ?μ_{eff}/ $\mu_{eff,0}$, where ?μ_{eff} = $\mu_{eff,str} - \mu_{eff,0}$, $\mu_{eff,0}$ is the initial mobility and $\mu_{eff,str}$ is the mobility after stress. It is noticed that ?μ_{eff}/ $\mu_{eff,0}$ exhibits a power-time dependent law of the form [19]

?$\mu_{eff}/\mu_{eff,0} = At^n$---**(Eq. 3.1)**

The pre-power law factor A is empirically expressed as [20]

A ? exp(-a/$V_{D,str}$)--**(Eq. 3.2)**

where a is a constant and depends only on the device process. According to hot-carrier degradation theory [20], exponent n of a power-time dependent law is independent of $V_{D,str}$ merely depending on $V_{G,str.}$ This indicates that n is associated to the mechanisms of device degradation. From Fig.3-15, the exponent n of the HCS and SHS are approximately 0.31 and 0.43 respectively. That is to say the degradation mechanisms of these two stress modes are quite different. It has been reported that the exponent n = 0.2 corresponding to carrier trapping mechanism and 0.5~0.7 corresponding to interface state generation mechanism for MOSFETs [21]. Therefore, we can deduce that exponent n = 0.31 is close to carrier trapping degradation due to impact ionization of hot carriers and exponent n = 0.43 is perhaps the interface state generation due to breaking bonds by high temperature operation.

Fig. 3-16 shows the atomic model of the SiO_2/poly-Si interface. For the case of the conventional TFTs, weak Si-H or Si-O bonds get broken during electrical stress thus enhance the formation of dangling bonds and strain bonds and further degrade the device performance. On the contrary, the incorporation of fluorine atoms by CF_4 plasma treatment not only passivates the dangling bonds and strain bonds but also forms strong Si-F bonds. Therefore, the stress immunity of TFTs with CF_4 plasma treatment gets raised.

3.4 Summary

The reliability test of hydrogenated poly-Si TFTs with and without CF_4 plasma treatment has been investigated by hot-carrier stress and self-heating stress. Under hot-carrier stress and self-heating stress, TFTs with CF_4 plasma treatment exhibit higher stress immunity than conventional TFTs. It cab be speculated that the incorporation of fluorine atoms by CF_4 plasma treatment not only passivates the dangling bonds and strain bonds but also forms strong Si-F bonds, thus raises the stress resistance.

3.5 References

[1] R. E. Proano, R. S. Misage, D. Jones, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 9, p. 1915, 1989.

[2] T. S. Li and P. S. Lin, "On the pseudo-subthreshold characteristics of polycrystalline-silicon thin film transistors with large grain size," *IEEE Electron Devices lett.*, vol. 14, no. 5, pp. 240, 1993.

[3] Y. Morimoto, Y. Jinno, K, Hirai, H, Ogata, T. Yamada, and K. Yoneda, "Influence of the grain boundaries and intragrain defects on the performance of poly-Si thin film transistors," *J. Electrochem. Soc.*, vol. 144, no. 7, p. 2495, 1997.

[4] T. I. Kamins, and Marcoux, "Hydrogenation of transistors fabricated in polycrystalline-silicon films," *IEEE Electron Devices lett.*, vol. 1, no. 8, pp. 159, 1980.

[5] Y. S. Kim, K. Y. Choi, and M. K. Han, "Different hydrogen passivation mechanisms between low-temperature and high-temperature poly-Si TFTs," *Jpn. J. Appl. Phys.*, vol. 34, no. 28, p. 719, 1995.

[6] M. Can, T. Zhao, K. C. Saraswat, and J. S. Plummer, "Study of hydrogenation of Polysilicon thin film transistors by ion implantation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, p. 1134, 1995.

[7] R. A. Ditizio, G. Liu, and S. J. Fonash, "Short time electron cyclotron resonance hydrogenation of polycrystalline silicon thin-film transistor structures," *Appl. Phys. Lett.*, vol. 56, no. 12, p. 1140, 1990.

[8] S. Banerjee, R Sundaresan, H. Schichijo, and S. Malhi, "Hot-carrier degradation of n-channel Polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p.

152, 1988.

[9] M. Hack, A. G. Lewis, and I. W. Wu, "Physical models for degradation effects in Polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, no. 5, p. 890, 1993.

[10] I-Wei Wu, Warren. B. Jackson, Tiao-Yuan Huang, Alan G. Lewis, and Anne Chiang, "Mechanism of device degradation in n- and p-channel polysilicon TFT's by electrical stressing," *IEEE Electron Devices lett.*, vol. 11, pp. 167-170, 1990.

[11] M. Koyanagi, I. W. Wu, A. G. Lewis, M. Fuse, and R. Bruse, "Evaluation of polycrystalline silicon thin-film transistor with the charge pumping technique," in *IEDM Tech. Dig.* 1990, p.863

[12] J. W. Lyding, K. Hess, and I. C. Kizilyalli, "Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing," *Appl. Phys. Lett.*, vol. 68, no. 18, p. 2526, 1996.

[13] S. Inoue, H. Ohshima, T. Shimoda, "Analysis of threshold voltage shift caused by bias stress in low temperature poly-Si TFTs," in *IEDM Tech. Dig.*, p.527, 1997,

[14] Y. Mishima, K. Yoshino, M. Takei, N. Sasaki, "Characteristics of low-temperature poly-Si TFTs on Al/glass substrates," *IEEE Trans. Electron Devices*, Vol. 48, p.1087-1091, June, 2001.

[15] N. Kato, T. Yamada, S. Yamada, T. Nakamura, T. Hamano, "Degradation mechanism of polysilicon TFTs under DC stress," in *IEDM Tech. Dig.*, p. 677-680, 1992

[16] G. Fortunato, A. Pecora, G. Tallarida, L. Mariucci, C. Reita, and P. Migliorato, "Hot Carrier Effects in n-Channel Polycrystalline Silicon Thin-Film Transistors: A Correlation Between Off-Current and Transconductance Variations," *IEEE Trans. Electron Devices*, Vol. 41, p.340-346, March 1994.

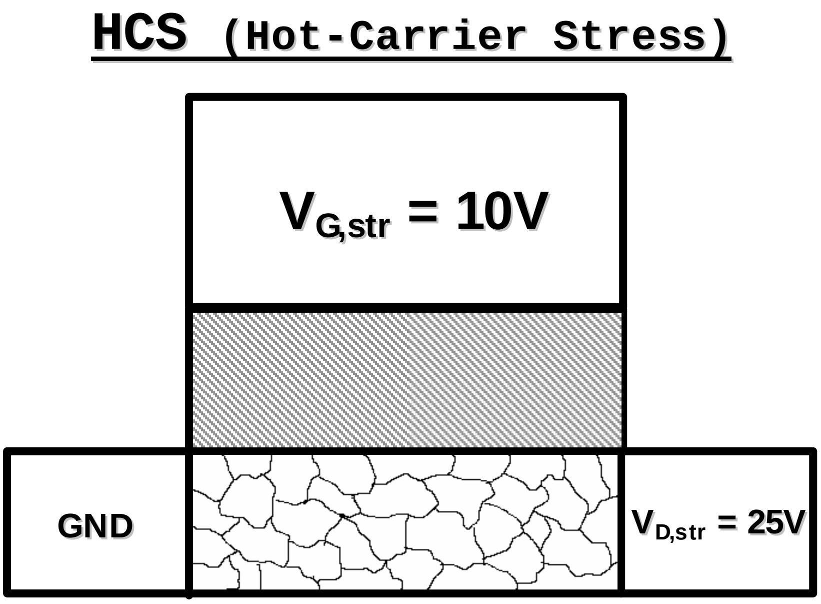
[17] Satoshi INOUE, Mutsumi KIMURA, and Tatsuya SHIMODA, "Analysis and Classification of degradation Phenomena in Polycrystalline-Silicon Thin Film Transistors Fabricated by Low-Temperature Process Using Emission Light Microscopy," *Jpn. J. Appl. Phys.*, vol. 42, pp. 1168-1172, March 2003.

[18] C. W. Lin, C. H. Tseng, T. K. Chang, Y. H. Chang, F. T. Chu, C. W. Lin, W. T. Wang, and H. C. Cheng, "An Investigation of Bias Temperature Instability in Hydrogenated Low-Temperature Polycrystalline Silicon Thin Film Transistors," *Jpn. J. Appl. Phys.*, vol. 41, pp. 5517-5522, September 2002.

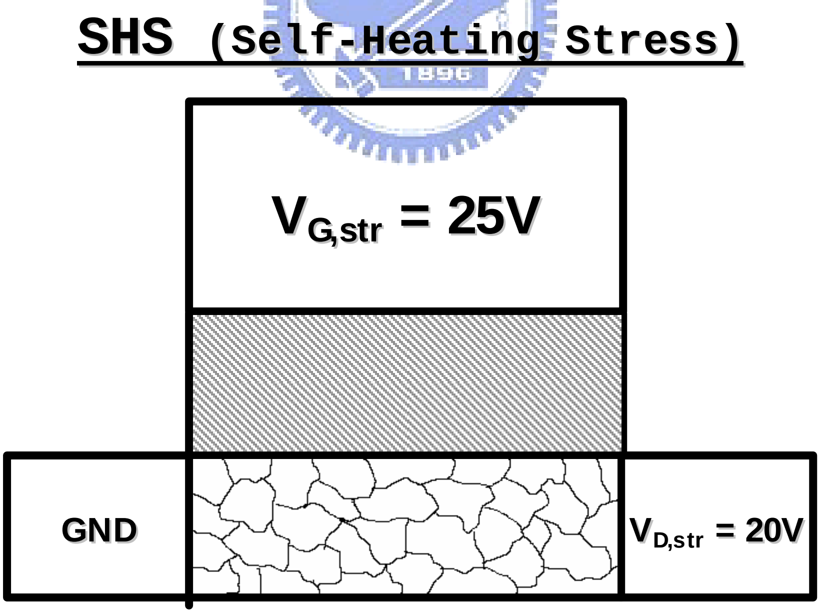
[19] F. V. Farmakis, J. Brini, G. Kamarinos, and C. A. Dimitriadis, "Anomalous Turn-On Voltage Degradation During Hot-Carrier Stress in Polycrystalline Silicon Thin-Film Transistors," *IEEE Electron Devices lett.*, vol. 22, pp. 74-76, 2001.

[20] E. Takeda, C. Y. Yang, and A. Miura-Hamada, "Hot-carrier Effects in MOS Devices," New York: Academic, p. 68, 1995.

[21] P. Heremans, R. Bellens, G. Groeseneken, H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs," *IEEE Trans. Electron Devices*, Vol. 35, p.2194-2209, Dec 1988.



(a) Hot-carrier stress



(b) Self-heating stress

Fig.3-1 Applying bias of the two electrical stress including (a) hot-carrier stress and (b) self-heating stress.

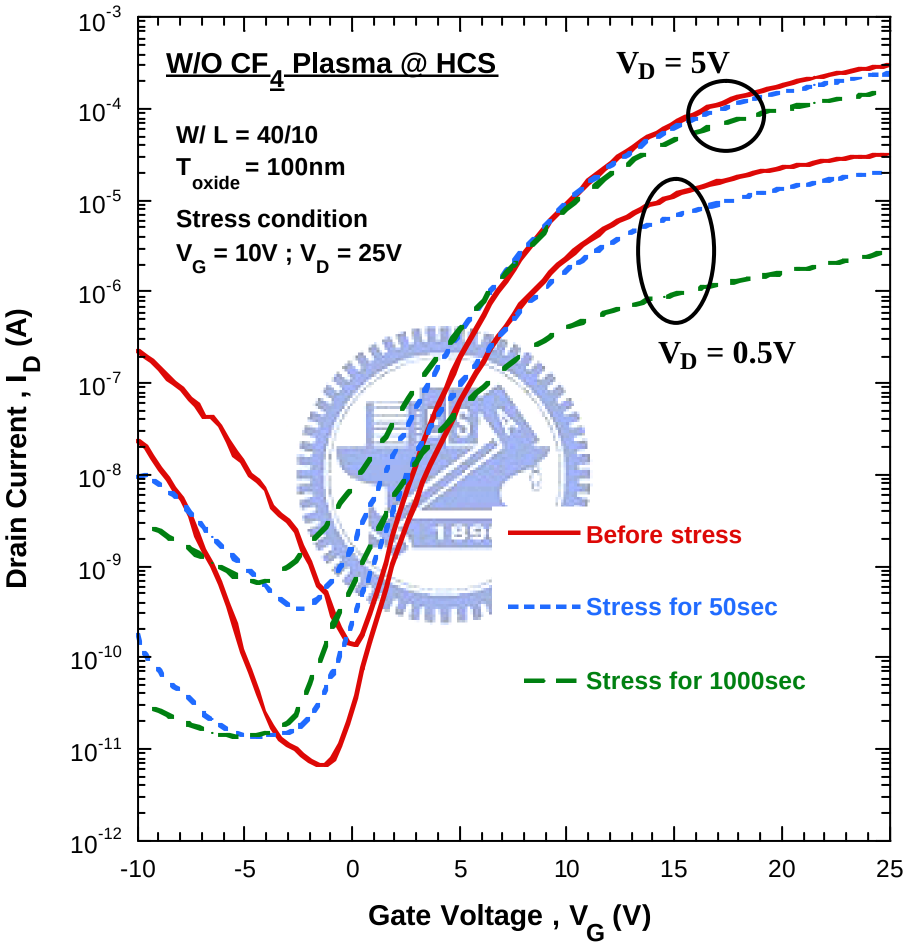


Fig.3-2 Transfer characteristic of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

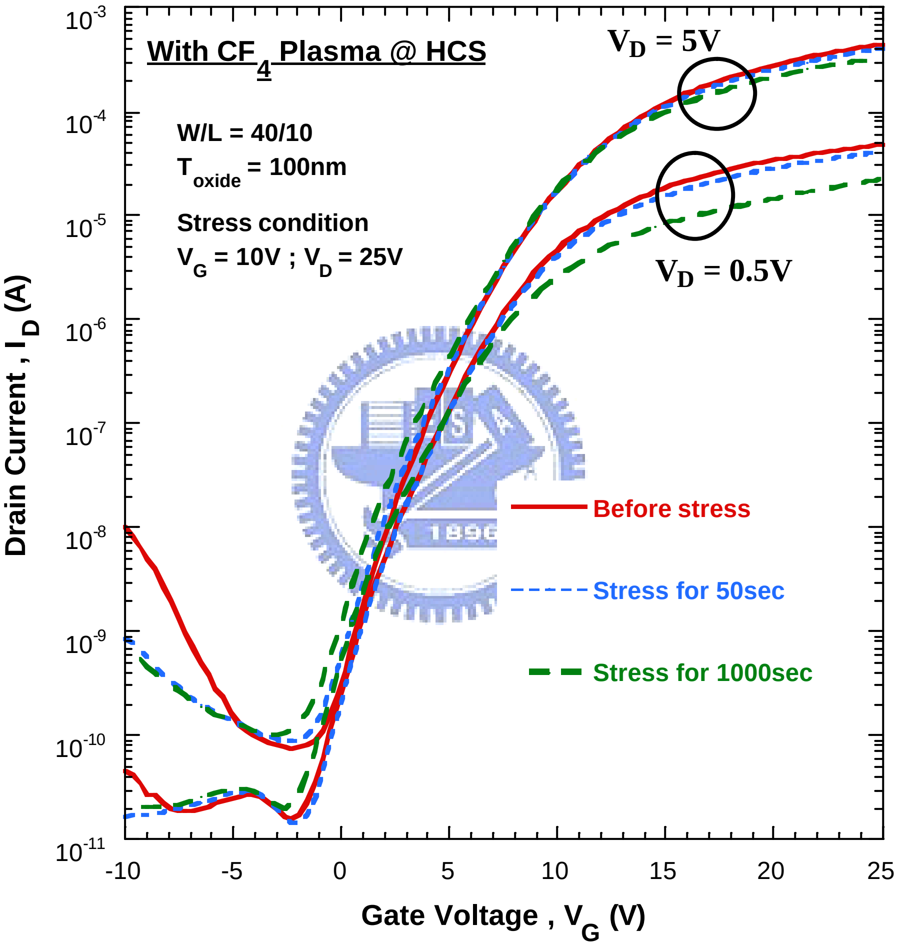


Fig.3-3 Transfer characteristic of the TFTs with CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

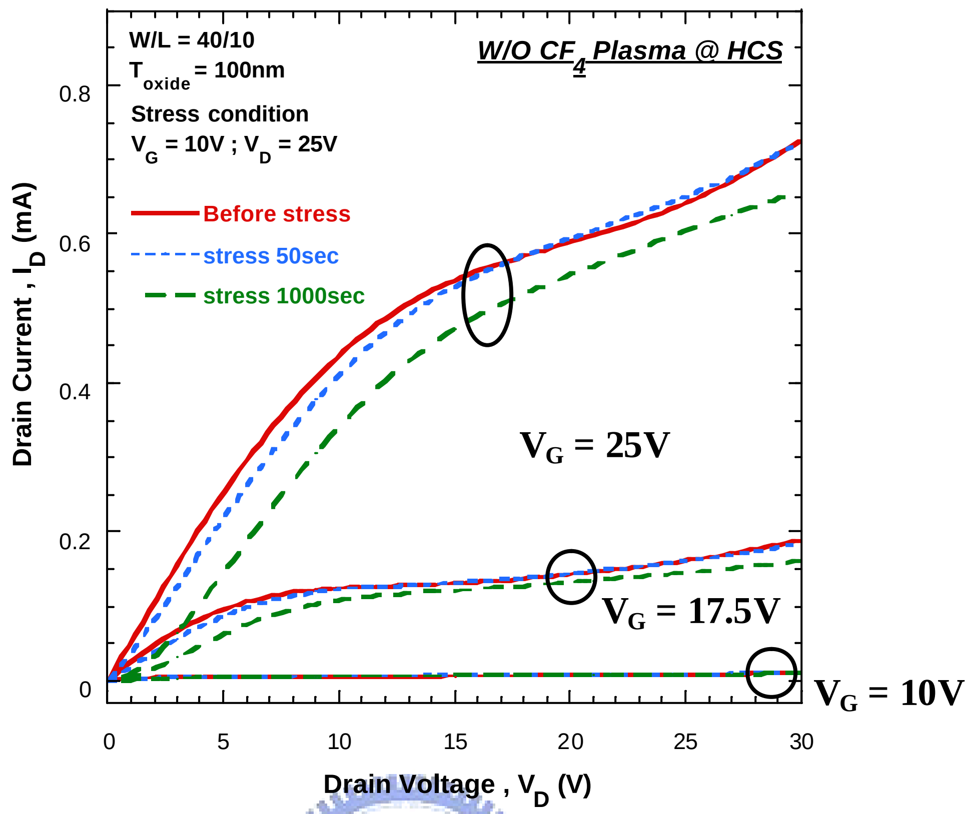


Fig. 3-4 Output characteristic of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

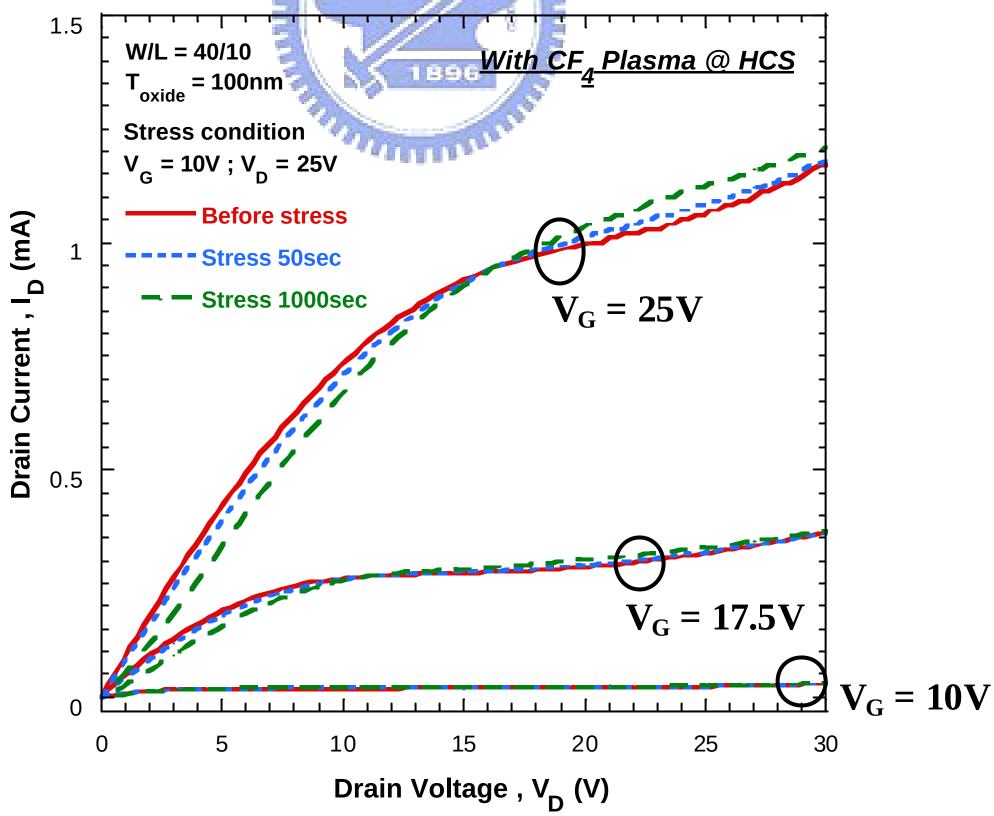


Fig.3-5 Output characteristic of the TFTs with CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

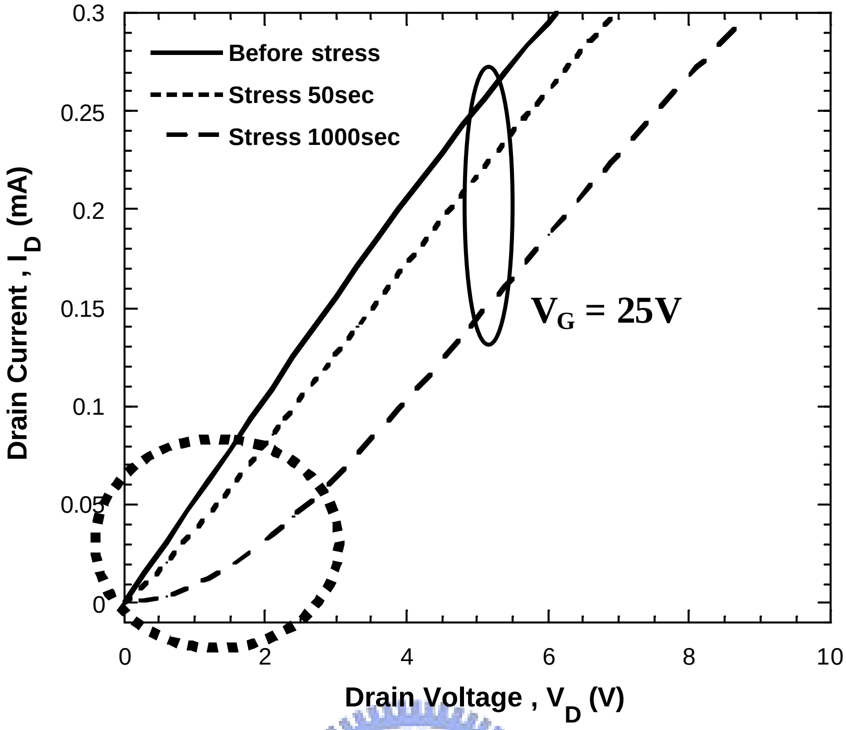


Fig. 3-6 Enlarged plot of the output characteristic of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

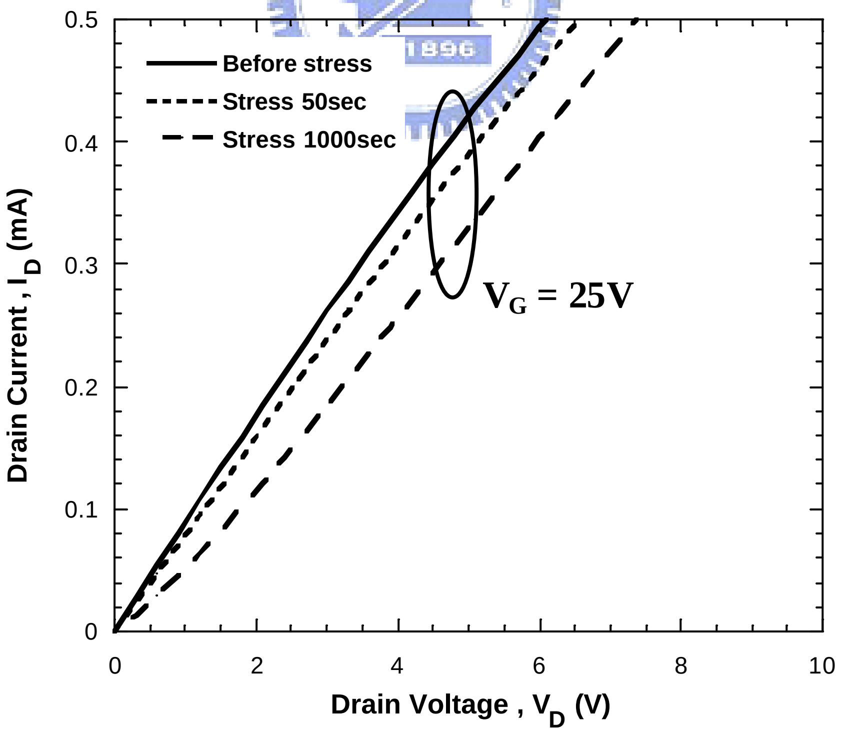
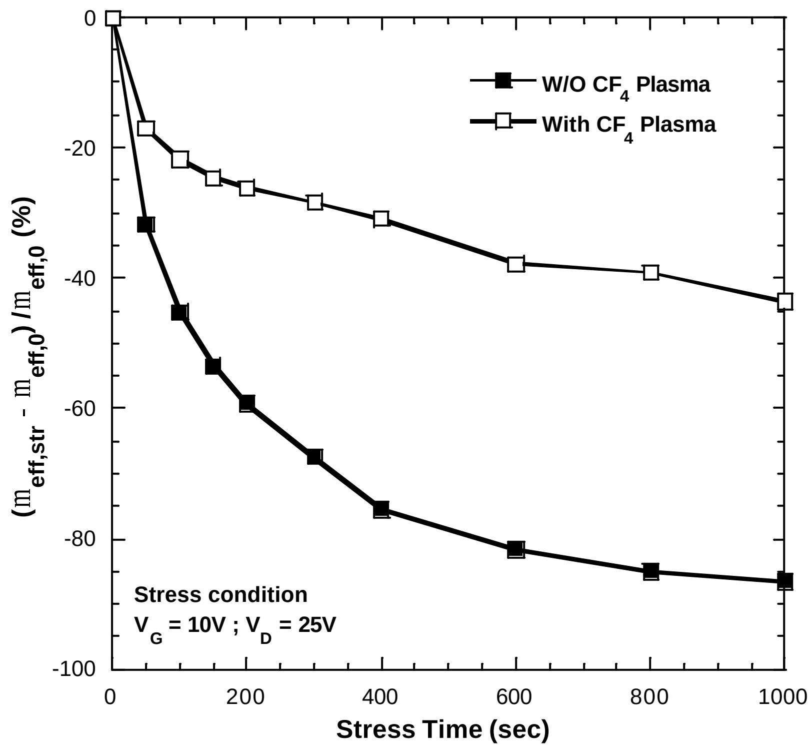
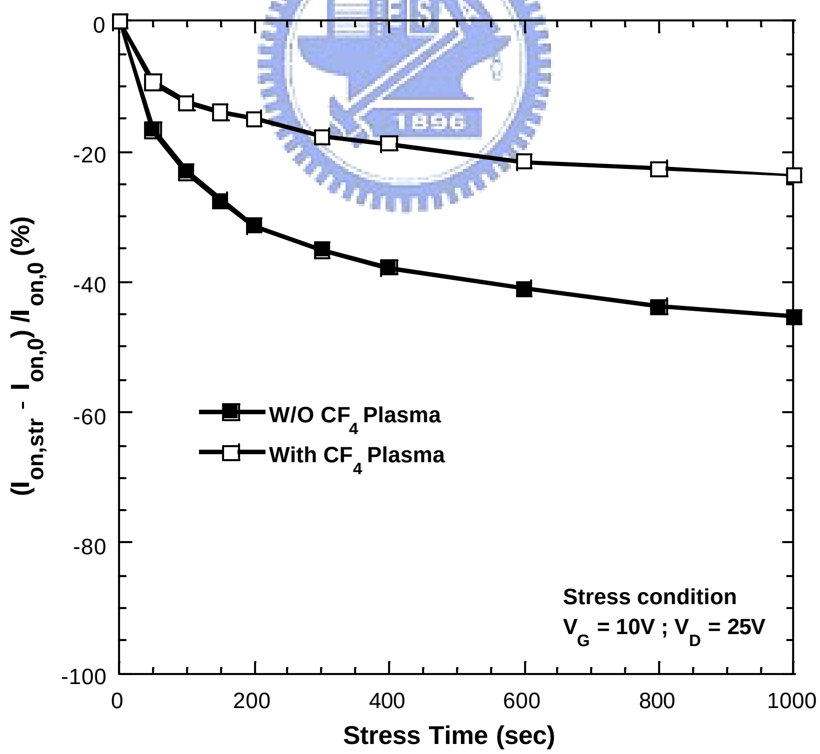


Fig.3-7 Enlarged plot of the output characteristic of the TFTs with CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.



(a) Mobility degradation with stress time



(b) ON-current degradation with stress time

Fig.3-8 (a) mobility and (b) ON-current degradation with time under self-heating stress.

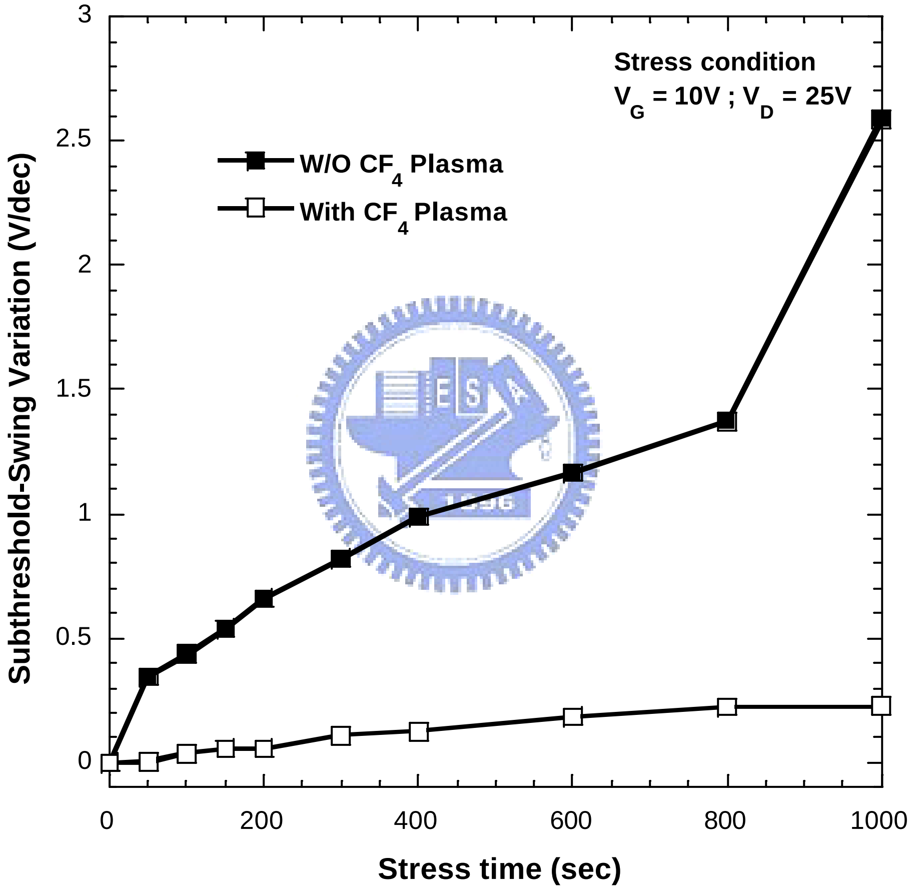


Fig.3-9 Subthreshold-swing degradation with time under hot-carrier stress.

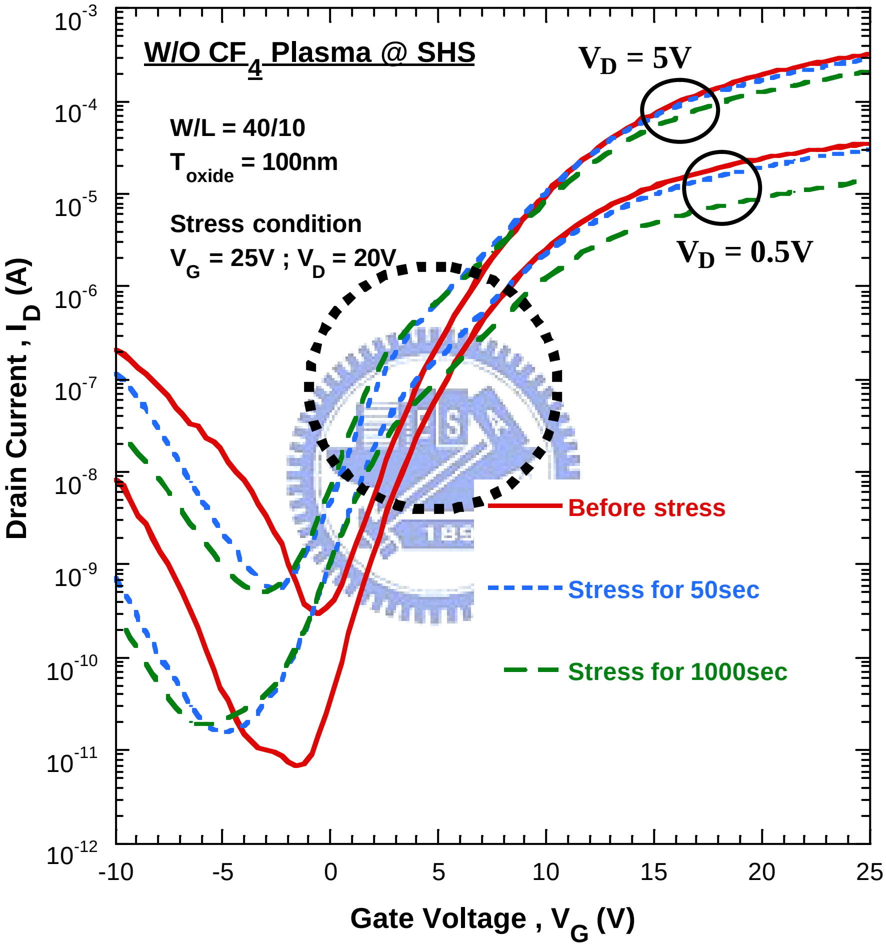


Fig.3-10 Transfer characteristic of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec self-heating stress.

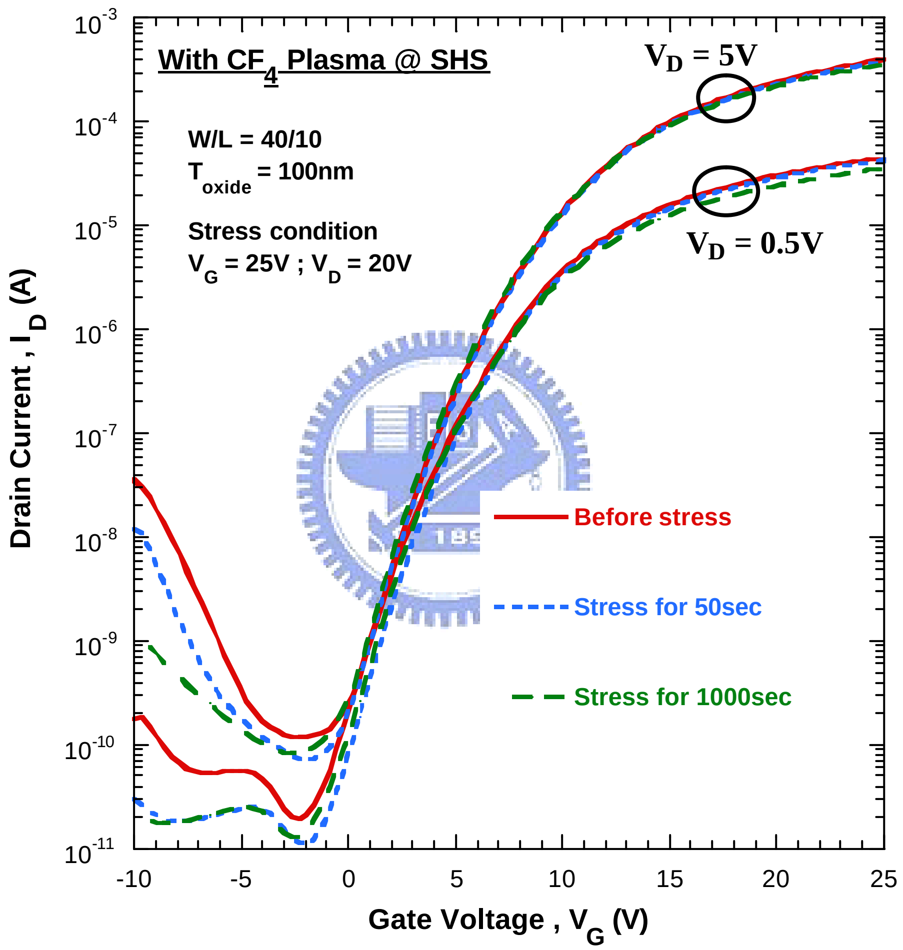


Fig.3-11 Transfer characteristic of the TFTs with CF_4 plasma treatment before and after 50sec and 1000sec self-heating stress.

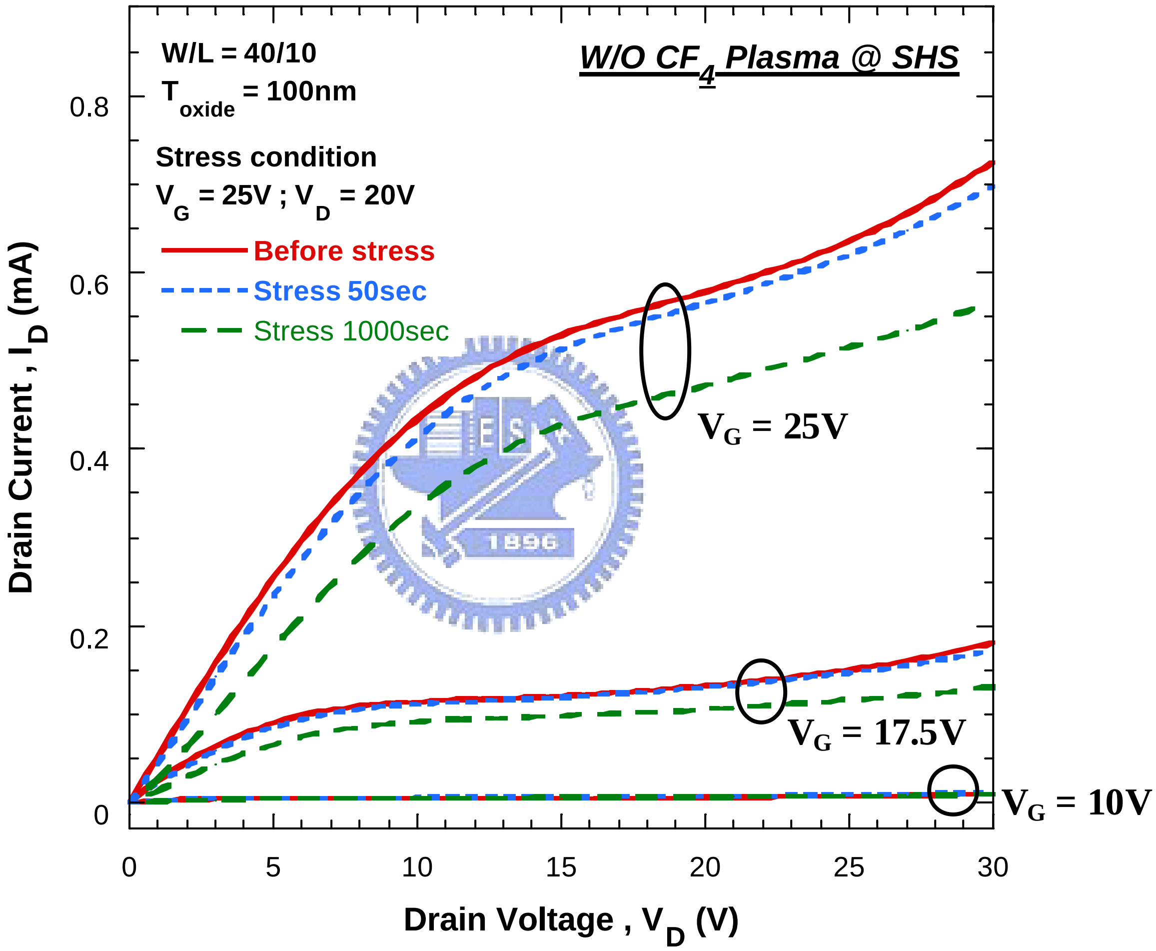


Fig. 3-12 Output characteristic of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec self-heating stress.

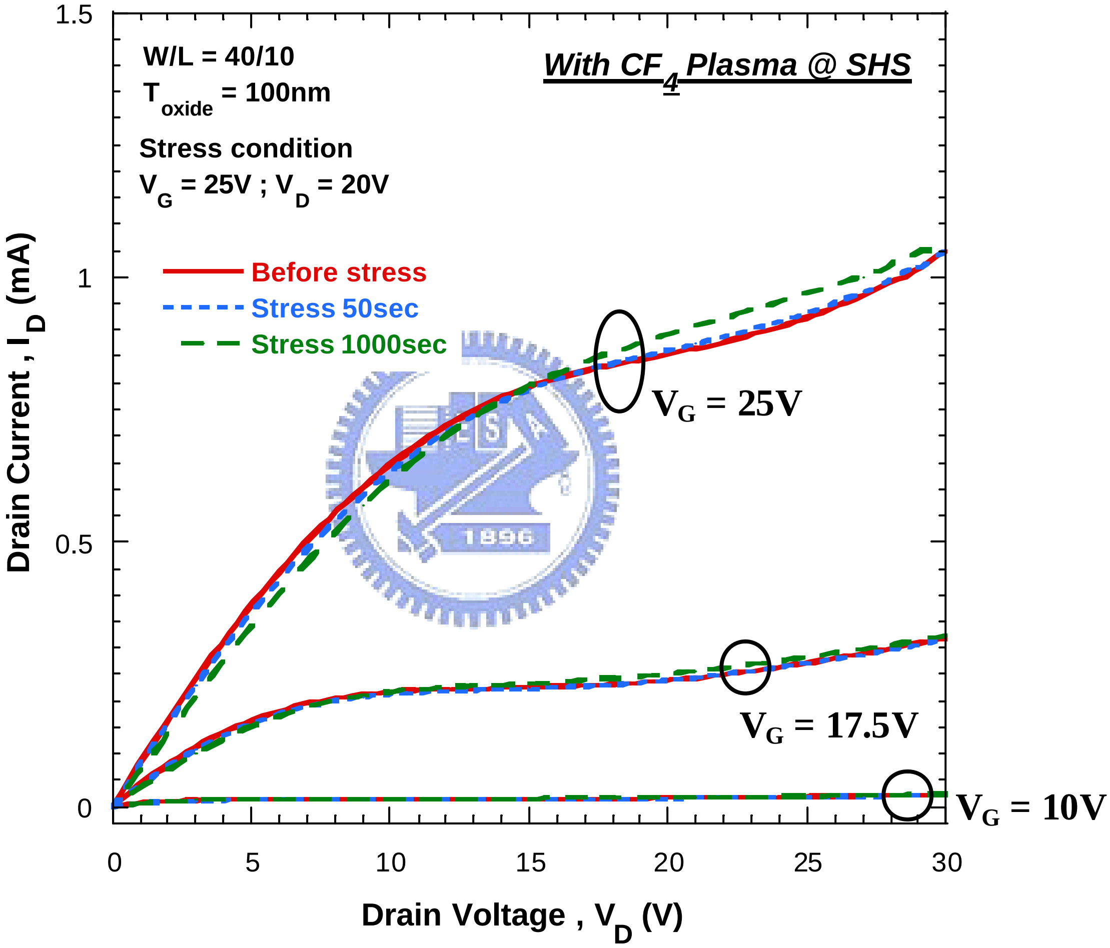
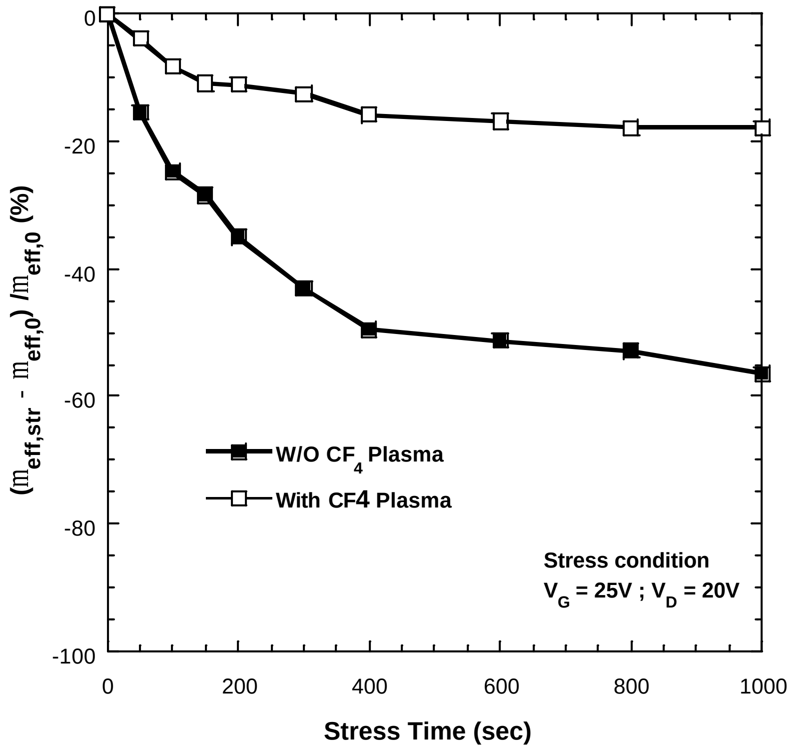
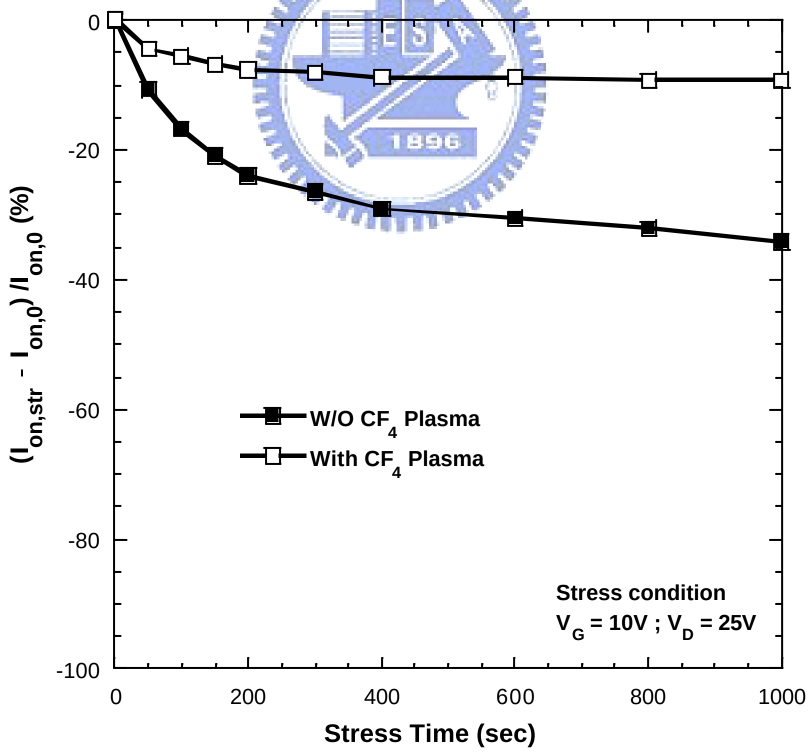


Fig. 3-13 Output characteristic of the TFTs with CF_4 plasma treatment before and after 50sec and 1000sec self-heating stress.

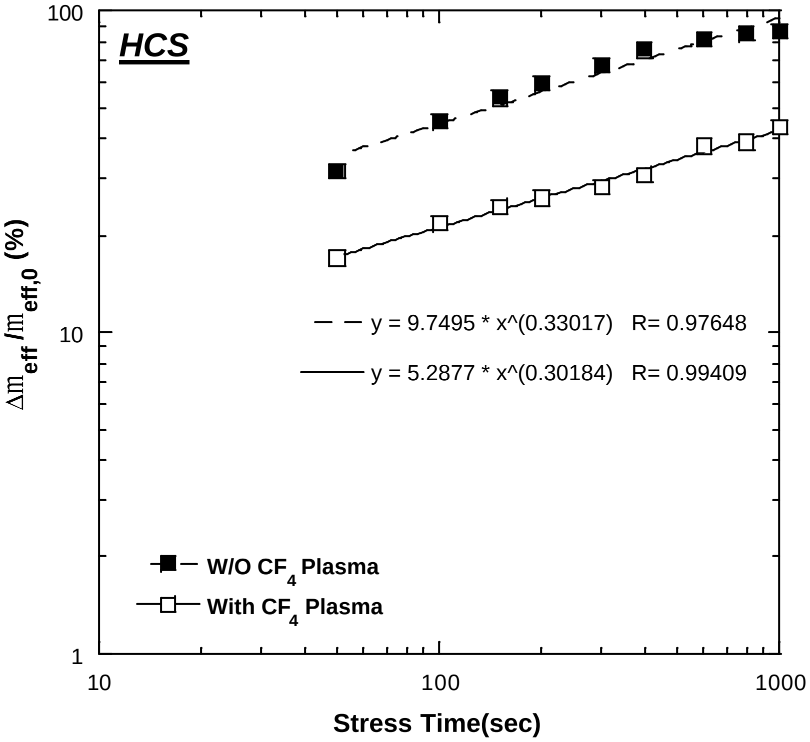


(a) Mobility degradation with stress time

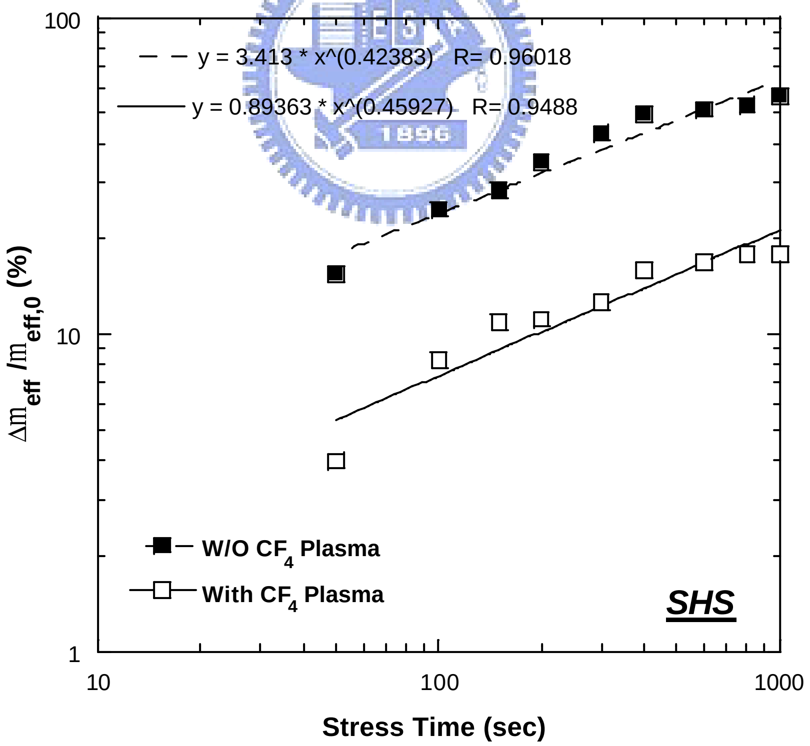


(b) ON-current degradation with stress time

Fig.3-14 (a) mobility and (b) on current degradation with time under self-heating stress.

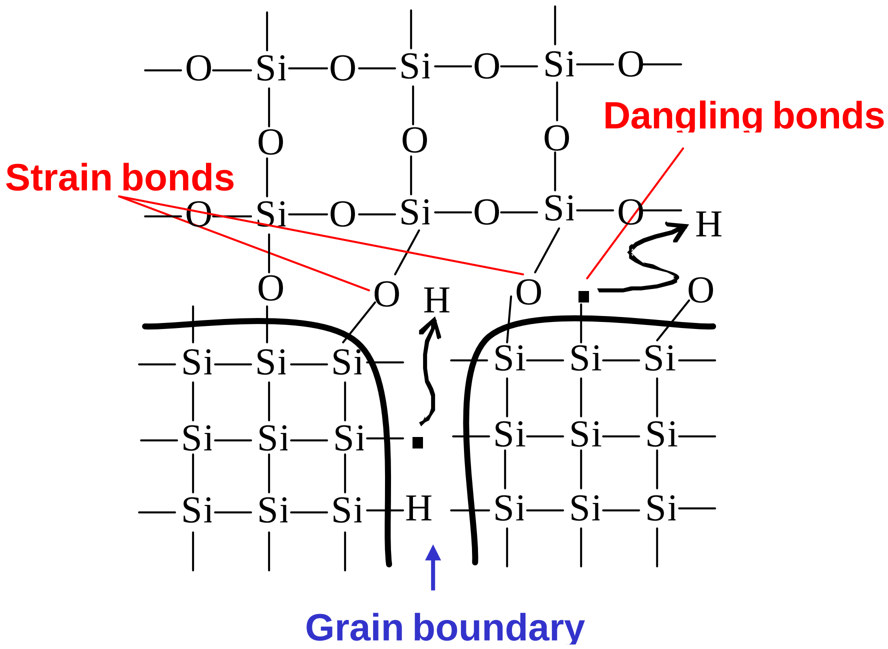


(a) Mobility degradation rate under hot-carrier stress

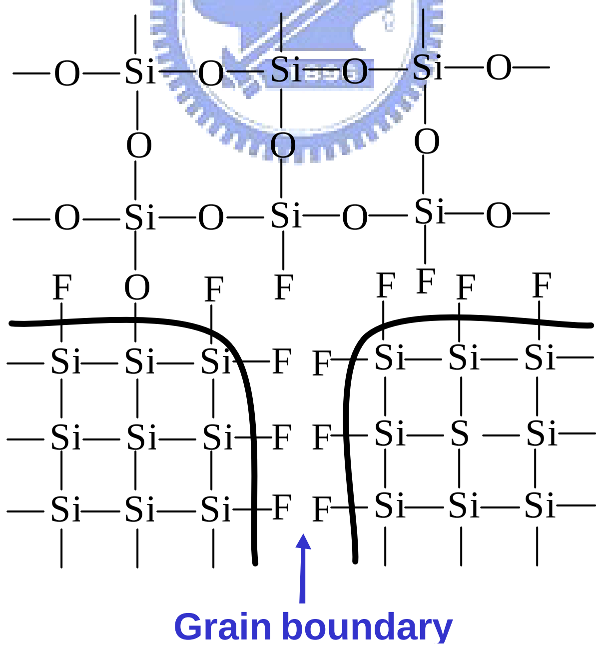


(b) Mobility degradation rate under self-heating stress

Fig.3-15 Mobility degradation rate fitted by power-time dependent law under (a) hot-carrier and (b) self-heating stress.



(a) Without CF_4 plasma



(b) With CF_4 plasma

Fig. 3-16 Atomic model of the SiO_2/poly-Si interface (a) without CF_4 plasma, and (b) with CF_4 plasma.