Chapter 4

Analysis of Hot-Carrier Induced Degradation in Hydrogenated Low Temperature Poly-Si TFTs

4.1 Introduction

For the realization of system-on-panel (SOP), one of the most highly expected next generation systems, the role of LTPS TFTs is getting more and more important. Since high-speed circuits such as processors, memories, drivers and so on are needed to be integrated with a pixel array on the same glass substrate; further advances of performance and reliability of LTPS TFTs are strongly required. However, hot -carrier degradation phenomena restricts the design of large-scale integrated circuits, increase the power dissipation and decrease the reliability of digital circuits [1-5]. It is worth pointing out that due to the high density of trap states lozalized at the grain boundaries in poly-Si [6-8], electric field will be enchanced [9], even at moderate biases. It is therefore essential to investigate the hot-carrier induced degradation in order to determine the long-term reliability of LTPS TFTs.

In this chapter, the stress gate voltage dependence of TFTs dagradation was carried out to determine at what stress gate voltage the maximum device degradation will happen. In order to further understand the degradation related to hot carriers, the on-current (I_{on}) and off-current (I_{off}) variation measured at different drain voltage were extracted under various stress modes. Finally, the mechanism of device degradation under these types stress conditions was proposed.

4.2 Experimental details

The samples used in this experiment were the conventional hydrogenated ELA poly-Si TFTs mentioned in the chapter 2. The fabrication flows were described in Fig. 2-1.

The HP4156 precise semiconductor parameter analyzer was used to perform stress measurement on the TFTs and extract the transfer characteristics after applying bias stress. The stress was performed at various gate voltages with a fixed drain voltage of 20V and source grounded. The I_{on} and I_{off} were defined at the gate voltage of 5V and drain voltage of 25V and -7V, respectively. The variation of I_{on} and I_{off} were defined as $(I_{on,stress} - I_{on,initial})/ I_{on,initial} \times 100\%$ and $(I_{off,stress} - I_{off,initial})/ I_{off,initial} \times 100\%$, where the $I_{on,initial}$ and $I_{on,stress}$ are the measured I_{on} prior to and after the electrical stress; $I_{off,initial}$ and $I_{off,stress}$ are the measured I_{off} prior to and after the electrical stress.

4.3 Results and Discussion

4.3.1 Stress gate voltage dependence of TFTs dagradation

Fig. 4-2 and 4-3 show the I_{on} and I_{off} variations under various static stress conditions. For I_{on} degradation, while $V_{G,stress} < V_{th}$ (2.5V), the channel was not formed and therefore the current was small, which led to a small I_{on} degradation observed. As $V_{G,sress}$ increase, the current increased and depredated device seriously. This is due to the impact ionization induced lots of hot carriers' generation near the drain side, which causes lots of trap states in the poly-Si. This phenomenon is also called drain avalanche hot carrier injection or DAHC. As $V_{G,sress}$ larger than 15V, the electric field of the pinch-off region is depressed and the acceleration of carrier dropped, small derogation of I_{on} was found. In this case, it has been report that weak bonds can be broken and causes lots of interface states due to the high temperature

created by large currents. These interface states are believed to distribute uniformly located in whole channel instead of at drain side. That is why we obsreved a small variations of I_{on} and I_{off}.

On the other hand, for the I_{off} variation, the first stage shows a lowering I_{off}, which is due to many positive charges trapped in oxide near the drain side. These positive charges can be attributed to a high electric field formed between the low gate voltage and the high drain voltage stress conditon [10]. In this cast, hot holes are favoerable to be injected into gate oxide above channel near the drain side and ease the local electric field to reduce the I_{off}. With $V_{G,stress}$ increases, lots of DAHC induced trap states increase and dominate the I_{off} variation, leading to a large increase of. I_{off}. As $V_{G,sress}$ larger than 15V, the variation is reduced.

Therefore, three stages can be distinguished: As $V_{G,stress} < V_{th}$, small current induce slight trap states. However, in this case, high electric field caused positive charges trapping reduce the I_{off}. As $V_{th} < V_{G,stress} <$ 15V, lots trap states, induced by hot carrier impact ionization (or DAHC) near the drain side dominate the increase of the I_{off}. As $V_{G,sress} >$ 15V, the degradation of devise decrease with the electric field in the channel near the drain side.

4.3.2 ON/OFF current variation at various drain voltage after hot-carrier stress

To clarified this assumption, the ?I_{off} defined as $I_{off,stress} - I_{off,initial}$ versus different drain voltage was measured in Fig. 4-4. It is well known that I_{off} can be attributed to thermionic emmission at low electric filed and field-enhanced generation (or filed emission) at high electric filed. This electric filed is relative to $(V_{DS}-V_{GS})/d_{ox}$. The

different curves are obtained by applied three types of $V_{G,stress}$ (0V, 10V and 20V) with $V_{D,stress}$ of 20V and stress time of 1000sec. We found that a great of ?I_{off} can be observed as $V_{DS}>8V$ dut to field-enhanced generation occurred. At $V_{G,stress}$ = 0V (type-A), favorable positive charges trapping trend to decrease $I_{off.}$ With $V_{G,stress}$ = 10V (type-B), the impact ionization increase during stress and cause a lot of trap states in poly-Si and poly-Si interface. In this case, I_{off} arise due to trap assisted leakage current and I_{off} increase with increaseing measured drain voltage. As $V_{G,sress}$ = 20V (type-C), the I_{off} become nearly unchanged. It is deduced that the stress induced interface states uniformly distribute in the whole channel, not especially near the drain side. Therefore, the I_{off} don't be affected strongly.

Fig. 4-5 shows the the variations rate (?$I_{on}/I_{on,initial}$) of I_{on} versus drain voltage with three types of stress conditions, First, the ?$I_{on}/I_{on,initial}$ decrease with the drain voltage. This indicates that the trap states near the drain junction will affected by the applyed drain voltage. It is believed that when the drain voltage increases, the potential barrier established by trap states near the drain side will be pulled down, and thus reduce the influence of trap states for carriers. The description of such effect is illustrated in Fig. 4-6. At $V_{G,stress}$ = 0V (type-A), the ?$I_{on}/I_{on,initial}$ become positive when V_D > 8V. This implies that after the lowering of the barrier of trap states, the positive charges trapping in gate insulator governs and trends to cause channel shorting near the drain junction, thus incraese the on-current. With $V_{G,stress}$ = 10V (type-B), the serious impact ionization causes damages near the drain junction, and thus create lots of trap states, which lead to serious I_{on} degradation. As $V_{G,sress}$ = 20V (type-C), the ?$I_{on}/I_{on,initial}$ is less affected with the drain voltage due to interface states generated uniformly in the whole channel. According to all the results observed in our experiments, the device degradation model has been proposed in Fig. 4-7, 4-8 and 4-9.

4.4 Summary

In this chapter, we propose a systematic experimental study of the on-current and off-current variations of ELA and hydrogenation processed poly-Si TFTs by applying a various static stress conditions. We found that the on and off-current are strongly affected by the applied static stress conditions. This is due to different amount of charge trapping in gate oxide and trap states generation in poly-Si caused by applying different stress conditions. These results help us to understand more about mechanisms responsible for the degradation of poly-Si TFTs under static stress.

4.5 References

[1] G. Fortunato, A. Pecora, G. Tallarida, L. Mariucci, C. Reita, and P. Migliorato, "Hot Carrier Effects in n-Channel Polycrystalline Silicon Thin-Film Transistors: A Correlation Between Off-Current and Transconductance Variations," *IEEE Trans. Electron Devices*, vol. 41, no. 3, p. 340, 1994.

[2] S. Banerjee, R. Sundaresan, H. Schichijo, and S. Malhi, "Hot-carrier degradation of n-channel Polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 152, 1988.

[3] I-Wei Wu, Warren. B. Jackson, Tiao-Yuan Huang, Alan G. Lewis, and Anne Chiang, "Mechanism of device degradation in n- and p-channel polysilicon TFT's by electrical stressing," *IEEE Electron Devices lett.*, vol. 11, pp. 167-170, 1990.

[4] T. Yoshida, Y. Ebiko, M. Takei, N. Sasaki, and T. Tsuchiya, "Grain Boundary Related Hot Carrier Degradation Mechanism in Low-Temperature Polycrystalline Silicon Thin-Film Transistors," *Jpn. J. Appl. Phys.*, Vol. 42, p.1999, 2003.

[5] L. Mariucci, A. Pecora, G. Fortunato, C. Reita, and P. Migliorato, "Hot Carrier Effects in Polycrystalline Silicon Thin-Film Transistors," Microelectronic Eng., vol. 19, pp. 109-114, 1992

[6] G. Fortunato, and P. Migliorato, "Determination of gap state density in polycrystalline silicon by field-effect conductance," *Appl. Phys. Let.*, Vol. 49, p.1025-1027, Oct. 1986.

[7] G. Fortunato, and P. Migliorato, "Model for the above-threshold characteristics and threshold voltage in polycrystalline silicon transistor," *J. Appl. Phys.*, Vol. 68, p.2463-2467, Sept. 1990.

[8] J. H. Werner, "Band tailing in polycrystalline and disordered silicon," in *Polycrystalline Semiconductor* , pp. 345-351, 1989.

[9] C. . Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-T. Chan, and K. W. Terril, "Hot-electron-induced MOSFET degradation model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 375-385, 1985.

[10] J. Chen, T. Y. Chan, P. K. Ko, and C. Hu, "Gate Current in OFF-State MOSFET," *IEEE Electron Devices lett.*, vol. 10, no. 5, pp. 203-205, May 1989.

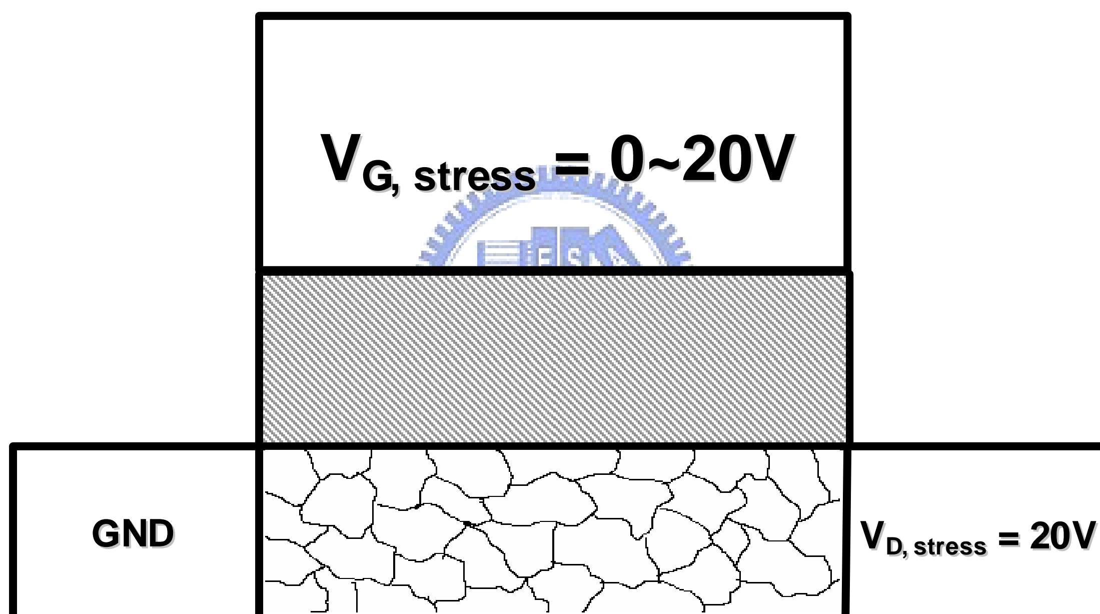

Fig.4-1 Schematic diagram of poly-Si TFT device structure and the applying stress conditions.

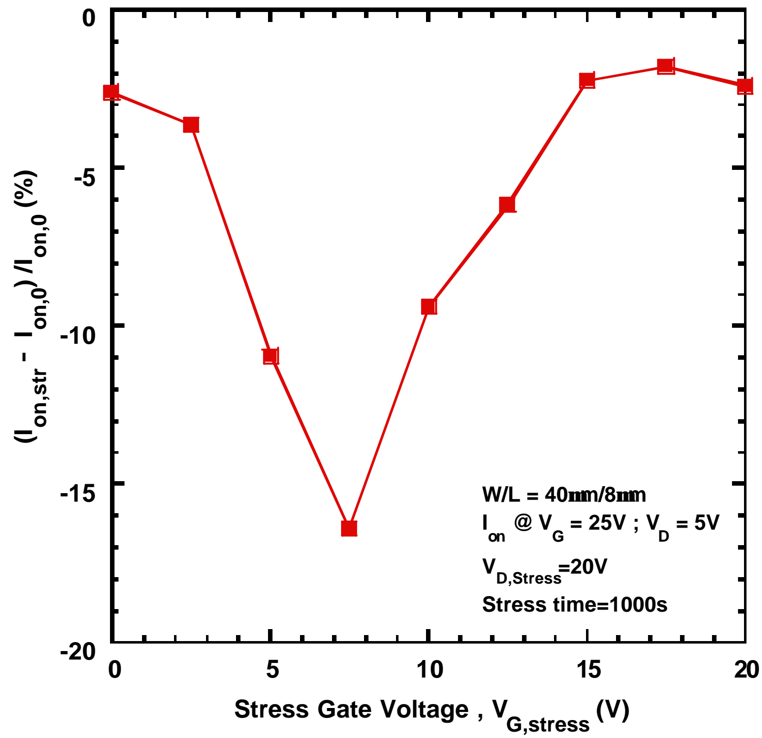

Fig.4-2 Stress gate voltage dependence of TFTs on-current degradation.

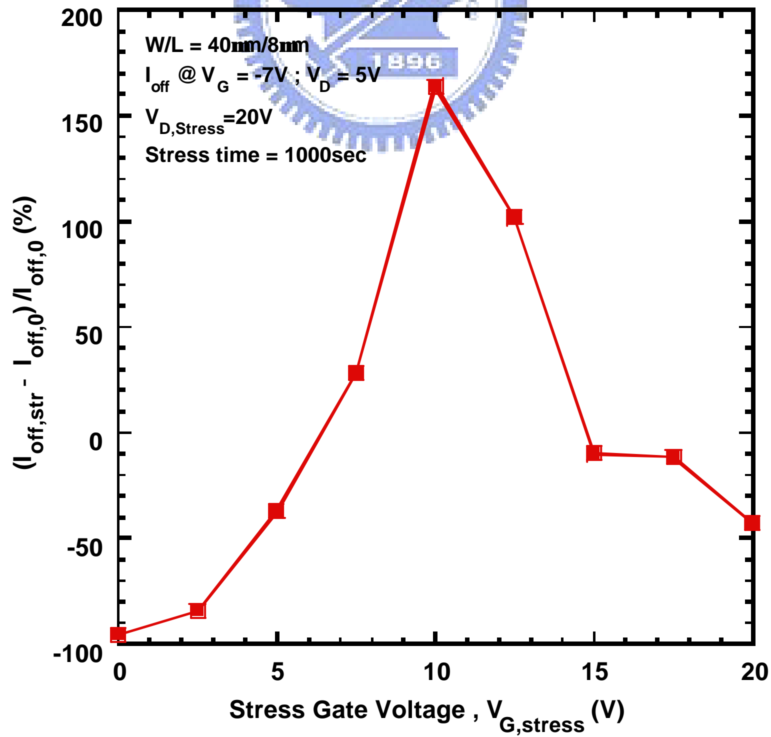

Fig.4-3 Stress gate voltage dependence of TFTs off-current degradation.

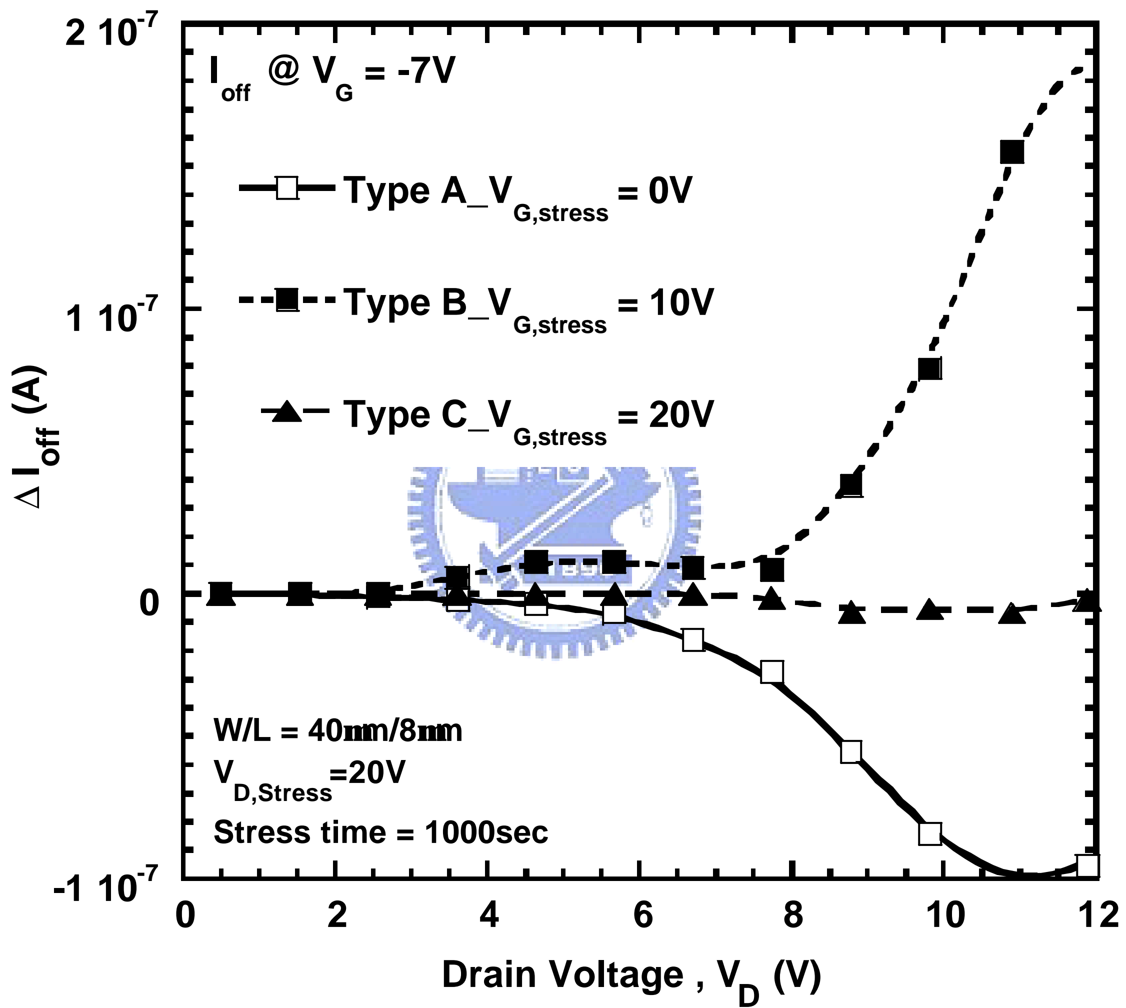

Fig.4-4 Off-current differences versus drain voltage at three types of stress condition, where ? $I_{off} = I_{off,stress} - I_{off,initial}$.

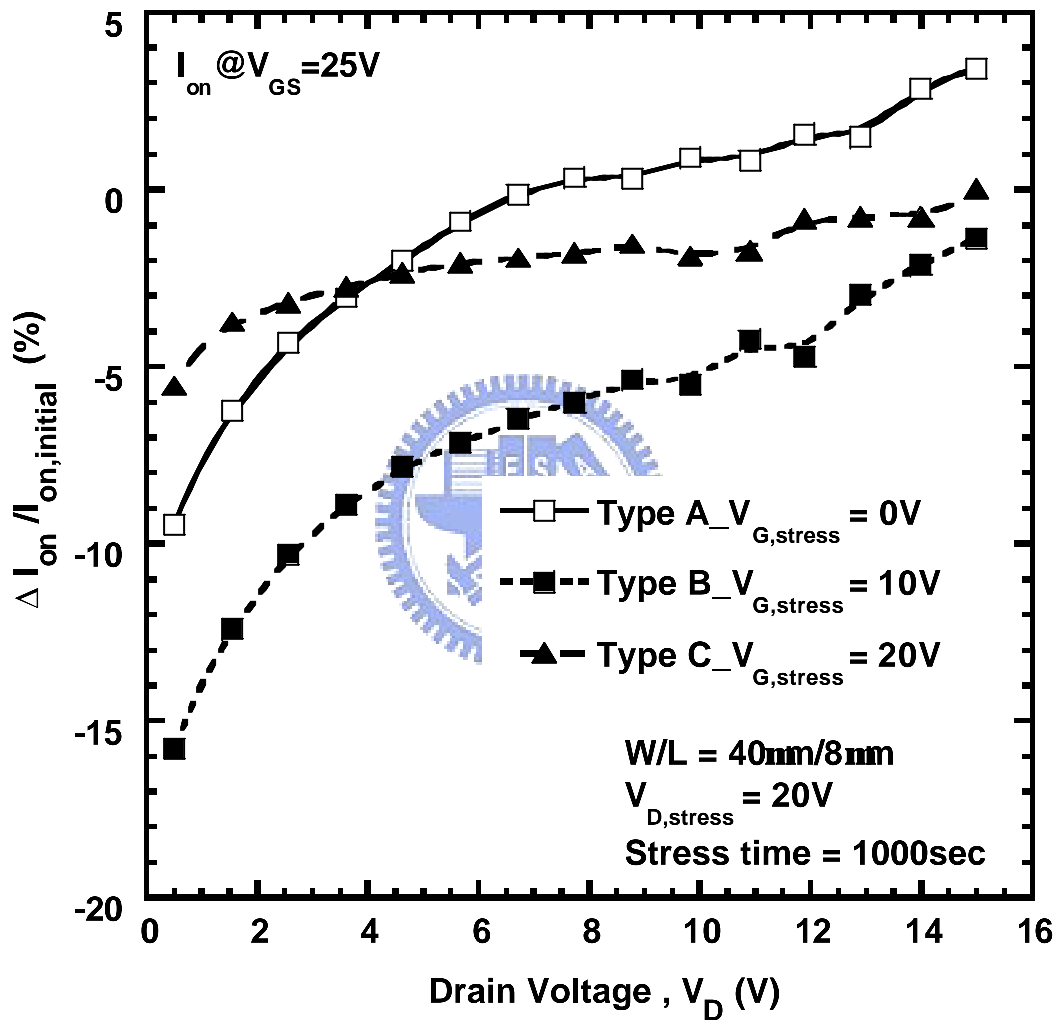

Fig.4-5 On-current differences versus drain voltage at three types of stress condition, where ? $I_{on} = I_{on,stress} - I_{on,initial}$.

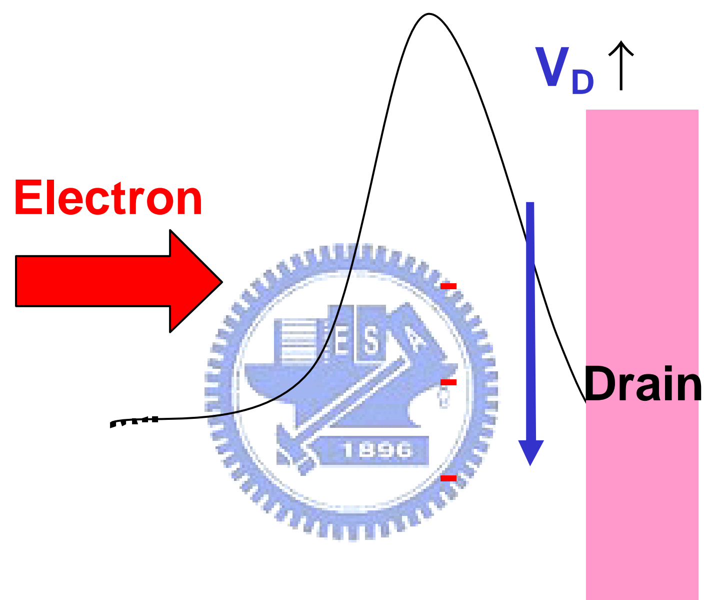

Fig.4-6 Schematic diagram of drain voltage related barrier variation of the trap states near the drain region.

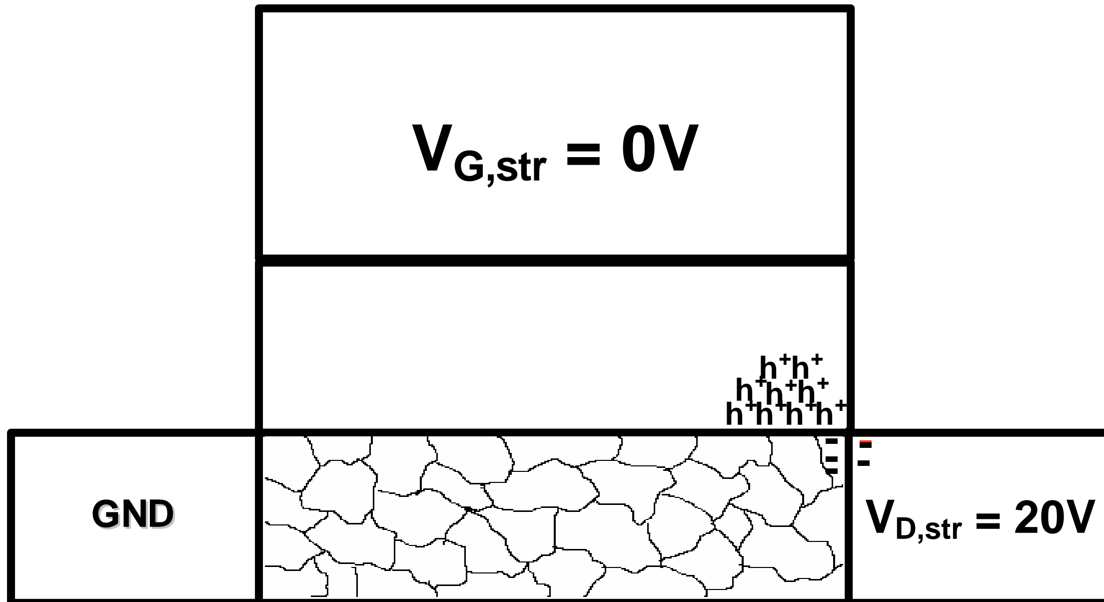

Fig.4-7 Schematic diagram of device cross section of the type-A stress ($V_{G\ stress}$ = 0V, $V_{D,\ stress}$ = 20V).

1896

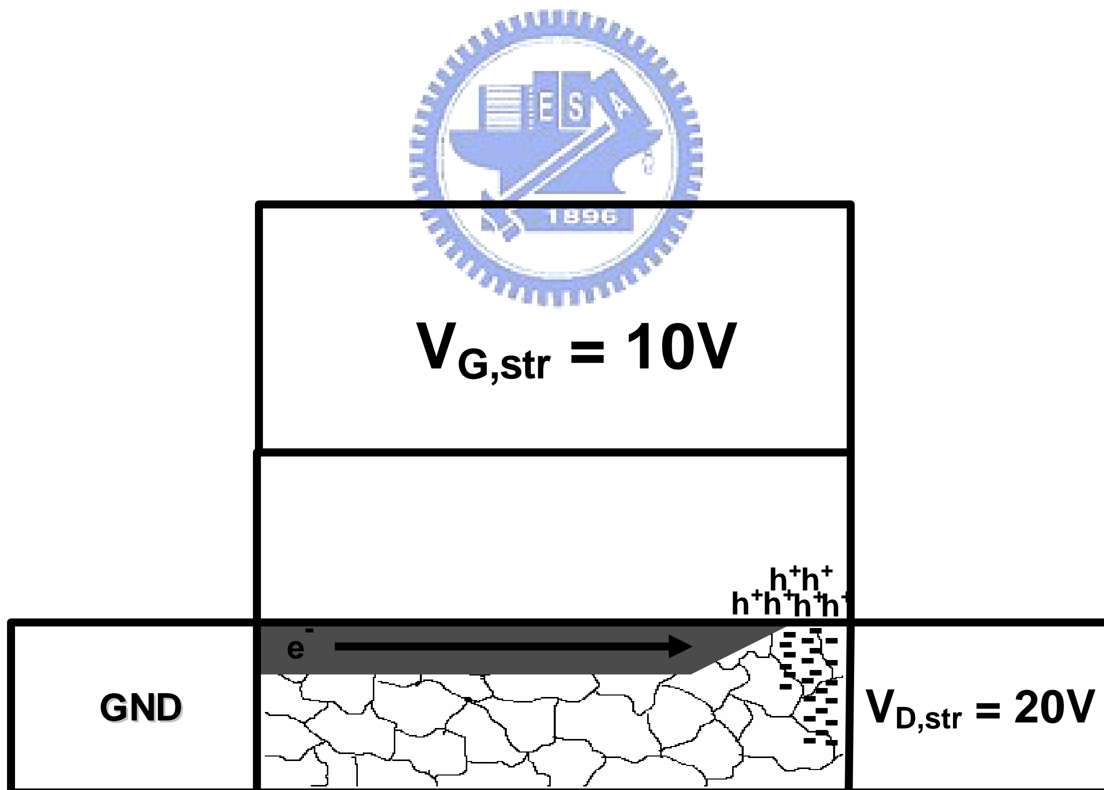

Fig.4-8 Schematic diagram of device cross section of the type-B stress ($V_{G\ stress}$ = 10V, $V_{D,\ stress}$ = 20V).

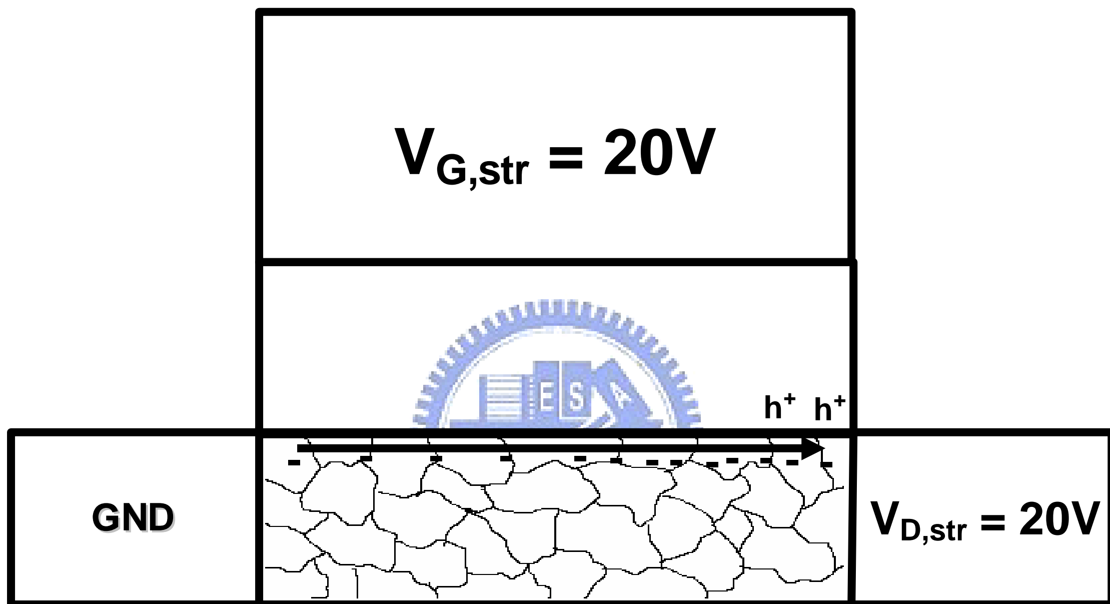

Fig.4-9 Schematic diagram of device cross section of the type-C stress ($V_{G,\ stress}$ = 20V, $V_{D,\ stress}$ = 20V).