# Chapter 1
# Introduction

## 1.1 General Background

The scaling down of active devices is an effective means of achieving two goals: improving circuit performance (mainly by increasing circuit speed) and increasing functional complexity of integrated circuits. However, continuous scaling down of active devices becomes less profitable, as the limitations of circuit speed and maximum functional density become more dependent on the characteristics of the interconnects than on the scaled devices. Figure1-1 shows the intrinsic gate delay versus interconnect RC time delay at minimum design rules of each technology node. The conventional aluminum-based (Al-based) interconnect scheme faces various performance and reliability challenges [1, 2]. Hence, new materials and processing techniques that can meet more rigorous material and process requirements are needed for future application. In recent years, copper (Cu) has been used to replace Al and its alloys as interconnection material in deep submicron integrated circuits because of its lower electrical resistivity and superior electromigration resistance [3-5].

## 1.2 Why Cu-CVD

Copper films can be deposited by various methods, such as sputtering (physical vapor deposition, PVD), electroplating (electrochemical deposition, ECD), and chemical vapor deposition (CVD). Since Cu films cannot be easily etched by dry etching process,

damascene scheme has been developed to fabricate the multilevel Cu interconnect structure. However, with the continuous scaling down of the device dimensions, more delicate gap filling capability, such as filling the high aspect ratio vias and trenches, is bound to be required. The ECD technique, i.e. electroplating, is currently being widely accepted as a primary bulk fill choice for Cu due to its unique bottom-up filling characteristics [1]. However, the gap filling capability of ECD is strongly dependent on the conformality of a PVD Cu seed layer. Thus, extendibility of the current PVD/ECD via filling approach for sub-0.9um technology remains questionable. In addition, the adhesion property of ECD Cu films is another important issue of serious concern. In contrast, the CVD technique inherently possesses an excellent capability of conformal film deposition in high aspect ratio micro-vias [6-20]. Thus, it is anticipated that the chemical vapor deposition of Cu film (CVD of Cu) will be gradually popularized and eventually become the main stream technique in the future due to its superior step coverage deposition.

## 1.3 Thesis Organization

This thesis consists of six chapters. Following the introductory remark in Chapter 1, the low pressure CVD system used for this thesis study is described in Chapter 2. Chapter 3 deals with the characteristics of Cu CVD on different underlayer substrates of TaN and TaSiN. Chapter 4 investigates the effects of substrate pretreatment by Ar- and $H_2$-plasma on the Cu-CVD. In Chapter 5, nucleation of Cu grains on various plasma-treated substrates was explored. Finally, Chapter 6 presents a conclusion for this thesis study along with suggestions for possible future work.

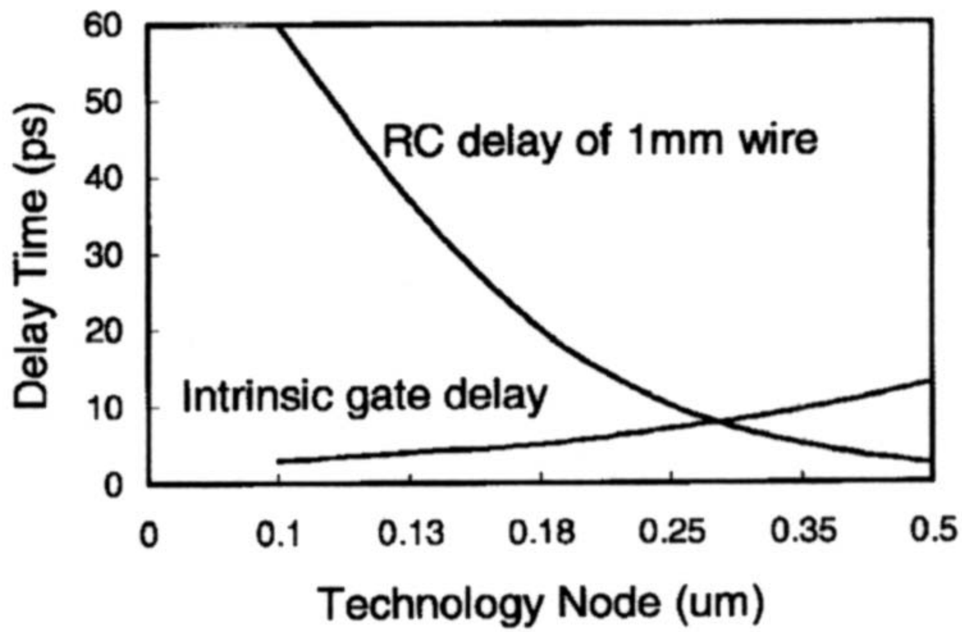


Fig.1-1 Intrinsic gate delay vs. interconnect RC delay at minimum design rules of each technology node.