國 立 交 通 大 學

材 料 科 學 與 工 程 學 系
奈 米 科 技 博 士 班

博 士 論 文

可撓曲軟性電子元件之設計製造與電性分析

Design, Fabrication and Characterization of Soft Electrical Devices on Flexible Substrate

研 究 生：孟杰新　　Jagan Singh Meena

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中 華 民 國 一 百 零 一 年 二 月

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可撓曲軟性電子元件之設計製造與電性分析

研究生：孟杰新　　指導教授：柯富祥

摘要

可撓曲式電子元件技術是目前各科技強國積極發展之領域，經由研究其材料基本特性，有系統地設計與製備可撓式電子產品將影響日常生活型態。本篇研究內容將針對各項可撓曲式電子元件進行探討，其中包括：金屬-絕緣層-金屬 (MIM) 與金屬-絕緣層-半導體 (MIS) 電容以及有機薄膜電晶體 (OTFT) 等。

本篇論文第一部分，我們利用溶膠-凝膠 (sol-gel) 法旋轉塗佈高界電係數材料-HfO_2 於 polyimide (PI) 基板，經由氧電漿 (O_2 plasma) 處理此 sol-gel 薄膜製作膜厚為 10 nm-HfO_2 之 MIM 電容。此方法在低溫 (250 ℃) 製程之薄膜，利用原子力顯微鏡 (AFM) 與掃描式電子顯微鏡 (SEM) 實驗分析，得知此薄膜表面有良好的連續性和均勻性，在 x 射線光電子能譜 (XPS) 分析也指出此薄膜在經過 O_2 plasma 處理後其化學特性與氧化程度有所改變。電性結果顯示此 MIM 電容具有低漏電流與高電容量之特性，且由於元件基板 PI 撓曲性高，經由 100,000 次以上與將近 360° 折疊測試後，此元件仍可保持其電子特性。

第二部分實驗，我們嘗試製作 p-type 之 poly-(3-hexylthiophene) (P3HT) 薄膜電晶體於 PI 基板上，並利用 Si_3N_4-HfO_2 為此電子元件之絕緣層。此薄膜電晶體製程步驟如下：1. 使用簡單、便宜 sol-gel 技術製作膜厚為 10 nm-HfO_2 之介電層於 PI 基板；2. 堆疊 50 nm Si_3N_4 於 HfO_2 之上；3. 旋轉塗佈 30 nm P3HT 薄膜作為 channel layer。此製作過程，由於 Si_4N_4 之作用有效地改善原先 MIM 電容漏電流之情況，在電性量測方面 (如：on-to-off ratio 及 saturation mobility 等)，結果皆顯示其特性良好。此外，針對此電晶體之可撓性，我們也量測元件在不同曲度及折疊後之電性，詳細探討撓曲對元件所造成之影響。

第三部分內容，我們使用聚合物 (EO_{20}-PO_{70}-EO_{20}; P123) 當作表面活性劑備製二氧化鈦 (nc-TiO_2) 薄膜，以旋轉塗佈技術將 P123-TiO_2 旋塗於 PI 基板製作成 MIS 電容結構。經由 XRD、AFM 與 XPS 等分析在 270 ℃ 退火 5 小時後觀察 nc-TiO_2 表面形貌及化學組成等參數，實驗結果顯示薄膜經由 P123 的作用促使其表面結構平坦且均勻度良好，此外我們也針對半導體層 (pentacene) 表面進行探討，利用 AFM 與 XRD 實驗得知其表面為連續平面且均勻度高。在 I-V 特性量測分析方面，此 MIS 元件電性良好，在外加偏壓為 -5 V 時，漏電流密度值為 8.7×10^{-12} A cm^{-2}，在 1 MHz 條件下，電容值為 102.3 pF，且介電常數值為 28.8。另外，針對此電子元件可撓性測試，我們量測元件在不同曲度的電性表現，發現經過 30 天置放後，此元件仍可保持其電子特性。

本論文最後一部分，我們將 P123 與聚苯乙烯 (polystyrene; PS) 兩種聚合物混合後當作製備有機薄膜層之材料 (P123-PS)，AFM 分析得知此薄膜表面均勻度高，且對於大氣水分有良好抵抗能力，利用接觸角量測儀實驗顯示，此平面為疏水表面，且表面自由能約為 7.12 mJ m^{-2}。之後我們嘗試利用此 P123-PS 薄膜製作成 MIM 結構之電子元件於 PI 基板，經由 I-V 特性量測分析結果得知，其漏電流密度值低於 1.07×10^{-11} A cm^{-2}，電容值為 88.2 nF cm^{-2}，而介電常數值為 2.7。此外，我們也利用此薄膜材料 (P123-PS) 當作絕緣層在 PI 基板上製作 OTFT，實驗結果顯示其電性參數值 saturation mobility: 0.16 cm^2 V^{-1} s^{-1}, on-to-off current ratio: 5×10^5，且經過拉伸與壓縮測試，此元件亦維持良好電子特性，表示其可撓性良好。

Design, Fabrication and Characterization of Soft Electrical Devices on Flexible Substrate

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Abstract

Flexible technology is rapidly exploding worldwide and it will revolutionize all aspects of our everyday life, since it will lead to fundamental breakthroughs in the way materials, devices and systems are understood, designed and manufactured. In this thesis, the advances and prospects of nanotechnology in the fields of novel active and functional thin films and nanocomposite-materials to be used for the production of flexible electronic devices, such as flexible metal-insulator-metal (MIM), metal-insulator-semiconductor (MIS) capacitors and organic thin-film transistor (OTFT), will be described.

In first section, we focused on the oxygen (O_2) plasma affected sol-gel spin-coating process to fabricate a new MIM capacitor comprising a 10 nm-thick high-k thin dielectric HfO_2 film on a flexible polyimide (PI) substrate. We observed the as-deposited sol–gel film was completely oxidized when employing O_2 plasma in together annealing at a relatively low temperature (ca. 250 ℃), thereby enhancing the

electrical performance. An O_2 plasma mechanism was proposed to explain the surface oxidation of the HfO_2 sol-gel film. The surface morphology of this HfO_2 film was investigated using atomic force microscopy (AFM) and scanning electron microscopy (SEM), which confirmed that continuous and crack-free film growth had occurred. We employed X-ray photoelectron spectroscopy (XPS) at both high and low resolution to examine the chemical composition of the film subjected to various treatment conditions. The shift of the XPS peaks towards higher binding energy revealed that O_2 plasma treatment was the most effective process for the complete oxidation of hafnium atoms at low temperature. To investigate the insulator properties of the HfO_2 film, we deployed it in sandwiched like cross sectional i.e., MIM structured capacitor, which exhibited a low leakage current density and a maximum capacitance density. The real-life flexibility study of the insulator properties indicated the excellent bendability of our MIM capacitor and the flexible PI substrate could be bent up to 100,000 times and folded to near 360° without any deterioration in its electrical performance.

In second section, we demonstrated a new and fully flexible Si_3N_4-HfO_2 stacked poly-(3-hexylthiophene) p-type OTFT on PI substrate. The success of the TFT manufacturing adopts a very simple and cost-effective sol-gel spin-coating technique to obtain 10-nm high-k HfO_2 as dielectric layer over PI; 50-nm Si_3N_4 as the most efficient passivation layer on top of HfO_2 film; and bendable 30-nm P3HT channel film by spin-coating method. The origin of unsatisfactory leakage current in MIM and TFT structures could be effectively suppressed by means of Si_3N_4 film as the efficient passivation layer. The bottom-gate TFT demonstrated the on-to-off ratio 2×10^4 for drain current and good saturation mobility (0.041 $cm^2\ V^{-1}s^{-1}$). The proposed devices were examined in convex and concave types of various radii of curvature (R_c) in order to explore the manufacturing feasibility and electrical reliability of the flexible TFT

for practical applications. Additionally, various folding times and environmental stability on aforementioned devices with respective to electrical performances were also evaluated.

In third section, we have synthesized triblock copolymer surfactant, EO_{20}-PO_{70}-EO_{20} (i.e. P123)-based nanocrystalline (nc)-TiO_2 thin film on organic flexible PI sheet for their application in organic MIS device. The nc-TiO_2 film over PI was successfully deposited for the first time by a systematic solution proceeds dip-coating method and by the assistance of triblock copolymer surfactant. The effect of annealing temperature (270 ℃, 5 h) on the texture, morphology and time-induced hydrophilicity was studied by XRD, AFM, and XPS, respectively, to examine the chemical composition of the film and the contact angle. The semiconductor-dielectric interface of pentacene and nc-TiO_2 films was characterized by current-voltage and capacitance-voltage measurements. This interface measurement in cross-link MIS structured device yielded a low leakage current density of 8.7×10^{-12} A cm^{-2} at -5 V, maximum capacitance of 102.3 pF at 1 MHz and estimated dielectric constant value of 28.8.

In last section, an organic–organic blend thin–film has been synthesized by solution deposition of triblock copolymer (Pluronic P123, EO_{20}-PO_{70}-EO_{20}) and polystyrene (PS), hereafter named P123-PS for blend film. AFM result revealed that the optimized blend P123–PS film was uniform, crack-free, and highly resistant to moisture absorption. Time-induced contact angle measurements for P123–PS surface was also evaluated by using contact angle meter, which showed excellent hydrophobic surface with surface free energy to about 7.12 mJ m^{-2}. The dielectric properties of P123–PS were characterized in cross linked MIM structured device over PI substrate showed a low leakage current density of 1.07×10^{-11} A cm^{-2}, large capacitance of 88.2 nF cm^{-2} and dielectric constant of 2.7. In addition, we demonstrate

OTFT device on flexible PI substrate by using P123–PS as insulator layer and pentacene as channel layer. The OTFT showed good saturation mobility (0.16 $cm^2 V^{-1} s^{-1}$) and on-to-off current ratio of 5×10^5. The OTFT should functions under bending condition; the flexibility tests for two types of bending modes (tensile and compressive) were also performed successfully.

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List of Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
AMOLED	Active Matrix Organic Light Emitting Display
ASTM	American Society for Testing and Materials
BE	Binding Energy
CA	Contact Angle
DSSC	Dye-Sensitized Solar Cell
ESCA	Electron Spectroscopy for Chemical analysis
eV	Electron Volt
GIDL	Gate Induced Drain Leakage
GIXRD	Grazing Incident X-ray Diffraction
HfO_2	Hafnium-Oxide
ITO	Indium Tin Oxide
ITRS	International Technology Roadmap for Semiconductors
LAE	Large Area Electronics
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Semiconductor
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
nc	Nanocrystalline
OTFT	Organic Thin-Film Transistor
OPT/A	Oxygen Plasma Treatment then Annealing
P123-PS	Pluronic P123-Polystyrene
Pa	Pascal
PI	Polyimide
PDMS	Poly dimethylsiloxane
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PEN	Poly-ether-sulfone

PET	Polyethylene terephthalate
PVD	Physical Vapor Deposition
RAM	Random Access Memory
RF	Radio Frequency
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
TiO_2	Titanium-Oxide
ULSI	Ultra Large Scale Integrated
XRD	X-ray Diffraction
XPS	X-ray Photoelectron Spectroscopy

Chapter 1: Overview

1.1 Background

In recent years nanotechnology has become one of the most important and exciting forefront field in physics, chemistry, engineering and biology which the characteristic dimensions are below c.a. 1000 nm. It shows great promise for providing us in near future with many breakthroughs that will change the direction of technological advances in a wide range of applications. Advances in materials and processing techniques for silicon electronics continue to derive improvements in the speed and performance of a wide range of devices for consumer electronics. More recent research efforts seek to develop unconventional materials and processing techniques for completely new type of electronics systems. This class of circuitry will be important (at least initially) not because of its potential for high speed, density etc., but because it can be mechanically flexible, lightweight, durable and easy to manufacture over large areas. The use of plastic-based substrates coupled with recent developments in solution deposition and injects printing for laying down organic light emitting polymers and active matrix TFT arrays opens up the possibility of cost effective processing in high volumes by use of roll-to-roll processing. That complement the types of systems that conventional electronics supports well (microprocessors, high-density RAM etc.). This field is new (i.e., there are no entrenched technologies) and it has a strong materials content.

The rapid increase in the power of computers described by Moore's Law has relied essentially on the down-scaling of the planar MOSFET. The smallest dimension in this structure is the thickness of the gate dielectric. In the past, the dielectric of choice was SiO_2 but the scaling requirements described in the ITRS require the

thickness of the SiO_2 to go well below 1 nm. At this level, the leakage current due to tunneling rises unacceptably and atomic limitations come into play, as discussed by Muller et al. Since the gate capacitance is a key parameter, one approach to overcoming such problems is to use a dielectric with a higher permittivity, so that the same gate capacitance is achieved with a higher physical thickness is equally important. Moreover, silicon and silicon-based components require millions of gallons of water and temperatures of 500-800 ℃ to manufacture. Polymers are lighter and can cost much less to manufacture, although cost comparisons vary as well as create components at atmospheric pressure, and at temperatures of no more than 150 ℃ than silicon. As a result, there are considerable opportunities for innovation and basic scientific research into new types of electronics materials and methods for patterning them into large-area and low-cost circuits.

The semiconductor industry uses hundreds of thousands of gallons of highly toxic solvents annually. The technologies being developed for flexible electronic devices to enable this all revolve around these building devices using eco-friendly materials and processing techniques. A piece of silicon for a fingerprint recognition device, that one-square-centimeter piece of highly purified silicon; which is quite large in terms of ultrapure silicon usage will be very expensive. And, the promise with organics is related to the lower cost of the raw materials, in particular the substrate on which the device is built a silicon wafer is more expensive than a sheet of plastic. Recently, in terms of their superior bending, it was found that flexible organic transistors can perform better than flexible inorganic transistors. The bending and stretching properties of flexible devices designed for bio-medical applications such as accurate sensors for hydrogen or for integration into artificial muscles or biological tissues.

1.2 Motivation and Purpose of the Thesis

This thesis focuses on the requirements and achievements to date on the topic of flexible transparent conductors, where high transparency and high conductivity are required. Worldwide research and design efforts are presented, both from research institutes and companies that are developing the necessary materials and processes. Several technical solutions available are compared, and forecasts are given for the next 10 years. The importance of TCF increasingly more and more flexible devices are required, from flexible displays for e-readers, OLEDs and other types to flexible photovoltaics and beyond. These devices require a conductor to close the layers of active materials, but that conductor needs to be transparent in applications such as displays and photovoltaics to allow light through. Today, transparent conductive oxides are widely used for rigid devices but these will become more expensive due to rare materials used, and are inadequate for most flexible electronics applications where they can easily crack under little strain. Alternatives are sought.

The goal of this project was to investigate the layers and the interfaces by selected high-k and low-k polymer dielectrics in device applications with the aim of improving the basic understanding of the outcomes of the deposition and processing methods. Although the technology of such films was developed to an extent, some fundamental problems remain unclear and only their solution can result in wide-scale commercialization of high-k films with very low thickness, especially as the efficient current leakage for portable flexible devices. The most critical problem is the development of efficient processing techniques, which would provide the long-term (for several thousand hours) operation of flexible devices without sacrificing their characteristics.

The principal techniques used were those of sol-gel spins coatings and dip-coating of these techniques were integral to the work of the project. The composite high-k materials of interest were also prepared by sol-gel techniques in order to gain more insight into the materials themselves. For the first time, we developed the process to deposit low-k film on flexible PI substrate via surface dip-coating solution process. We developed a low-temperature O_2 plasma–enhanced technique for preparing HfO_2 thin film–based MIM capacitors as well as a flexible Si_3N_4–HfO_2 stacked poly–(3–hexylthiophene i.e., P3HT) p-type TFT on PI substrate using surface sol-gel techniques. We also investigated the O_2 plasma oxidation growth mechanism in different kinetic regimes to understand the surface oxidation process. The insulator properties of the films were determined; which showed low leakage currents and good capacitances. A bending test revealed that the capacitors on the PI surface showed very stable performance after bending up to 100,000 times, minimum up to 1 or 2 cm radii of curvature for both convex and concave type settings even after period of time about one month. The device's electrical properties with respect to saturation mobility, on/off current ratio, and bending conditions (i.e., the number of bends and the bending radii) are also investigated to use for many practical applications. As detailed above, international sematech withdrew part way through the project. The particular systems to be studied and the areas to be concentrated on were specified and modified in the light of developments in the field by discussion at regular project meetings with these partners.

Further, we demonstrate an innovative and easy-to-follow synthesis approach for deposit a new polymer blend film on organic flexible polyimide substrate by a dip-coating technique at low temperature (c.a. 100 ℃). This method is the most desirable to open up the way of preventing the problem of pin-hole defects in pure thin (<100 nm) polystyrene film. We have used dip-coating process to deposit

nanocrystalline-TiO_2 film for their application in electronic devices at processing low temperature (~ 200 ℃). It should be emphasize that this novel synthesis dip-coating method provides a new way to investigate the surface of polymeric blend films (< 50 nm) and could be a promising approach for practical applications since it is a low-cost and low-temperature manufacturing technique. Moreover, the results of this research support the idea of sustainable and environment friendly as useful for flexible electronics technology. Their detailed knowledge of developments and thinking in the field of flexible electronics were central object in ensuring that the key areas requiring the development of fundamental understanding are pursued.

1.3 Thesis Organization

The remainder of this thesis consists of eight chapters and is organized as follows: In chapter 3, we have given a detailed description of the experimental methods and procedures used in this study, and the materials and chemical chosen to accomplish this research work. Chapter 4 described a low-temperature O_2 plasma-enhanced method for preparing HfO_2 thin film-based MIM capacitor fabricated on a flexible organic PI substrate using sol–gel spin processing. To determine the insulator properties of the film, we determined their current density-electric field and capacitance-voltage characteristics. We also investigated the O_2 plasma oxidation growth mechanism in different kinetic regimes to understand the surface oxidation process. Moreover, XPS suggested the feasibility of using this low-temperature processing approach toward achieving high-performance flexible devices. A test revealed that the capacitor on the PI surface performed reliably after bending up to 100,000 times. In chapter 5, we have explained about the use of Si_3N_4 as passivation layer over HfO_2 film, enable one to obtain reliable OTFT on a fully

flexible PI substrate, as regards to passivate the surface traps and considerably improve the electrical properties and mechanical flexibility and environmental stability. The device's electrical properties with respect to saturation mobility, on/off current ratio, and bending conditions (i.e., the numbers of bending times and the bending radii) are also carefully investigated in OTFT. They have attracted much attention because it provides strong, yet good dielectric properties against surfaces of varying roughness and orientation. In chapter 6, we developed a new and facile dip-coating solution process to fabricate the organic MIS device over flexible PI substrate. In order to reduce the cost and simplify the procedure, we studied the nc-TiO_2 film as gate dielectric and pentacene as organic semiconductor layer for extending the MIS capacitor. For the practical application in real-life, we tested flexible tests in various bending conditions. In chapter 7, we present an easy-to-follow synthesis procedure to prepare new organic-organic P123-PS blend thin film as dielectric layer at low temperature. This method is provided the way of preventing the problem of pin-hole defects in pure ultrathin polystyrene film. The electrical properties of the P123-PS blend thin-film have been examined for advanced flexible MIM capacitor and OTFT applications. These new polymer blend dielectric materials have good stability when using in electronic device as composite dielectric layer, and gives excellent results compared to other polymer dielectric materials.

Finally in chapter 8, we concluded the experimental results and discussion; plus, some future works are also involved. Moreover, we have described thesis organization in a schematic way using a flowchart as depicted in Figure 1.1.

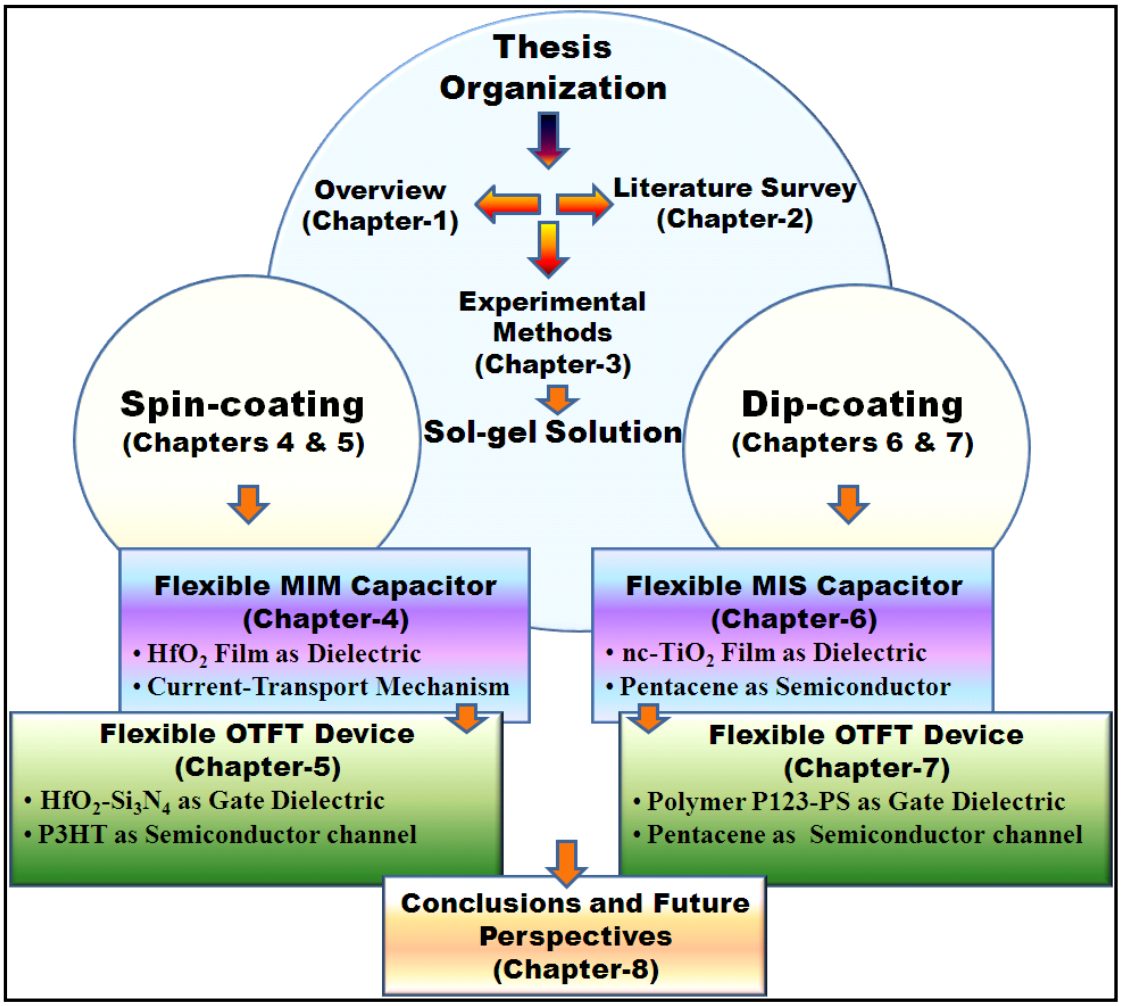


Figure 1.1 Schematic representation of thesis organization showing eight chapters sequencly.

Chapter 2: Literature Survey

2.1 Flexible Substrates

2.1.1 Flexible Electronic Devices

Flexible electronics promises with the route to the development of displays that are thin, light, robust, conformable, and can, if required, be rolled away when not in use. This area of new technology first began to emerge, the substrate on which the eletcronic structures were being applied was not regarded as very important. This may have been acceptable for demonstrating the potential of the technology, but as this technology has moved to closer to prototype device and commercial production processes it has become clear that to make flexible technology to viable, choice of substrates with the required set of properties is essential. The requirements for the different applications are very different and will require substrates with different sets of properties. In the context of the set of properties required for flexibe organic circuitry, PET e.g. DuPont

Teijin Films Melinex®, PEN e.g. DuPont Teijin Films Teonex®, polyester film, are biaxially oriented semicrystalline films. The success of polyester films in general applications is because of the properties include high glass transition temperature (T_g), high mechanical strength, good resistance to a wide range of chemicals and solvents, excellent dielectric properties, good dimensional stability, and good thermal resistance in terms of shrinkage and degradation of the polymer chains. It is also intresting to contrast these films with the other films being considered for flexible electronics

especially for the higher performance flexible display market. The main candidates are shown in Figure 2.1 which lists the substrates on the basis of increasing T_g [**1, 2**]. The surface smoothness and cleanliness of the flexible substrates are both essential to ensure the integrity of subsequent layers such as conductive coatings, TFT arrays, or barrier coatings, these properties could be considered separately.

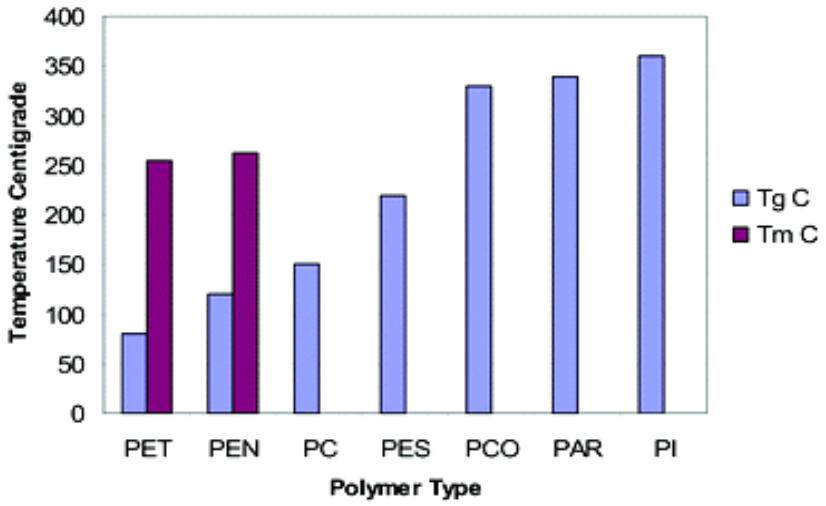


Figure 2.1 The comparison of plastic substrates by T_g of interest for applications in flexible electronics. [Cited from ref. **2**]

For applications where a transparent flexible substrate is required, a plastic film is necessary. In choosing an appropriate plastic film, it is useful to categorize the available options of T_g as this sets the scale for the accessible processing temperatures and time [**3-5**]. Particularly, polyimide (sometimes abbreviated as PI) is a polymer of imide monomers. The molecular structure of imide is as shown in Figure 2.2 (a). PI is often used in the electronics industry for flexible cables and as an insulating film on magnet wire. For example, in a laptop computer, the cable that connects the main logic board to the display (which must flex every time the laptop is opened or closed) is often a PI base with copper conductors. The semiconductor industry uses PI as a high-temperature adhesive. Photograph of PI film shown in Figure 2.2 (b); have

inherent advantage over the other plastic films being more thermaly stabile, good chemical resistance, and for their excellent mechanical properties. PI films compounded with graphite or glass fiber reinforements have flexural strengths of up to

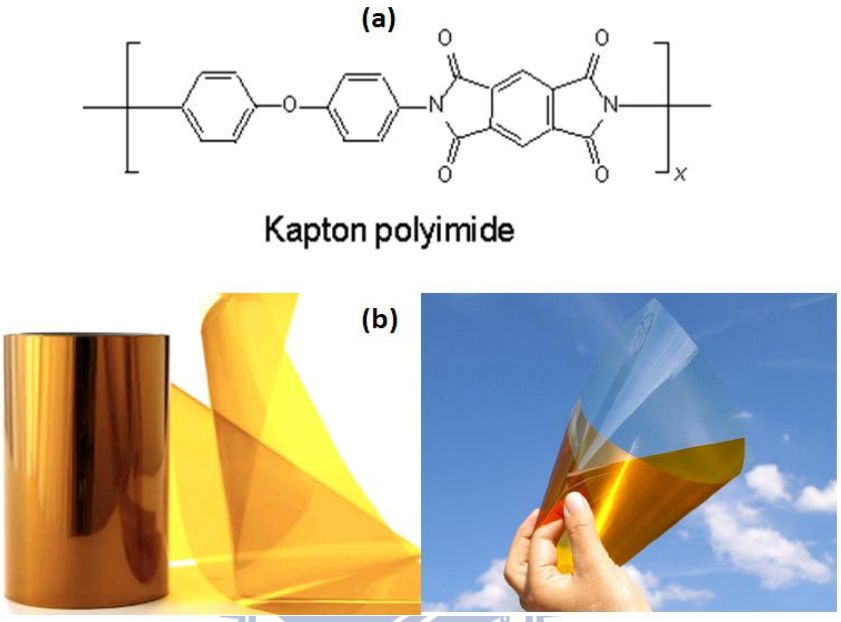


Figure 2.2 (a) Molecular structure of polyimide Kapton® and (b) Typically Kapton® films of amber-color near-transparent for applications in flexible electronics [Cited from http://www.kaptontapeonline.com/catalog/product_info.php?products_id=55].

50,000 p.s.i. and flexural moduli of 3 million p.s.i. The low coefficient of thermal expansion, high T_g and low shrinkage of Kapton PI films help minimize stress at the interface with other materials of construction, both during processing and during end use in temperature extremes. The thermal stability of PI Kapton films is excellent and allows processing temperature in excess of 400 ℃. Table 2-1 revealed the typical properties, those were tested at high temperatures representative of actual procesisng conditions [**6**].

Typical Properties	DuPont Kapton® Polyimide Film
Density	1430 kg/m^3
Young's Modulus	3200 MPa
Tensile Strength	75-90 MPa
Elongation@ break	4-8%
Notch test	4-8 kJ/M
Glass Transition Temperature (T_g)	~ 400 °C
Heat Transfer Coefficient	0.52 W/m.K
Dielectric Constant	3.5 at 1MHz
Water Absorption	0.32

Table 2-1 List of typical properties of DuPont Kapton® polyimide film. [Data taken from http://en.wikipedia.org/wiki/Polyimide]

DuPont is putting science to work to accelerate the development of additional Kaptopm PI films for the flexible and thin-film PV industry (Figure 2.3). Reinforced PIs with higher tempertaure processing capability abd dimensional stability are expected to provide increased efficiency in CIGS PV applications, while maintaining the desirable properties of polymeric substrate. Flexible, insulating, nonorganic approaches are also being developed for even higher temperature processing capability for monolithic CIGS thin-film PV. DuPont has additional capabilities which may be suitable for PV technology developments in the future, including: Near-transparent films for superstrate PV configurations such as DSSC, Organic PV and CdTe. Casting or laminating PI onto a range of metal, including copper, stainless steel, aluminum and titanium.

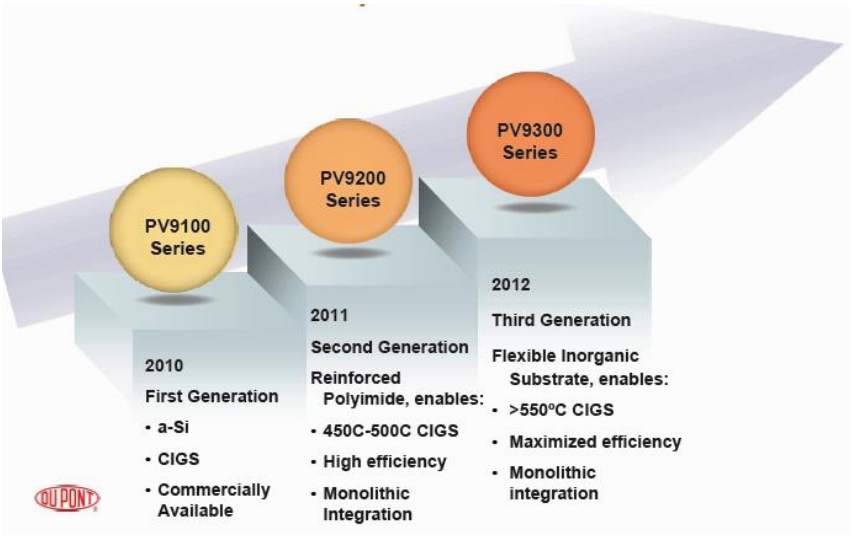


Figure 2.3 Technology Roadmap: DuPont Kapton® PI films for flexible and thin-film photovoltaic substrates. [Cited from http://www2. dupont.com/Kapton/en_ US/ assets/ downloads/pdf/Kapton_for_PV.pdf]

2.1.2 Highly Reliable and Mechanically Stable

Trends from past decade, researchers have dreamed of building electronic circuits that would bend and stretch, rather than being confined to rigid chips and boards. Flexible circuitry would be able to do many things that rigid circuits cannot and an essential prerequisite for the development of rollable displays, conformable sensors, biodegradable electronics and other applications with unconventional form factors. Stretchable electronic skin could connect an artificial hand to the nervous system[**7, 8**].

The ultimate goal is electronic systems that cannot only be flexed (into a bending radius of a few centimetres or perhaps a few millimetres), but can also be tightly rolled, bent around sharp edges or repeatedly creased without degradation of the electronic functionality. This requires the development of devices that can withstand extremely small bending radii without suffering damage. Flexible OTFTs demonstrated reliable device performance, even under the bending mode as depicted

in Figure 2.4 (a). Figure 2.4 (b) shows the bent test for one TFT device at a radius of curvature 20 mm.

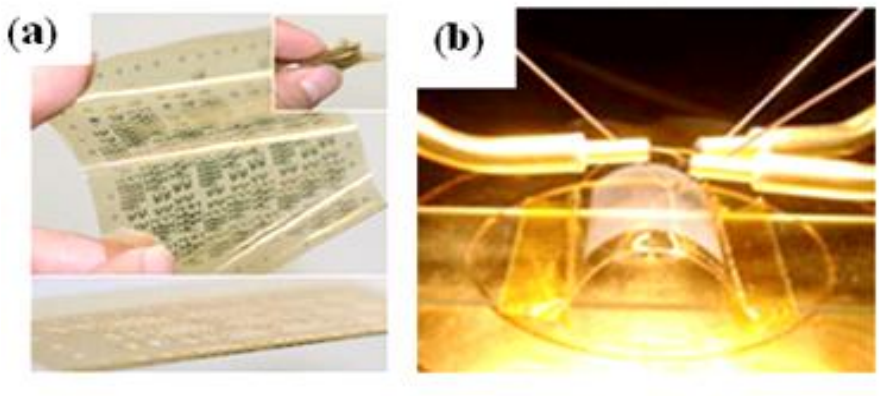


Figure 2.4 (a) Photographs of a polyimide substrate with functional organic TFTs bending mode and (b) The device was bent at a radius of curvature 20 mm. [Cited from ref. **9**]

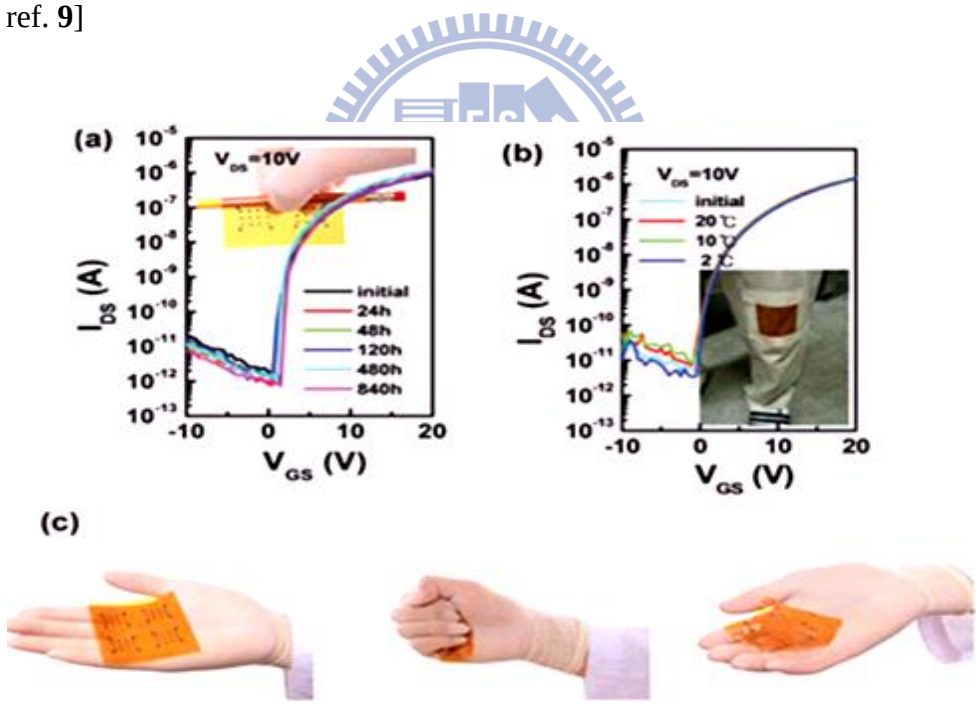


Figure 2.5 Electrical characteristics and flexibility tests of the ZnO-TFTs without passivation to various bending conditions; (a) Variations in the transfer charateristics over a long bending period (wrapped around a pencil). Even though stressed for approximately a month, no electrical parameters changed, (b) One array of 48 TFTs on a flexible large-area substrate was virtually characterized for wearable applications

under different temperatures and humidities, (c) Demonstration of the foldable test. Flexible arrays were repeatedly crumpled in the palm of the hand. [Cited from ref. **10**] It was pointed out that the device performance was almost completely unaffected by bending the device minimum down up to 20 mm [**9**]. Figure 2.5 (a) shows the long term performance stability if the device is wrapped around a pencil (diameter of 10 mm) at room temperature in air. There was no noticeable degradation over a month. We also investigated the performance of an array of flexible TFTs on a large-area substrate under simulated wearable conditions. As shown in the Figure 2.5 (b) inset, the sample was attached to the knee joint, the most active part of the body. The person wearing the device walked for 4 h on days with different ambient temperatures of 2 ℃, 10 ℃, and 20 ℃. The devices without passivation were surprisingly stable, although the off current slightly varied compared to its initial value. They performed a folding test as shown in Figure 2.5 (c). To observe the foldable behavior of flexible FETs, they fabricated a flexible array containing 48 TFTs [**10**].

2.1.3 Adding Features to Applications

As you design and develop your applications, you should consider how your decisions can affect your ability to deploy updates to your applications. Based on the same principles of how a cornstarch solution hardens on impact, Singapore researchers have invented a new flexible, lightweight, impact-resistant composite material (Figure 2.6). Then here's military applications, where flexible electronics could enable soldiers to shed as much as 20 lbs of equipment, with GPS, threat detection, and health monitoring systems built into their clothes. The technology can be applied to a number of areas, including body armour, sports protective equipment, surgical garments, and even aerospace energy absorbent materials [**11**].

Figure 2.6 The Paper flexible electronics: The soldiers to shed as much as 20 lbs of equipment. [Cited from ref. **11**]

One of the first major commercial applications of flexible displays will be in handheld mobile devices. The flexible displays that arrive on the market will be limited in size for technical reasons. And, many of the benefits of flexible displays, such as portability, are ideally suited for mobile form factors. Mobile devices benefit most from the power efficiency of electrophoretic displays in Figure 2.7 (a). For these reasons, PaperPhone, a smartphone prototype designed around a 3.7 electrophoretic display are developed [**12**]. A flexible smartphone; the Nokia 888 currently is a concept, and we have to wait till the phone enters the market as viewed in Figure 2.7 (b). The Nokia 888 basically has superb flexible form factor and is a feather-weight light communication device [**13**]. Yet, you're not going to see this phone in stores any time soon. But if you'd like to get an idea of what Nokia thinks the future.

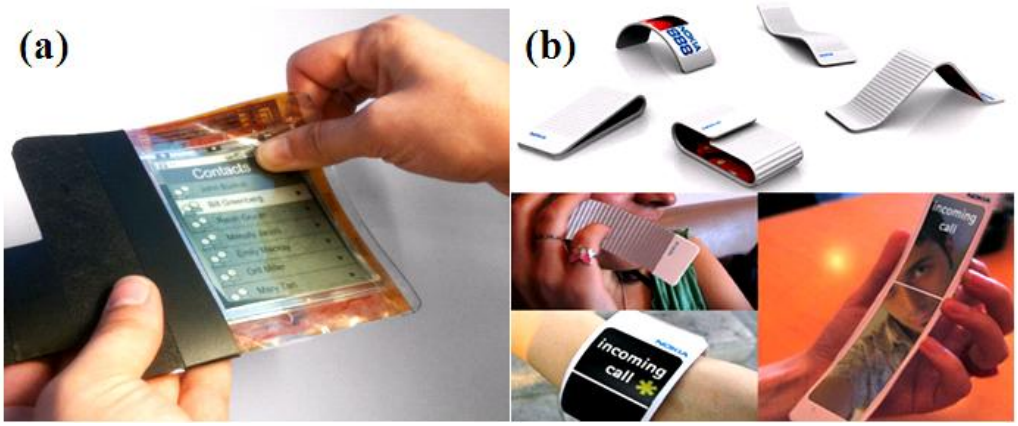


Figure 2.7 (a) The Paper Phone prototype with flexible E-Ink display features bends gesture input recognition, (b) The Nokia 888 concept phone. [Cited from ref. **12**]

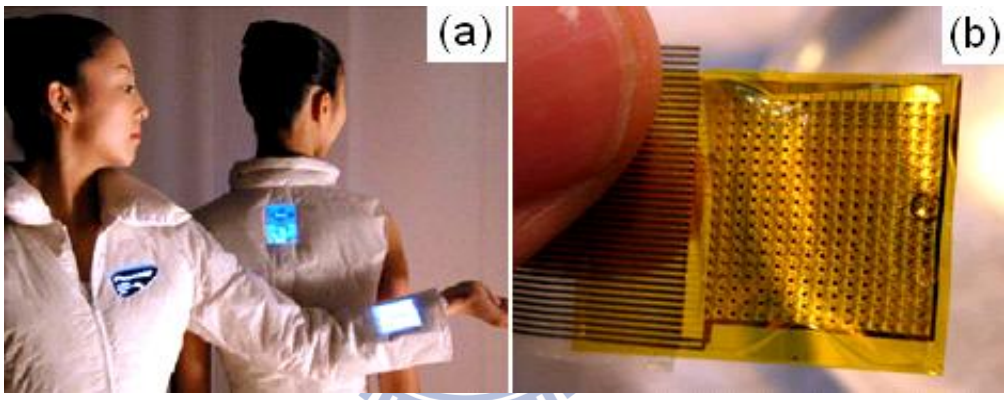


Figure 2.8 (a) Integrates electronic devices into textiles, like clothing and (b) Flexible heart sensor array. [Cited from ref. **13**]

Moreover, these flexible structures could find useful applications as sensors and as electronic devices that can be integrated into artificial muscles or biological tissues. In addition to a biomedical impact, flexible electronics are important for energy technology as flexible and accurate sensors for hydrogen [**14**]. Communication devices may be integrated into textiles, like clothing as shown in Figure 2.8(a). Flexible electronics could help put off-beat hearts back on rhythm. Rogers and his team have built a flexible sensor array, shown in Figure 2.8 (b); that can wrap around the heart to map large areas of tissue at once. The array contains 2,016 silicon

nanomembrane transistors, each monitoring electricity coursing through a beating heart [**15**].

2.2 High-k Gate Dielectrics

The term high-k dielectric refers to a material with a high dielectric constant (as compared to SiO_2) used in semiconductor manufacturing processes which replaces the SiO_2 gate dielectric (Figure 2.9). The implementation of high-k gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law [**16, 17**]. SiO_2 has been used as a gate oxide material for decades. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current and device performance.

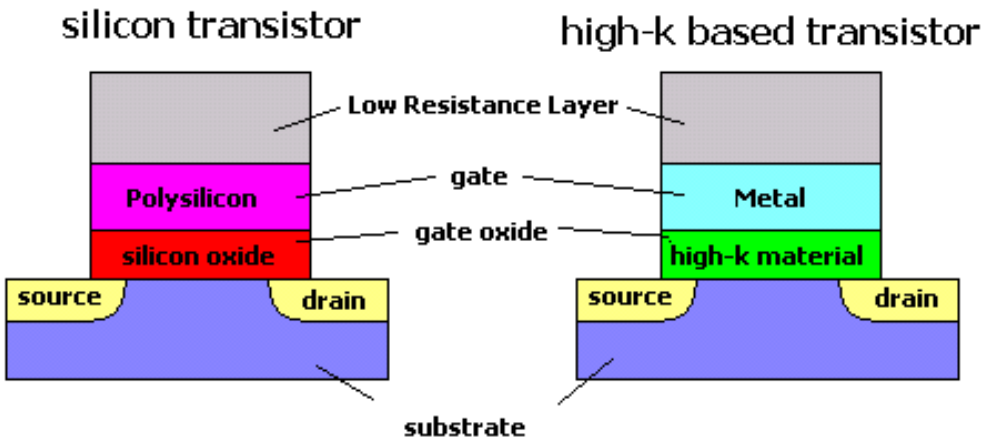


Figure 2.9 High-k used in semiconductor manufacturing processes which replaces the SiO_2 gate dielectric. [Cited from ref. **19**]

As the thickness scales below 2 nm [**18**], leakage currents due to tunneling increase drastically, leading to unwieldy power consumption and reduced device reliability. Replacing the SiO_2 gate dielectric with a high-k material allows increased

gate capacitance without the concomitant leakage effects. As a consequence, development efforts have focused on finding a material with a requisitely high dielectric constant that can be easily integrated into a manufacturing process. Materials which have received considerable attention are hafnium and zirconium oxides and silicates. It is expected that defect states in the high-k dielectric can influence its electrical properties [**19**]. Defect states can be measured for example by using zero-bias thermally stimulated current, zero-temperature-gradient zero-bias thermally stimulated current spectroscopy[**20**], or Inelastic electron tunneling spectroscopy (IETS). In early 2007, Intel announced the deployment of hafnium-based high-k dielectrics in conjunction with a metallic gate for components built on 45 nm technologies, expected to ship in 2007 [**21**]. At the same time, IBM announced plans to transition to high-k materials, also hafnium-based, for some products in 2008. While not identified, it is most likely the dielectrics used by these companies are some form of HfSiON, HfO_2 and HfSiO are susceptible to crystallization during dopant activation annealing [**22**]. However, even HfSiON and HfO_2 is susceptible to trap-related leakage currents, which tend to increase with stress over device lifetime. There is no absolute guarantee that hafnium will be the basis of future high-k dielectrics. The 2006 ITRS roadmap predicts the implementation of high-k materials to be commonplace in the industry by 2010.

2.3 Low-k Gate Dielectrics

With the development of ultra large-scale integrated circuits, the feature sizes of integrated circuits have decreased to about 180 nm or even smaller.1–3 Consequently, reduction in the electrical resistance induced by interaction between interconnect lines, time delay caused by wire capacitance, crosstalk and power

dissipation have become bottleneck problems limiting the progress of high-speed, low power cost and multi-functional integrated circuits. In semiconductor manufacturing, a low dielectric constant (low-k) dielectric is a material with a small dielectric constant relative to silicon dioxide. Although the proper symbol for the dielectric constant is the Greek letter κ (kappa), in conversation such materials are referred to as being "low-k" (low-kay) rather than "low-κ" (low-kappa). Low-κ dielectric material implementation is one of several strategies used to allow continued scaling of microelectronic devices, colloquially referred to as extending Moore's law. In digital circuits, insulating dielectrics separate the conducting parts (wire interconnects and transistors) from one another [**23**]. As components have scaled and transistors have got closer together, the insulating dielectrics have thinned to the point where charge builds up and cross-talk adversely affects the performance of the device. Replacing the silicon dioxide with a low-κ dielectric of the same thickness reduces parasitic capacitance, enabling faster switching speeds and lower heat dissipation. Apart from the above, low-k materials have been considered to decrease lower cross-talk noise, power dissipation, and, when incorporated in device systems, can dramatically decrease resistance–capacitance (R–C) delays.

2.4 Oxygen-Plasma Surface Treatment

Plasma is a low temperature glow discharge or a low pressure partially ionized gas consisting of large concentrations of excited atomic, molecular ionic and free radical species. Plasmas are collections of highly excited atomic, molecular, ionic, and radical species, the bulk of which remain at room temperature. Each of these components has the potential of interaction with surfaces upon which they come in contact [**24**]. Plasmas can be employed to modify surface properties of a material without affecting the general characteristics of the base material. Excitation of the gas

molecules is accomplished by subjecting the gas, which is enclosed in a vacuum chamber, to an electric field, typically at radio frequency (RF). Free electrons gain energy from the imposed RF electric field, colliding with neutral gas molecules and transferring energy dissociating the molecules to form numerous reactive species. It is the interaction of these excited species with solid surfaces placed in the plasma which results in the chemical and physical modification of the material surface.

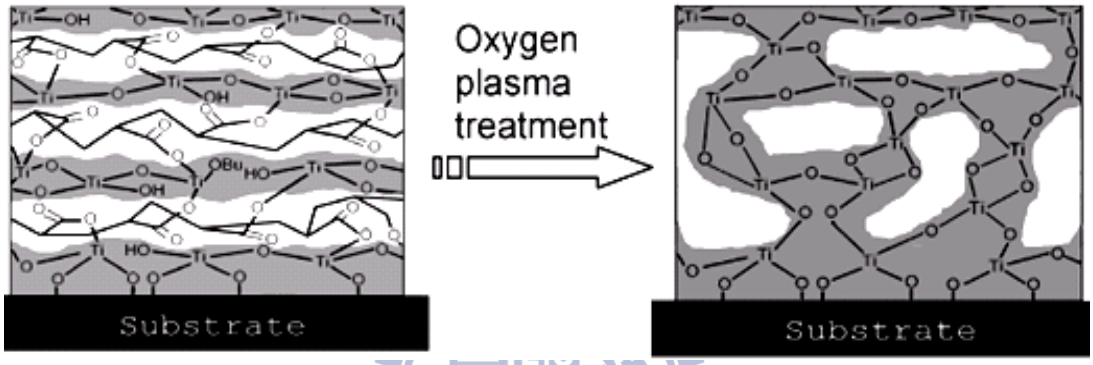


Figure 2.10 Low-temperature oxygen plasma treatments on titania/PAA nanocomposite film. [Cited from ref. **25**]

To understand the mechanism of oxygen plasma treatment was carried out as control on titania films prepared by means of stepwise adsorption of titanium n-butoxide alone. This suggests removal of 2-mercaptoethanol layer and the small amount of unhydrolyzed butoxide groups that remained in the original titania gel film as shown in Figure 2.10. In the as-prepared film, the plasma treatment removed the mass corresponding to the carbon impurities available on the film surface. The plasma etching is mainly caused by direct interaction of active atoms and molecules in the plasma (O^+,O^-,O^{2+},O^{2-},O,O^3, ionized ozone, metastably excited O_2, free electrons, etc.) with organic species in the sample, and the photon in the UV region can break the C-C and C-H bonds. The product includes CO_2, CO, H_2O, and hydrocarbons of low molecular weight, and they are removed in vacuo [**25**].

2.5 Metal-Insulator-Metal Capacitor

2.5.1 Introduction

A capacitor is a passive electronic component consisting of a pair of conductors separated by a dielectric (insulator). When there is a potential difference (voltage) across the conductors, a static electric field develops across the dielectric, causing positive charge to collect on one plate and negative charge on the other plate as depicted in Figure 2.11 [**26, 27**]. Energy is stored in the electrostatic field. An ideal capacitor is characterized by a single constant value, capacitance, measured in farads. This is the ratio of the electric charge on each conductor to the potential difference between them. Capacitors are widely used in electronic circuits for blocking direct current while allowing alternating current to pass, in filter networks, for smoothing the output of power supplies, in the resonant circuits that tune radios to particular frequencies and for many other purposes.

A very important characteristic of a capacitor is its capacitance which is a measure of how much electrical charge it can store for a given voltage applied across the two metal layers. The capacitance of a parallel-plate MIM capacitor can be calculated by Equation 2.1[**28**]

$$C = \frac{\varepsilon_0 k}{d} A \qquad (2.1)$$

Equation 2.1 shows that the capacitance depends on the dimensions of the capacitor and the properties of the insulator material. The important dimensions are the area of the capacitor (A) and the thickness of the insulator layer (d).

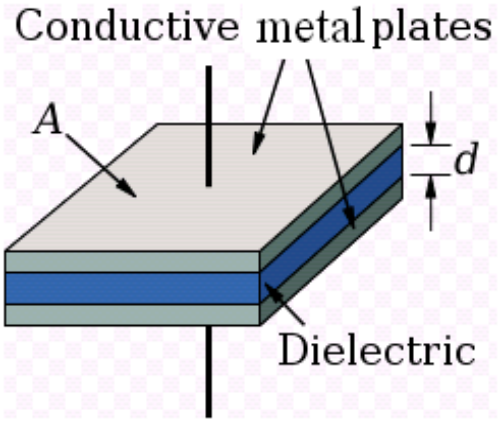


Figure 2.11 Schematic of Metal-Insulator-Metal structured capacitor. [Cited from http://en.wikipedia.org/wiki/Capacitor]

The capacitance increases if the area, A, is increased or if the insulator thickness, t, is reduced. The capacitance also depends on a physical constant, ε_0, which does not change with technology, and a property of the insulator material called the dielectric constant, k. The value of k for the most commonly used dielectric, silicon dioxide, is approximately 3.9. With each new generation of technology there is a demand to reduce the size of the components to fit more of them into a single IC.

2.5.2 Leakage Current

Recently, there are many researches for examining the leakage current of MOS capacitor devices with high dielectric gate oxide. In the MOS structure there are several conduction mechanisms that have been proposed to describe the leakage current conduction in dielectric films [**29**]. Leakage current is the unintended loss of electrical current or electrons. In fact, leakage is a problem that inhibits faster advancements in computer performance. The term also applies to electronics and consumer electronics devices. Semiconductors make use of millions of transistors to perform calculations and store data in computer microprocessors. Transistors are devices used to amplify and switch electronic signals. Leakage current in

semiconductors occurs at the transistor level. As semiconductor manufacturers continue to make transistors smaller to squeeze more onto a chip, leakage current problems increase. The small size of transistor, having thin insulating layer may cause more leakage current. Leakage in transistors causes semiconductors to require more power to operate, as they must replace the current lost to leakage [**30**].

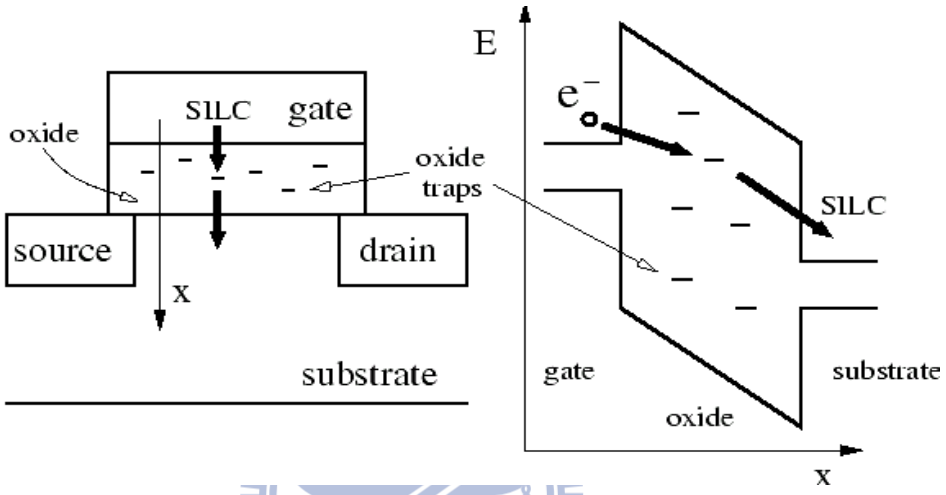


Figure 2.12 Schematic plot of the trap generation in the gate oxide. The presence of traps in the energy barrier yields the Trap Assisted Tunneling mechanism. [Cited from ref. **30**]

The leakage current of an electrolytic capacitor is based on the physical properties that lead to electrical losses. These are as follows: (i) Energy required to building up oxide layers (ii) Weaknesses in the dielectric which result in a low current flow and (iii) Tunnel effects. The corresponding configuration for the measurement of each current is illustrated in Figure 2.12. The conduction mechanism for three current components indicates that the electron tunneled through the traps to the substrate, produces the problem of leakage current. Therefore authors focus on the role of those carriers for the generation of oxide traps and hence leakage current problems in electronic devices.

2.5.3 Traps Influenced Current-Transport Mechanism

Recently, high-k dielectrics have been investigated widely in order to replace conventional SiO_2 for reducing gate leakage current. However, because of the high density of bulk traps, device with high-k based dielectric also suffers mobility degradation and poor reliability as sketched viewed in Figure 2.13. In addition, it has been reported that the bulk traps significantly enhance the gate induced drain leakage (GIDL) current in high-k devices [**31**].

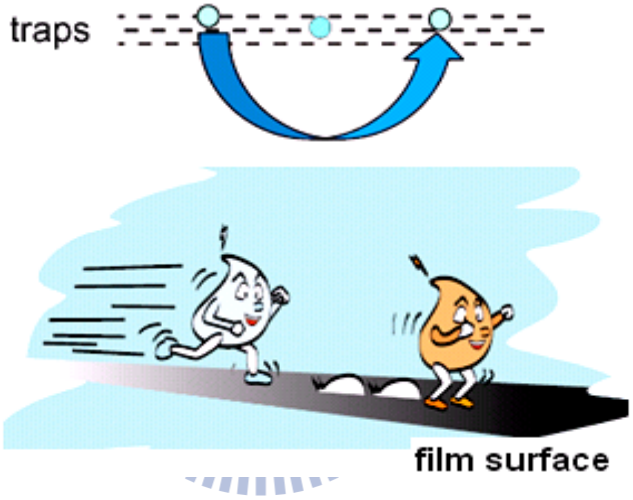


Figure 2.13 Schematic pictures to represent the traps over film surface. [Cited from ref. **31**]

The Poole–Frenkel emission [**32**], is a means by which an electrical insulator can conduct electricity. It is named after Y. Frenkel, who published on it in 1938, [**33**] and also after H. H. Poole (Horace Hewitt Poole, 1886-1962), Ireland. Electrons can move (slowly) through an insulator by the following method. The electrons are generally trapped in localized states (loosely speaking, they are "stuck" to a single atom, and not free to move around the crystal). Occasionally, random thermal fluctuations will give that electron enough energy to get out of its localized state, and move to the conduction band. Once there, the electron can move through the crystal, for a brief

amount of time, before relaxing into another localized state (in other words, "sticking" to a different atom). The Poole–Frenkel effect describes how, in a large electric field,

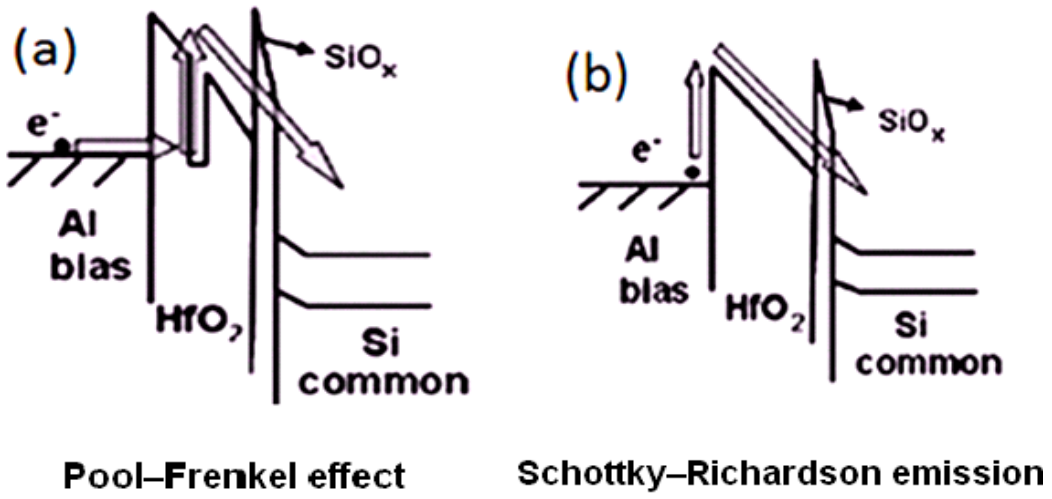


Figure 2.14(a) Schematic energy band diagram for HfO_2 film to explain Pool–Frenkel effect, and (b) Schematic energy band diagram to explain the Schottky–Richardson emission. [Cited from refs. **35** & **36**]

the electron doesn't need as much thermal energy to get into the conduction band (since part of this energy comes from being pulled by the electric field), so it does not need as large a thermal fluctuation and will be able to move more frequently. Taking everything into account (both the frequency with which electrons get excited into the conduction band, and their motion once they're there), the standard quantitative expression for the Poole–Frenkel effect [**34**] is described by the equation

$$J = CE\exp(\frac{-q\phi_t}{kT})\exp\left[\frac{1}{r\,k\,T}\sqrt{\frac{q^3}{\pi\varepsilon_0 K_T}}\sqrt{E}\right] \qquad (2.2)$$

The energy barrier separating the traps from the conduction band as shown in

Figure 2.14 (a), for HfO_2 film showed the energy band affected because of partial traps remained and procure poorer dielectric properties [**35**]. Further curing treatment to reduce the surface traps, the Poole–Frenkel emission is gradually restrained. Finally, the current transport mechanism is replaced by Schottky–Richardson emission. For standard Schottky–Richardson emission [**36**], can be expressed as

$$J = A^{*}T^{2}\exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0})}{KT}\right] \tag{2.3}$$

The inset of Figure 2.14 (b), which is independent of traps, dominates the conduction mechanism. The conversion of current transport mechanism from trap-assisted tunneling to Schottky–Richardson emission demonstrates theoretically that the traps were really terminated during the thermal or passivation curing process.

2.5.4 Capacitance and Dielectric Constant

Capacitance is a property that exists between any two conductive surfaces within some reasonable proximity (Figure 2.15). A change in the distance between the surfaces changes the capacitance. It is this change of capacitance that capacitive sensors use to indicate changes in position of a target. Capacitance (symbol '*C*') is a measure of a capacitor's ability to store charge. A large capacitance means that more charge can be stored. Capacitance is measured in farads, denoted by symbol '*F*'.

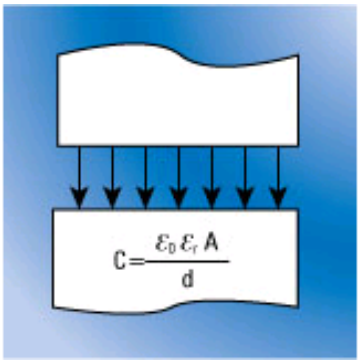


Figure 2.15 The plates are metallic and they are separated by a distance (*d*). [Cited from ref. **37**]

A substance in which an electric field may be maintained with zero or near-zero power dissipation, i.e., the electrical conductivity is zero or near zero. A dielectric material is an electrical insulator, when a dielectric is placed in an electric field; electric charges do not flow through the material, as in a conductor, but only slightly shift from their average equilibrium positions causing dielectric polarization. Because of dielectric polarization, positive charges are displaced toward the field and negative charges shift in the opposite direction. This creates an internal electric field which reduces the overall field within the dielectric itself. If a dielectric is composed of weakly bonded molecules, those molecules not only become polarized, but also reorient so that their symmetry axis aligns to the field [**37**]. The latter is expressed by a number called the dielectric constant. A common, yet notable example of a dielectric is the electrically insulating material between the metallic plates of a capacitor.

2.6 Metal-Insulator-Semiconductor Capacitor

MIS capacitor is a capacitor formed from a layer of metal, a layer of insulating material and a layer of semiconductor material [**38**]. It gets name from the initials of the metal-insulator-semiconductor structure (Figure 2.16).

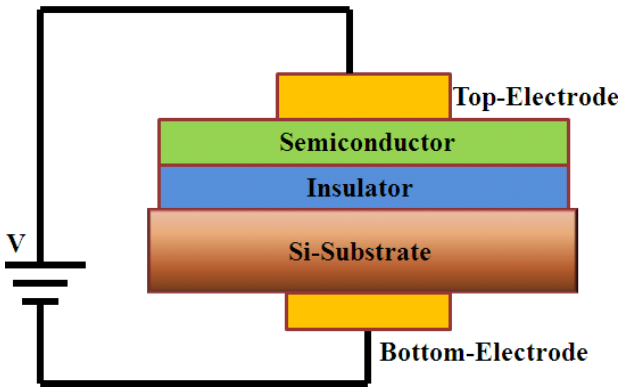


Figure 2.16 Schematic of Metal-Insulator-Semiconductor structured capacitor.

As with the MOS field-effect transistor structure, for historical reasons, this layer is also often referred to as a MOS capacitor, but this specifically refers to an oxide insulator material. The maximum capacitance, $C_{MIS\ (max)}$ is calculated analogously to the plate capacitor,

$$C_{MIS}=\frac{\varepsilon_0 k}{d}A \qquad (2.4)$$

Where, k is the insulator's dielectric constant, ε_0 is the permittivity of the vacuum, A is the area, and d is the insulator thickness.

2.7 Organic Thin-Film Transistor

2.7.1 Introduction

Organic transistors are transistors that use organic molecules rather than silicon for their active material. The motivations in using organic active materials come from their ease in tuning electronic and processing properties by chemical design and synthesis, low cost processing based on low temperature processes and reel-to-reel printing methods, mechanical flexibility, and compatibility with flexible

substrates [**39, 40**]. There are some benefits of being lower-cost deposition processes requirements such as spin-coating, printing, evaporation and less need to worry about dangling bonds makes for simpler processing. Organic thin film transistors (OTFTs) are the basic building blocks for flexible integrated circuits and displays. There are some constraints with OTFT of lower mobility and switching speeds compared to silicon wafers and usually do not operate under inversion mode.

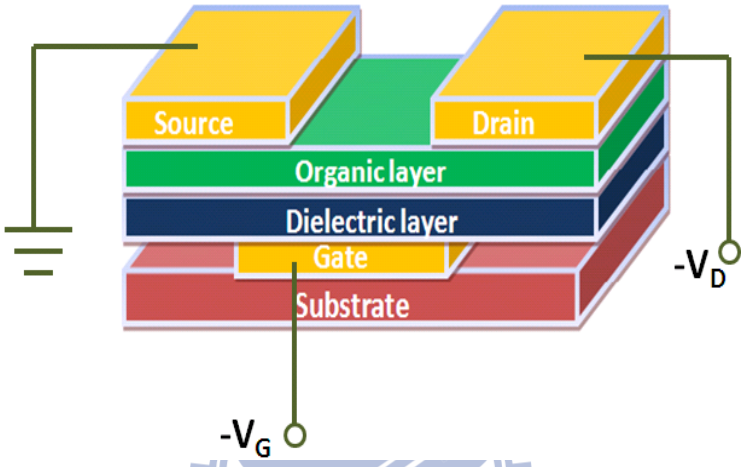


Figure 2.17 Schematic structure of an organic thin-film transistor OTFT.

A schematic structure is shown in Figure 2.17. During the operation of the transistor, a gate electrode is used to control the current flow between the drain and source electrodes. Typically, a higher applied gate voltage leads to higher current flow between drain and source electrodes. The semiconductor material for a fast switching transistor should have high charge carrier mobility and on/off current ratio. For pixel switching transistors in liquid crystal displays, mobility greater than 0.1 cm^2 $V^{-1}s^{-1}$ and on/off ratio greater than 10^6 are needed.

2.7.2 On-to-Off current-ratio and Carrier-Mobility

One measurement of the TFT performance is the ratio between the highest ON current measured (I_{on}) and the minimum leakage current measured when the TFT is

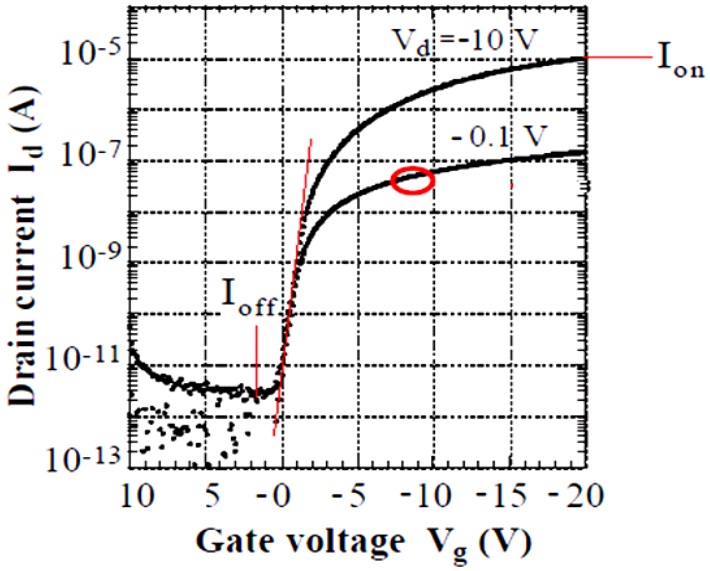


Figure 2.18 TFT transfer characteristics. ON current, OFF current, and sub-threshold form this plot. [Cited from ref. **42**]

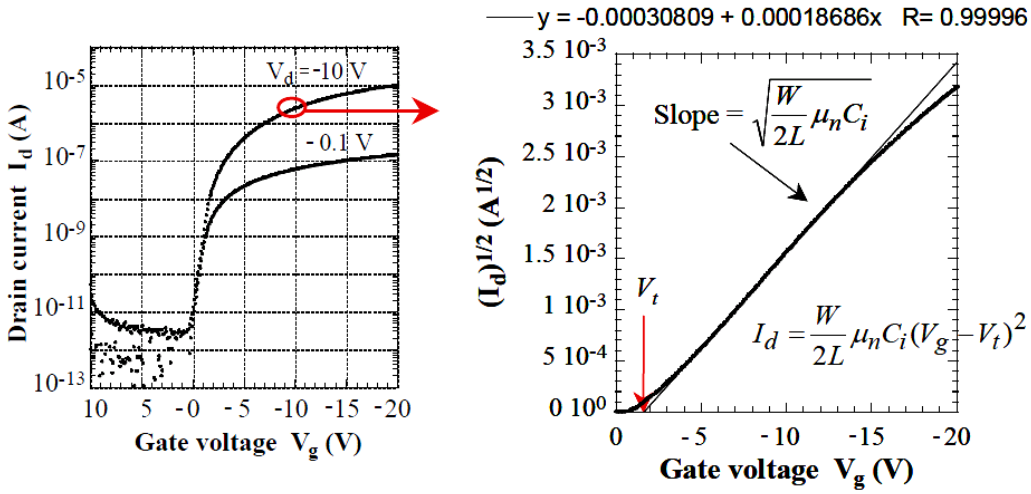


Figure 2.19 Drain current is plotted against gate voltage for the high drain voltage condition, V_d = 10 V. Threshold voltage (V_t) and saturation mobility ($\mu_{n,sat}$) can be extracted from such a plot. [Cited from ref. **42**]

OFF (I_{off}) and we define I_{on}/I_{off} current ratio as [**41**]

$$\frac{I_{on}}{I_{off}} = \frac{I_d(V_d, V_{g,Max})}{I_d(V_d, V_{g,Min})}$$

(2.5)

The ON/OFF ratios were calculated between a maximum gate bias of $V_{g,Max}$ and a minimum gate bias just below the switch-on voltage as indicated in Figure 2.18 [**42**]. One measure of the ease with which electrons flow between source and drain when the channel is biased into accumulation is the electron field-effect mobility, μ_n. Specifically, it is the velocity of electrons per unit (source-drain) electric field, with units [$cm^2\ V^{-1}s^{-1}$]. They are related by 1 $m^2\ V^{-1}s^{-1}$ = $10^4\ cm^2\ V^{-1}s^{-1}$ the carrier mobility characterizes how quickly an electron or hole can move through a metal or semiconductor, when pulled by an electric field. There are, in fact, two field-effect mobilities evaluated, linear-region mobility and saturation-region mobility, which have similar but usually not identical values. Carrier mobility is special cases of electrical mobility of charged particles in a fluid under an applied electric field. In semiconductors, there is an analogous quantity for holes and electrons, called hole or electron mobility. The term carrier mobility refers in general to both electron and hole mobility in semiconductors. All transistors operate in the accumulation regime, the charges being transported by the radical cations of the p-type organic semiconductors. Carrier mobilities were extracted from the transfer characteristics in the saturation regime according to [**43**].

To determine the saturation-region mobility, consider the drain-to-source current in saturation region when $V_{ds} > V_{gs} - V_t$

$$I_{d,sat} = \frac{W}{2L}\mu_{nsat}C_i\left(V_{gs} - V_t\right)^2$$

(2.6)

Taking the square-root of $I_{d,sat}$ of equation (2.6) we obtain

$$\sqrt{I_{d,sat}} = \sqrt{\frac{W\mu_{n_{sat}}C_i}{2L}}\left(V_{gs} - V_t\right)$$

(2.7)

This equation (2.7) reveals that $\sqrt{I_{d,sat}}$ is linear with respect to V_{gs}, with the x-intercept corresponding to the threshold voltage, V_t. Plotting $\sqrt{I_{d,sat}}$ versus V_{gs}, from the actual experimental data will reveal a linear region from Figure 2.19. The threshold voltage can be determined by extrapolating down to the x-intercept. The slope of this plot can be determined analytically,

$$Slope = \frac{\partial\sqrt{I_{d,sat}}}{\partial V_g} = \sqrt{\frac{W\mu_{n,sat}C_i}{2L}}$$

(2.8)

The saturation mobility is

$$\mu_{n_{sat}} = Slope^2\left(\frac{2L}{WC_i}\right)$$

(2.9)

The saturation mobility can be calculated from the slope, capacitance, length and width of the TFT.

2.7.3 Semiconductor Materials for Channel

To make OTFTs, semiconductors for active channel materials are needed. This active channel material can be composed of a wide variety of molecules. There are two types of organic semiconductors based on the type of majority charge carriers: p-type (holes as major charge carriers) and n-type (electrons as major charge carriers). To facilitate charge transport, the organic semiconductor layer usually consists of π-conjugated oligomers or polymers, in which the π–π stacking direction should ideally be along the current flow direction. The chemical structures of some representative materials are shown in Figure 2.20 p-Channel compounds [**44**] in this category include substituted thiophene oligomers, pentacene, acenes, and their derivatives, phthalocyanine- and thiophene-based fused ring compounds, and fluorene oligomer derivatives.

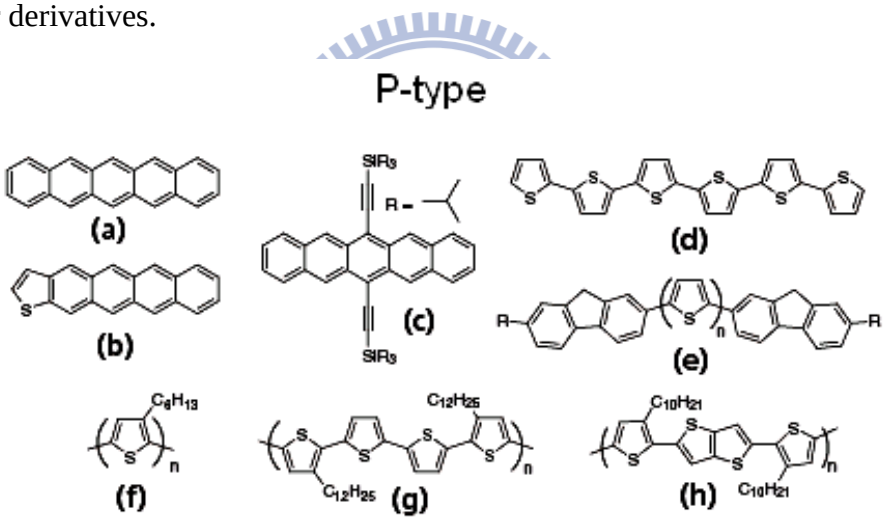


Figure 2.20 Chemical structures of some representative p-channel organic semiconductors such as (a) pentacene; (b) tetraceno[2,3-b]thiophene; (c) TIPS-pentacene; (d) a-sexithiophene; (e) oligothiophene-fluorene derivative; (f) regioregular(poly3-hexylthiophene); (g) poly(3,3’’’-didodecylquaterthiophene); (h) poly(2,5-bis(3-decylthiophen-2-yl)thieno[3,2- b]thiophene). [Cited from ref. **44**]

Regioregular poly(3-hexylthiophene) is one of the few polymer semiconductors that spontaneously assembles into well ordered structures upon solution deposition by

drop casting or spin coating [**45**] (Figure 2.20) and gives a mobility greater than 0.1 $cm^2\ V^{-1}s^{-1}$ [**46**]. More recently, a few new polythiophene derivatives have been reported and show improved mobility and air stability (Figure 2.20 (g, h)) [**47, 48**]. Several classes of organic materials have displayed good n-channel activity, including C60, perfluoro-copper phthalocyanine, and naphthalene and perylene-based compounds [**49-52**]. Figure 2.21 shows the chemical structures of some representative high performance air-stable n-channel semiconductors [**44**]. More recently, ambipolar behavior for certain organic semiconductors has also been reported [**53**]. This type of material can be used for the fabrication of complementary circuits without the need to pattern the p- and n-channel semiconductors separately.

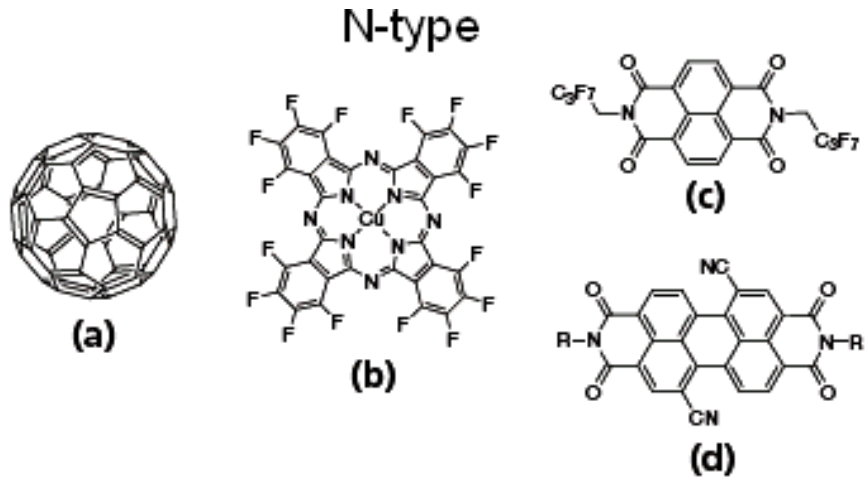


Figure 2.21 Chemical structures of some representative n-channel organic semiconductors, (a) C_{60}; (b) hexadecafluoro copper phthalocyanine (F_{16}CuPc); (c) naphthalene diimide derivative; (d) perylene diimide derivative. [Cited from ref. **44**]

In a 2000 white paper by IBM, C. D. Dimitrakopoulos and D. J. Mascaro proposed that, the most widely used organic semiconductors, such as pentacene, thiophene oligomers and regioregular polythiophene; seem to have reached maturity as far as their performance is concerned. This assumption was based upon a graph in Figure 2.22 that showed an apparently asymptotic limit of carrier mobility for OTFT.

The limit may be seen as an extension of the charge transport mechanisms between amorphous and polycrystalline silicon and organics.

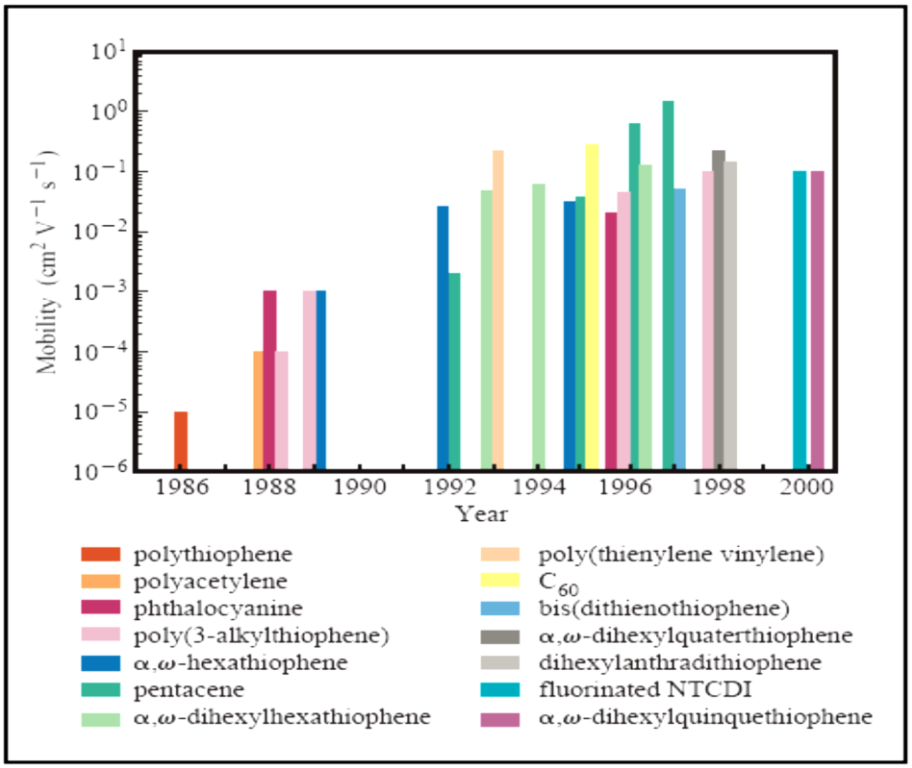
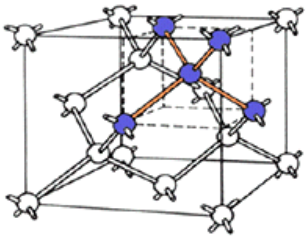


Figure 2.22 Chart showing different average electron mobility in commonly investigated OTFT-semiconductor materials. [Cited from ref. **54**]

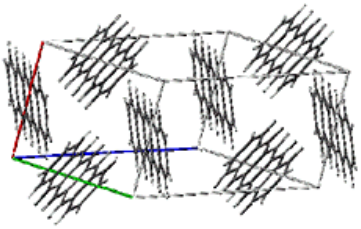
In silicon semiconductors, the atoms are connected with strong covalent bonds and charge carriers move as delocalized waves and thus have a high mobility. However, in this case of organic semiconductors, carrier transport takes place by hopping between localized states. However, the IBM researchers also proposed that by either strengthening the bonds in the organics or by using singular chains for charge transport, this apparent limit could be breached [**54**].

2.7.4 Relation of Inorganic to Organic Semiconductor Materials

Inorganic and organic hybrids have become a creative alternative with unusual features for materials in the electronic industry. The possibilities to combine the characteristics of inorganic with organic structures and tailoring the properties of new products have emerged during the last couple of decades. With the availability of a range of inorganic silicon based raw materials, with a variety of functional organic and inorganic groups, new materials have been developed in different fields of the industry. For flexible electronics organic semiconducting materials are most suitable and have advantage over silicon based inorganic materials as compared in Figure 2.23.



- Silicon based inorganic material
- Covalently bonded crystals



- Polymer based organic material
- Van der Waals bonded crystals

Figure 2.23 Comparison between inorganic and organic semiconductor based material. [Cited from http://www.scribd.com/doc/48232855/Organic-Semiconductor]

It turns out that, at low temperature, the charge transport in a number of organic crystals and highly organized thin films can be described in a band-like regime similar to that in inorganic semiconductors. The biggest advantage of conductive polymer based Organic materials are their processability, mainly due of Van der Walls forces hold molecules together over their counterpart inorganic materials. The charge hopping, the major factor limiting mobility, takes place from

molecule to molecule but phonons help electron's hop, therefore increasing mobility. Mobility increases in organic TFT devices with temperature because of phonons.

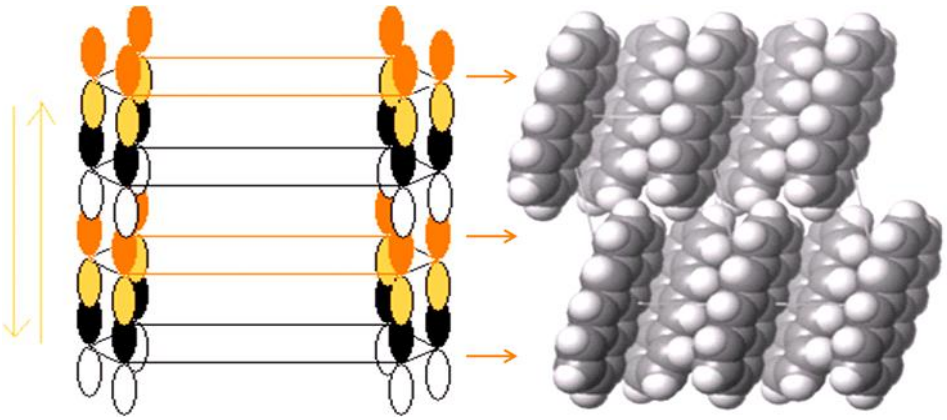


Figure 2.24 Illustration of the highly ordered structures and arrangement may facilitate the intermolecular hopping process. [Cited from ref. **55**]

Here, quantum-chemical calculations are performed on model systems as shown in Figure 2.24 to address the way transfer integrals between adjacent chains are affected by the nature and relative positions of the interacting units. Compounds under investigation include oligothienylenes, hexabenzocoronene, oligoacenes, and perylene. It is shown that the amplitude of the transfer integrals is extremely sensitive to the molecular packing. Interestingly, in contrast to conventional wisdom, specific arrangements can lead to electron mobilities that are larger than hole mobilities, which is, for instance, the case of perylene. There are two major overlapping classes of organic semiconductors. These are organic charge-transfer complexes and various linear-backbone conductive polymers derived from polyacetylene. Highly ordered structures and arrangement may facilitate the intermolecular hopping process. There are many different fabrication techniques on different substrates are being developed to make organic materials based devices on debate in the future implications of nanotechnology [**55**].

Chapter 3: Experimental Methods

3.1 General Introduction

All the experiments were preceded in National Chiao Tung University (NCTU), Taiwan. All the equipments were also conducted in our laboratories in NCTU. The reagents were purchased commercially available and used by following with the directions unless specially mentioned. All the reagents were listed alphabetically in the form of "Name {abbreviation; chemical formula; purity; manufacturer}. Some information is omitted if not available or not necessary.

3.2 Material Synthesis and Experimental Flowcharts

An overall vision is to utilize our strength in material synthesis as a basis for approaching rational design of improved catalysts and adsorbents. A number of materials types are of necessary in synthesis and fabrication were used.

DuPont™ Kapton® Polyimide (abbreviated as PI) film, Thickness: 25, 30 & 38 μm: PV9100 series.

Kapton® PI films were used as substrate to fabricate the devices.

Deionized and distilled water {DI water, ddH_2O}

The water used was purified with filters, reverse osmosis, and deinized system until the resistance was more than 18 MΩ.cm^{-1}. DI water was used to clean, wash, and

be a solvent.

Ethanol {C_2H_5OH, Fluka, water content < 0.1%}

In our experiment, it was used as a solvent in making sol-gel solution

$HfCl_4$, Hafnium (IV) chloride: ≥ 98 %, and $TiCl_4$, Titanium (IV) Tetrachloride, 99.5 %, All purchased from Aldrich.

PAA: Chart 1; Polymer Source, Inc.

Pluronic® P123 Block Copolymer Surfactant: Triblock copolymer: $HO(CH_2CH_2O)_{20}(CH_2CH(CH_3)O)_{70}$ $(CH_2CH_2O)_{20}H$ ($EO_{20}PO_{70}EO_{20}$, MW = 5800, O-BASF Corporation

Polystyrene ($(C_8H_8)_n$, MW=54000, Aldrich), catalyst chloroform ($CHCl_3$, 98%, Aldrich), and toluene ($C_6H_5CH_3$, Tedia Co. Inc.)

All solvents were guaranteed reagents and used as precursor solvents without further purification.

P3HT (Merck), Poly (3-hexylthiophene-2, 5-diyl, Electronic grade, UniRegion Bio-Tech)

Pentacene ($C_{22}H_{14}$); (**Seed Chem. Co., Electronic grade, PTY. LTD.)**

P3HT and Pentacene were used as active semiconductor materials in devices fabrication processes.

Chromium (Cr) shots {99.999%, ADMAT}, Size: 3-5 mm, Aluminum (Al) shots {99.999%, ADMAT}, Size: 3-5 mm, Gold (Au) shots {98.999%, ADMAT}, Size: 1-2 mm

The Cr, Al and Au films an electrode were deposited over PI substrate by a thermal coater evaporation system which Chromium, aluminum and Gold shots and tungsten boat were used during deposition process.

Film-thickness measured by Ellipsometry techniques

The experimental procedures and structure property analysis methods for each

process is discussed separately in more details using the process flowchart in the following sections.

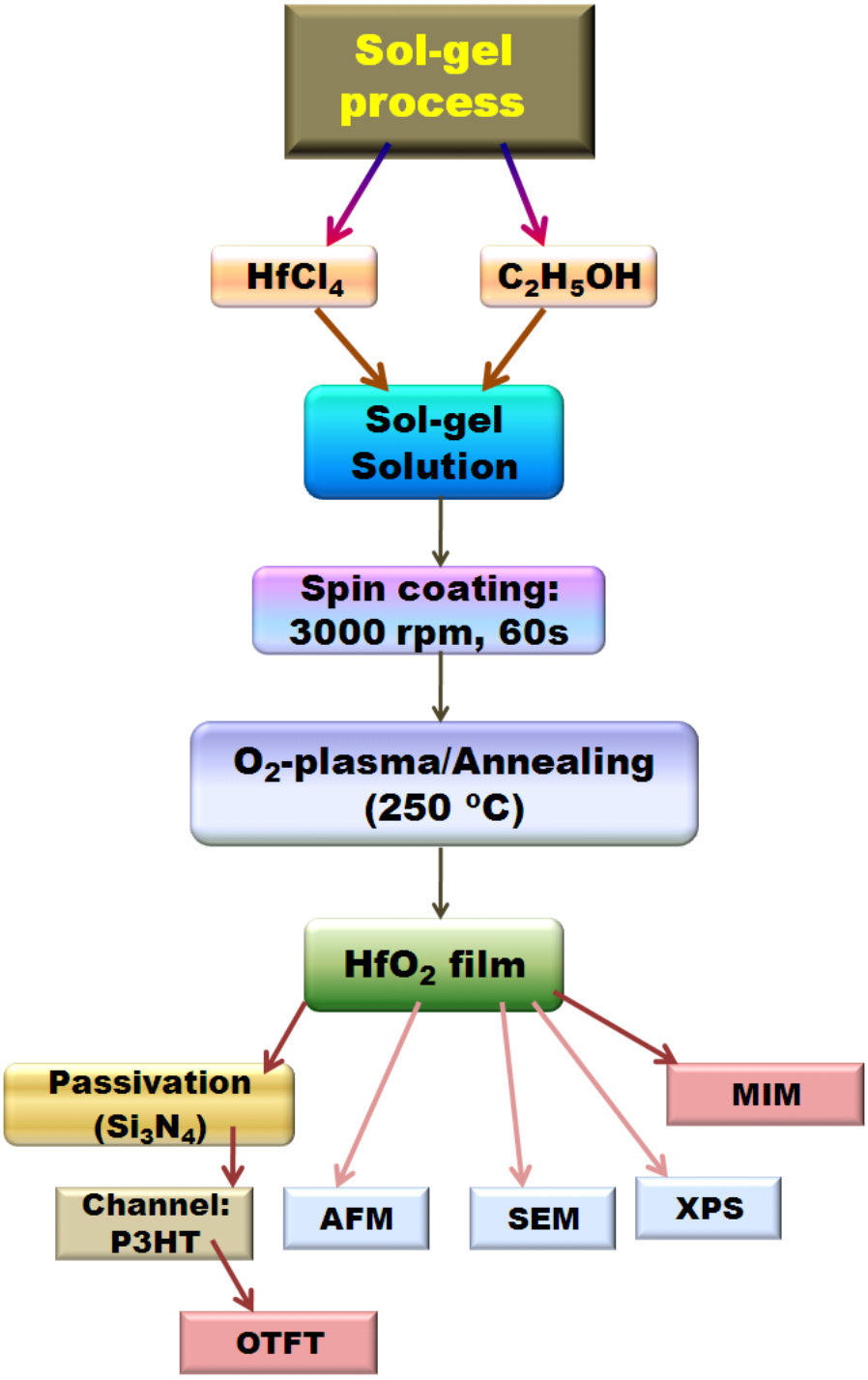


Figure 3.1 Experimental flowchart of fabrications of MIM capacitor and P3HT-TFT devices using high-k gate dielectrics of HfO_2 film via surface sol-gel spin coating processes.

Figure 3.1 shows the experiment flowchart to how fabricate MIM capacitors using high-k gate dielectrics of HfO_2 film via surface sol-gel spin coating processes; while OTFT using HfO_2-Si_3N_4 as dielectric layer and P3HT as channel layer. The surface morphology and chemical composition were analyzed by SEM, AFM, XPS and XRD etc. The electrical measurements of HfO_2 were performed at room temperature using a conventional 4-probe system, for MIM capacitor and OTFT devices.

Figure 3.2 illustrates the flowchart of fabrication of MIS capacitor device via dip-coating solution processes using nc-TiO_2 as gate dielectric and pentacene as an organic semiconductor. The surface morphology and chemical composition for both TiO_2 and pentacene films were analyzed by SEM, AFM, XPS and XRD etc. For electrical measurements, we made MIS structured device. Figure 3.3 shows the experimental flowchart of fabrication of MIM and OTFT devices via dip-coating solution processes using P123-PS as gate dielectric and pentacene as semiconductor layer. Composite materials analysis has been discussed by FT-IR and AFM analyses. All the experiments and analyses were performed over flexible DuPoint Kapton® PI films.

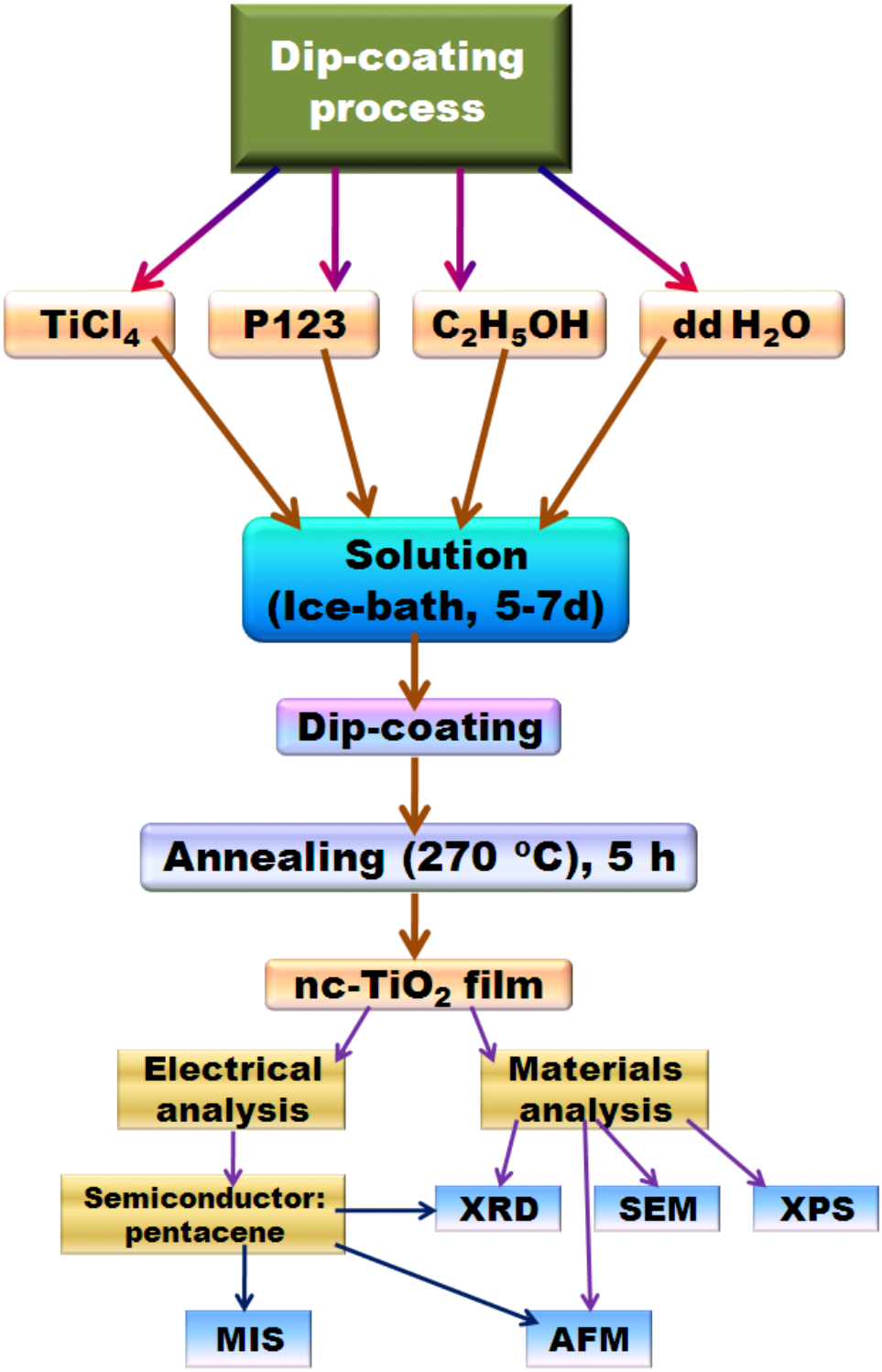


Figure 3.2 Experimental flowchart of fabrication of MIS capacitor via dip-coating solution processes using nc-TiO_2 as gate dielectric and pentacene as semiconductor layer.

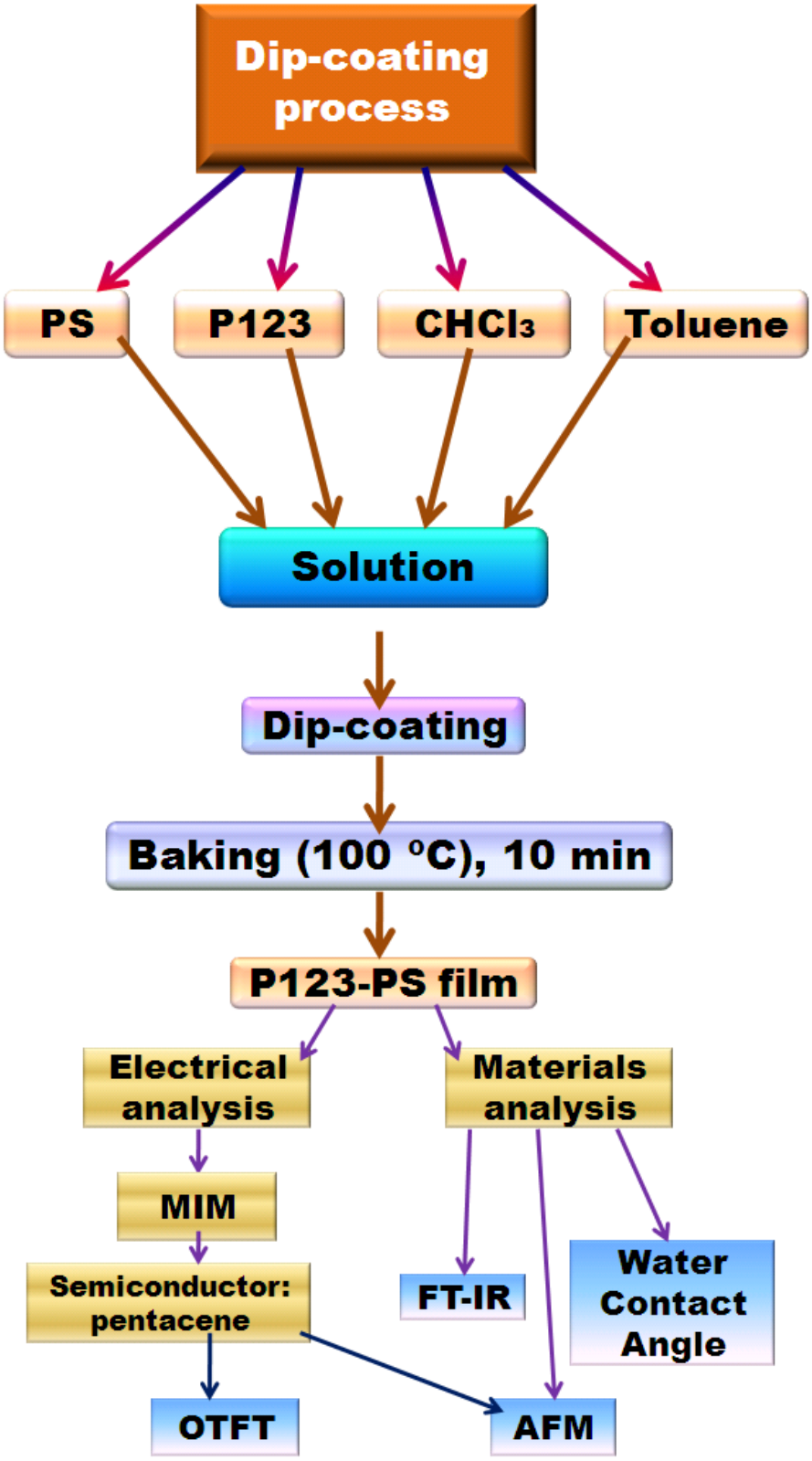


Figure 3.3 Experimental flowchart of fabrication of MIM and OTFT devices via dip-coating solution processes using P123-PS as gate dielectric and pentacene as semiconductor layer.

3.3 Sol-Gel Spins Coating Techniques

Sol-gel spins coating is perfectly adapted for substrates which present the rotation symmetry, as molding tools for the production of thin film in electronics components. The solution is versed in a continuous flux on the rotating sample as shown in Figure 3.3. The solution is then homogeneously dispersed on all the surface of the sample. Spin coating technique allows the production of homogeneous film in term of thickness. The first, although incidental, observation of sol-gel process dates back to 1846. It covered the hydrolysis and poly-condensation of silicic acid under humidity, which progressed to the point of a silicate glass formation. An extension of the chemical principles involved was shown in 1969-1971, pointing out the importance of reactions of several metal alkoxides in solution under formation of metal (I)–oxygen–metal (II) bonds. This made the possibility of production of defined multi-component oxide glasses, glass-ceramics and crystalline layers. This research effort into the involved basic chemistry followed the path used in the study of reactions of metal-organic compounds [**1**]. Sol–gel processing has been widely used because it permits fabrication of oxide materials under mild conditions and with a wide range of adjustable experimental parameters. To give a very brief definition, a sol–gel procedure encompasses any process that involves polymerization of soluble precursor molecules to afford a polymeric material, via the intermediate formation of a colloidal sol phase [**2**].

Sol-gel processing can be divided into two main steps, that is, hydrolysis and condensation, as shown in Figure 3.4. Basically, Hydrolysis and condensation are influenced by partial substitutions of alcoolates groups with organic groups [**3**]. Typically, organic acids as acetic acid or acetylaceton are used. After hydrolysis and condensation, organometallic polymers are present; this is the so called sol which will

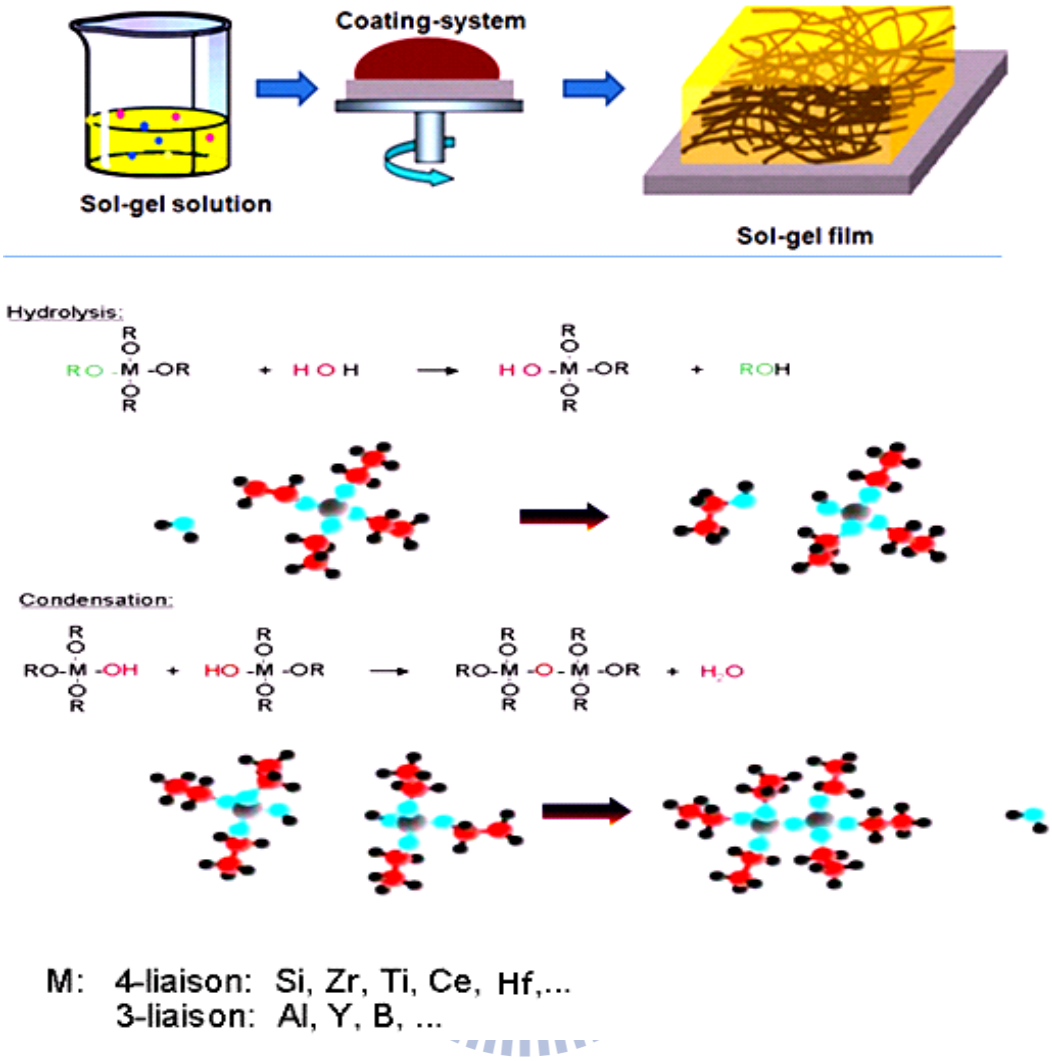


Figure 3.4 The basic steps and the reaction of sol-gel process on substrate surface: Hydrolysis and condensation are influenced by partial substitutions of alcoolates groups with organic groups.

make possible the deposition of thin oxyceramic films as SiO_2, ZrO_2, TiO_2, and Al_2O_3. Solutions used for the coating of sol-gel oxydoceramic are mainly based on metal-alcoolate components on a form of $M(OR)_n$, where M is the metal with 3 covalent liaisons (Aluminum, Yttrium, Bore) or 4 (Silicate, Titanium, Zirconium). The metallic atom is linked, through an oxygen atom, to an acrylic group, as ethylic ($-C_2H_5$), propylic ($-^{n(i)}C_3H_7$) or butylic ($-^{n(s,t)}C_4H_9$) [**4**]. By hydrolysis, the alcoolate

groups (-OR) will react with water, and will be replaced by OH-groups. This leads to the condensation and to the formation of monomers chains which will ramify and will create alcoolates polymers [**5**].

3.4 Dip-Coating Techniques

Dip coating is the ideal technique for translation symmetric substrates. The substrate is placed in the solution and is withdrawn with a controlled constant velocity, that the film covers uniformly the immerged surface. This film is left drying for some minutes to allow the sol-gel transition to take place. In IWT we use a self constructed dip coater. The available withdraw velocities are from 1 up to 50 cm.min^{-1}[**6**]. The dip-coating process is depicted in Figure 3.5.

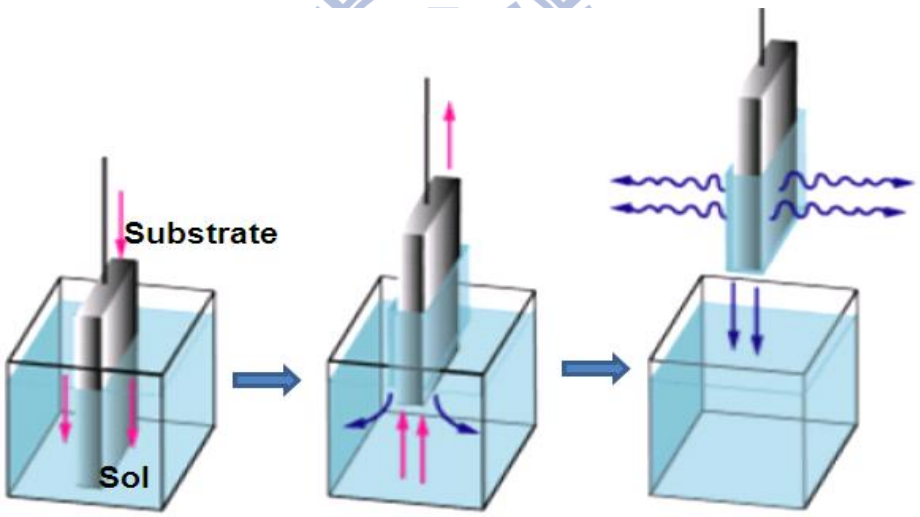


Figure 3.5 The dip-coating process cycle.

The dip coating process can be separated into five stages [**7**] as follows

- Immersion: The substrate is immersed in the solution of the coating material at a constant speed (preferably jitter-free).
- Start-up: The substrate has remained inside the solution for a while and is starting to be pulled up.

- Deposition: The thin layer deposits itself on the substrate while it is pulled up. The withdrawing is carried out at a constant speed to avoid any jitters. The speed determines the thickness of the coating (faster withdrawal gives thicker coating material).
- Drainage: Excess liquid will drain from the surface.
- Evaporation: The solvent evaporates from the liquid, forming the thin layer. For volatile solvents, such as alcohols, evaporation starts already during the deposition & drainage steps.

3.5 Harrick Plasma Systems

Plasma, the fourth state of matter, is a distinct processing medium for the treatment and modification of surfaces. Harrick Plasma Cleaners serve as excellent tools for nanoscale surface cleaning, surface preparation and surface modification [**8**]. The basic plasma system as shown in Figure 3.6; a plasma cleaner, plasma gas flow mixer, rotary vane pump with minimum pump speed of 1.4 m^3 h^{-1} (23 L min^{-1}) and ultimate total pressure of 200 mTorr or less, vacuum hose clamps and accessories to connect pump, plasma chamber outlet Suitable for concentrated oxygen and nonreactive gases (e.g. air, N_2, or Ar) and RF power [**9**].

Note: No hydrocarbon oil used (the combination of concentrated oxygen and hydrocarbon oil is an explosion hazard).

Some benefits of plasma treatment [**10**];

▪ Remove residual organic impurities and weakly bound organic contamination.

▪ Eliminate the use of chemical solvents as well as storage and disposal of solvent waste.

▪ Clean surfaces and change surface properties without affecting the bulk material.

▪ Modify surface chemistry and wet ability to tailor surface properties for specific

applications.

▪ Promote surface coverage and spreading of coatings on plasma-activated surfaces

▪ Promote adhesion and enhance bonding to other surfaces.

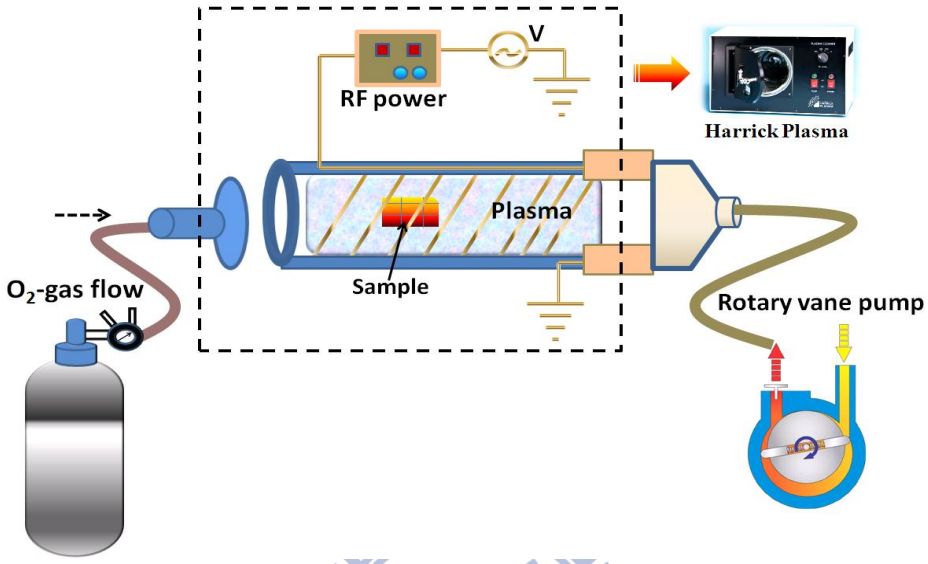


Figure 3.6 The basic configuration of oxygen plasma system

3.6 Thermal-Annealing System

It is a process that produces conditions by heating to above the recrystallization temperature, maintaining a suitable temperature, and then cooling. Annealing is used to induce ductility, soften material, surface oxidation, relieve internal stresses, refine the structure by making it homogeneous, and improve cold working properties [**11, 12**]. A schematic configuration of thermal annealing system is shown in Figure 3.7. Typically, large ovens are used for the annealing process. The inside of the oven is large enough to place the work piece in a position to receive maximum exposure to the circulating heated air.

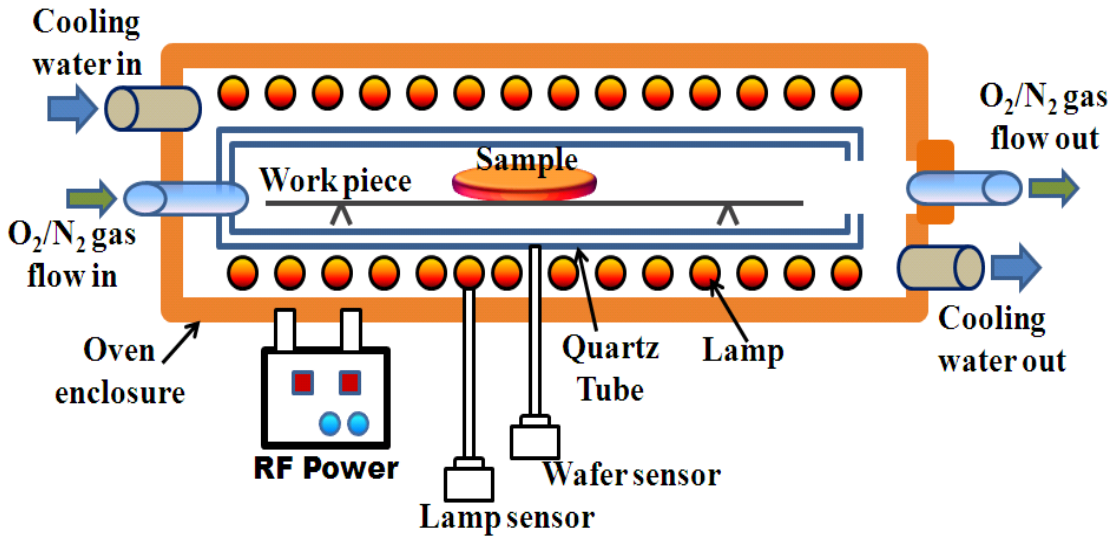


Figure 3.7 Schematic configurations of thermal annealing system of quartz isolation tube with an oven enclosure and cooling system.

For high volume process annealing, gas fired conveyor furnaces are often used. The O_2/N_2 gases are used in order to move the parts in and out with ease surface oxidation. Once the annealing process has been successfully completed, the work pieces are sometimes left in the oven i n order for the parts to have a controlled cooling process. While some work pieces are left in the oven to cool in a controlled fashion, other materials and alloys are removed from the oven. After being removed from the oven, the work pieces are often quickly cooled off in a process known as quench hardening.

3.7 PECVD System

Figure 3.8 shows Plasma Enhanced Chemical Vapor Deposition (PECVD) system is mainly used for the deposition of dielectric films and passivation films like silicon oxide or nitride or ONO layers at low temperature. The necessary energy for the chemical reaction is not introduced by heating the whole reaction chamber but just

by heated gas or plasma. It is the best method, if dopant diffusion has to be kept low, wafers have to be treated, which are sensible to high temperature or have been aluminium metallized already. The thermal budget of the treated wafers stays low with PECVD. Using an RF generator, the plasma is formed in the reaction chamber. It contains reactive ions and radicals [**13**]. The growth of the deposit starts easily because of the activation and cleaning of the surface by the more of less intense bombarding with ions from the plasma. You get good adhesion and high growth rates. The properties of the coated layers can be better influenced with PECVD than in simply thermal deposition technique, because more process parameters can be varied. Important are the adjustment of adhesion, compressive and tensile stress causing warpage, hydrogen content and density, etchability, etch rate and selectivity in etching, step coverage as well as stoichiometry (consistence) and cleanliness of the deposited layers, which can be measured by the refractive index.

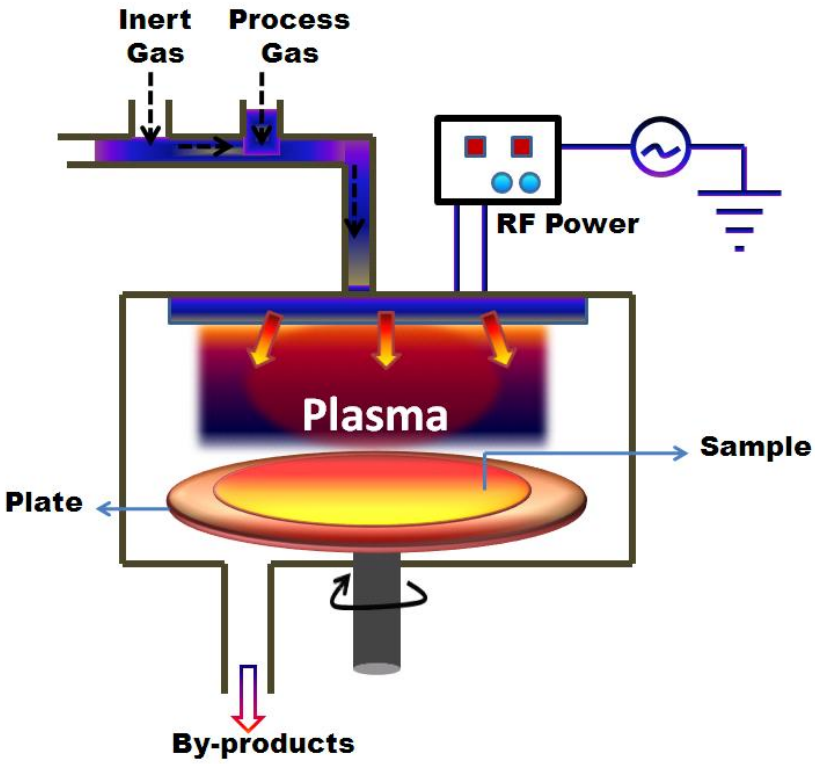


Figure 3.8 Plasma Enhanced Chemical Vapor Deposition System.

The maximum thickness of the deposit and the best uniformity of the coating is also dependent of the PECVD process parameters. Some film properties can be modified also subsequently. PECVD nitride can easily be deposited in a reproducible, very pure and uniform way. This leads to layers with good electric features, very good coverage of edges; high thermal stability and low etch rates. However; high temperatures are necessary for deposition and reaction rate is slower.

3.8 Thermal-Metal-Coater

The vacuum thermal evaporation deposition technique consists in heating until evaporation of the material to be deposited. The material vapor finally condenses in form of thin film on the cold substrate surface and on the vacuum chamber walls. Usually low pressures are used, about 10^{-6} or 10^{-5} Torr, to avoid reaction between the vapor and atmosphere. At these low pressures, the mean free path of vapor atoms is the same order as the vacuum chamber dimensions, so these particles travel in straight lines from the evaporation source towards the substrate. This originates 'shadowing' phenomena with 3D objects, especially in those regions not directly accessible from the evaporation source (crucible). Besides, in thermal evaporation techniques the average energy of vapor atoms reaching the substrate surface is generally low (order of kT, i.e. tenths of eV). This affects seriously the morphology of the films, often resulting in a porous and little adherent material. In thermal evaporation techniques, different methods can be applied to heat the material. The equipments available in the laboratory use either resistance heating. The general layout of this technique is shown in this following Figure 3.9. This method is called thermal evaporation method. It is the most versatile means of vacuum evaporation and deposition.

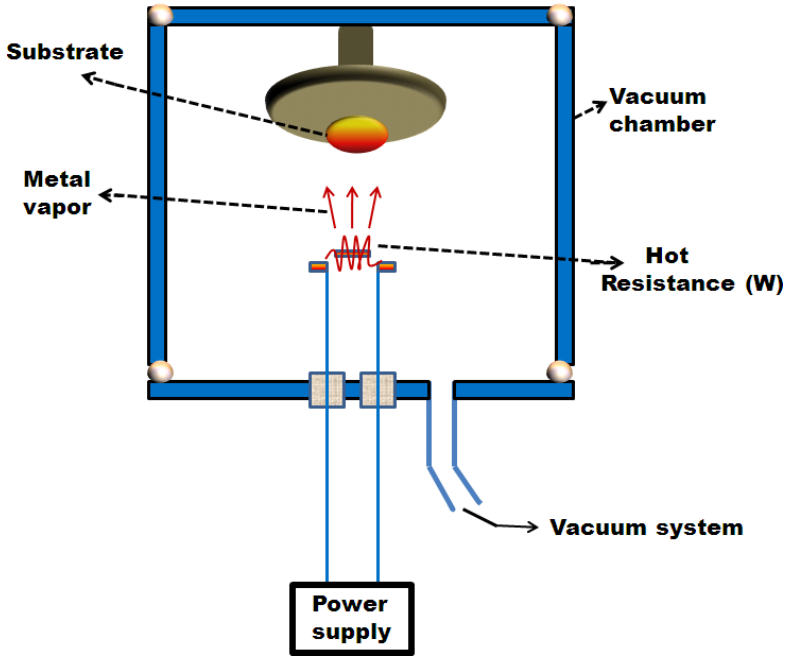


Figure 3.9 General layouts for thermal evaporation method.

This technique allows the production of thin film coatings from pure elements, including most metals, as well as numerous alloys and compounds. It offers several advantages over competing processes including precise control of low or high deposition rates, excellent material utilization, co-deposition and sequential deposition systems and a uniform low temperature deposition. Thermal evaporation offers higher evaporation rates, freedom from contamination, and precise rate control at very low deposition levels, precise film composition and cooler substrate temperatures. The materials used for evaporation are available in near limitless shapes and forms, the most common being pellet slugs. In our case we used the pallets of Cr, Au and Al to deposit the bottom and top electrode films.

3.9 Thin-Film Analysis Methods

3.9.1 SEM

Scanning electron microscopy (SEM) is used to examine the surface morphology of the samples at a high magnification [**14**]. The high magnification range of the SEM

is achieved due to its resolving power of approximately 3-6 nm. The SEM is useful and popular for many reasons. One of the great advantages of SEM is its large depth of field (the amount of sample that is in sharp focus at one time). This makes it possible to examine surfaces with a relatively high level of surface variability (and at much higher magnifications). This is because the depth of field of the SEM can be up to four hundred times greater than that of a light microscope.

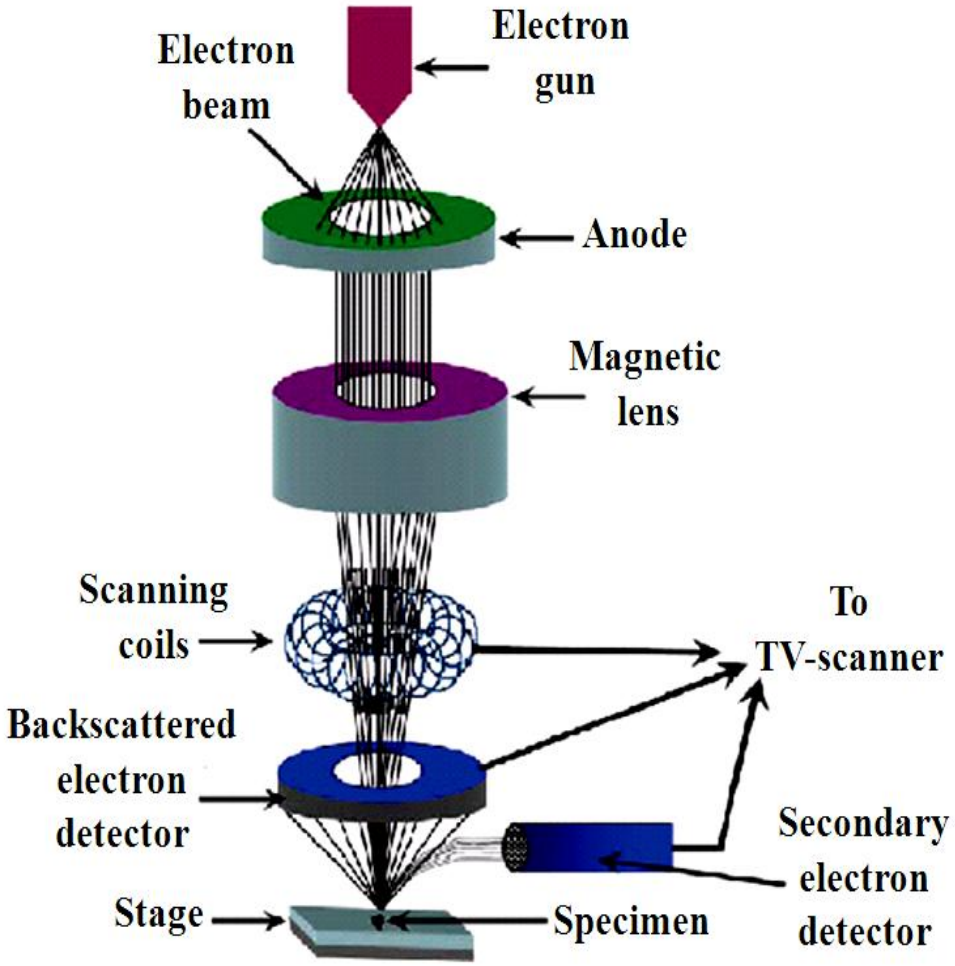


Figure 3.10 Schematic drawing of the basic principle of the SEM.

Moreover, it has the advantage of easy sample preparation, and high image resolution. A common SEM is equipped with an electron gun to generate electron beams to be 46 accelerated under 0-40 kV voltage. By deflecting the incident beams

with focusing coils, a two dimensional image can be obtained by detecting the reflected secondary electrons and the backscatter electrons. The model mainly engaged is field emission type SEM JEOL-6700. Accelerating voltage is 10 kV with current of 10 μA. Working distance is 10 mm under 9.63×10^{-5} Pa. The Figure 3.10 shows a simple schematic drawing of the basic principle of the SEM.

3.9.2 Ellipsometery

Ellipsometry is based on measurements of the changes in light polarisation upon reflection from a sample surface. A basic ellipsometer configuration [**15**] is shown in Figure 3.11. The method enables the measurement of the thickness and optical constants (refractive index) of the film. In this thesis, a Rudolph Research AutoELIV ellipsometer was used to measure the film thicknesses of silicon dioxide on silicon wafers. A monochromatic light source was generated from a white light source and a wavelength of 633 nm was used.

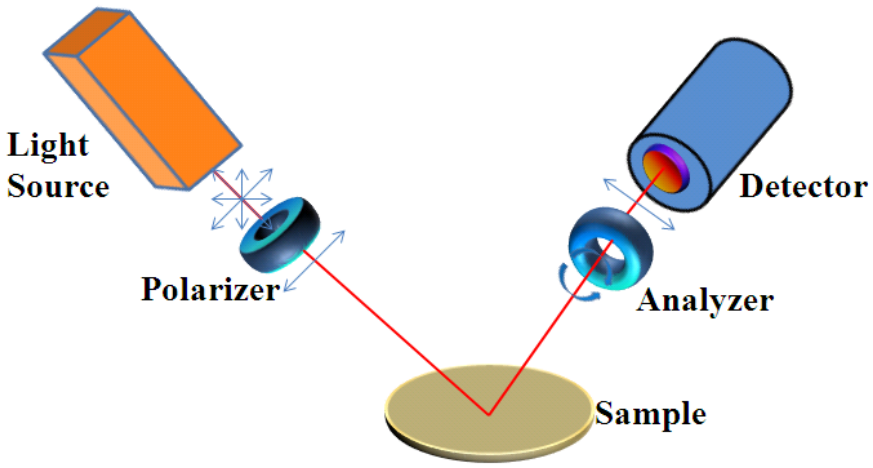


Figure 3.11 The basic configuration of the ellipsometer.

3.9.3 AFM

The Atomic Force Microscope (AFM) is one type of scanning probe microscopes,

which is used to image surface structures on nm or even sub-nm level and to measure surface roughness [**16**]. The standard AFM contains a microscopic tip (curvature radius of ~10-50nm) attached to a cantilever spring. The underlying principle of AFM is the detection of the bending of this cantilever spring as a response to external forces. In the case of adhesive interaction between the tip and a surface, this force is of the order 0.1-1 nN.

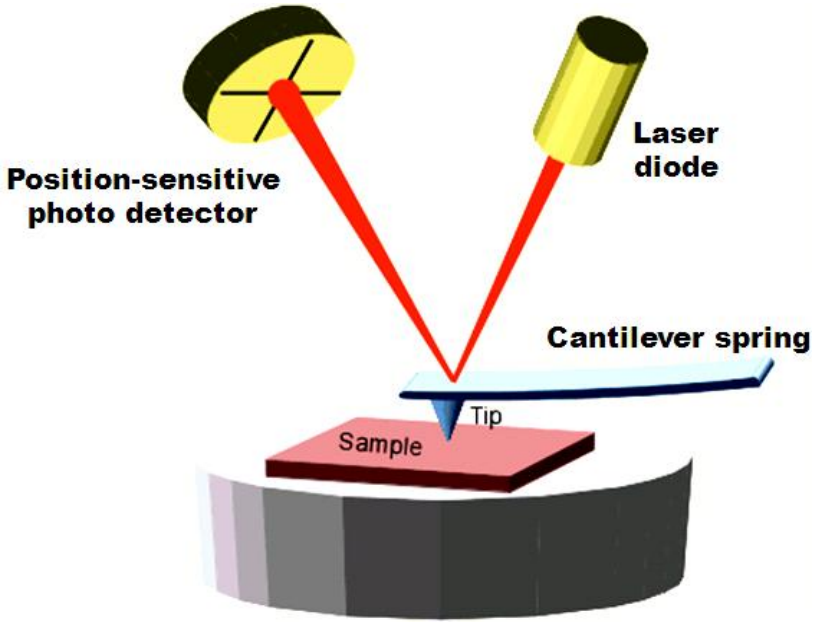


Figure 3.12 Schematic drawing of the basic principle of the AFM.

To measure such small forces one must use not only very sensitive force-measuring springs but also very sensitive ways for measuring their bending. In order to detect this bending, which is as small as 0.01 nm, a laser beam is focused on the back of the cantilever. From there the laser beam is reflected towards a position-sensitive photodetector. Depending on the cantilever deflection, the position of the reflected beam changes. The photodetector converts this change in an electrical signal. An Atomic Force Microscope can reach a lateral resolution of 0.1 to 10 nm. The Figure 3.12 shows a simple schematic drawing of the basic principle of the AFM.

3.9.4 XPS

Principle of XPS (X-Ray Photoelectron Spectroscopy) makes it possible to measure the electrons emitted in an interval of energy according to the binding energy of the electrons. Each chemical element being characterized by a single spectrum, this spectroscopic method makes it possible to precisely analyze the chemical nature of a given material [**17, 18**]. Semi quantitative analyses can be also extracted from normalized XPS spectra while being based on the height of the peaks and surface under the peaks. The identification of the chemical state of an element can be obtained starting from the exact measurement of the position of the peaks and their separation in energy. The Figure 3.13 represents the general diagram of an XPS setup or ESCA.

The basic parts of XPS-system are as follows X-rays tube, Sample, Electronic focusing system, Spectrometer, Electrons detector (channeltron), Data acquisition. The analyzer, which allows a selection in energy of the photoelectrons, consists of two hemispherical electrodes. The potential difference between these two electrodes defines the path energy of the electrons. Only the electrons having a kinetic energy included in an interval of energy centered on this path energy will arrive at the detector. At the end of the analyzer a multiplying detector (channeltron) which makes it possible to create secondary electrons. In our experiment, EDX (Oxford-Link ISIS 300 energy-dispersive X-ray) was used to the analytical elements for the specimen.

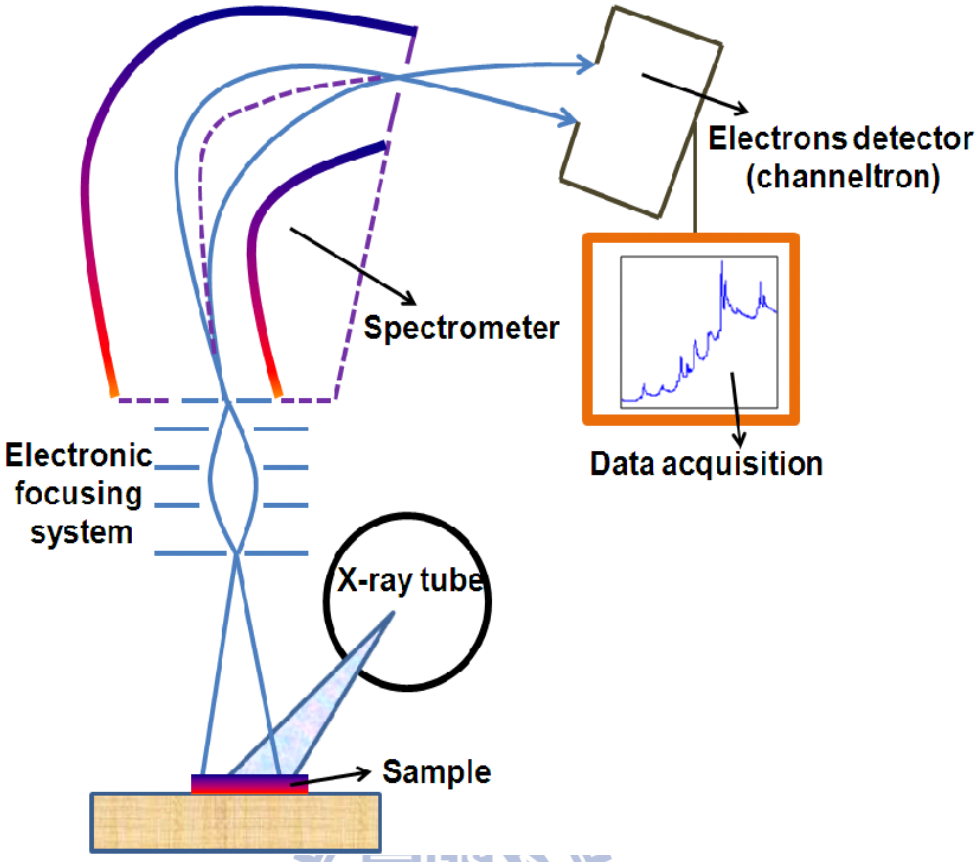


Figure 3.13 General diagram of the basic principle of an XPS or ESCA setup.

3.9.5 XRD

X-ray scattering techniques are a family of non-destructive analytical techniques which reveal information about the crystallographic structure, chemical composition, and physical properties of materials and thin films. These techniques are based on observing the scattered intensity of an X-ray beam hitting a sample as a function of incident and scattered angle, polarization, and wavelength or energy [**19, 20**].

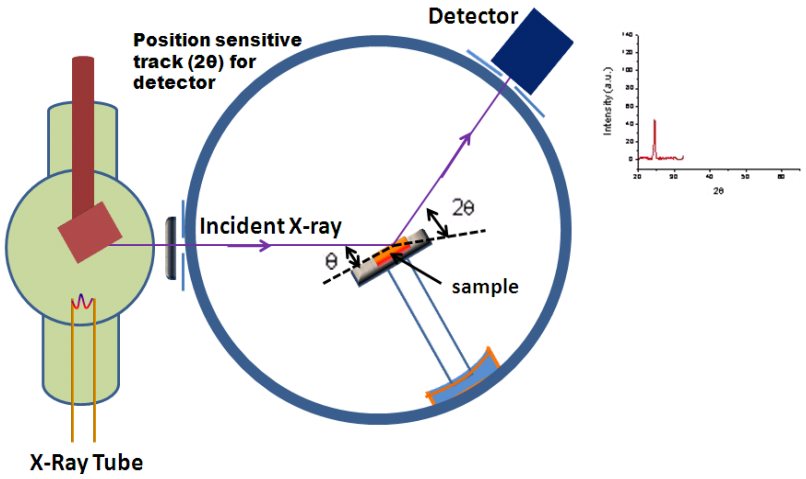


Figure 3.14 General diagram of the basic principle of an XRD.

Figure 3.14 shows a schematic diagram for a X-ray diffractometer, showing the rotating detector. Diffraction occurs at all the angles of 2θ simultaneously in powder or thin film samples. In order to obtain a diffraction pattern, the detector (in most designs) rotates to various 2θ angles to measure diffraction from the sample. The interaction of the incident rays with the sample produced constructive interference (and a diffracted ray) when conditions satisfied Bragg's law ($n\lambda=2d \sin\theta$) [**21**]. These diffracted X-rays are then detected, processed and counted.

3.9.6 FT-IR

The Figure 3.15 represents the general diagram of an FT-IR. Typical photoacoustic Fourier transform infrared (FT-IR) setup for analysis of solid and liquid samples contains an interferometer, a focusing mirror, and a photoacoustic cell. FT-IR interferometer consists of a beamsplitter and two mirrors. The infrared beam is split into two beams: one is reflected from a fixed mirror and one from a moving mirror. By combining the two beams each wavelength of the light is modulated with a different modulation frequency. The combined beam is then focused into the solid or

liquid sample in the photoacoustic cell. The generated photoacoustic signal can be directly transformed into absorption spectrum. Depth-varying information of the sample can be obtained by varying the mirror velocity or phase angle of detection. Typically for polymer materials the depth from where the spectrum is obtained can be varied from few micrometers to about 100 micrometer.

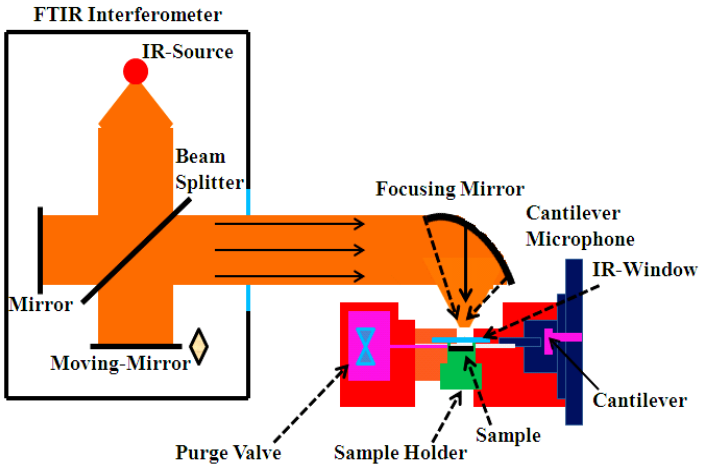


Figure 3.15 General diagram of the basic principle of an FT-IR

3.10 Electrical Measurements

3.10.1 Four-Point Probe System

Figure 10.16 shows our four-point probe apparatus used for electrical characteristic measurements of our flexible transistor and capacitor devices. The system included with a home-built chamber with a microscope inside, a pump to draw out the NO_2, a gas source bottle with mixed air and NO_2, and the Agilent 4156 mainly to detect the conductivity. There is one monitor is also connected to I-V system.

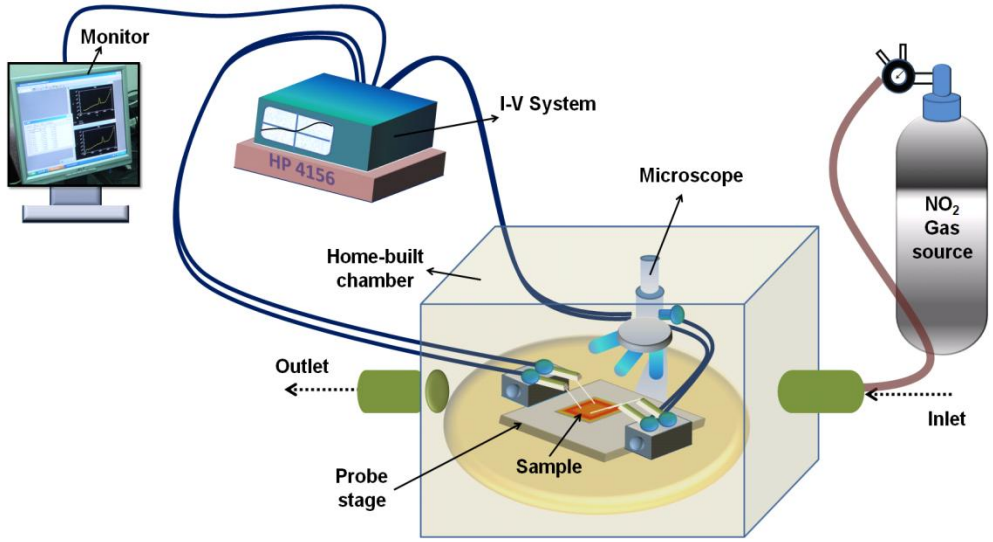


Figure 3.16 General layout of four-point probe station.

The purpose of the 4-point probe is to measure the leakage current (I) and capacitance (C) for dielectric layers in MIM structured device. The output characteristic (source-drain current (I_{DS}) versus drain voltage (V_{DS}) at different gate voltages (V_G)), and transfer characteristic (I_{DS}-V_{DS}) when V_G ranges from 0 to -50V measurements were performed using an Agilent-4156 probe station. It can measure either bulk or thin film specimen, each of which consists of a different expression.

Chapter 4: Improved Reliability from a Plasma-Assisted Metal–Insulator–Metal Capacitor Comprising a High-k HfO_2 Film on a Flexible Polyimide Substrate

4.1 Introduction

Plastic circuits have received growing interest because they combine plastic substrates with new classes of organic materials using low-cost fabrication approaches, such as inkjet printing and liquid film casting [**1, 2**]. They are considered to be a key emerging technology for this century with their potential as an ultralow-cost and light-weight alternative to Si wafers [**3, 4**]. In some instances, they are compatible with continuous, high-speed reel-to-reel fabrication, high mechanical flexibility, transparent to visible/UV radiation, and can allow the circuit board to conform to a desired shape or flex during its use [**5, 6**]. Subsequently, plastic circuits appear to be a foundation for future electronic devices, such as electronic papers, wearable sensors, low-cost smart cards, radio frequency identification tags, and flexible arrays of plastic microphones [**7-9**]. Recently, in terms of their superior bending, it was found that flexible organic transistors can perform better than flexible inorganic transistors [**10, 11**]. Reliability stress testing is very important method for analyzing the bending and stretching properties of flexible devices designed for such applications as accurate sensors for hydrogen [**12**] or for integration into artificial muscles or biological tissues [**13**].

The additional number of steps and high-temperature processing required to

achieve high-performance flexible devices, however, has limited the rate of implementation of semiconductor devices fabricated on flexible organic substrates. In part, this problem can be solved by reducing the transistor size; for example, by reducing the thickness of the SiO_2 gate dielectric in proportion to the shrinkage of the gate length of 70 nm. Nevertheless, such a thin SiO_2-dielectric layer imposes severe constraints on the device performance because this thickness approaches the quantum-tunneling limit and decreases the reliability of a MOSFETs [**14**].

For a small system with scaled-down thickness, the need for advanced materials is progressively focusing on composite systems that maintain or enhance the device performance. To address the issue of the leakage current, hafnium oxide (HfO_2) has become one of the most promising candidate for use as an alternative gate dielectric to replace SiO_2. It exhibits high temperature stability and excellent insulator properties against heat and electricity. HfO_2 is attractive high-k dielectric material with relatively very high dielectric constant (k ~ ca. 25) and wide band gap (ca. 5.68 eV) relative to that of SiO2 [**15, 16**]. Among the various methods for preparing metal oxide film, dc sputtering [**17**], atomic layer deposition (ALD) [**18**], physical vapor deposition (PVD) [**19**], and metal organic chemical vapor deposition (MOCVD) [**20**] appear to be the most useful new technologies. Sol–gel spin-coating is a very efficient approach toward smooth, crack-free films exhibiting excellent surface conformity and uniformity over large areas. In addition, such films can be fabricated at room temperature and normal pressure, obviating the need for high-vacuum systems [**21-23**]. The thin films are produced on a substrate by spin-coating or dip-coating; i.e., a small puddle of the fluid resin is placed at the center of a substrate, which is then spun at high speed (typically ca. 3000 rpm). Dielectric films deposited at low temperature generally exhibit poorer properties and higher degrees of current leakage because of the many traps present

within the film. Hence, high-temperature annealing (at ca. 600–800 ℃) is traditionally required to improve the electrical properties of such thin films [**23**]. Plastic thin PI substrates, however, become damaged at the higher temperatures (≥ 300 ℃) employed during annealing or depositing the film because of their intrinsic low thermal compatibility. Thus, a challenge remains to develop a promising method to overcome these processing limitations. Several researchers have observed that oxygen (O_2) plasma treatment affects the performance of thin films deposited at low temperature through sol–gel spin-coating [**24, 25**]. The electrical properties of such films can improve considerably after O_2 plasma exposure, with enhanced remnant polarization and decreased leakage current density.

In this study, we developed a low-temperature O_2 plasma–enhanced method for preparing a HfO_2 thin film–based MIM capacitor fabricated on a flexible organic PI substrate using sol–gel spin processing. To determine the insulator properties of the film, we determined their current density–electric field (*J–E*) and capacitance–voltage (*C–V*) characteristics. We also investigated the O_2 plasma oxidation growth mechanism in different kinetic regimes to understand the surface oxidation process. Moreover, X-ray photoelectron spectroscopy (XPS) suggested the feasibility of using this low-temperature processing approach toward achieving high-performance flexible devices. A test revealed that the capacitor on the PI surface performed reliably after bending up to 10^5 times.

4.2 Materials and Methods

They were cleaned ultrasonically with ethanol (Fluka; water content: < 0.1%) for 30 min and deionized water for 10 min and then high-pressure N_2 gas was used

to remove the water and any remaining particles from the PI surface. Next, Cr (thickness: 10 nm; adhesion layer) and Au (thickness: 100 nm) were deposited for the gate electrode over the PI substrate using a thermal coater. To deposit the high-k HfO_2 film, a sol–gel solution was prepared by dissolving $HfCl_4$ (98%, Aldrich, USA) in ethanol (95%) at a suitable concentration. We added ethanol (10 mL) as the solvent to yield a molar ratio of $HfCl_4$ to C_2H_5OH of 1:1000; after adding a magnetic stirrer, the solution was heated under reflux while stirring for 30 min. The film was grown by spin-coating the sol–gel solution over PI at 3000 rpm for 30 s at room temperature using a Clean Track Model-MK8 (TEL, Japan) spin coater. The as-prepared samples were treated with O_2 plasma for 2 min in oxygen plasma reactor (Harrick Scientific Corp.), which supplied a plasma power of 30 W; subsequent annealing was performed in the presence of O_2 at 250 ℃ for 12 h (refer, OPT/A). Finally, 300 nm–thick Al films were patterned as the top electrodes using a shadow mask and a thermal coater.

The surface morphology of the high-k HfO_2 film over PI was evaluated using scanning electron microscopy (FE-SEM, JOEL JSM-5410, operated at 5 kV) and atomic force microscopy (AFM, Digital Instruments Nanoscope, D-5000) at a scan size of 2 μm × 2 μm and a scan rate of 1 Hz. We used ellipsometry techniques to measure the thickness of the HfO_2 film. We used XPS to analyze the chemical bonding of the elements of interest under various treatment conditions. To characterize the leakage currents and capacitances of the films, we prepared them in MIM configuration represented in Figure 4.1 (a).

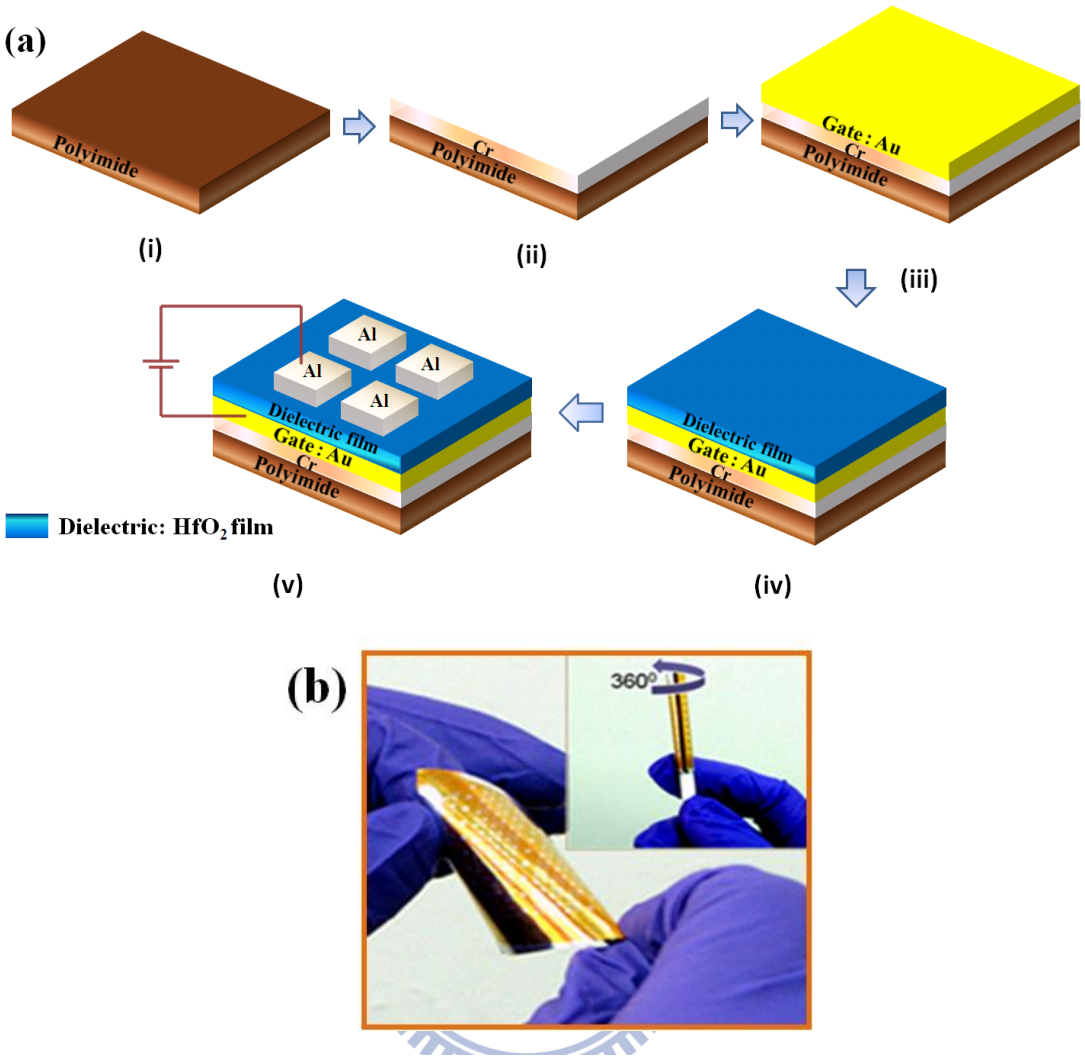


Figure 4.1 (a) Schematic representation of an MIM capacitor featuring a high-k HfO_2 thin film on a PI substrate in fabrication steps (i-v); (b) Photograph of our MIM capacitor on the flexible ultra-thin PI substrate; inset: unlimited bend test up to an angle of 360° angle.

The *J*–*E* measurements were performed using an Agilent-4156 probe station; the capacitance was measured using an HP-4284A *C*–*V* analyzer. Figure 4.1 (b) displays a photograph of the flexible capacitor device on a 30 μm–thick PI substrate under a large surface strain, but without any cracks appearing on the surface; the inset reveals the bending characteristics of this capacitor with unlimited fold-up to an angle of 360°. Thus, it is possible to apply a large mechanical strain to the devices fabricated onto the plastic substrate to evaluate

their test strain. A customized bending machine (depicted and described in detail elsewhere in this text) was used to perform bending tests with the flexible MIM capacitor device.

4.3 Results and discussion

4.3.1 Film Quality and Surface Roughness

The HfO_2 film was prepared by spin-coating a sol–gel mother solution onto the chromium (Cr) coated flexible PI substrate used as a gate insulator layer. Cr was used to make firm adhesion between PI and sol-gel derived HfO_2 film [**26**]. Figures 4.2 (a) and (b) present top-view SEM images of the as-deposited, sol–gel spin-coated films after baking at 80 ℃ and annealing at 250 ℃ for 12 h. Many trap states are present over both film surfaces, suggesting that they would directly affect the electrical performance of the device. When O_2 plasma pretreatment was employed for 2 min on the as-grown sol–gel film and then annealing was performed at 250℃ for 12 h (abbreviated as OPT/A), a clean surface was generated. Figure 4.2 (c) displays the well-ordered, smooth, and crack-free HfO_2 film that was grown successfully on the PI substrate. The surface roughness of the insulator layer is another important factor affecting the performance of MOS devices. Here, we used tapping-mode AFM on a length scale of 2 μm × 2 μm to determine the surface roughness of the film. Figure 4.2 (d) indicates that the surface roughness of the film surface of the sample treated with OPT/A was 1.43 nm. The thickness of HfO_2 film subjected to OPT/A-treatment was measured to be 10 nm using ellipsometry techniques.

4.3.2 Effect of O_2 Plasma on HfO_2 Thin Film Formation

We measured the quantitative leakage current and capacitance to evaluate the

dielectric performance of the high-k HfO_2 film in the MIM configuration. Figure 4.3 (a) displays the *J–E* characteristics for flexible MIM capacitors prepared under various sample treatment conditions. The as-deposited samples that were baked at 80 ℃ and annealed in the presence of O_2 at 250 ℃ for 12 h did not have sufficiently high thermal budgets and, thus, their breakdown electric fields were relatively low and their leakage current densities were very high (1.69×10^{-5} and 1.59×10^{-7} A cm^{-2}, respectively, at an applied voltage of 5 V). The leakage current density was 3.64×10^{-9} A cm^{-2} for the sol–gel-deposited HfO_2 film subjected to OPT/A treatment conditions. The baking-only treated HfO_2 film exhibited the largest leakage current among these treated films because it had poor dielectric characteristics and numerous

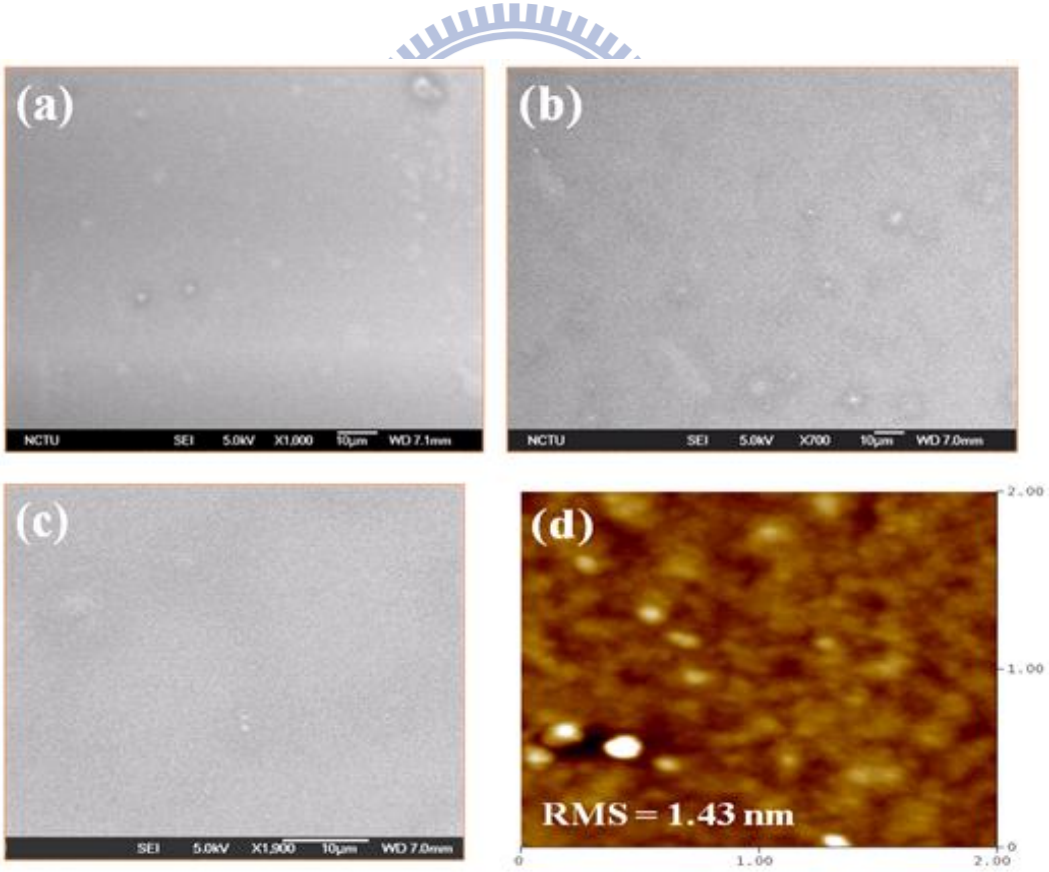


Figure 4.2 (a-c) Top-view SEM images of as-deposited HfO_2 films on Cr/PI substrates after (a) baking, (b) annealing at 250℃ for 12 h, (c) sequential O_2 plasma treatment and annealing at 250℃ for 12 h (OPT/A), (d) Tapping-mode AFM image of the film subject to OPT/A-

treatment.

traps present within the film. A slight improvement in the electrical characteristics occurred for the annealing-only treated sample. The leakage current density decreased when the sample was treated with O_2 plasma for 2 min and then annealed at 250 ℃ for 12 h, indicating that the poorer leakage properties of the other two treated samples arose because of the existence of numerous traps over their film surfaces. The breakdown electric field (ca. 2.3 MV cm^{-1}) also increased when the sample was subjected to the OPT/A treatment conditions. The OPT/A-treated sample exhibited excellent electrical characteristics on the PI substrate because (i) the wet hafnium film underwent a high degree of oxidation under O_2 plasma treatment and (ii) subsequent annealing led to a reduction in the number of traps. The low leakage current of our flexible MIM capacitor is comparable with that of silicon- and glass-based capacitor devices [**27**-**29**].

To understand the carrier transport mechanisms of the OPT/A-treated hafnium dielectric film, Figure 4.3 (b) presents a plot of ln(J) with respect to the square root of the applied electric field ($E^{1/2}$). For standard Schottky–Richardson (SR) emission, the plot of ln(J) versus $E^{1/2}$ should be linear; can be expressed as[30]

$$J = A^{*}T^{2}\exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0})}{KT}\right] \tag{4.1}$$

Where, A^{*} is the effective Richardson constant, $q\phi_B$ is the Schottky barrier height, ε_0 is the permittivity in a vacuum, and ε_r or (k) is the dynamic dielectric constant of HfO_2. SR emission induced by the thermionic effect is caused by electron transport across the potential energy barrier, as indicated in the inset to Figure 4.3 (b); it is

independent of traps and dominates the conduction mechanism [**31**]

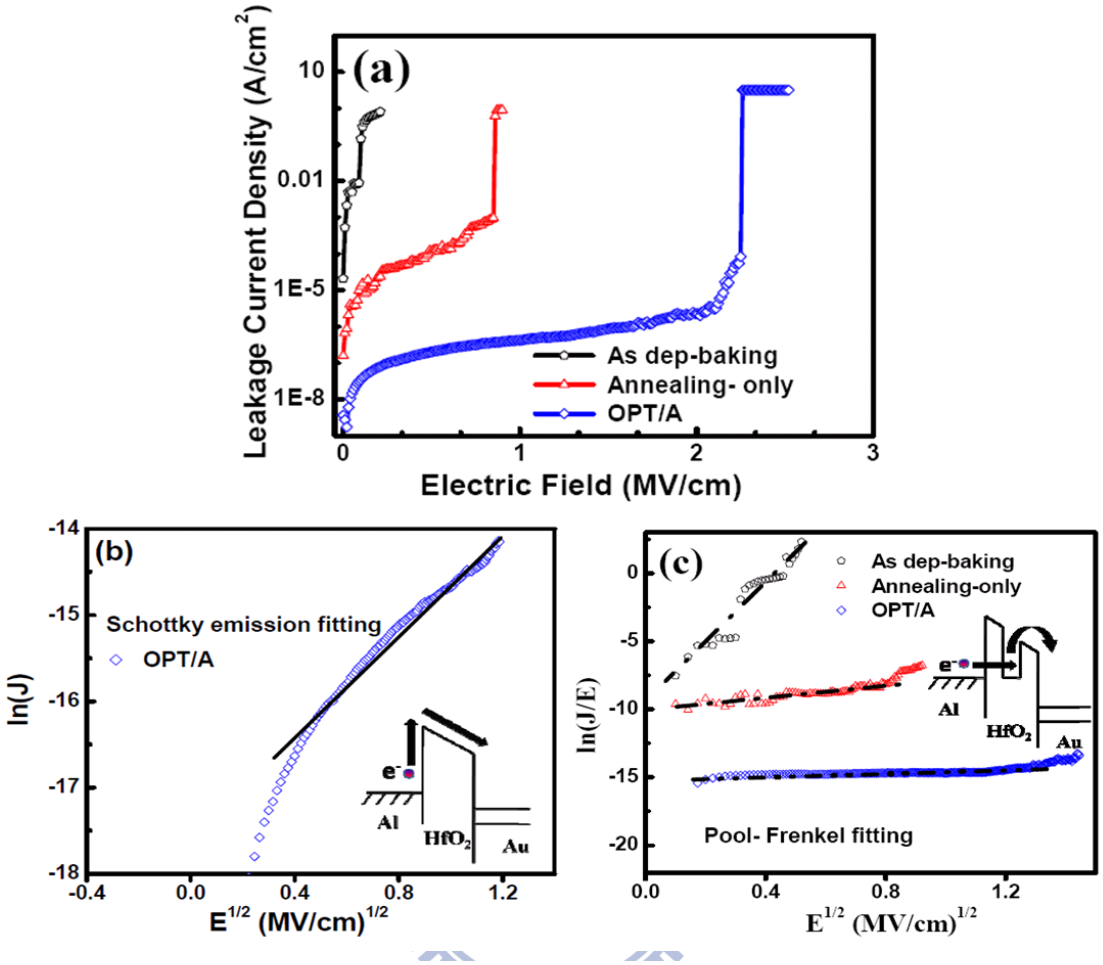


Figure 4.3 (a) Plots of leakage current density versus electric field under an applied positive voltage for samples prepared using all three treatment conditions. (b) Plot of ln(*J*) versus the square root of electric field ($E^{1/2}$) for the OPT/A-treated sample. (c) Plot of ln(*J*/*E*) versus ($E^{1/2}$) for the three samples. The corresponding schematic energy band diagram is presented to explain the S-R and P-F emissions.

The conversion of the current transport mechanism from trap-assisted tunneling for the as-deposited and annealing-only samples to SR emission for the OPT/A sample demonstrates theoretically that the sol–gel hafnium film was oxidized and traps were completely terminated. Figure 4.3 (c) presents plots of ln(*J*/*E*) versus $E^{1/2}$ for the baking, annealing, and OPT/A-treated HfO_2 films; the inset displays a schematic energy band diagram that elucidates the leakage transport mechanisms. It is

believed that the Poole–Frenkel (PF) emission is due to field-enhanced thermal excitation of trapped electrons in the bulk of the insulator. The conduction process at higher voltages is likely due to the PF emission [**32**], which is described by the equation

$$J = CE\exp\left(\frac{-q\phi_t}{kT}\right)\exp\left[\frac{1}{r\,k\,T}\sqrt{\frac{q^3}{\pi\varepsilon_0 K_T}}\sqrt{E}\right] \tag{4.2}$$

where C is a constant, q, k, T, and E represent the electronic charge, the Boltzmann constant, the temperature, and the electric field, respectively, ε_0 denotes the permittivity of free space, K_T is the high-frequency dielectric constant (square of the refractive index), and ϕ_t is the energy barrier separating the traps from the conduction band. The coefficient r is introduced in the expression to take into account the influence of the trapping or acceptor centers ($1 \leq r \leq 2$). As a result, the plot of $\ln(J/E)$ as a function of $E^{1/2}$ in Figure 4.3(c) reveals that the as-deposited baking- and annealing-only samples possessed huge numbers of traps, which decreased the band gap in the HfO_2 films because the thermal budget was insufficient to form dense and trap-free dielectric layers. For the as-deposited sample, the linear dependence began at a very low electric field (ca. 0.2 MV cm^{-1}). The traps within the HfO_2 film were not reduced after baking-only treatment; the device featured a high leakage current and a low breakdown electric field. For annealing-only sample, the traps inside the HfO_2 films had been reduced and the current transport mechanism was improved from trap-assisted tunneling to FP emission, but this improvement remained less obvious and resulted in poorer dielectric properties. Under treatment with O_2 plasma, the PF emission was gradually restrained. Finally, the current transport mechanism was replaced by SR emission after OPT/A treatments of the as-grown film. These findings

confirm that the number of traps was minimized within the low temperature–deposited HfO_2 film after plasma treatment.

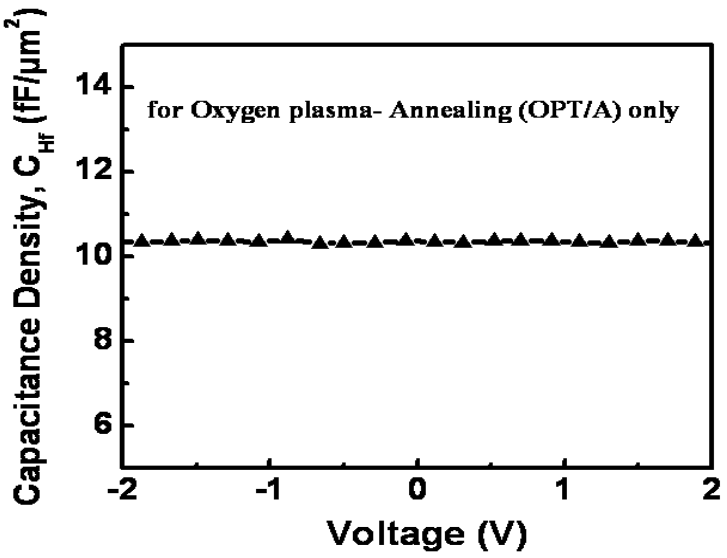


Figure 4.4 Plot of capacitance density (*C*) as a function of the applied voltage (*V*) for the OPT/A-treated capacitor device.

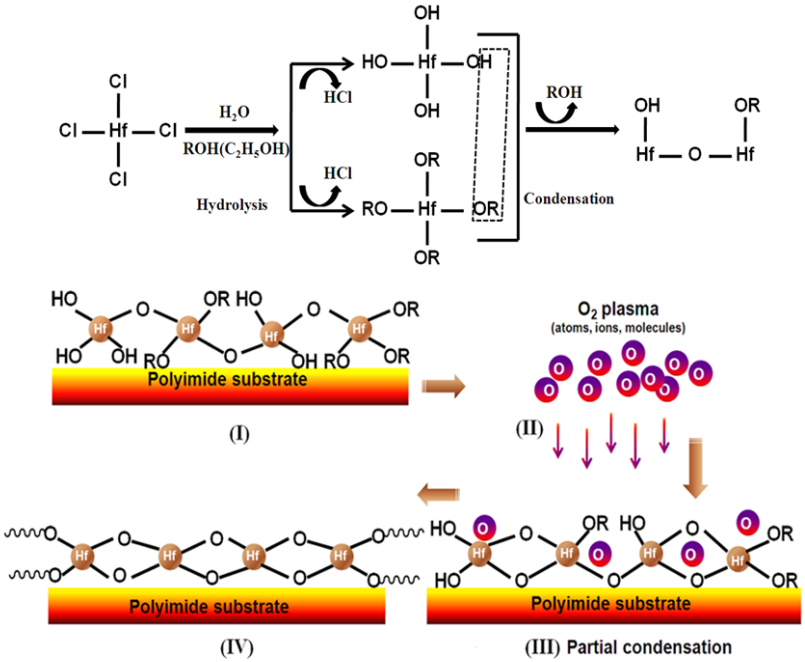


Figure 4.5 Schematic representation of the O_2 plasma growth mechanism for sol-gel-derived spin-coated HfO_2 film.

Figure 4.4 displays the *C–V* characteristics of our flexible MIM capacitor. Here, we have only measured the capacitance density for the OPT/A-treated HfO_2 film; the maximum measured capacitance density was 10.35 fF μm^{-2} at 1 MHz. The high capacitance of this low temperature–deposited HfO_2 film after OPT/A treatment would allow its future flexible electronic devices to be operated in the low voltage regime. In addition, according to the capacitance and thickness data, we estimated the dielectric constant (k) of the HfO_2 film to be 11.7. The observation of the calculated value of k is lower than that of pure HfO_2 film, but consistent with the previous results for calculated dielectric constant of sol-gel derived HfO_2 films [**33-35**]. The calculated value of k is sharply decreased as the film thickness is very low (~ 10 nm) by means of Lorenz's local field theory [34]. However, the k value for our sol-gel derived flexible capacitor is still higher than that of SiO_2 on silicon wafer (k = 3.8). Thus, one approach is the use of materials with dielectric constants higher than that of SiO_2 materials as thin-film dielectric materials, whereby the HfO_2 dielectric materials with dielectric constants of about 11.7 or above, demonstrate the possibility to replace the conventional SiO_2-based materials.

We used a plasma oxidation growth mechanism at low temperature to examine the influence of O_2 plasma on the as-deposited hafnium film. It was expected that there would be a direct interaction of active atoms and molecules in the plasma (O^+, O^- O, O_2, free electrons, etc.) with organic species in the sample [**36**]. The sol–gel solution comprising $HfCl_4$ dissolved into alcohol and was coated over the flexible PI substrate. Figure 4.5 displays the possible chemical transformation, the hydrolysis and condensation reactions with an exothermic elimination of HCl; which also includes decomposition_reactions for O_2 plasma on the as- deposited sol–gel film. In (I) step, the as-deposited film existed in the solid-state, presumably

with a HO–Hf–O–Hf–OR model structure based structure. It appeared that an homogeneous network of –O–Hf–O–Hf–O– bonds had not developed in the thin film. In (II & III) steps, the power plasma induced the formation of some active oxygen species that reacted with model structure of HO–Hf–O–Hf–OR, resulting in partial oxidation to hafnium oxide. The imposing plasma gradually oxidized the as deposited thin film. In the final step (IV), the film surface was near-complete oxidation to $–(O–Hf–O)_n–$ using plasma oxidation; the organic part were mostly removed. Oxidation through O_2 plasma treatment of the thin film was occurred at low temperature than conventional high-temperature annealing on thin film; this process allows high-performance electronic devices to be fabricated on plastic substrates.

To obtain a better understanding of the O_2 plasma effect, we used XPS analysis to examine the chemical composition of the films obtained under different treatment conditions. Figure 4.6 displays high-resolution spectra of the Hf 4f energy levels of the three samples. The spectra were deconvoluted into two spin-orbit doublet peaks for the Hf $4f^{7/2}$ and Hf $4f^{5/2}$ energy levels at different binding energies of the Hf–O bonds. For the baking-only treatment (Figure 4.6 (a)), the peaks for the $4f^{7/2}$ and $4f^{5/2}$ binding energies were detected at 16.1 and 17.6 eV, respectively. After annealing-only treatment (Figure 4.6 (b)), these binding energies were raised to 16.4 and 17.9 eV, respectively. Furthermore, excellent advancement of the O–Hf–O bonds was achieved through O_2 plasma treatment (Figure 4.6 (c)), the binding energies of $4f^{7/2}$ and $4f^{5/2}$ were raised to 16.8 and 18.5 eV, respectively; fit well more likely to previous studies [**37, 38**]. Compared to the as deposited sample, the Hf 4f spectra of the plasma treated HfO_2 film is shifted roughly 0.7 eV to the higher binding energy (BE). The shift toward higher BE for the Hf–O bonds suggests that oxygen plasma treatment introduced

some bonding structures [i.e., $-(O-Hf-O)_n-$ units] for the complete oxidation of the Hf atoms [**39**]. Figures. 4.6 (b) and 4.6 (c) imply that O_2 molecules reacted

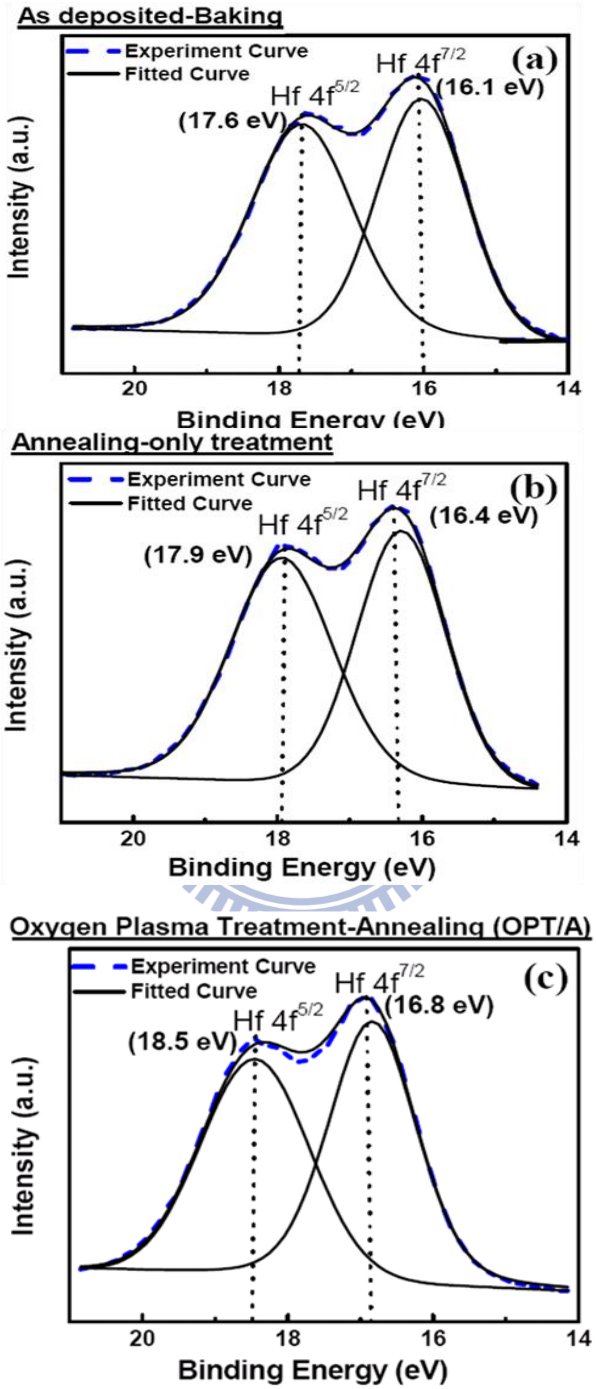


Figure 4.6 High-resolution XPS spectra of the Hf 4f energy levels for as-deposited HfO_2 films subjected to (a) baking, (b) annealing at 250 ℃ for 12 h, and (c) OPT/A-treatment. The dotted curve represent the experimental data; solid curves represent the fitted peaks

and the summarized results of the fitted data.

with the Hf dangling bonds (or traps) to form stronger Hf–O bonds and that subsequent annealing in the O_2 plasma effectively transported O_2 molecules into the HfO_2 film to passivate the traps. In addition, we recorded the low-resolution XPS spectra for the Hf 4f bonds for HfO_2 film subjected to as-prepared, annealing and OPT/A-treatment conditions to examine its chemical composition. Figure 4.7 (a) displays the spectrum of the as-deposited film with a broad O(1s) peak at around 531 eV and the O(1s) peak for annealed-only sample at around 532.3 eV. In the as-deposited film, the intense C(1s) peak at around 286.6 eV is attributed to C-O-H from the ethanol solvent. This observation is in excellent agreement with the reported literature value [**40**]. The C(1s) peak for annealed sample is at around 285.0 eV and band intensity significantly decreases than the as deposited film due to solvent evaporation.

Figure 4.7 (b) reveals that the sample consisted of hafnium, oxygen, and a small amount of contaminating carbon; no other impurities (e.g., chloride ions) were present on the film surface. This good composition is similar to those reported previously [**14, 41**]. We calibrated the binding energies by setting the residual C(1s) peaks at 284.6 eV and 288.0 eV, and the O(1s) peak at 533.9 eV. We find the band intensity of O(1s) peak remains strong and C(1s) peak decreases upon plasma treatment. The existence of low intense C(1s) peak can be attributed to a partially oxidized carbon species with a slight peak broadening, since the oxygen atoms bond to a portion of carbon. The peak appeared at the higher BE of 288.0 eV is due to C–O related bonding as shown in inset of Figure 4.7 (b). Although, the C(1s) peak at 284.6 eV may be associated with (C–H) bond (Inset: Figure 4.7 (b)), and it remains unchanged even after plasma treatment. It indicates the availability of

residual carbon species is still found over the film. This spectroscopic result reveals that

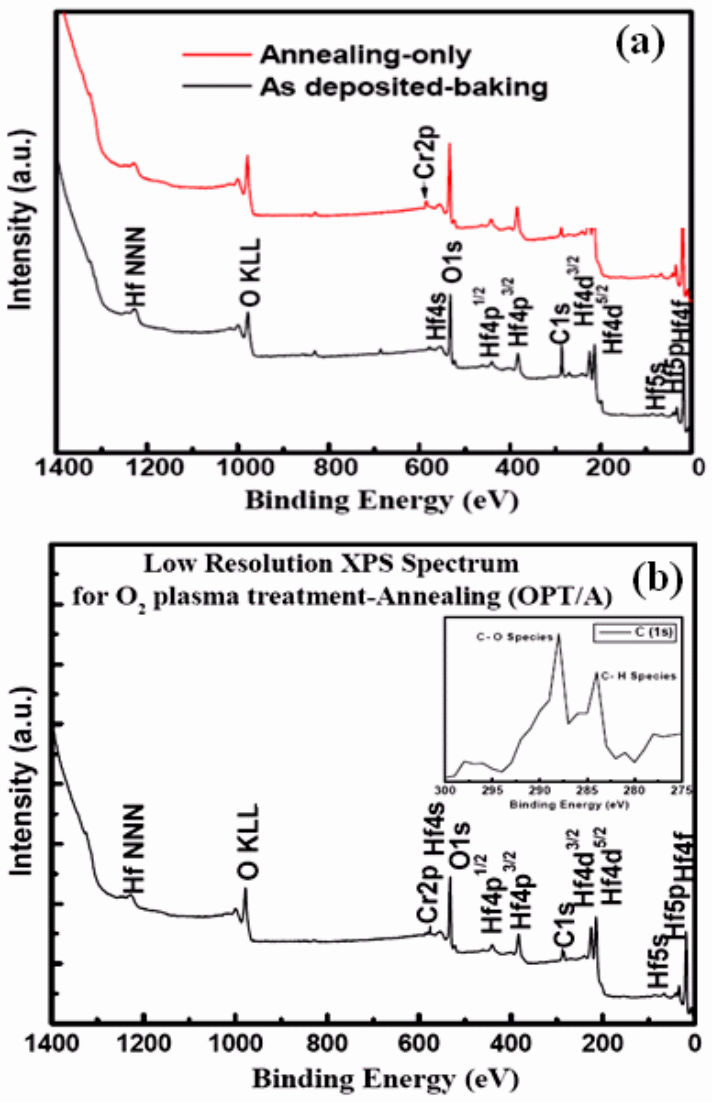


Figure 4.7 (a) Low resolution XPS spectra of sol-gel deposited HfO_2 film on Cr/PI substrate for as deposited-baking and annealing at 250℃ treated samples. (b) Low resolution XPS spectrum of the OPT/A-treated HfO_2 film on the PI substrate. **Inset**: XPS spectra in the BE regions of C (1s).

the content of defects was much reduced after subjecting the sample to OPT/A treatment and subsequent annealing to form the complete composite oxide hafnium film (i.e., HfO_2). The XPS analysis confirms the chemical reaction of the HfO_2 film

prepared through the O_2 plasma–induced transformation of the sol–gel-derived thin film. This approach possesses one particular advantage over other standard plasma oxidized technologies: it provides a higher rate of oxidation of the wet-state of the film at lower treating temperatures.

4.3.3 Bending Treatment for Mechanical Flexibility and Stability

Figure 4.8 displays the leakage current densities for the OPT/A-treated HfO_2 films subjected to four different bending times. We measured the leakage currents prior to bending treatment to understand the performance of the initial MIM capacitor, revealing that the HfO_2 film exhibited superior electrical performance. The film retained its low leakage current density (ca. 10^{-9} A cm^{-2}) after bending the device 10^3 or 10^5 times. All of the curves overlapped, with no further increments in the leakage current density for either positive or negative biasing conditions after bending the capacitor up to 10^5 times. Indeed, the HfO_2 film over PI exhibited superior reliability after bending the device. The photograph in the inset to Fig. 8 displays our homemade bending machine and our flexible capacitor under an applied strain; the counter of the number of bends and the set time is also indicated. After performing the bending test, the breakdown field (E) remained the same as it was prior to bending (ca. 2.25 MV cm^{-1}), indicating that using the spin-coating process to form the HfO_2 films provides superior electrical characteristics and reliability for the MIM structure. Again, we conclude from this result that the performance of our flexible-base capacitor device is comparable to that of silicon and glass-based capacitor devices, even after folding or bending the sample unlimitedly. To the best of our knowledge, there are no parallel reports describing reliability tests of flexible capacitors employing HfO_2 films as insulator

layers that exhibit satisfactory electrical properties.

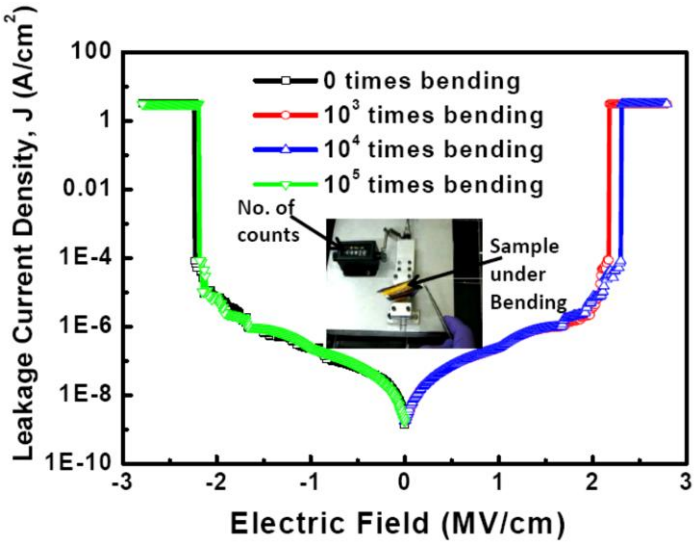


Figure 4.8 Leakage current density plotted as a function of the electric field, measured at both negative and positive biased voltages, for the OPT/A-treated flexible MIM capacitor after being subjected to repeated bendings for various times.

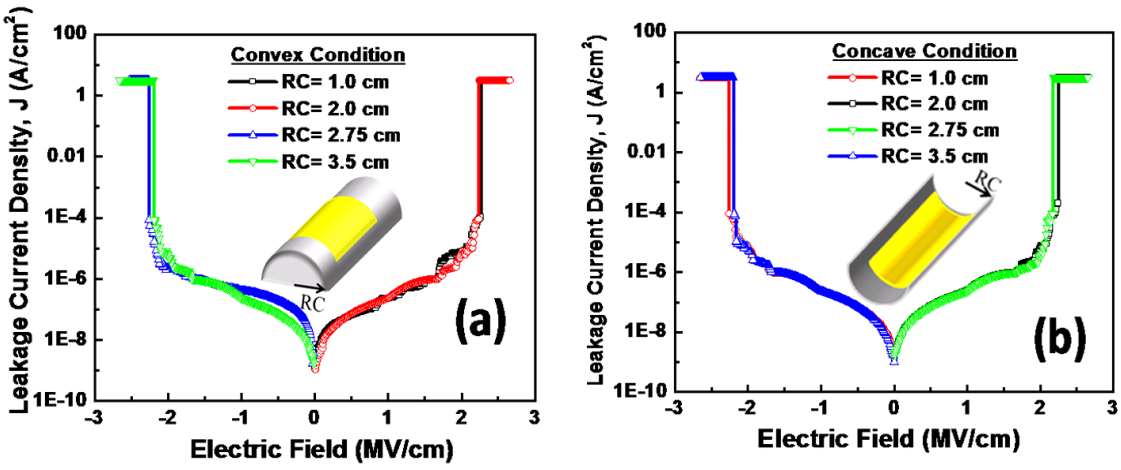


Figure 4.9 Leakage current density measurements for (a) convex and (b) concave devices; radii of curvature (RC) were varied from 1 to 3.5 cm.

We tested two additional features of our sol–gel-derived capacitor on a

flexible substrate to explore its feasibility for use in practical applications. Namely, we measured the current density in both convex (Figure 4.9 (a)) and concave (Figure 4.9 (b)) settings, varying the radii of curvature (R_C) from 1 to 3.5 cm. During the manufacturing process, a foil was used as a substrate support to provide these specific bending conditions. We observed the electrical characteristics, such as the leakage current density ($<10^{-8}$ A cm^{-2}) and breakdown field (ca. 2.25 MV cm^{-1}) under both negative and positive biasing conditions. The sol–gel-derived HfO_2 film obtained after OPT/A treatment behaved as a stable electrical insulator, even after bending the device at the different radii of curvature. Under the R_C (3.5 cm) concave conditions, the change in the thickness of the film, relative to that of the flat device, was ca. 0.00001%. Thus, we conclude that the thickness of the HfO_2 film remained unchanged when the device was subjected to 3.5 cm concave- or convex-type bending conditions. Even when the sample was bent under R_C (1 cm) concave conditions, the variation in the HfO_2 film thickness was only ca. 0.0001%. Bending led to nearly no changes in the electrical characteristics under the various RC concave or convex conditions. The low deviations in leakage current density ($<10^{-8}$ A cm^{-2}) upon bending between 1 and 3.5 cm reveal that no clear trend can be attributed to repeated driving under either set of conditions.

4.4 Summary

We have prepared MIM-structured capacitors using ultrathin 10-nm high-*k* HfO_2 films deposited through sol–gel spin-coating on flexible PI substrates. The material properties and electrical performances of these films verified the effectiveness of applying low temperature plasma processing to the fabrication of future soft devices. The HfO_2 film exhibited a low leakage current density of 3.64

$\times 10^{-9}$ A cm^{-2} at 5 V and a maximum capacitance density of 10.35 fF μm^{-2} at 1 MHz. The electrical behavior analyzed under various bending treatment conditions revealed that our flexible capacitor functioned independent of the bending conditions (i.e., the number of bends and the bending radii). The electrical characteristics of our flexible MIM capacitors suggest are comparable with those of silicon- and glass-based capacitor devices, even after bending the devices up to 10^5 times. We believe that amorphous high-k HfO_2 is a leading candidate for use in future flexible devices as a stable gate dielectric fabricated through processing at low temperatures.

Chapter 5: Highly Reliable Si_3N_4-HfO_2 Stacked Heterostructure to Fully Flexible Poly-(3-hexylthiophene) Thin-Film Transistor

5.1 Introduction

Rapid progress in the performance of organic thin film transistor (OTFT) devices has positioned the technology as a potential replacement for many portable electronic applications. The flexible organic TFTs have potential advantages because of their use in a new class of applications such as radio-frequency identification tags, light-emitting diodes, wearable sensors, smart cards and other types of signal conditioning and processng functions [**1-3**]. Literatures have been envisioned and demonstrated: owing to excellent thermal stabilty and mechanical flexibility, PI has been considered as one of the most attractive organic flexible substrate [**4, 5**]. Room temperature manufacturing is the highly important issue for plastic device and will widen bendable device application for future transparent and flexible microelectronics. The HfO_2 film has been reported to be scalable to below 1 nm, but there still exist several issues that need to be tackled before they can eventually replace SiO_2 dielectric for flexible electronics [**6**].

A challenge remains to develop a low-cost and promising method to overcome room temperature processing and device reliability limitations. As to the silicon-based devices, a potential film of silicon nitride (Si_3N_4) has been proposed

to play an important role on passivation and improve the growth film's quality [**7, 8**]. The large area issue for the low cost of solution-based manufacturing on inorganic or organic substrate has been enabled by the use of conducting or semiconducting polymers [**4-8**]. Their compatibility with plastic substrates makes it possible to create flexible, lightweight, and portable electronic devices. Among many soluble polymers, regioregular poly(3-hexylthiophene) (P3HT) has been extensively studied in organic field-effect transistors (OFETs) due to its comparatively high hole carrier mobility, simple solution processability, and commercial availability [**4**]. However, P3HT-based OFETs typically face the problem of relatively poor ambient stability and unfull flexibility, which has strongly limited its practical application for industry. The bending stability in relation to above device reliability is also one of the most challenging issues for choosing the suitable device structures towards fully flexible electronic device application.

In present study, we attempt to use the Si_3N_4 as passivation layer on the plasma treated HfO_2 film enable one to obtain reliable OTFT on a fully flexible PI substrate, as regards their mechanical flexibility and environmental stability. The device's electrical properties with respect to saturation mobility, on/off current ratio, and bending conditions (i.e., the numbers of bending times and the bending radii) are also carefully investigated.

5.2 Materials and Methods

Plastic 30 μm-thick DuPont Kapton® PI films were used as flexible substrates for device fabrication process. They were cleaned ultrasonically with ethanol (Fluka; water content < 0.1%) for 30 min and deionized water for 10 min, and then high-pressure N_2 gas was used to remove the water and any remaining surface

particles from the PI. PI films were annealed at 200 ℃ for 2 h in vacuum to achieve relatively thermal stable, and enhance the adhesion strength. Next, Cr (thickness: 50 nm; adhesion layer) and Au (thickness: 100 nm) films were sequentially deposited for the gate electrode over the PI substrate by using a thermal evaporation system under patterning with designed mask. To deposit the HfO_2 dielectric layer, a sol-gel solution was prepared by dissolving $HfCl_4$ (98%, Aldrich, USA) in ethanol (95%) at a suitable concentration. Ethanol (10 mL) as the solvent was prepared to yield a molar ratio of $HfCl_4$ to C_2H_5OH of 1:1000. Under a magnetic stirring condition, the solution was heated under reflux while stirring for 30 min. The dielectric film was grown by spin-coating the sol-gel solution over PI at 1000 rpm for 10 s and then 3000 rpm for 30 s at room temperature by using a spin coater. The as-prepared samples were treated with O_2 plasma for 2 min in an oxygen plasma reactor (Harrick Scientific Corp.), which supplied a plasma power of 30 W. The silicon-nitride (Si_3N_4) layer was deposited as a passivation layer onto the high-*k* film by plasma-enhanced chemical vapor deposition (Oxford-PECVD).

To deposit the channel layer, the commercially available poly-(3-hexylthiophene) i.e., P3HT (obtained from Merck) was used as an organic semiconductor layer. The desired solution was prepared when 1.2 mg P3HT were obtained and placed in a sealable clean glass container. Then, 10 mL of $CHCl_3$ was added to a flask containing the P3HT. The solution was then gently heated at 50 ℃ using a hot plate to further break down the polymer chains in solution. After stirring the solution with reflux for 1 h, and then placed in an oven to be cooled. The light intensity was shielded under a standard aluminum foil to minimize the oxidation. The organic semiconductor layer of mixed solution was fabricated by spin-coating a P3HT chloroform solution at 1000 rpm for 20 s. After the deposition, the film was dried at 80 ℃ for 2 min and then dried gel film was

annealed in nitrogen atmosphere using different thermal treatment techniques for 1 h. Au electrodes (100 nm) for TFT devices on the PI sheet with a device structure as shown in Figure 5.1 (a) were formed through a shadow mask by using a thermal coater. The molecular structure of the P3HT was shown on right-side of Figure 5.1(a). The channel width (W) and length (L) for our flexible device were 200 and 60 µm, respectively. Figure 5.1 (b) illustrated the semi-transparent images of 30 µm-thick DuPont Kapton PI film, demonstrating the text on the layer behind the PI substrate was clearly visible. Our P3HT-TFT device on plastic PI film under a large surface strain was displayed in Figure 5.1 (c), and the surface appeared no cracks.

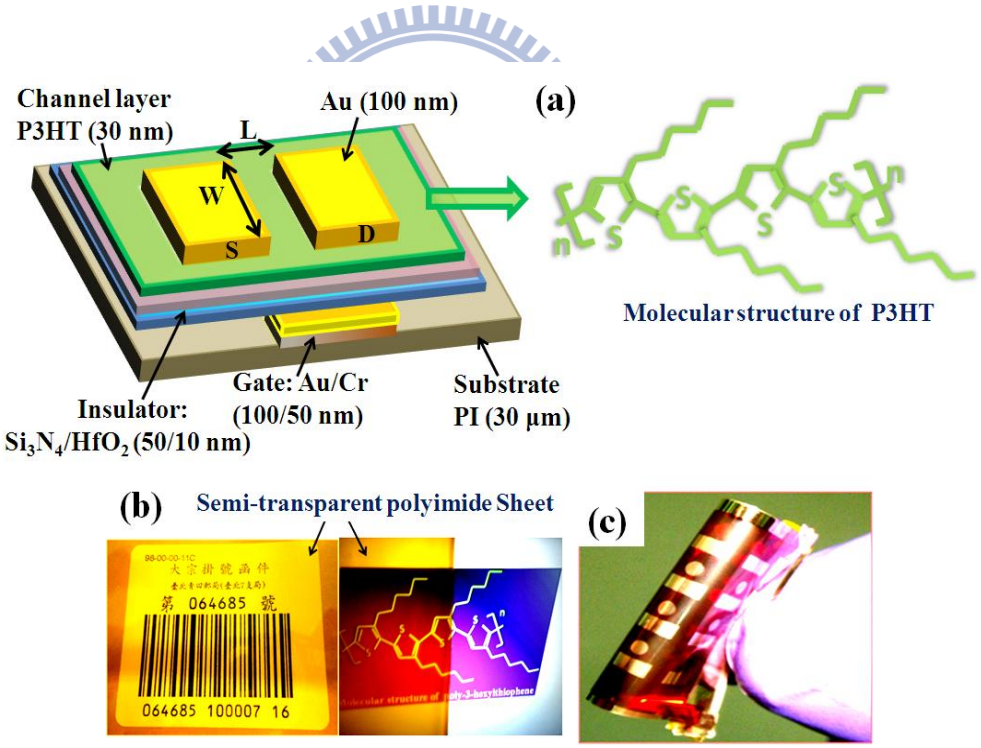


Figure 5.1 (a) Schematic structure of P3HT-based OTFT with HfO_2-Si_3N_4 as a dielectric layer on PI substrate; (b) the photograph of semi-transparent polyimide sheet; (c) photograph of proposed TFT device on a 30 µm-thick flexible PI substrate and under a large surface strain.

The surface morphology of the high-k HfO_2 and passivation layer Si_3N_4 films over PI was evaluated using atomic force microscopy (AFM, Digital Instruments Nanoscope, D-5000) at a scan size of 1 μm and a scan rate of 1 Hz. The surface morphology of the P3HT film as channel area on Si_3N_4–HfO_2/Au/Cr/PI substrate by AFM measurement in tapping mode at 2 μm scan size and a scan rate of 0.5 Hz. We used ellipsometry technique to measure the thickness of the HfO_2 and P3HT layers. The current density-electric field (*J-E*) measurements were performed by using an Agilent-4156 probe station. A customized bending machine (depicted and described elsewhere in this text) was used to perform the bending test in tension or compression modes where the bending radious ranged from 2 to 4 cm for both convex and concave types of bending.

5.3 Results and Discussion

5.3.1 Effect of passivation layer on leakage-current density

Prior to achieve the flexible organic-inorganic hybrid TFT devices based on P3HT material, we firstly fabricated the MIM device with 10 nm high-*k* HfO_2 as dielectric layer over fully flexible PI substrate. Under high electric field stress, the carriers of leakage current will impact the weak bonding and result in the high leakage current. We measured the quantitative leakage current to evaluate the electrical performance of the HfO_2 film which was fabricated by very simple and cost-effective sol-gel spin-coating technique in MIM configuration. Figure 5.2 (a) displayed the leakage current density and electric field (*J-E*) characteristics for the fully flexible MIM capacitors prepared by HfO_2 film with O_2 plasma treatment. The O_2 plasma treated sample did not have sufficiently high thermal budgets and many trap states still existed over film surface. Inset of Figure 5.2 (a) showed

AFM image of HfO_2 film with existance of numerious trap states over film surface. The RMS roughness was about 1.52 nm. Hence, their breakdown electric field was relatively low and their leakage current density was very high (i.e. 4.6×10^{-6} A cm^{-2}) at the applied voltage of 1 V. This observation was attributed to the availablity of the traps over film surface. In order to achieve the better device, the Si_3N_4 passivation layer was proposed to deposit onto the HfO_2 film in Figure 5.2 (b). Interestingly, the surface roughness was minimized by the passivation layer. AFM image in inset of Figure 5.2 (b) revealed that the surface of Si_3N_4 film was smooth, and rms roughness decreased almost 5 times from 1.52 nm to 0.34 nm. In addition, the superior low leakage current density for the corresponding films subjected to 50-nm Si_3N_4 as the efficient passivation layer on top of 10-nm HfO_2 film was found as low as 10^{-11}A cm^{-2} at the applied voltage of 1–10 V as shown in Figure 6.2 (b). The proposed MIM device structure, including of Si_3N_4 layer on O_2 plasma-treated HfO_2 film, exhibited the superior low leakage current than that only O_2 plasma treated HfO_2 film. The high leakage current density from the sample adopted O_2 plasma treated HfO_2 film could be attributed to the existence of numerous traps over the film surface and hence poor dielectric characteristics. Similarly, the traps over the film surface could also affect the performance of the following TFT device. In a simple-minded classical approach, it might appear that electrons tunneled easily as moved through the trap states of HfO_2 surface. However, the trap induced breakdown effect was effectively suppressed by HfO_2-Si_3N_4 film structure. In addition, the schematic energy band diagrams in Figure 5.2 (c) were proposed to explain the trap-dependent leakage and the passivation of traps over HfO_2 film surface. The traps in HfO_2 film had occurred and affected the energy band, indicating that the electrons can easily move through the HfO_2 film due to trap-assisted tunneling effect.

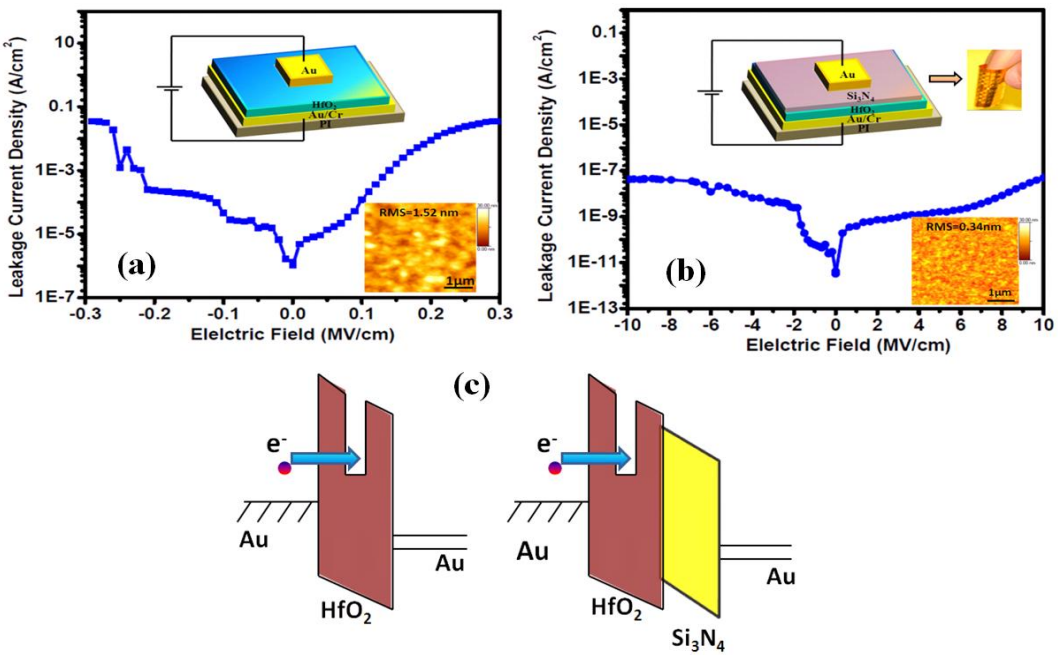


Figure 5.2 (a) J-E Plot of leakage current density versus electric field for MIM-structural sample prepared by using sol-gel HfO_2 film and inset of AFM image (surface roughness: 1.52 nm) from HfO_2 film; (b) J-E plot for MIM-structural sample prepared by using Si_3N_4-HfO_2 stacked film and inset of AFM image (surface roughness: 0.34 nm) from Si_3N_4-HfO_2 stacked film; (c) schematic energy band diagrams to explain trap-dependent leakage and the passivation of traps.

This observation was responsible for high leakage current in the MIM device [**9**]. These trap centers created intermediate energy levels due to the presence of impurities in the material [**10**]. After surface Si_3N_4 film passivation, the reliability related current transport mechanism was improved from reduction of trap-assisted tunneling. Under passivation treatment with Si_3N_4 film, the potential barrier became thick enough not to allow electrons from gate to tunnel through the barrier. Thus, the leakage current densities apparently decreased as strong energy band-pass for electrons can shift toward a higher energy level. The O_2 plasma

treated-HfO_2 film after Si_3N_4 passivation exhibited better reliability even under high electric field in Figure 5.2 (b). This observation suggested that HfO_2 film was extremely suitable as a gate dielectric in future flexible devices. From the formation of a passivated Si_3N_4 layer, the reduction of parasitic resistance could suppress the surface trap density effect and improve the performance of flexible devices.

5.3.2 Surface Morphology of P3HT Film

The surface morphology of the P3HT film by AFM measurement in tapping mode at 2 μm scan size was demonstrated in Figure 5.3; the sample was deposited by sol-gel spin-coating process on Si_3N_4–HfO_2/Au/Cr-coated flexible PI film. It could be seen from the figure that the surface morphology of the spin-coated P3HT film was dense and crack-free. Thin films of P3HT with regioregularity and order structure were obtained with the thermal treatment at 80 ℃ of curing, and the performance of the device would be enhanced. The average thickness was about to 30 nm measured by ellipsometery technique. The root-mean-square (RMS) surface roughness of the P3HT film as channel area grown on Si_3N_4–HfO_2/Au/Cr/PI surface was 1.02 nm. We observed that the fabrication process with chloroform solvent yields higher mobility over a wide variety of tested devices mentioned in the following. Goetz et al., revealed that P3HT films from chloroform solution behaved a higher tendency to form ordered fibrillar networks without sharp boundaries [**11**]. By the utilization of AFM for the analysis of the surface morphology of the P3HT film, we suggested that the sol-gel deposited P3HT film was crack-free, uniform, and well adhered on Si_3N_4–HfO_2/Au/Cr-coated PI for the fabrication of high performance flexible devices.

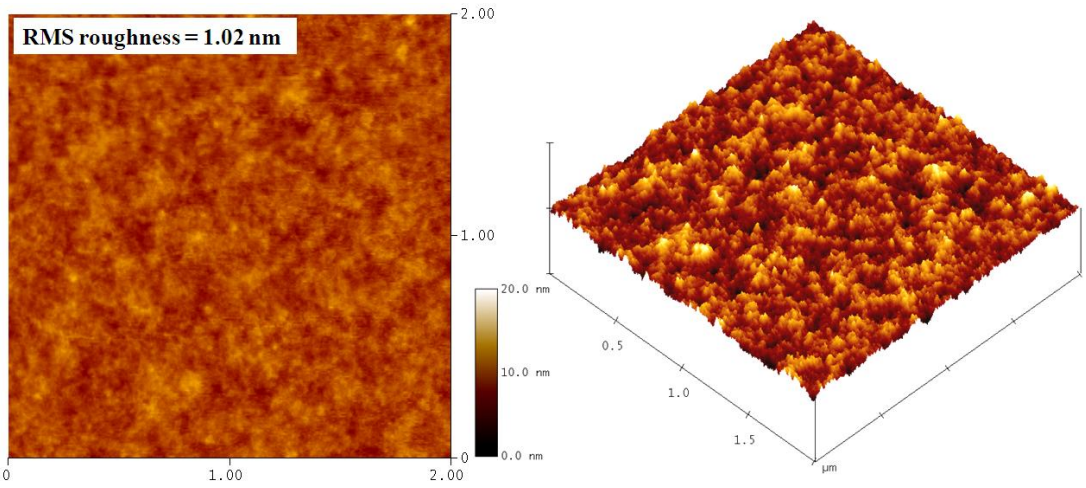


Figure 5.3 AFM image from P3HT thin film as channel area on Si_3N_4–HfO_2/Au/Cr/PI substrate at a length scale of 2 μm (surface roughness: 1.02 nm).

5.3.3 Transfer and Output Characteristics

The TFT devices were fabricated after the beneficial effect of HfO_2-Si_3N_4 film structure in MIM device was understood. To indicate the influence of the gate leakage current, we measured the transfer characteristic of P3HT-OTFT for HfO_2 as gate dielecric layer on flexible PI substrate where V_{DS} was set at -5 V. Figures 5.4 (a) & (b) showed the transfer and output characteristic curves of the P3HT-TFT on the flexible PI substrate with O_2 plasma treated HfO_2 film as dielectric layer. The output characteristics of the applied drain voltage (V_{DS}) ranged from 0 to -5 V with gate biases (V_{GS}) varying from 0 to -5 V in steps of 1 V. The trap state problem in the HfO_2 film of this TFT device might also contribute to leakage property. The transfer characteristic curve was abnormal and the output characteristics were only observed at a higher gate voltage. Even under -5 V of gate and drain voltage, reasonable device properties were not observed with an

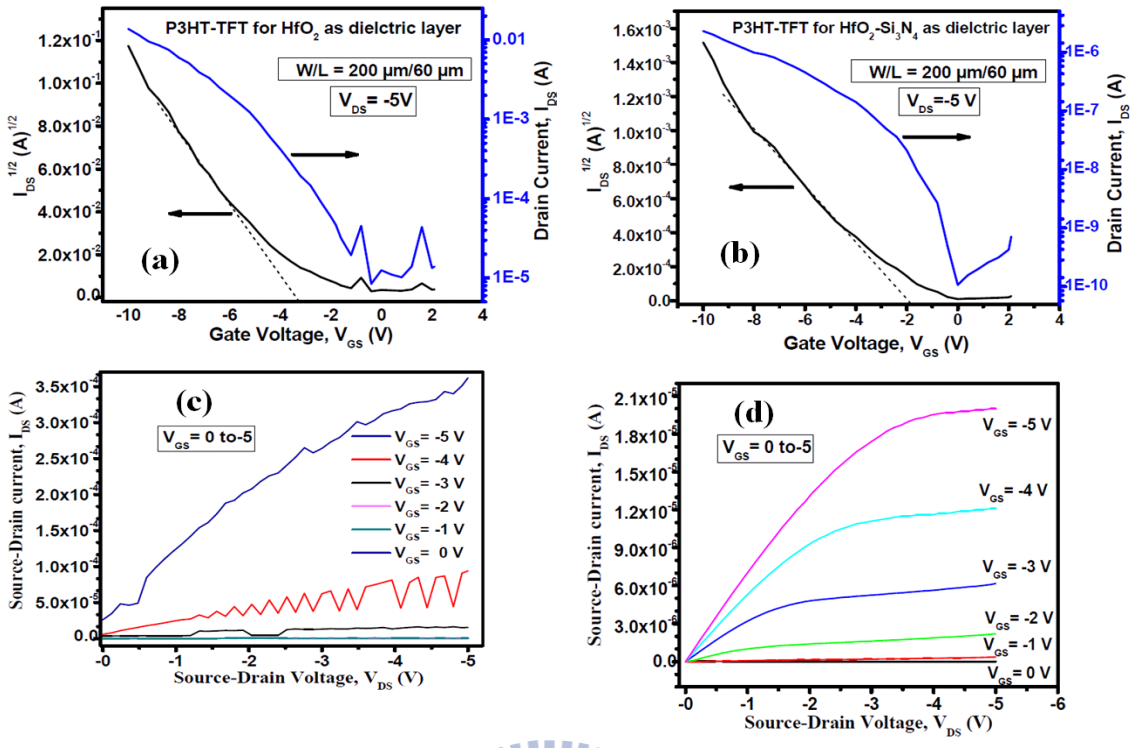


Figure 5.4 (a) Plot of drain current and square root of drain current with respective to gate voltage (I_{DS}-V_{GS}) for P3HT-OTFT on flexible PI substrate by using HfO_2 as gate dielectric under V_{DS}=-5 V, and (b) output characteristic (I_{DS}-V_{DS}) as V_{GS} ranging from 0 to -5.0 V at 1 V step for above device. (c) Plot of drain current and square root of drain current with respective to gate voltage (I_{DS}-V_{GS}) for P3HT-OTFT on flexible PI substrate by using Si_3N_4-HfO_2 stacked film as gate dielectric under V_{DS}=-5 V, and (d) output characteristic (I_{DS}-V_{DS}) as V_{GS} ranging from 0 to -5.0 V at 1 V step for above device.

on/off current ratio of about 10^2, which would not afford to minimum requirement of TFT devices. Moreover, as Figure 5.4(b) illustrated, the output characteristics were not stable and drain currents were not satisfactory. The OTFT device achieved a much better performance while using Si_3N_4 as a passivation layer onto O_2 plasma treated HfO_2 film. As shown in Figure 5.4(c), P3HT-OTFT exhibited typical p-type output characteristics [source-drain current (I_{DS}) versus drain

voltage (V_{DS}) at different gate voltages (V_{GS})], when operated in the accumulation mode. The OTFTs operated in the accumulation mode when a negative gate voltage was applied, since positive carriers were generated in the P3HT organic semiconductor layer. In order to get a reasonable estimation for the possible dependence of the mobility along the TFT device channel, we have plotted the linear and saturated field-effect mobilities extracted from the transfer characteristics of the TFT according to Eqs. (5.1) & (5.2). In the linear regime, the field-effect mobility (μ_{lin}) can be calculated from transconductance [**12**]

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{WC_i}{L}\mu_{lin}V_{DS} \quad (5.1)$$

Where, C_i was the gate capacitance and W/L was the ratio of the channel width to channel length. In the saturation region ($V_{DS} > V_{GS} - V_{Th}$), I_{DS} can be described by following equation [**12, 13**] and then the saturated field-effect mobility (μ_{sat}) can be calculated as

$$I_{DS} = W\mu_{sat}\frac{C_i}{2L}(V_{GS} - V_{Th})^2 \quad (5.2)$$

Where, μ_{sat} was the field-effect mobility, C_i (=10.2 nF cm^{-2}) was the capacitance of the Si_3N_4-HfO_2 dielectric layer, W=200 μm, L=60 μm, and V_{Th} was the threshold voltage. As Eq. (5.2) implied, a plot of V_{GS} versus square root of I_{DS} gave a straight line, and V_{Th} was obtained. The threshold voltage and the field-effect mobility were to be −1.9 V and 0.041 cm^2 $V^{-1}s^{-1}$. The on/off current

ratio was 2.0 $\times 10^4$ when V_{GS} was scanned from +2 to −10 V. In addition, the output characteristic illustrated in Figure 5.4 (d) indicated that the device had good saturation behavior. The drain current increased linearly with an increase in drain voltage in the low drain-voltage regime, whereas it tent to saturate in the higher drain-voltage regime because of the pinch-off of the accumulation layer. Furthermore, a large increase of the electrical conductivity was expected due to an enhancement of the hole mobility in these crystalline P3HT domains. A thermal treatment had intense effects on the charge carrier for P3HT blending from chloroform. Annealing at 80 ℃ for this channel layer resulted in the formation of crystalline P3HT and thus enhanced the hole mobility in these regions by an order of magnitude. It was also likely to happen that the use of high-k materials as the gate insulator had reduced the device operating voltage for flexible devices. The field-effect mobility, on/off current ratio and threshold voltage of P3HT-based OTFTs on silicon/glass substrates were summarized in Table 5-1 for comparision with literatures [**14-19**].

Refs.	Dielectric material	V_{Th} (v)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	Substrate
This work	HfO_2-Si_3N_4	-1.9	0.041	2×10^4	Polyimide
[14]	SiO_2	-14	0.015	10^5	Silicon
[15]	Al_2O_3	-3.6	0.008	10^4	Silicon
[16]	PVP/TiO_2	1.14	0.014	10^3	Silicon
[17]	Ta_2O_5/PVP	1.7	0.032	---	Glass
[18]	HfO_x	-0.5	0.062	150	Silicon
[19]	TiO_2	1.0	0.054	10^2	Silicon

Table 5-1 The comparison of various dielectric layers and corresponding electrical performance of P3HT-based OTFTs fabricated on silicon or glass substrates.

The field-effect mobilities' obtained here were lower than previously reported values for other high performance TFTs but it was expected that higher field-effect mobility could be further improved through the optimization of the device fabrication process by choosing appropriate solvents as previously mentioned.

5.3.4 Bending Treatment to Three-Point Bending Conditions

Mechanical stability was the most important factor for flexible devices when dealing with the long-term application. We estimated the electrical properties of our OTFT after different bending times, convex and concave type bending stages to make sure the possibility for use in advanced flexible electronic devices. Figure 5.5 (a) showed the transfer characteristics for plasma treated high-k HfO_2 film followed by Si_3N_4 layer subjected to number of bending times. Inset of Figure 5.5 (a) presented an image of the setup of the frontward and backward bending tests and the number of bending times. For the initial measurement, the on/off currents ratio was calculated about to 10^4 and remained almost unchanged even after bending the TFT up to 100, 500 and 1000 times. Here in our case, the P3HT as channel material and HfO_2 film as gate dielectric followed by Si_3N_4 layer over flexible organic PI substrate revealed superior stability even after bending the TFT device up to 1000 times. After the bending test, the on/off current ratio and threshold voltage remained almost the same as it was prior to initial bending. This observation indicated that the sol-gel spin-coating method to form OTFT by using high-k film as gate dielectric passivation provided superior electrical performance and stability on PI substrate. Furthermore, we tested two additional features of our OTFT on PI to explore its feasibility for use in practical applications. Namely, we estimated the transfer characteristics in both

convex (Figure 5.5 (b)) and concave (Figure 5.5 (c)) settings, varying the radii of curvature (R_c) for 2 and 4 cm. Prior to manufacturing process, a hard plastic foil was used as a substrate support to provide these specific bending conditions. Figure 5.5 (a) & (b) suggested, the P3HT retained its transfer characteristics after the both convex and concave types bending conditions. All of the curves demonstrated the on/off current ratio to be about 10^4 at applied V_{DS}= -5 V.

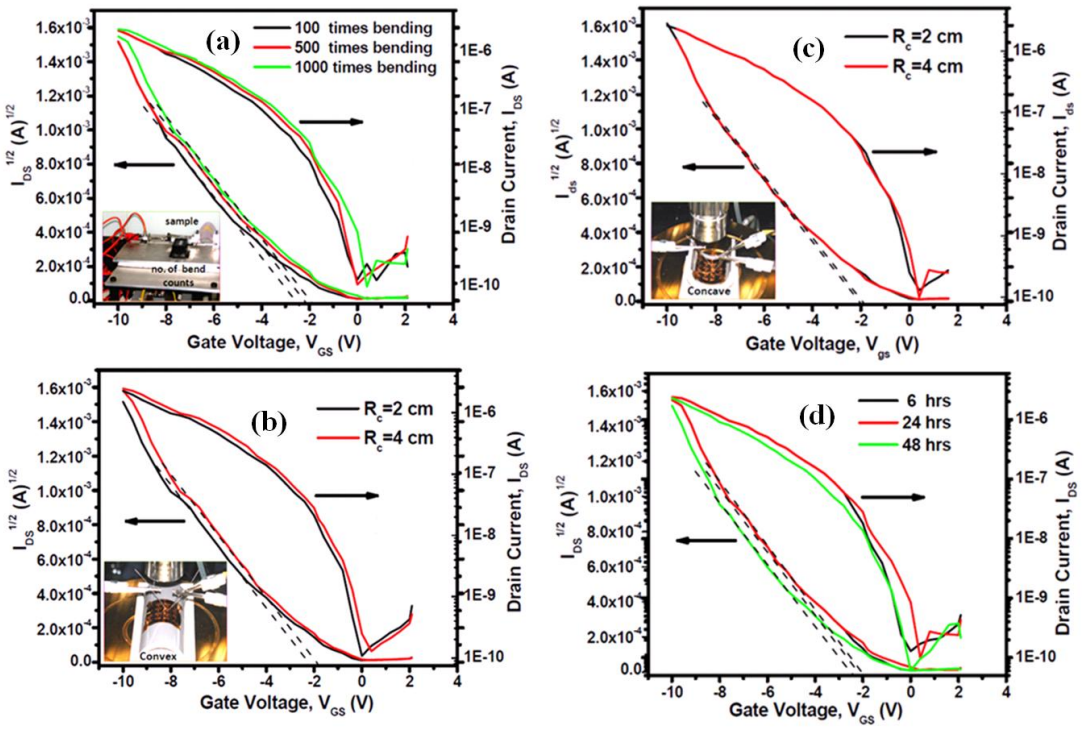


Figure 5.5 I_{DS}-V_{GS} plots for P3HT-OTFT by using Si_3N_4-HfO_2 stacked film as gate dielectric on flexible PI substrate: (a) bending time test and inset of customized-homemade bending system, (b) convex shape test and inset of convex setting, (c) concave shape test and inset of concave setting, and (d) time-dependent I_{DS}-V_{GS} characteristics over 6 hours, 1 day and 2 days.

This value of on/off current ratio was consistent with the ratio of pristine device. This observation implied that the plasma treated HfO_2 film followed by Si_3N_4 passivation

as gate dielectric over flexible organic PI substrate revealed superior stability after bending the OTFT device. After the bending measurement, the threshold voltage (V_{Th}) was almost in the same with no bending condition (i.e. -1.9 V). Therefore, the dielectric Si_3N_4 passivation film was supposed to enhance the electrical characteristics of the TFT devices at low temperature manufacturing. Our results demonstrated better performance when compared to the report for flexible OTFTs [**14, 16**]. Zhang's group had fabricated the flexible pentacene-based TFT arrays, whose mechanical flexibility represented the best values till date [**20**]. From this concave and convex examinations, we concluded that the P3HT based TFT device fabricated on plastic substrate had an excellent stability even bending the device up to 2 cm in convex or concave status.

5.3.5 Improved device stability in air

The ambient stability of the TFT device was monitored through the time-dependent performance for the device. To evaluate the reliability of the P3HT-transistor device, environment dependent transfer characteristic measurements were carried out under normal environment. Time-dependent transfer characteristic was measured in Figure 5.5 (d) for the period of 6, 24, and 48 hours. The resultant mobilities were calculated between 0.04-0.05 $cm^2\ V^{-1}\ s^{-1}$, on/off currents ratio 10^4, and threshold voltage about -2.0 V for our flexible P3HT-TFT device. This observation was very close with the illustration in Figure 6.4 (c). By considering the performance, the data suggested that over a day period of time, our flexible P3HT-TFT did not degrade the mobility. Meanwhile, we had pointed out that the device stability actually reduced for a long period of time over 10 days or more although it was not illustrated here. However, this was not a challenge issue because the commercial flexible device required the package process to avoid contamination. But, less than 48 hrs, the air stability of our flexible OTFT device without package

was observed in comparison with the P3HT-FET on bare SiO_2 substrate. This subtle difference in on/off currents ratio and mobility meant that our flexible TFT had an excellent reliability after placing the devices in normal environment for 48 hours and was able to use for advanced microelectronic devices. Our flexible TFT device showed a relatively excellent bias stability with the use of Si_3N_4 layer passivation on the HfO_2 film. O_2 plasma treated high-k film and following Si_3N_4 layer seemed to improve the P3HT-OTFT stability and reduce the absorption effect of humidity, and thereby retarded the degradation of the OTFTs under ambient condition. These results suggested that the possibility of using highly reliable Si_3N_4-HfO_2 stacked heterostructure to fully flexible poly-(3-hexylthiophene) thin-film transistor for future commercial manufacturing.

5.4 Summary

We have successfully fabricated a new and fully flexible organic poly-3-hexylthiophene (P3HT) p-type TFT on a transparent flexible polyimide substrate using high-k HfO_2 as dielectric layer and Si_3N_4 as passivation layer via very simple and cost-effective sol-gel spin-coating technique. Defects in the HfO_2 films are expected to be rarely induced, because of the low temperature deposition process and plasma treatment. Current-voltage characteristics of the device in metal-insulator-metal structural device imply the success of using Si_3N_4 over HfO_2 to achieve the satisfactory leakage current. The fabricated devices exhibit good electrical performance with saturation mobility of 0.041 $cm^2\ V^{-1}\ s^{-1}$. Moreover, the device demonstrates stable performance over the course of bending up to 1000 times and radii of curvature minimum down to 2 cm in both convex and concave type structures. Our results suggest that the P3HT semiconductor material in together with HfO_2 film

followed by Si_3N_4 as passivation layer are promising materials for the low-cost flexible electronic devices.

Chapter 6: Facile Synthetic Route to Implement a Fully Bendable Organic Metal-Insulator-Semiconductor Device on Polyimide Sheet

6.1 Introduction

Flexible technology in electronics production has attracted considerable attention for a wide-range of applications because it is a new process of creating electronic circuits on a roll of plastic sheets. This is a new technology, which is expected to meet the growing demand for low-cost, large-area, flexible and lightweight devices, such as roll-up displays, e-papers, connectors, and keyboards [**1, 2**]. Being a novel technique, much attention has been paid to the development of electronic circuits on flexible substrates since the end of 20th century. An important consideration for active devices is the isolation between an input and output signal. Insulators are widely used to provide this isolation [**3**]. Subjected to fabricate the flexible devices over plastic substrates, it is necessary to grow gate dielectrics at relatively low temperature compared with those of conventional silicon (Si) substrate based devices owing to temperature stringency associated with plastic sheets. Organic/polymer materials [**4, 5**] have attracted a lot of attention for building large-area, mechanically flexible electronic devices. These materials are widely pursued since they offer numerous

advantages for easy-processing (e.g., spin-coating, printing, evaporation), good compatibility with a variety of substrates including flexible substrates, and great opportunity for structural modifications. Owing to the limitations in development of flexible devices, the present mainstream strategy is an attempt in achieving bendable electric devices and is not to develop new materials, but instead is to engineer new structural constructs from established materials. As shown in the international technology roadmap for semiconductors (ITRS) guidelines, interlayer metal insulating materials need to have dielectric constants of about 20-30 to effectively isolate devices having sizes <100 nm [**6**]. Thus, much attention has been given to the research and development of new materials with high-k value and new deposition processes. Titanium dioxide (TiO_2, titania) is the most promising candidate used as gate dielectric material for its high efficiency, safety, cleanness and low cost [**7, 8**]. In general, researchers concentrate on one aspect to improve the performance of the electronic devices by improving the dielectric efficiency at low temperature. The highly hydrophilic property presents interesting applications of TiO_2 films such as anti-fogging and self-cleaning [**9, 10**]. There is also a strong desire on the part of microelectronic industry to develop advanced, large-scale new techniques that can meet the growing demand of low temperature (ca. 25 ℃) deposition processing on flexible substrates, miniaturization, and which should be easy-to follow. But researchers have had little success in making ultrathin films at low temperature using spin-coating [**11**] or printing techniques [**12**]. However, limitations in such existing approaches to interoperation at the network transport and application levels are observed for the flexible devices. A major goal for the realization of flexible electronics is the development of solution processing, functional materials that afford both direct deposition of electronic components (including resistors, diodes, capacitors, transistors and interconnects) and high performance devices. The

dip-coating technology [**13, 14**] is exceptionally promising because patterns can be generated without any material waste, which could lead to drastic reductions in production costs and in environmental impact. In our previous study, we have assessed the use of specific sol-gel preparation to obtain useful spin coated high-k HfO_2 film to be used as dielectric layer in organic thin-film transistor [**15**]. However, the spin coating technique is not suitable for fabricating the TiO_2 based MIS device on PI substrate due to cracking problem on the surface.

In current study, for the first time, we present an interestingly new and easy-to-follow synthesis procedure to prepare triblock copolymer surfactant $HO(CH_2CH_2O)_{20}(CH_2CH(CH_3)O)_{70}(CH_2CH_2O)_{20}H$-based nc-$TiO_2$ thin film dielectric layer at room temperature via the dip-coating solution process. The electrical insulating properties of fully bendable MIS device prepared employing nc-TiO_2 film as a dielectric layer and pentacene as semiconductor layer, exhibited low leakage current density, and good capacitance with high durability. In this way, we realized that the dip-coating technique provides a uniform thin film deposition level on flexible substrate at low temperature than other standard thin film deposition techniques. This new synthesis process to fabricate nc-TiO_2 at low temperature have good stability when using in electronic device as dielectric layer, and gives excellent results compared to other high-k dielectric materials. We expect that these important features will allow this novel synthesis route and deposition method to be used at large scale in flexible electronic device applications.

6.2 Materials and Methods

Pluronic® P123 hydrocarbon surfactants [triblock copolymer with molecular weight of 5800 Da and formula of $HO(CH_2CH_2O)_{20}(CH_2CH(CH_3)O)_{70}(CH_2CH_2O)_{20}H$, abbreviated as P123] was

purchased from O-BASF Corporation. Ethanol (C_2H_5OH, 99.5% Aldrich)) and titanium chloride ($TiCl_4$) were obtained from Sigma Aldrich Chemie GmbH. Deionized water (DI water) used was purified with filters, reverse osmosis, and deinized system until the resistance was more than 18 MΩ.cm^{-1}. DI water was used to clean, wash, and as a solvent. Chromium shots (Cr, 99.999%, ADMAT), size: 3-5 mm, Aluminum shots with size 3-5 mm (Al, 99.999%, ADMAT), and gold shots with size 1-2 mm (Au, 98.999%, ADMAT), were purchased form Praxair (Danbury, CN, USA). All chemicals were used without further purification. Pentacene as the organic semiconductor material was purchased from Seed Chem. Co. (electronic grade, PTY. LTD). DuPont™ Kapton® Polyimide (abbreviated as PI) film (38-µm thickness of PV9100 series) was used as substrate to fabricate the device.

To deposit nc-TiO_2 thin film, a synthesis solution was prepared by dissolving 2.0 g P123 into mixture solution of 20 g C_2H_5OH and 1.0 g DI water; depicted in Figure 6.1 (a). Then, poured slowly 1.5 g of $TiCl_4$ to the solution as shown in Figure 6.1 (b). Proper caution should be taken during the addition of $TiCl_4$ into mixed solution of C_2H_5OH/H_2O/P123, because of the exothermic reaction takes place in situ. It is then vigorously stirred for 24 h in an ice-water bath. For the first day, the color of the solution was yellowish-green and almost after 5 to 7 days, the color of the solution disappeared and colorless solution was obtained as shown in the photographs given in the Figure 6.1 (b). This colorless solution remains stable for several weeks at room temperature. Before coating the film, the solution was aged at 60% relative humidity for 2 h at room temperature, and then thin film was deposited by dip-coating the PI sheet rapped over glass substrate at a constant withdrawal rate of 1 mm sec^{-1}, a home-made instrument for film deposition via dip-coating process is shown in image below the Figure 6.1 (c). After dip-coating, ageing the film for another 5 min at 80 ℃, the evaporation of C_2H_5OH, HCl, H_2O and a disorder-to-order transition occurred

(Figure 6.1 (d)). Finally, as-synthesized film was subsequently calcined by annealing in presence of O_2-flow at 270 ℃ for 5 h (Figure 6.1 (e)). This thermal treatment produced uniform nc-TiO_2 film further in device fabrication and material characterizations.

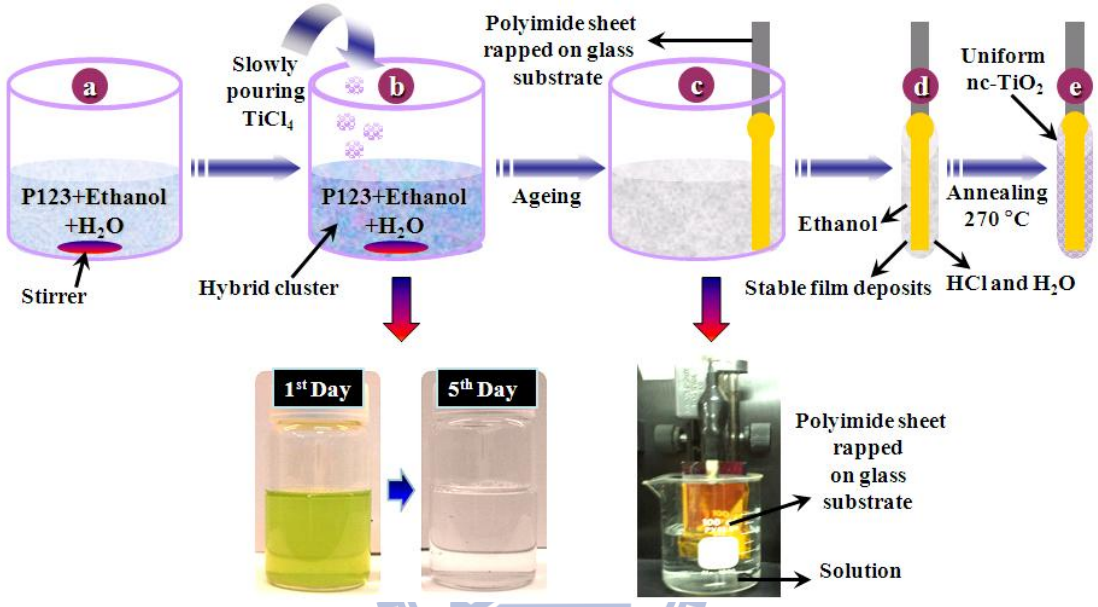


Figure 6.1 (a-e) Schematic illustration of the proposed synthetic solution proceeded dip-coating approach for the preparation of the uniformed nc-TiO_2 film presented in this work.

The process steps in fabrication of MIS device over PI including its bending structured formation is described in Figure 6.2 (a) & (b); plastic 38-μm thick DuPont Kapton® PI sheet was used as flexible substrate for the fabrication of MIS capacitor. The PI film was cleaned ultrasonically with ethanol (Fluka; water content: < 0.1%) for 30 min and DI water and then high-pressure N_2 gas was used to remove the water and any remaining particles from the PI surface. PI substrate was annealed at 200 ℃ for 15 min in vacuum to achieve a relative thermal stability, and enhancement of the adhesion strength. After cleaning up a PI substrate, a 50-nm thick Cr as adhesion layer

and 100-nm thick Au were deposited sequentially on the PI substrate by thermal coater. The Cr layer was used as the adhesion layer between the PI substrate and the Au film. Au was deposited for the gate electrode over the Cr coated PI substrate. The 25-nm TiO_2 film from organic-inorganic blend via dip-coating process was used as dielectric layer; the thickness of the above film was measured by ellipsometery techniques. And then, pentacene film of 50-nm as a semiconductor layer was deposited using a thermal evaporator with substrate temperature maintained the room temperature. At the end of the experiments, 200-nm thick Al film was pattered as the top electrode using shadow mask and a thermal coater. Figure 6.2 (c) shows a photograph of an array of MIS devices (c.a. 80 devices) patterned on area of 5× 5 cm^2 fabricated on the fully flexible PI substrate under a large surface strain.

The surface morphology of the TiO_2 thin film from organic-inorganic blend over PI was evaluated using AFM, Digital Instruments Nanoscope, D-5000) at scane size of 2 μm × 2 μm at a scane rate of 1 Hz. From AFM images, the nanocrystals of TiO_2 were also determined over the film surface. XRD patterns were obtained using a Rigaku D/max-IIIB diffractometer using Cu Kα radiation (λ = 1.5406 A°). In addition, the surface morphology of pentacene film was also evaluated by AFM at a scan size of 3 μm × 3 μm and a scan rate of 1 Hz, and the XRD analysis as described above. We used XPS to analyze the chemical bonding of the elements of interest under various treatment conditions for TiO_2 film. The hydrophilicity of the nc-TiO_2 surface was evaluated by contact angle measurement by use of a commercial contact angle meter. Deionized water was used as the water source in the contact angle experiment. The contact angles measured for 5 min after the drop has made contact with the film surface under test over PI. Measurements for leakage current and capacitance of the device were performed using an Agilent-4156 probe station and an HP-4284A capacitance-voltage (*C*–*V*) analyzer, respectively.

We tested two additional features for our MIS fabricated on PI flexible substrate to explore its feasibility for use in practical applications. We estimated the mechanical

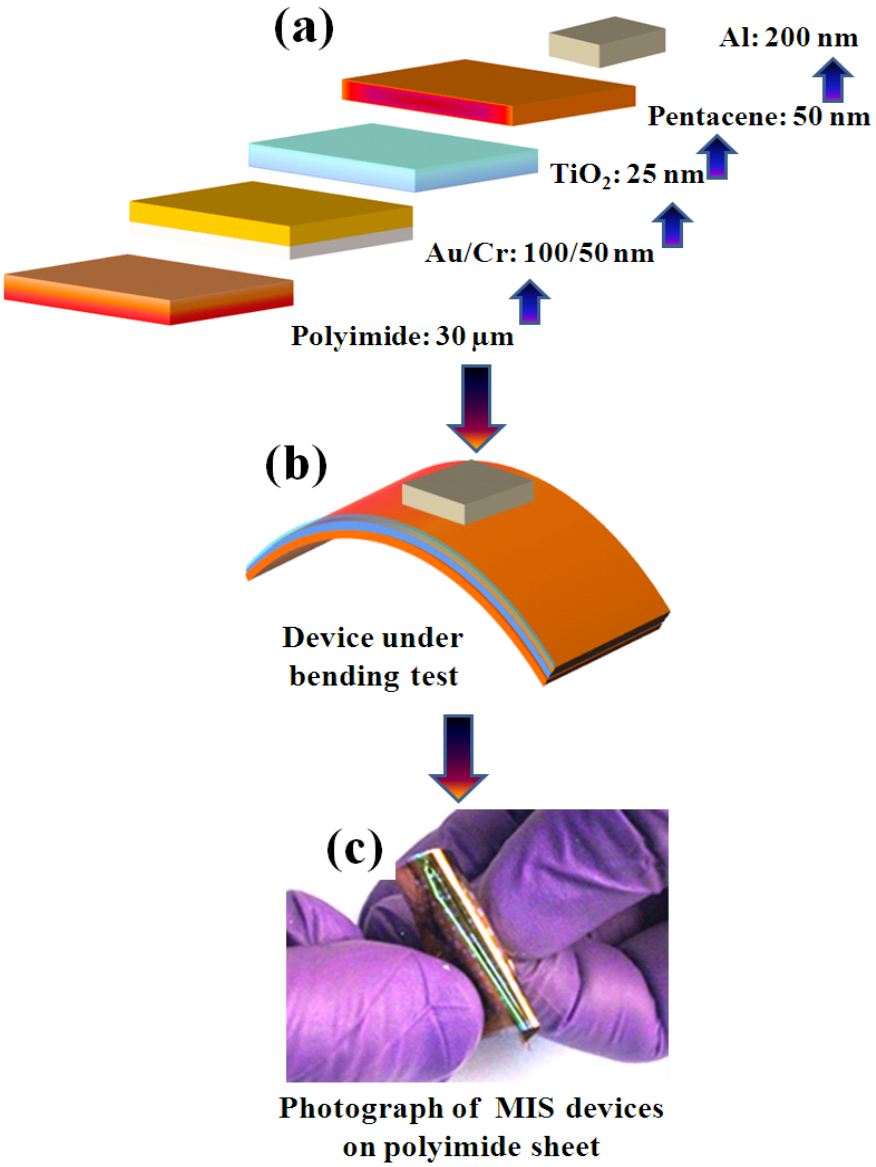


Figure 6.2 (a) Schematic representation of an MIS device features a high-*k* TiO_2 thin film and organic pentacene as semiconductor layer on a PI substrate in their fabrication steps; (b) MIS device featuring a bend test. (c) Photograph of an array of MIS devices on the flexible ultra-thin PI substrate.

strain on the electrical properties under a serial flexibility test including convex and concave for different radii of curvatures using which the course of time period stability was acquired. Prior to manufacturing process, a foil was used as a substrate support to provide these specific bending conditions in convex and concave settings for different radii of curvatures varies from 1.5 cm to 4.0 cm. Next, we performed the real life flexibility tests for one array of flexible MIS devices repeatedly crumpled in the palm of a hand and then electrical performance was estimated.

6.3 Results and Discussion

6. 3.1 Film quality and surface roughness of nc-TiO_2

The prepared and annealed samples of TiO_2 thin films for AFM surface analysis were deposited on clean Au/Cr coated PI substrate using similar conditions as depicted in MIS structure. The texture and surface morphology of nc-TiO_2 films were investigated for as-deposited then baking at 80 ℃ and annealing in O_2-flow at 270 ℃ for 5 h, as shown in Figure 6.3 (a) & (b), respectively. The scans were carried out in a tapping mode for 2 µm×2 µm scales. The images on the right are from their 3dimensional images from films of as-deposited and annealed. Figure 6.3 (a) clearly shows particles with almost uniform size in the calcined nc-TiO_2 thin film and the film surface is crack-free in nature. Another important observation is the TiO_2 crystallites grown on Au/Cr coated PI tend to arrange into somewhat self-assembled uniform structures with minimum distance between them. However, when the calcinations temperature is increased to 270 ℃ for 5 h, aggregation of the TiO_2 crystallites occurs more specifically; which can clearly be seen from Figurre 6.3 (b). It was found that there is no pronounced increase in the crystal size as the calcinations

temperature mentioned at 270 ℃ is only for 5 h or more. We cannot mention the temperature above 300 ℃ or more because of low thermal compatibility of PI film.

The respective root-mean-square (rms) values of the surface roughness of as-deposited and annealed films are 2.34 and 2.18 nm, respectively. This effect could be ascribed to the fact that the primary TiO_2 crystallites aggregate to larger secondary

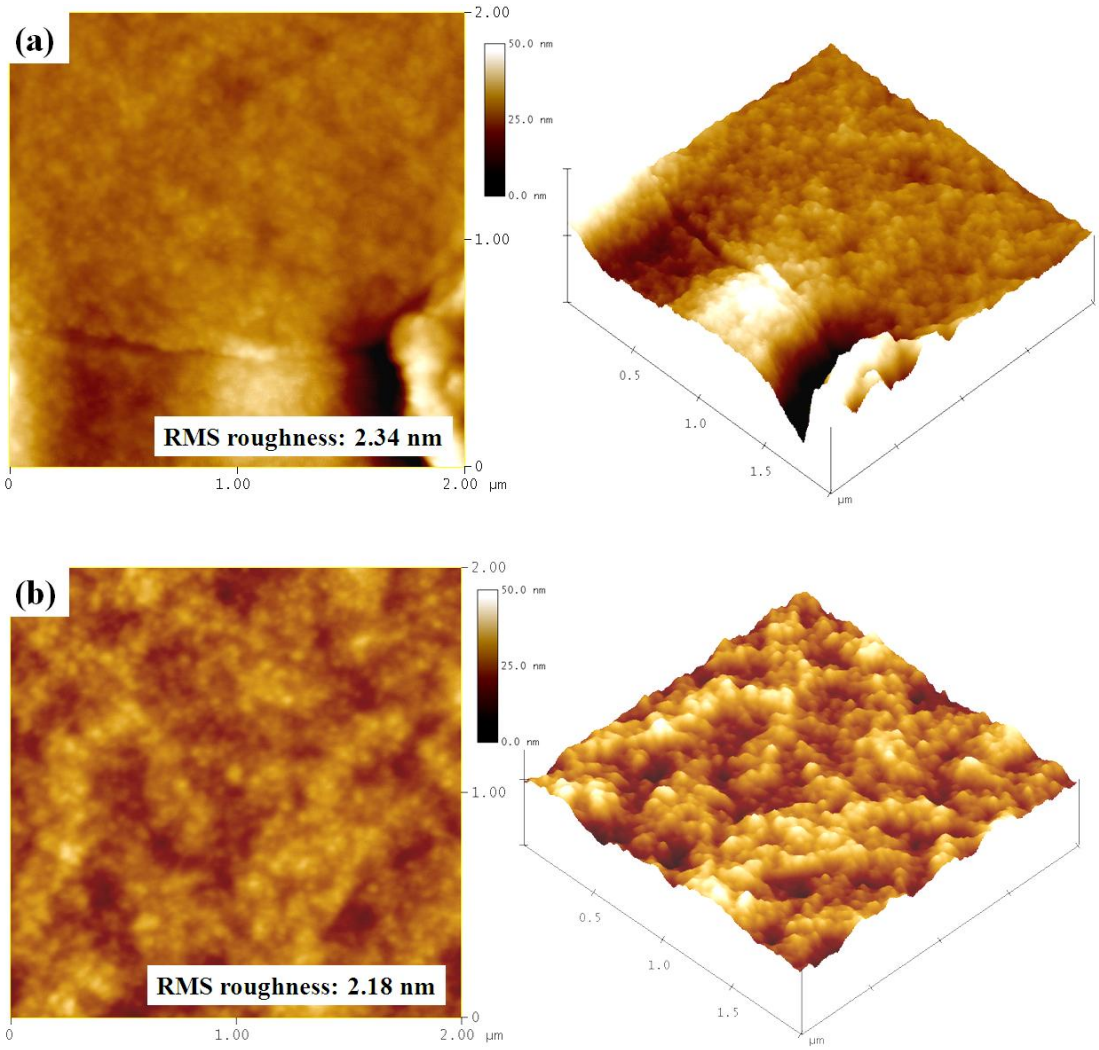


Figure 6.3 AFM images from thin film of nc-TiO_2 coated on Au/Cr/PI surface calcined at different temperatures conditions for (a) as-deposited then baking at 80 ℃, and (b) annealed in O_2 flow at 270 ℃, 5 h.

particles minority when the calcination temperature is increased. Thus, 270 ℃ could be considered to be the optimum reaction temperature range for obtaining nc-TiO_2

thin films with uniform morphology and particle size. There is only a small decrease in thickness for dip-coated film annealed at 270 ℃ for 5 h. The thickness of as-deposited film is 28 nm, while the thickness of the annealed film is 25 nm estimated by ellipsometry techniques. There is only a small decrease in thickness for dip-coated film annealed at 270 ℃ for 5 h, but without degrading the surface smoothness. This observation confirms that the P123 surfactant plays an important role to smooth the crystalline film of TiO_2 via surface dip-coating process on PI. The observed small change in the thickness is consistent with the relatively small volume of triblock copolymer P123 surfactant present, which favors particle–particle contact in the multilayers prior to calcination. Therefore, , there is only a small decrease in the film thickness as the nanoparticles of TiO_2 do not collapse on one another; instead smooth film surface has appeared as shown in Figure 6.3 (b).

6.3.2 XRD analysis

The identification of the phase structure of TiO_2 film calcined at temperature 270 ℃ in O_2- ambient was investigated by XRD analysis and the result is shown in Figure 6.4. As can be seen, the XRD result of the as deposited then baked at 80 ℃ for 5 min TiO_2 film is considerably the amorphous phase. There was hardly any peak observed for baking at 80 ℃ treatment condition. However, the amorphous phase is turned into a stable grained naocrystalline anatase phase under a temperature of 270 ℃ for 5 h, and this structure does not alter on subsequent cooling to room temperature. The XRD patters for annealed at 270 ℃ treatment condition features the six intensity diffraction peaks in the range of 25.3°-62.8°. Those are indexed as (101), (004), (200), (105), (211), and (204) diffraction peaks. They showed the typical patterns for the anatase structure of Joint Committee on Power Diffraction Standards (JCPDS) No. 21-1272. The crystallite size was estimated for the broadening of the

diffraction peaks using the Scherrer equation: $D = 0.89\lambda/\beta \cos \theta$, where D is the crystallite size, λ is the wavelength of the x-ray radiation (λ = 1.5406 A°), β is the peak width at half-maximum height after subtraction of the equipment broadening, 2θ = 25.3° for anatase (101), and 0.89 is the Scherrer constant.

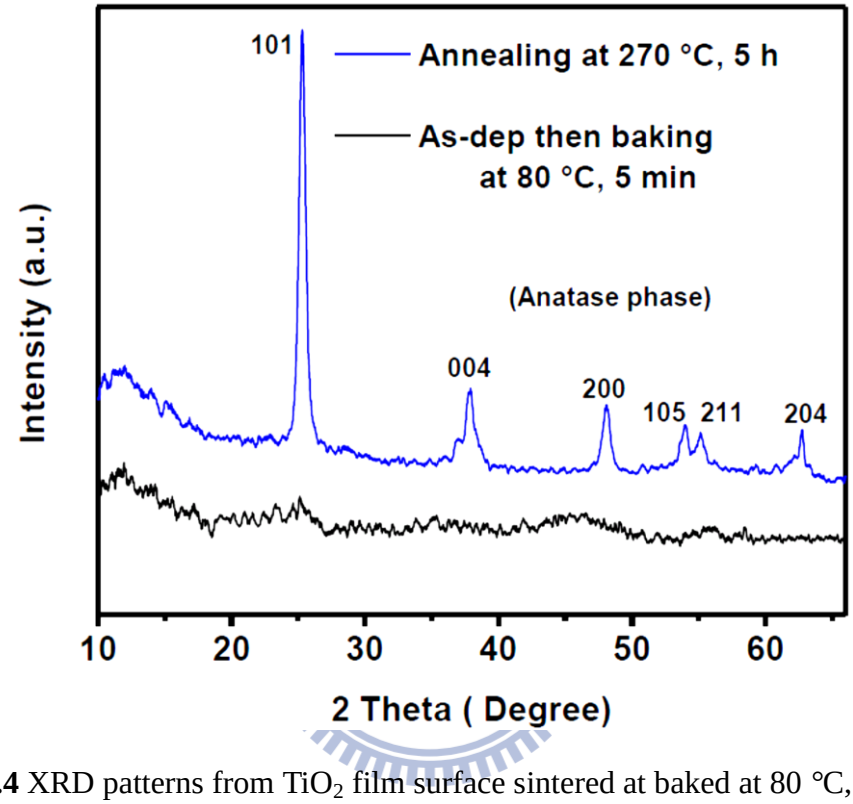


Figure 6.4 XRD patterns from TiO_2 film surface sintered at baked at 80 ℃, 5 min and annealed 270 ℃, 5 h. *I*: intensity in arbitrary units, but the intensity scale is identical for both patterns.

As calculated from the Scherrer equation using the (101) diffraction peak of anatase for sample annealed at 270 ℃, the average crystalline size was 8.0 nm. It was found that there is a pronounced phase change for TiO_2 surface as the calcination temperature increases, which attributed to the growth of crystalline TiO_2 surface. It is of interest to note that for Au/Cr/PI system, the inclusion of Au and Cr in the deposits was almost completely suppressed under suitable conditions. Here, the gold and chromium shots contained in the tungsten crucible were thermally evaporated in a

high vacuum chamber by heating it to near its evaporated point. The resulting treats with the spray of chromium and gold layers deposited on a flexible PI substrate. The resulting treats with the spray vapor of chromium and gold layers deposited on a flexible PI substrate. It may depends on several factors, notably the temperature of the substrate during growth, the temperature after growth and the length of time the substrate is held at that temperature, the flux of chromium and gold atoms striking the substrate, the flatness and cleanliness of the substrate, and the ambient environment of the substrate during and after growth.

6.3.3 XPS Analysis

Quantitative XPS analysis was performed for both as deposited and the annealed nc-TiO_2 films act over the Au/Cr/PI substrate. We performed the XPS measurement over Au/Cr/PI substrate because of matching the similar conditions as in MIS device demonstrated over Au/Cr/PI substrate. Typical survey for low-resolution spectra is presented in Figure 6.5 (a). The observed binding spectra of the TiO_2 film contain the Ti 2p and O 1s peaks of the titanium dioxide and a small amount of contaminating carbon; no other impurities (e.g., chloride ions) were present on the film surface. The survey spectrum of the film surface also contains C 1s and Au 4f, Au 4d peaks in addition to the Ti 2p and O 1s peaks, confirming the presence of the titanium oxide surface modifier. Cr peak is hardly observed at peak position 74.8 eV for Cr 2p, because the emitted photoelectron cannot diffuse out of the TiO_2 and Au films. The spectrum for as-deposited sample contains C 1s peak at 284.8 eV, may be associated with (–C–H–) bond or other carbon contaminated particles in the presence of surfactant triblock copolymer Pluronic P123 over film surface. Further, it was observed that the peak intensity of C 1s was decreased as the sample annealed at 270

℃ for 5 h in O_2-ambient. While the O 1s peaks at 531.8 (as-deposited) and 532.2 eV (annealed at 270 ℃, 5 h), confirm the presence of the surface modifier as peak shifts to higher binding energy (BE) site. The other components near the binding energies of 531.8 and 532.2 eV may mainly correspond to hydrated bonds or carbonate caused by contamination on the film surface.

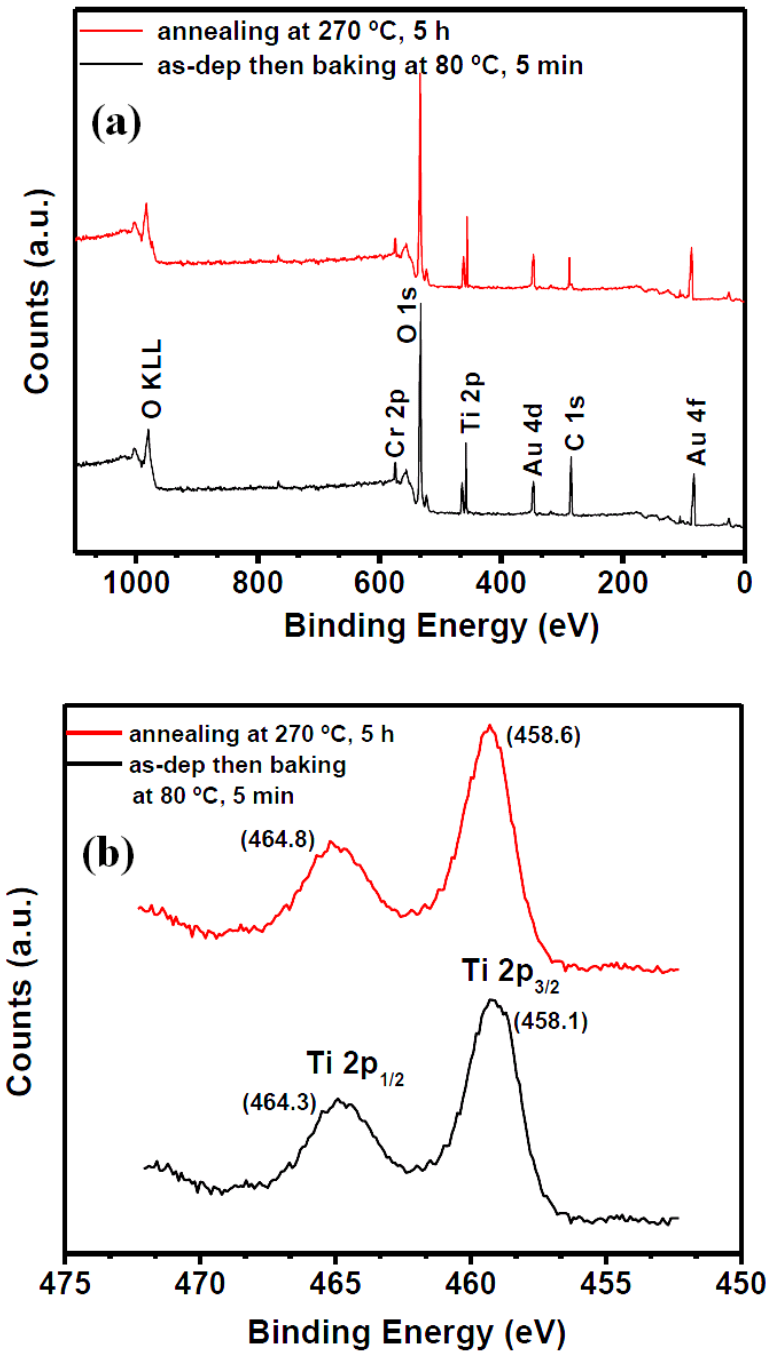


Figure 6.5 (a) Low resolution XPS spectra for dip-coated nc-TiO_2 film over Au/Cr/PI

surface, and (b) high-resolution XPS spectra of the Ti 2p energy levels subjected to baking, and annealing at 270 ℃, 5 h treatment conditions.

The triblock copolymer Pluronic P123 is the uniform-structure-directing agent to prepare nc-TiO_2 film in an aqueous solution and it has been evaporated when the sample heated in O_2-flow at 270 ℃ for 5 h. In order to understand the formation mechanism, the effect of P123 on the morphology of the products was examined first. In an aqueous solution, triblock copolymer micelles tend to form a core–shell structure by the segregation of insoluble blocks into the core and hydrophilic blocks into the shell. From the XPS results, we concluded the that P123 could confine and direct the growth of pure TiO_2 surface observed over flexible PI by dip-coating solution process, which enhance the property of the MIS device. Figure 6.5 (b) displays high-resolution spectra of the Ti 2p energy levels for as-deposited then baked at 80 ℃ for 5 min and annealed at 270 ℃ for 5 h samples. For the baking-only treatment the spin-orbital splitting of Ti $2p_{1/2}$ (464.3) and Ti $2p_{3/2}$ (458.1) peaks was observed with a separation of 6.2 eV. After annealing-only treatment, these binding energies were raised to 464.8 and 458.6 eV, and with the same separation of 6.2 eV. This binding energy shift towards higher BE, which imply that during the annealing in presence of O_2, oxygen molecules reacted with the Ti dangling bonds to form stronger Ti–O bonds and that effectively oxide the as deposited film into the pure TiO_2. This observation is in excellent agreement with the reported literature value [**16, 17**]. From this result, it is clear that the TiO_2 film by dip-coating process was successfully deposited over PI substrate. The shift toward higher BE for the Ti–O bonds suggests that annealing treatment introduced some bonding structures for the oxidation of the Ti atoms.

6.3.4 Water contact angle measurements for nc-TiO_2 film

Self-cleaning properties of TiO_2 film are very desirable, and potentially has various advantages. For example, it can defog glass, and it can also enable oil spots to be swept away easily with water. The effect of calcination temperatures (the as-synthesized samples were calcined at different temperatures) on the physical parameters for time-induced hydrophilicity of TiO_2 film was investigated in this study. The contact angles of water droplets were measured for both the as-synthesized then baking at 80 ℃ and annealing at 270 ℃ samples under ambient conditions. The observed trends can be easily found from Figure 6.6 (a), a noticeable decrease in the water contact angles does not occur upon increase of time. The behavior of contact angle, for sample of as-synthesized then baking at 80 ℃, is probably due to presence of polymer surfactant P123 species. In this case, temperatures are not high enough to promote decomposition of P123, and micelles may be formed because of both organic and inorganic components. It seemed that structural migration of the residual polymer surfactant P123 may affect the contact angle change at the surface of TiO_2 film because the P123 material has amphiphilic nature. For the waiting period of 5 min, no dramatic change (only from 88° to 63° in contact angle) was found over 10 cycles of continuous wetting. The as synthesized then baking only sample showed stable surface with some extent of hydrophobic character, which is probably due to the balance of both polymer surfactant P123 and precursor of TiO_2.

Meanwhile, we performed contact angle measurement for nc-TiO_2 film annealed at 270 ℃ for 5 h in O_2-ambient over 10 cycles of continuous wetting and drying. It was pointed out that the water contact angles of nc-TiO_2 thin films were dramatically decreased with time for 5 min. On the contrary, the sample showed liable hydrophilic nc-TiO_2 film surface, probably due to evaporation of P123. Figure 6.6 (b)

shows the time-dependent change of water contact of nc-TiO_2 film coated over Au/Cr/PI surface. For nc-TiO_2 film, the water contact angle decreased progressively with the number of cycles. After 5 cycles, the water contact angle started decreasing and gradually decreased from 69° (some extent of hydrophobic character) to about 28° (hydrophilic character), while performing the process for 5 min.

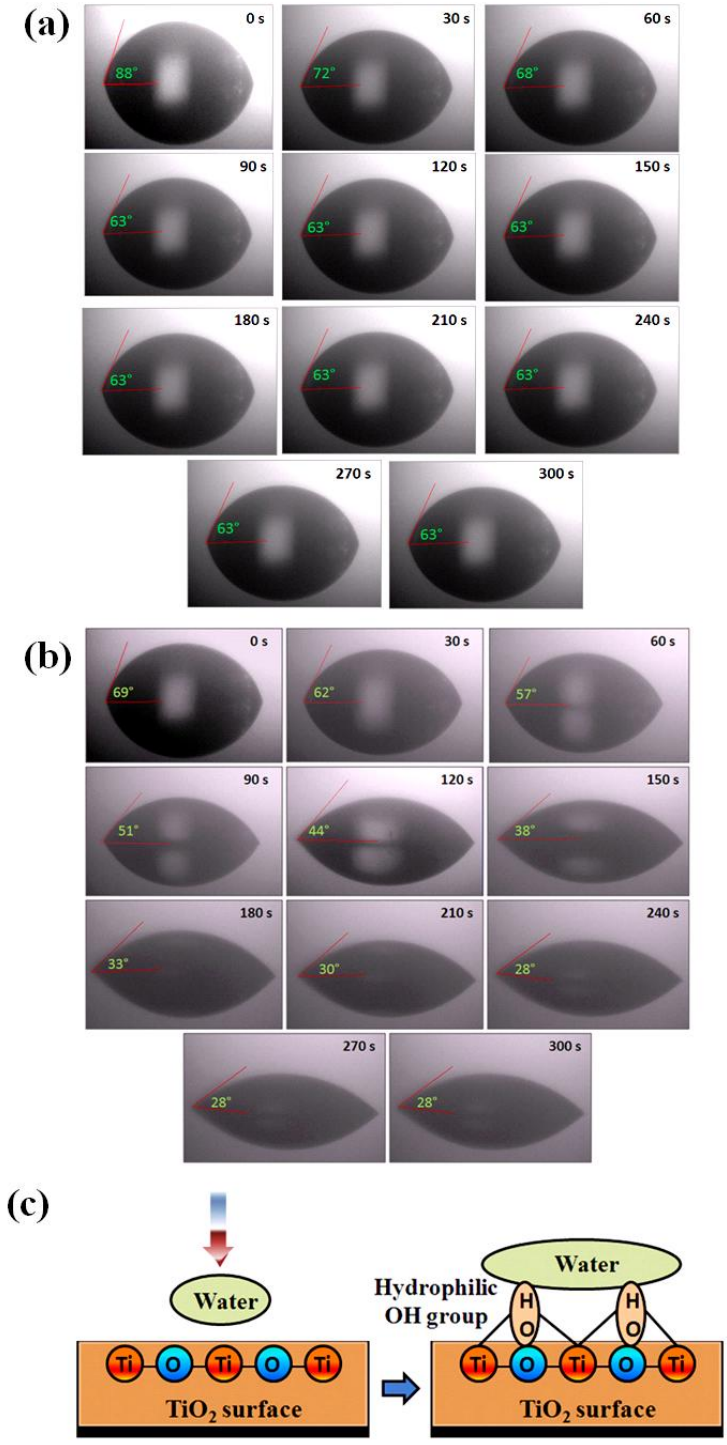


Figure 6.6 (a) Time-dependant change in contact angle of water droplet on as synthesized TiO_2 thin film dip-coated over Au/Cr/PI surface, (b) Time-dependant change in contact angle of water droplet on nc-TiO_2 thin film (annealed at 270 ℃ for 5 h in O_2-ambient) dip-coated over Au/Cr/PI surface, and (c) a schematic for the water drop exposed to the above TiO_2 surface.

A fast decrement in the contact angle occurs for the first 180 sec and then the contact angles gradually decrease and remained constant. The concentration of OH groups available on the surface of nc-TiO_2 film results into time-induced hydrophilicity. Furthermore, our obtained nc-TiO_2 thin film presents more hydrophilic nature than previously reported sol–gel nc-TiO_2 thin film [**13**]. It is significantly interesting that the discovery of the time-induced superhydrophilicity of TiO_2 films has generated numerous exploring issues for future applications such as antifogging, self-cleaning, antibacterial and stain-proofing agents in advanced nanoelectronics. Figure 6.6 (c) depicts the possible surface structure route for sample of nc-TiO_2 film annealed at 270 ℃ for 5 h in O_2-ambient. Initially, the sample surface exhibits some extent of hydrophobic character due to the fabrication sample from P123-assisted dip-coating. However, once the surface contacts with the water drop, the extra surface hydrophilic OH group is formed and the interaction with water drop is gradually increased. [18] How to apply this surface character from both types of samples is an important issue for future study.

6.3.5 Surface analysis study for organic pentacene film

Figure 6.7 (a) shows the XRD pattern and AFM image of 50 nm-thick-pentacene layer grown on as-deposited TiO_2 surface. AFM and XRD experiments were performed in order to investigate the effects of the surface properties of the pentacene

on the surface morphology of gate dielectric. The structure of pentacene layer was elucidated by XRD in reflection mode at 20 kV and Cu Kα radiation (λ=1.5406 Å) with a coupled (θ–2θ) scans configuration. The corresponding XRD pattern contains a series of sharp (0 0 k) peaks indicating that the pentacene film is highly ordered. The first peak at 5.7° (thin-film phase) corresponds to a lattice parameter of 15.6 Å . XRD analysis shows that pentacene film on TiO_2-Au/Cr coated PI have a better crystal quality. The estimated grains size for pentacene film using Scherrer formula for the broad peak at 5.7° is about 500 nm. Since, the pentacene layer is deposited on as-deposited TiO_2 surface, there is no peak observed for TiO_2 film due to the amorphous surface.

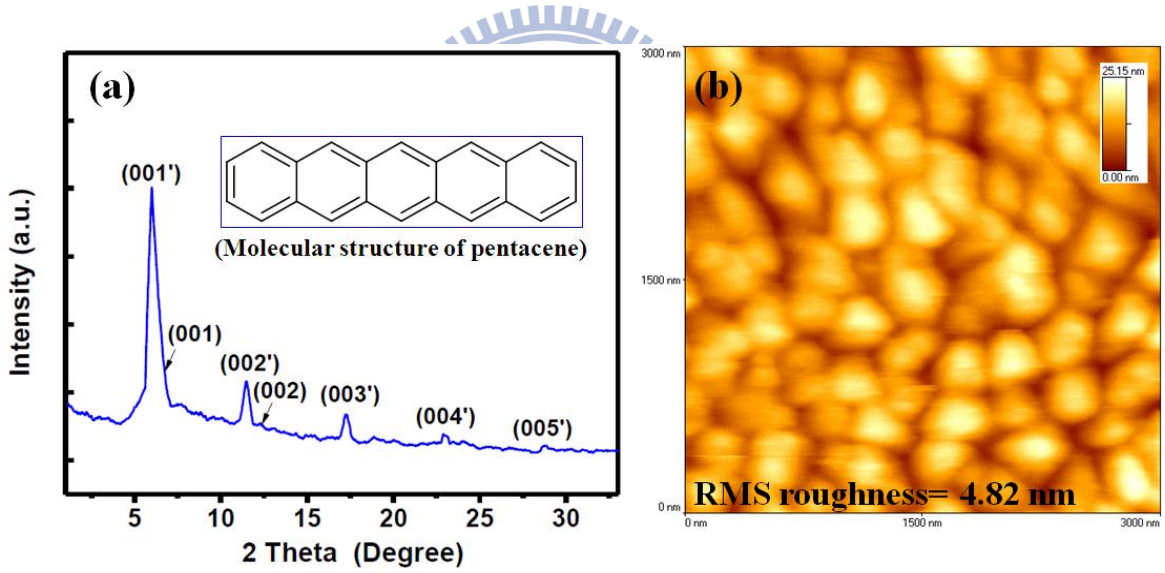


Figure 6.7 (a) X-ray diffraction pattern of the pentacene deposited over TiO_2-Au/Cr/PI. Inset: molecular structure of pentacene, (b) AFM image (3μm ×3μm) of the pentacene over TiO_2-Au/Cr/PI.

Moreover, the grain size and morphology of pentacene film was observed by AFM to assess the crystalline quality, as shown in Figure 6.7 (b). It is well known that the root-mean-square surface roughness (R_{rms}) of a film influences the electrical

characteristics of electrical devices. The R_{rms} evaluated from AFM of pentacene is 4.82 nm as indicated in Figure 6.7 (b). The AFM images of pentacene layer on as-deposited TiO_2 surface also revealed a dendritic structure with a grain size of 500 nm. The data suggest a robust and pinhole-free TiO_2 film, where the growth morphology of pentacene was similar to those prepared on silicon or glass substrate [19, 20]. After analyzing the surface morphology of pentacene film by using XRD and AFM, we confirmed that the deposited pentacene was crack-free, uniform, and well adhered on the surface of TiO_2–Au/Cr/PI. Thus, the pentacene had uniform morphological surfaces.

6.3.6 Electrical measurements from pentacene/TiO_2-Au/Cr/PI structured MIS device

The good quality of an interface between an insulator and a semiconductor layer are extremely crucial for practical device operation and application. The leakage current and capacitance measurements allow the extraction of material parameters, such as dielectric constant and interface density. Here, the MIS structured devices were fabricated over flexible PI substrate for both conditions of as-deposited and annealed films. The dielectric properties of nc-TiO_2 film were evaluated via quantitative current density and capacitance measurements. Figure 6.8 (a) shows typical current density-voltage (J-V) plots for MIS geometry as shown in Figure 6.2 (a) with TiO_2 as insulator layer and pentacene as semiconductor layer.

As Figure 6.8 (a) displayed, the leakage current density of TiO_2 film for as deposited then baked at 80 ℃ is of the order of 10^{-8} A cm^{-2} at applied negative voltage of 0-3 V. After annealing at 270 ℃ for 5 h, it decreased to the order of 10^{-12} A cm^{-2} at negative voltage of 0-5 V. As compared with the silicon based devices under high thermal process, the devices in Figure 6.8 (a) were achieved on relatively low

temperature budget. Hence, the dielectric property of nc-TiO_2 film in the soft device would be expected to affect from some remaining carbon materials and lack of uniformity over nc-TiO_2 surface. However, we noted that the device with nc-TiO_2 film of 25-nm thickness deposited by dip-coating process exhibited superior insulating properties than the conventional silicon based MOS capacitor [**19-24**]. Table 6-1 [24-28] listed various deposition methods, deposited film thicknesses, dielectric constants, leakage current densities and processing temperature on our PI substrate and other silicon-based devices. In general, our soft device with P123-assisted nc-TiO_2 film demonstrated the superior property for low temperature processing issue and low leakage current. The J-V characteristics were measured by inject electron from bottom Au layer to TiO_2 layer (negative bias). Figure 6.8 (b) presents a plot of ln(J) with respect to the square root of the applied voltage ($V^{1/2}$). For standard Schottky–Richardson (SR) emission, the plot of ln(J) versus $V^{1/2}$ should be linear; which can be expressed as [29]

$$J = A^{*}T^{2}\exp\left[\frac{-q(\phi_B - \sqrt{qV/4\pi\varepsilon\, d})}{KT}\right] \tag{6.1}$$

Where A^{*} is the effective Richardson constant, ϕ_B is barrier height, ε is the dynamic electric permittivity, and d is the thickness of the dielectric layer. The plot between ln(J) and $V^{1/2}$ has a linear behavior under negative bias. Thus, due to the fact that the conduction mechanism of the MIS device is Schottky emission, this device has threshold voltage which blocks the leakage current through insulator layer. Further, SR emission induced by the thermionic effect is caused by electron transport across the potential energy barrier, as indicated in the inset to Figure 6.8 (b). This is independent of traps and dominates the conduction mechanism.

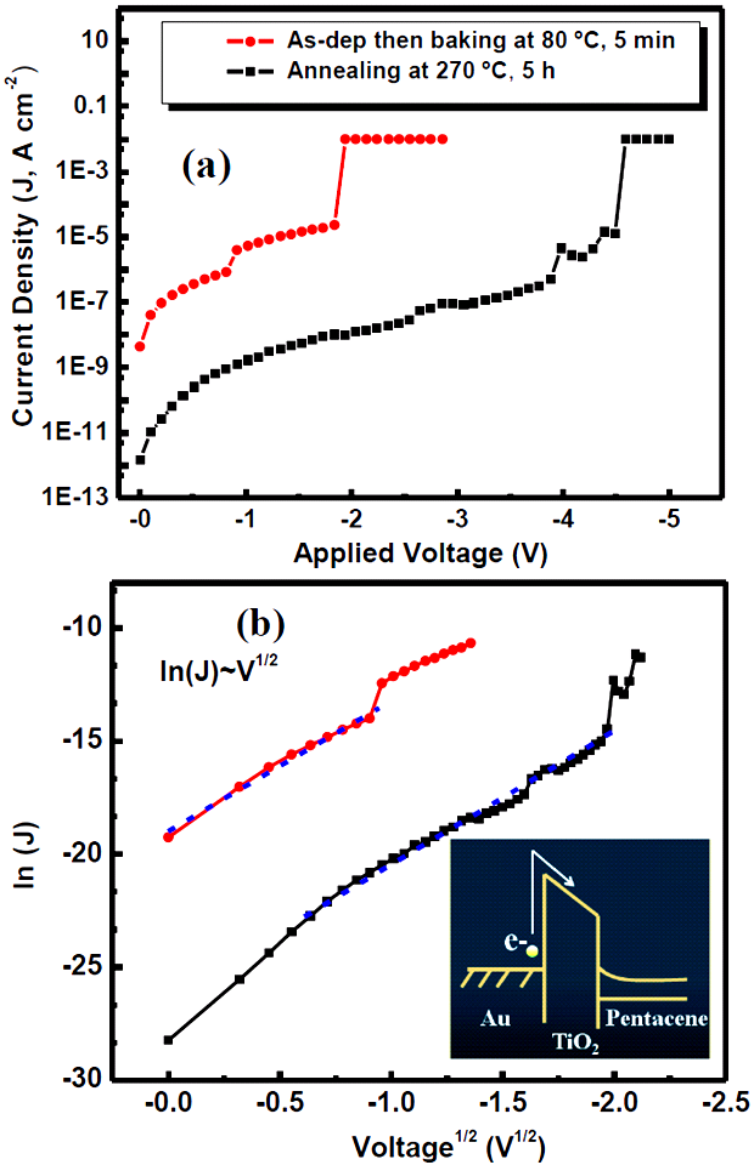


Figure 6.8 (a) J-V characteristic when negative voltage applied, (b) Schottky emission ln(J) versus the square root of the electric field ($V^{1/2}$); Inset: a schematic energy band diagram.

Reference	Deposition process	Film thickness(nm)	Dielectric constant[a]	Leakage current density ($A\ cm^{-2}$)	Temperature (℃)	Substrate
This work	Dip-coating	25	28.8	8.7×10^{-12}	270	Polyimide
[24]	ALD	70	83	10^{-6}-10^{-8}	250	Silicon
[25]	Spin-coating	70	23	10^{-9}-10^{-10}	700	Silicon
[26]	CVD	50	50	5.0×10^{-5}	600	Silicon
[27]	LPD	73	29.5	1.1×10^{-6}	450	Silicon
[28]	Sputtering	15.5	22	2.8×10^{-6}	350	Silicon

[a] Calculated from equation $C_i = \varepsilon_\circ kA/d$ (where k is the dielectric constant, $\varepsilon_\circ$ the vacuum permittivity, A the capacitor's surface area and d the insulator thickness)

Table 6-1 Comparison of various TiO_2 film deposition methods (dip-coating, atomic layer deposition/ALD, spin-coating, chemical vapor deposition/CVD, liquid phase deposition/LPD and sputtering) with respective to thickness, dielectric constant, leakage current, substrate type and growth temperature

Figure 6.9 displays capacitance-voltage (C-V) measurements for TiO_2 films for as deposited then baked at 80 ℃ for 5 min and after annealed at 270 ℃ for 5 h. As viewed by inset of Figure 6.9, the capacitance for as deposited then baked TiO_2 film at 1 MHz is very low. Reasonable capacitance is not observed, which could not afford to minimum requirement of MIS devices. Moreover, good capacitance characteristic is measured while film annealed at 270 ℃ in O_2 ambient for 5 h. Furthermore, according to the capacitance and thickness data, we evaluated the k-value of the annealed sample of nc-TiO_2 film for specific area. The capacitance, C_{MIS} is calculated analogously to the plate capacitor [**30**],

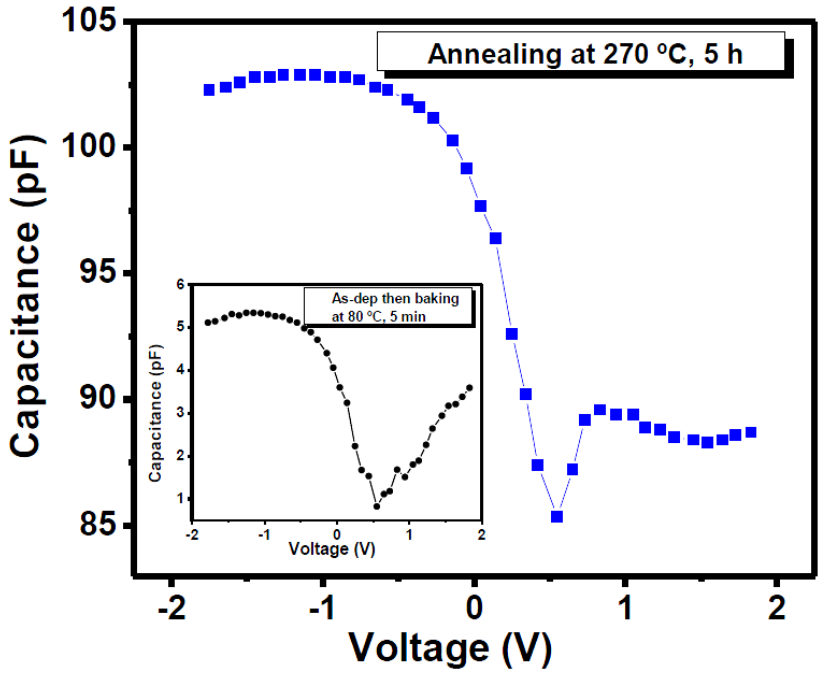


Figure 6.9 C-V plot for MIS structures fabricated with nc-TiO_2 as dielectrics and pentacene as semiconductor layer: Inset shows C-V plot for as-deposited sample.

$$C_{MIS} = \varepsilon_o k.\frac{A}{d} \quad (6.2)$$

Where, k is the insulator's dielectric constant, ε_0 is the permittivity of the vacuum, A is the area, d is the thickness of insulator layer. For specific area (0.01 mm^2), thickness of TiO_2 layer (25 nm) and maximum capacitance (102.3 pF), the calculated dielectric constant is 28.8. This calculated value of k is lower than the standard k-value of TiO_2, consistent with previous calculated k value for TiO_2 on silicon substrate [27, 31, 32]. In table 6-1, the dielectric constant obtained from our nc-TiO_2 film deposited over PI by dip-coating process was similar and equivalent to some of TiO_2 films deposited over silicon substrate. We expect that the good capacitance and high k-value of our flexible MIS device using TiO_2 as dielectric layer would allow future flexible nanoelectronic

devices to be operated in the low voltage and low temperature regime.

6.3.7 Real-Life Flexibility Tests

We estimate the leakage current density for sample treated with annealing (270 ºC, 5 h) in different convex and concave type bending stages to confirm the possibility for use in advanced flexible electronic devices in real life uses. During the manufacturing process, a foil was used to provide these specific bending structures. Both convex (Figure 6.10 (a)) and concave (Figure 6.10 (b)) settings were measured, and the radii of curvature (denoted by R_c) were varied from 1.5 to 4.0 cm. Figure 6.10 (a) shows the current density, J vs R_c measurements plot for 4.0 to 1.5 cm to TiO_2 film. All of the curves exhibited the lowest leakage current densities were found to be about 10^{-12} A cm^{-2} at applied voltage of 0-5 V at stressing for negative biasing conditions after bending the MIS device up to 4.0, 3.5, 3.0, 2.5, 2.0 and 1.5 cm. Here, we choose randon number of device to test the bending efficiency of of MIS devices onto flexible PI. TiO_2 retained its low leakage current density after bending the device minimum upto 1.5 cm in convex type bending shape only a minor change is measured among current density for different R_c but this subtle variation is acceptable. On the other hand, we measured the current density for radius of curvature from 1.5 to 4 cm in concave stages as shown in Figure 6.10 (b). Again, we acquired the lowest leakage current densities under negative biasing conditions for TiO_2–Au/Cr/PI substrate, which were about 10^{-12} A cm^{-2} at 0-5 V. As displayed in Figure 6.10 (a) & (b), the thickness of nc-TiO_2 remained unchanged when the MIS device was subjected to bend from 4.0 to 1.5 cm concave-or convex settings.

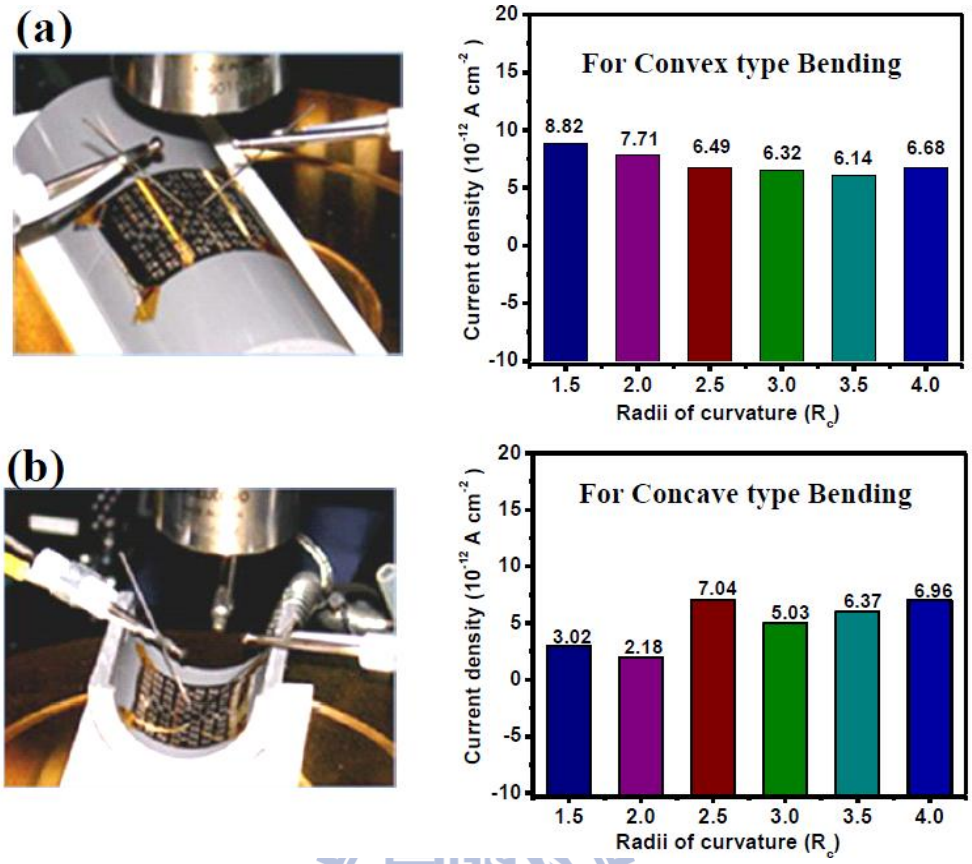


Figure 6.10 Plots for J-R_c measurement from out MIS device fabricated with nc-TiO_2 film; (a) convex shape test, (b) concave shape test.

As PI sheet is bent into convex and concave shapes, the outer surface experiences a tensile strain and the inner surface experiences a compressive strain [2]. During device for convex case, MIS device located on the PI surface suffered tensile strain. In contrast, the device on PI surface suffered compressive strain while concave case. The observed strain effect for MIS device on PI exhibited according to the shift direction of substrate. Thus for many flexible electronic devices, the induced strain could be calculated by the following simple approximation of the relationship between film strain of MIS device (ε_{MIS}) and radius of curvature [33, 34],

$$\varepsilon_{MIS} = \frac{t}{2R_c} \tag{6.3}$$

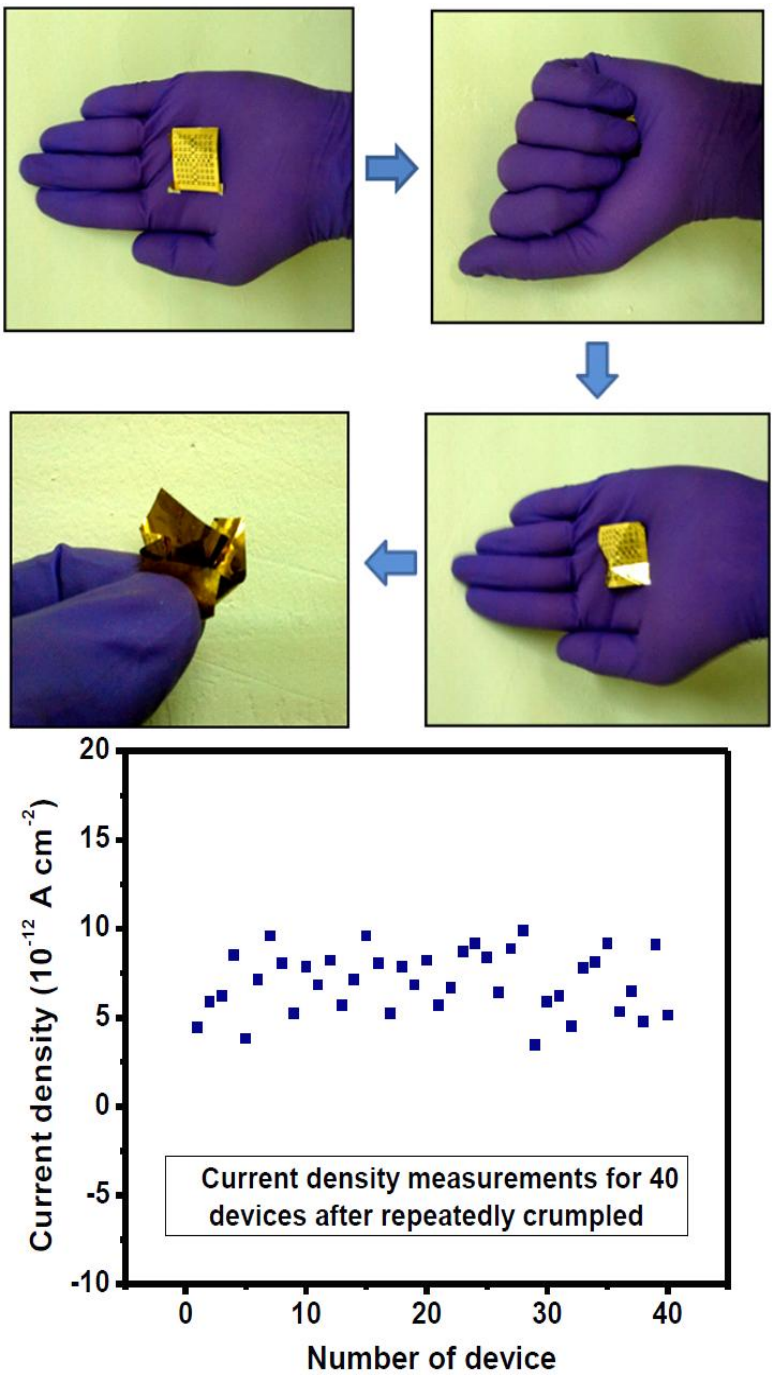


Figure 6.11 Demonstration of the foldable test, one array of flexible MIS devices repeatedly crumpled in the palm of a hand, and the current density measurements for 40 devices.

Where t is the thickness of the substrate and R_c is the radius of curvature. The maximum strain estimation to a minimum radius of curvature (1.5 cm) at which we

measured leakage current for MIS device on PI substrate of thickness of 38-µm is 0.126%. At this strain value, our MIS device functions well without any failure mode. We observed that our flexible MIS device was exceptionally stable against various bending stresses and are bendable, rollable, wearable, and foldable, exhibiting no degradation at maximum tensile strain up to 0.126%. In addition, the dip–coating derived nc-TiO_2 film as dielectric layer and pentacene as semiconductor layer behave towards very stable electrical properties. This observation is consistent with the bending results. From this concave and convex test, we conclude that the nc-TiO_2 based MIS device on a PI substrate had an excellent stability. Hence, these tests open up further application in real life for flexible electronic devices.

After the extent success of bending test in convex and concave type stages, we performed a folding test as shown in Figure 6.11. To observe the foldable behavior of our flexible MIS device, a fabricated flexible array containing 80 MIS devices patterned on an area of 5×5 cm^2. This flexible array was repeatedly crumpled within the palm of the hand, images sequencly depicted in Figure 6.11. Even during this severe mechanical stress, about 50% (c.a. 40 devices) devices operated well with high durability (c.a. 30 days), although some failed due to cracking in the electrode, the semiconductor or the insulator. But, the flexible MIS recovers its initial state after crumpled within the palm of the hand for number of times.

6.4 Summary

We successfully fabricated a fully bendable dip-coated solution-processed nc-TiO_2 thin film based MIS device over flexible PI sheet subjected to a variety of virtual experiences of flexible applications in future. The triblock copolymer P123 was used as a uniform-structure-directing agent. XRD, AFM and XPS analyses

confirmed that the unprecedented flexibility of the solution-deposited TiO_2 by dip-coated originates from the formation of an ultrathin, conformable, coherent semiconductor layer of pentacene with a crystalline-like phase occurred on the plastic PI substrate. For the prepared nc-TiO_2 thin film surface, over 5 cycles of continuous wetting and drying were used to measure the contact angle to further explore applications such as antifogging, self-cleaning, antibacterial and stain-proofing agents in advanced nanoelectronics. Our flexible MIS device was exceptionally stable against various bending stresses and is bendable, rollable, wearable and foldable for waiting period of 30 days; exhibited no degradation at tensile strains up to 0.126%. Thus, the MIS device on flexible PI substrate exhibited high dielectric constant, low leakage current and good capacitance, which is sufficient for the future practical applications. Thus, it should be emphasized that this dip-coating solution process in making organic semiconductor MIS device could be used to demonstrate the low-temperature and large-area flexible electronic devices in future for disposable applications.

Chapter 7: Novel Chemical Route to Produce a New Polymer Blend Gate Dielectric for Flexible Low-Voltage Organic Thin-Film Transistor

7.1 Introduction

Over recent years, there has been increasing diverse curiosity in the development of electronic circuits on flexible substrates to meet the growing demand for low-cost, large-area and lightweight flexible devices for several types of applications such as roll-up displays, e-papers, connectors and keyboards [**1, 2**]. The use of various polymer materials as the dielectric layer has become a topic of interest, which allows an inexpensive solution-phase process desirable for the planned commercialization of flexible OTFTs. Indeed, polymer dielectrics [**3**] are very attractive in electronics applications, because these materials show good characteristics, which can often be formed simply by spin-coating, casting, or printing at room temperature and under ambient conditions [**4, 5**]. Organic/polymer materials have attracted a lot of attention for building large-area, mechanically flexible electronic devices, and thus allowing an inexpensive solution-phase process desirable in the commercialization of OTFTs. These materials are widely pursued since they offer numerous advantages for easy-processing and good compatibility with a variety of substrates including flexible substrates, and great opportunity for structural modifications. Apart from the above, low dielectric constant (low-k) polymer materials are known to decrease lower cross-talk noise, power dissipation, and, when incorporated in device systems, can dramatically decrease resistance–capacitance (R–C) delays [**6**]. As shown in ITRS

guidelines, interlayer metal insulating materials need to have dielectric constants < 2.4 to effectively isolate devices having sizes < 100 nm [**7, 8**]. There is also a strong desire on the part of microelectronic industry to develop advanced, large-scale new composite polymer materials that can meet the growing demand for miniaturization with high-speed performance, and flexibility. To be useful in technological applications, polymer films should have a morphology that either remains stable within an acceptable range of temperatures, or undergoes a transformation in morphology which is controllable and predictable. But researchers have had little success in making new polymer low-k ultrathin films on flexible substrates at room temperature.

A major goal of organic electronics is the development of compatible materials sets, including semiconductors, and insulators, that enable the fabrication of electronic circuits on flexible substrates at low cost and low temperature. The polymer blend dielectric strategy is a general approach to enhance the charge carrier mobility at low temperature. Whether there is a correlation between semiconductor-polymer junction and the nature of the dielectric surface chemical factors underlying such interfacial effects on charge transport. The centre of interest is to demonstrate that OTFT with high mobility for certain semiconductor-polymer interface can be modulated to a very large extent. More recently, the implementation of appropriate insulators facilitates electron transport for typical organic p-type semiconductors have been used as active elements in optoelectronic devices such as OLED [**9**], organic solar cells [**10**], and OTFTs [**11**]. There are many advantages of organic semiconductors, such as easy fabrication, mechanical flexibility, and low cost. Organic semiconductors offer the ability to fabricate electronic device at lower temperature and over large area of various substrates such as plastic and paper. They can be processed using existing techniques used in semiconducting industry as well as chemical synthesis based

dip-coating processing. This manufacturing advantage can bring into exist drastically low-cost, low-temperature processing and pervasive electronic applications such as flexible displays and RFID tags.

In this contribution, for the first time, we present an easy-to-follow synthesis procedure to prepare new organic-organic P123-PS blend thin film as dielectric layer at low temperature. This method is provided the way of preventing the problem of pin-hole defects in pure ultrathin polystyrene film. The electrical properties of the P123-PS blend thin- film have been examined for advanced flexible MIM capacitor applications. The electrical insulating properties of flexible MIM device prepared employing organic P123-PS blend thin film as a dielectric layer exhibited low leakage current density, and better capacitance density. Moreover, the solution-processed P123-PS blend film acted as the gate dielectric to fabricate OTFT device on flexible PI substrate, making them suitable candidates for use in future flexible devices as a stable gate dielectric. We also performed the functional testing for our OTFT device under tensile and compressive bending modes without any deterioration and sterile loss in its electrical performance. These new polymer blend dielectric materials have good stability when using in electronic device as composite dielectric layer, and gives excellent results compared to other polymer dielectric materials.

7.2 Materials and Methods

Common materials used in present work are shown in Figure 7.1 with their respective molecular structures. All the reagents were used without the further purifications. Pluronic® P123 block copolymer surfactant: Triblock copolymer $EO_{20}PO_{70}EO_{20}$, MW=5800, O-BASF Corporation, pluronic P123 is a difunctional

block copolymer surfactant terminating in primary hydroxyl groups, and a nonionic surfactant that is 100% active and relatively nontoxic. Polystyrene ($(C_8H_8)_n$, MW=54000, Aldrich), catalyst chloroform ($CHCl_3$, 98%, Aldrich), and toluene ($C_6H_5CH_3$, Tedia Co. Inc.). Deionized and distilled water (DI water, ddH_2O); DI water used was purified with filters, reverse osmosis, and deinized system until the resistance was more than 18 MΩ.cm^{-1}. DI water was used to clean, wash, and be a solvent. Chromium shots (Cr, 99.999%, ADMAT), size: 3-5 mm, aluminum shots (Al, 99.999%, ADMAT), size: 3-5 mm, gold shots (Au, 98.999%, ADMAT), size: 1-2 mm, were purchased form praxair (Danbury, CN, USA). Organic semiconductor materials, pentacene ($C_{22}H_{14}$) was purchased from Seed Chem. Co., Electronic grade, PTY. LTD. DuPont™ Kapton® Polyimide (i.e., PI) film, of 38-μm thickness of PV9100 series was used as substrate to fabricate the device. Note that all the experiments were performed in air or in a standard fume hood.

Preparation of blend thin-film, P123-PS was synthesized as shown in Figure 7.2. In a typical synthesis experiment, polystyrene (8.5 g) was added into a mixture of P123 (8.0 g), toluene (15.2 ml) and a catalytic amount of chloroform (1.5 g) under static condition. It is then stirred for 12 hour with a magnetic stirrer at room temperature. After P123 and PS were completely dissolved, the solution was used to prepare P123-PS composite thin film. Mixed solution was then applied by dip-coating onto flexible PI substrate in two steps. First, PI raped glass substrate is dipped into a mixed solution for a while and then is withdrawn. Second, it was cured in a vacuum oven at 100 ℃ for 10 min. Then, further characterizations and applications in flexible electronic devices (MIM and OTFT) will be investigated.

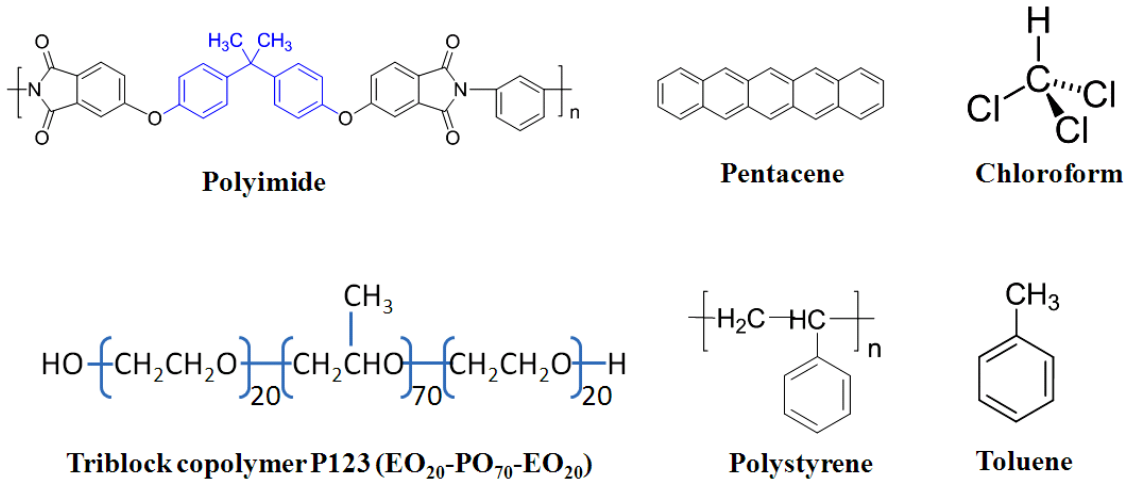


Figure 7.1 Common materials used in present work, Kapton® polyimide, pentacene, chloroform, triblock copolymer P123, polystyrene and toluene and their respective molecular structures.

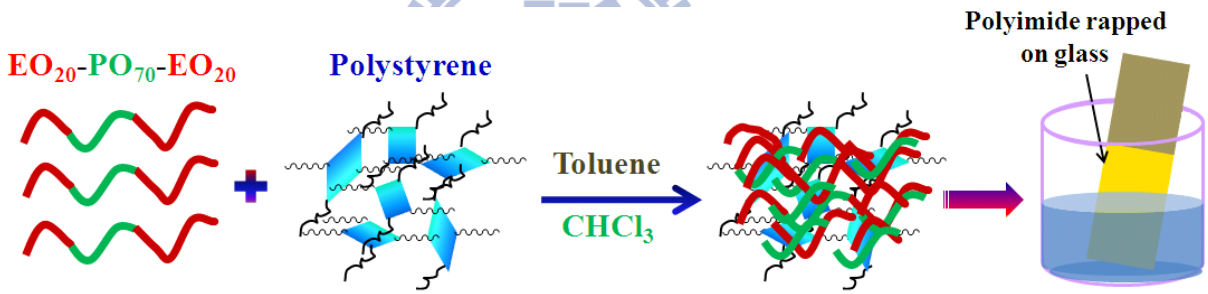


Figure 7.2 Schematic synthesis of triblock copolymer P123 and PS precursors mixed into toluene and chloroform employed for the fabrication of polymer P123-PS blend thin-film on a flexible PI substrate by dip-coating process.

The fabrication process for the flexible MIM and OTFT devices is described as follows: a plastic 38-μm thick DuPont Kapton® PI substrate was used as flexible substrate for the fabrication of MIM capacitor. The PI substrate was cleaned ultrasonically with ethanol (Fluka; water content: < 0.1%) for 30 min and DI water and then high-pressure N_2 gas was used to remove the water and any remaining

particles from the PI surface. After cleaning up, PI substrate was annealed at 200 ℃ for 1 h in vacuum to achieve relatively thermal stability, and enhancement of the adhesion strength. Next, Cr, (20-nm thick) and Au (80-nm thick), were deposited sequentially on the PI substrate by thermal coater. The Cr layer was used as the adhesion layer between the PI substrate and the Au thin film. Au was deposited for the gate electrode over the Cr coated PI substrate. Finally, the P123-PS film for dielectric layer was deposited by using the process as we described in previous section by dipping the sample strip into the solution then cured in a vacuum oven at 100 ℃ for 10 min. At the end of the experiments, 300-nm thick Al films were pattered as the top electrode using shadow mask and a thermal coater. Figure 7.3 (a) shows the schematic view of the P123-PS composite thin film-based MIM device and Figure 7.3 (b) shows a photograph of an array of MIM devices patterned on area of 5× 5 cm^2 on flexible PI substrate.

Making them suitable candidates for use in advanced flexible electronic devices as a stable intermetal dielectric, the electrical insulating properties of P123-PS blend film have been optimized for OTFT on the PI substrate. Figure 7.3 (c) shows the schematic view of the P123-PS blend thin film-based OTFT device and Figure 7.3 (d) shows a photograph of an array of OTFT devices patterned on area of 5× 5 cm^2 on flexible PI substrate. First, we deposited gate electrode Cr (20-nm)/Au (80-nm) sequentially through shadow mask by using thermal coater. Then the P123-PS film as insulator layer was deposited using the solution proceed dip-coating as described in previous section and then pentacene film was deposited as channel layer by a thermal evaporator with the substrate temperature maintained at room temperature. Finally, source (S) and Drain (D) of Au (100 nm) were deposited onto pentacene and P123-PS films through a shadow mask yielded the top-contact electrode OTFTs. The channel length (L) and width (W) were 70 and 2000 μm, respectively.

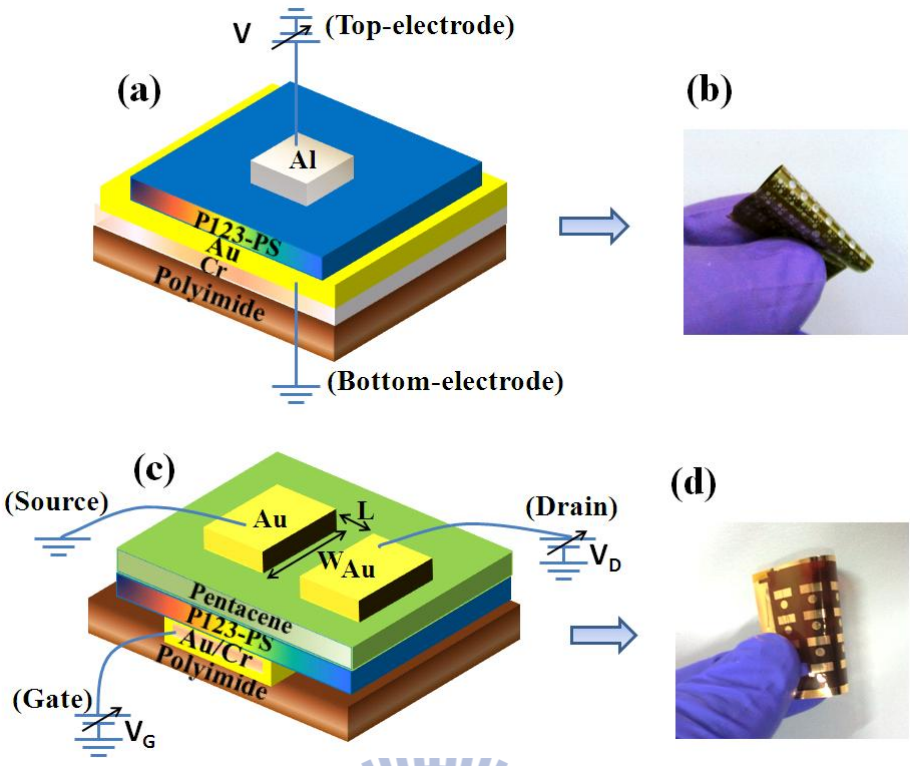


Figure 7.3 (a) Schematic view of P123-PS blend thin film-based MIM capacitor, (b) photograph of flexible MIM capacitors on area of 5× 5 cm^2 on flexible PI substrate; shows the sample bent by hand, (c) Schematic representation of OTFT device features P123-PS as gate insulator and pentacene as semiconductor layer, (d) photograph of the OTFT devices on area of 5× 5 cm^2 on flexible PI substrate.

The surface morphology of the organic-organic, P123-PS blend film over PI was evaluated using AFM (Digital Instruments Nanoscope, D-5000) at scan sizes of 2 μm x 2 μm and a scan rate of 1 Hz. We used ellipsometery techniques to measure the thickness of the P123-PS thin-film. FT-IR spectrum was collected with the use of KBr pellets (2 mg per 300 mg KBr) on a spectrometer (Model 580, Perkin-Elmer) with a resolution of 4.00 cm^{-1}. An infrared spectrum was recorded in the range of 500–4000 cm^{-1} to determine the functional groups in molecular structure. The FT-IR measurement was carried out at room temperature. The water contact angle for P123-PS film surface was measured using a commercial contact angle meter.

Deionized water was used as the water source in the contact angle experiment. The contact angles measured for 1 h after the drop has made contact with the film surface under test over flexible PI substrate. X-ray diffraction (XRD) pattern for organic pentacene film was also observed using a Rigaku D/max-IIIB diffractometer using Cu Kα radiation (λ =1.5406 A$^{\circ}$). Measurement of leakage currents and capacitances in MIM structured device for P123-PS film was performed using an Agilent-4156 probe station and an HP-4284A C–V analyzer, respectively. The output and transfer characteristics of the OTFT measured using Agilent-4156 probe station in the normal environment conditions.

We tested two additional features of our OTFT on PI to explore its feasibility for use in practical applications. We estimated the mechanical strain on the electrical properties under the flexibility test, which includes tensile and compressive strains for minimum radii of curvature (R_c = 1.5 cm). In prior to manufacturing process, a foil was used as a support substrate to provide this specific bending conditions in convex and concave settings for radii of curvature of 1.5 cm, (shown elsewhere). We have also calculated the maximum strain for the OTFT device to be bent to a radius of curvature of 1.5 cm without any degradation loss.

7.3 Results and discussion

7.3.1 P123-PS film quality and surface roughness

When a new cross-linker polymeric dielectric film is fabricated on flexible substrate, it is necessary to optimize the nature of the film surface. AFM data provide important information of surface roughness for initial material evaluation. It is well known that pure PS film below 100 nm thickness suffers by pinhole defects as reported previously [**12-14**]. In our experiment, we also observed the pinhole defects

in polystyrene film of thickness about 20 nm as shown in Figure 7.4 (a). But this problem was prevented when we used P123 and PS mixed with organic additives as P123-PS blend film was successfully deposited without any pinhole defects. The thickness of the film was 28-nm, estimated by ellipsometery techniques. The surface morphology of P123-PS film was investigated using AFM picture analysis at scan size of 2 µm × 2 µm, shown in Figure 7.4 (b). For AFM image, this sample was prepared by a dip-coating process on flexible PI substrate. The surface morphology of the P123-PS film deposited on flexible PI, a clear and easy to perceive, uniform and crack-free surface has occurred. The average root-mean square (R_{rms}) roughness evaluated from AFM image of P123-PS was approximately 0.86 nm. In case, the possible reason for the excellent surface roughness in P123-PS may be due to the presence of P123. It is believed that in-situ deposition of matrix composite deposition, P123 acts as a uniform structure-directing agent [**15**]. The block copolymer P123 in a ternary system makes it possible to deposit uniform film through organic–organic cooperative assembly. It is well know that, in a ternary copolymer-selective solvent system, block copolymers can self-assemble into a variety of lyotropic liquid crystals microstructures consisting of lamellar, cubic or hexagonal structure [**15, 16**]. After analysis of the surface morphology of polymer blend film, we confirmed that the deposited P123-PS film was crack-free, uniform, and well adhered on the surface of PI.

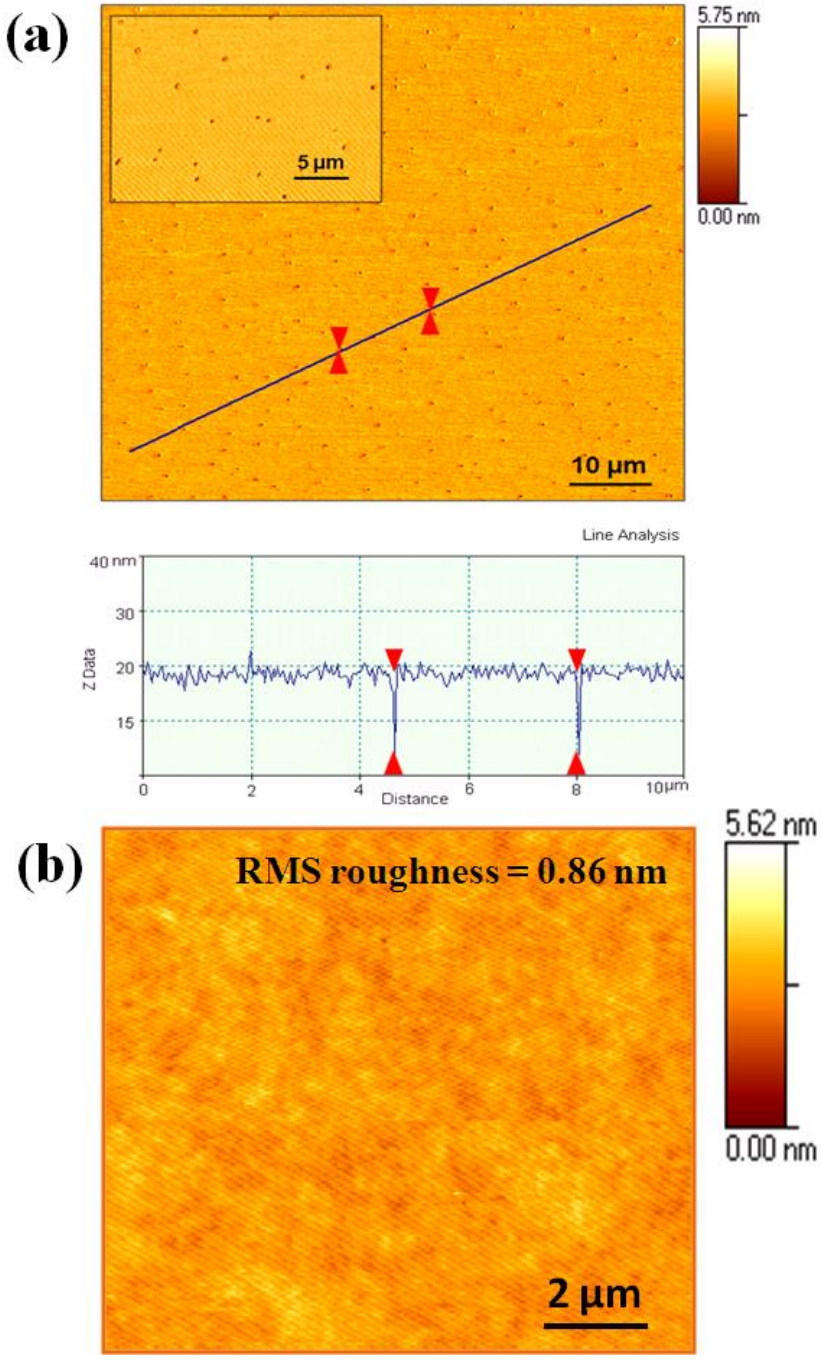


Figure 7.4 (a) AFM image from pure polystyrene film coated on flexible PI substrate, where pinholes defective surface clearly viewed, and (b) AFM image from P123-PS blend film coated on flexible PI substrate.

These materials are made up of a long string molecules consisting of carbon atoms covalently bonded with other atoms. The covalent bonds within the molecules are very strong and rupture only under extreme conditions. This mechanism of aggregation of copolymer P123 and PS molecules is based on the physical evolution during aging, suggested by A. C. Pierre [**17**]. From a physical point of view, the major differences come from the rather weak Van der Waals intermolecular forces that bind together the molecules in crystalline π-conjugated organic solid and the chains in polymer compounds. Addition of pluronic P123 leads to an association of the surfactant molecules to the PS micelles and mixed micelles are formed. The size and structure of the mixed micelles as well as interparticle interactions were studied by varying the surfactant-to-copolymer (P123/PS) molar ratio. The novelty of this study consists of a composition-induced structural change of the mixed micelles with aging at constant temperature. The current mechanism is just a theoretical assumption and at the same time reasonably not confirmed by any experimental analysis. When the solution used for film deposition, they gradually change to a stable polymer-blend film during in-situ growth, as well as self-organized for further characterizations and device applications.

7.3. 2 FT-IR analysis

To gain the more insight about the functional groups, FT-IR spectrometer was used to examine the functional groups of the polymer blend P123-PS thin film surface. The IR absorption spectrum of the organic P123-PS blend thin film after baked at 100 ℃ is shown in Figure 7.5. The spectra for the P123-PS film deposited with organic additive thin film have a sharper spectral profile, which means that films have less disordered structure. As shown in Figure 7.5, a sharp peak due to the benzene functionalized PS stretching mode appears at 720, 758, 1385 and 1452 cm^{-1} in the

absorption spectrum. The two peaks at 2929 and 3030 cm^{-1} are due to methylene group of PS. Bands between 2877 cm^{-1} and 2960 cm^{-1} are believed to be due to CH_3, CH_2 and CH stretching, which can be detected from copolymer P123. While a sharp peak at 1170 cm^{-1} for C-O-C bending mode probably occurred from P123. It is ambiguous to tell the origin of the 1720, 1735 and 1780 cm^{-1} peaks appeared for C=O from organic PI surface. The peaks at 1496 and 1600 cm^{-1} from stretching mode for the C=C in ring for PS or PI surface can be detected also. The IR spectrum of P123-PS blend thin film over PI is more consistent for PS and P123 with that reported previously [**18, 19**]. From the FT-IR spectrum, it could be concluded the disappearance of the toluene, and chloroform successfully when the sample was baked at 100 ℃. Finally, we concluded from the results that the sample consisted of PS, P123, and a small amount of contaminating carbon; no other impurities (e.g., chloride and organic ions) were present on the film surface.

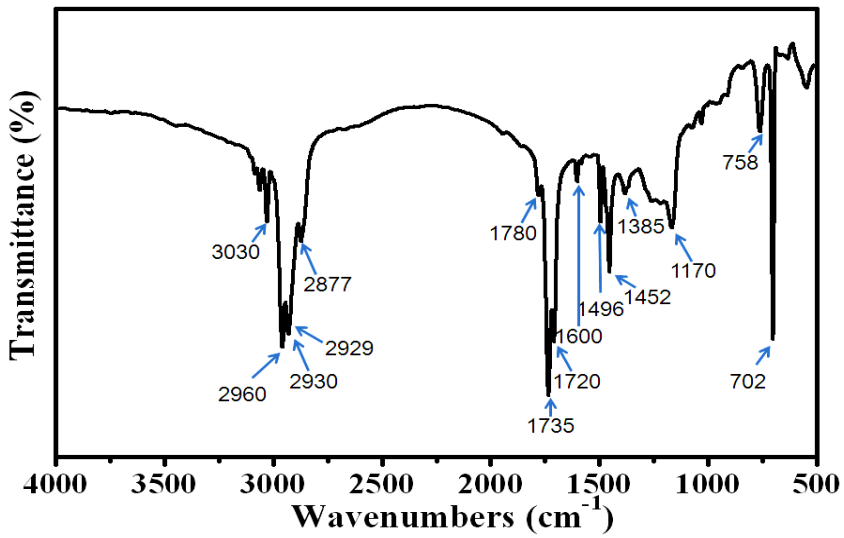


Figure 7.5 FT-IR spectra from P123-PS thin film over flexible PI substrate.

7.3.3 Water contact angle measurements for P123-PS film

We combine experimental and theoretical study to characterize the aggregation steps at the surface of P123-PS blend film. This blend surface from

triblock copolymer P123 and PS materials is of great interest in its own right. Distilled-water contact angle measurements were carried out to investigate the surface energy of the P123-PS blend surface (Figure 7.6). The contact angle of a sessile drop on P123-PS layer was directly measured by aligning a tangent for 1-60 min with the drop profile at the point of contact with the surface. The film surface showed hydrophobic effect with contact angle of 111° at the point of contact. For P123-PS film, the water contact angle negligibly changed from 111° to 105° after 1 h. We measured the contact angles 111°, 108°, 105° and 105° for 1, 20, 40, and 60 min, respectively as shown in Figure 7.6 (a). We concluded that the P123-PS blend film deposited on flexible substrate had stable hydrophobic surface as water contact angle did not significantly change with time.

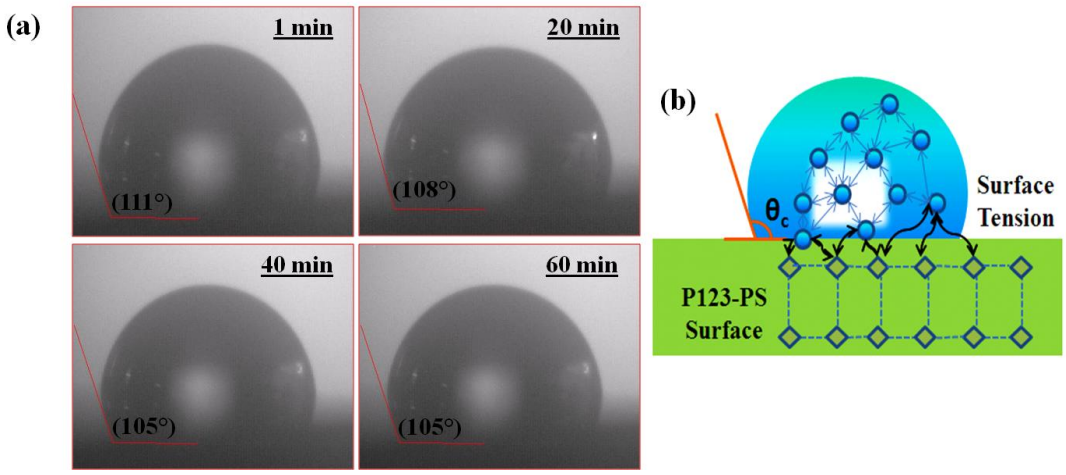


Figure 7.6 (a) The contact angle measurements for 0-60 min with the drop images at the point of contact on the P123-PS surface, (b) schematic representation of surface tension to calculate the surface energy for P123-PS surface.

If the surface is hydrophobic then the contact angle of a drop of water must be larger and the lower surface energy (or Surface tension). A rather simple method of

estimating the surface energy of solid surface was developed by Fox et al. [**20**]. The surface energy value for most inorganic solids is on the order of hundreds or thousands of mJ m^{-2}, and for polymers it is at least an order of magnitude lower. Solid substrates are often considered to be either high energy surfaces (metals, glass, and ceramics) or low energy surfaces (polymers). Based on the theoretical explanations, we designed a schematic illustration to calculate the surface free energy for the blend surface of P123 and PS, shown in Figure 7.6 (b), indicating the surface tension, contact angle and attraction force. The surface free energy ($\gamma_{P123\text{-}PS}$) for P123-PS layer can be calculated using the following equation [**21**];

$$\gamma_{P123\text{-}PS} = \frac{\gamma_W}{4} \times (1 + \cos\theta_c)^2 \qquad (7.1)$$

Where θ_c is the contact angle at equilibrium and γ_W is the water surface free energy (73 mJ m^{-2}). The values of $\gamma_{P123\text{-}PS}$ for P123-PS blend film from contact angles were determined to be 7.5 mJ m^{-2}, 8.7 mJ m^{-2} and 10.1 mJ m^{-2} for contact angles 111°, 108°, 105°, respectively by using the Equation 1. We have pointed out the very low surface energy for composite P123-PS surface than pure PS surface [**21**]. The improvement of the stable hydrophobic surface with the incorporation of P123 is the main reason for the suppression of the lowest surface energy in the P123-PS blend surface. The subtle change in surface energy of 0.025% is estimated for the contact angle of a sessile drop on P123-PS layer after the waiting period of 1 h. Excellent hydrophobic nature of the P123-PS suggests the use of this new polymer blend film in screening for excellent hydrophobic surface mutants and in the isolation of hydrophobic bacteria from nature. Moreover, in OTFTs, the surface of the dielectric layer is important for effective performance because it allows for a conducting

channel in the interface between the dielectric layer and semiconductors. The low surface energy of the dielectric layer allows the vertical growth of pentacene molecules. As the holes could easily be move in the vertical direction of pentacene molecules, these vertical alignments of pentacene enhance mobility in OTFTs [**22**].

7.3.4 Electrical measurements from MIM capacitor device

A capacitor (formerly known as condenser) is a passive two-terminal electrical component used to store energy in an electric field. The forms of practical capacitors vary widely, but all contain at least two electrical conductors separated by a dielectric (insulator). When there is a potential difference (voltage) across the conductors, a static electric field develops across the dielectric, causing positive charge to collect on one plate and negative charge on the other plate. In practice, the dielectric between the plates passes a small amount of leakage current and also has an electric field strength limit, resulting in a breakdown field. Electrical characterizations were undertaken to investigate the electrical insulation properties of the polymer blend film. First, we measured the insulator properties for PS film as shown in Figure 7.7. Leakage current density-electric field (J-E) measurements were performed on P123-PS blend thin film in MIM structured device (Figure 7.3 (a)) to determine the leakage current characteristics and dielectric breakdown field. The J-E response is also used to determine the available range for high-quality capacitance density-voltage (C-V) measurement.

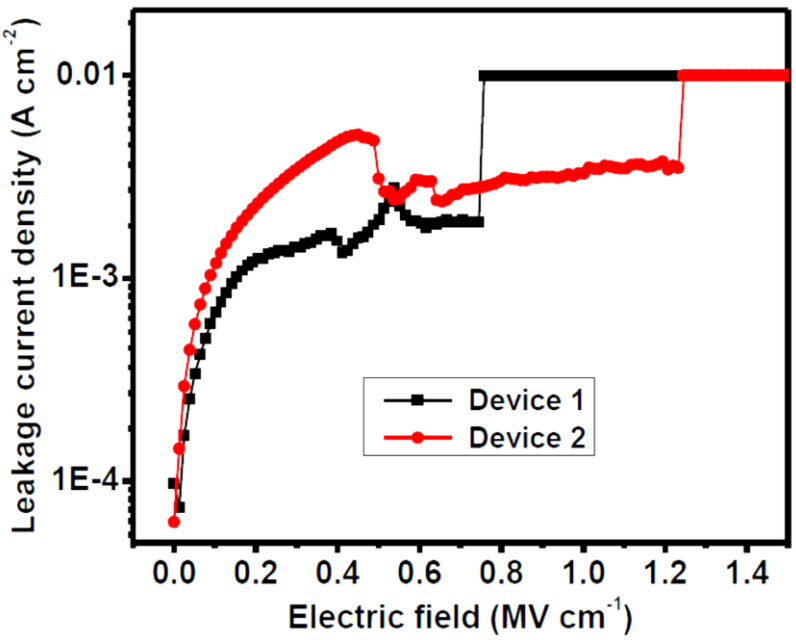


Figure 7.7 J-E plots from MIM structured device having PS film as gate insulator layer

We pointed out the poor device performance since the leakage current was very high (~10^{-4} A cm^{-2}) and breakdown field very low (< 1 MV cm^{-1}) due to the film affected by pinhole defects. But, the insulator properties were enhanced further for P123-PS film as this film was free from pinhole defects. Figures 7.8 (a) & (b) show typical J-E and C-V plots for MIM configurations fabricated with P123-PS blend thin film as an insulator layer. As displayed in Figure 7.8 (a), the lowest leakage current density of P123-PS film, are 1.17×10^{-11} A cm^{-2}, 1.19×10^{-11} A cm^{-2} and 1.07×10^{-11} A m^{-2} at applied electric field of 5 MV cm^{-1}, 6 MV cm^{-1} and 10 MV cm^{-1}, respectively. The probe was moved to different three points in random order on P123-PS based MIM capacitor and exhibited a similar leakage current behavior and excellent break down limit of the film. The break down field for the P123-PS blend film was about 8.5 MV cm^{-1}. On the basis of this result, we concluded that the film is of very high quality and showed extremely good insulator properties.

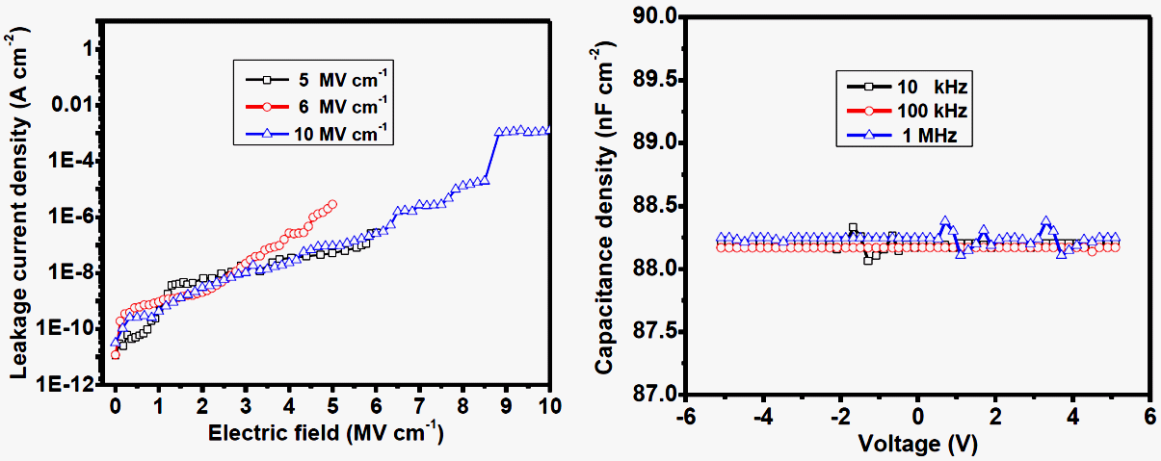


Figure 7.8 (a) J-E and (b) C-V plots for MIM structured device fabricated with P123-PS blend thin film as gate insulator layer.

Figure 7.8 (b) displays a characteristic C-V plot for P123-PS. As shown in Figure, the capacitance of P123-PS blend film to different three points at 10KHz, 100KHz and 1 MHz are 88.2 nF cm^{-2}, 82.01 nF cm^{-2} and 81.1 nF cm^{-2}, respectively. J-E and C-V results demonstrated that the blend film generated by P123 and PS materials dissolve into organic solvents exhibit superior insulating properties versus the corresponding neat polymers, and compared many other previously reported materials (Table 7.1) [**3, 23-25**]. Then, according to the capacitance and thickness data, we evaluated the k-value of the P123-PS blend film using the following equation [**26**].

$$C_{P123\text{-}PS} = \frac{C}{A} = \frac{k\varepsilon_o}{d} \quad (7.2)$$

Where, *k* is the insulator's dielectric constant, ε_0 ~8.85 × 10^{-12} F m^{-1} is the permittivity of the vacuum, *A* is the area of the capacitor, *d* is the thickness of insulator layer. The average k-value of P123-PS film is approximately 2.7 estimated from three point measurements for $C_{P123\text{-}PS}$ 88.2 nF cm^{-2} (at 10 kHz), 88.2 nF cm^{-2} (at 10 kHz) and 88.2 nF cm^{-2} (at 1 MHz). This calculated low-k value is consistent with other polymer gate dielectrics as indexed in table 7.1. The obtained results show that the P123-PS blend polymer is a good potential candidate to replace SiO_2 or other low-k intermetal dielectric materials, and could be an ideal alternative for flexible devices. Moreover, the flexible capacitors invent using this blend polymer could be widely used in electronic circuits for blocking direct current while allowing alternating current to pass. In filter networks, for smoothing the output of power supplies, in the resonant circuits that tune radios to particular frequencies and for many other purposes. This blend film based capacitors has to be proposed excellent general purpose plastic film capacitors; ideal for low power RF and precision analog applications.

Reference	Material	Film thickness (nm)	RMS roughness (nm)	Dielectric constant[a]	Leakage current density (A cm^{-2})	Substrate
This work	P123-PS	28	0.86	2.7	1.07×10^{-11}	Polyimide
Org Elec[23]	PMMA	100	0.52	3.5	$\sim10^{-7}$	Glass
JACS[24]	PVP	133	6	6.4	$\sim 10^{-8}$	Silicon
JACS[24]	PS	122	2	2.6	$\sim 10^{-9}$	Silicon
JACS[24]	CPVP-C_n	18-20	2-8	6.1-6.5	10^{-9}-10^{-10}	Silicon
JACS[24]	CPS-C_n	10-13	1-10	2.5-3.0	10^{-8}-10^{-9}	Silicon
Chem Com[3]	PAA	330	4	4.9	$\sim 10^{-8}$	ITO Glass
Lit value[24]	SiO_2	300	2	3.9	10^{-9}-10^{-10}	Silicon
APL[25]	Al_2O_3	120	--	8.6	10^{-8}-10^{-9}	Silicon

*n = 0, 2, 6 & *a = calculated dielectric constant

Table 7-1 Comparison of electrical properties of various low-k dielectric materials

7.3.5 Pentacene: a model for ordered organic semiconductors

High quality interface between an insulator and a semiconductor layers is dramatically impacts semiconductor devices in practical applications to the operation and markets of the electric power industry. It has been suggested that it might be possible to achieve higher mobilities by designing π-conjugated molecules that stack face-to-face (π-stacking) in the close crystalline state, thus increasing the intermolecular interactions [**27, 28**]. In particular, we used typical crystal structured planar π-conjugated pentacene for semiconductor organic layer to demonstrate the OTFT device using P123-PS blend polymer as gate insulator. Figure 7.9 (a) & (b) show the AFM image and reflective XRD pattern of 50 nm-thick pentacene layer grown over P123-PS/Au/Cr/PI substrate. AFM and XRD experiments were performed in order to investigate the effects of the surface properties of the pentacene on the surface morphology of P123-PS blend film. AFM image of pentacene at scale length of 5 μm (Inset: 2 μm) showed the crystalline quality (Figure 7.9 (a)). The R_{rms} evaluated from AFM of pentacene is 5.14 nm. The AFM images of pentacene layer over P123-PS surface showed the growth of thick, uniform, high-quality film. The data suggest robust and almost symmetric crystalline pentacene, which also has large, densely packed and well-interconnected grains. The growth morphology of pentacene was similar to those prepared on silicon and PI substrates as previously reported [29, 30].

The structure of pentacene layer was elucidated by XRD data (Figure 7.9 (b)) in reflection mode at 20 kV and Cu Kα radiation (λ=1.5406 Å) with a coupled (θ–2θ) scans configuration. The corresponding XRD pattern contains a series of sharp (0 0 k) peaks indicating that the pentacene film is highly ordered. The first peak at 5.3° (thin-film phase) corresponds to a lattice parameter of 15.6 Å. XRD analysis showed that pentacene film on P123-PS have a better crystalline quality. The crystallite size

was estimated for the broadening of the diffraction peaks using the Scherrer equation: $D = 0.89\lambda/\beta \cos\theta$, where D is the crystallite size, λ is the wavelength of the x-ray radiation (λ=1.5406 A°), β is the peak width at half-maximum height after subtraction of the equipment broadening, 2θ = 5.3° for (101), and 0.89 is the Scherrer constant. The estimated grains size for pentacene film using Scherrer formula for the broad peak at 5.3° are about 550 nm.

Pentacene is the material of popular choice for research on OTFTs because of the good charge carrier mobility and its ability to form large well-ordered crystalline structure [**31**]. Pentacene exhibits a conjugated π-electron system, formed by the p_z-orbitals of sp^2-hybridized atoms, which extends over the whole molecule. In a single pentacene molecule, the weakest π-bonding results in a lower electronic excitation (π-π* transitions). The occupied π level is also commonly called highest occupied molecular orbital (HOMO), while the unoccupied π* level is referred as lowest unoccupied molecular orbital (LUMO). As in inorganic solid materials, the electron levels responsible for the electrical conduction are the ones which are closest to the Fermi energy, which lies between the HOMO and the LUMO and characterize therefore the electronic states responsible for the conduction and for the optical properties. The bands structure of conjugated pentacene molecules are schematically represented in Figure 7.9 (c). The larger molecular orbitals (HOMO-LUMO) become narrow bands (small bandwidth, ω ≈ 1.1 ev) and makes for better π-π* overlap to reduce the energy bandgap about 2.3 eV. In general, the HOMO-LUMO gap in pentacene is found to be 2.7 eV. In particular, assuming a relative molecular orientation similar to the single-crystal phase; the both of HOMO and LUMO bandwidths increase by a few tenths of an electron volt with respect to the bulk phase, with a consequent reduction in the energy band-gap.

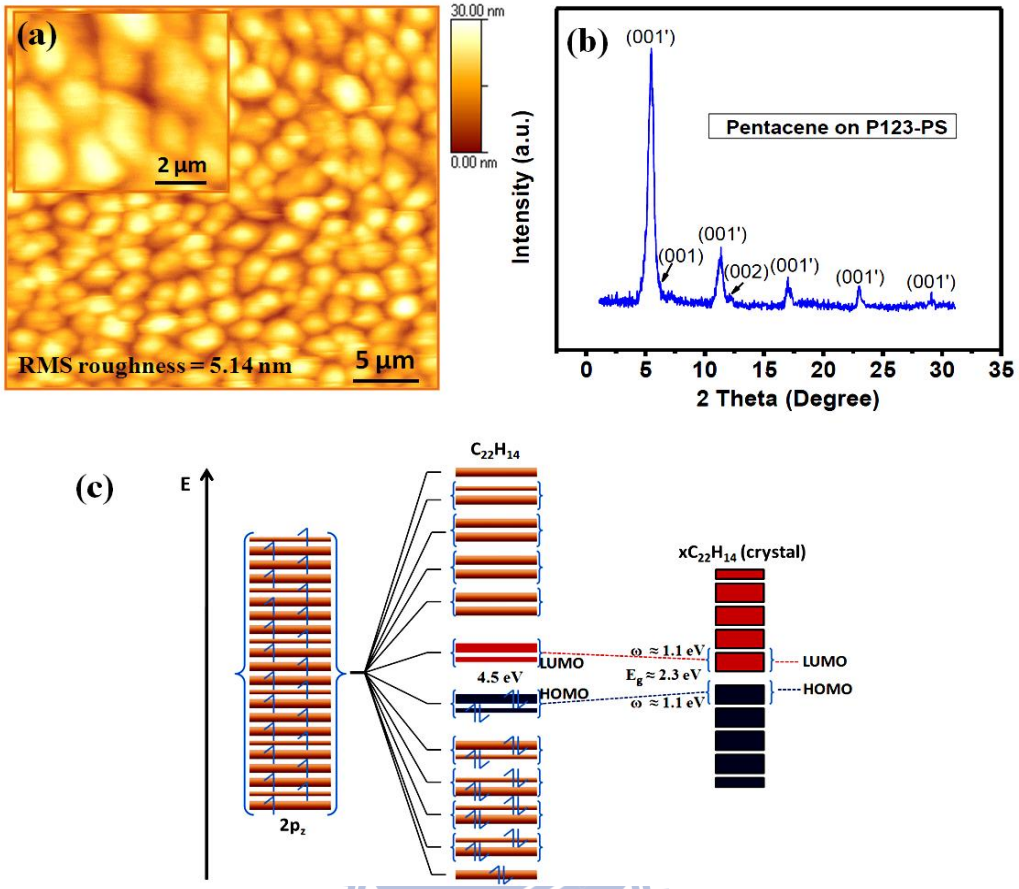


Figure 7.9 (a) AFM image (b) XRD pattern from Pentacene film deposited on P123-PS film over Au/Cr/PI substrate, and (c) schematic representations of the orbital energies and the corresponding symmetries of molecular orbitals of a pentacene molecule in HOMO-LUMO states obtained from density-functional theory calculation.

This theoretical explanation suggest the assumed molecular arrangement as a possible candidate for the orientation in real pentacene thin film samples, and call for further experimental work aimed to determine the real mutual molecular orientation. This theoretical simulation for the pentacene molecule is based on the excellent agreement with recent study [**32, 33**], as far as the symmetries and the orbital character of HOMO and LUMO are concerned. Thus the strong contribution of $2p_z$ orbitals in pentacene's HOMO and LUMO is the molecular reason of pentacene's

semiconductivity. In comparison to inorganic crystals, the reduced bandwidth tends to localize the charges. But in case of single crystalline pentacene, the concept of valence and conduction band are replaced by the HOMOs and LUMOs of the organic crystals, which are mainly located at the molecules sites but weakly interacting with each other. Only at low temperature and in case of pentacene well ordered purified organic crystals the transport may be described in term of band transport for pentacene. Thus, pentacene in our experiment is good choice to use as semiconductor active channel layer than other organic materials to demonstrate OTFT.

7.3.6 Electrical measurements from OTFT device

In order to show the performance of the polymeric P123-PS blend film as a dielectric layer, we fabricated the pentacene-based OTFT with device geometry as shown in Figure 7.3 (b). Figure 7.10 (a) represents the drain current-drain voltage (I_{DS}-V_{DS}) output curve obtained from our OTFT with P123-PS as dielectric layer and pentacene as channel layer with channel length (L) = 70 μm and channel width (W) = 2000 μm. The device demonstrated desirable low-operating voltage p-type OTFT characteristics at an operating voltage of -5 V. The maximum saturation current of ~ 6.1 $\times 10^{-5}$ was achieved at V_{GS}= -5 V. The observed OTFT characteristics conformed closely to conventional transistor characteristics in both the linear and saturation regimes to drain current increasing linearly at low drain voltage, and clear saturation behavior at high drain voltage. The drain current–gate voltage (I_{DS}–V_{GS}) transfer curve of pentacene OTFT on P123-PS blend gate dielectrics (Figure 7.10 (b)) showed that OTFT yielded high current on/off ratios ($I_{on/off}$ = 5×10^5) and negligible gate-sweep hysteresis. The values of carrier mobility, (μ_{OTFT}) and threshold voltage (V_{th}) were calculated in the saturation regime using the equation [11],

$$I_{DS} = \mu_{OTFT} C_i \frac{W}{2L} (V_{GS} - V_{th})^2$$

(7.3)

Where, C_i is capacitance of the polymer blend P123-PS gate dielectric. The OTFT displayed a threshold voltage of -1V and carrier mobility of 0.16 cm^2 V^{-1} s^{-1}. The OTFT performance is comparable to values recently reported for polymer gate dielectrics and surpassing to those of devices employing organic semiconductor materials for channel layer grown on the silicon/glass substrate [**34, 35**]. In particular, replacement of the traditional gate dielectrics used in complementary metal-oxide semiconductor (CMOS)-like logic circuits with the polymer blend gate dielectric systems introduced here requires formation of an OTFT at the interface between the organic semiconductors and the P123-PS gate dielectric.

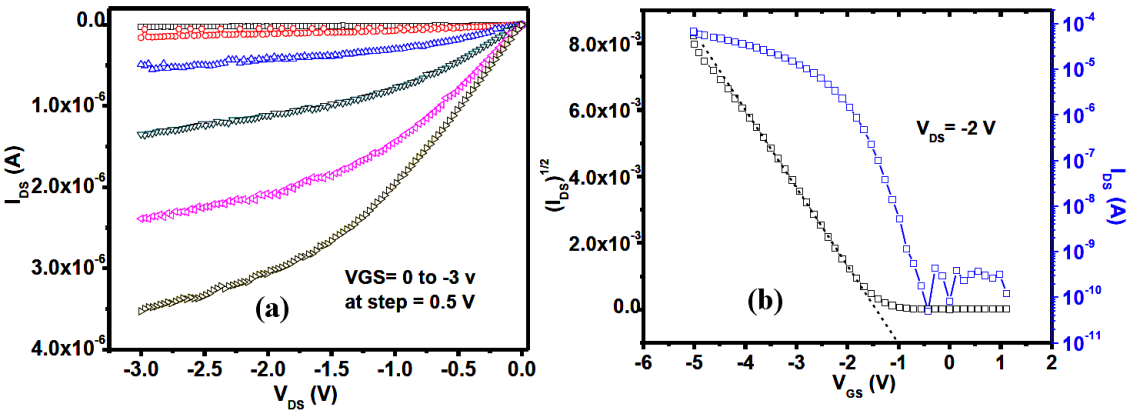


Figure 7.10 Plots for OTFT (a) output characteristic (I_{DS}–V_{DS}), while V_{GS} ranging from 0 to -5.0 V at -1 V step, and (b) transfer characteristic (I_{DS} – V_{GS}), when V_{DS}= -2 V.

7.3.7 Flexibility test for OTFT

Every material, in its native form, has an inherent molecular structure that gives it certain tendencies in terms of film stress. Thus, to gain the feasibility of our OTFT device, we tested two additional features for its use in practical applications. Namely, we estimated the transfer characteristics both in tensile mode (Figure 7.11 (a) and compressive mode (Figure 7.11 (b)), for minimum radius of curvature (R_c) of 1.5 cm to gain maximum strain for our OTFT. Prior to manufacturing process, a hard plastic foil was used as a substrate support to provide these specific bending conditions as presented in inset of Figures 7.11 (a) & (b), respectively. The transfer characteristics show very little change in terms of on–to–off current (3×10^5), V_{th} (-0.8), and mobility (0.15) for both tensile and compressive strains were applied. We concluded from the results that the flexible OTFT device with good transistor properties has been developed with P123-PS as a gate insulator and pentacene as p-channel organic semiconductor.

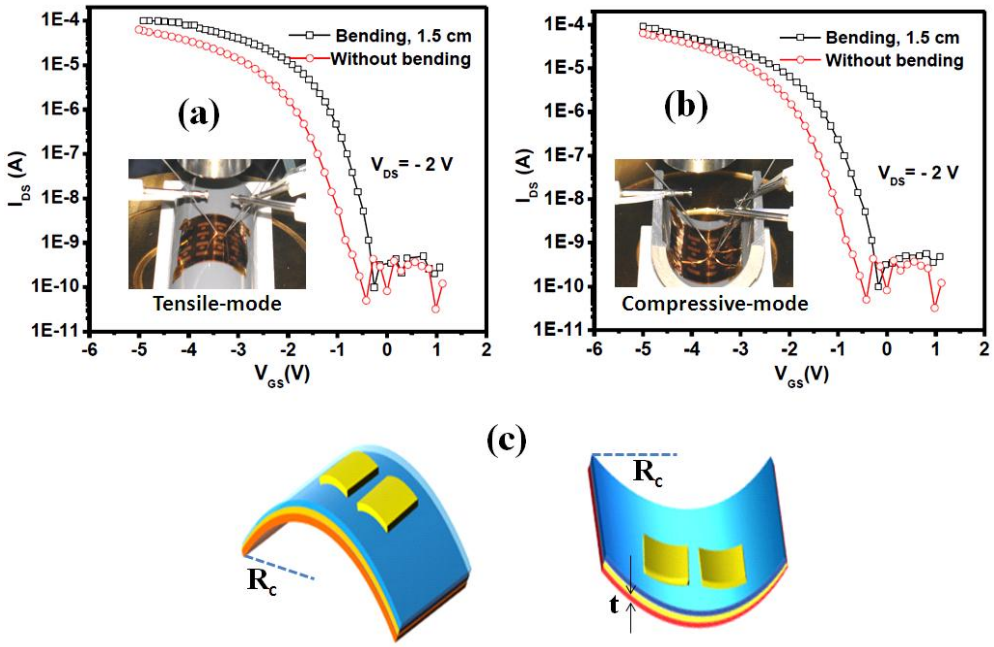


Figure 7.11 I_{DS}–V_{GS} plots for OTFT, while device experiences (a) tensile mode for bending deflection at1.5 cm, (b) compressive mode at1.5 cm; Inset: images show

their respective actual images during measurement, (c) schematic geometries for flexible substrate, the thin film experiences tensile and compressive strain; R_c: radius of curvature, and t: thickness of substrate.

Additionally, we deduced that mechanical strains influence the energy barrier height between the grains of pentacene thin films, thereby resulting in the variation of channel resistances. Finally, the fatigue test revealed that the OTFTs in this study exhibited supreme flexibility, especially under tensile and compressive bending conditions for radius of curvature of 1.5 cm. The flexible PI substrate is bent into convex and concave shapes, the outer surface experiences tensile strain and the inner surface compressive strain as indicated in Figure 7.11 (c). Films deposited on flexible substrate that may shift strain distribution, thus for many flexible electronic devices, the strain could be calculated by the following simple approximation for the relationship between film strain and radius of curvature [**36, 37**].

$$\varepsilon_{OTFT} = \frac{t}{2R_c} \tag{7.4}$$

Where t is the thickness of the substrate and R_c is the radius of curvature. To make a rough strain estimate for our OTFT to a minimum radius of curvature (1.5 cm) at which we measured the transfer characteristics to gain maximum strain for substrate (ca. PI) of thickness 38-μm. The estimated strain is 0.126%; at this value, our OTFT device functions well without any failure mode. We observed that our flexible OTFT device using polymer blend P123-PS as gate dielectric was exceptionally stable against various bending stresses and could become bendable, rollable, wearable, and

foldable, exhibiting no degradation at maximum tensile strain up to 0.126%. From this concave and convex test, we conclude that the P123-PS as gate insulator based OTFT device on a PI substrate had an excellent stability. This result emphasized the importance of these tests in future to open up a way to use them in real life flexible electronic device applications.

7. 4 Summary

We demonstrated an innovative approach for deposit a new organic–organic (P123-PS) blend thin film on flexible polyimide substrate by a novel chemical synthesis dip-coating method at low temperature (c.a. 100 ℃). The planar aggregation of pluronic EO_{20}-PO_{70}-EO_{20} triblock copolymer P123 and polystyrene materials is probably due to strong dipole-dipole interaction and high molecular weights. Good insulating properties in the polymer matrix made it, an ideal dielectric film to be use in device applications. The time-induced contact angle measurement for P123–PS layer shows excellent hydrophobic surface with low surface free energy of 7.12 mJ m^{-2}. In addition, the polymeric P123-PS in a sandwich-like configuration (metal-insulator-metal) shows low leakage current density (~10^{-11} A cm^{-2}) and good capacitance density (88.2 nF cm^{-2}). OTFT device based on P123-PS as gate insulator and conjugated π-electron system organic pentacene as semiconductor layer was successfully constructed and exhibit excellent device performance (e.g. carrier mobility, 0.16 cm^2 V^{-1} s^{-1}; on-to-off current ratio, 5×10^5) and good device stability. Moreover, the OTFT device performance under bending modes of tensile and compressive strain are among the best results for these materials adopting bottom-gate configuration, which is attributed to the high-quality dielectric/organic semiconductor interface formed. Finally, it should be emphasized that this novel synthesized dip-coating method provides a new way to investigate the surface of polymeric blend

films and could be a promising approach for practical applications since it is a low-cost and low-temperature manufacturing technique.

Chapter 8: Conclusions and Future Perspectives

8.1 Conclusions

Flexible organic electronic devices offer significant benefits compared to traditional silicon based electronics. The flexible devices designed and fabricated in this work are light weight, flexible, conformal, and can be formed entirely on a flexible substrate utilizing a room temperature, low cost sol-gel and dip-coating solution proceeding techniques. These high-k films are good candidates for reducing feature size in microelectronic products to meet challenging requirements.

In chapter 4, we prepared MIM-structured capacitors using ultrathin 10-nm high-k HfO_2 films deposited through sol–gel spin coating on flexible PI substrate. The material properties and electrical performances of these films verified the effectiveness of applying low temperature plasma processing to the fabrication of future soft devices. The HfO_2 film exhibited a low leakage current density of 3.64×10^{-9} A cm^{-2} at 5 V and a maximum capacitance density of 10.35 fF μm^{-2} at 1 MHz. The electrical behavior analyzed under various bending treatment conditions revealed that our flexible capacitor functioned independent of the bending conditions (i.e., the number of bends and the bending radii). The electrical characteristics of our flexible MIM capacitors suggest they are comparable with those of silicon- and glass-based capacitor devices, even after bending the devices up to 100,000 times. We believe that

amorphous high-*k* HfO_2 is a leading candidate for use in future flexible devices as a stable gate dielectric fabricated through processing at low temperatures.

In chapter 5, we fabricated a new and fully flexible organic poly-3-hexylthiophene (P3HT) p-type TFT on a transparent flexible polyimide substrate using high-k HfO_2 as dielectric layer and Si_3N_4 as passivation layer via very simple and cost-effective sol–gel spin-coating technique. Defects in the HfO_2 films are expected to be rarely induced, because of the low temperature deposition process and plasma treatment. Current–voltage characteristics of the device in MIM structural device imply the success of using Si_3N_4 over HfO_2 to achieve the satisfactory leakage current. The fabricated devices exhibit good electrical performance with saturation mobility of 0.041 $cm^2\ V^{-1}s^{-1}$. Moreover, the device demonstrates stable performance over the course of bending up to 1000 times and radii of curvature minimum down to 2 cm in both convex and concave type structures. Our results suggest that the P3HT semiconductor material in together with HfO_2 film followed by Si_3N_4 as passivation layer are promising materials for the low-cost flexible electronic devices.

In chapter 6, for the first time, we present an interestingly new and easy-to-follow synthesis procedure to prepare triblock copolymer surfactant P123-based nc-TiO_2 thin film dielectric layer at room temperature via the dip-coating solution process. The electrical insulating properties of fully bendable MIS device prepared employing nc-TiO_2 film as a dielectric layer and pentacene as semiconductor layer, exhibited low leakage current density, and good capacitance with high durability. We realized that the dip-coating technique provides a uniform thin film deposition level on flexible substrate at low temperature than other standard thin film deposition techniques. This new synthesis process to fabricate nc-TiO_2 at low temperature have good stability when using in electronic device as dielectric layer, and gives excellent results compared to other high-k dielectric materials. We expect that these important features will allow this

novel synthesis route and deposition method to be used at large scale in flexible electronic device applications.

In chapter 7, for the first time, we present an easy-to-follow synthesis procedure to prepare new organic–organic P123–PS blend thin film as dielectric layer at low temperature. This method is provided the way of preventing the problem of pin-hole defects in pure ultrathin polystyrene film. The electrical properties of the P123–PS blend thin-film have been examined for advanced flexible MIM capacitor applications. The electrical insulating properties of flexible MIM device prepared employing organic blend thin film as a dielectric layer exhibited low leakage current density, and better capacitance density. Moreover, the solution-processed blend film acted as the gate dielectric to fabricate pentacene OTFT device on flexible PI substrate, making them suitable candidates for use in future flexible devices as a stable gate dielectric. We also performed the functional testing for our OTFT device under tensile and compressive bending modes without any deterioration and sterile loss in its electrical performance. These new polymer blend dielectric materials have good stability when using in electronic device as composite dielectric layer, and gives excellent results compared to other polymer dielectric materials.

8.2 Future Perspectives

The future research plan will revolve around issues facing the electronics engineering (more specifically flexible) community. As a part of the present work, it could be focus on incorporating four major components into future research program: design, fabrication, circuits and applications. As a part of this rapidly evolving field of flexible, it is extremely necessary to look beyond conventional CMOS to develop low-power, high performance devices and systems solutions for the future electronics.

In addition, this issue intends to investigate further design and fabrication using solutions precede and develop a design automation flow for the same. We strongly feel that for these new device concepts to be applied into real-world solutions, it is extremely necessary that they fit into the well-refined design flow used in today's semiconductor industry. It is also necessary to develop roll-to-roll capable of fully utilizing the power and performance afforded by these novel devices along-with mechanically-stable support to extract maximum benefits. While the research community understands and recognizes these challenges in flexible electronics, there is relatively low understanding of the economic impact of manufacturing decisions. In future research interest is to fabricate bendable functional devices from DNA and Proteins. Researchers are ready to constantly seek the formation of conducting nanowires to study charge transfer in one or two dimensions rather than in the bulk. Such wires also hold promise as novel materials for optoelectronics, energy storage devices, logic circuits and sensors. DNA has several inherently useful properties such as long-range order and flexibility.

Considering that flexible electronics in future finds several applications in displays, healthcare, bio-medical implants in together which enables cost reduction of these products would be a big advantage for the semiconductor industry in the times to come. In some instances, it is compatible than traditional Si-based electronics by high-speed reel-to-reel fabrication, high mechanical flexibility, transparent to visible/UV radiation, and the circuit board to conform to a desired shape or flex during its use. Thus, in future research program intend to integrate all the four above mentioned components while at the same time keeping economic feasibility an important consideration. We expect brighter flexible electronics future.

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Appendix

Curriculum Vitae

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CAREER-OBJECTIVE

Intend to build a career with leading research institute/corporate of hi-tech environment with committed and dedicated people, which will help me to explore? Myself fully and realize my potential and to put all my efforts in a deed that enriches the life of my fellow beings.

EDUCATIONAL-QUALIFICATION

Doctor of Philosophy (**Ph D)**
Institute of Nanotechnology, National Chiao Tung University, Taiwan
Year of completion: February, **2012**
Course work (Total credits: **16**) **Percentage: 88 %**

Master of Technology (Solid State Technology),
Department of Physics and Meteorology, Indian Institute of Technology (IIT)
Kharagpur (WB), India
Year of passing: May, **2007** **CGPA: 7.81/10**

Master of Science (Physics), 1st Div
Department of Physics, Aligarh Muslim University, Aligarh (UP), India
Year of passing: **2005** **Percentage: 61.00%**

Bachelor of Science (Physics-Hons), **1st Div**
Department of Physics, Aligarh Muslim University, Aligarh (UP), India
Year of passing: **2002** **Percentage: 60.01%**

List of Publications

International Journals

[**1**]**. Jagan Singh Meena**, Ming-Ching Chu, Yu-Cheng Chang, Chung-Shu Wu, Feng-Chih Chang and Fu-Hsiang Ko, "Novel chemical route to produce polymer blend gate dielectric for advanced flexible organic thin-film transistor", Manuscript to be submitted.

[**2**]**.** Min-Ching Chu, Hsin-Chiang You, **Jagan Singh Meena**, Shao-Hui Shieh, Chyi-Yau Shao, Feng-Chih Chang, and Fu-Hsiang Ko, "Low cost zinc-acetate solution processed ultra-thin film transistors" *J. Electrochem. Soc.* Manuscript to be submitted.

[**3**]**. Jagan Singh Meena**, Min-Ching Chu, Yu-Cheng Chang, Chung-Shu Wu, Feng-Chih Chang, Srikanth Ravipati and Fu-Hsiang Ko, "Facile synthetic route to implement a fully bendable organic metal-insulator-semiconductor device on polyimide sheet", *Org. Electron.* **2012**, Accepted, in press. (**SCI, IF=3.99**)

[4]. **Jagan Singh Meena,** Ming-Ching Chu, Chung-Shu Wu, Srikanth Ravipati and Fu-Hsiang Ko, "Environmentally stable flexible MIM capacitors using zirconium-silicate and hafnium-silicate thin film composite materials as gate dielectrics", *J. Nanosci. Nanotechnol.* **2011**, 11, 6858-6867 **(SCI, IF=1.41)**.

[5]. **Jagan Singh Meena,** Ming-Ching Chu, Chung-Shu Wu, Feng-Chih Chang and Fu-Hsiang Ko, "Highly reliable HfO_2-Si_3N_4 stacked heterostructure to fully flexible

poly-(3-hexylthiophene) thin-film transistor", *Org. Electron*. **2011**, 12, 1414-1421. **(SCI, IF=3.99)**

[6]. Jitendra N. Tiwari, **Jagan Singh Meena**, Chung-Shu Wu, Rajanish N. Tiwari, Min-Ching Chu, Feng-Chih Chang and Fu-Hsiang Ko, "Thin-Film Composite Materials as a Dielectric Layer for Flexible Metal–Insulator–Metal Capacitors", *Chem. Sus. Chem*. **2010**, 3, 1051-1056. (**SCI, IF=6.32**)

[7]. Jagan Singh Meena, Min-Ching Chu, Shiao-Wei Kuo, Feng-Chih Chang and Fu-Hsiang Ko, "Improved reliability from a plasma-assisted metal-insulator-metal capacitor comprising a high-k HfO_2 film on a flexible polyimide substrate", *Phys. Chem. Chem. Phys*. **2010**, 12, 2582-2589. (**SCI, IF= 3.45**)

[8]. Jagan Singh Meena, Min-Ching Chu, Jitendra N. Tiwari, Hsin-Chiang You, Chung-Hsin Wu, Fu-Hsiang Ko, "Flexible metal–insulator–metal capacitor using plasma enhanced binary hafnium–zirconium–oxide as gate dielectric layer", *Microelectron. Reliab*. **2010**, 50, 652-656. (**SCI, IF= 1.1**)

[9]. Min-Ching Chu, **Jagan Singh Meena**, Chih-Chia Cheng, Hsin-Chiang You, Feng-Chih Chang, Fu-Hsiang Ko, "Plasma-enhanced flexible metal–insulator–metal capacitor using high-k ZrO_2 film as gate dielectric with improved reliability", *Microelectron. Reliab*. **2010**, 1098-1102. (**SCI, IF= 1.1**)

International Conferences and Symposiums

[1]. **Jagan Singh Meena**, Min-Ching Chu, Chung-Shu Wu, Feng-Chih Chang and Fu-Hsiang Ko "Highly reliable HfO_2-Si_3N_4 stacked heterostructure to fully flexible poly-(3-hexylthiophene) thin-film transistor" *Symposium on Nano Device Technology (SNDT)*, pp.32 April **2011**, Hsinchu, Taiwan. (Poster)

[2]. **Jagan Singh Meena**, Min-Ching Chu, Jitendra N.Tiwari and Fu-Hsiang Ko, "Flexible poly (3-hexylthiophene) thin-film transistor with improved reliability" *218th ECS Meeting*, 1814, October **2010**, Las Vegas, USA. (Oral)

[3]. **Jagan Singh Meena**, Min-Ching Chu, and Fu-Hsiang Ko, "Flexible MIM Capacitors using Zirconium-Silicate and Hafnium-Silicate as Gate-Dielectric Films" *IEEE International Nanoelctronics Conference (INEC)*, pp. 97, January **2010**, Hong Kong, China. (Oral)

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[5]. Min-Ching Chu, **Jagan Singh Meena**, Hsin-Chiang You and Fu-Hsiang Ko, "Flexible Metal-Insulator-Metal Capacitor using Plasma-Enhanced High-k ZrO_2 film as Gate Dielectric film with Improved Reliability using Zirconium-Oxide as Gate Dielectric Layer", *International Electron Devices and Materials Symposium (IEDMS)*, November **2009**, Taoyuan, Taiwan. (Poster)