國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

矽質奈米級電子元件的研究

A Study of Silicon Nanoelectronics Devices

研 究 生： 林建宏

指導教授：張國明 博士

中華民國九十三年六月

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摘要

操作奈米尺度的元件近年來在各個產業被都被廣泛的討論著。在奈米尺度下，材料的特性以及載子的傳輸的機制，因為表面原子數佔總原子數的比例上升，與塊材(Bulk Material)有相當程度上的差異。在本篇論文中，我們採用掃描探針微影術 (Scanning Probe Lithography)，以鄰近樣品表面的探針引起局部的陽極氧化反應，配合 Tetramethylammonium Hydroxide (TMAH) 對矽的晶向選擇性蝕刻，在 Silicon on Insulator (SOI) 的晶片上，製作出不同的奈米元件結構，探討在奈米尺度下的一些電流傳導現象。我們嘗試製作具有單電子傳輸特性的元件，並在低溫下確實的發現其特性。

A Study of Silicon Nanoelectronics Devices

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Abstract

Manipulating devices in nanometer scale have been widely studied in many industries recently. The characteristics of material and the carrier transport phenomena in nanometer scale structures are much different to which in the bulk material due to the increasing ratio of surface atoms to volumetric atoms. In this thesis, we utilize the scanning probe lithography method, employing a proximal probe near the sample's surface to induce local anodic oxidation, and orientation dependent wet etching with tetramethylammonium hydroxide (TMAH) on SOI wafer. We fabricate different nanostructures devices to measure some carrier transport phenomena in nanometer scale. In advance, we tend to fabricate a device with single electron transport phenomenon, and recover the characteristic we wish in the low temperature.

誌 謝

回首兩年來的點點滴滴，要感謝的人實在太多。如果不是這麼多的人在特定的時間點的適時的出現，本論文是沒有辦法順利完成的。首先，要感謝我的指導教授 張國明博士，在他悉心的指導和鼓勵下，使我能順利的完成學業和實驗，以及同步輻射的 許鉦宗博士，熱心提攜和幫忙，讓本研究得以順利的進行。

接著，要感謝實驗室的成員們，學長們無私的訓練和提供經驗，特別是游凱翔學長，一步一步的傳授做實驗的秘訣與方法，使我受用不盡。以及同期的夥伴們在做實驗時互相的扶持與協助，讓實驗的進行在嚴謹中卻又多了一份活力。

感謝交大電子所梁年來的栽培及系所老師們的教導，奈米中心、國家豪微米實驗室、同步輻射中心提供研究的環境和設備。由於你們的幫忙，使我能在一流的環境中從事研究工作。

最後，要感謝我的父母親和兄長們，因為你們的關心與支持，讓我在無後顧之憂下，順利的完成學業和論文，謝謝你們。

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Chapter 1

Introduction

1.1 General Introduction

As the feature size of ULSI devices continue to shrink, the ability to precisely control the device patterns becomes more and more series. The lithography performance is a key issue for us to entrance the next generation ULSI device. But with the shrinkage of the device size to the nanometer scale, quantum effects become feasible and play an important role to influence the device's property. Despite the difficulty we faced in device fabrication, manipulating device structures below 100 nm is a marvelous thing to researchers in many different fields, just like Richard Feynman [1] said: "There's Plenty of Room at the Bottom". With the device size decrease to the nanometer scale, the ratio of surface atoms to the bulk atoms in the device becomes more significant. This small device property is good for us to fabricate bio-sensors [2] with high sensitivity. Also, since the device size is as small as the size of DNA [3], the nanometer structure devices have high potential to be used in biologic systems, so called lab on a chip (LOC) [4].

1.2 Organization of the Thesis

In this thesis, all the theories and previous works related to fabrication methods used in this thesis will be reviewed in Chapter 1. We will introduce the scanning probe lithography (SPL) method and orientation dependent etching methods in 1.3. They are the main fabrication techniques we used in our experiments. Theories and properties of nanometer scale devices will be mentioned in section 1.4. Experiment's details and results will be introduced in Chapter 2. Applications of nanoscale device will be discussed in Chapter 3. A short conclusion and future works are addressed in Chapter 4. All references and figures associated are given in full at the end of each chapter.

1.3 Scanning Probe Lithography

1.3.1 Lithography Methods in the Recent Era

According to Rayleigh criterion, the resolution (R) in optical lithography system is

$$R = k1 * \lambda / NA \qquad (1.1)$$

Where k1 is a process dependent factor, range between 0~1 at the atmosphere environment, λ is the wavelength of the light source, and NA is numerical aperture.

Several methods are used to improve k1 in the optical lithography system, including optical proximity correction (OPC) [5], phase shift mask, photo resist engineering, and adding anti-reflective layer (ARC) [6]. The most interesting invention in the recent is the immersion lithography [7], which uses the diffraction index difference between atmosphere and liquid to improve the NA. As a result, the resolution of the lithography system has obvious progress. The key point to push the optical lithography scale down to sub-micron region is using the light with shorter wavelength as the exposure source. Such as DUV light, x-ray, e-beam, and ion beam are widely surveyed as the candidates of light source in the next generation optical lithography system. But each of them still has some problems need to be solved [8,9].

Some methods different to optical lithography have also been proposed, like nano-imprinting [10,11], and scanning probe lithography [12]. They provide researchers another way to fabricate nanometer devices.

Some properties about different lithography methods are given in short in Table 1.1.

1.3.2 Atomic Force Microscopic

HISTORY

In 1982, Binnig et al. invented the scanning tunneling microscope (STM) and demonstrated that STM could explore the three-dimensional topography of surfaces on atomic scale in air [13]. With this invention, Binning, Rohrer and Ruska won the Nobel Prize of physics in 1986.

In 1986, Binnig et al. introduced another apparatus for surface characterization in atomic scale, the atomic force microscope (AFM) [14]. Since it can be applied to any types of material and environment, AFM has thus been used widely in surface characterization.

At present, atomic force microscope and scanning tunneling microscopy (AFM/STM) based nano-oxidation of H-passivated Si [15], elemental metal [16], and refractory metal nitride films [17] has been reported. Furthermore, several prototypes of micro devices have been demonstrated [18]. Owing to its atomic scale resolution capability, AFM is a powerful tool for nano-structure fabrication.

SYSTEM CONSTRUCTION

There are two major modules to compose an AFM system:

1. Cantilevers and tips module [19]

   It plays the important role as the interface between sample surface and the whole system. It also determines the ultimate lateral resolution of the system.

2. Piezoelectric scanner, position sensing and feedback module [20]

   This module is used to precise locate the tip to the place where we are interest in. Most AFMs use optical principle to form the feedback system.

Figure 1.1 shows the system of AFM.

OPERATION MODE

The AFM can be operated in three regimes: contact mode, non-contact mode and intermittent contact (tapping) mode. Each mode can be associated with a specific region in the force-distance curve, see Figure 2 [21].

1. Contact mode (CM)

At this mode, the tip is close to the surface. The force (F) between the tip and sample surface is repulsive, which typically in the range 10^{-6} N < F < 10^{-9} N. The applied DC force regulates the tip to sample distance.

2. Non-contact mode (NCM)

This mode is performed when the distance of the tip and sample surface is about 10 to 100 nm. The force is attractive (typically 10^{-9} N < F < 10^{-12} N). Far away from the sample, the cantilever is exited at a frequency ω_0 slightly above the cantilever's resonance frequency ω_r (typically from 50 kHz to 400 kHz). When the tip is brought closer to the sample, the resonance frequency will decrease according to

$$\omega_r = [\omega^2_0 - (1/m)(\partial F/\partial z)]^{1/2} \qquad (1.2)$$

This induces a decrease of the amplitude (typically < 10 nm) of the vibration. The amplitude is then used as a feedback signal to control the tip to sample distance.

3. Intermittent contact mode

This mode relies on the same principles as the NCM imaging, but the cantilever is now driven at a frequency below the resonance frequency ω_r. The amplitude (typically ranging from 20 nm to 100 nm) of the vibration will increase when bringing the tip closer to the sample, up to the point when during part of the cycle the tip touches the sample. This induces a decrease of the vibration amplitude, which is used to control the tip to sample distance.

NANO-OXIDATION

Like any electrochemical anodization, when there is a potential difference between sample surface and the tip, ions move towards the anode and react with it [17,22]. Typically, a positive bias voltage is applied to sample surface respect to the tip during oxidation. The electric field created between the tip and the sample directs the oxidation species (OH^-) towards the sample surface. For silicon substrate, when the applied electric field is above 10^6 V/cm, the intensity to product native oxide, the species react with silicon to form oxide locally (Figure 1.3). The oxide is treated as the hard mask (Figure 1.4) in the traditional optical lithography process.

The main parameters to control the oxidation quality (oxide quality and width) in SPL method are humidity, scanning speed, bias voltage [2], distance between tip and sample surface, and the sharp of the tip. The conductivity of the tip itself is also an issue should be emphasized [19].

1.4 Orientation Dependent Etching

Orientation dependent etching (ODE) is one of the anisotropic wet etching methods. The different etching rate may be due to the resistivity-dependant selectivity [23], doping type different and so on. ODE in single crystal silicon can always make (111) facet. The slow etch rate in <111> directions is a consequence of the diamond lattice. A (111) plane is a double layer bound together by more atomic bounds than are found between other planes, as illustrated is Figure 1.5 [24].

Because the high selective etching in different planes, (i.e. for TMAH the etching rate between (111) and (100) is about 50) high aspect ratio pattern can be easily formed by ODE method [25].

Compared to the other widely used wet etching etchant KOH, although TMAH has lower etching rate but take advantage of higher etching selectivity to oxide [26], (oxide to Si (100) etching ratio is above 3000) and less mobile ion (K^+) pollution. The later issue is very important in VLSI device processing. Figure 1.6 show the idea of anisotropic etching pattern on silicon wafer with different surface orientations.

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Table 1.1 COMPARISONS BETWEEN DIFFERENT LITHOGRAPHY METHODS

Parameters	EUV	X-Ray	E-beam	Ion-Beam	AFM
Light Source	In Development	In Development	Mature	Mature	None
Mask Fabrication	Mature	Very Difficult	Mature	Mature	None
Lens Fabrication	Need to be Solved	None	Mature	Mature	None
DOF	Good	Very Good	Very Good	Very Good	N/A
Resolution	High	High	High	High	High
Cost	High	High	High	High	Medium
Throughput	High	High	High	Low	Low*

Reference: H. Xiao, “Introduction to Semiconductor Manufacturing Technology”, Prentice Hall (2001).

* IBM use tips array to overcome this problem [50].

Table 1.2 COMPARISONS BETWEEN THE CHARACTERISTICS OF OPTICAL MICROSCOPY, SCANNING ELECTRON MICROSCOPIC AND SCANNING TUNNELING MICROSCOPE.

Parameters	Optical Microscopy	Scanning Electron Microscopy	Scanning Probe Microscopy
Sample Operation Environment	Ambient air, liquid or vacuum	Vacuum	Ambient air, liquid or vacuum
Depth of Focus	Medium	Large	Medium
Resolution: X, Y	~ 100 nm	~ 5 nm	~2nm for AFM 0.1 nm for STM
Resolution: Z	N/A	N/A	0.1 nm for AFM 0.01 nm for STM
Sample Preparation Requirement	Little	Little to substantial	Little or none
Characteristics Required of Sample	Sample must not be completely transparent to light wavelength used	Surface must not build up charge and must be vacuum compatible	Sample must not have local variations in surface height > 10 um

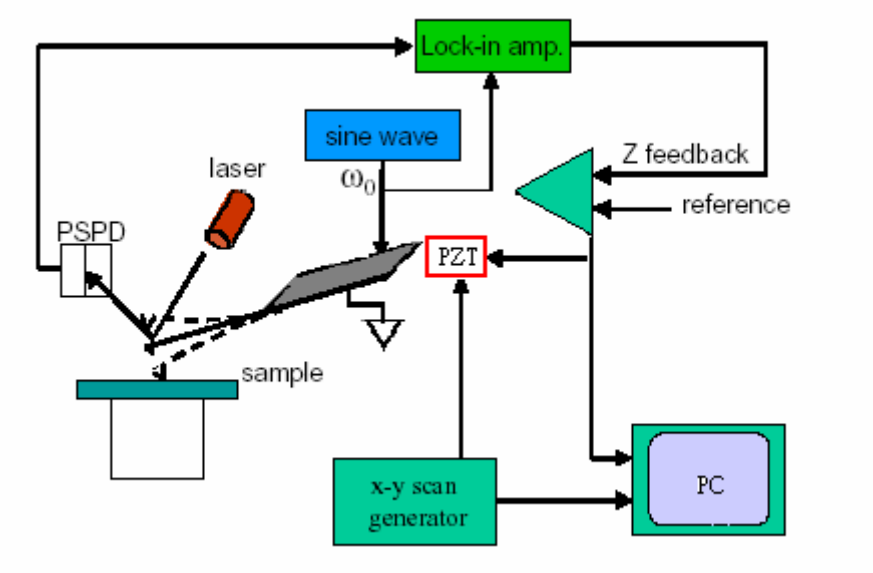


Figure 1.1 Main components to set up atomic force microscopic

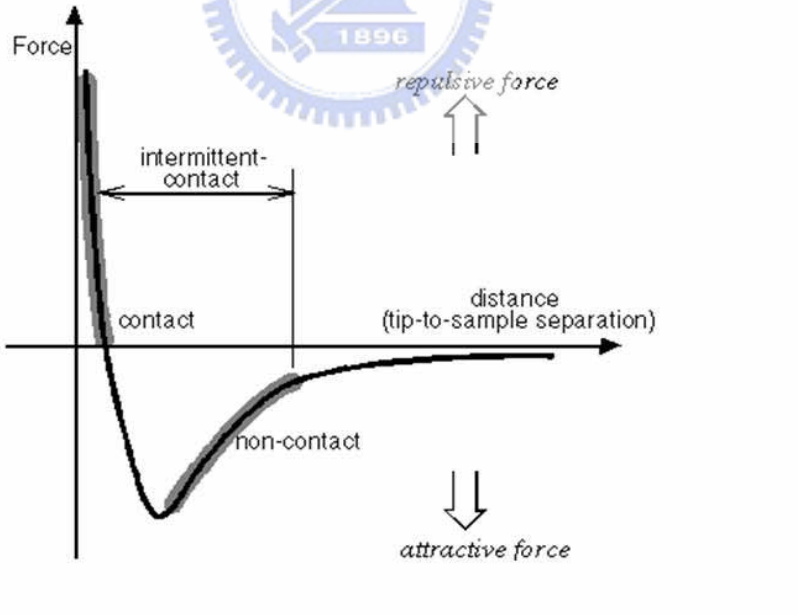


Figure 1.2 Vander Waals force versus distance graph illustrating various types of forces being accessed by the tip at the sample surface.

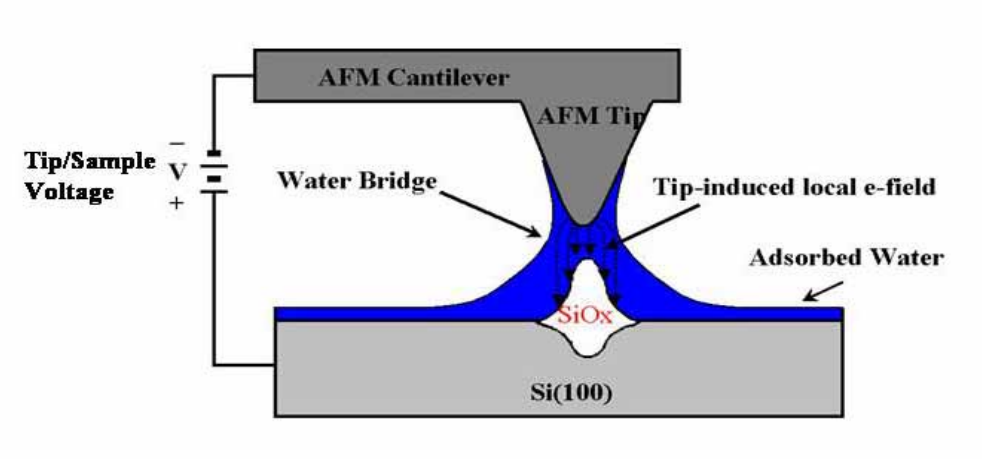


Figure 1.3 Schema of AFM local oxidation process.

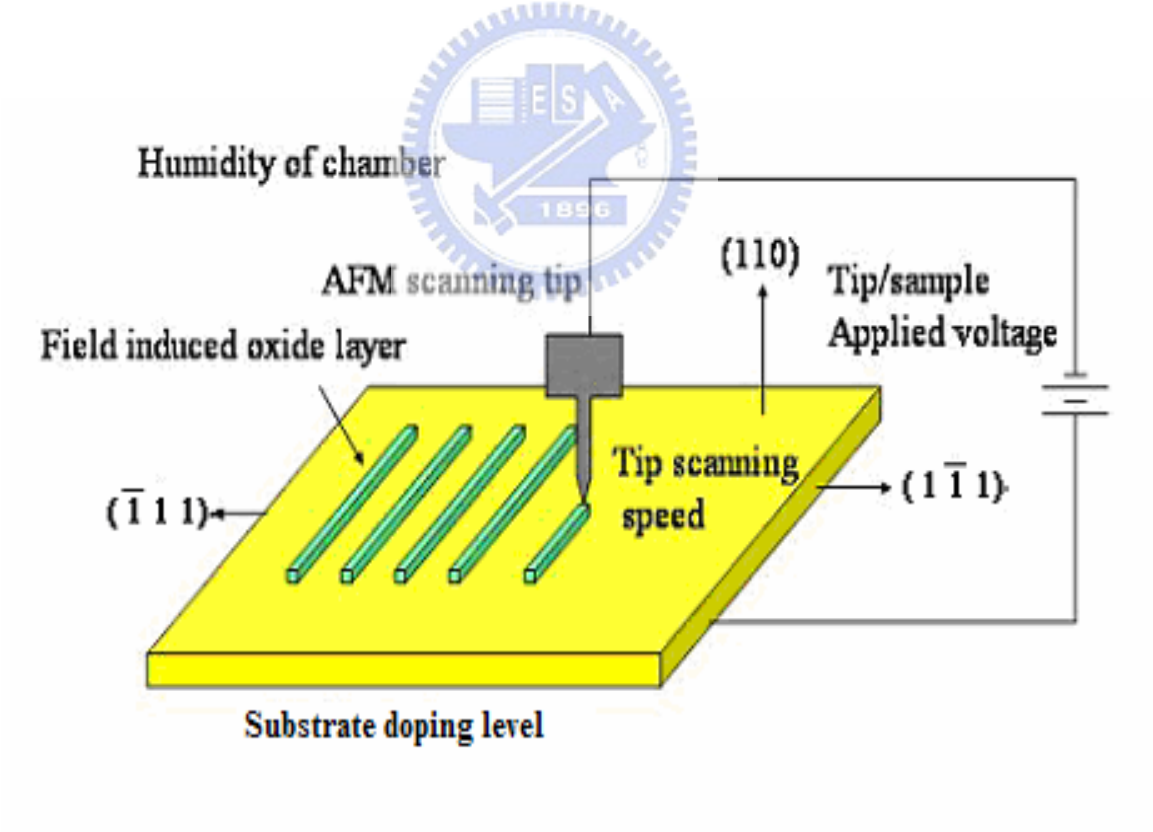
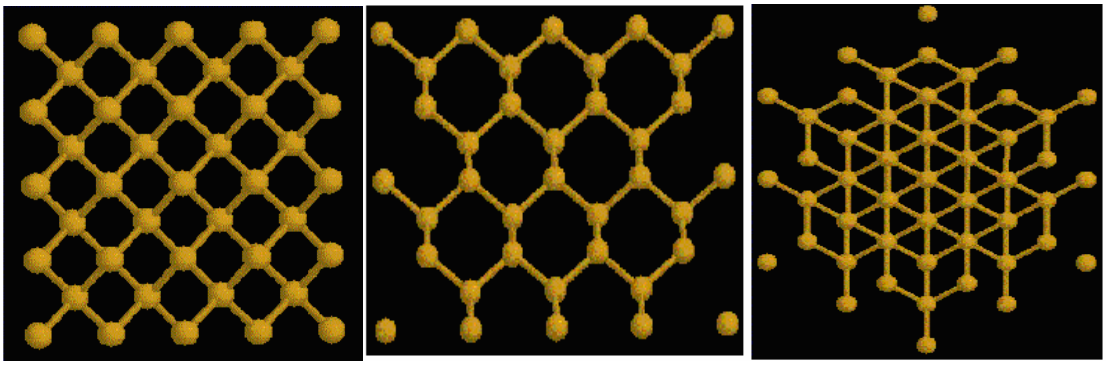
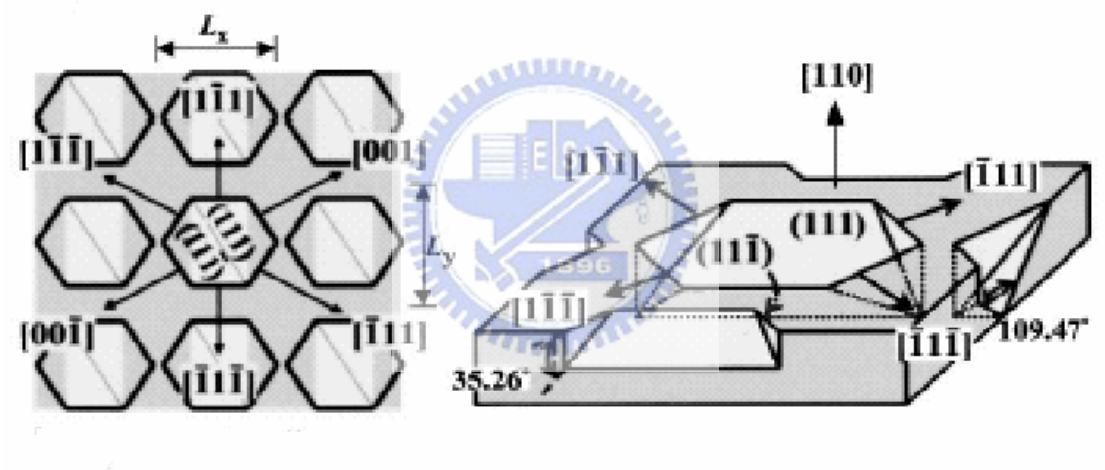


Figure 1.4 Oxide produced by SPL is used as etching mask.

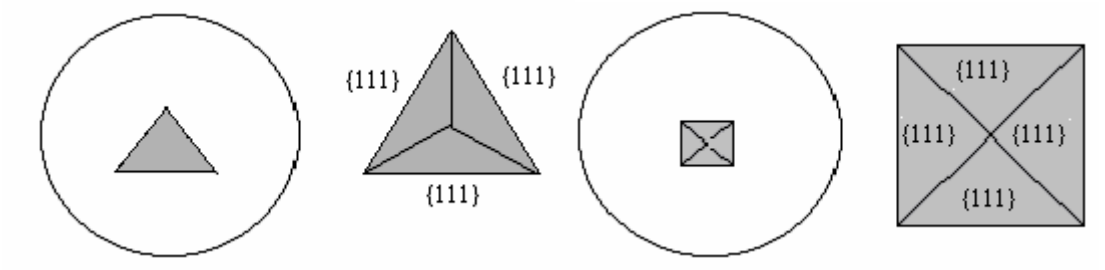


(a) (100) surface (b) (110) surface (c) (111) surface

Figure 1.5 Atoms arrangement in diamond structure seen by different directions.



(a) Pits formation after anisotropic etching on (110) surface.



(b) Pits on (100) Wafer, (c) pits on (111) Wafer

Figure 1.6 Anisotropic etching on wafer with different surface orientations, (a) (110) surface, (b) (100) surface, (c) (111) surface.

Chapter 2

Device Fabrication

We use scanning probe lithography and orientation dependent etching methods to fabricate many different nanostructures. There are some other methods to fabricate silicon based nanometer scale devices like nano-imprinting (Figure 2.1 [1]), e-beam lithography plus RIE (Figure .2.2 [2]), two-angle evaporation (Figure 2.3), vertical pattern-dependent method (Figure 2.4 [3]), and break junction (Figure 2.5 [5]). The most benefit of our procedure is its relative low cost, high controllability and flexibility to researchers. A brief comparison is summarized in Table 2.1.

General Fabrication Process

2.1 Wafer preparation

All experiments were performed with intrinsic (110)-oriented Uni-bond SOI wafer, where the initial silicon on insulator is 72.1 nm $\pm$ 2.3 nm, and the box oxide is 2326 nm $\pm$ 1.9 nm. Samples are prepared with following processes.

2.2 Define Active Area Regions

2.2.1 Standard RCA Clean and Dry Oxidation

Oxide layer is used as an ion implantation mask layer. During the dry oxidation process, we also thin the top silicon layer to our designed thickness.

2.2.2 Ion Implantation

2.2.3 Define AA region with Mask 1.

2.3 Define Desired Nanostructures

We use AFM to induce local anodic oxidation as hard mask, and orientation dependent wet etching with TMAH to etch top silicon layer in AA region.

2.4 Passivation (Optional)

According to different usage, we can choose different kind of passivation methods. (Grow thermal oxide, deposit silicon nitride or do nothing). Through this thesis, right now, we only use thermal oxide as a passivation layer.

2.5 Contact Formation

2.5.1: Define Contact Plug with Mask 2 (without P/R remove)

Since passivation is not necessary in the experiment, we didn't remove photo resist immediately after contact plug formation to avoid Al diffuse into silicon. Photo resist is removed after step 2.5.4.

2.5.3: Coating Aluminum with Thermal Coater

2.5.4: Define Contact Pad with Mask 3

2.5.5 Al sintering

The full schema of process flow is given in Figure 2.6. The AFM pictures of our devices are displayed in Figure 2.7 to Figure 2.11, SEM images are given in Figure 2.12.

Figure 2.7 shows single electron transistor structures, associated properties are given in section 3.2. Figure 2.8 shows the schema of bio detector device, details will be described in section 3.3. Structure in Figure 2.9 is designed to see how the influence of the corner in the nano-scale devices. We want to tell if the back scattering is a dominant factor in such device (particle behavior) or the current is a dependent issue to the field we applied in drain

(wave like). Figure 2.10 shows the idea about quantum influence [6] device. Due to the wave property of the electron, we wish to discover the influence behavior by measuring source-drain current with sweeping control gate voltage. Figure 2.11 displays the prototype of point contact device, some properties of point contact device can be find in reference [7] and [8]. SEM images in Figure 2.12 confines our ability in both device structure and dimension control.

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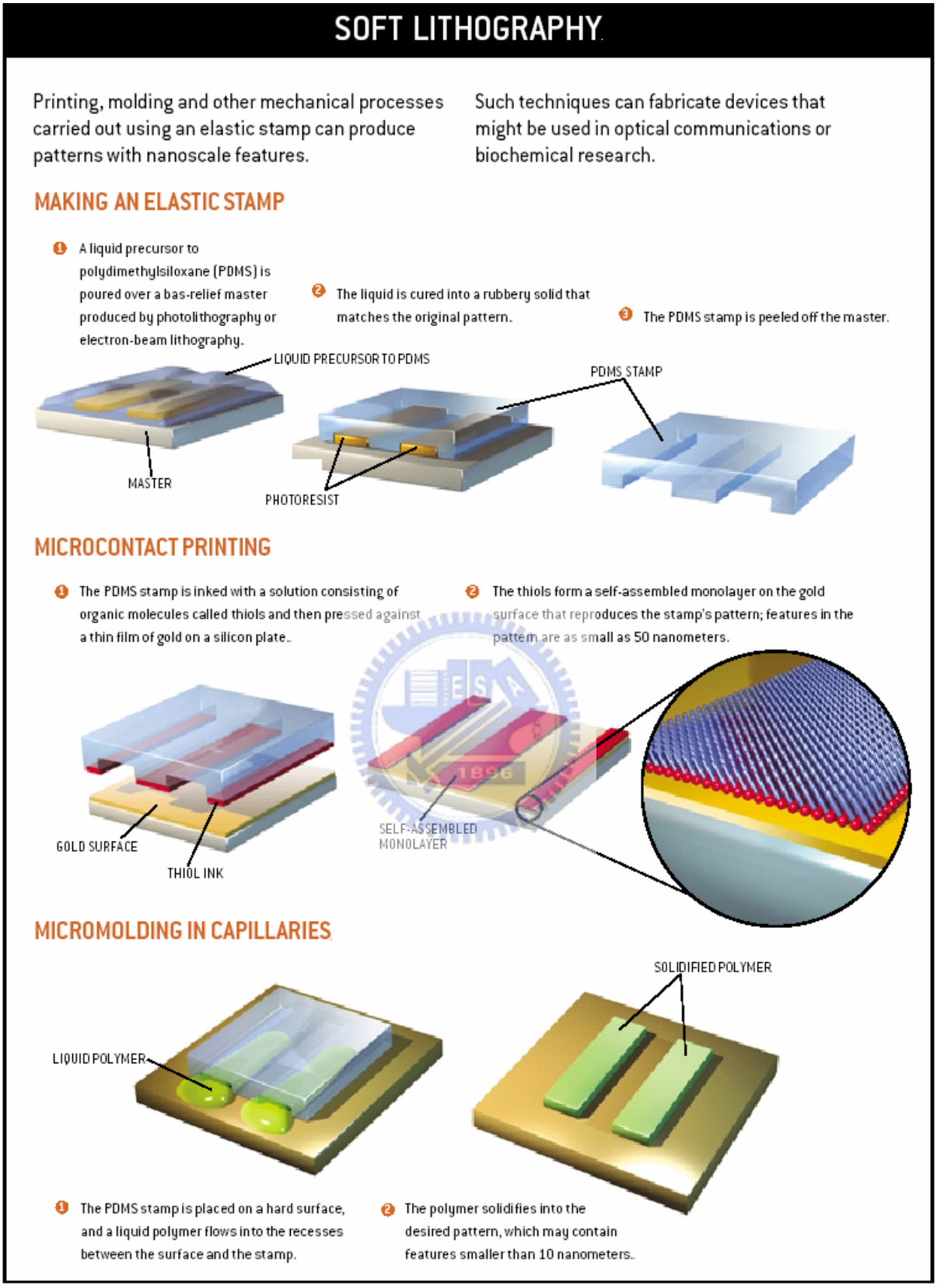


Figure 2.1 Schema of nano-imprinting method

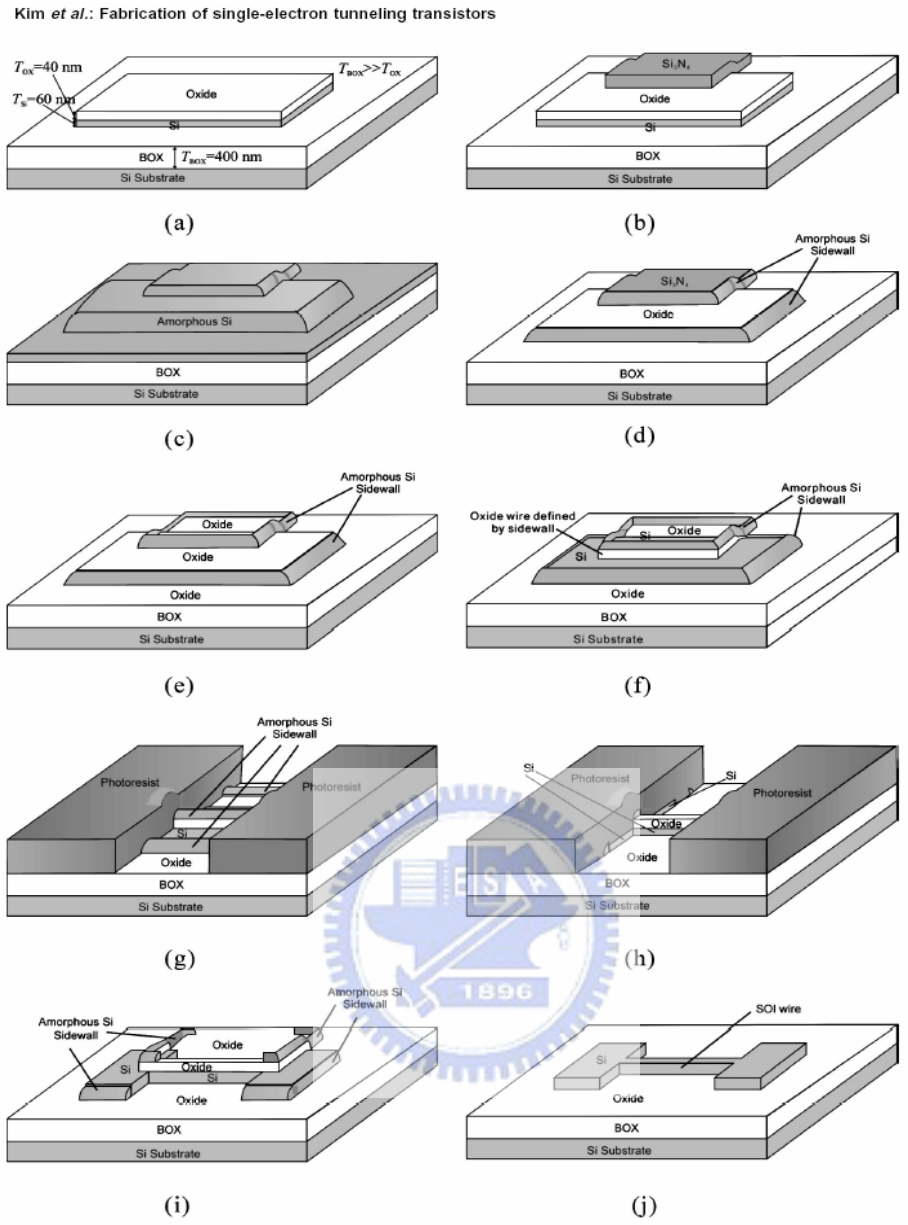


Figure 2.2 E-beam lithography plus reactive ion etching

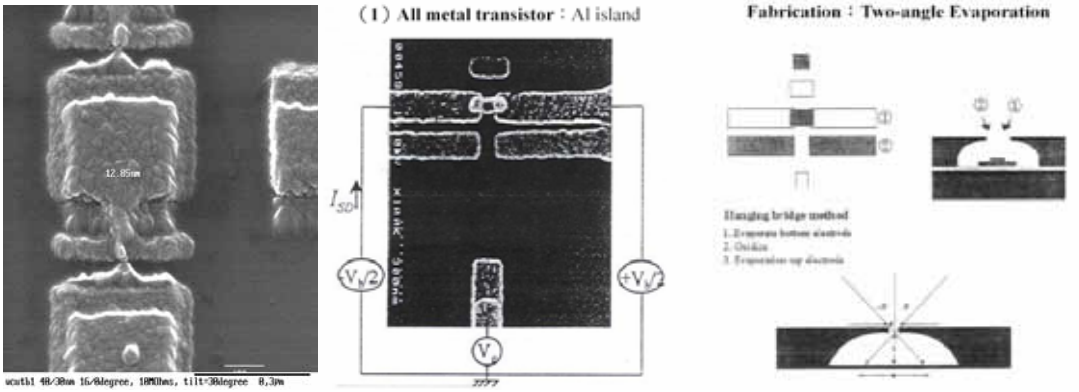


Figure 2.3 Schema of two-angle evaporation method

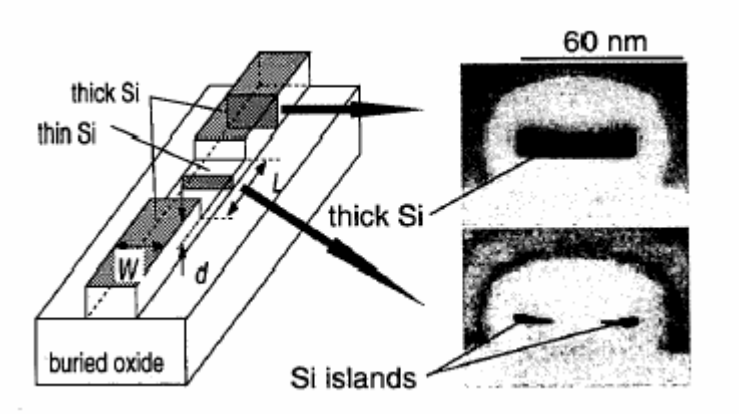


Figure 2.4 Schema of vertical pattern-dependent oxidation (V-PADOX) method

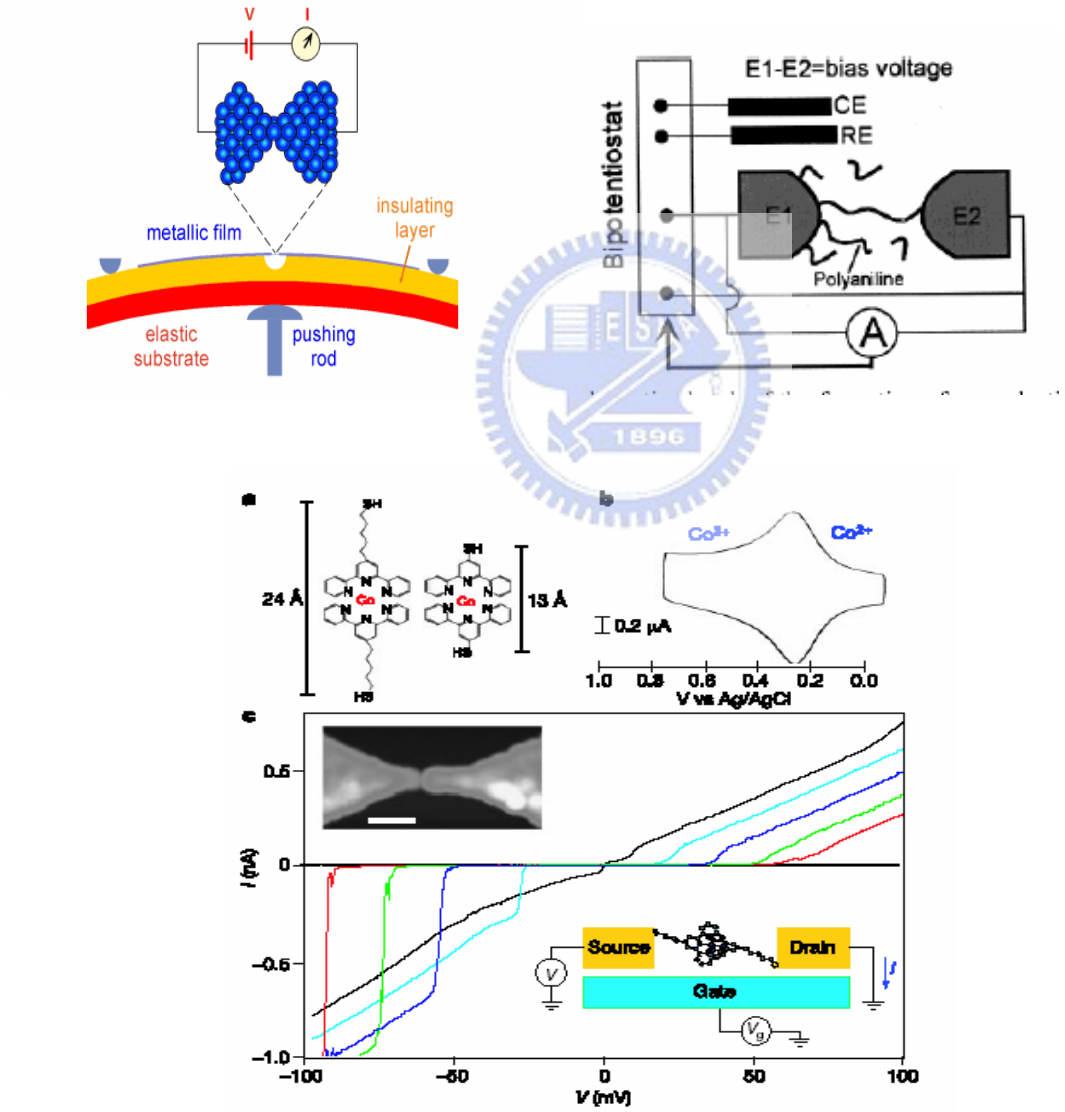


Figure 2.5 Schema of break junction method

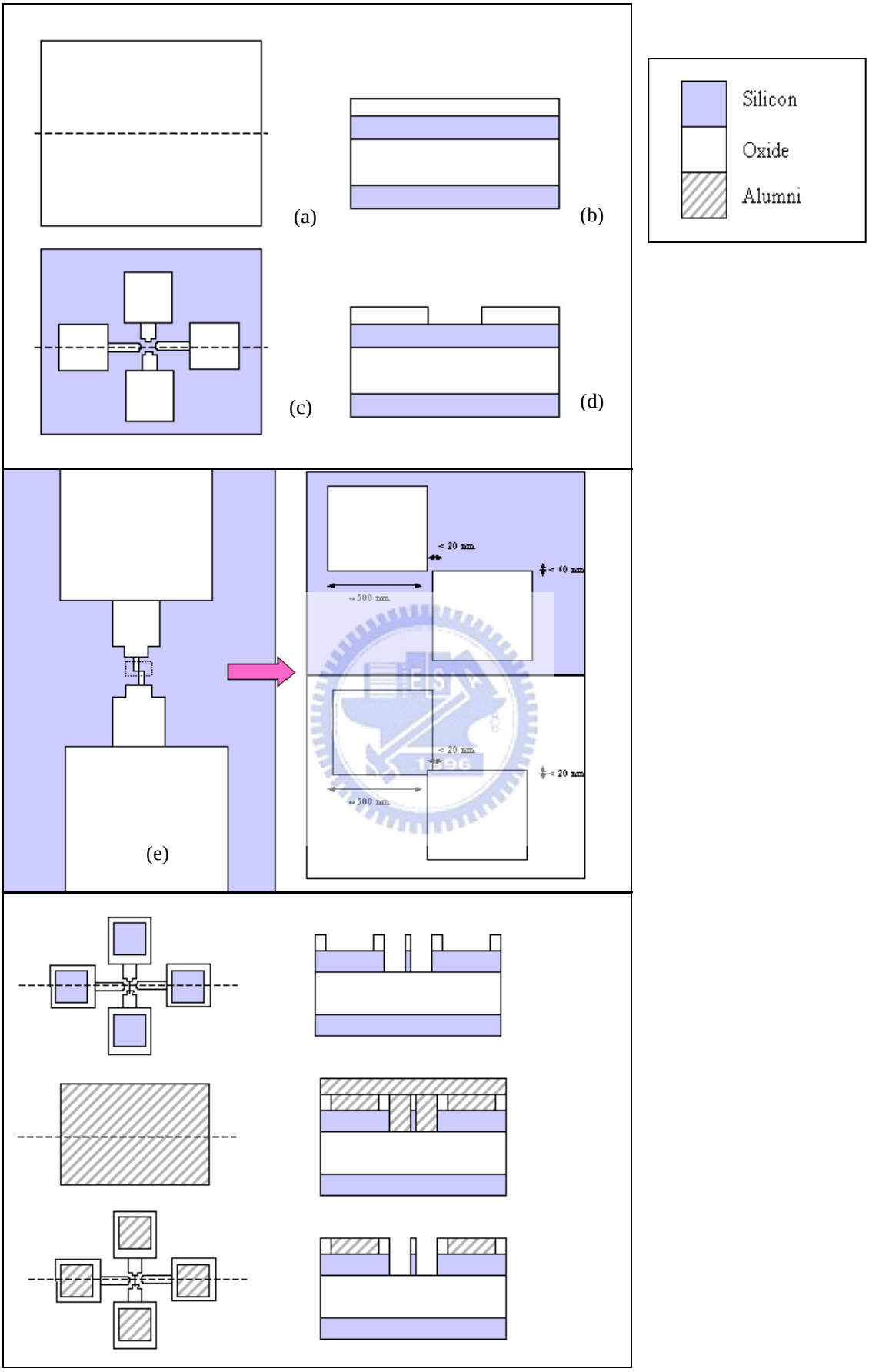
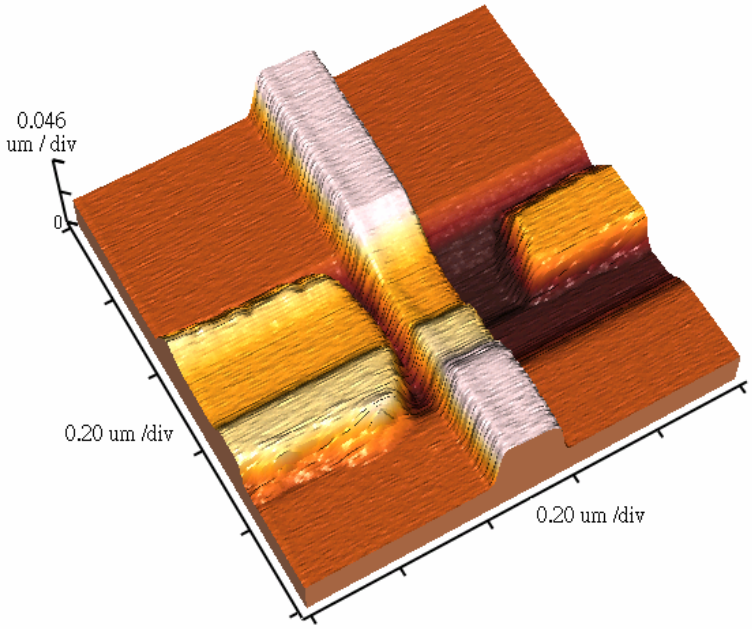
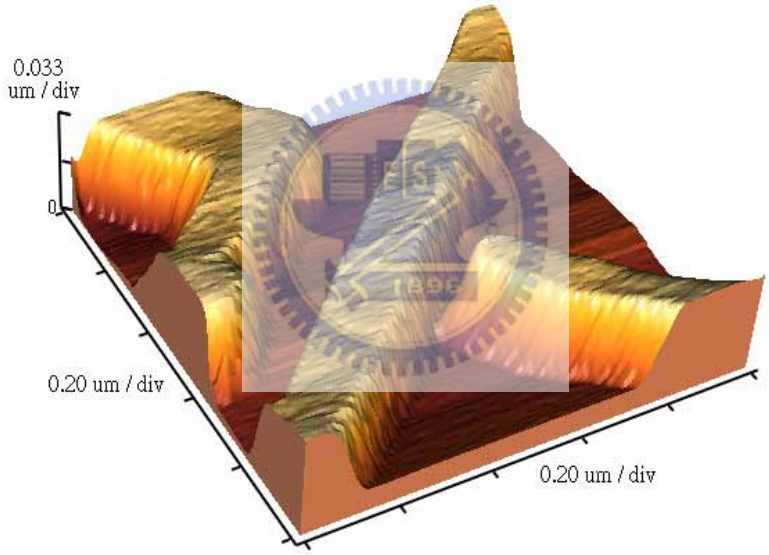


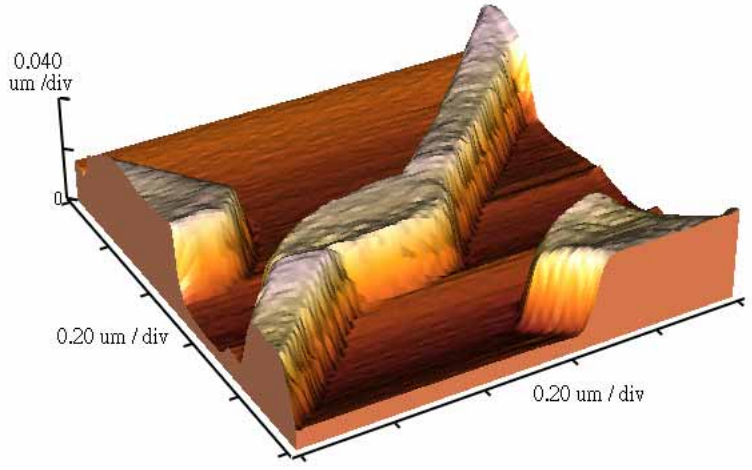
Figure 2.6 Process Flow



(a)

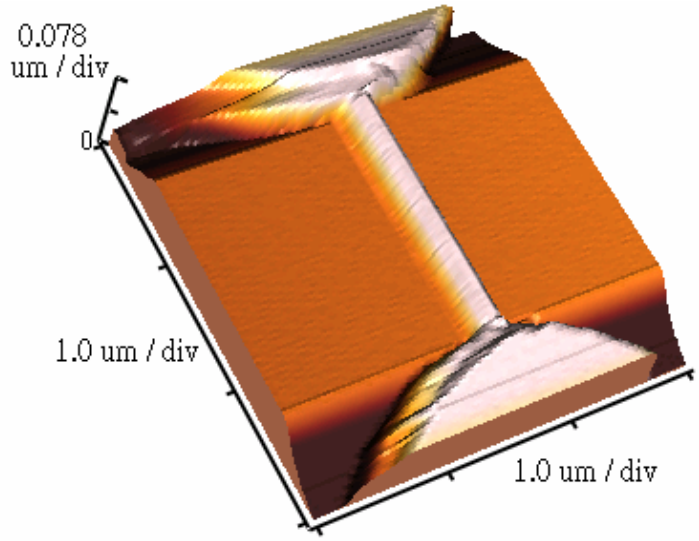


(b)

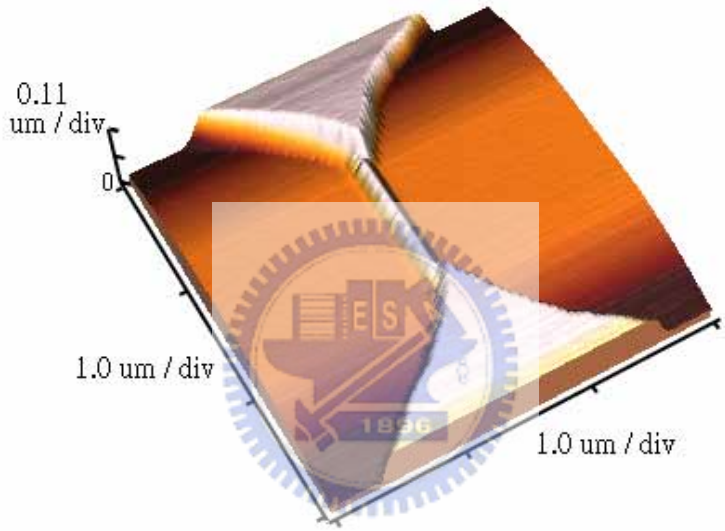


(c)

Figure 2.7 AFM image of SET device



(a)



(b)

Figure 2.8 AFM image of bio detector device

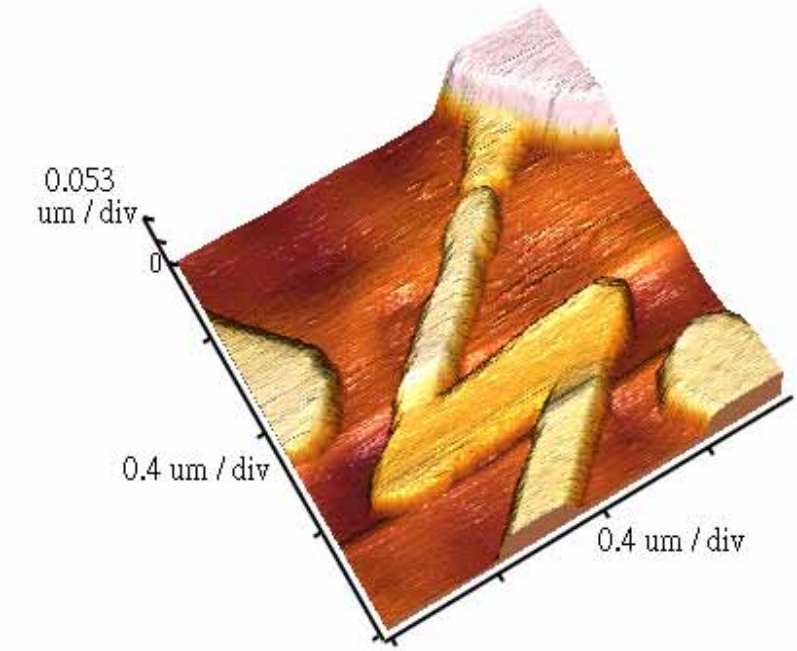


Figure 2.9 AFM image of scattering influence device

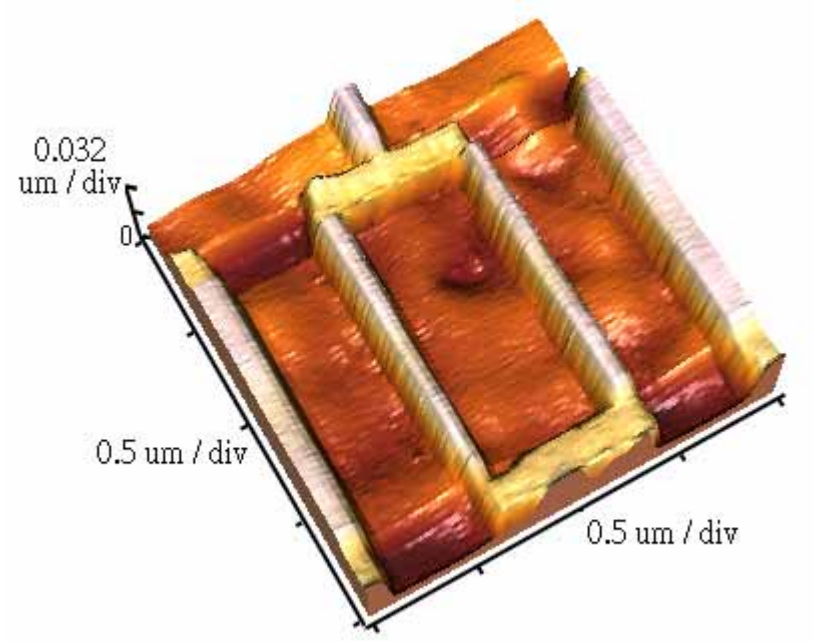


Figure 2.10 AFM image of quantum influence device

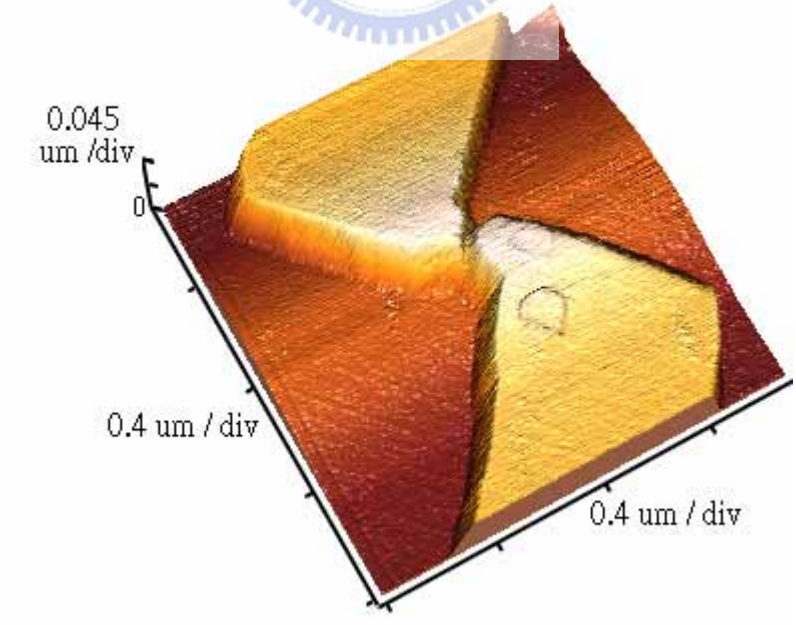


Figure 2.11 AFM image of point contact device

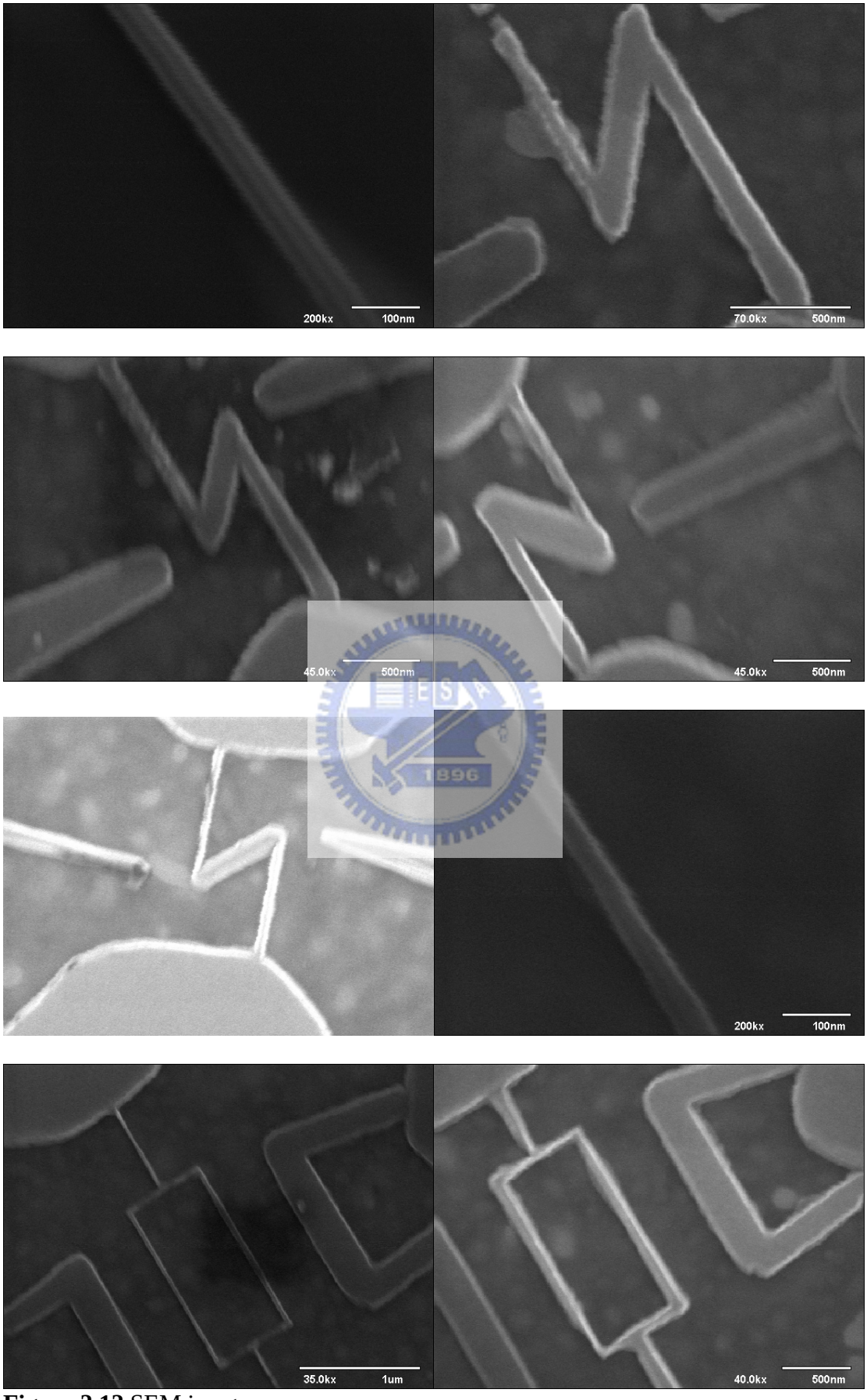


Figure 2.12 SEM images

Chapter 3

Experiment 2 – Device Characteristics

3.1 Mesoscopic Phenomena

When devices scale down to the size comparable with the electron's Fermi wavelength of its composed material (i.e. The Fermi wavelength in metal is at the scale about 1 nm, but in semiconductors is about 10 to 100 nm), we called such a system a mesoscopic system. Such system is at a transparency state between macroscopic (bulk material property) and microscopic (atomic level consideration) system. The number of atoms in the system is not large enough for us to apply the statistics to describe it precisely, but is still too huge for us analyzed it with quantum mechanism from bottom up. Weak localization [1] and universal conductance fluctuation [2] are two major characteristics when we describe such a system. The variety and uncertainty in the mesoscopic system make it an interesting topic for researchers to devote to.

3.2 Single Electron Devices

As described in the section 1.1, nanometer scale devices are interested to numerous researchers in various fields; so many different kinds of device are fabricated with dissimilar operation principles. Depends on the dimensions of the device (0D, 1D, 2D or 3D), the density of state of the device has dramatically changed [3]. Here we only focus on the devices structures that have a small island between two tunneling barriers. The extent of the electrons in the island defines three basic categories of solid-state nanoelectronic devices [4].

- Quantum Dots (QD's or "artificial atoms") [5].

Island confines electrons with zero classical degrees of freedom remaining.

- Resonant Tunneling Devices (RTD's) [6].

  Island confines electrons with one or two classical degrees of freedom.

- Single-Electron Transistors (SET's) [7].

  Island confines electrons with three classical degrees of freedom

Figure 3.1 [8] shows the basic idea of device structure. Figures of band diagram and theoretical Is-Vd curve for devices just discussed above are given in Fig 3.2. SET's characteristic current-voltage curves are displayed in Figure 3.3 [9], and Figure 3.4. Here, we showed many pioneer's great works in Fig. 3.5 to Fig 3.9 [10,11,12].

3.2.1 Depletion Gate Single Electron Device

Our efforts are mainly on the single electron device. We start to analyze our device with the theory of single electron transistor. The basic ideas of SET are quantum confinement in the island between two tunnel barriers. When the charging energy in the system is larger than quantum uncertainty, coulomb blockade phenomena will be discovered. Detailed theories about SET can read reference [7,9,13,14].

Based on the process we developed in Chapter 2, we fabricated a device operated like SET. We use the depletion gate concept [15] to make a five terminal (bottom gate, side gate, control gate, source, and drain) device (Device diameters are given in Table 3.1). With the interaction among Vbg (bottom gate), Vsg (side gate), and Vg (control gate), we created an island and two tunneling barriers. Device's structure is present on Figure 3.10, AFM images are given in 2.7, and measured IV curves are showed from Figure 3.11 to Figure 3.22. Some quantities about quantum effects are given in Table 3.2.

Although the categories of single island device descried above are specified clearly, till now, devices can't be fabricated just meet one of the objects. We can see that device's

characteristics are transient among three basic categories.

First, we see Figure 3.11, and Figure 3.12. The device D5 works properly with the theoretical SET's characteristic Id-Vd and Id-Vg curves. And in Figure 3.13, and Figure 3.14, the device C5 presents resonance tunnel devices' (RTD) current-voltage relationship. This may due to the electron's Fermi wavelength in silicon become longer with lowering temperature (Compare with the same device C5 measured at different temperature). Longer wavelength changed the island dimension seen by electron, for example, from three dimensions to two or one dimension. The Id-Vd's behavior may be explained by quantum well module. The maximum likelihood to describe electron's behavior is standing wave like. The quantized energy levels correspond to the peak transition current. Gate voltage gives the different potential energy in the island, so we see the similar behavior of periodic oscillation current and voltage relationship.

Second, refer to Figure 3.15, and Figure 3.16, both Id-Vd and Id-Vg curves showed staircase. The origin of formation staircase Id-Vd curve is due to the asymmetry resistance of two tunneling barriers. The reason of Id-Vd showed staircase is that control gate Vg not only influent the electron potential in the island but also the number of electrons. Unlike the current is limited by electron tunneling rate of tunneling junction between island and source (Jis), with higher temperature, the tunneling junction has higher tunneling rate (the tunneling rate relates to temperature with the fact exp(-1/kT)). The current now is not limited by tunneling rate of junction Jis but the number of electrons in the island. As the result, we can observed the quantization Id-Vg behavior, each step imply one more electron participated. Based on the Id-Vg curve measured in this experiment, we can calculate the average electron mobility of our system. We find our devices have the mobility around 20500 cm^2/V-s at 30 K and 11500 cm^2/V-s at 60 K. Our device is phosphorous doped ($5*10^{15}$ cm^{-3}). This result falls in a reasonable range (see Figure 3.23 [16]).

Third, Figure 3.17 to Figure 3.21 showed us another Id-Vg pictures. We suppose that there exist a leakage path from drain to source. This assumption is reasonable, since with increasing control gate voltage, the accumulation region become more and more wider. Above certain voltage, the accumulation region is wider than depletion region caused by side gate and the tunneling barriers disappeared near control gate (see Figure 3.24). It means that, there exist another path (MOSFET like) for current flow between source and drain. When the effective resistance seen by electron is higher than 25.6 MΩ, the electron confinement phenomenon is still can be observed. As a result, our device at this category performed like a SET parallel with a MOSFET. The periodic oscillation is SET's characteristics and the increasing current is due to the conducting of parallel MOSFET.

3.2.2 Discussions of Depletion Gate Single Electron Device

After qualitative discusses our device in previous section, we try to describe it in more quantitative way. We start at compare parameters extracting from theoretic calculated (first order approximation) by device dimensions and measured IV curves. We find Cg is at a deviation of 50% (2.42 aF v.s. 5 aF), which is still at an acceptable range, but there exist obvious difference in Cd (5.9 aF v.s. 35.6 aF), more detailed data are given in Table 3.4. In addition, the parameter we extract from measurement shows that we measured the device at a condition out of the device's operation widow. This is unreasonable. This factor implies using the theory for SET to describe our device is not suitable. The oscillation caused in sweep Vd should not be contributed to single electron charging effect but quantized states in the quantum dot. We use the particle in a box model to estimate the dot dimension, and we find the island is at the size about 20 nm. This result agrees to our control gate dimension (60 nm). Father more, we can see the size of the island is about the half electron's de Broglie wavelength in the low temperature (refer to Table 3.2), this convinced

that the characteristics we measured are something meaningful. By including the information about the QD size, we re-calculate the Cd and combine measured Cg to get the charging energy and operation window for our device. It shows a self-consistent result. All discussions in previous section are still the same except that the charging energy needs to be replaced by quantized energy level. We try to find the staircase in our device C5 caused by charging energy in the Id-Vd curve but in vain (can refer to Figure 3.25). This may due to there doesn't exist significant difference in the depletion junction Jis and Jid. Some associated data can be found in Table 3.5.

3.3 Measurement Issues of Single Electron Device

3.3.1 Material Preparation

As we can see in Section 3.2, drain current of single electron device is relative small to traditional MOS device. The current level is at the range at the pico to micron ampere. For device isolation requirement, silicon on insulator substrate is desired. From reference [17], we know the resistivity of thermal oxide is at the range of 10^{12}-10^{16} Ω-cm (applied field depedent), contact pad dimension of our device is 100 um * 100 um. The allowed leakage current level is about 1 pA at Vd = 2 V. That is, at the worst case, the required buried oxide thickness of the SOI wafer is 2000 nm. At the beginning of our experiment, we use Uni-bond SOI wafer and get some results. But when the wafer is spent, we change to use the SIMOX SOI wafer, and find the leakage current is too huge to achieve single electron device. As a result, most of our proposed structures presented in Chapter 2, cannot be analyzed in this theses. Material preparation is very important.

3.3.2 Ohmic Contact

We cannot observe Coulomb blockade behavior near Vd ~ 0V (Figure 3.3), because our device use aluminum as contact metal, it forms schottky barrier with silicon. If we change the contact metal from Al to Pt or W, the schottky contact can be improved. At the moment, we can observe Coulomb blockade behavior near Vd ~ 0V, electron transport in negative drain bias, hole transport in positive drain bias. It will provide more data to analysis carrier transport phenomena. But as mentioned in 3.3.1, our efforts are all in vain due to the SIMOX SOI leakage.

3.3.3 Sweeping Method

When we sweep drain voltage, we should sweep from zero voltage to positive voltage and from zero voltage to negative voltage (two steps) instead sweep Vd from negative voltage to positive voltage (one step) or vice versa. Because measurement system itself also has resistors, capacitors components will cause RC time delay during measurement. When sweeping drain voltage from positive to negative voltage (or vice versa), we can observe that at Vd = 0 V, the drain current is not close to the zero level of the system (For example, in HP 4155 system, the zero level is about several fA), but some orders larger (see Figure 3.26). The current may at the range of several pA to uA, depends on device structure. This is not a series issue to traditional MOS structure, but when referring to single electron device, it really is a big problem. It makes a false signal at the zero drain bias condition, but this condition is a key point to observe coulomb blockade behavior. Also, when sweeping drain voltage, SOI substrate should be set a value (i.e. zero) to avoid undeserved charging effect at the BOX surfaces (between SOI layer or substrate). The charging and de-charging effect will affect measurement results (so called floating body effect, see ref. 18 and compare Figure 3.26 and Figure 3.27). On the other hand this imperfect phenomenon should be take into consideration when we sweep bottom gate voltage (body voltage, see

Figure 3.28). Same measurement principle should be obeyed in order to obtain more exact device characteristics.

Time setting is also an issue in the measurement. As discussed above, charging and de-charging effect in SOI has significant influence to the device, we should delay the time interval between two measurements to obtain effective results. Also, in order to obtain meaningful results, voltage step in sweep mode should as small as possible, and long integral time is required to eliminate noise in the system.

3.4 Design Issues of Single Electron Device

3.4.1 Room Temperature Operation

Many researchers want to solve this issue by making structure small (i.e. smaller tunneling junction region make smaller capacitance). This is theoretically right, but there still have the other restriction. If we want to see single electron transport phenomenon, we must let the device driving in tunneling limited but drift limited. But refer to Figure 3.23, we see electron mobility at room temperature is quit lower compared to which in the low temperature. It means the current we want to measure is quite small ~ about 0.5 pA, which is really a big challenge. We can refer to our device C5's performance above 50 K, the Id-Vd curve have smell out and hard to observe SET's characteristic Id-Vd curve.

Quantitative speaking, $\Delta Vd = e / Cd$, we wish ΔVd is as larger as possible for circuit design. And $Cd \propto$ (junction and dot contact area) / (junction length). It means that we should product a junction with small junction and dot contact area and longer junction length. Prior requirement is fabrication limited, and later one is physically limited (Tunneling probability is inversely proportional to junction length). Afterwards, if we really

produce such device, the current we can measured will be very small because electron tunneling rate is positive proportional to Cd. We cannot obtain both large ΔVd and ΔId at the same time.

3.4.2 Random Background Charge Problem [7]

If an impurity is trapped in the insulation environment, the impurity will polarize the island, creating a polarization charge of the order a/r, where 'r' is the distance from the impurity to the island, and 'a' is the diameter of the island. This charge affects all the characteristics of the single electron transistor.

3.4.3 Universal Conductance Fluctuation at Low Temperature

Considering the island with the scale about 10 nm*10 nm*10 nm (10^{-16} cm3), and the doping density of the device is 10^{17} cm^{-3}. We can calculate that the number of dopants (N) in the island is about 10, and the fluctuation of the device is about $N^{-1/2}$. Which means the device-to-device variation can be as large as 50 percent. And the positions of the dopants give the different current voltage characteristics due to the universal conductance variation. This phenomenon can also be observed at low temperature. Since at low temperature (freeze out region), the material tend to have the same property as intrinsic ionization rather than doping dependence. But generation-recombination process is occurred all the time. Thermal statistics tells us the average behavior but the exact situation at certain place and moment. On the other hand, when our device is measured at low temperature, we cannot tell the precise situation about the island properly. Each time the island formed by our manipulating control gate and side gate, it has different inner condition (i.e. the number of electrons in the island is unknown and in variation). Figure 3.12 and Figure 3.22 can assert this assumption. The characteristic I-V curve has the same properties (oscillation and increasing), but the exact relationships are different.

3.4.4 Universal Conductance Fluctuation at Room Temperature

As discussed in 3.3.3, to reduce the non-uniform device operation property due to the variation of dopants in the island, we will wish increase the doping density in the device. But, higher doping density means higher impurity in the device (For example, for a boron doped device, with more boron in the lattice site caused more silicon in the interstitial site), and the device will tend to be poly-Si like than single crystalline structure. Every grain boundary exists in the island will change the electron transport property of the device. However, if we use intrinsic silicon, the peripheral resistance near the island will become very large. This will shift the device's characteristic from tunneling domination (single electron device like) to drift domination (Resistor like).

3.4.5 Single Crystal Island

Single electron tunneling process is hard to observe in semiconductor material. Because single crystal island is hard to fabricated in semiconductor material than metal, co-tunneling cannot be avoided in such condition. But on the other hand, quantum effect is difficult to see in metal due to shorter Fermi wavelength (at the length near few angstroms about one to two order shorter than that in the semiconductor). Usually, metal dot is fabricated from bottom up (i.e. Figure 2.3), and semiconductor islands are formed from top down method. Despite what material we choose, we will face the challenge in production technique whether in size control or single crystal island formation.

According to the discussions above, we can conclude that to "optimize" a silicon based single electron device is very difficult due to some conflicts. To avoid some problems we may face, using molecular to replace to the island and two tunneling junctions is the most suitable way. Since molecular are well defined object, with highly consist properties and dimensions between one to another.

With traditional MOSFET scale down to tens of nanometer diameter, the leakage current due to thin gate oxide and short channel effect may led the off current too large to integrate circuits applications. Single electron transistor has been proposed at 1986, but it faces so many problems (part are discussed just above). The combination of fabrication method both from bottom up (self-assembly molecular) and top down to achieve nanometer scale device are widely surveyed nearby. Single molecular transistor is one of possible solutions. Using our fabrication method with proper over etching may provide a base structure for SMT. This may be achieved in our future work.

Chapter 3 References

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TABLE 3.1 DEVICE DIAMETERS

Fabricated	Symbol	C5	D5
Height (nm)	H	70	70
Width (nm)	W	60	60
SgW (nm)	Sw	150	200
GtoL (nm)	gl	60	50
Line (um)	L	2	2

Table 3.2 REFERENCE QUANTITIES

Doping Desity (cm^{-3})	$5*10^{15}$
Dopants in QD	3
Dopants in NW	48
Vbi (Al) at 30 K (V)	0.285
Vbi (Al) at 60 K (V)	0.255
BOX (nm)	2300
de Broglie wave length (nm) ~ 30 K	27
de Broglie wave length (nm) ~ 16 K	40

Table 3.3 PREDICTION OF ELECTRON MOBILITY IN THE EXPERIMENT

	C5_30K	D5_60K
Vds	1.5	0.8
drift_Id (A)	2E-11	5E-12
Mobility ($cm^2/V \bullet s$)	20500	11160

Table 3.4 DEVICE PARAMETERS

		C5	D5	C5_20K	C5_30K	D5_16K
Ccg (aF)	ε_{SiO2}*W*H/gl	2.42	2.90	5	3.56	5.33
Cd (aF)	ε_{Si}*W*H/(Sw/2)	5.9	4.42	35.56	35.56	40
Ctot (aF)	2*Csg + Ccg	14.21	11.75	77.04	74.67	85.93
Delt Vd (mV)	e/Cd	27.13	36.17	4.50	4.50	4
Delt Vg (mV)	e/Ccg	66.22	55.19	32	45	30
ChrE (meV)	e^2/(Ctot*2)	5.63	6.81	1.05	1.07	0.76
Opr Tmp (K)		65.46	79.20	12.22	12.46	10.90

Table 3.5 DEVICE PARAMETERS (MODIFIED)

		C5	D5	C5_20K	C5_30K	D5_60K
Ccg (aF)	ε_{SiO2}*W*H/gl	2.42	2.90	5	3.56	5.33
Cd (aF)	ε_{Si}*W*H /(Sw-QD)/2	6.70	4.94	6.70	6.70	4.90
Ctot (aF)	2*Csg + Ccg	15.82	12.78	18.40	16.96	15.13
Delt Vd (mV)	e/Cd	23.87	32.37	23.88	23.88	32.00
ChrE (meV)	e^2/(Ctot*2)	5.06	6.26	4.35	4.72	5.29
Opr Tmp (K)	ChrE / k	58.80	72.77	50.56	54.86	61.47

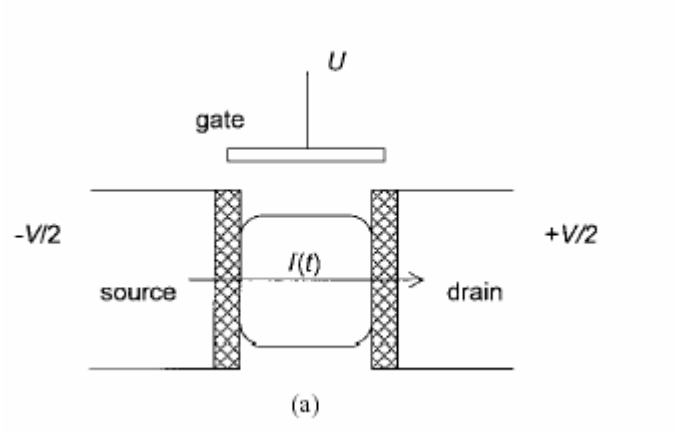

Figure 3.1 Schema of Single Electron Transistor [8]

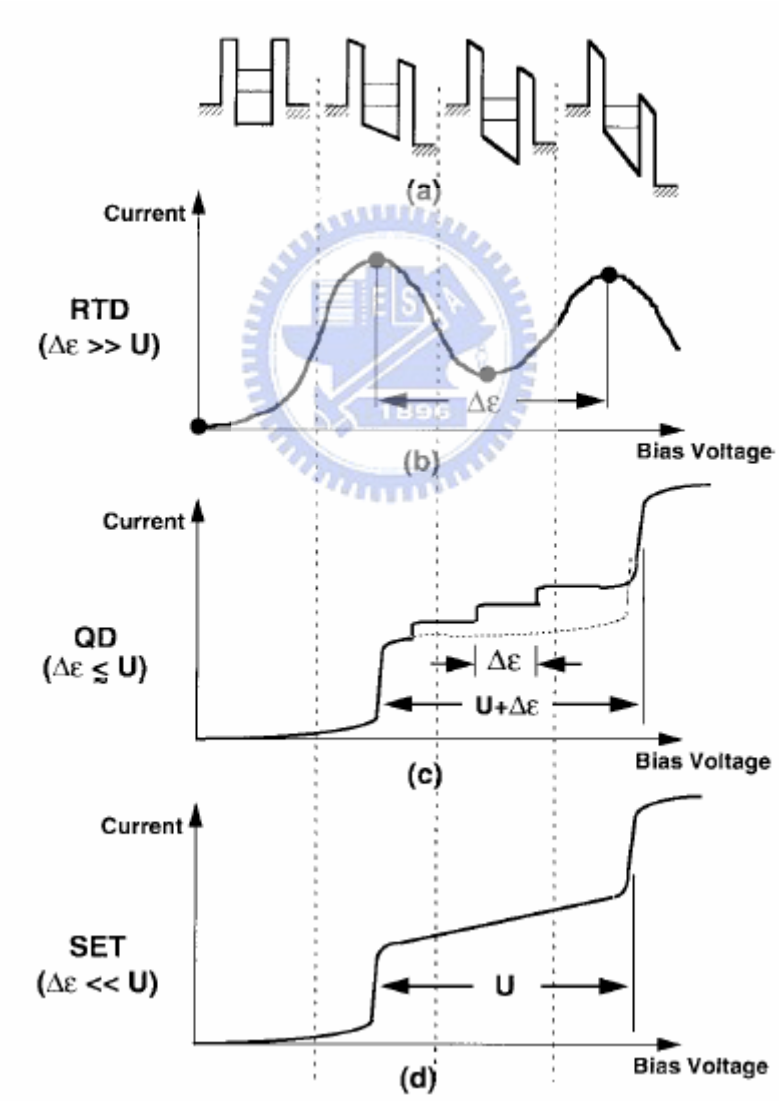

Figure 3.2 Id-Vd curves for three categories of solid-state nanoelectronic devices [4]

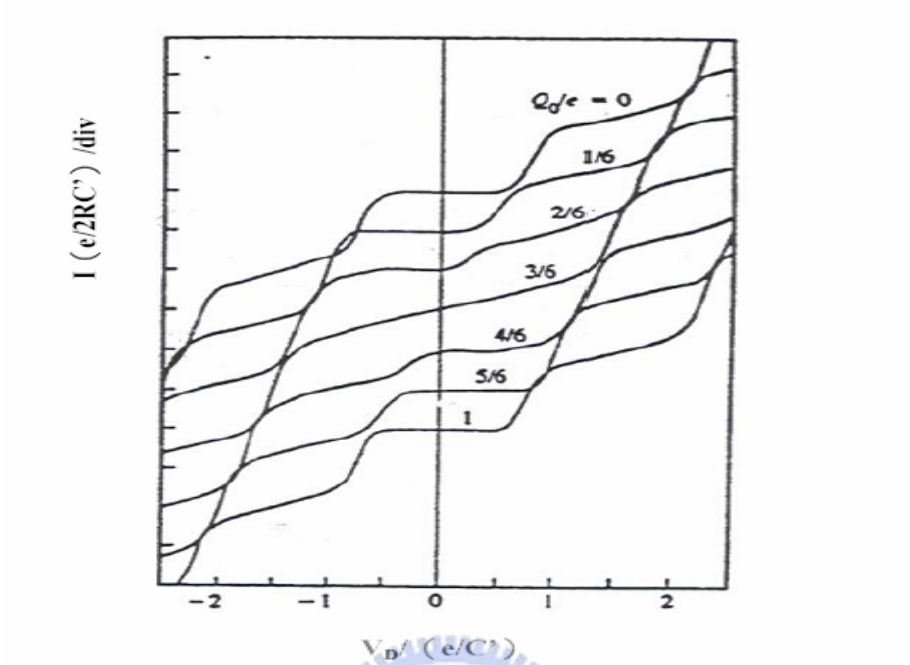

Figure 3.3 SET's Theoretical Id-Vd Curve [9]

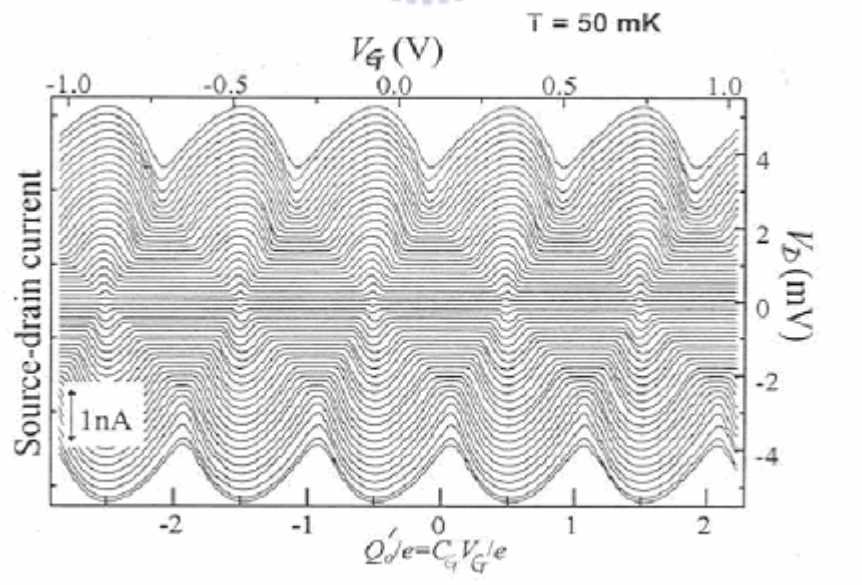

Figure 3.4 SET's Theoretical Id-Vg Curve

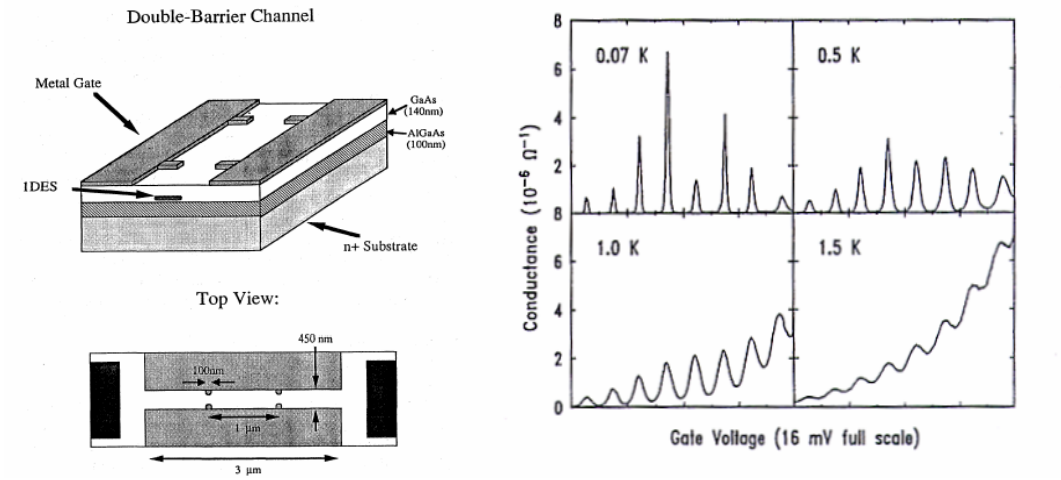

Figure 3.5 (a) Depletion Gate SET and (b) its Id-Vg curve [10]

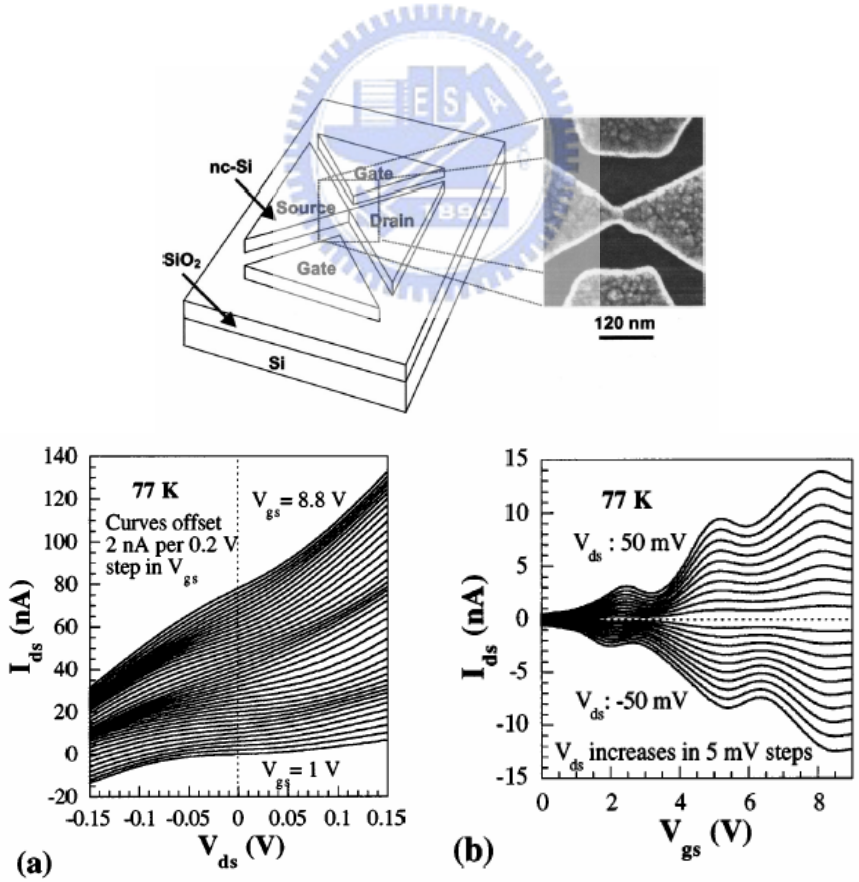

Figure 3.6 (a) Point Contact SET and its (b) Id-Vd and (c) Id-Vg curves [11]

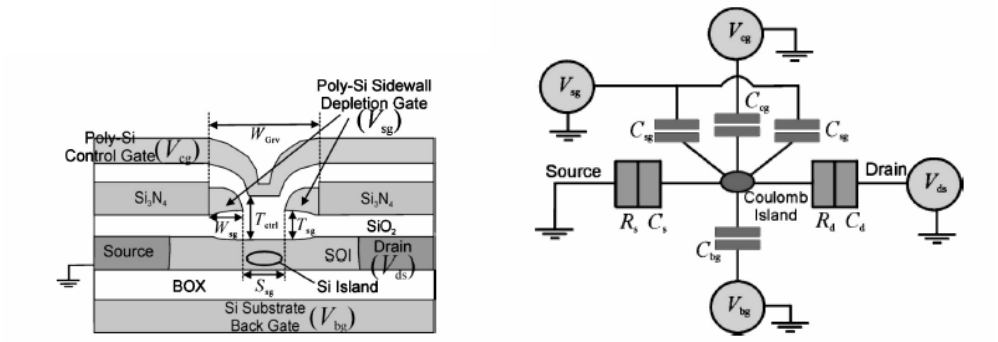

Figure 3.7 (a) Schema of Depletion Gate SET and its (b) Equilibrium Circuits [13]

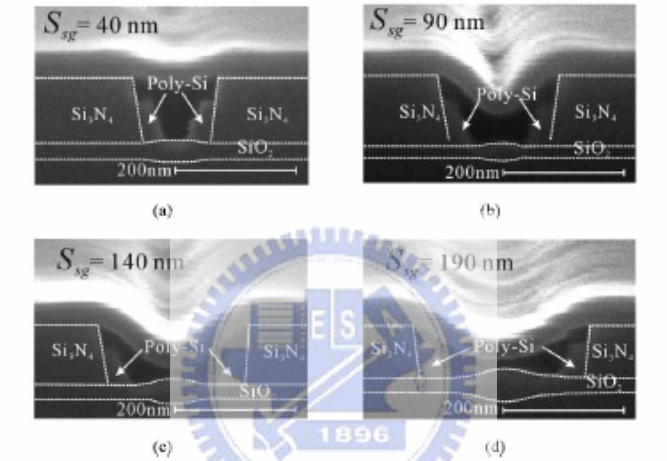

Figure 3.8 SEM images for SET with Different Island Diameter [13]

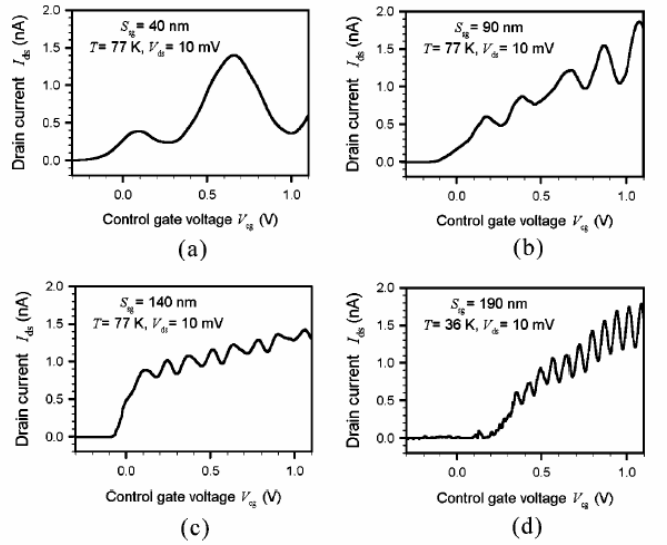

Figure 3.9 Depletion Gate SET's Id-Vg Curve Measured at Different Conditions [13]

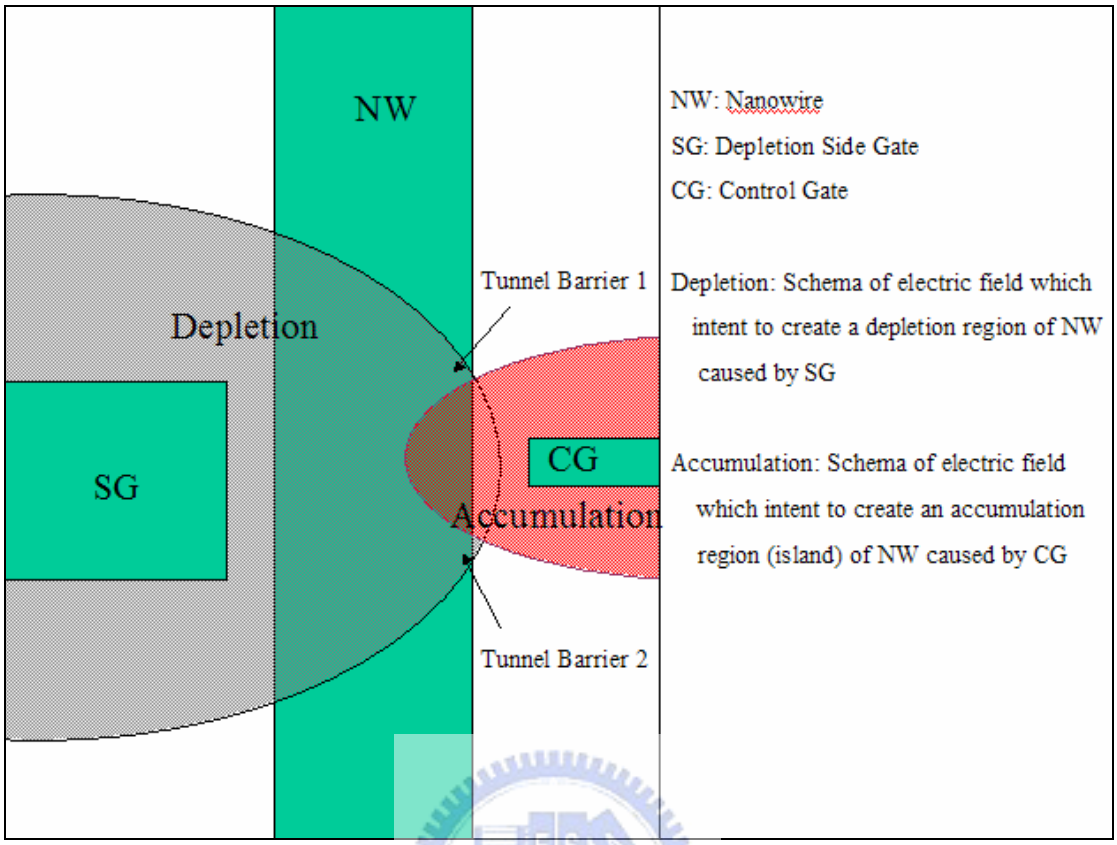

Figure 3.10 Schema of depletion gate device in this experiment

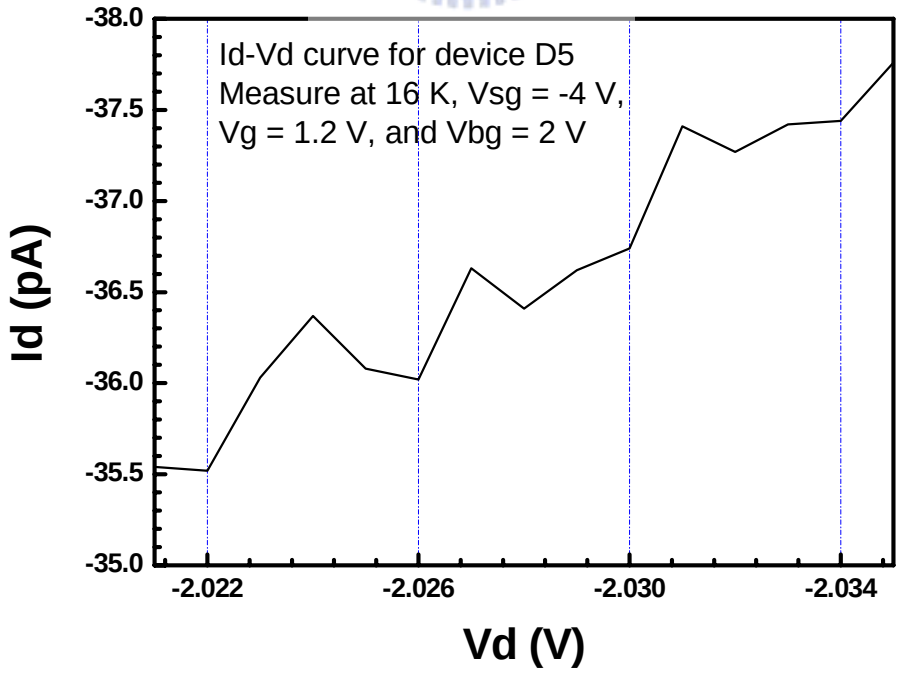

Figure 3.11 Id-Vd measure at 16 K, Vsg = -4, Vg = 1.2 V, and Vbg = 2 V (D5)

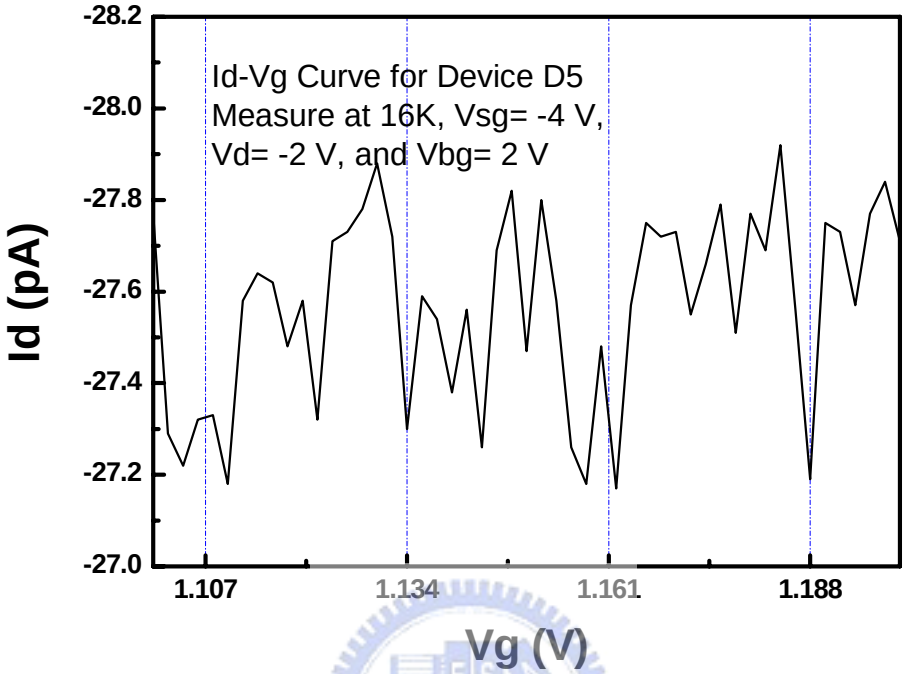

Figure 3.12 Id-Vg measure at 16 K, Vsg = -4 V, Vd= -2 V, and Vbg= 2 V (D5)

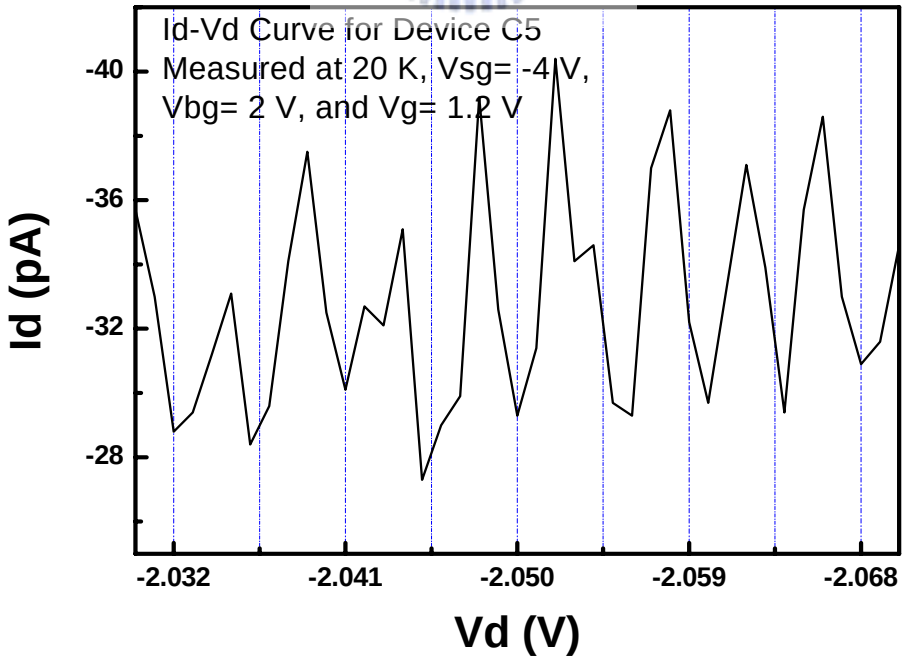

Figure 3.13 Id-Vd measured at 20 K, Vsg = -4 V, Vbg = 2 V, and Vg = 1.2 V (C5)

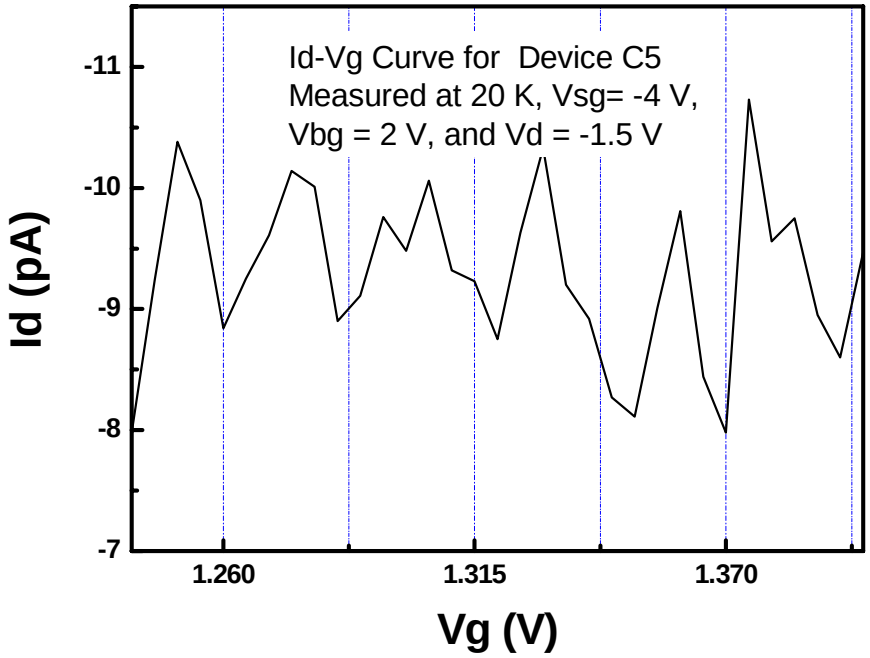

Figure 3.14 Id-Vg measured at 20 K, Vsg= -4 V, Vbg = 2 V, and Vd = -1.5 V (C5)

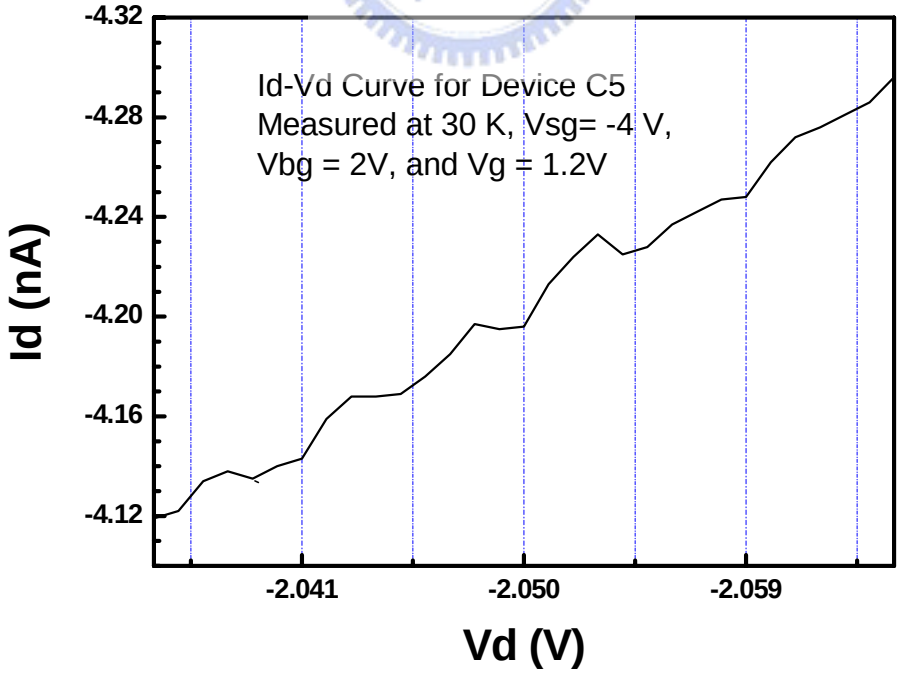

Figure 3.15 Id-Vd measured at 30 K, Vsg = -4 V, Vbg = 2 V, and Vg = 1.2 V (C5)

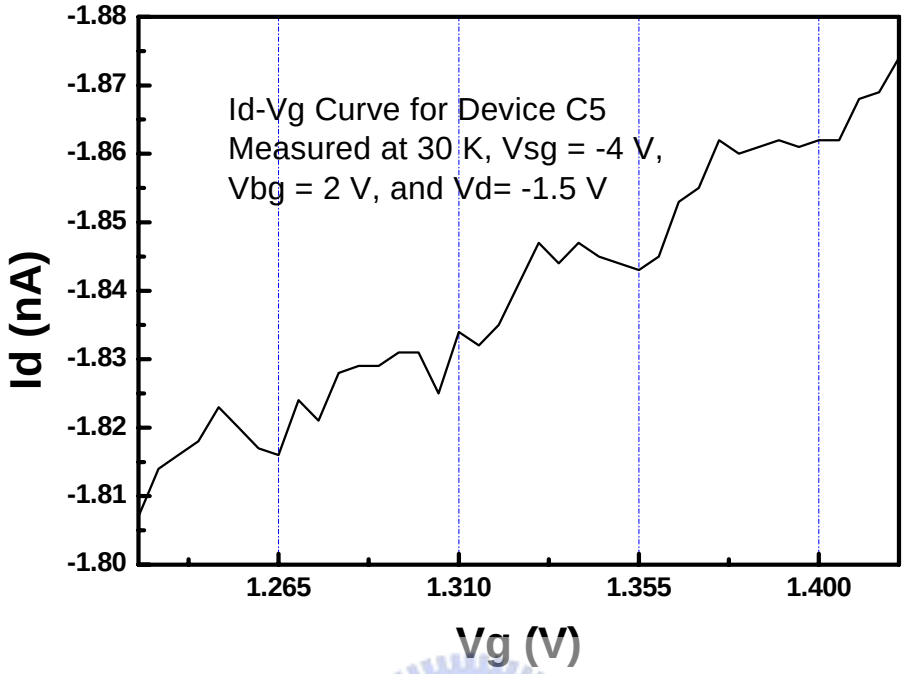

Figure 3.16 Id-Vg measured at 30 K, Vsg = -4 V, Vbg = 2 V, and Vd = -1.5 V (C5)

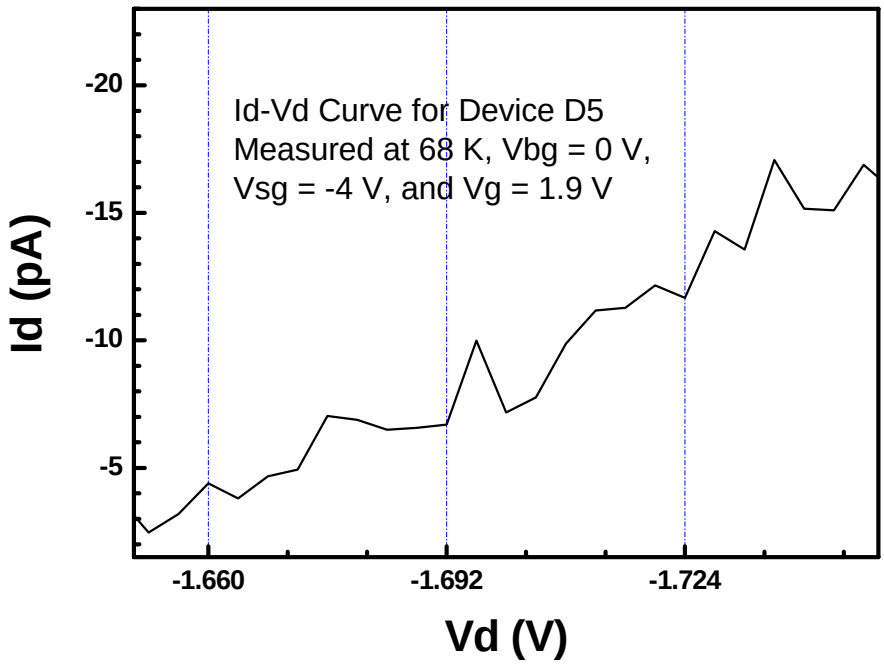

Figure 3.17 Id-Vd measured at 68 K, Vbg = 0 V, Vsg = -4 V, and Vg = 1.9 V (D5)

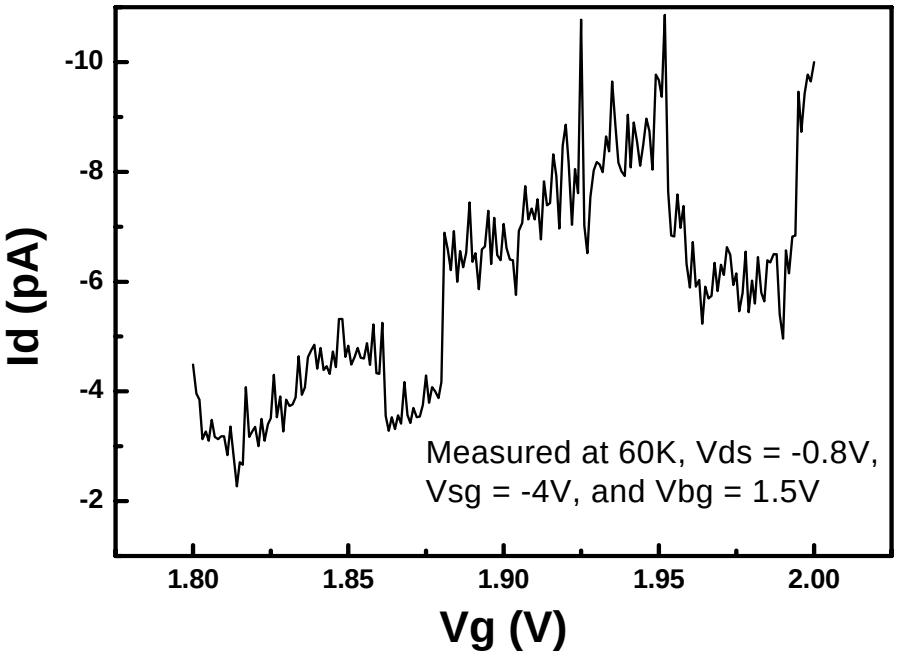

Figure 3.18 Id-Vg measured at 60K, Vds= -0.8V, Vsg= -4V, Vbg= 1.5V (D5)

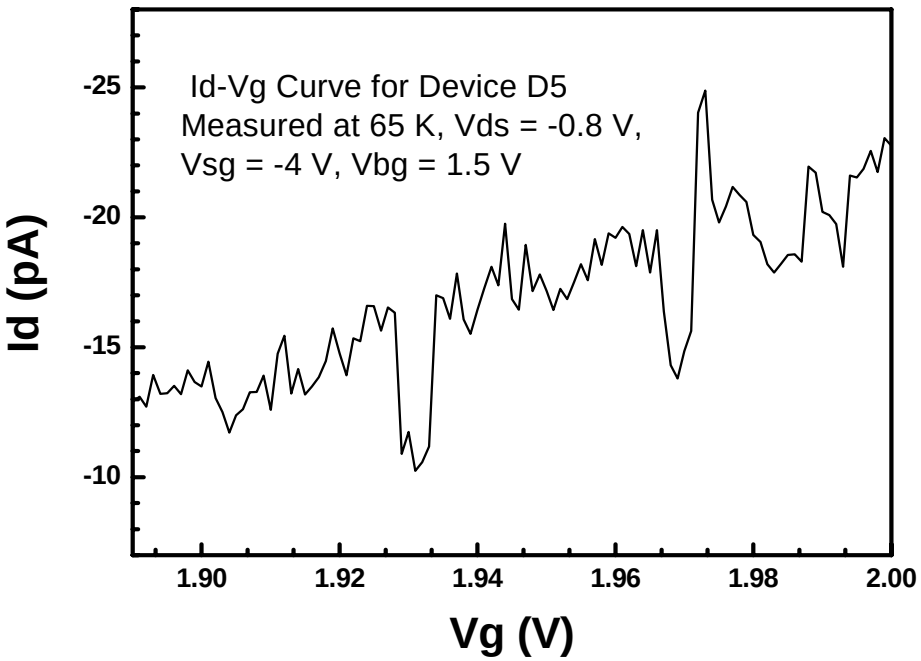

Figure 3.19 Id-Vg measured at 65 K, Vds = -0.8 V, Vsg = -4 V, Vbg = 1.5V (D5)

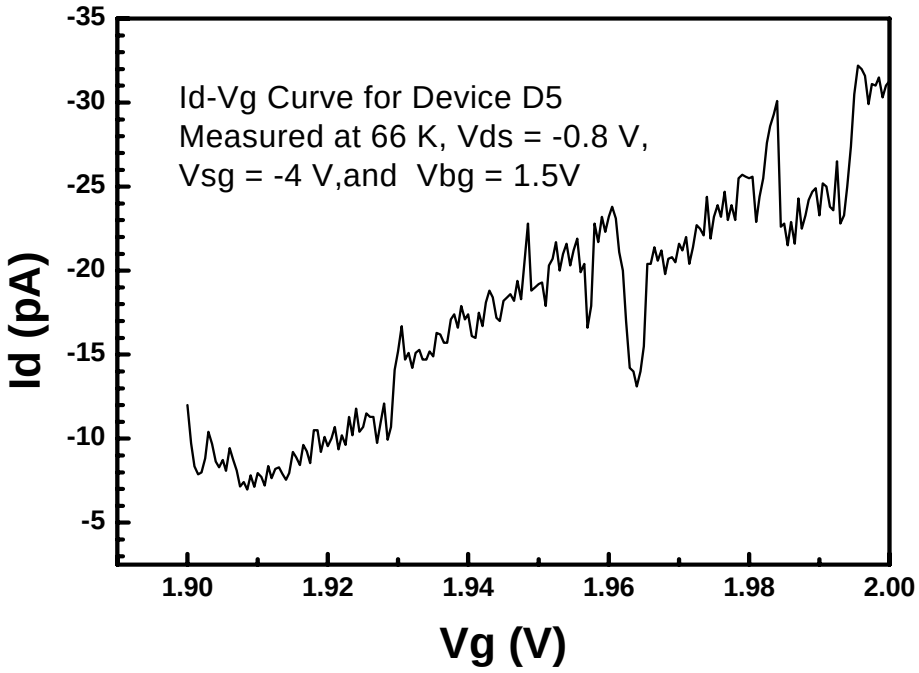

Figure 3.20 Id-Vg measured at 66 K, Vds = -0.8 V, Vsg = -4 V, and Vbg = 1.5 V (D5)

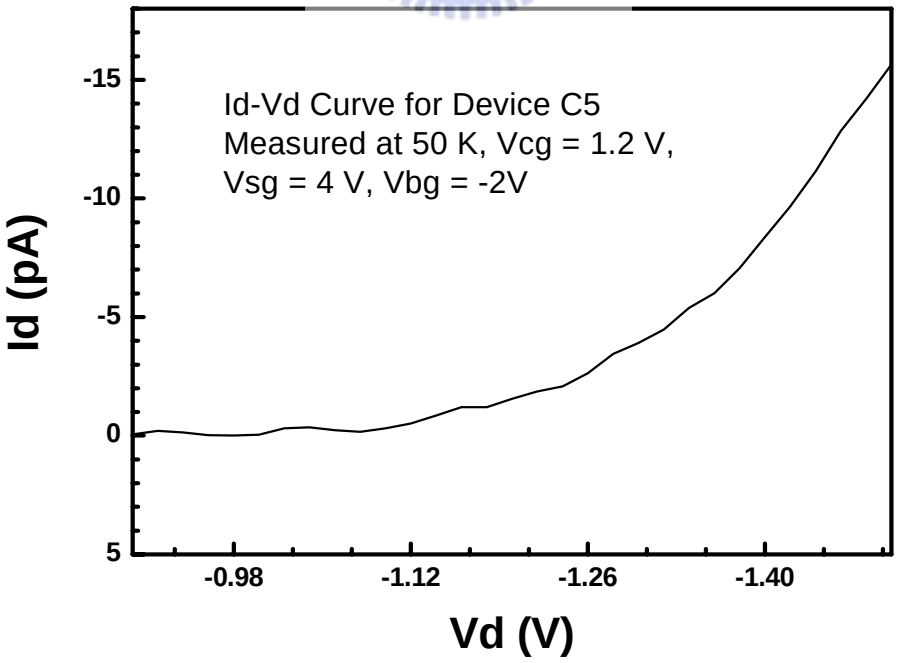

Figure 3.21 Id-Vd measured at 50 K, Vcg = 1.2 V, Vsg= -4 V, and Vbg = -2V (C5)

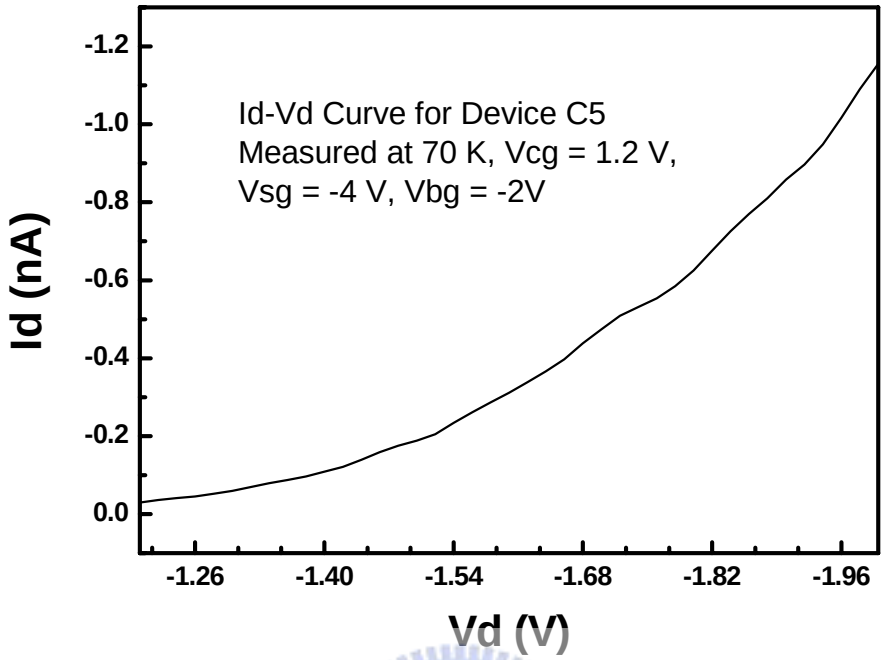

Figure 3.22 Id-Vd measured at 50 K, Vcg = 1.2 V, Vsg= -4 V, and Vbg = -2V (C5)

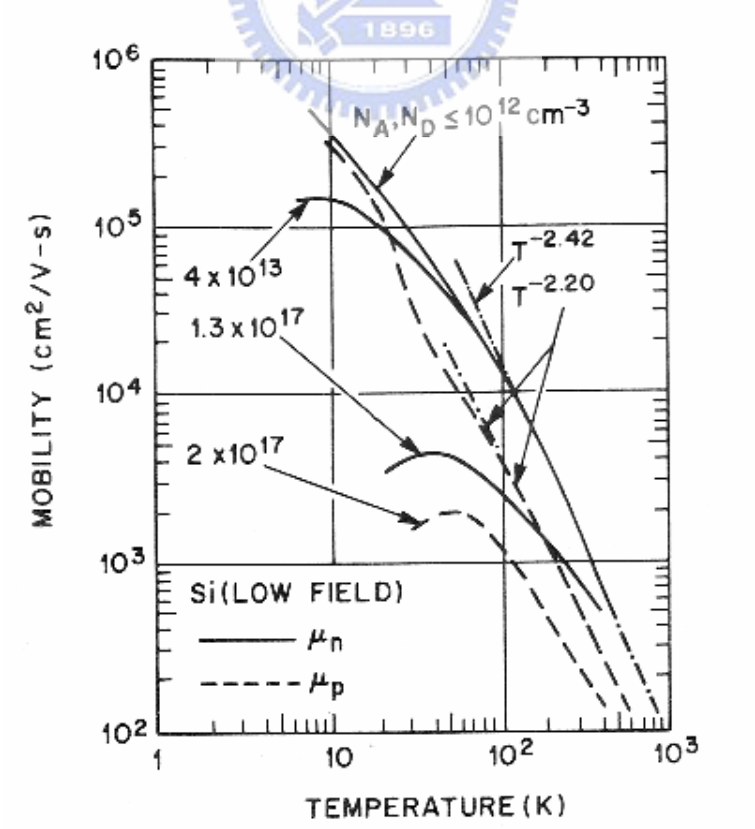

Figure 3.23 Mobility of electrons and holes in Si as a function of temperature. [16]

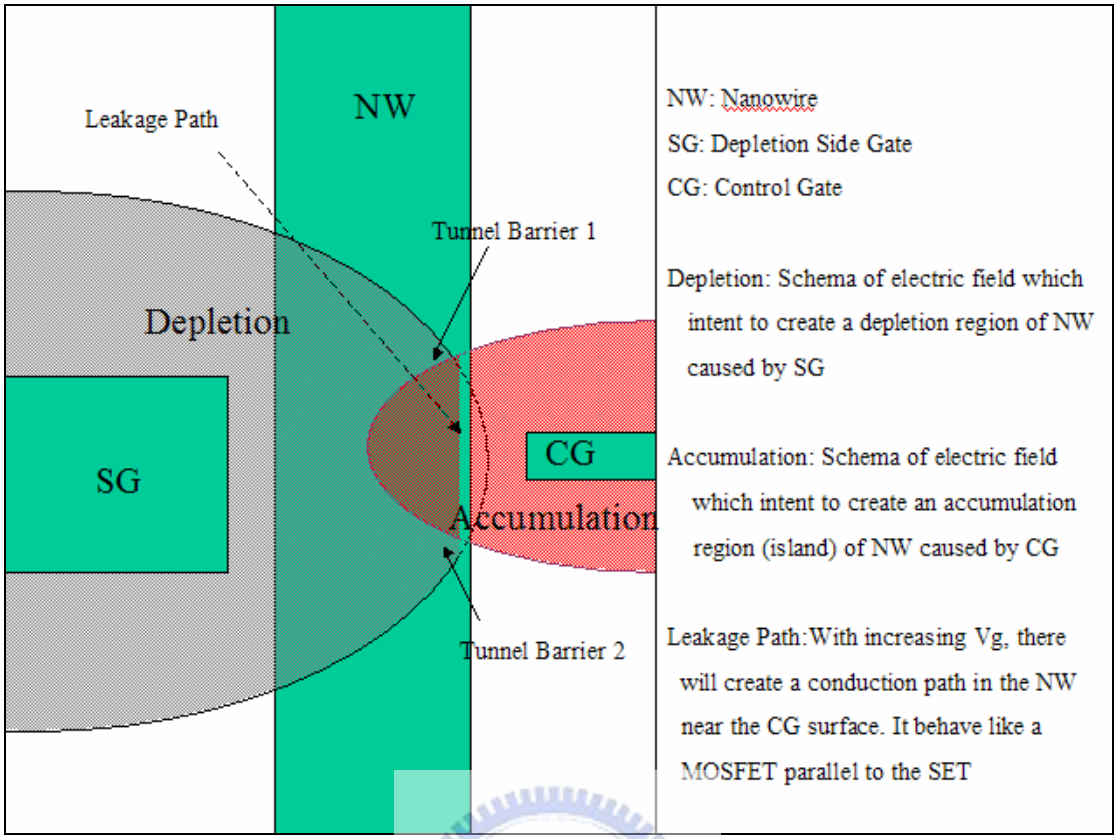

Figure 3.24 Schema of depletion gate device with leakage path in this experiment

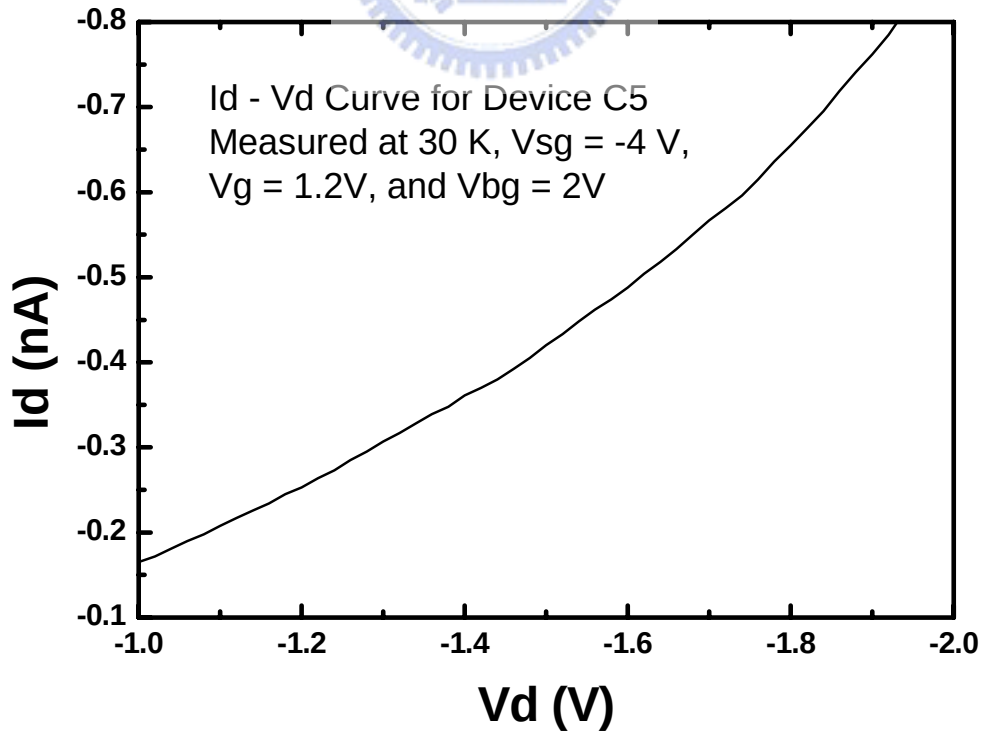

Figure 3.25 Id-Vg curve measured at 30 K, Vsg = -4 V, Vg = 1.2 V, and Vbg = 2V.

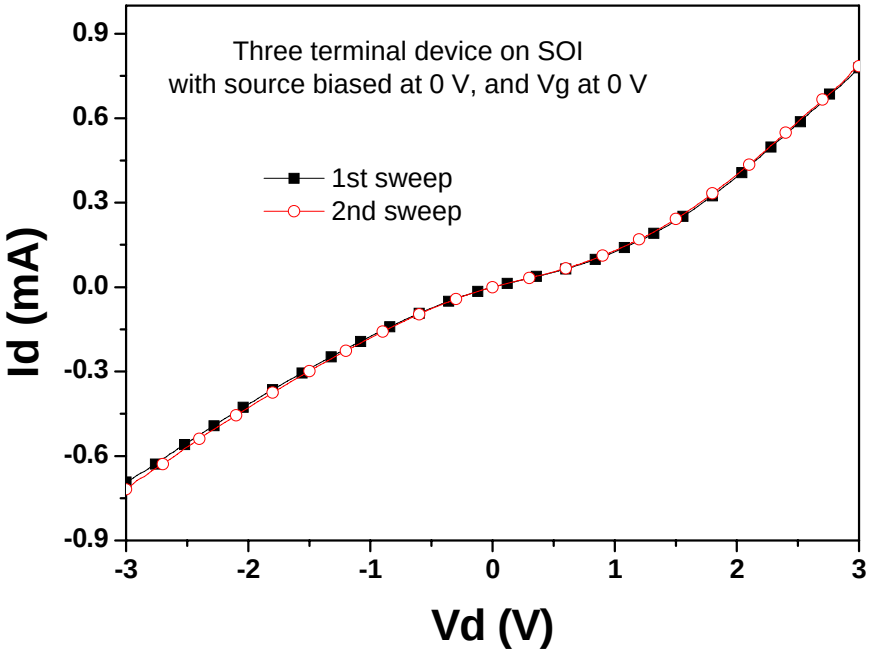

Figure 3.26 Id-Vd curve measured by sweeping Vd from –3 V to 3 V at Vg = 0 V. Id measured at Vd = 0 V is 40 nA. Interval between two measurements is 20 s. These two measurements show highly reliability.

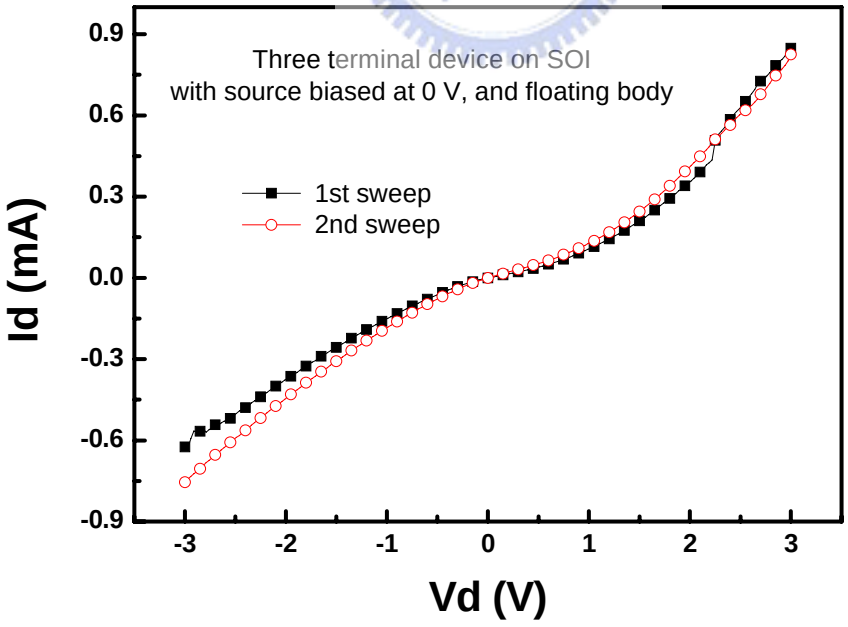

Figure 3.27 Id-Vd curve measured by sweeping Vd from –3 V to 3 V with floating body. Interval between two measurements is 20 s. These two measurements show the floating body effect.

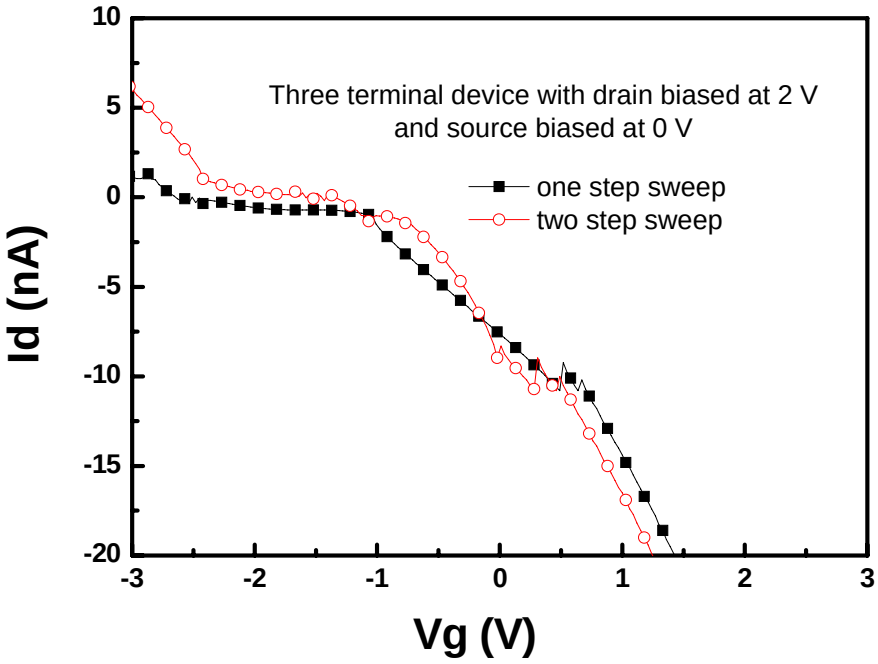

Figure 3.28 Id-Vg curves measured by sweeping Vg from 0 V to –3 V and 0 V to 3 V (two step sweep), and sweeping Vg from –3 V to 3 V. Two measurements show different results due to charging effect.

Chapter 4 Conclusion

In Chapter 2, we have demonstrated that silicon nanometer devices can be well fabricated by top-down process with combining the scanning probe lithography (SPL) and orientation dependent etching (ODE) wet etching methods. The SPL process shows the well ability to define the silicon device's structure in nanometer scale. The low temperature wet etching process by 25% TMAH solution shows the low cost of setup and the well controlled etching ability to fabricate silicon nanometer device with high aspect ratio. In conclusion, the silicon nanometer devices can be easily fabricated from 10 nm to several hundreds nanometer in line-width with great stability and reliability. We set up a standard process flow to make nanometer devices, which provide a conventional basis for future studies in nanometer scale phenomena.

In Section 3.2, we demonstrate the transport characteristics of silicon based single electron device. Device fabrication process follows the technique developed in Chapter 2. The basic idea to achieve SED is using the depletion gate method. We also observed many other non-ideal phenomena with our device at different bias conditions and temperatures. We analyzed these characteristics and give them reasonable explains. These understandings can become good basis for us to design new device structures and predict their properties.

Future Work

As device shrikes down to nanometer scale, quantum effects become more series. The study in the Chapter 3 may give some ideas about single electron tunneling behavior. Some researchers [1,2] declare that the traditional MOSFET structure may out of use in sub –10-nm scale due to direct electron tunneling from source to drain. Our study in Section 3.2 gives an easy approach to observe quantum phenomena in nanometer scale but still not meet the requirements to be the post-MOSFET device (i.e. virtual dimension smaller than 5 nanometer). It seems that the single molecular transistor (SMT) [3] is most possible way to achieve this requirement. By the technique developed in Chapter 2, we will try to establish a base model for SMT device in the future.

We also use the technique established in Chapter 2 to fabricate silicon nanowire (SiNW) devices. The device shows high potential in biologic detection application. Relative results are not included in this thesis, but can be find in reference 4. We will devote to establish a suitable model to explain our results. And we will integrate the SiNW and micro-fluid channel (eliminate the noises in the atmosphere environment) together to give more robust device design.

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2. M. S. Lundstorm, IEEE Electron Dev. Lett. 22 ,pp.293-295 (2001)
3. W. Wang, T. Lee, and M. A. Reed, Physica E 19, pp. 117-125 (2003)
4. K. S. You. “”Fabrication technique and characterization of silicon nanowire divice”, Ph. D dissertation, department of electronics engineering, NCTU (2004)