國　立　交　通　大　學

電子工程學系電子研究所碩士班

碩　士　論　文

高功率碳化矽金氧半場效電晶體之元件結構與應用之探討

Investigation of Device Structure and Application of SiC Power MOSFET

學生：楊志潘　　Student：Chih-Pan Yang

指導教授：張國明 博士　　Advisor：Dr. Kow-Ming Chang

中華民國九十三年六月

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碩士論文

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摘　要

基本上功率電晶體是含有數微米了磊晶矽耐壓區及垂直式的元件結構，在傳統的雙擴散金氧半功率電晶體，由於在平面通道元件密度及導通阻抗有其極限，未達高元件密度與低阻抗的要求，往往限制了傳統雙擴散功率的電晶體的表現。溝槽式閘極高功率金氧半場效電晶體雖有助於改善導通阻抗以增進元件密度，然在溝槽底部卻需要考慮尖端電場的問題，限制了最大操作電壓。在此嘗試提出一個高功率碳化矽增強型電晶體結構將有助於改善傳統功率元件的缺點。

由於以矽為基底的功率電晶體在操作電壓及導通電阻的受限，因碳化矽本身優越的物質特性，碳化矽功率電晶體逐漸為人所用，本篇論文首先強調碳化矽在高功率元件元件應用的優勢，引用正確的模型與參數的修正。以期能對不同結構下的高功率元件所比較的結果做一精確的分析，藉著討論傳統溝槽式及雙擴散式功率電晶體所面臨的閘極氧化層崩潰及夾止效應，提出一個新式的改良結構，並以 MEDICI 模擬軟體討論參數的最佳化，並與傳統結構的電晶體做比較，證明其優越的性質。

Investigation of Device structure and Application of SiC Power MOSFET

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ABSTRACT

The basic structure of power MOSFET consists of an epitaxial layer for voltage blocking and a drain electrode at the substrate contact. In the conventional double diffused MOSFET, the poor channel resistance and JFET effect limited the DIMOS performance. The trench gate MOSFET, have a much improved on-resistance and packing density because of its vertical channel, however, a high local electric field at the trench corner is of critical importance to the performance of the device. A innovative structure of SiC accumulation-mode MOSFET designed to improve the performance of conventional structure of power MOSFET.

This thesis focused on the design of high voltage MOSFET on SiC power devices. Parameter extraction for 4H-SiC MOS devices is the main focus for this thesis, which includes the mobility parameter extraction. Detailed analysis of the important design parameters of the innovative structure is performed using MEDICI with the parameter been used in calibration process.

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Contents

Table Captions

Figure Captions

Fig. 4.7(c) Effects of P-base thickness on Ron resistance.

Chapter 1
Introduction

1-1 Introduction to power devices

The development of electronic power systems based on semiconductor devices can be traced to the early 1950s. At that time, the first rectifiers and thyristors are capable of operating at high current and voltage levels. Since that time considerable progress has been made in discrete power semiconductor device technology. The most important development is the creation of a new family of power devices with high-input-impedance metal oxide semiconductor (MOS) gates. The silicon power MOSFET has become the dominant device technology for these applications. These devices greatly reduce the size and complexity of the control circuitry. This has allowed a large reduction in system cost, marking the power electronics attractive for many new applications such as control of home appliances and for automotive electronics as shown in Fig. 1.1[3].

The power MOSFET is a unipolar device. Current conduction occurs through transport of majority carriers in the drift region without the presence of minority carrier injection required for bipolar transistor operation. No delays are observed as a result of storage or recombination of minority carriers in power MOSFETs during turn-off. Their inherent switching speed is orders of magnitude faster than that for bipolar transistors. This feature is particularly attractive in circuits operating at high frequencies where switching power losses are dominant.

Power MOSFETs have also been found to display an excellent safe operating area, that is,

they can withstand the simultaneous application of high current and voltage (for a short duration) without undergoing destructive failure. These devices also easily paralleled because the forward voltage drop of power MOSFETs increase with increasing temperature. This feature promotes an even current distribution between paralleled devices.

However, for blocking voltages exceeding e.g., 500V state of the art, silicon power MOSFETs cannot compete against bipolar switches because of high resistance of the drift region. A much favorable situation is given for silicon carbide (SiC) power MOSFETs. Silicon carbide is rapidly maturing as a semiconductor material system since the commercial available single crystal substrates. Due to its high breakdown field, high thermal conductivity, and high-temperature operation, SiC is a attractive semiconductor for future power devices.

1-2 Basic Structure And Operation of Power MOSFET

1-2-1 Basic Structure

An understanding of the operation of MOSFETs can best be gleaned by the first considering the lateral N-channel MOSFET shown in Fig. 1.2. Such devices have the drain, gate, and source terminals on the same surface of the silicon wafer. Although this feature makes them well suited for integration, it is not optimum for achieving a high power rating. The vertical channel structure with source and drain on opposite surfaces of the wafer is more suitable for a power device because more area is available for the source region and because the electric field crowding at the gate is reduced.

Three discrete vertical-channel power MOSFET structure have evolved. A cross section

of these structures is provided in Fig. 1.3. The first structure was the vertical channel V-MOS power FET, shown in Fig. 1.3(a) whose name is driven from the V-shaped groove within which the gate is located. Although the V-MOSFET was the first commercial structure, it was replaced by the DMOSFET because of stability problems during manufacturing and a high local electric field at the tip of the V-groove.

The DMOS structure shown in Fig. 1.3(b) is fabricated by using planar diffusion technology with a refractory gate such as polysilicon, as a mask. In these devices, the P-base region and the N^+ source region are diffused through a common window defined by the edge of the polysilicon gate. The name for this device is driven from this double-diffusion process. The P-base region is driven in deeper than the N^+ source. The difference in the lateral diffusion between the P-base and N^+source regions defines channel region. This has been the most commercially successful structure.

The third power MOSFET structure that has been explored is the U-MOSFETs structure shown in Fig. 1.3(c). The name for this structure is driven from the U-shaped groove formed in the gate region b using reactive ion etching. The U-groove structure has a higher channel density than either the VMOS or DMOS structures which allows significant reduction in the on-resistance of the device.

1-2-2 Operation of power MOSFETs

The operation of the power MOSFET relies upon the formation of a conductive layer at the surface of the semiconductor as shown in Fig. 1.4. In order to carry current from source to drain in the power MOSFET, it is essential to form a conductive path extending between the

N^+ source regions and the N^- drift region. This can be accomplished by applying a positive bias to the gate electrode. The gate modulates the conductivity of the channel region by the strong electric field crated normal to the semiconductor surface through the oxide layer. Note that the current flow occurs solely by transport of majority carriers along a resistive path comprising the channel and drift regions. No minority carrier transport is involved for the power MOSFET during current conduction in the on-state. In order to switch the power MOSFET into the off-state, the gate bias voltage must be reduced to zero by externally shorting the gate electrode of the source electrode. When the gate voltage is removed, the electrons are no longer attracted to the channel and the conductive path from drain to source us broken. The power MOSFET then switches rapidly from the on-state to the off-state without any delays arising from minority carrier storage and recombination as experienced in bipolar devices.

Breakdown voltage and on-resistance are two major consideration in designing a power MOSFET. Breakdown voltage can be determined from Id-Vd characteristics of the device. On-resistance is the total series resistance between the source and the drain terminals when the device is turned on. An ideal power MOSFET exhibits high breakdown voltage and low on-resistance simultaneously. Unfortunately, these two requirements are always not met in real design.

1-3 The Application of SiC in Power Devices

Silicon carbide is a wide energy gap semiconductor that possesses a combination of parameters that makes it ideal for various applications in the electronic industry. Its physical properties such as high electric field strength, high saturation drift velocity, and high thermal

conductivity, has made SiC as the center of a renewed focus of semiconductor material and device research amongst the other wide energy gap semiconductors. Compare with other wide energy gap semiconductor suchⅢ/Ⅴ Nitrides, SiC has tremendous advantages because of rapidly maturing technology for making single crystal substrates.

The relatively low breakdown field in Si and the resistance of the drift region that increases rapidly with increasing blocking voltage generally limit the use of Si MOSFET to 500V and below. The advantage of SiC material properties, See Table 1.1, in particular the high breakdown field, makes SiC MOSFETs a very promising candidate for high power switching devices. The specific on-resistance of the SiC power device is expected to be 100~200 times lower than a similarly rated silicon device. Its much lower thermal minority carrier generation implies lower leakage currents and device operation at higher temperatures, arising from self-heating due to power dissipation, is more tolerable. Moreover, the thermal conductivity of SiC is three higher than Si and even higher than cooper at room temperature, also implying a higher efficiency of heat extraction from the device and a further reduction in the requirements for device cooling.

1-4 Thesis Organization

The first part is the introduction which briefly introduces the topic. Chapter 2 begins with the introduction of the two-dimension device simulator, MEDICI, which is used throughout this thesis. It is followed by the important bulk parameter set for 4H-SiC devices. Chapter3 the SiC power device is then proposed and analyzed. We also make the general analysis of 4H-SiC as compared to Si power MOSFET. The fourth part is “result and discussion” which represents the advantages of silicon carbide applied in power devices.

Finally a conclusion of this thesis is given some recommendation of future work are suggested.

Chapter 2

Models and Parameters for Device Simulation.

Numerical device modeling and simulation are essential for analyzing and developing semiconductor devices. They help a design engineering not only gain an increased understanding of the device operation, but also provide the ability to predict electrical characteristics, behavior, and parameter-effects influence of the device. With this knowledge and abilities the designer a better structure, estimate device performance, perform the analysis of worst case, and optimize device parameters to yield an optimize device performance.

2.1. Introduction

Medici is a powerful device simulation program that can be used to simulate the behavior of MOS and bipolar transistors, and other semiconductor devices [2]. It models the two-dimensional distributions of potential and carrier concentrations in a device. The program can be used to predicted electrical characteristics for arbitrary bias conditions. As in any device simulator, any quantitative, or even qualitative, simulation of device relies heavily on applicable device models and their parameter values. A number of physical models are incorporated in MEDICI for accurate simulations. Furthermore MEDICI also supports a variety of semiconductor materials including SiC [13].

2-2 MEDICI Description

The primary function of Medici is to solve the following three partial differential equations [2].

The Poisson equation

$$\varepsilon\nabla^2\psi = -q\left(p - n + N_D^+ - N_A^+\right) - \rho \tag{1}$$

Continuity equation for electron and hole.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - U_n \tag{2}$$

$$\frac{\partial p}{\partial t} = \frac{-1}{q}\nabla \bullet J_p - U_p \tag{3}$$

Throughout Medici, ψ is always defined as the intrinsic Fermi potential. That is, $\psi = \psi_{\text{intrinsic}}$. N_D^+ and N_A^+ are the ionized impurity concentrations and ρ_s is a surface charge density that may be present due to fixed charge in insulating materials or charged interface states .

The numerical algorithms used in MEDICI to solve the fundamental equations are based on the finite element method, which discretized these equations on a simulation grid. This discretization process yields a set of coupled nonlinear algebratic equations which represent a number of grid points, for the unknown potentials and free-carrier concentrations. This set of coupled nonlinear equations in return must be solved a nonlinear iteration method. Two iteration methods, Gummel's and Newton's method are available in MEDICI. Regardless which iteration method used, the solutions are carried out over the entire grid until a self-consistent potential and free-carrier concentrations are obtained. Once the potentials and free-carrier concentrations have been calculated at a given bias, it is possible to determine the quasi-Fermi levels and the hole and electron currents (Jn and Jp **).**

2-3 Simulation Physical Models

2-3-1 The Parameter Set for 4H-SiC

In order to achieve realistic results, it is imperative to use proper models for the 4H-SiC properties. The most important physical models employed in the simulations are for intrinsic concentration, carrier mobility in bulk, transverse and parallel field within the channel region, SRH recombination, Auger recombination and impact ionization.

(1) Intrinsic concentration:

Accurate models for the carrier concentration in semiconductor devices are a necessity if qualitatively and quantitatively correct simulation results are to be obtained. The intrinsic carrier concentration n_i is determined by the fundamental energy gap E_g and the effective density of states N_C and N_V in the conduction and valence bands. Where, neglecting band gap narrowing, the intrinsic carrier concentration is [2]

$$\mathrm{n_i(T)} = \sqrt{\mathrm{NcNv}}\exp\left(\frac{-\mathrm{E_g}}{2\mathrm{kT}}\right) \tag{4}$$

where $\boldsymbol{E_g}$ is the bandgap energy of the semiconductor, that is,

$$\mathrm{E_g} = \mathrm{E_c} - \mathrm{E} \tag{5}$$

where N_C and N_V are defined as

$$\mathrm{Nc(T)} = \mathbf{NC300}\left(\frac{\mathrm{T}}{300}\right)^{3/2} \tag{6}$$

$$\mathrm{Nv(T)} = \mathbf{NV300}\left(\frac{\mathrm{T}}{300}\right)^{3/2} \tag{7}$$

the parameters **NC300** and **NV300** are user specified and can be modified from their values on the Material statement to fit the 4H-SiC in unipolar devices.

At high doping levels, the carrier-carrier interaction and overlap of the electron wave functions are not negligible. Since no study of bandgap narrowing effects has been performed, these BGN (bandgap narrowing effects) known from Si are taken into account by an effective carrier concentration [13].

$$n_{ie}(T) = n_i(T)\exp(\frac{V_g}{2kT}) \quad (8)$$

$$V_g = C_g\left(F + \sqrt{F^2 + 0.5}\right) \quad (9)$$

with

$$F = \ln\left(\frac{N_D + N_A}{N_{BGN}}\right) \quad (10)$$

In MEDICI [2]

$$n_{ie}(x,y) = n_i \bullet \exp\left\{\frac{\mathbf{V.BGN}}{2kT}\left[\ln\frac{N_{total}}{\mathbf{N.BGN}} + \sqrt{\left(\ln\frac{N_{total}(x,y)}{\mathbf{N.BGN}}\right)^2 + \mathbf{CON.BGN}}\right]\right\} \quad (11)$$

The **V.BGN, N.BGN, and CON.BGN** are constant parameters that can be adjusted from their default values.

2-3-2 Carrier mobility in bulk

By definition, mobility is a measure of average velocity of free carriers in the presence of an impressed electric field. In the presence of an electric field in a semiconductor, the free electrons and holes are accelerated in opposite directions [23]. As the free carriers are transported along the direction of the electric field, their velocity increases until they undergo scattering. In the bulk, the scattering can occur by either interaction with lattice or at ionized

donor and acceptor atoms. In analyzing the influence of the preceding parameters on the mobility, one assumes the electric field strength to be small. The mobility is then defined as the proportionality constant relating the average carrier velocity to the electric field. At high electric field such as those commonly encountered in power devices the velocity is no longer found to increase in proportion to the electric field and in fact attains a saturation value [11]. Since the free-carrier mobility depend strongly on the magnitude of the mobility model on MEDICI consists of low field and high field mobility components. These effects have important implications to current flow in power devices. So the accurate I-V model is strongly based on physical and accurate mobility and velocity saturation models [26].

Low Field Mobility

At low electric fields the electron velocity increases almost linearly with field and the mobility has the constant value μ_0. The low-field mobility is a function of the doping concentration and the temperature. A widely used empirical expression given by Caughey-Thomas equation for modeling the doping dependence of the low-field mobility has been proposed [25].

$$\mu_0 = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N}{N_{ref}} \right)^{\alpha}} \tag{12}$$

where N is the total doping concentration, and μ_{min}, μ_{max}, N_{ref} ,and α are fitting parameters. The parameter μ_{max} in (12) represents the mobility of undoped or unintentionally doped samples, where lattice scattering is the main scattering mechanism, while μ_{min} is the mobility in highly doped material, where impurity scattering is dominant [18]. And N_{ref} is the doping concentration at which the mobility is halfway between μ_{min} and μ_{max} , and α is a measure of how quickly the mobility changes from μ_{min} to μ_{max} .For modeling the

low-field mobility of 4H-SiC at room temperature. Equation (12) has been used. Several sources of experimental data were available for good fitting. Fig. 2.1 shows the experimental low-field mobility fit for 4H-SiC, which the following parameters were determined shown in Table 2.1

High Field Mobility

When strong electric fields are applied, the electron velocity is no longer proportional to the field, and can thus no longer be described by a field independent mobility. An expression frequently used for modeling the field dependence of the mobility in Si is [25]

$$\mu = \frac{\mu_0}{\left(1+\left(\frac{\mu_0 \times E}{v_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \qquad (13)$$

where μ_0 is the low field mobility described in (12) v_{sat} is the saturation velocity, and β is a constant specifying how abruptly the velocity goes into saturation. To obtain the velocity-field characteristics, both sides of (13) have to be multiplied by the electric field. Only little is known about the high-field mobility of SiC. For 4H-SiC the only experimental data on this comes from Khan and Cooper [26], where the drift velocity in epitaxial 4H-SiC (n-doped to about $10^{17}cm^{-3}$) was measured as a function of the applied electric field. A fit of equation (13) through the experimental high field data by Khan and Cooper is shown in Fig. 2.2, and the μ_0, v_{sat}, and β parameter values at 300K are 450 cm^2/Vs, $2.2x10^7cm/s$, and 1.2 respectively.

2-3-3 Channel mobility model

SiC is a viable semiconductor for high-power device applications due to its superior material properties. Although several MOS-based high-voltage devices have been demonstrated, most of them suffer from large on-state resistance due to poor inversion-layer mobility, attributed to a large interface state density at the interface [19]. The use of accumulation-mode MOSFETs was suggested to circumvent the poor inversion-layer mobility problem because a larger accumulation-layer mobility is expected compared to inversion-layer mobility as seen in Si MOS technology [22]. Extracted parametric mobilities and threshold voltage are shown for inversion and accumulation mode MOSFETS on both 4H-SiC and 6H-SiC in Fig. 2.3

Medici also incorporates an empirical model that combines mobility expressions for semiconductor-insulator interfaces and for bulk silicon. The basic equation is given by Mathiessen's rule [27]:

$$\mu_s = \left[\frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} \right]^{-1} \tag{14}$$

where

μ_s is total electron or hole mobility accounting for surface effects.

μ_{ac} is the carrier mobility limited by lattice scattering (surface acoustic phonons).

μ_b is mobility in bulk silicon.

μ_{sr} is mobility degraded by surface roughness scattering.

Where μ_b is the carrier mobility in bulk of the semiconductor, μ_{ac} is the carrier mobility limited by lattice scattering (surface acoustic phonons), and μ_{sr} is the carrier mobility limited by surface roughness scattering. In this model, the contributions of various scattering mechanisms are separated, thus offering advantages in terms of initial estimation of

the model parameters, needed for any curve fitting, as well as convenience for including more scattering mechanisms without altering the model structure itself. At low normal electric fields, the carrier mobility in a semiconductor is a function of the total doping concentration and the temperature. The bulk or low field mobility, μ_b, was modeled using the empirical model proposed by Caughey-Thomas as mention above (12). The acoustic-phonon term, used in MEDICI simulator, has the following form [2]:

$$\mu_{ac} = \frac{\mathbf{B}}{E_{\perp}} + \frac{\mathbf{C}N_{total}^{\alpha l}}{T^{3}\sqrt{E_{\perp}}} \tag{15}$$

There are two fitting parameters, **B** and **C**, allowing adjustment of the strengths of the effects due to parallel electric field and temperature, respectively.

Surface roughness is known to cause severe degradation of the surface mobility at high electric fields. The electron mobility term due to the surface-roughness scattering is frequently expressed in the following way:

$$\mu_{sr} = \left(\frac{\mathbf{D}}{E_{\perp}^{2}} \right) \tag{16}$$

Where **D** is the fitting parameter.

The surface-mobility parameters have not been studied for 4H SiC because of the erratic behavior of the inversion layer mobility in the case of MOSFETs with ordinary dry or wet oxides. However, recently made MOSFETs with nitrided gate oxides exhibit not only significantly increased mobility, but also mobility behavior that is similar to the case of Si MOSFETs. This indicates that it is possible to use the existing mobility models by setting the parameter values. MEDICI two-dimensional device simulation program was used to

determine the surface-mobility parameters. Two-dimensional impurity profile was generated using the same parameters as the experimental test MOSFET and material parameters for 4H SiC. Lombardi surface mobility model, available in MEDICI, was used as the combination of low field and transverse field effects. The complete list of parameter value, providing the good fit shown in Fig. 2.4, is listed in Table 2.2.

2-4 Impact ionization

Impact ionization, punch through mechanism, and oxide breakdown due to high electric stress are the major factors for determining the maximum voltage that a device can stand. Impact ionization results in the generation of electron-hole pairs during the transport of the mobile carriers through the depletion layer. To characterize this process, it is useful to define the ionization coefficients [20]. The probability that electrons or holes create electron-hole pairs is given by the product of a proportionality factor α（called impact ionization rate）and the electron/hole concentration. The maximum E_B and the blocking capability V_B is determined by the impact-ionization rate for electron-hole pairs. In the forward blocking mode, the gate electrode of the power MOSFET is externally short-circuited to the source. Under these conditions, no channel forms under the gate at the surface of the P-base region. Thus impact ionization coefficient rates are the key parameters that have to estimate accurately to get reliable prediction of the device blocking performance. In ordered to obtain the critical electric field as function of doping, we had to solve the integral equation (17)

$$\int_0^w \alpha_p \exp\left(\int_0^x (\alpha_n - \alpha_p)dx\right)dx = 1 \tag{17}$$

numerically. For the avalanche generation rates α the same model used for Si was taken [9]:

$$\alpha_{n,p} = a_{n,p} \exp\left(-\frac{b_{n,p}}{|E|} \right) \tag{18}$$

$\alpha_{n,p}$ are the electron and hole ionization rates that are defined as the generated electron-hole pairs per unit length of travel by per electron and hole. It is not importance whether the ionization integral for the holes or the electrons is calculated since both reach unity at V=V_B. Therefore, the kind of dopants (N or P) in the space charge region is not important. It was determined that the coefficient a_p in 4H-SiC has a value of $(3.25 \pm 0.3) \times 10^6 \, {}^{1}\!/\!_{cm}$ at room temperature and b_p has a value $(1.79 \pm 0.04) \times 10^7 \, {}^{V}\!/\!_{cm}$ at room temperature from Fig. 2.5 .

2-5 Summary

MEDICI simulations are able to obtain the breakdown voltage using the obtained ionization coefficients. However, in real devices, tunneling may take place before avalanche breakdown at high doping levels. Normally breakdown occurs at edges of the space charge region or at the surface prior than in the bulk. And in this chapter, the important material parameter set for 4H-SiC device simulation in MEDICI 2D-simulation program has been complied from literature data.

Chapter 3

SiC Power MOSFET

The physics of the operation of power MOSFETs is simpler than that for other power devices because of the absence of minority carrier injection. However, it is necessary to understand the interaction between the cell geometry and the devices characteristics before taking an accurate device design. In the following, the on-state characteristics are first treated followed by analysis of the blocking characteristics.

3-1 On-resistance

The on-resistance is an important device parameter because it determines the maximum current rating. The on-resistance of a power MOSFET is the total resistance between the source and drain terminals in the on-state. The specific on-resistance of silicon carbide power MOSFET's have been projected to be far superior to their silicon counterparts due to the high breakdown field strength of SiC. The power dissipation in the power MOSFET during current conduction is given by [7]:

$$P_D = I_D{}^2 Ron \tag{1}$$

$$\frac{P_D}{A} = J_D{}^2 R_{on,sp} \tag{2}$$

where $(\frac{P_D}{A})$ is the power dissipation per unit area; J_D is the on-state current density and

$R_{on,sp}$ is the specific on-resistance, defined as the on-resisitance per unit area. These expressions are based upon the assumption that the power MOSFET is operated in its linear region at a relatively small drain bias during current conduction. The maximum power dissipation per unit area is determined by maximum allowable junction temperature and the thermal impedence. The specific on-reisitance of the power MOSFET is determined by the resistance component for the DMOS structure. Fig. 3.1 shows a cross section of a power DMOS MOSFETs structure.

$$R_{on,sp} = R_{n^+} + R_C + R_A + R_J + R_D + R_S \tag{3}$$

Where R_{n^+} is the contribution from the N^+ source diffusion. R_C is the channel resistance, R_A is the accumulation layer resistance, R_J is the resistance from the drift region between the p-base region due to JFET pinch-off action, R_D is the drift region resistance and R_S is the substrate resistance. In a power MOSFET, blocking voltage is supported across the drift layer and thus, drift-region resistance is considered to be minimum possible theoretical limit for the on-resistance of a MOSFET. This assumption is not accurate at lower breakdown voltages where the drift-region resistance R_D is compariable to other resistive components and these resistances should also be included in calculating $R_{on,sp}$. However, at higher breakdown voltage, R_D is significantly higher than other resistances and $R_{on,sp}$. could be approximately by R_D. The specific on-resistance of the power MOSFET will then be determined by the drift region alone. Thus:

$$R_{on-sp} = R_{on-drift} \tag{4}$$

3-2 The analysis of blocking voltage

The drift region analysis can be performed to express the relation between the specific on-resistance (R_{on}) and the blocking voltage capability (V_B) of a MOSFET. By approximating the depletion layer in the drift region as an abrupt one-dimension junction, and it is uniform doped ; the doping level $N_B(cm^{-3})$ required to supported a given breakdown voltage V_B and depletion width W (cm) at breakdown can be calculated as follows [7]:

$$N_B = \frac{\varepsilon \cdot E_B^{\,2}}{2 \cdot q \cdot V_B} \tag{5}$$

$$W = \frac{2V_B}{E_B} \tag{6}$$

where V_B is the breakdown voltage. The ideal specific on resistance is the resistance per unit area of this layer of material required to support the voltage. Using the above doping and thickness, this given by

$$R_{on,sp\,(ideal)} = \frac{W}{q \cdot N_B \cdot \mu} = \frac{4V_B^{\,2}}{\varepsilon \cdot \mu \cdot E_B^{\,3}} \tag{7}$$

Thus, the ideal specific on-resistance decreases inversely proportional to the mobility and as the cube of the breakdown electric field strength. The denominator ($\varepsilon \cdot \mu \cdot E_B^{\,3}$) in Eq. (7) has been referred to as Baliga's figure of merit (BFOM) for unipolar power devices. In 1983, Baliga drived a figure of merit

$$\text{BFOM} = \varepsilon \cdot \mu \cdot E_B^{\,3} \tag{8}$$

which defines material parameters to minimize the conduction losses in power MOSFET's. Here μ is the mobility and E_B is the critical electric field of the semiconductor. The BFOM is based upon the assumption that the power losses are solely due to the power dissipation in

the on-state by current flow through the on-resistance of the power MOSFETs.

3-3 Material advantages of 4H-SiC for power devices

By using the known material properties of semiconductors, it is possible to select those that will exhibit a lower ideal specific on-resistance when compared with silicon by using this expression It has been found that most promising semiconductor are gallium arsenide, whose Baliga's figure of merit is 12.7 times larger than silicon, and silicon carbide whose Baliga's figure of merit is 200 times larger than silicon. Although some research has been performed on the fabrication of vertical power MOSFET's from gallium arsenide, this material has been found to be difficult to work with due to dissociation of the compound during processing. In contrast, silicon carbide offers a such larger improvement in ideal specific on-resistance and is stable even at extremely temperatures.

In the case of Si, the extract dependency of the electron mobility and the breakdown field on the doping concentration is known [23]

$$\mu_n = \frac{5.10\times10^{18} + 92N_B^{0.91}}{3.75\times10^{15} + N_B^{0.91}} \tag{9}$$

Based on this known dependence of μ_n and E_B on the doping concentration for Si power MOSFET's, a closed form analysis which requires the solution of ionization integral, using an abrupt junction diode, is used for calculating expressions for N_B and

W for a Si power MOSFET are obtain as [17]

$$N_B = 2.01\times10^{18} V_B^{-3/4} \tag{10}$$

$$W = 2.58\times10^{-6} V_B^{-7/6} \tag{11}$$

$$R_{on-sp} = 5.93\times10^{-9} V_B^{2.5} \tag{12}$$

the dependency of the breakdown field strength of 4H-SiC and 6H-SiC on N_B was determined from the calculated values from [17,9]. The empirical relationship between E_B and V_B on N_B was obtained as

$$V_B^{6H-SiC} = 6.3\times10^{14} N_D^{-5/7} \tag{13}$$

$$V_B^{4H-SiC} = 7.5\times10^{14} N_D^{-5/7} \tag{14}$$

$$E_B^{6H-SiC} = 1.52\times10^{4} N_D^{1/7} \tag{15}$$

$$E_B^{4H-SiC} = 1.64\times10^{4} N_D^{1/7} \tag{16}$$

Table 2.1 provides of N_B, W, μ_n, and $R_{on,sp}$ of an ideal DMOS as a function of breakdown voltage for Si and SiC power MOSFET's. This analysis suggests that 4H-SiC MOSFET would have lower R_{on} than 6H-SiC. For a given breakdown voltage, R_{on} for the SiC MOSFET is at least two orders of magnitude smaller than for Si MOSFET, and the ratio of R_{on} of the Si MOSFET to that of SiC MOSFET increases with increasing breakdown voltage. Due to the excellent characteristics of SiC, it would be desirable to utilize power MOSFET for high voltage power applications. Unfortunately, the specific on-resistance of the drift region increases very rapidly with increasing breakdown voltage because of the need to reduce its doping concentration and increase its thickness [4]. Thus, in spite of the ability to obtain nearly ideal specific on-resistance with silicon power MOSFET structures, they are not

satisfactory for applications that require breakdown voltages above 300V due to their high on-state power dissipation. So, many reasons make SiC an attractive candidate for fabricating power devices.

3-4 Summary

The superiority of 4H-SiC illustrated in this chapter is just one of the potential projections in using this wide semiconductor material for high power devices. These advantages in terms of calculated figure of merits provide a motivation for the design and development of power devices on SiC. Despite the unique problems in device fabrication, which many are not yet totally resolved, promising progress in the device development has taken place in the area of power MOSFETs.

Chapter 4

The electrical performance of SiC MOSFET

Silicon-based switching devices have reached the theoretical limitations for high power and for high power and high temperature applications whereas silicon carbide (SiC) has emerged as an alternate material system to overcome the limitations and can be used in extreme environment.

4-1 Introduction

Since SiC is a attractive semiconductor materials for high-power electric devices because they have excellent physical properties such as a wide bandgap, high breakdown voltage, and high saturation electron drift velocity. However, due to higher layer mobility as compared to inversion layer mobility, ACCUFETs emerge as the preferred solution for power MOSFETs on SiC [24]. Channel mobility of power MOSFET's is one of the most important parameters that determines the on-resistance in the conducting state. More work need to be done to reduce the specific on-resistance and increase the blocking voltage capability in SiC power MOSFEET. The emergence of ACCUFET structures in SiC reveals important advantages in terms of higher channel-carrier mobility [6]. The ACCUFETs structure shows a much promising result in terms of their specific on-resistance compared to the inversion power MOSFET. The main focus in this chapter based on the introduction of design of accumulation-mode power MOSFETs and its optimization using MEDICI two-dimensional device simulator [1].

It should be noted, however, that the contribution and the conclusions in this thesis do

not rely on quantitative results. The methodology used in this paper focuses on the merits of the devices structure itself, independent of the specific parameter values, which are still dominated by different technology imperfections.

4.2. The trench and planar ACCUFET

4-2-1 The trench ACCUFET

Many researchers focus their attention on the SiC MOSFET designed using trench technology, since it offers high channel density and eliminates JFET effect characteristic of DMOS structure. In spite of their advantages, the trench MOSFET have several drawbacks such as high threshold voltage and poor mobility in the channel, which is adversely affects the on-state resistance. Another serve drawback of the trench MOSFET is the gate oxide breakdown, which can occur in off state, under high electric field [8,16].

As it was mentioned earlier, the strongest limitations of SiC trench MOSFET are the dielectric breakdown can occur before semiconductor breakdown. Writing the Gaussian low in the SiC-SiO_2 interface

$$\varepsilon_{SiC} E_{SiC} = \varepsilon_{SiO_2} E_{SiO_2} \quad (1)$$

Considering the ration of dielectric constant of SiC/ SiO_2 (9.7/3.9) and $E_{SiC\text{-}BR}$ is 3MV/cm ,it is found that the maximum allowable of electric field in the oxide is 7.46×10^6V/cm. However, due to two-dimensional simulations at the trench corner, the value in the oxide can be higher

than $7x10^6$ V/cm without encountering semiconductor breakdown. Nevertheless, in ordered to have a reliable device, the oxide electric field should be kept under it practical value of $7x10^6$ V/cm.

The simulations of breakdown structure have been shown in the Fig 4.1, drift thickness and concentration are 10 μm and $1x10^{16}cm^{-3}$ respectively, channel length of 2.0 μm, an N^+ polysilicon gate electrode over an 100nm thick gate oxide (Q_F=$1x10^{11}$ cm^{-2}), an N^+ region concentration of $1x10^{20}$ cm^{-3}. It has been found that, for a breakdown voltage of 980V, the electric field at the trench corner has the value of $7.8x10^6$ V/cm, consider the theoretical value calculated earlier, it is clear that the device will breakdown because of oxide rupture. To improve this problem, try to wide the trench and round the corner. Because in this way, the curvature of potential lines at the trench corner would be soften [10].

In Table 4.1 the value of electric field as a function of the trench width, for rectangular and rounded corners and a t_{ox} of 0.1 μm, breakdown voltage of 980V are simulated. As a consequence, by using wide trench in conjunction with rounded trench corners, the electric field in the oxide corner can be kept in the critical value. The influence of gate oxide thickness upon the breakdown voltage has also been investigated. For the rounded trench MOSFETS , breakdown simulation has been carried out, for different oxide thickness and trench width. The simulation results are shown in Table 4.2.

From the results shown in Table 4.2, it can be inferred that there is an inverse proportionality relationship between the oxide thickness and breakdown voltage. Although the simulator does not taken into account the oxide breakdown, we can state that above $7.46x10^6$ V/cm the device breakdown through the avalanche tunneling gate oxide.

4-2-2 The planar ACCUFET

In silicon, a double-diffused MOSFET (DMOSFET) is the most common structure used for fabricating power MOSFETs [12]. The DIMOS/DMOS structure offers high reliability, ease of integration with ICs and simplicity of fabrication because the gate oxide is shielded from the high electric fields by the adjacent p-type base regions. The cross section of the ACCUFET structure is shown in Fig. 4.2 the n-drift region doping and thickness have been designed to support a high voltage, the entire device is expected to have a high blocking voltage, and since the ACCUFET is a planar device, it does not suffer from any enhanced electric fields, unlike the UMOSFET. In this structure, a thin n-type region is formed below the MOS gate by using a buried p implanted layer. The thickness and doping of this n layer is carefully chosen such that it is completely depleted by the built in potentials of the p /n junction and the MOS gate at zero bias, resulting in a normally-off To obtain reasonable reliability for a device, the electric field in the SiC must be restricted to below 3 MV/cm. The ACCUFET achieves this by suppressing the peak electric field from the surface between SiC and SiO_2, to below the p base region [5].

Two different P-base region spacing L_P designs were fabricated with different lengths observe the effect of this parameter on the performance of this device. From the simulations, it was found that the electric field near the interface of SiO_2 and SiC can be controlled by adjusting When L_P was reduced, When L_P was reduced, the region above it gets shielded from the high drain voltage thereby reducing the electric field near the oxide. The relationship between P-base spacing (L_P) and R_{on} also be simulated by MEDICI simulator. The dominant sources of on-resistance in an ACCUFET are [14]: the channel resistance of the accumulation layer; the “JFET resistance” between the adjacent P-base regions; and the drift resistance of

the low doped, voltage-blocking layer. The simulation results of Fig. 4.3 show that a distinct minimum exists for specific on-resistance as is changed from 1 μm to 6 μm. This is because a trade-off exists between the JFET region resistance and the channel resistance. An increase in results in an increase in unit cell pitch, which increases the channel resistance per unit area. On the other hand, as is reduced below 2.5 μm, a dramatic increase in the JFET region resistance occurs because of a reduced current carrying width between adjacent P-base regions [15].

4-3 The innovative SiC ACCUFET

The cross section of the proposed structure is shown in Fig. 4.4 In this structure, a thin N-type region is formed below the MOS gate by using a buried P implanted layer. The thickness and doping of this N-layer is carefully chosen such that it is completely depleted by the built-in potentials of the P+/ N- junction and the MOS gate at zero gate bias, resulting in a normally-off device with the entire drain voltage supported by the P+/N-drift junction. Since this P+/ N- junction can support high voltages. When a positive gate bias is applied, an accumulation channel (of electrons) is created at the interface between SiO2 and SiC. This results in a low resistance path for the electron **c**urrent flow from the source through the channel, then down to the drain through the drift region to the drain. Assuming that the higher accumulation layer mobility (as compared to the inversion layer mobility) observed in silicon applies to silicon carbide also, a lower on-resistance is expected for the device, which will be referred to as the planar ACCUFET. The main feature of this accumulation type MOSFET is the N-type channel, epitaxially grown on P-base region. Two-dimensional numerical simulations were done using MEDICI with parameters taken from [28] for the ACCUFET structure.

4-4 Analysis and optimization of device parameters

In the following, we will discuss the relationship blocking and driving capability of this structure upon these parameters including, the doping concentration and thickness of P-base layer, and the peak doping concentration of ion-implanted trench region. Two-dimensional numerical simulation structure (including the mesh, the boundaries, and the impurity profiles) for the device was generated in MEDICI. Due to the symmetry of the devices, only half of the device structure was simulated. The structure has a fixed 10 μm N-drift region at $1x10^{17}cm^{-3}$, an N^+ type polysilicon gate electrode with an 100nm thick oxide($Q_F=1.0x10^{11}cm^{-2}$) , a channel length of 2.0 μm. The simulation results were used to calculate Baliga's Figure of Merit (BFOM) as the criterion for structure optimization and comparison.

Peak trench region concentration

We choose the peak concentration of ion-implanted trench region has to be set higher than the P-base concentration (N_A). The two P-base concentration $1.1x10^{17}$ cm^{-3}, $1.6x10^{17}$ $cm^{-3}$of 2 μm thick p-base thick epilayer, were selected. The peak trench concentration of ion-implanted region was varied from $1.15x10^{17}$ cm^{-3} to $1.6x10^{17}$ cm^{-3} for $N_A = 1.1x10^{17}cm^{-3}$, from $1.65x10^{17}cm^{-3}$ to $2.1x10^{17}$ cm^{-3} for $N_A=1.6x10^{17}$ cm^{-3}.

The simulation results were shown in Fig. 4.5, Fig. 4.6 the maximum blocking voltage was 1780V with $N_A=1.1x10^{17}$ cm^{-3} with a slightly higher peak trench region concentration of $1.15x10^{17}$ cm^{-3}. The maximum operating voltage in this region is determined by the dielectric breakdown before the semiconductor breakdown. When $N_A=1.6x10^{17}$ cm^{-3}, avalanche breakdown occurring in the trench region determines the blocking capability of the device.

From the results, to obtain the maximum operating voltage of the device, also thinking about figure of merit for power devices that is used to optimize the considered parameters. The best trade-off between the breakdown voltage and on-resistance in terms of BFOM is achieved with peak trench region concentration $1.45x10^{17}cm^{-3}$for $N_A=1.1x10^{17}cm^{-3}$

.

P-base layer thickness

The simulation results of p-base thickness upon blocking voltage, on-resistance are shown in Fig. 4.7.In this simulations, the optimum values of the parameter considered in the previous simulation with peak trench region concentration $1.45x10^{17}cm^{-3}$ for $N_A=1.1x10^{17}cm^{-3}$. As shown in Fig. 4.7, the P-base thickness play an important role on Blocking voltage. The simulation results shows that the p-base epilayer thickness of 2 μm is the optimum value in terms of BFOM. Furthermore, we use the same models and parameters in the MEDICI device simulator to obtain and compare the performance characteristics of the structures mention above with innovative ACCUFET. These structures set to have a drift region thickness and concentration 10 μm and $1.1x10^{17}cm^{-3}$, respectively, channel length of 2.0 μm, an N+-type polysilicon gate electrode over an 100nm thick gate oxide($Q_F=1.1x10^{11}$ cm^{-2}) , an N+ region concentration of $1.0x10^{17}cm^{-3}$, and a Gaussian doping profile with characteristic width of 0.15 μm. The results of simulation are shown as for Table 4.3.The results show clearly that the innovative ACCUFET structure enables a better performance than the trench and planar structure.

4-5 Summary

Power devices made with silicon carbide (SiC) are expected show great performance advantages as compared to those made with other semiconductor. Therefore, conventional SiC

MOSFETS suffer high specific on-resistance due to low channel mobility.

The innovative structure of accumulation mode MOSFET for high power applications has been proposed and analyzed in MEDICI. The peak concentration of the ion-implanted trench region strongly influences the breakdown voltage and on-resisitance of the device. To obtain the maximum operating voltage, the peak concentration of the ion-implanted trench region has to be slightly higher than the p-base epilayer. The thickness of p-base epilayer does not play an important role in on-resistance. How ever, it changes the maximum blocking voltage significantly. By using the MEDICI simulator, the best trade off between on-resistance and maximum blocking voltage by setting the thickness of p-base layer precisely. The electrical performances of trench and planar ACCUFET, are mainly limited by the oxide breakdown and p-well spacing.

Chapter 5 Conclusion

The analysis of 4H-SiC as compared to Si as a semiconductor material for power MOSFET has been shown in favor of 4H-SiC due to its superior material properties. An improvement of two-order magnitude in the specific on resistance of ideal 4H-SiC MOSFET over ideal Si MOSFET is projected. However, a review of the state of the art of SiC power MOSFETs indicates that the performance progress of SiC power devices have been hampered by MOS interface related issues which resulted in high channel resistance and oxide breakdown. Numerical device simulation-based optimization efforts for this novel device have been performed which resulted in optimum device with blocking voltage more than 1.2kV.

Parameter extraction for numerical device simulation of 4H-SiC unipolar devices is the first major topic developed in this thesis. Using 2D numerical device simulation MEDICI , in the models describing electronic devices, the material parameters of Si are replaced by respective parameters of 4H-SiC reported in literature. Using the MEDICI two-dimension simulator, with already existing models to design and optimization of 4H-SiC MOSFETs.

As the main objective of the MOS device research is to bring the channel mobilities in SiC MOS devices as high as the bulk mobilities in SiC and improve reliability of SiO_2 layer. The future generation of SiC MOS based devices should the necessary quality dielectric layers and low defect between dielectric and semiconductor interface.

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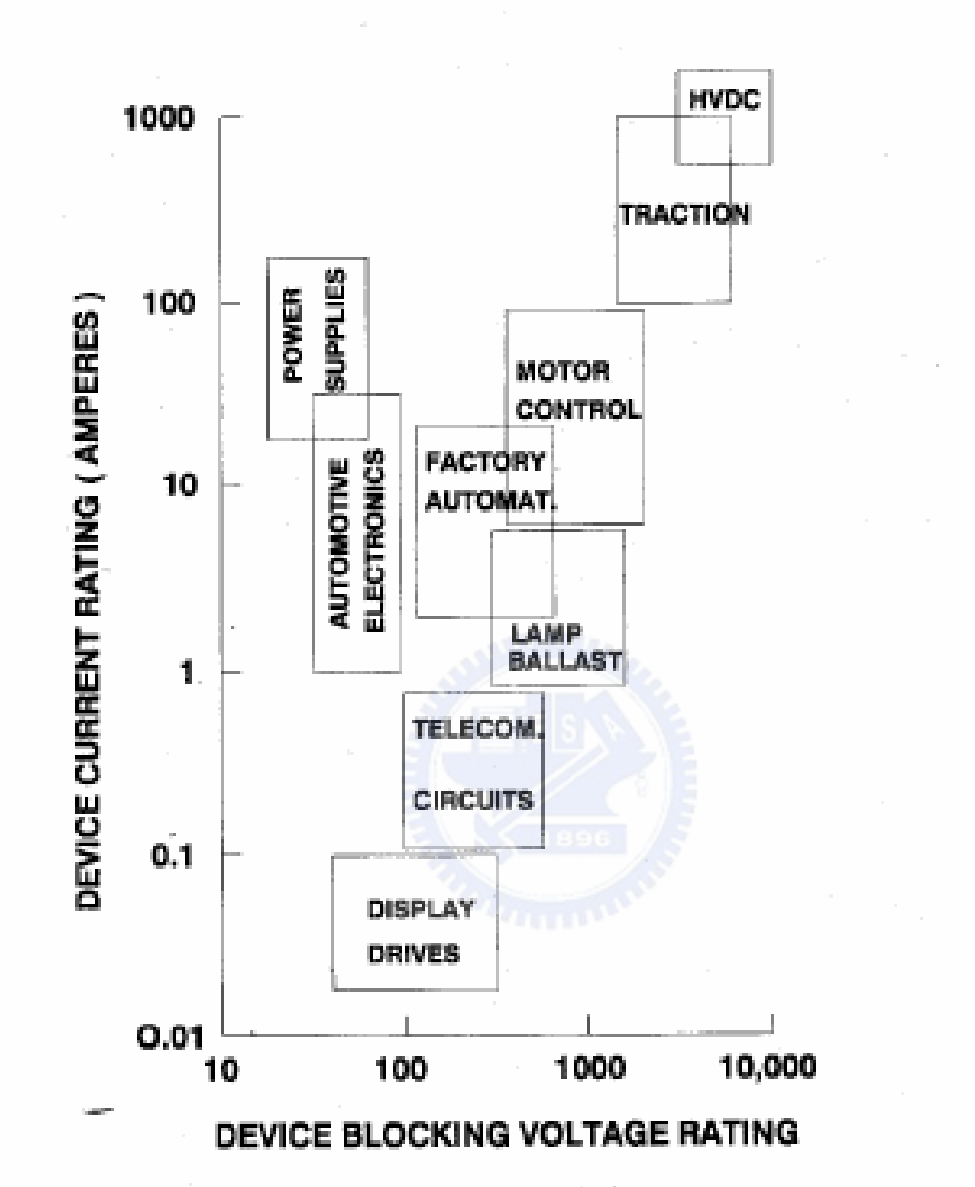


Fig.1.1 Applications for power devices in relation to their voltage and current ratings

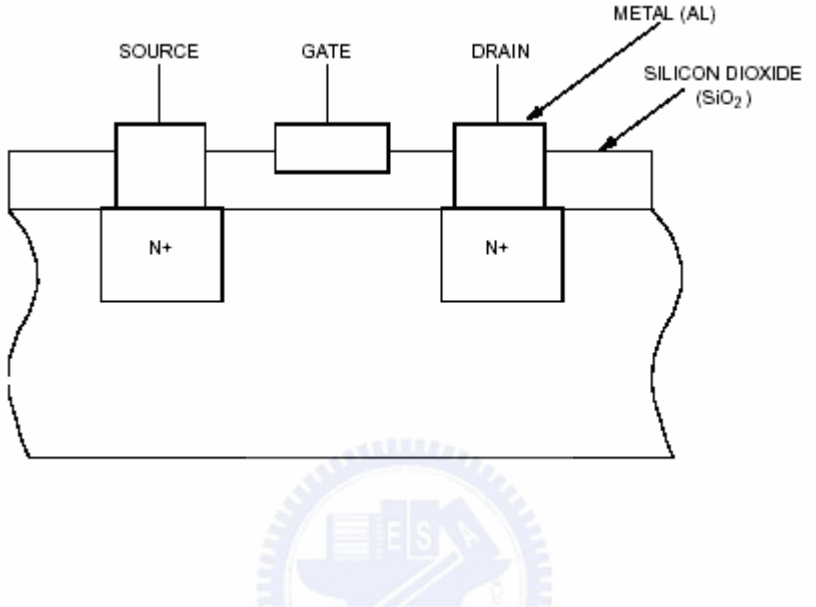
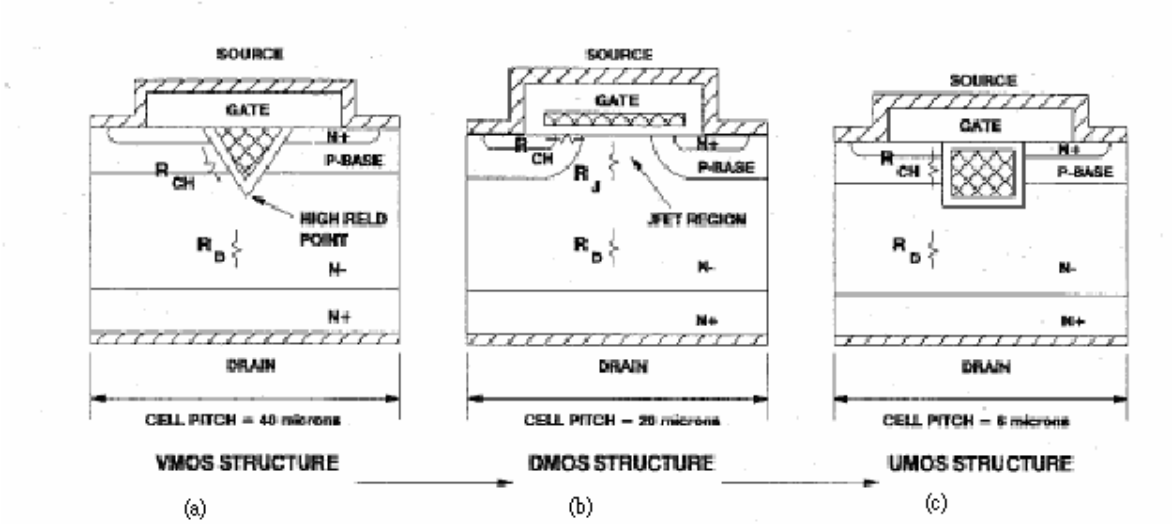


Fig.1.2 Lateral n-channel MOSFETs cross section.



Evolution of power MOSFET structures.

Fig. 1.3 The cross section of various power MOSFET structure

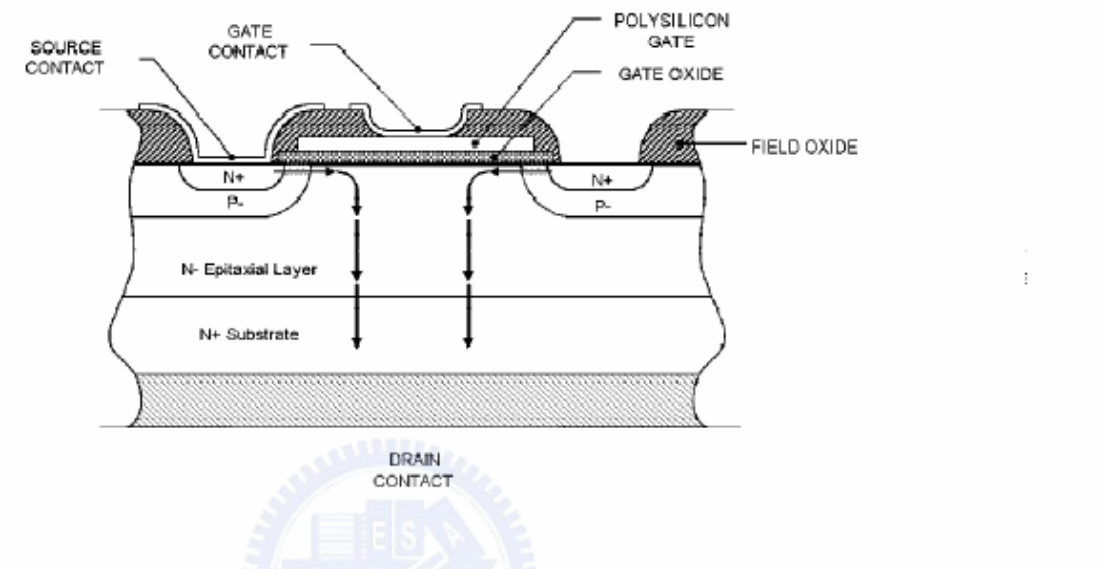


Fig.1.4 The operation of power DMOS

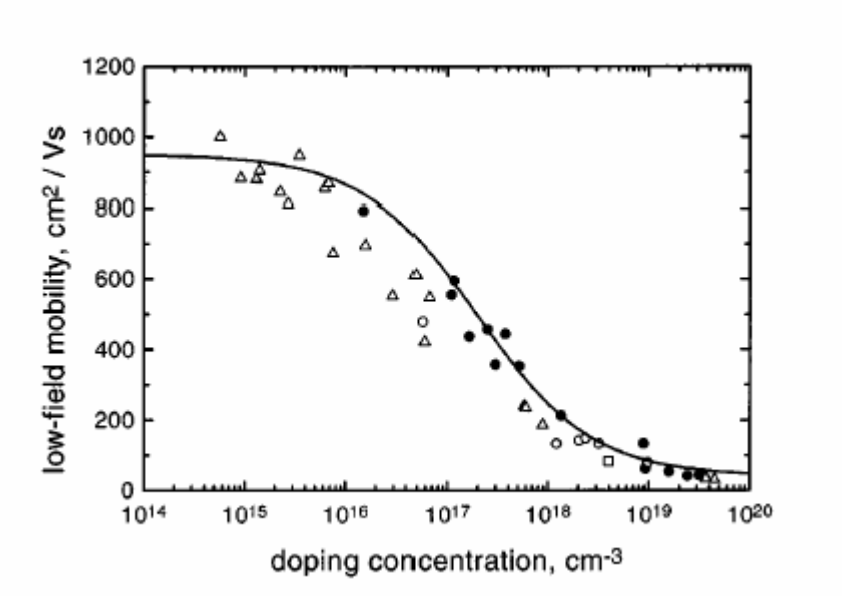


Fig. 2.1 Low-field electron mobility as a function of doping concentration in 4H-SiC (perpendicular to the c-axis, T = 300 K).

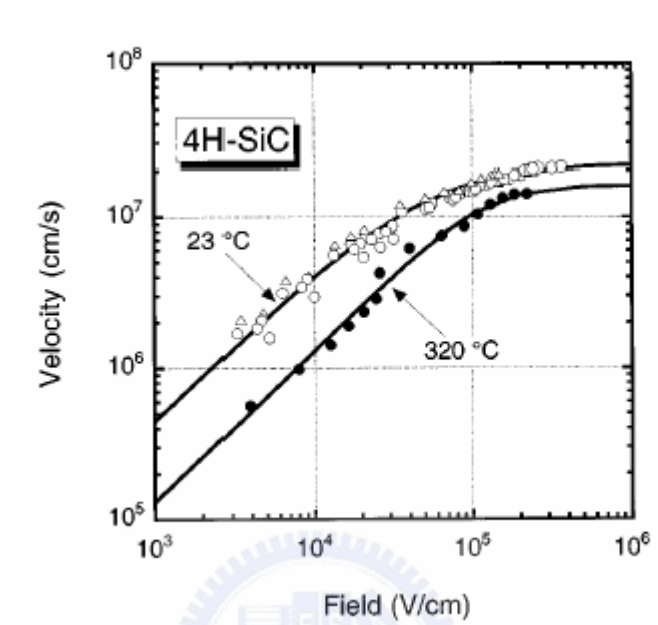


Fig. 2.2 Drift velocity of electron in 4H-SiC as functions of the applied field.

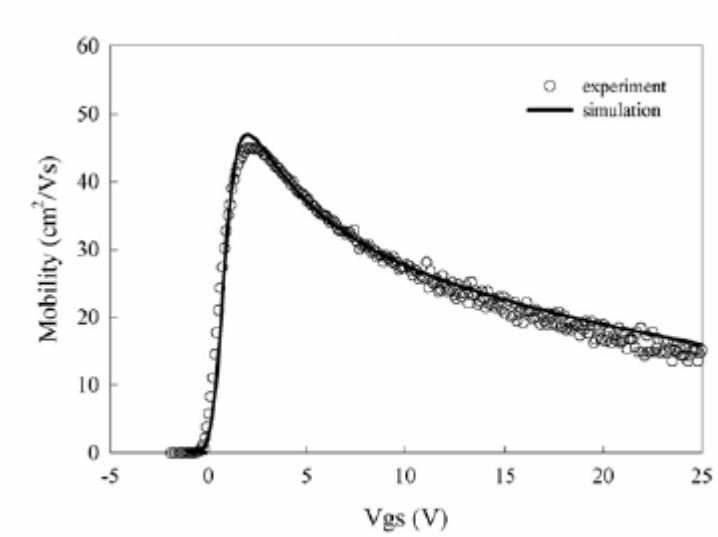


Fig. 2.3 Mobility between the experimental data and simulation with the parameter values listed in Table 2-2

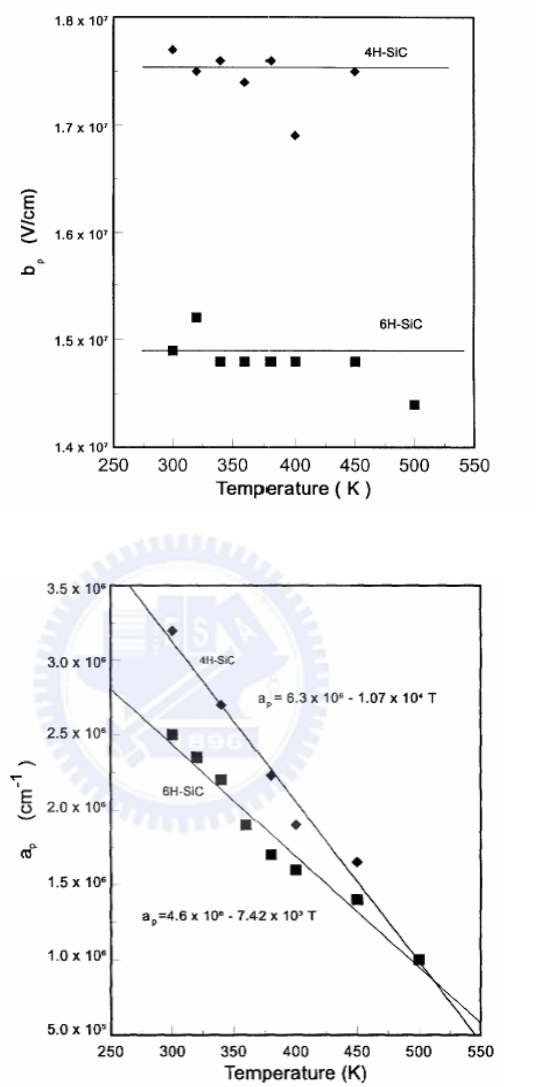


Fig. 2.4 Temperature dependence of the coefficients a_p and b_p for 4H-SiC

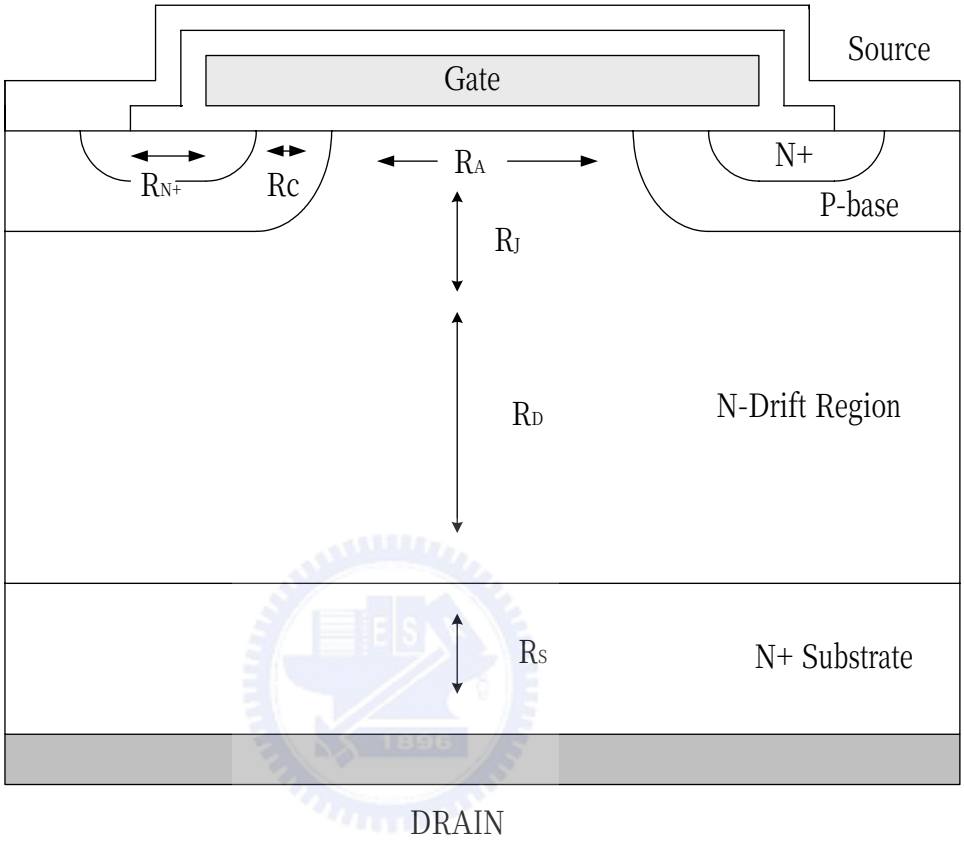


Fig. 3.1 A cross section of a power DMOS MOSFETs structure

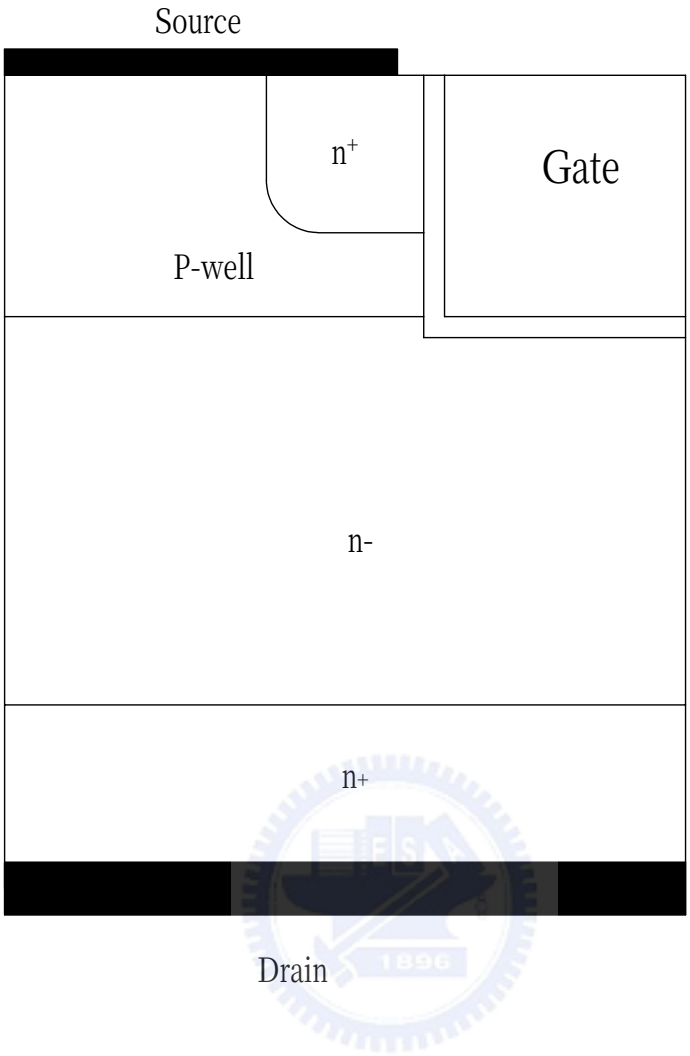


Fig. 4.1 The cross section of trench MOSFET

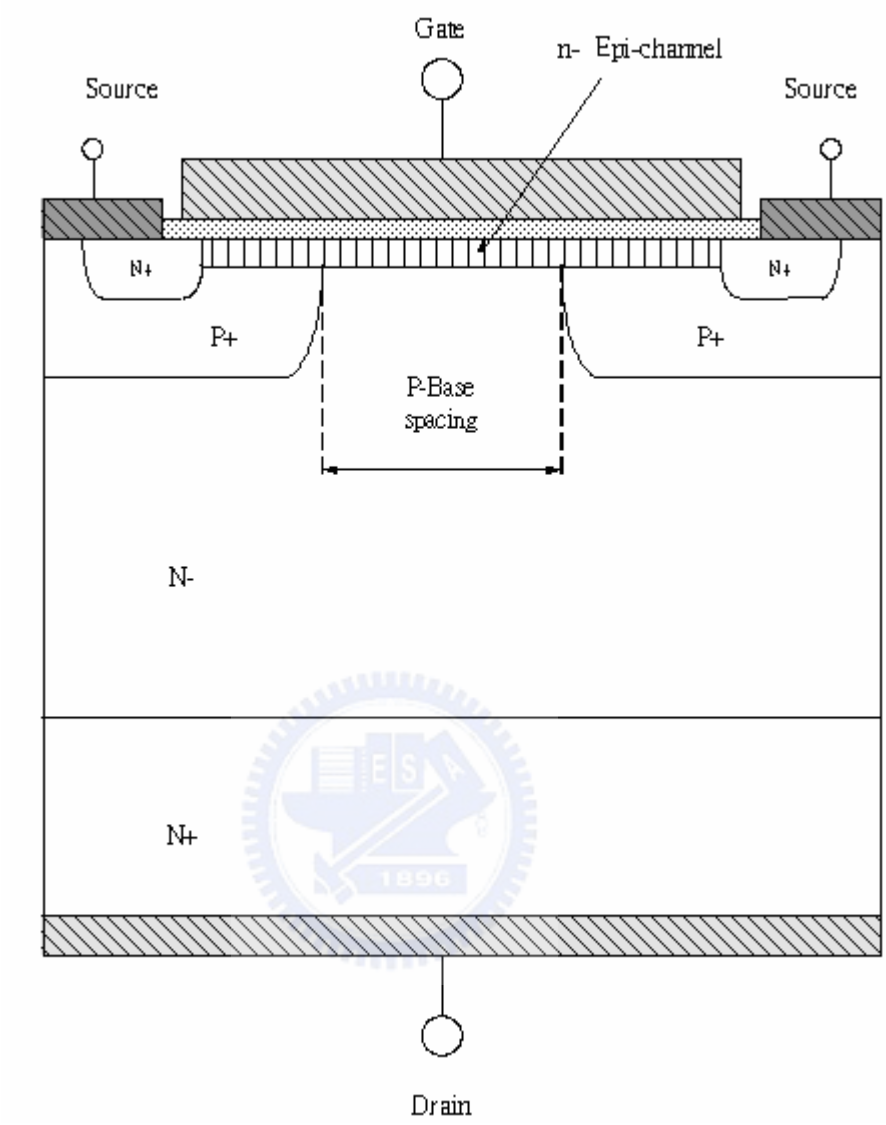


Fig. 4.2 The cross section of accumulation DMOS

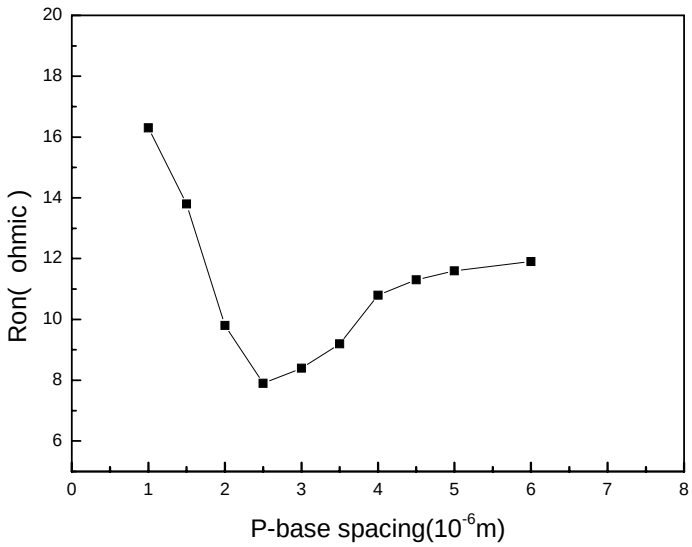


Fig. 4.3 The relationship between P-base spacing (L_P) and R_{on}

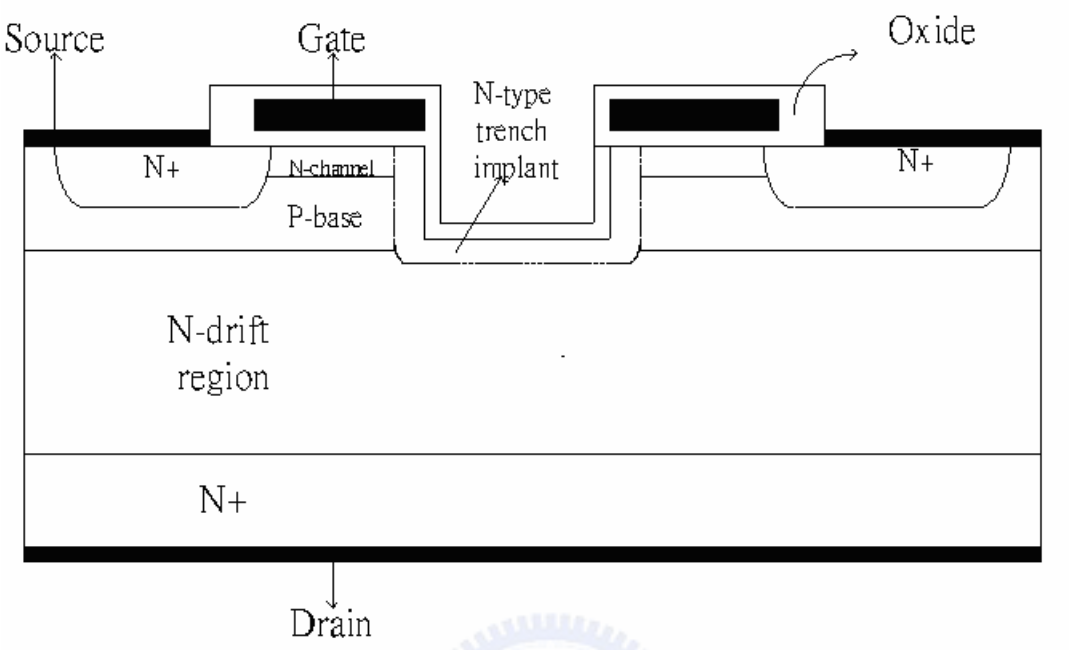


Fig. 4.4 The cross section of Innovative SiC ACCUFET

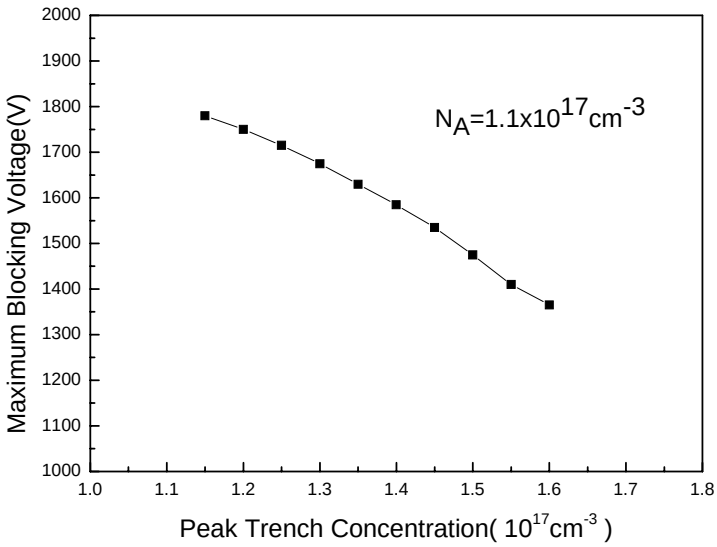


Fig. 4.5(a) Effect of peak trench-region concentration on maximum operating voltage.

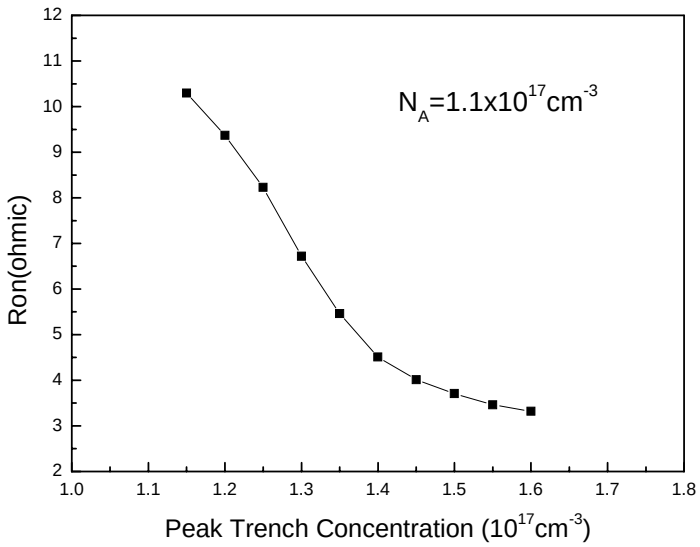


Fig. 4.5(b) Effect of peak trench-region concentration on Ron resistance

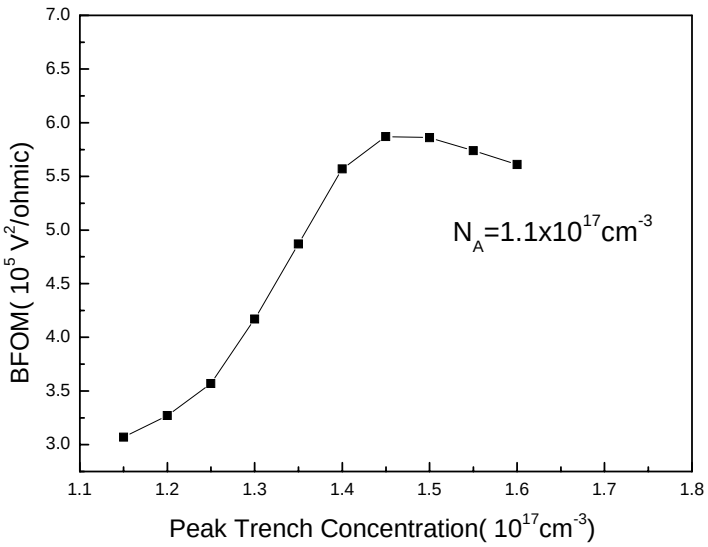


Fig. 4.5(c) Effect of peak trench-region concentration on BFOM

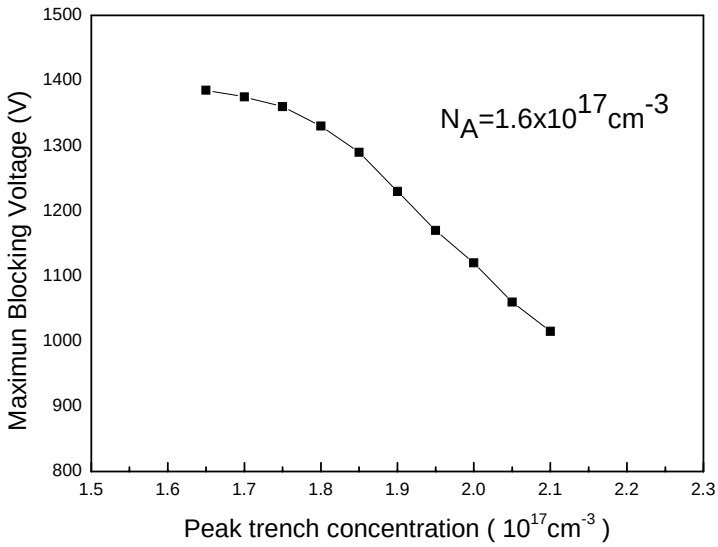


Fig. 4.6(a) Effect of peak trench-region concentration on maximum operating voltage.

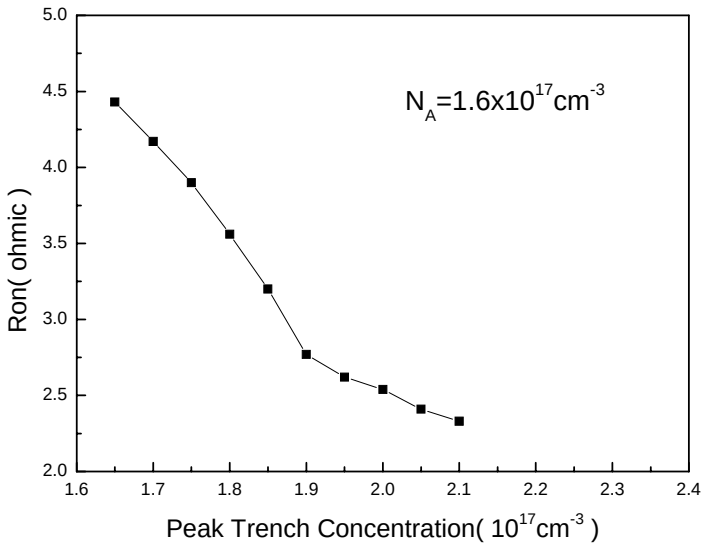


Fig. 4.6(b) Effect of peak trench-region concentration on Ron resistance.

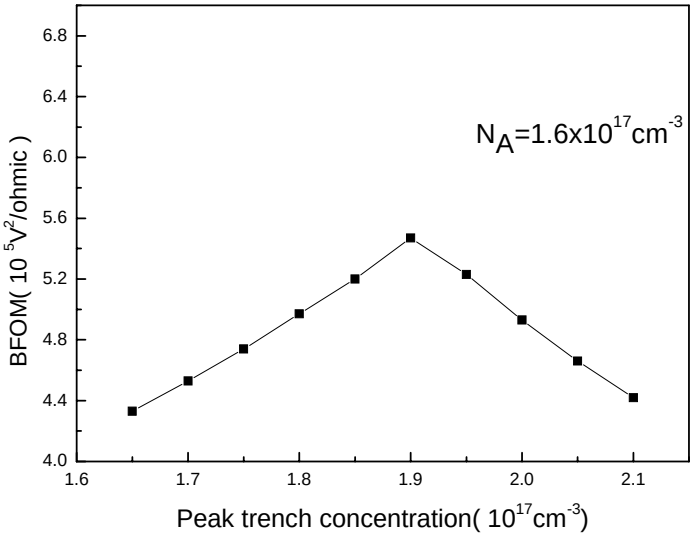


Fig. 4.6(c) Effect of peak trench-region concentration on BFOM.

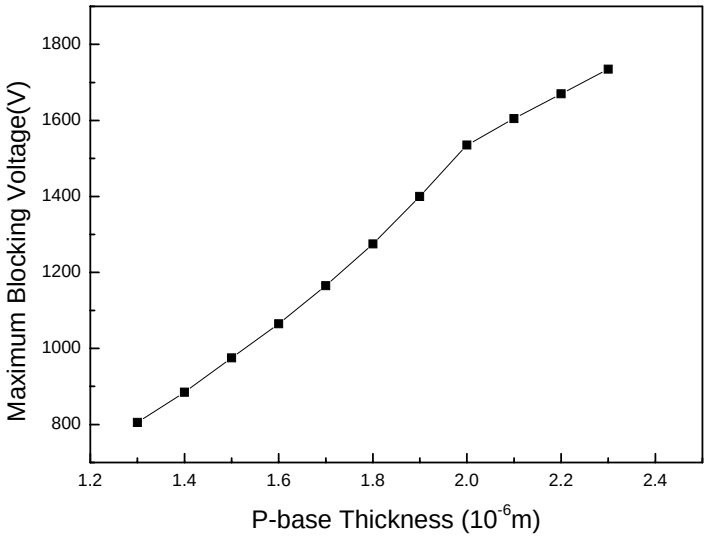


Fig. 4.7(a) Effects of P-base thickness on blocking voltage.

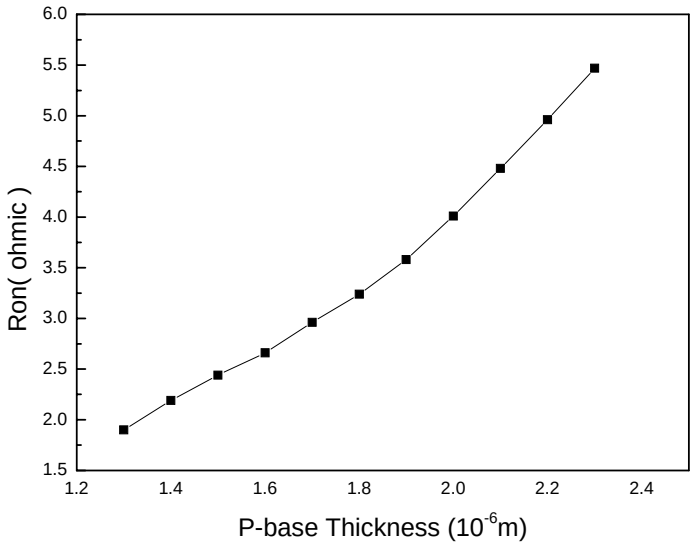


Fig. 4.7(b) Effects of P-base thickness on Ron resistance.

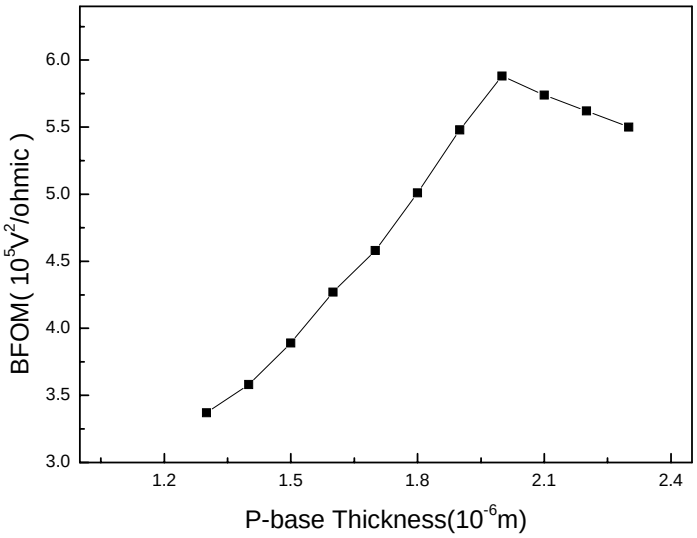


Fig. 4.7(c) Effects of P-base thickness on Ron resistance.

Table 1.1 Comparison of Si and SiC material properties

Properties	Si	6H-SiC	4H-SiC
Band gap (eV)	1.11	2.9	3.2
Dielectric constant	11.8	9.7	9.7
Breakdown field (V/cm)	$6x10^5$	$35x10^5$	$35x10^5$
Saturated velocity (cm/sec)	$1x10^7$	$2x10^7$	$2x10^7$
Electron mobility (in bulk) (cm^2/V-sec)	1350	380	800
Hole mobility (in bulk) (cm^2/V-sec)	450	95	120
Thermal conductivity (W/cm-°K)	1.5	4.9	4.9
Melting point (°C)	1420	2830	2830

Table 2.1 Parameter of low field model for 4H-SiC at 300K

Parameter	**4H-SiC**
MUN.MIN	**40cm^2/Vs**
MUN.MAX	**950 cm^2/Vs**
NRFEN	**2x10^{17}cm^{-3}**
ALPHAN	**0.76**

Table 2.2 Parameters for 4H-SiC MOSFET mobility models.

parameter	**Unit**	**4H-SiC**
μ_{min}	**cm^2/Vs**	**40**
μ_{max}	**cm^2/Vs**	**950**
N_{ref}	**cm^{-3}**	**2x10^{17}**
α		**0.76**
B		**1.0x10^6**
C		**1.74x10^5**
$\alpha 1$		**0.0516**
D	**V/s**	**5.82x10^{14}**

Table 3.1 Values of doping concentration, electron mobility, drift layer thickness, and specific on-resistance as a function of breakdown voltage for ideal 4H-SiC and Si power MOSFET at room temperature condition.

Breakdown Voltage(V)	Doping Concentration (cm^{-3})	Electron Mobility $(cm^2/V \cdot s)$	Width (μ_m)	Specific On-Resistance $(\Omega \cdot cm^2)$
Si				
200	1.72×10^{15}	1336	12.48	3.35×10^{-3}
1000	2.01×10^{14}	1356	81.59	1.88×10^{-1}
5000	2.35×10^{13}	1360	533.44	1.05×10^{1}
6H-SiC				
200	1.60×10^{17}	267	1.16	1.69×10^{-5}
1000	1.81×10^{16}	435	7.69	6.11×10^{-4}
5000	2.04×10^{15}	530	51.12	2.95×10^{-2}
4H-SiC				
200	3.74×10^{17}	388.95	0.75	3.23×10^{-6}
1000	3.93×10^{16}	745.55	5.19	1.11×10^{-4}
5000	4.13×10^{15}	905.05	35.83	5.98×10^{-3}

$\frac{R^{Si}_{on.sp}}{R^{SiC}_{on.sp}}$	200V	1000V	5000V
4H-SiC	1037.1	1693.1	1755.9
6H-SiC	198.2	305.7	355.9

Table 4.1 Oxide electric field in the trench corner as a functions of trench width, for rectangular and round corner.

Trench width(μ m)	4	8	12
Oxide electric field (10^6V/cm) Rectangular corner	7.8	7.1	6.4
Oxide electric field (10^6V/cm) Rounded corner	6.9	6.3	5.8

Table 4.2 The dependence of the oxide electric field at the trench corner of the oxide

thickness.

Oxide thickness(μm)	0.1	0.2	0.3
$E_{oxide}(10^6 V/cm)$ Trench width (8 μm)	6.3	5.7	4.9
$E_{oxide}(10^6 V/cm)$ Trench width (12 μm)	5.8	5.1	4.3

Table 4.3 Comparison of ACCUFET structure

Structure	MAX.Blocking Voltage（V）	On-resistance (Ω)	BFOM (V^2/Ω)
Trench	980	3.87	$2.48x10^5$
DIMOS	1150	7.9	$1.67x10^5$
Innovative	1535	4.01	$5.88x10^5$