國 立 交 通 大 學

電子工程學系電子研究所

碩 士 論 文

奈米級金氧半場效電晶體之通道背向式散射係數萃取

Extraction of Channel Backscattering Coefficients in Nanoscale MOSFET

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摘要

閘極氧化層厚度為 1.65 奈米的 N-型通道金氧半電晶體，在靠近源極的 k_BT layer 內之通道背向式散射係數被分為兩個要素探討：背向式散射在半熱平衡狀態下的平均自由路徑，以及 k_BT layer 的寬度。另外確認此分離方法正確性的證據也更進一步提出：(i) 靠近源極的導帶概觀圖；(ii) 另一個透過跟溫度有關的汲極電流公式來求得背向式散射係數的方法。這些發現彼此之間更具有相當的一致性，並支持著背向式散射確實是此係數的起源。因此，我們可以合理的宣稱：這些被分離的要素，以及相對應與溫度及偏壓的關係，可以被適宜地用以描述在通道背向式散射理論架構之下運作的元件操作情形。

Extraction of Channel Backscattering Coefficients in Nanoscale MOSFET

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Abstract

Abstract:

Channel backscattering coefficients in the k_BT layer (near the source) of 1.65-nm thick gate oxide n-channel MOSFETs are systematically separated into two distinct components: the quasi-thermal-equilibrium mean-free-path for backscattering and the width of the k_BT layer. Evidence to confirm the validity of the separation procedure is further produced: (i) the near-source channel conduction-band profile; and (ii) an analytic temperature-dependent drain current model for the channel backscattering coefficients. The findings are also consistent with each other and therefore corroborate channel backscattering as the origin of the coefficients. Consequently, it can be reasonably claimed that the separated components, as well as their dependencies on temperature and bias, are adequate while being used to describe the operation of the devices undertaken within the framework of the channel backscattering theory.

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碩士兩年的時光，過得比想像中快許多，也過得比想像中快樂充實，這實在要感謝很多人的幫忙。

首先要感謝，也最感謝的是陳明哲教授。在研究生兩年的經驗及聽聞中，我慢慢的體會到，沒有最好的指導教授，只有最適合你的指導教授；而老師便是我各方面都相當投契指導教授。不管是做學問時，遇到困難時的點子，舊有東西做新發揮的創意；投論文時一絲不苟的嚴謹；閒聊時對研究對人事的態度；請假爬山時的欣然應許。在此雖然紙短，但實在衷心的希望能表達對老師的感謝。

研究生的幸福取決於老師跟實驗室，我們人少但感情融洽的實驗室是這快樂兩年不可或缺的因素。大師兄卓煜盛教我軟體使用；二師兄呂明霈指導我諸多疑問並教我量測；林大文學長做人做事認真的態度；李亨元的戰友情誼；陳榮挺超時守護實驗室的督促；林盈秀的美食資訊。少了這些我的碩士生涯是不可能圓滿的。

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謹以此微不足道的感言獻給每一位我認識的人，感謝你們。

Contents

Figure Captions

Chapter 1

Introduction

As MOSFET channel lengths continue to decrease with a rapid pace toward nanoscale regime, quantum mechanics is expected to govern the underlying transport details. It is generally recognized that while carriers, during the operation of the device, encounter significant space confinements and few scatterings, the conventional semiconductor transport theory would lose its accuracy in addressing such situations. To circumvent this issue, alternative researches devoted to the areas of mesoscopic physics have been proposed one after another [1]-[4]. Among them, channel backscattering theory [5],[6] has attracted increasing attention due to the potential of being able to provide a new perspective about carrier transport in nanoscale MOSFETs.

The channel backscattering theory describes a wave-like transport of carriers through the channel from source to drain. As schematically shown in Fig. 1, the channel length L_{eff} is divided into two parts: $0 < x < l$ and $l < x < L_{eff}$. Here l represents the critical length from the source the conduction band bends down by a thermal energy of k_BT, where k_B is Boltzmann's constant and T the temperature [5],[6]. At the top of the source-channel junction barrier, the carriers are injected from the source reservoir into the channel. The height of the barrier is essential and can be modulated through applied gate voltage (V_G) and drain voltage (V_D). The latter is involved with well-known DIBL [5]. During above-threshold operation, the barrier still exists but gains less influence from the gate. Inside the k_BT layer, a certain fraction, denoted r_c, of carriers with incident flux F are reflected back to source, so this ratio being named backscattering coefficient. The resultant drain current is thus effectively a function of the extent of backscattering, as in terms of r_c. Therefore, by

means of extracting r_c, we could assess certain key factors such as defining the performance limits [7],[8] or evaluating the efficiency of devices by specific technology.

According to channel backscattering theory, the drain current, I_D, is simply related to Q_{inv} and v_{inj} [5],[6]:

$$I_D = Q_{inv} v_{inj} \frac{(1 - r_C)}{(1 + r_C)} \tag{1}$$

, where Q_{inv} is the inversion layer charge density per unit area at the top of the source-channel junction barrier and is composed of both injected and reflected flux; and v_{inj} is the thermal injection velocity. Here the term $Q_{inv}/(1+r_c)$ could be considered as the carriers injected from source and $(1-r_c)$ the ratio of carriers traveling across the barrier to drain. With this relationship, assessment of r_c has been proposed by I-V fitting method [7],[10],[11]. Furthermore, another temperature dependent method [9] developed recently is introduced as a new way to explore the device.

It is worthy to notice that through multiple backscattering events in the k_BT layer, r_c is related to l by [5]:

$$r_c = 1 \Big/ 1 + \frac{\lambda}{\ell} \tag{2}$$

where λ denotes the quasi-equilibrium mean-free-path for backscattering. The relationship implies that once we could decouple λ and l from r_c, we would be able to gain physical insights into underlying mechanism.

In this thesis, the extraction of rc and the decoupling of λ and l both are performed on 1.65-nm thick gate oxide n-channel MOSFETs having physical gate

length of 68nm. First of all, a quantum mechanical simulation [12] on a MOS system furnishes values of Q_{inv} and v_{inj} with process parameters as input, followed by fitting of I-V to determine backscattering coefficients. The temperature dependent extraction technique is then applied to provide extra experimental evidence. The dependencies on applied bias and temperature are crucial to clarify the origin responsible. In addition, interpretations and clarifications are drawn in the way, which can substantially improve current understandings of the channel backscattering theory and its potentials.

Chapter 2

I-V Fitting Methodology

2-1 Theory

In this section, we would first explain the main formula in more detail and demonstrate the derivation of simulation parameters.

Main Formula

We are deriving the main formula from (1). Assuming operation under saturation region, the current flux in the channel could be deduced to be just that from source to channel, F, whereas that from drain to channel could be ignored. Here F can be presented as:

$$F = n_S^+ \cdot v_{inj} \tag{3}$$

where n_S^+ denotes the carrier density per unit area injecting toward +x direction into channel and v_{inj} indicates the corresponding thermal velocity. Assuming certain ratio r_c of F is backscattered within k_BT layer, the reflected part toward –x direction and the transmitted part to drain could be expressed respectively by r_cF and $(1-r_cF)$. Note that it is assumed that no energy loss during backscattering so both r_cF and $(1-r_cF)$ move with the original velocity, v_{inj}. At the interface between source and channel, the total carrier density per unit area, $n_{Stot(0)}$ can therefore be obtained by:

$$n_{S_{tot}(0)} = \frac{1}{v_{inj}} \cdot (F + r_c F) = n_S^+ \cdot (1 + r_c) \tag{4}$$

Since the flux arriving at the drain which constitutes the resultant drain current is F_{drain}

= (1-r_c)F and the MOS electrostatic equation of inversion layer charge density is [5]:

$$n_{S_{tot}(0)} = \frac{C_{eff}}{q}(V_G - V_{th}) \tag{5}$$

then we can derive:

$$\begin{aligned} I_{D_{sat}} &= W \cdot q \cdot n_{drain} \cdot v_{inj} = W \cdot q \cdot v_{inj} \cdot (1 - r_c) n_S^+ \\ &= W \cdot q \cdot v_{inj} \cdot \frac{1 - r_c}{1 + r_c} n_{S_{tot}(0)} = W \cdot C_{eff}(V_G - V_{th}) v_{inj} \cdot \frac{1 - r_c}{1 + r_c} \end{aligned} \tag{6}$$

Derivations of simulation parameters

In (6), the terms C_{eff} and v_{inj} could not be directly assessed by experimental data; so, to circumvent it, alternative methods are necessary such as temperature-dependent method [9] discussed later and the theoretical calculation via quantum mechanical simulation [8],[12], which is to be discussed in this chapter.

The one-dimensional quantum mechanical simulation [13],[14] dedicated to an n^+ polysilicon/gate oxide/p-type substrate MOS system is initiated by setting a distinct physical environment through three significant process parameters: T_{ox}, N_{sub}, and N_{poly}. Here T_{ox} is the thickness of gate oxide and N_{sub} and N_{poly} are the doping concentration in substrate and in polysilicon, respectively.

With a distinct physical environment set up as shown in Fig. 2, the Fermi level, E_F, and subband energy levels, E_{ij}, can be subsequently derived by [14]:

$$E_F = q(\varphi_s - \varphi_{bn}) \tag{7}$$

$$E_{ij} = (\frac{\hbar^2}{2m_{Zj}})^{1/3}(\frac{3\pi q F_{Si}(i-\frac{1}{4})}{2})^{2/3} \quad (8)$$

In (8), i represents subband index; j the valley index being 1 for two-fold valley or 2 for 4-fold valley; m_{Zj} the corresponding normal electron effective mass in the jth valley; and the most important parameter, F_{Si}, the silicon surface electric field, is solved by an iteration procedure [14].

E_F and E_{ij} together characterize a specific MOS system. Once they can be determined, a series of parameters leading to C_{eff} and v_{inj} can immediately be quantified. At first, the charge density associated with subband i for specific valley is

$$n_s^i = \gamma \frac{m_{di}}{\pi\hbar^2}\frac{k_B T}{2}\ell n[1+\exp(\frac{E_F - E_i}{k_B T})] \quad (9)$$

where γ denotes the valley degeneracy; m_{ci} the density-of-states effective mass for subband i. (9) could be further interpreted in two aspects: one for C_{eff} and the other for v_{inj}. The charge density in underlying 2DEG (two-dimensional electron gas) inversion layer, Q_{inv}, could be obtained by summing all n_s^i for correspondent subband i and valley j so as to assess C_{eff} by fitting MOS electrostatics formula $Q_{inv} = C_{eff}(V_{GO} - V_{tho})$. On the other hand, for each distinct subband i, the thermal injection velocity is [8]:

$$v_{inj}^i = \sqrt{\frac{2k_B T m_{ci}}{\pi m_{di}^2}}\frac{\Im_{1/2}(\frac{E_F - E_i}{k_B T})}{\ell n[1+\exp(\frac{E_F - E_i}{k_B T})]} \quad (10)$$

where m_{ci} is the conductivity effective mass for subband i and $\Im_{1/2}$ the Fermi-Dirac

integral of order one-half. Finally, the effective thermal injection velocity at the top of the source-channel junction barrier is defines as [8]:

$$v_{inj} = \frac{\sum n_s^i v_{inj}^i}{\sum n_s^i} \tag{11}$$

In 2DEG MOS system, the effective mass is separated into two sorts due to the z-direction confinement: the longitudinal mass $m_l = 0.916m_o$ and the transverse mass $m_t = 0.19m_o$, where m_o means the original electron mass. This thus causes further difference in conductivity effective mass, m_{ci} and density-of-states effective mass m_{di}: $m_{ci} = m_t$ and $m_{di} = m_t$ for 2-fold valleys and $m_{ci} = 2m_lm_t/(m_l + m_t)$ and $m_{di} = (m_lm_t)^{0.5}$.

2-2 Devices under Study

Halo-implanted bulk n-channel MOSFETs under investigation were fabricated in state-of-the-art manufacturing process. Tox = 1.65 nm; channel width, W = 10 μm; and mask gate length, L_{mask} from 10 μm to 0.075 μm. The main extraction procedure would be demonstrated on L_{mask} = 0.09 μm. As for the measure conditions, we adopt the following systems: HP4156B and a thermal chuck and cooling system to set up the conditions: V_G = 0.1~1.2V; V_D = 0.025, 0.1, 0.5, and 1.0V; and temperature = -40°C, -10°C, and 25°C.

2-3 Parameter Extraction

Flowchart

Fig. 3 summarizes schematically the procedure of extracting r_c and l. The round-corner frames indicate the experiment data; the indented-corner frames imply the extraction and simulation data; and the connection lines illustrate the relationship

between the data and how to derive them in series. We would then demonstrate the extraction procedure step by step based on the connection lines of the flowchart.

C-V curve

The C-V measurement is performed on 50 μm×50 μm testkey. Fig. 3 shows experimental results of capacitance with unit in μF/cm^2.

T_{ox}, N_{sub}, N_{poly}

As shown in Fig. 3, T_{ox}, N_{sub}, and N_{poly} are obtained by C-V comparison. The measured C-V curve is compared with that calculated by the quantum simulator with T_{ox}, N_{sub}, and N_{poly} as input. Since T_{ox}, N_{sub}, and N_{poly} separately affect the C-V curve in different ways, a distinct set of T_{ox}, N_{sub}, and N_{poly} can be found with optimum C-V match. In Fig. 4, we get T_{ox} = 1.65 nm, $N_{sub} = 8\times10^{17}$ cm^{-3} and $N_{poly} = 9\times10^{19}$ cm^{-3}

Q_{inv}, v_{inj}, C_{eff}

With T_{ox}, N_{sub}, and N_{poly} known, Q_{inv}, v_{inj}, and C_{eff} can be directly assessed by the simulator. Fig. 5 shows the resulting inversion charge, Q_{inv}, versus gate voltage under T = -40°C, -10°C and 25°C. Furthermore, C_{eff} fitted by one-dimensional MOS electrostatics formula $Q_{inv} = C_{eff}(V_{GO}-V_{tho})$ is depicted in Fig. 6. The corresponding v_{inj} is given in Fig. 7.

I_D-V_G

The drain current-gate voltage, I_D-V_G curve is measured under temperature = -40°C, -10°C, and 25°C with L_{mask} = 90nm as shown in Fig. 8. It is worthy noticing that the curves of different temperature intersect each other at a critical gate voltage around V_G = 0.45V as mentioned in [9]. Besides, I_D-V_G is also measured with drain voltage V_D as parameter. The results are shown in Fig. 9 in order to compensate the

insufficiency of the 2DEG quantum simulator concerning the effect of V_D.

V_{th} threshold voltage

In order to circumvent potential uncertainties such as DIBL in determining threshold voltage of nanoscale devices, we adopt a two-step method.

First, V_{tho}, the threshold voltage under low V_D (25mV) is extracted by maximum-transconductance method at T = -40°C, -10°C, and 25°C. Fig. 9 shows a typical procedure of extracting V_{tho}. Initially I_D is differentiated with respect to V_D and the maximum transconductance, G_m-max is then picked up. Next, we draw a tangent line which intersects the I_D-V_G curve at the corresponding G_m-max point. The intersection of this tangent line with the V_G-axis determines V_{tho}.

Second, on the purpose of incorporating DIBL effect in determining threshold voltage under higher V_D, the magnitude of barrier lowering which induces ΔV_{th} is evaluated by the constant current method (CCM) as shown in Fig. 10. The specific constant current is chosen to be around $(W/L)\times 10^{-7}$ A, in order to intersect the exponentially-growing region of drain current, leading to $\Delta V_{th.}$ Thus the V_{th} under different V_D can be approximated by $V_{th} = V_{tho} - \Delta V_{th}$.

μ_{no}, mobility

We adopt a drain conductance method (G_d method) [15] to estimate the near-thermal-equilibrium mobility μ_{no} on long-channel devices. This method is initiated with the usual current-voltage relationship under very low drain bias:

$$I_D = \mu \cdot C_{eff} \cdot \frac{W}{L}[(V_{Go} - V_{th})V_D - \frac{1}{2}V_D^2] \approx \mu \cdot C_{eff} \cdot \frac{W}{L}(V_{Go} - V_{th})V_D \qquad (12)$$

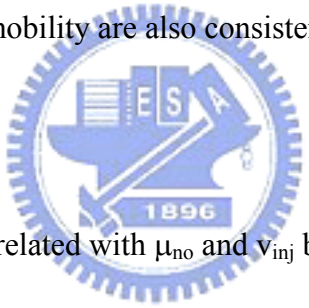
By differentiating (12) with respect to V_D we would get:

$$\frac{dI_D}{dV_D} = \mu \cdot C_{eff} \cdot \frac{W}{L} \cdot [(V_{GO} - V_{th}) - V_D \cdot \frac{dV_{th}}{dV_D}] = \mu \cdot C_{eff} \cdot \frac{W}{L} \cdot [(V_{GO} - V_{th}) - V_D \cdot DIBL] \tag{13}$$

Finally, the near-thermal-equilibrium mobility μ_{no} is derived in the form

$$\mu = \frac{dI_D}{dV_D} \cdot \frac{L}{C_{eff} \cdot W \cdot [(V_{GO} - V_{th}) - V_D \cdot DIBL]} \tag{14}$$

Fig. 11 reveals the mobility curve separated into three governing effects: Coulombic scattering, phonon scattering, and surface roughness scattering. The corresponding temperature dependencies of mobility are also consistent with our expectation.



λ, mean-free-path

The mean-free-path λ is related with μ_{no} and v_{inj} by:

$$\lambda = 2\frac{k_B T}{q}\frac{\mu_{no}}{v_{inj}} \tag{15}$$

Therefore, the finished extraction of μ_{no} and v_{inj} makes it straightforward to evaluate λ as shown in Fig. 11. We could see that the λ dependency on temperature is distinctly separated into two parts: below V_G = 0.45V, λ increases with increasing temperature and above V_G = 0.45V, λ decreases with increasing temperature. The former effect against the usual idea that λ decreases with increasing temperature is due to thermal motion dominating over phonon scattering or surface roughness scattering. On the other hand, the individual λ-V_G curve is coincident with the mobility-V_G relationship. The extraction of λ value would play a significant role

later on the separation of k_BT layer length, *l*.

I_G-V_G

I_G-V_G curves are measured on various L_{mask} in linear region in order to get the corresponding gate length, L_G, which would be adopted as a more precise reference when deriving R_{SD}.

L_G, gate length

Gate length is extracted simply by the gate current ratio. On a well-fabricated wafer, the L_G-L_{mask} plot shows a common linear relationship. The reason why L_G is used as reference instead of L_{mask} is that L_G serves as a more accurate gauge. Because certain differences do exist unavoidably when defining L_G from L_{mask} = 10μm to 0.075μm, a more reliable L_G reference is then developed to take charge of L_{mask} = 1.2μm to 0.075μm. That is said, I_G-V_G of L_G = 1.2μm is now set as typical long channel length for comparison with shorter channel length to distinguish the slight deviation occurring in patterning L_G.

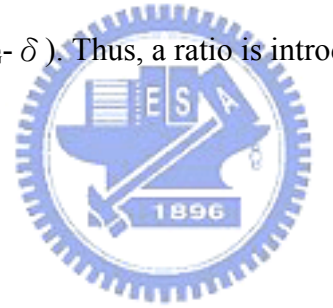
R_{SD}, series resistance

As shown in Fig. 13, there exists series resistance R_{SD} between the external terminal and the active region. Here the drain resistance R_D is reasonably assumed to be the same as source resistance R_S. As a result, the internal V_{Go} should be corrected by $V_{Go} = V_G' - I_D R_S$. Similarly, $V_{Do} = V_D' - I_D R_{SD}$.

The source-drain series resistance R_{SD} lying between the intrinsic MOSFET and the external terminal is extracted by shift-and-ratio method [15]. It is initiated from the attempt separating the total external resistance into two parts [15]:

$$R_{tot} = R_{SD} + R_{ch} = R_{SD} + \frac{L_{eff}}{\mu_{eff} C_{ox} W (V_G - V_{th})} = R_{SD} + L_{eff} \cdot f(V_G - V_{th}) \qquad (16)$$

where R_{SD} is assumed to be roughly constant under a matured fabrication process and the effective channel resistance R_{ch} defined as $R_{ch} \equiv V_{ds}/I_{ds}$ could be taken as function of gate voltage and effective channel length. Further differentiating (16) by gate voltage to skip R_{SD} and to take use of the R_{ch}-L_{eff} relationship yields $S(V_G) \equiv dR_{tot}/dV_G$. A simple concept that R_{ch} and corresponding R_{SD} could be obtained by comparing $S(V_G)$ for long channel and short channel, is thus generated. However, $f(V_G\text{-}V_{th})$ of short channel and long channel would be affected by divergent effects such that distorted comparison ratio. Some hurdle develops in terms of unfavorable effects in a shifting term $S(V_G\text{-}\delta)$. Thus, a ratio is introduced [15]:



$$r(\delta, V_G) \equiv \frac{S^o(V_G)}{S^i(V_G - \delta)} \qquad (17)$$

where $S^o(V_G)$ is from long channel and $S^i(V_G\text{-}\delta)$ from short channel. By calculating δ to meet the minimum standard deviation of $r(\delta, V_G)$, L_{eff} could be acquired by [15]:

$$< r >_{\delta_{\min}} = \frac{L^o_{eff}}{L^i_{eff}} \approx \frac{L^o_{mask}}{L^i_{eff}} \qquad (18)$$

Note here L^o_{mask} could also be approximated by L^o_{gate} which is expected to give a more precise reference. Since L^i_{eff} has been derived, R_{SD} can be immediately calculated by [15]:

$$R_{SD} = \frac{< r >_{\delta_{\min}} R^{i}_{tot}(V_G - \delta_{\min}) - R^{o}_{tst}(V_G)}{< r >_{\delta_{\min}} - 1} \tag{19}$$

The resultant R_{SD} is shown in Fig. 14, in which we could observe a steady value of R_{SD}. Therefore an average value of R_{SD} = 150Ω-μm could be reasonably chosen. It is worthy noticing that R_S becomes 7.5Ω accounting for channel width = 10μm while being applied in the form (V_G'-$I_D R_S$).

2-4 Results

As shown in Fig. 3, once all necessary parameters acquired, the backscattering coefficient r_c extraction and *l* separation are instantly available. First, (6) is adjusted to include DIBL and R_{SD} effect as:

$$I_{D_{sat}} = W \cdot C_{eff}\{V_G - I_D R_S - [V_{tho} - DIBL \times (V_D - I_D R_{SD})]\} v_{inj} \cdot \frac{1 - r_c}{1 + r_c} \tag{20}$$

The resultant r_c value versus gate voltage is illustrated in Fig. 15, where we take the set of L_{mask} = 90nm at saturation region (V_D = 1V) under different temperatures as example. The first glance tells that the r_c values decrease with gate voltage at above threshold region and would tend to saturate when V_G > 0.7V, which implies that increasing gate voltage makes a significant effect upon the k_BT layer barrier so as to reduce r_c and that the influence would saturate if gate voltage arrives at a certain critical value. This goes well with our general expectation. Later indicated is the dependency on temperature. While comparing different r_c-V_G curves with temperature as parameters, a distinct increase of r_c with increasing temperature could be observed. It could be simply clarified that rising temperature increases a vibration in the lattice

and causes an increase in scattering probability.

The value of r_c which is equivalent to $(1+\lambda/l)^{-1}$ could be separated as λ and l. Since λ has been shown in Fig. 12, l can be instantly obtained in Fig. 16. Similarly, we could first observe a decreasing tendency toward increasing gate voltage in above-threshold region. However, instead of being saturated, the l-VG curve keeps lowering with rising gate voltage. It could be understood that gate bias physically forces the potential profile in such a way to reduce the k_BT layer length l. As far as temperature dependency is concerned, we can simply specify the direct proportion that relates l actually to k_BT potential drop with T as parameter. Additionally observed is that when V_G is large enough, the temperature dependency of l slightly lessens, which can be attributed to the more domination of gate voltage than that of temperature.

With reasonably extracted key parameters, we can preliminarily judge the validity of the r_c extraction and l separation methodology. Then the temperature dependency as supporting evidence is extensively carried out. Further discussions and interpretations are presented in following chapter.

Chapter 3

Temperature-dependent Method

3-1 Model Description

An alternative method is introduced to assess r_c and l based on the temperature dependency. To reveal it, we first replace the r_c in (6) to be $(1+\lambda/l)^{-1}$ so that we can assess the more direct dependencies of λ and l:

$$I_D = W \cdot C_{eff}(V_G - V_{th}) \cdot v_{inj} \cdot \frac{\lambda/l}{2+\lambda/l} \tag{21}$$

Next we set up a hypothesis about the temperature-dependent power coefficients of individual terms:

$v_{inj} \propto T^a$,

$\mu_{no} \propto T^b$,

$l \propto T^d$,

$and\ then\ \lambda = \frac{2k_B T \cdot \mu_{no}}{q \cdot v_{inj}} \propto T^{b+1-a}$

Differentiating (21) with respect to temperature leads to

$$\frac{dI_D}{dT} = W \cdot C_{eff} \left\{ v_{inj} \cdot \frac{\lambda}{2l+\lambda} \cdot \frac{d(V_G - V_{th})}{dT} + (V_G - V_{th}) \cdot \frac{\lambda}{2l+\lambda} \cdot \frac{dv_{inj}}{dT} + (V_G - V_{th}) \cdot v_{inj} \frac{d(\frac{\lambda}{2l+\lambda})}{dT} \right\} \tag{22}$$

Further dividing (22) by I_D to eliminate the common factors and letting the term

dV_{th}/dT, i.e. temperature coefficient of threshold voltage to be η, we obtain

$$\frac{dI_D}{dT}\times\frac{1}{I_D}=\frac{-\eta}{(V_G - V_{th})}+\frac{1}{T}\left\{a+\frac{2(b+1-a-d)}{2+\lambda/l}\right\} \tag{23}$$

Again let $dI_D/(dT\times I_D) = \alpha$, (23) reduces to

$$\lambda/l=\frac{2(a-b+d-1)}{a-T(\alpha+\eta/V_{th})}-2 \tag{24}$$

Finally λ/l taking into account DIBL and series resistive potential drops is rewritten as:

$$\lambda/l=\frac{2(a-b+d-1)}{a-T\alpha-\frac{T\cdot\eta}{V_G'-I_DR_S-V_{tho}+DIBL\cdot(V_D'-I_DR_{SD})}}-2 \tag{25}$$

3-2 Experiment

According to (25), extra parameters to be solved are a, b, d, α and η. Here a, b, and d are simply fitted respectively by the temperature-dependent power coefficients of v_{inj} in Fig. 7, the mobility in Fig. 11, and the l in Fig. 16. η and α can be got from temperature dependencies of threshold voltage and I_D-V_G.

a, b, d

The temperature-dependent power coefficients are directly calculated as shown in Fig. 17. We can see that the v_{inj} component, a, and l component, d, both keep a

steady value around 0.4 and 0.8, respectively. On the other hand, the mobility component, b, showing a decreasing and saturating tendency with increasing gate voltage, corresponds to the mobility-temperature relationship as shown in Fig. 11.

η

According to the extracted near-thermal-equilibrium threshold voltage, η was extracted to be -0.49 mV/^{o}K.

α

Defined as $dI_D/(dT \times I_D)$, α can be directly derived by I_D-V_G curves under different temperatures as shown in Fig. 18. Note that α value increases with gate voltage and its polarity changes at V_G = 0.4~0.5V.

3-3 Results

The consistency of temperature-dependent method with I-V fitting method is summarized by Fig. 19. Here we can see coincidence at $V_G \geqq 0.6$V. Therefore the work can reasonably confirm not only the validity of r_c-extraction methodology but also the channel backscattering theory.

Chapter 4

Discussion and Interpretation

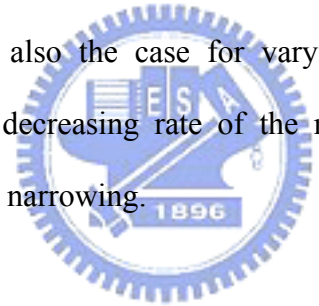
Here the potential profile near the source is addressed on the basis of k_BT layer in channel backscattering theory.

The source-channel junction barrier height is electrically modulated by the applied gate and drain voltage. The influence of gate voltage has been successfully included in the one-dimensional quantum simulator whereas the effect of drain voltage is estimated in the DIBL terms. As mentioned in section 2-4, we observed that increasing gate voltage causes a decreasing and saturating r_c. The decreasing tendency could be reasonably interpreted in order: increased gate voltage ➔ narrowed K_BT layer width ➔ lowered r_c. The saturation in r_C could be attributed to comparable dependencies on temperature between K_BT layer width and mean-free-path. As for drain voltage, there also exists a relationship: increasing drain voltage yields decreased r_c as shown in Fig. 20. Such relationship can be explained in terms of two aspects. First, higher drain voltage makes a more drastic change slope in potential profile near drain, which in turn narrows the width of KBT layer near the source. How to relate such change to r_c will be explained later. Second, as channel length shrinks, the k_BT layer profile experiences a reduction in width.

Within the framework of the channel backscattering theory, the channel conduction band is bent downward by a thermal energy k_BT while traversing from the injection point (i.e., the top of the source-channel junction barrier) to the end of the k_BT layer. According to this definition, the temperature dependent k_BT-layer widths were transformed into the near-source channel conduction-band profile as plotted in Fig. 21. Strikingly, it can be seen that the potential gradient increases in magnitude with increasing distance from the source. Thus, the conduction-band profile in Fig. 21

can serve as strong evidence for the work.

As demonstrated in Fig. 22, we can see that the K_BT layer narrows with decreasing gate length. Apparently, only with such quantified information can we draw a substantially clear picture of the potential profile where the channel backscattering takes place. In the case of L_{GM} = 75 nm, V_G = 1 V, and V_D = 1 V, for instance, the conduction band is bended down KT to a distance l = 5.3 nm from the source, followed by a bending of approximately 1 eV across the remainder of the channel. The gate voltage of 1 V determines the mean-free-path λ of 10 nm for backscattering in 5.3-nm wide K_BT layer, effectively producing a backscattering coefficient r_C of 0.35. The response of r_C to gate length down-scaling under the same bias applied is solely through the KT layer narrowing because the mean-free-path remains unchanged. This is also the case for varying drain voltage. As for the increasing gate voltage, the decreasing rate of the mean-free-path is considerably comparable with the KT layer narrowing.



Chapter 5

Conclusion

Extraction and separation of channel backscattering coefficients of nanoscale n-channel MOSFETs has been systematically performed. Consistent evidence has confirmed the validity of the separation procedure and has corroborated channel backscattering as the origin of the assessed coefficients. The separated components have eventually been used to describe the operation of the underlying device within the framework of the channel backscattering theory.

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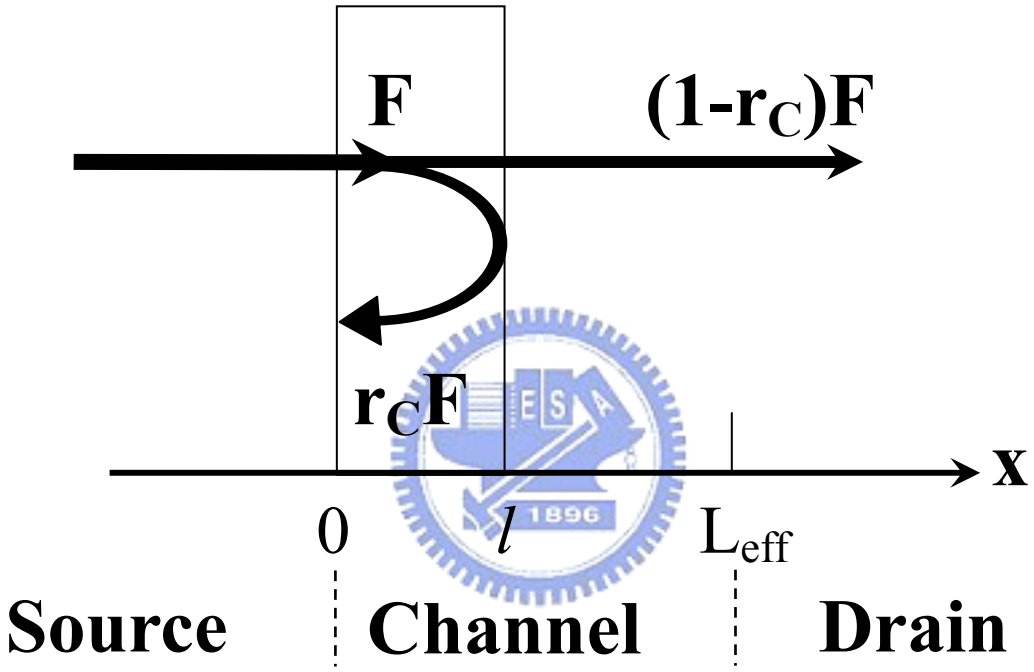

Fig. 1

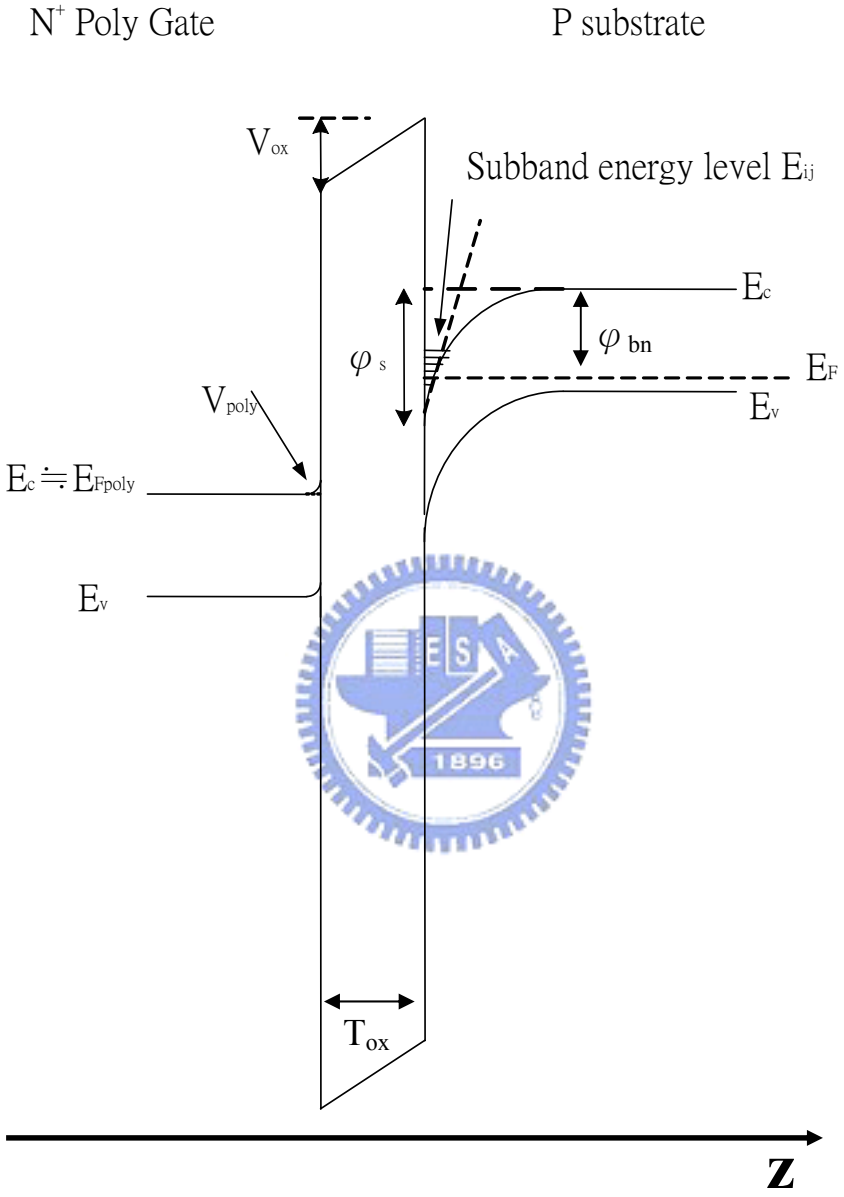
N+ Poly Gate
P substrate
Vox
Subband energy level Eij
Ec
φ bn
φ s
EF
Ev
Vpoly
Ec ≒ EFpoly
Ev
Tox
z

Fig. 2

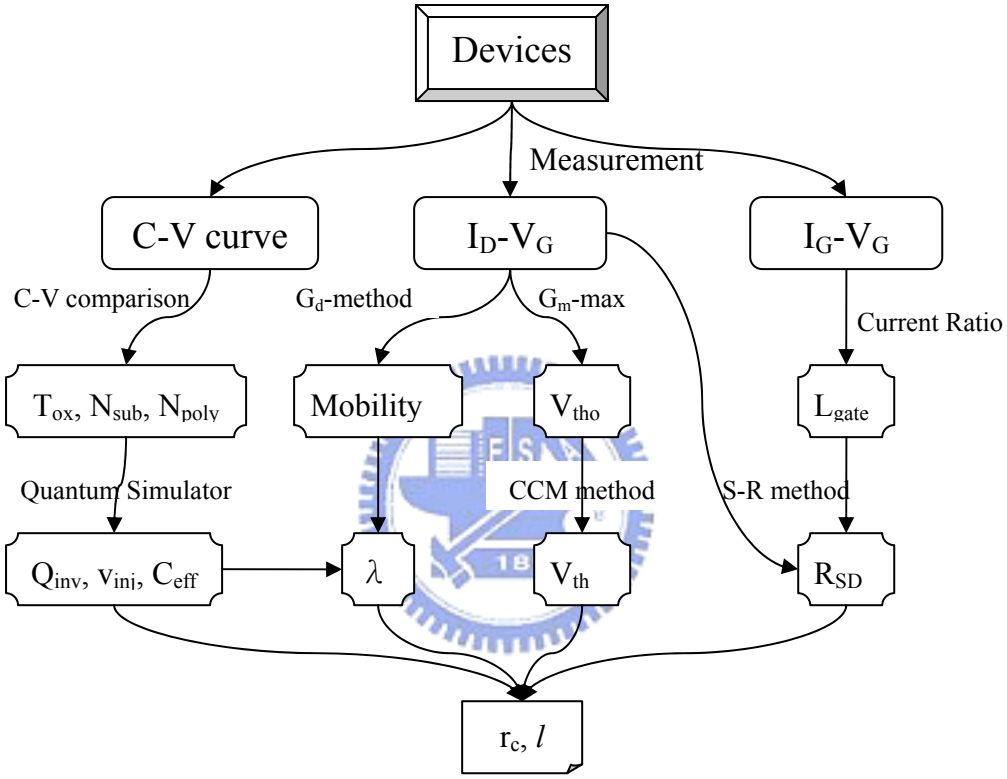
Devices
Measurement
C-V curve
I_D-V_G
I_G-V_G
C-V comparison
G_d-method
G_m-max
Current Ratio
T_{ox}, N_{sub}, N_{poly}
Mobility
V_{tho}
L_{gate}
Quantum Simulator
CCM method
S-R method
Q_{inv}, v_{inj}, C_{eff}
λ
V_{th}
R_{SD}
r_c, l

Fig. 3

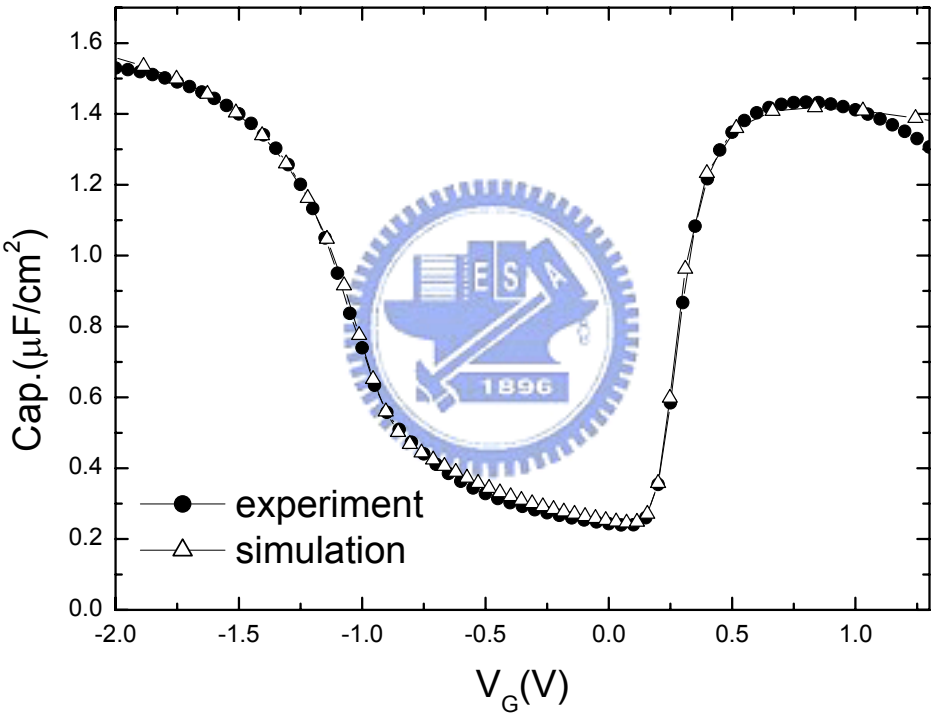
Cap.(μF/cm²)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-2.0
-1.5
-1.0
-0.5
0.0
0.5
1.0
V_G(V)
experiment
simulation

Fig. 4

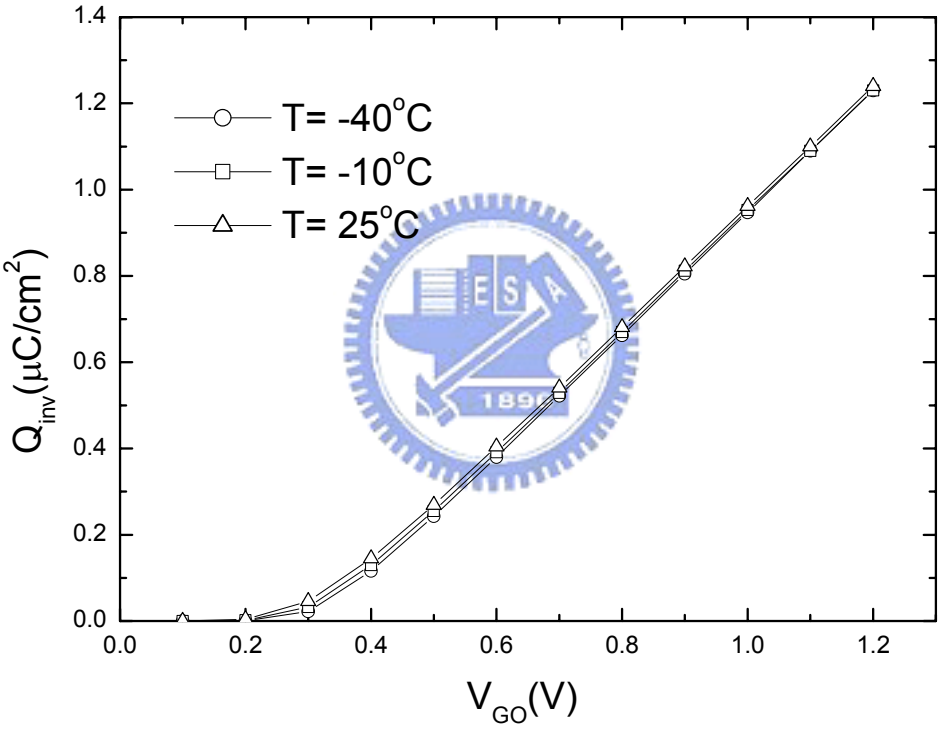

Fig. 5

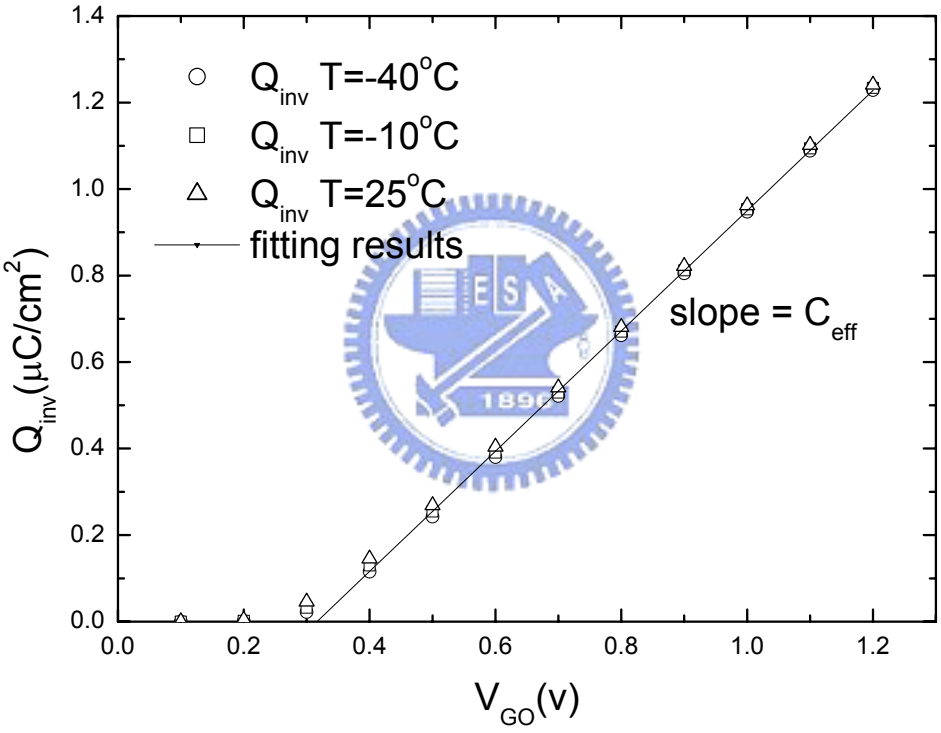
Q_inv T=-40°C
Q_inv T=-10°C
Q_inv T=25°C
fitting results
slope = C_eff
Q_inv(μC/cm²)
V_GO(v)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4

Fig. 6

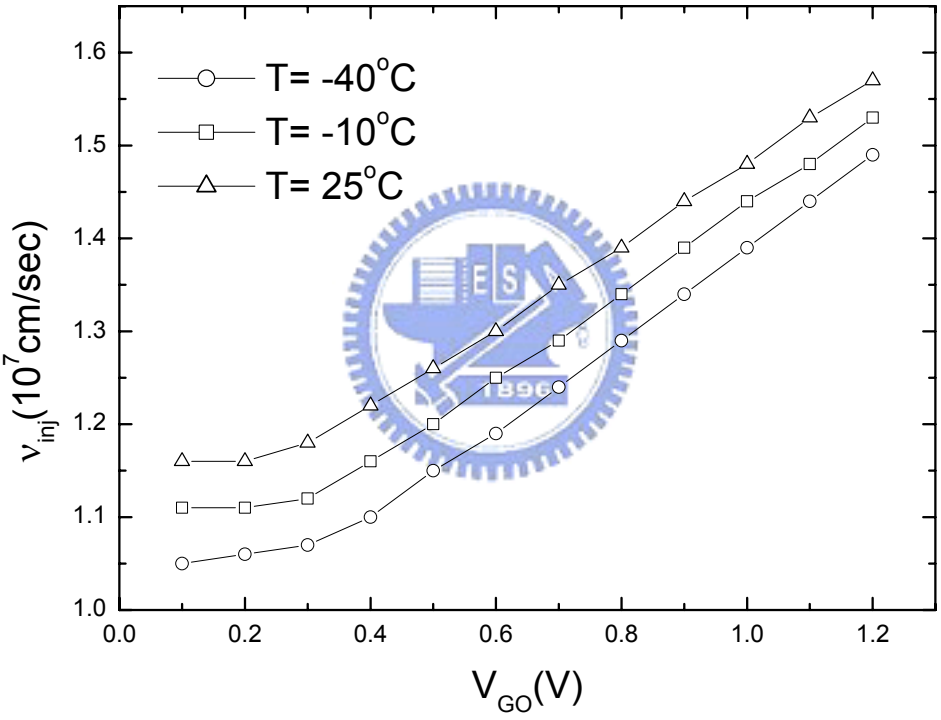
T= -40°C
T= -10°C
T= 25°C
$\nu_{inj}(10^7 cm/sec)$
$V_{GO}(V)$
1.0
1.1
1.2
1.3
1.4
1.5
1.6
0.0
0.2
0.4
0.6
0.8
1.0
1.2

Fig. 7

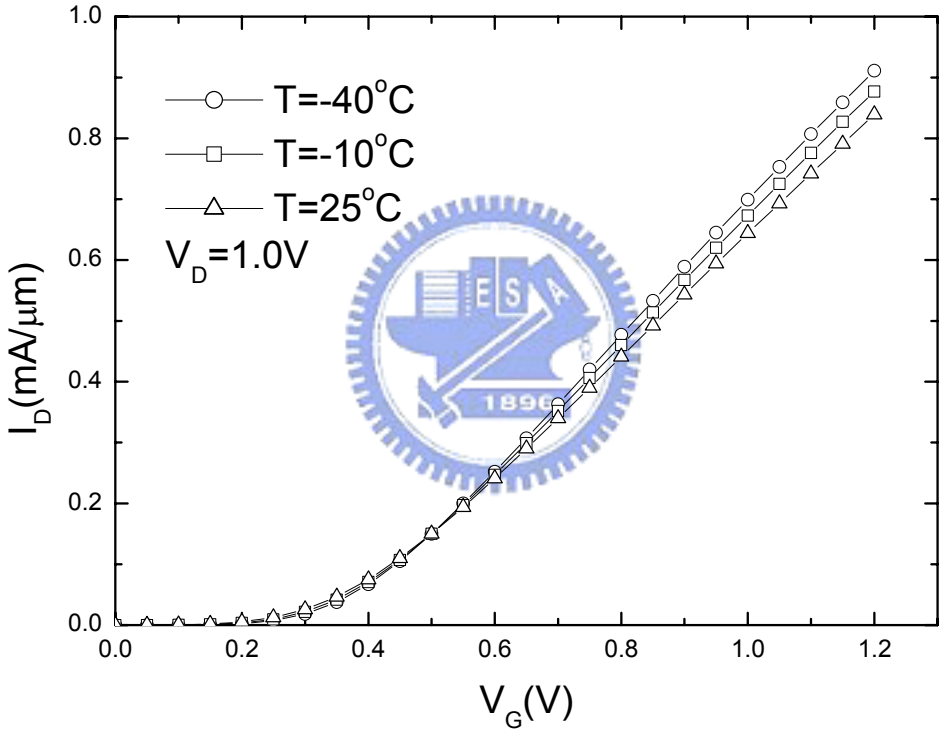

Fig. 8

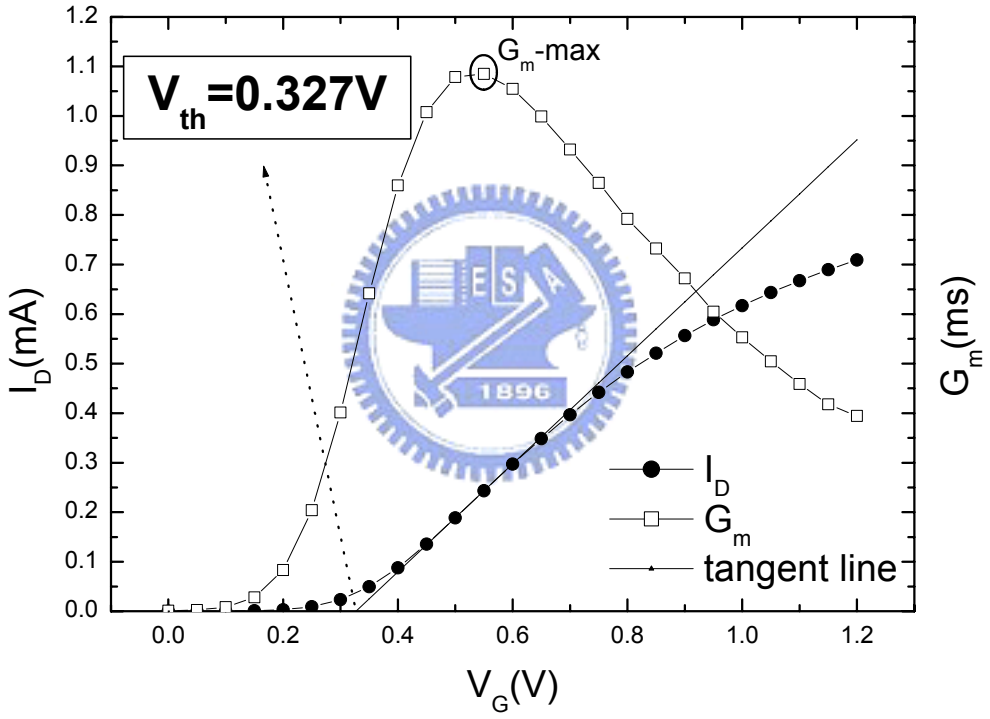
V_th=0.327V
G_m-max
I_D
G_m
tangent line
I_D(mA)
G_m(ms)
V_G(V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2

Fig. 9

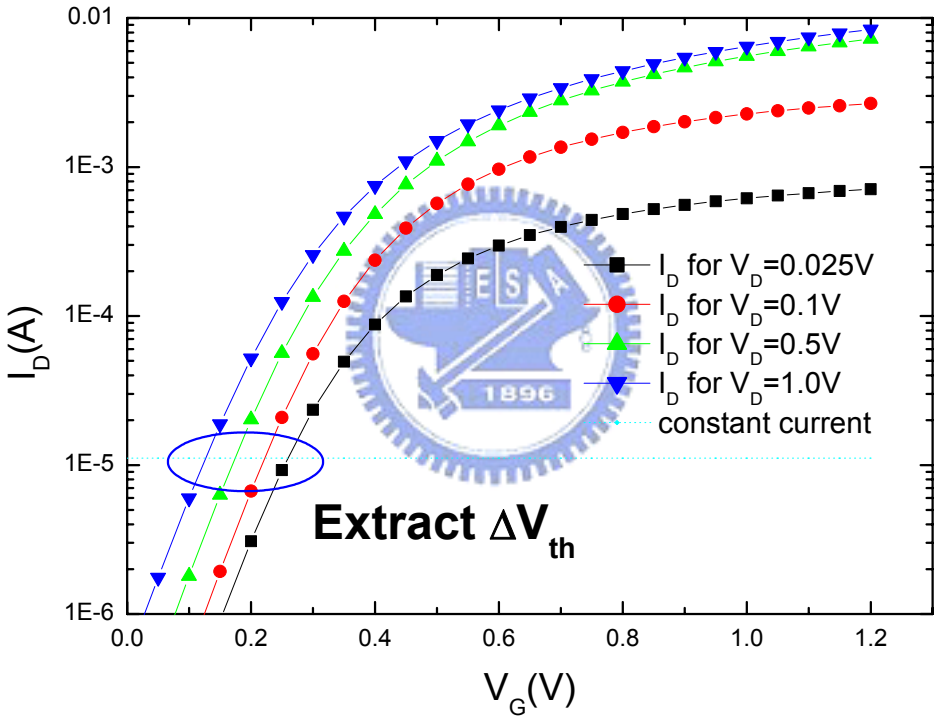
0.01
1E-3
1E-4
1E-5
1E-6
I_D(A)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
V_G(V)
I_D for V_D=0.025V
I_D for V_D=0.1V
I_D for V_D=0.5V
I_D for V_D=1.0V
constant current
Extract ΔV_{th}

Fig. 10

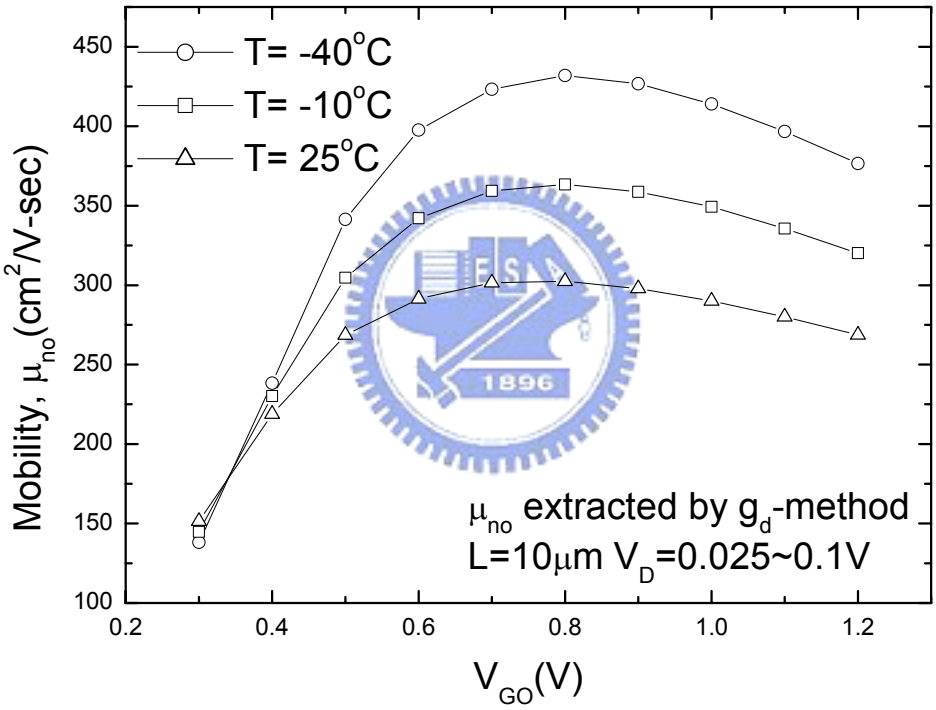
T= -40°C
T= -10°C
T= 25°C
μno extracted by gd-method
L=10μm VD=0.025~0.1V
Mobility, μno(cm2/V-sec)
VGO(V)
450
400
350
300
250
200
150
100
0.2
0.4
0.6
0.8
1.0
1.2

Fig. 11

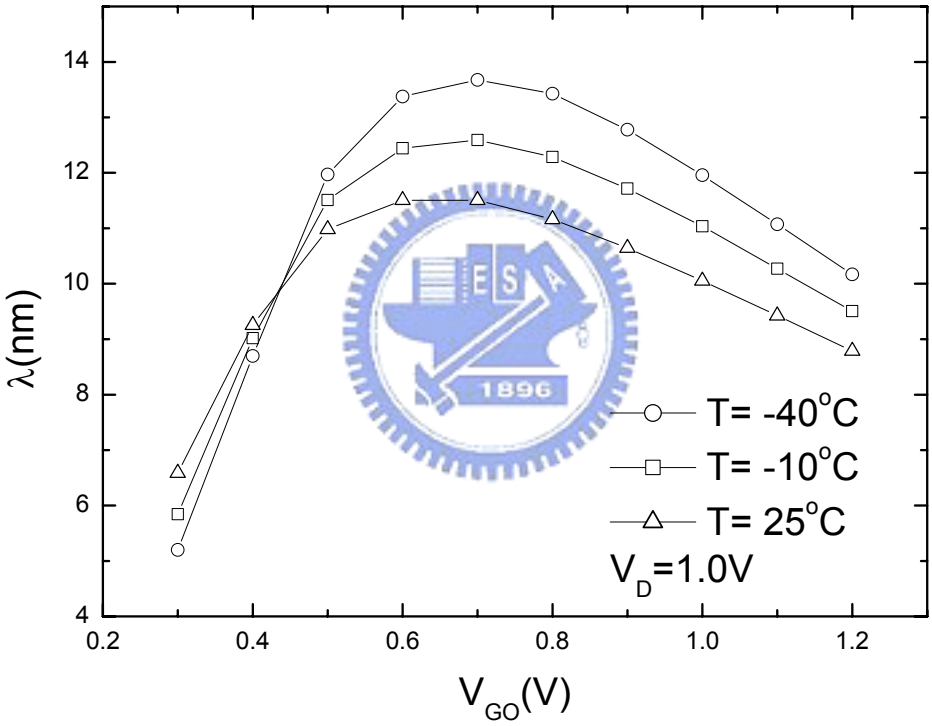

Fig. 12

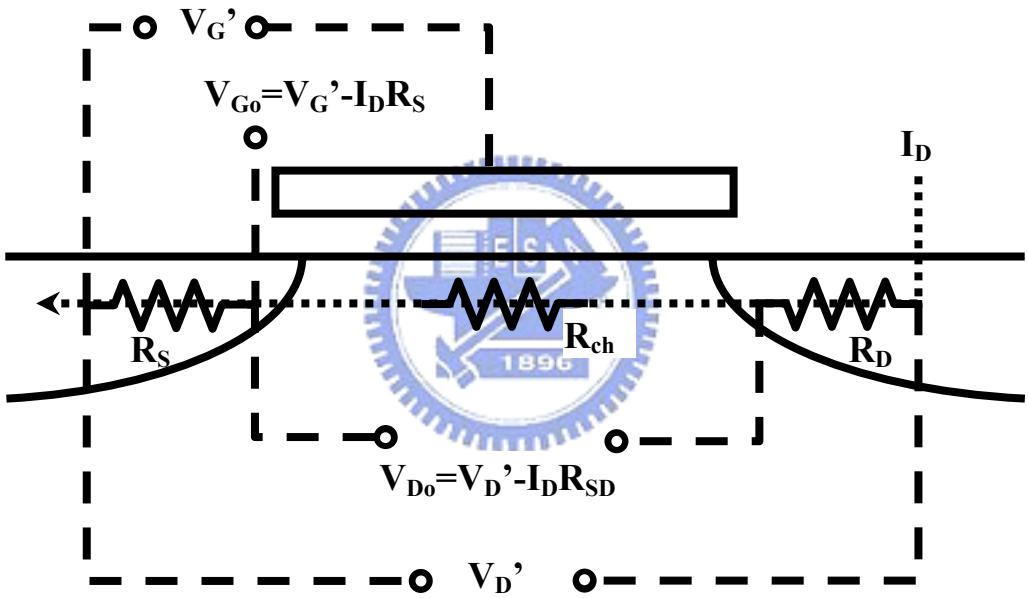

Fig. 13

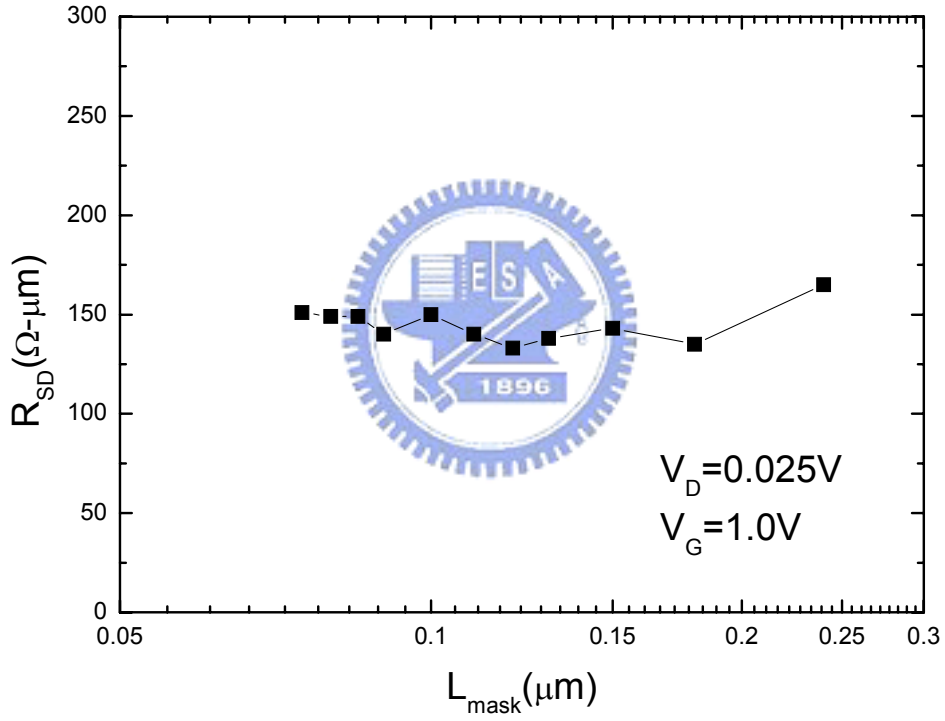
300
250
200
150
100
50
0
0.05
0.1
0.15
0.2
0.25
0.3
$R_{SD}(\Omega\text{-}\mu m)$
$L_{mask}(\mu m)$
V_D=0.025V
V_G=1.0V

Fig. 14

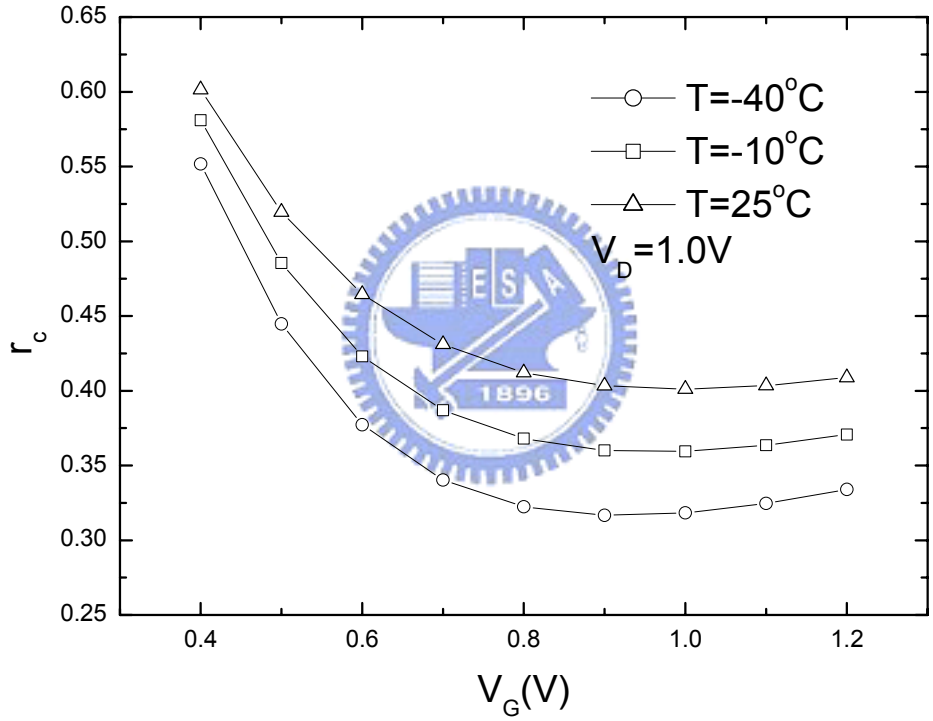
0.65
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
r_c
0.4
0.6
0.8
1.0
1.2
V_G(V)
T=-40°C
T=-10°C
T=25°C
V_D=1.0V

Fig. 15

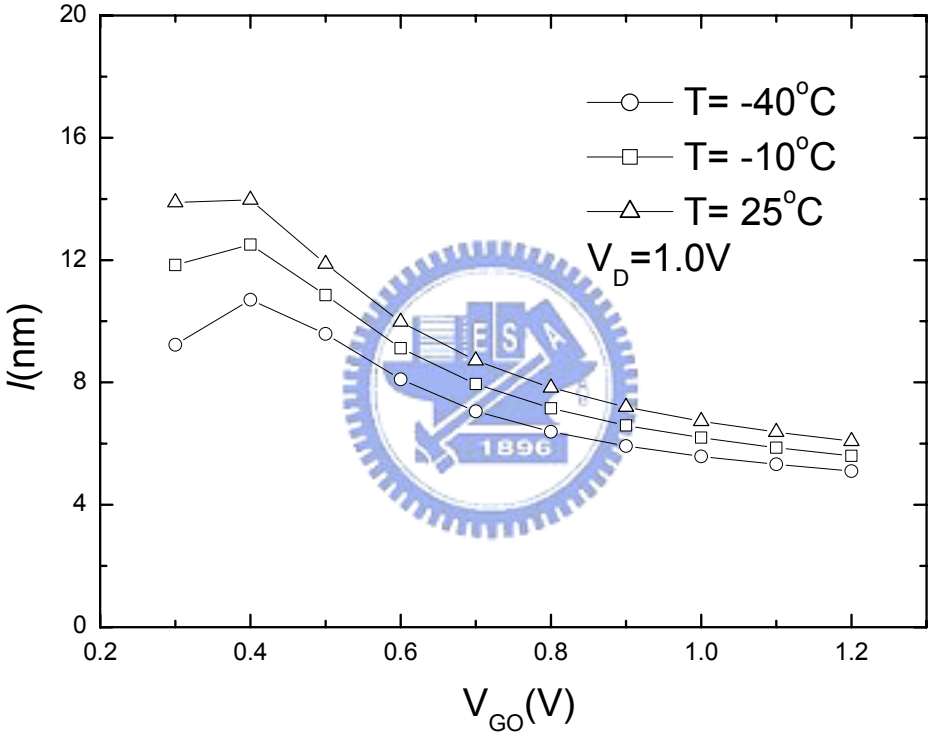

Fig. 16

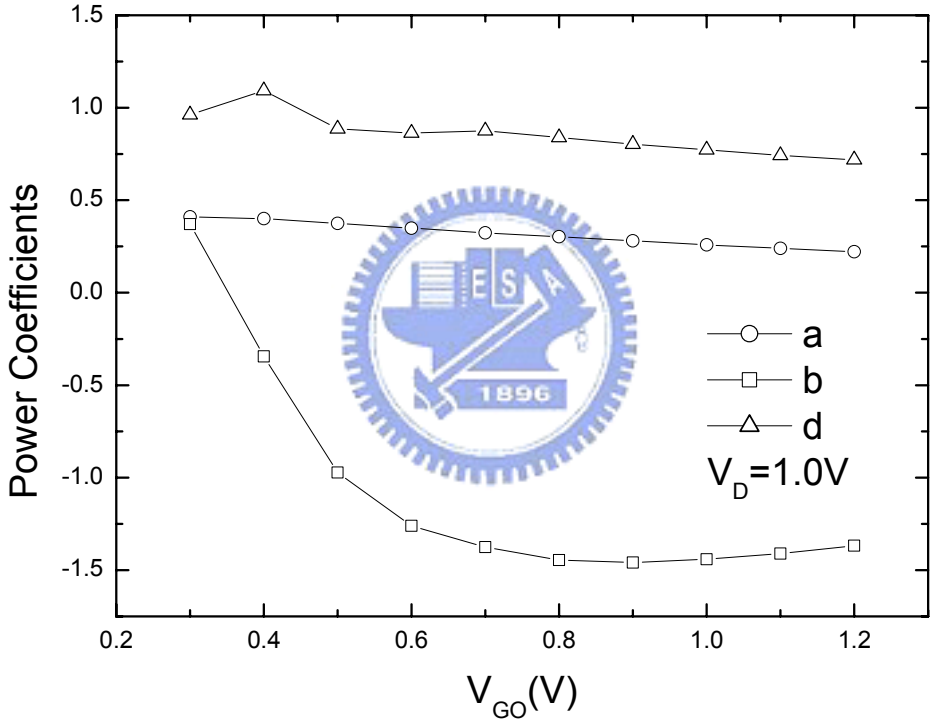
Power Coefficients
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
0.2
0.4
0.6
0.8
1.0
1.2
V_GO(V)
a
b
d
V_D=1.0V

Fig. 17

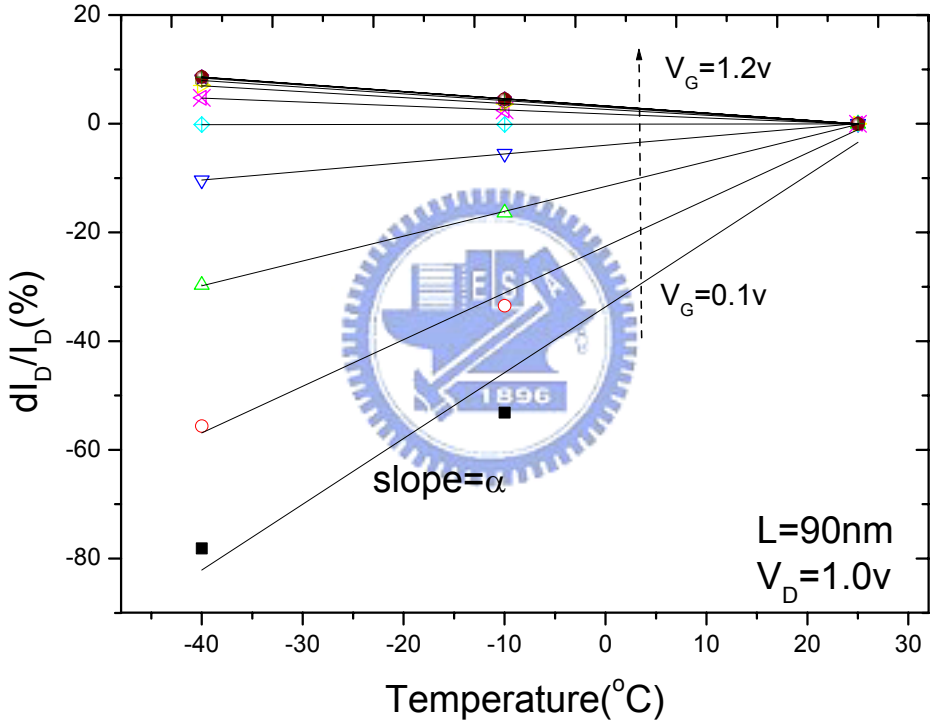
20
0
-20
-40
-60
-80
dI_D/I_D(%)
-40
-30
-20
-10
0
10
20
30
Temperature(°C)
V_G=1.2v
V_G=0.1v
slope=α
L=90nm
V_D=1.0v

Fig. 18

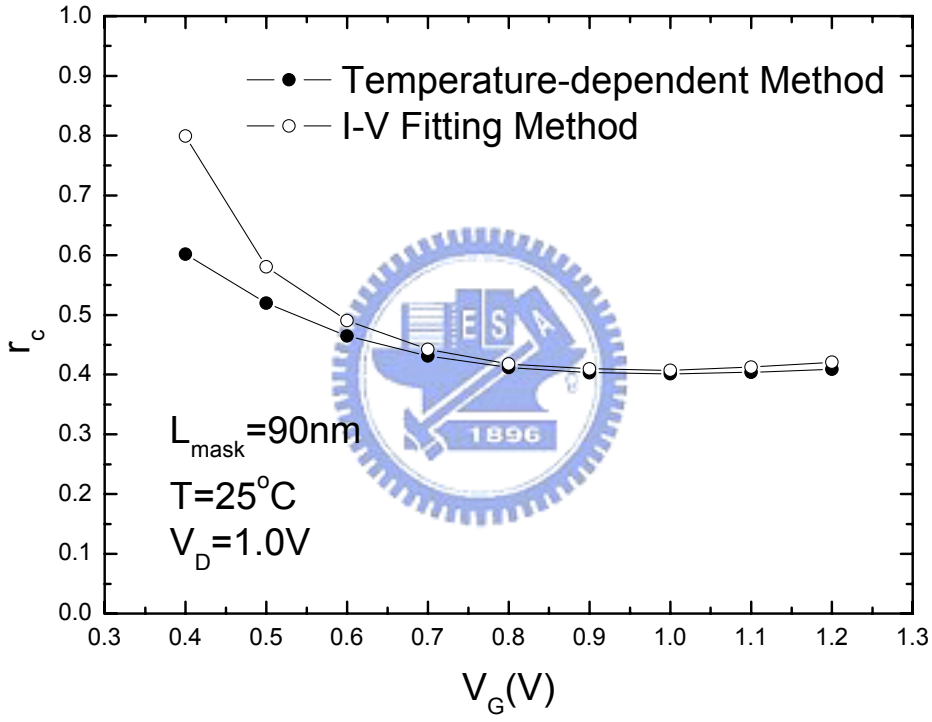
Temperature-dependent Method
I-V Fitting Method
L_{mask}=90nm
T=25°C
V_D=1.0V
r_c
V_G(V)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3

Fig. 19

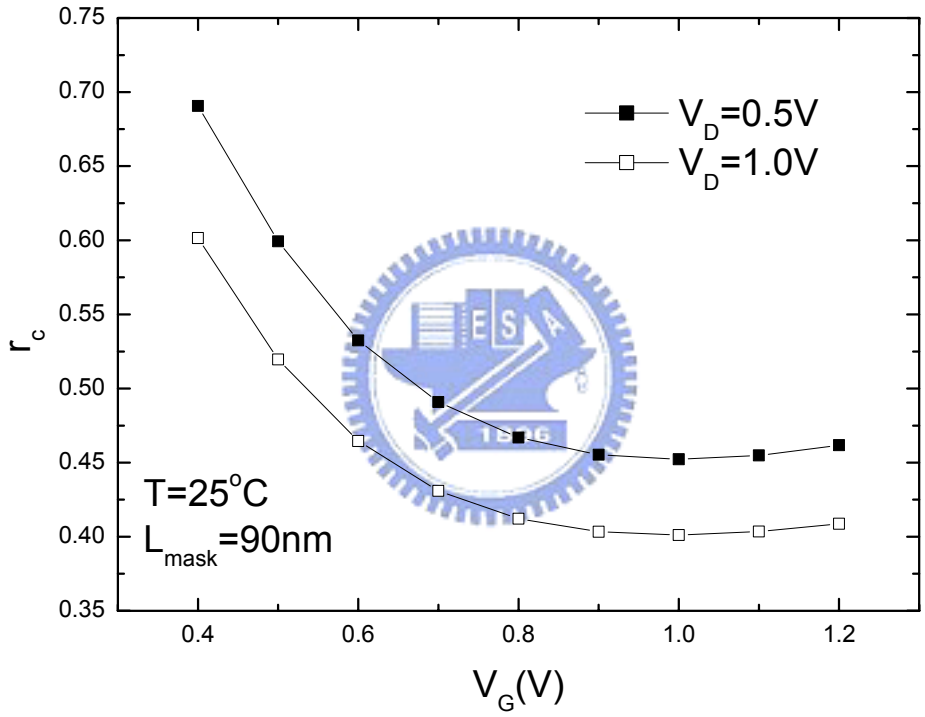
0.75
0.70
0.65
0.60
0.55
0.50
0.45
0.40
0.35
r_c
0.4
0.6
0.8
1.0
1.2
V_G(V)
V_D=0.5V
V_D=1.0V
T=25°C
L_{mask}=90nm

Fig. 20

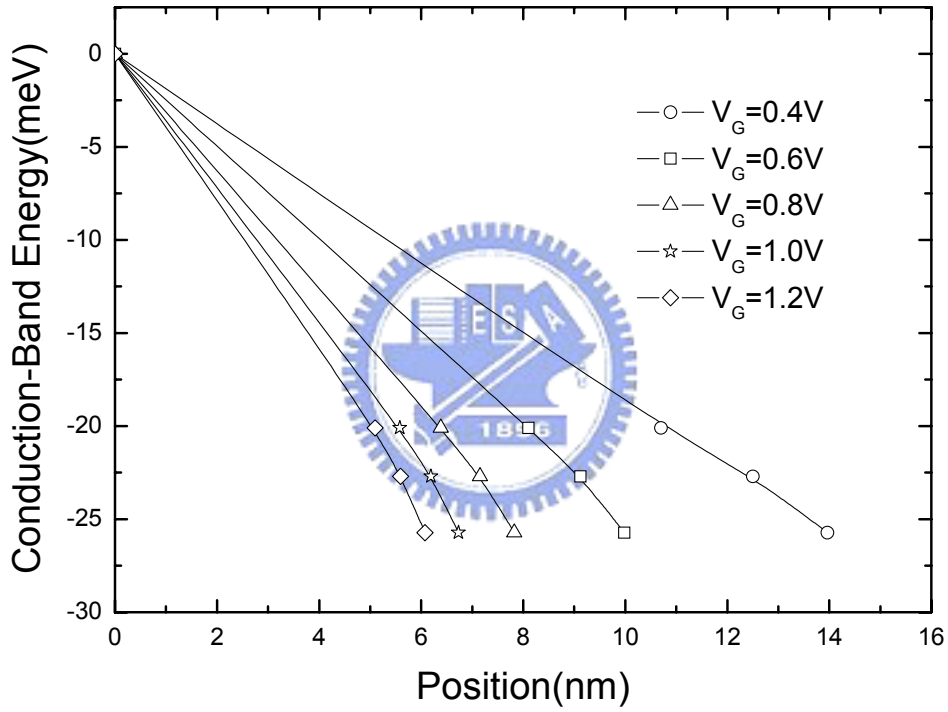
Conduction-Band Energy(meV)
0
-5
-10
-15
-20
-25
-30
0
2
4
6
8
10
12
14
16
Position(nm)
V_G=0.4V
V_G=0.6V
V_G=0.8V
V_G=1.0V
V_G=1.2V

Fig. 21

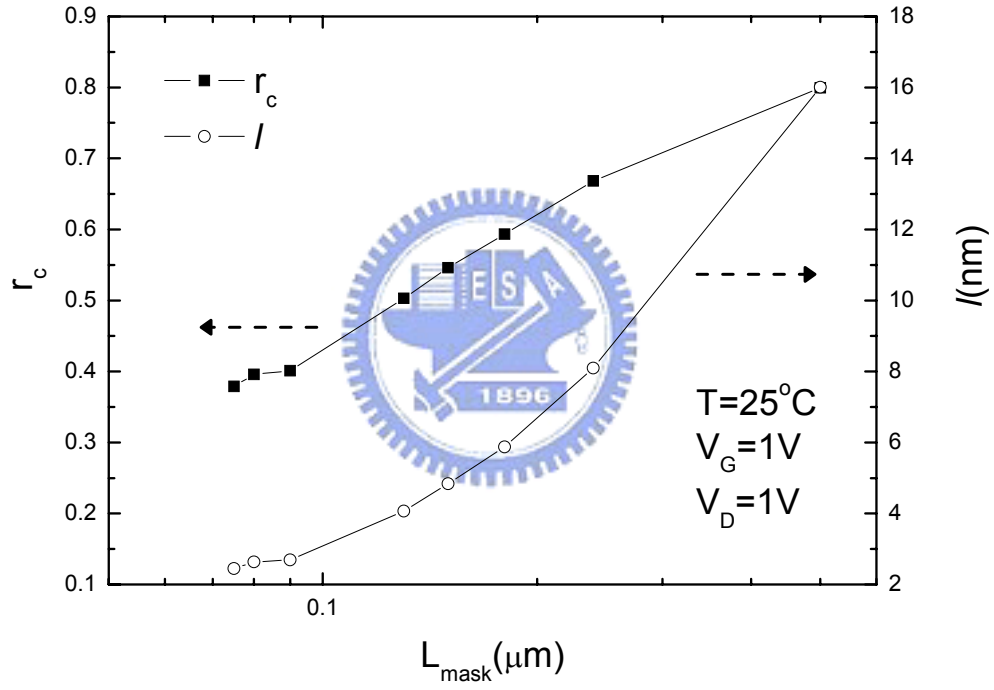
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
r_c
18
16
14
12
10
8
6
4
2
l(nm)
r_c
l
T=25°C
V_G=1V
V_D=1V
0.1
L_{mask}(μm)

Fig. 22