

應用於 IEEE 802.11a/b/g 無線區域網路中 雙頻帶射頻接收器模組電路之設計與實現

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在這篇論文中設計並製作了兩大類的雙頻帶射頻接收器，第一類包含“切換模式”和“並行模式”，而第二類則是由“共存模式”和“寬頻模式”所組成。設計部分完成了 2.4GHz 和 5GHz 頻帶的“切換模式”和“並行模式”前端接受器以及 2.4/5GHz 雙頻帶“共存模式”前端接受器和“寬頻模式”低雜訊放大器。而實作電路則包含一個 5.25GHz 頻帶的射頻前端接受器以及一個“共存式”雙頻帶低雜訊放大器，並採用聯電 0.18 μm 1P6M mixed-mode/RF CMOS 製程，智森高頻元件模組和矽品 QFN 系列封裝。量測結果顯示當前端接收器消耗 30mA 電流的同時，可以提供 18dB 的電壓增益(A_v)，1dB 增益壓縮點(P_{1dB})為-27dBm，三階交調點(IIP3)和二階交調點(IIP2)分別為-3dBm 以及-12dBm，而雜訊指數(NF)則為 6.4dB。低雜訊放大器有 27mW 功率消耗，可同時在 2.4GHz 提供 6.7dB 的功率增益(S_{21})，在 5.25GHz 則為-7.2dB，但由於輸入阻抗匹配的偏移，最大增益點則發生在 2.74GHz，有 11.9dB 以及在 5.25GHz 為-5.1dB。

The Design and Implementation of Dual Band RF Receiver Module for IEEE 802.11a/b/g WLAN Applications

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Abstract

In this thesis, two groups of dual band receiver are designed and fabricated. The first group consists of “switched mode” and “parallel mode”. The other group is composed of “concurrent mode” and “wideband mode”. The circuit design comprises 2.4 GHz and 5 GHz dual band receiver frontend for “switched mode” and “parallel mode”, and 2.4/5 GHz dual band receiver frontend for “concurrent mode” as well as “wideband mode” LNA. The chip implementations include a 5.25 GHz receiver frontend and a concurrent dual band LNA employing UMC 0.18 μ m 1P6M mixed-mode/RF CMOS process, RF device models, and QFN series package provided by Giga-solution and SPIL respectively. The experimental results show that the receiver drains 30 mA of current and achieves the voltage gain of 18 dB, P1dB of -27 dBm, IIP3 of -12 dBm, IIP2 of -3 dBm, and NF of 6.4 dB. The LNA has a power gain of 6.7 dB at 2.4 GHz band, -7.2 dB at 5 GHz band having power dissipation of 18 mW, while the maximum power gain of this LNA is 11.9 dB at 2.74 GHz, -5.1 dB at 5.25 GHz due to the shift of input matching.

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Contents

中文摘要.....	I
Abstract.....	II
誌謝.....	III
Contents.....	IV
List of Tables.....	VI
List of Figures.....	VII
Chapter 1 Introduction.....	1
Chapter 2 System Planning.....	3
2.1 Standard Overview.....	3
2.1.1 IEEE 802.11a.....	3
2.1.2 IEEE 802.11b.....	4
2.1.3 IEEE 802.11g.....	5
2.1.4 Comparisons.....	6
2.2 From Standard to System Specification.....	7
2.2.1 Standard Requirement.....	7
2.2.2 Design Parameters.....	9
2.3 From Receiver Specification to Circuit Specification.....	17
Chapter 3 Receiver Architecture.....	22
3.1 Switched Dual Band Architecture.....	22
3.1.1 Comparisons of Receiver Architectures.....	25
3.2 Concurrent Dual Band Architecture.....	36
Chapter 4 Device Characteristic and RF Modeling.....	44
4.1 Device Characteristic.....	44
4.1.1 Technology Comparisons.....	45
4.2 RF Modeling.....	53
4.2.1 MOSFET Modeling.....	54
4.2.2 Noise Modeling.....	57
4.2.3 Modeling of Passive Devices.....	58
Chapter 5 Circuit Design.....	71
5.1 Low Noise Amplifier.....	71

5.1.1	Topologies.....	72
5.1.2	Power matching.....	73
5.1.3	Noise matching.....	74
5.1.4	Stability.....	76
5.2	Mixer.....	77
5.2.1	Active Mixer.....	77
5.2.2	Passive Mixer.....	78
5.3	Switched Dual Band Receiver.....	80
5.4	Concurrent Dual Band Receiver.....	86
5.5	Wideband LNA.....	91
Chapter 6	Chip Implementation.....	97
6.1	Layout Consideration.....	97
6.2	ESD Protection	102
6.3	Package and Modeling.....	103
Chapter 7	Measurement.....	105
7.1	Testing Plan.....	106
7.1.1	Matching Measurement.....	106
7.1.2	Power Measurement.....	107
7.1.3	Noise Measurement.....	109
7.2	Experimental Results.....	110
7.2.1	Packaged 5 GHz Band Receiver.....	110
7.2.2	On-wafer 5 GHz Band Receiver.....	114
7.2.3	Concurrent 2.4/5 GHz Dual Band LNA.....	117
7.3	Discussion.....	118
Chapter 8	Conclusions.....	121
8.1	Conclusions.....	121
8.2	Future Work.....	122
Appendix-A	Package Data Sheet.....	126
Appendix-B	PCB Data Sheet.....	128
Bibliography		130

List of Tables

Table 2-1 WLAN standard overview -----	6
Table 2-2 Receiver specification of IEEE 802.11a standard -----	8
Table 2-3 Noise Figure versus Data Rate -----	11
Table 2-4 IIP3 versus Data Rate -----	13
Table 2-5 IIP2 versus Data Rate -----	14
Table 2-6 System specification summaries -----	17
Table 2-7 Receiver link budget calculation -----	20
Table 2-8 802.11a/b/g receiver front-end specifications -----	21
Table 5-1 The comparisons between common source and common gate topologies--	73
Table 5-2 Comparisons of some published LNAs at 5 GHz ranges [17] -----	84
Table 5-3 Comparisons between published papers and concurrent dual-band LNA --	88
Table 5-4 The summaries of simulation between switched and concurrent dual-band receiver -----	91
Table 5-5 Comparisons of the ideal and practical wideband LNAs -----	96
Table 7-1 Comparisons between simulation and measurement of 5 GHz receiver frontend -----	117

List of Figures

Fig. 2-1 Channel allocation and power levels of the IEEE 802.11a standard within the UNII band-----	4
Fig. 2-2 IEEE 802.11a data rate versus modulation-----	4
Fig. 2-3 IEEE 802.11b channel location for 2.4GHz ISM band-----	5
Fig. 2-4 Receiving band distribution of WLAN in the range of 2.4~6 GHz-----	7
Fig. 2-5 Adjacent channel rejection example-----	9
Fig. 2-6 (a)IP3 curve (b)Desired signal corrupted by third order intermodulation----	11
Fig. 2-7 Interference specification in WLAN 802.11b receiver-----	16
Fig. 2-8 Out-of-band emission specification in WLAN 802.11b receiver-----	16
Fig. 2-9 Out-of-band blocking specification in WLAN 802.11b receiver-----	16
Fig. 2-10 Intermodulation specification in WLAN 802.11b receiver-----	17
Fig. 2-11 Behavior simulation of 802.11a standard-----	21
Fig. 2-12 Behavior simulation of 802.11b/g standard-----	21
Fig. 3-1 Switched dual-band receiver (a)Switched mode (b)Parallel mode-----	24
Fig. 3-2 Dual-IF heterodyne receiver-----	26
Fig. 3-3 (a)Image problem (b)The function of image reject filter-----	26
Fig. 3-4 Conceptual architecture of a switched dual-band receiver [16] -----	27
Fig. 3-5 (a)Simple direct-conversion receiver (b)Direct-conversion receiver with quadrature downconversion-----	28
Fig. 3-6 DC offsets in direct conversion receiver-----	29
Fig. 3-7 DC offset cancellation techniques-----	29
Fig. 3-8 Effect of even-order distortion-----	30
Fig. 3-9 Signal constellations due to gain and phase mismatch-----	31
Fig. 3-10 Effect of I/Q phase imbalance on demodulated QPSK data-----	32
Fig. 3-11 Power spectral density of flicker noise-----	33
Fig. 3-12 The proposed switched dual-band architecture-----	33
Fig. 3-13 Hartley image-reject receiver-----	34
Fig. 3-14 Weaver image-reject receiver-----	34
Fig. 3-15 Dual-band implementation of the Weaver architecture [13] -----	35
Fig. 3-16 Dual-band direct-conversion architecture (wideband mode) [15] -----	37
Fig. 3-17 Evolution process of two parallel receivers to a concurrent dual-band receiver [11] -----	38

Fig. 3-18 An architecture for the concurrent dual-band receiver employing image rejection [11] -----	38
Fig. 3-19 Frequency-domain signal evolution of the concurrent dual-band receiver in Fig. 3-18 [11] -----	40
Fig. 3-20 Evolution process of concurrent dual-band direct-conversion receiver-----	42
Fig. 3-21 Block diagrams of concurrent dual-band direct-conversion receiver (concurrent mode) -----	42
Fig. 3-22 Downconversion operation of concurrent dual-band direct-conversion receiver-----	43
Fig. 4-1 The definition of f_t -----	46
Fig. 4-2 The definition of f_{max} -----	47
Fig. 4-3 Comparison of f_t and f_{max} versus Collector/Drain current and voltage[29]-	47
Fig.4-4 The illustration of thermal noise-----	48
Fig.4-5 The model of thermal noise -----	48
Fig. 4-6 The illustration of shot noise -----	49
Fig. 4-7 The illustration of shot noise -----	49
Fig. 4-8 The characteristic of flicker noise -----	51
Fig. 4-9 (a)Noise model of BJT (b)Noise model of MOSFET- -----	51
Fig. 4-10 Gain-to-DC power ratio plotted versus noise figure for 2-GHz LNA [29]--	52
Fig. 4-11 Linearity versus DC power for 2-GHz LNA [29] -----	52
Fig. 4-12 (a)Distributed transmission line effect on the gate (b)Channel induced gate resistance -----	54
Fig. 4-13 Elmore non-quasi-static equivalent circuit -----	56
Fig. 4-14 RF N/P MOSFET extension model of UMC 0.18 μ m mixed-mode/RF CMOS process -----	56
Fig. 4-15 An equivalent circuit to illustrate the noise source in a MOSFET -----	57
Fig. 4-16 Equivalent circuit of a well resistor -----	59
Fig. 4-17 Layout and equivalent circuit of N+/P+ non-salicyded poly resistor in UMC 0.18 μ m mixed-mode/RF CMOS process -----	61
Fig. 4-18 Circuit model of resistors -----	62
Fig. 4-19 Vertical cross section of a poly-poly capacitor structure -----	63
Fig. 4-20 (a)Top view of a fringe capacitor with fractal geometry and equivalent lumped circuit model -----	64
(b)Cross-section view of fringe capacitor using five metal layers -----	65
Fig. 4-21 Cross section view of general MIM capacitor with equivalent circuit model -----	65

Fig. 4-22 Cross section view of MIM capacitor with equivalent circuit model by UMC 0.18 μ m CMOS process -----	65
Fig. 4-23 Capacitance-voltage characteristics and circuit model of MOS capacitor--	65
Fig. 4-24 Layout and equivalent model of spiral inductor -----	67
Fig. 4-25 The illustration of eddy current -----	68
Fig. 4-26 Two-layer stacked inductor [16] -----	68
Fig. 4-27 Patterned ground shield -----	68
Fig. 4-28 Monolithic transformer (a)Physical layout (b)Schematic symbol -----	69
Fig. 4-29 (a)Planar transformer layout (b)Transformer model -----	70
Fig. 4-30 Stacked transformer [17] -----	70
Fig. 5-1 Commonly used single-band CMOS LNAs (a)Common-gate (b)Common-source with inductive degeneration -----	73
Fig. 5-2 Inductively degenerated LNA -----	74
Fig. 5-3 Trade off between power matching and noise matching -----	76
Fig. 5-4 (a)Single balanced mixer (b)Double balanced mixer -----	78
Fig. 5-5 Passive mixer -----	79
Fig. 5-6 (a)Time varying conductance model for passive mixer (b)Thevenin model of (a) -----	79
Fig. 5-7 Topologies of receiver frontend in this design -----	80
Fig. 5-8 2.4 and 5 GHz LNA circuits -----	81
Fig. 5-9 S-parameter and noise figure simulation of switched dual-band LNA-----	82
Fig. 5-10 Compromise between gain and NF simulation of switched dual-band LNA-----	82
Fig. 5-11 Stability factor of switched dual-band LNA -----	83
Fig. 5-12 Linearity simulation of switched dual-band LNA -----	83
Fig. 5-13 The simulation of 5 GHz mixer -----	85
Fig. 5-14 Simplified receiver circuit -----	85
Fig. 5-15 The simulation of switched dual-band receiver circuit -----	86
Fig. 5-16 NF simulation of switched dual-band receiver circuit at IF=5 MHz-----	86
Fig. 5-17 Simplified concurrent dual-band LNA -----	87
Fig. 5-18 The S-parameter and NF simulation (concurrent dual-band LNA) -----	88
Fig. 5-19 The input matching of differential RF and LO port (concurrent dual-band receiver) -----	89
Fig. 5-20 The gain and P1dB simulation (concurrent dual-band receiver) -----	89
Fig. 5-21 NF simulation of concurrent dual-band receiver at IF = 5 MHz -----	90
Fig. 5-22 IP3 and IP2 simulation of concurrent dual-band receiver -----	90
Fig. 5-23 The ideal wideband LNA covering 2.4 and 5 GHz -----	92

Fig. 5-24 Matching techniques of a wideband LNA -----	92
Fig. 5-25 The S-parameter and NF simulation of the ideal wideband LNA-----	93
Fig. 5-26 IP3 simulation of the ideal wideband LNA -----	93
Fig. 5-27 Capacitor-tapped impedance transformation technique -----	94
Fig. 5-28 The practical wideband LNA covering 2.4 and 5 GHz -----	94
Fig. 5-29 S-parameter & NF simulation of the practical wideband LNA -----	95
Fig. 5-30 IP3 simulation of the practical wideband LNA -----	95
Fig. 6-1 Fabricated circuits in this thesis -----	97
Fig. 6-2 Common centroid layout -----	98
Fig. 6-3 (a)5GHz receiver frontend (packaged) (b)2.4/5GHz dual-band LNA(packaged) -----	98
Fig. 6-4 Parasitic effects caused by microstrip discontinuities -----	99
Fig. 6-5 The PCB layout technique -----	100
Fig. 6-6 The EM simulation of a 180° balun -----	100
Fig. 6-7 The phase and impedance measurements of a 180° balun -----	101
Fig. 6-8 Board design of (a)5GHz receiver frontend (b)2.4/5GHz dual-band LNA -----	102
Fig. 6-9 ESD protection circuits -----	103
Fig. 6-10 I-V characteristic of gate-grounded NMOS -----	103
Fig. 6-11 Package model -----	103
Fig. 6-12 Pin-to-Pin isolation for package model -----	104
Fig. 7-1 Measurement environment -----	105
Fig. 7-2 Matching measurement setup -----	106
Fig. 7-3 Power measurement setup -----	108
Fig. 7-4 (a)The comparison between the two measurement conditions for packaged 5 GHz Rx -----	108
(b)The comparison between the two measurement conditions for on-wafer 5 GHz Rx -----	109
Fig. 7-5 Noise measurement setup -----	110
Fig. 7-6 Gain & P1dB measurement of packaged 5 GHz receiver -----	111
Fig. 7-7 (a)IP3 measurement of packaged 5 GHz receiver -----	112
(b)IP2 measurement of packaged 5 GHz receiver -----	113
Fig. 7-8 Noise figure measurement of packaged 5 GHz receiver -----	113
Fig. 7-9 (a)RF port matching of differential 5 GHz receiver (b)LO port matching of differential 5 GHz receiver-----	114
Fig. 7-10 Gain&P1dB measurement of on-wafer 5 GHz receiver -----	115

Fig. 7-11 (a)IP3 measurement of on-wafer 5 GHz receiver -----	115
(b)IP2 measurement of on-wafer 5 GHz receiver -----	116
Fig. 7-12 Noise figure measurement of on-wafer 5 GHz receiver -----	116
Fig. 7-13 S-parameter measurement of concurrent dual band LNA -----	117
Fig. 7-14 Bond wire used as source inductor of LNA -----	118
Fig. 7-15 Inductance of two wires as a function of spacing -----	118
Fig. 7-16 Layout issues of on-wafer 5 GHz receiver -----	119
Fig. 7-17(a) 3-port inductor (b) Monolithic transformer -----	120
Fig. 7-18 Device modeling flow -----	120
Fig. 8-1 IP-revise design mythology proposed in this thesis -----	124
Fig. 8-2 The interconnection between 5 GHz receiver and 5 GHz synthesizer -----	125
Fig. 8-3 The measurement of connecting 5 GHz receiver and 5 GHz synthesizer design -----	125
Fig. 8-4 Embed VCO into receiver frontend -----	125

