Chapter 1

Introduction

1.1 Motivation

Wireless services industry has experienced a tremendous growth in the past few years. Mobile cellular and home cordless telephones are fast becoming a part of our daily lives. The wireless local area network (WLAN) communication is becoming popular as well. The IEEE 802.11a, which is based on orthogonal frequency division multiplexing (OFDM) modulation, provides nearly five times the data rate and as much as ten times the overall system capacity as currently available 802.11b wireless LAN systems. The 802.11a standard operates in the 5-GHz unlicensed national information infrastructure (UNII) band, which provides a total available signal bandwidth of 300 MHz, as compared to the 83.5 MHz available for 802.11b. The IEEE 802.11g standard, an extended version of IEEE 802.11b, has come out in 2003 and hence multi-mode WLAN applications have recently emerged in the market. Therefore, the dual-band receiver front-end circuits which correspond to IEEE 802.11a/b/g standard are designed and implemented in this thesis. The circuits are developed according to both switched and concurrent dual-band architectures.

1.2 Thesis Organization

This thesis is organized as follows:

Chapter 2 is an overview of the WLAN standard and the specification is derived in aspects of system and circuit respectively according to the 802.11/a/b/g standard. Chapter 3 deals with some common receiver architectures, introducing various topologies and presenting the switched and concurrent dual-band architecture. Chapter 4 emphasizes the importance of device characterization and RF modeling. Based on the circuit specification derived in chapter 2, chapter 5 delves into the circuit aspects of 2.4&5 GHz receiver front-end, concurrent dual-band receiver and wide-band LNA. Chapter 6 deals with chip implementation and discusses the testing plan, layout issues, and EM simulation. Chapter 7 shows the measurement results and analyzes the causes of mismatch between simulation and experiment. Chapter 8 describes the future work based on the concept of RF-SOC and the special design methodology in this thesis is explained.

Chapter 2
System Planning

The 802.11b standard at the 2.4 GHz ISM band provides data rates up to 11 Mbps with the direct sequence spread spectrum (DSSS). This technology first appeared in the market in 1999. The 802.11a standard, released by IEEE in 1999, is based on an orthogonal frequency division multiplexing (OFDM) modulation technology with data rate up to 54 Mbps in the 5 GHz band. The 802.11a standard entered the market with first end-user products in early 2002. Recently the IEEE extended the 802.11b standard to higher data rates up to 54 Mb/s by using the OFDM modulation of the 802.11a standard in the 2.4 GHz band, resulting in the new standard 802.11g. In the next section, IEEE 802.11a/b/g standard will be briefly described respectively.

2.1 Standard Overview

2.1.1 IEEE 802.11a

As illustrated in Fig.2-1, the 802.11a standard supports channel bandwidths of 20 MHz, with each channel being an OFDM modulated signal consisting of 52 subcarriers. Each of the subcarriers can be either a BPSK, QPSK, 16QAM, 64QAM signal. The data rate versus modulation scheme is shown in Fig. 2-2. The composite

radio frequency (RF) signal has a data rate of up to 54 Mb/s in 20-MHz channel. A huge problem with 802.11a is that it's not directly compatible with 802.11b or 802.11g networks. In other words, a user equipped with an 802.11b or 802.11g radio card will not be able to interface directly to an 802.11a access point. The superior performance of 802.11a offers excellent support for bandwidth hungry applications, but its spectral efficiency comes at the expense of a more complicated transceiver with strict requirements on the radio performance.

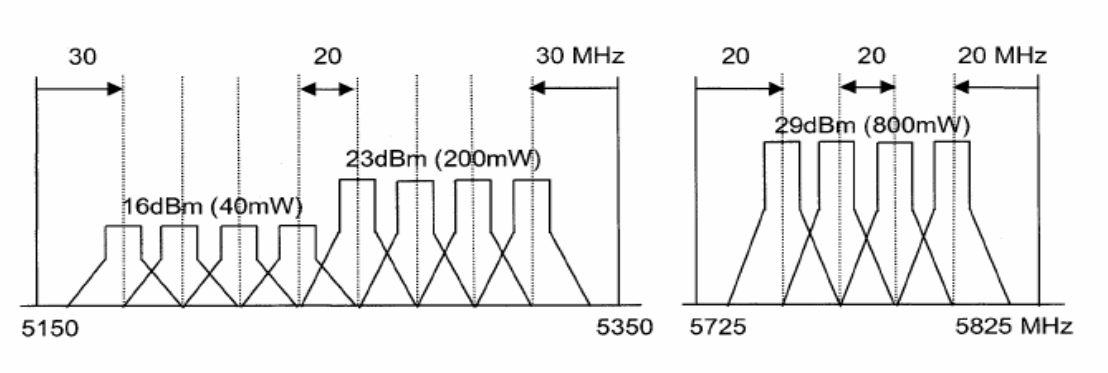


Fig. 2-1 Channel allocation and power levels of the IEEE 802.11a standard within the UNII band

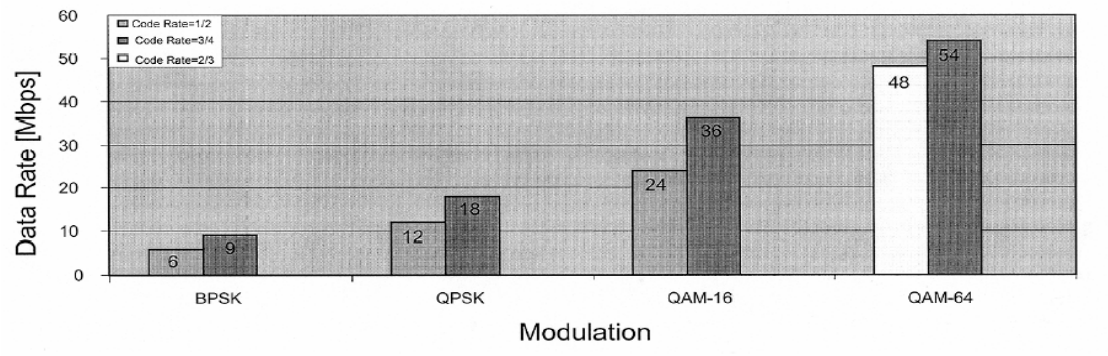


Fig. 2-2 IEEE 802.11a data rate versus modulation

2.1.2 IEEE 802.11b

The 802.11b standard operates in the 2.4GHz range and offers a data speed up

to 11Mbps. While slower than 802.11a, 802.11b is still as fast as 10BaseT Ethernet service. 802.11b uses direct sequence spread spectrum (DSSS) and complementary code keying (CCK) modulation. Fig. 2-3 shows the channel location of IEEE 802.11b standard.

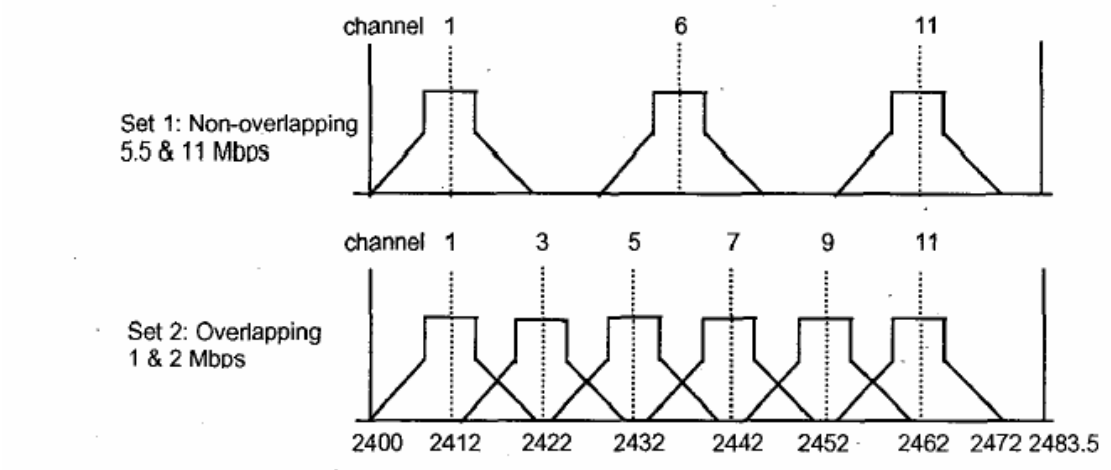


Fig. 2-3 IEEE 802.11b channel location for 2.4GHz ISM band

2.1.3 IEEE 802.11g

802.11g is an extension to 802.11b, the basis of the majority of wireless LANs in existence today. 802.11g will broaden 802.11b's data rates to 54 Mbps within the 2.4 GHz band using OFDM (orthogonal frequency division multiplexing) technology. Similar to 802.11b, 802.11g operates in the 2.4GHz band, and the transmitted signal uses approximately 30MHz, which is one third of the band. This limits the number of non-overlapping 802.11g access points to three, which is the same as 802.11b. This means that you'll have the same difficulty with 802.11g channel assignment as you do with 802.11b when covering a large area where there is a high density of users. A big

issue with 802.11g, which also applies to 802.11b, is considerable RF interference from other 2.4 GHz devices, such as the newer cordless phones.

2.1.4 Comparisons

The comparison of IEEE 802.11a/b/g standard is listed in Table 2-1. Fig. 2-4 illustrates the receiving band distribution of current wireless communication standards in the range of 2.4GHz~6GHz. With so many communication standards, one may consider to develop multi-functional devices, which can operate at several bands and different modes. Therefore, to migrate from an installed 802.11b network to 802.11g and maintain a high degree of interoperability. The dual-band 802.11a/b/g network will eventually help eliminate the interoperability issues, and is also the design objective in this thesis.

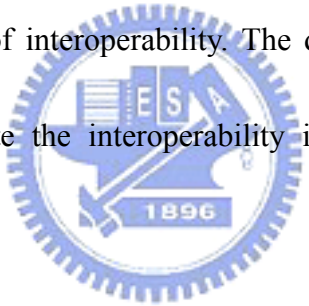


Table 2-1 WLAN standard overview

Mode	Data rate (Mbps)	Modulation scheme	Frequency (GHz)	non-overlapping channels	Channel spacing (MHz)	Available Spectrum (MHz)
802.11a	6-54	OFDM	5.150 - 5.350 5.725 - 5.825	27	20	300
802.11b	1-11	CCK	2.400 - 2.4835	3	25	83.5
802.11g	6-54	OFDM	2.400 - 2.4835	3	25	83.5
	1-11	CCK	2.400 - 2.4835	3	25	83.5

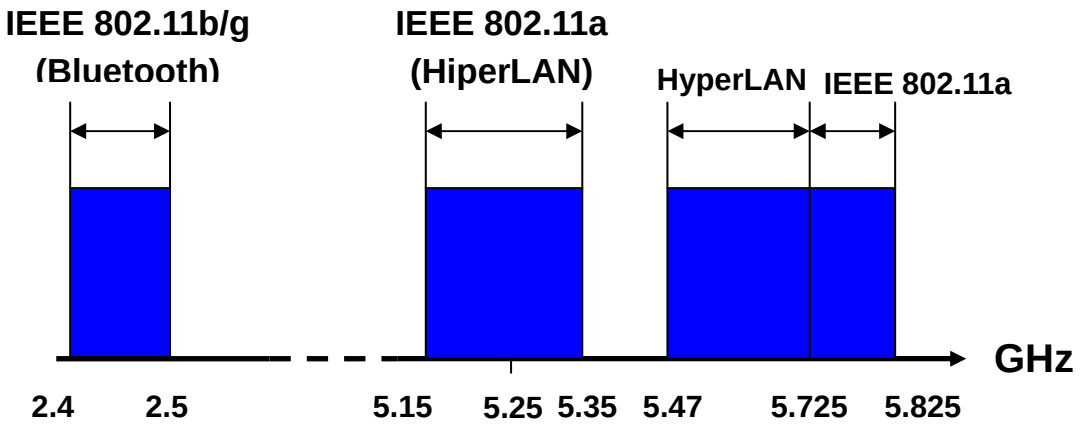


Fig. 2-4 Receiving band distribution of WLAN in the range of 2.4~6 GHz

2.2 From Standard to System Specification

The 802.11a/b/g standard specifies receiver minimum input level sensitivity, maximum input level, and adjacent channel rejection; therefore, the requirements of the standard are systematically mapped onto a set of measurable specifications for a receiver front-end. In the following subsection, the way how the system specification is derived will be verified.

2.2.1 Standard Requirement

A. Receiver minimum input level sensitivity

802.11a standard specifies minimum input power at the antenna connector for packet error rate < 10%, and the data rate versus sensitivity is listed in Table 2-2

Table 2-2 Receiver specification of IEEE 802.11a standard

Data rate (Mbits/s)	Minimum sensitivity (dBm)	Adjacent channel rejection (dB)	Alternate adjacent channel rejection (dB)
6	–82	16	32
9	–81	15	31
12	–79	13	29
18	–77	11	27
24	–74	8	24
36	–70	4	20
48	–66	0	16
54	–65	–1	15

–76 dBm at antenna port for frame error ratio (FER)< 8×10^{-2} is the sensitivity requirement specified by 802.11b. According to the the extended rate PHY (ERP), 802.11g has different requirement. If the ERP is OFDM, 802.11g is the same as 802.11a, while if the ERP is DSSS (direct sequence spread spectrum), 802.11g is the same as 802.11b.

B. Adjacent/Non-adjacent Channel Rejection

802.11a standard specifies that the adjacent channel rejection shall be measured by setting the desired signal's strength 3 dB above the rate-dependent sensitivity specified in Table 2-2. Take data rate 6 Mbps for example; Fig. 2-5 illustrates the relation between sensitivity and adjacent channel.

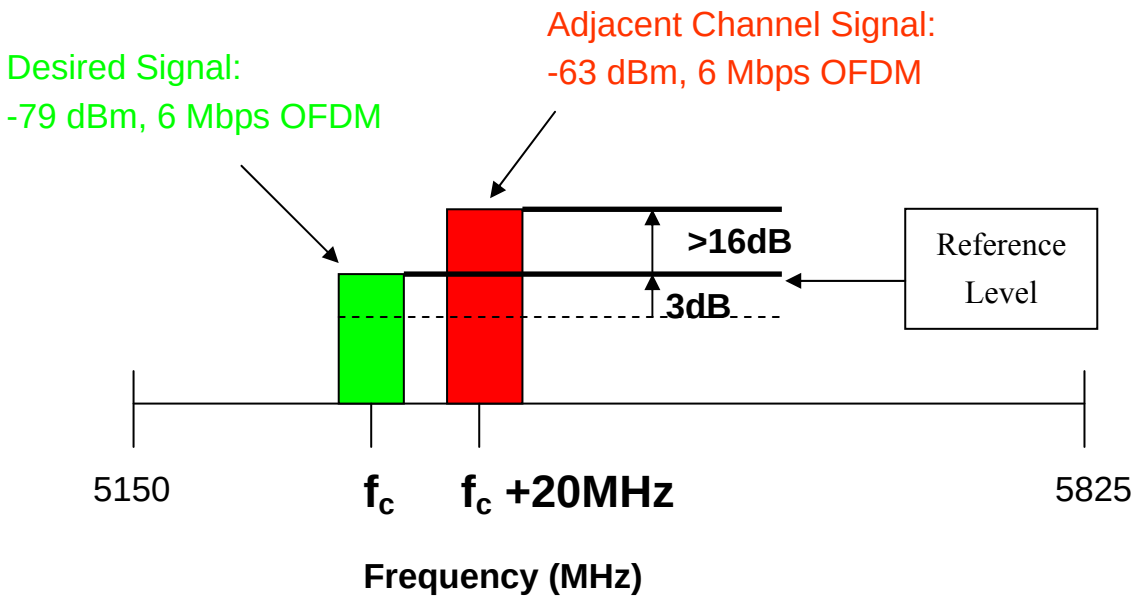


Fig. 2-5 Adjacent channel rejection example

In a similar way, 802.11b specifies that the adjacent channel rejection shall be equal to or better than 35 dB. Regarding 802.11g, the corresponding rejection shall be no less than that specified in IEEE802.11a for OFDM PHY, and should follow 802.11b for DSSS PHY.

C. Receiver Maximum Input level

The maximum input level specified by 802.11a/b/g is -30 dBm, -10 dBm and -20dBm measured at the antenna connector respectively.

2.2.2 Design Parameters

The next step is to translate the above-mentioned standard requirements to the key design parameters, such as noise figure (NF), IIP3, IIP2 and spurious free dynamic range (SFDR).

A. NF

The total noise figure of the cascaded chain is shown as Eq. (2-1), which is called Friis formula. As the equation indicates, the preceding stage dominates the system noise performance.

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1}A_{p2}\cdots A_{p(m-1)}} \quad (2\text{-}1)$$

The sensitivity of an RF receiver, which is defined as the minimum signal level that the system can detect with acceptable signal-to-noise ratio (SNR). Based on IEEE 802.11a standard, the minimum sensitivity is -82dBm when data rate is 6Mb/s, and the minimum SNR requirement is 6.5dB by simulation. Therefore, noise figure can be calculated as 12.5dB by Eq. (2-2).

$$Sensitivy = -174dBm/Hz + 10\log_{10}(Bandwidth) + NF + SNR_{\min} \quad (2\text{-}2)$$

The SNR_{min}, which is determined by the maximum packet error rate (PER) of 10% at a PSDU length of 1000 bytes for rate-dependent input levels. Table 2-3 lists the requirements of noise figure versus all the data rates specified by 802.11a.

TABLE 2-3
Noise Figure versus Data Rate

Data Rate (Mbits/sec)	SNR_{min} (dB) (by simulation)	Sensitivity (dBm)	Noise Figure
6	6.5	-82	12.5
9	9.04	-81	11
12	6.5	-79	15.5
18	10.8	-77	13.5
24	12.6	-74	14.4
36	17.35	-70	13.65
48	18.15	-66	16.85
54	23.31	-65	12.69

B. IIP3

Due to intermodulation, the large signal in adjacent channel may induce interference into the operation channel. In IEEE 802.11a WLAN standard, it clearly specifies the adjacent channel rejection ratio, as listed in Table 2-2. Therefore, the adjacent/non-adjacent channel rejection ratio decides the IP3 system specification. The IP3 is defined as the interception point when the linear fundament term is just covered by the nonlinear third-order term due to the intermodulation of two-tone test. The IP3 curve and its effect is illustrated in Fig. 2-6 (a) and (b).

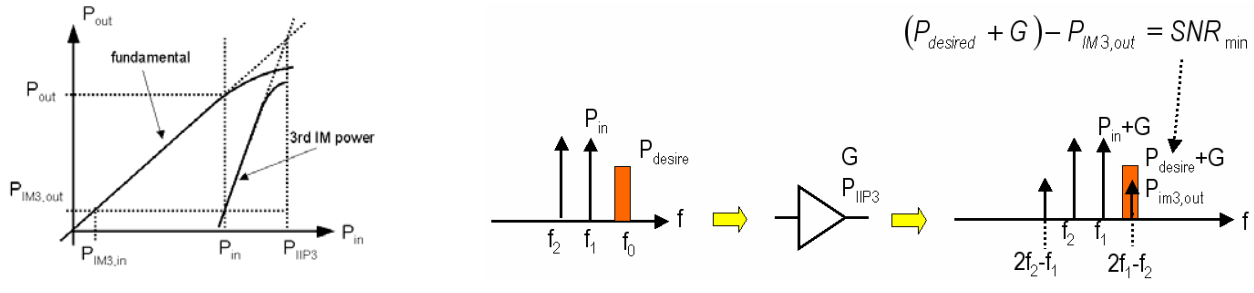


Fig. 2-6 (a) IP3 curve (b) Desired signal corrupted by third order intermodulation

The linearity of the cascaded stages can be easily proven as following:

$$\frac{1}{P_{IIP3}} = \frac{1}{P_{IIP3,1}} + \frac{A_{p1}}{P_{IIP3,2}} + \frac{A_{p1}A_{p2}}{P_{IIP3,3}} + \cdots \tag{2-3}$$

The Eq. (2-3) reveals that the more latter stage requires higher P_{IIP3} to maintain the system linearity, and the larger gain in former stage will cause difficulty designing latter stages. It results in the trade-off in gain design of LNA between noise figure and linearity. Fig. 2-6 shows that the input IP3 (P_{IIP3}) has the significant relation with 3rd order intermodulation term and input power, as shown in Eq. (2-4)

$$\begin{aligned} P_{IIP3} &= P_{in} + \frac{P_{out} - P_{IM3,out}}{2} \\ &= P_{in} + \frac{(P_{in} + G) - (P_{IM3,in} + G)}{2} \\ &= \frac{3P_{in} - P_{IM3,in}}{2} \\ &= \frac{3P_{in} - P_{desired} + SNR_{\min}}{2} \end{aligned} \tag{2-4}$$

where G is system gain. By Eq. (2-4), the P_{IIP3} can be calculated, as listed in Table 2-4.

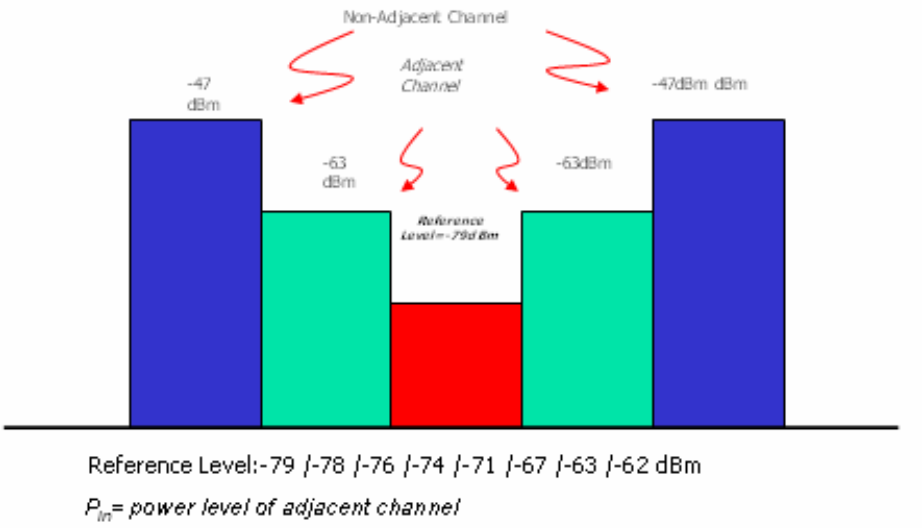


Table 2-4 IIP3 versus Data Rate

Data rate (Mbps)	Modulation & Coding Rate	Reference Level ($P_{desired}$)(dBm)	Required SNR (SNR_{min}) (dB)	Caculated IIP3 (@20MHz)
6	BPSK 1/2	-79	6.5	-51.75dBm
9	BPSK 2/3	-78	9.04	-50.98dBm
12	QPSK 1/2	-76	6.5	-53.25dBm
18	QPSK 3/4	-74	10.8	-52.1dBm
24	16-QAM 1/2	-71	12.6	-52.7dBm
36	16-QAM 3/4	-67	17.35	-52.325dBm
48	64-QAM 1/2	-63	18.15	-53.925dBm
54	64-QAM 3/4	-62	23.31	-51.845dBn

C. IP2

Typical RF receivers are susceptible to only odd-order intermodulation effects. In direct conversion, on the other hand, even-order distortion also becomes problematic. Second-order nonlinearity can be characterized using the “second order intercept point”. In a manner similar to the definition of the third order intercept point, two equal-amplitude interferers are applied at the input and their low-frequency beat signal is observed at the output. Plotting the beat signal power versus the input power

and extrapolating the results yield the IP2. Analogous to the derivations of IIP3 system specification, the IIP2 specification is characterized by Eq. (2-5) and derived in Table 2-5.

$$P_{IIP2} = 2P_{in} - P_{desired} + SNR_{\min} \tag{2-5}$$

TABLE 2-5
IIP2 versus Data Rate

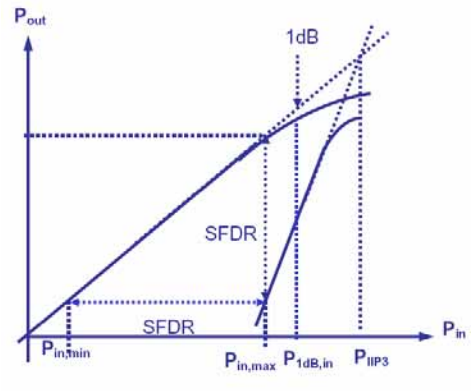
Data rate (MBits/s)	Modulation & Coding Rate	Reference Level (dBm)	Required SNR (dB)	Caculated IIP2 (@20MHz)
6	BPSK 1/2	-79	6.5	-40.5dBm
9	BPSK 2/3	-78	9.04	-38.96dBm
12	QPSK 1/2	-76	6.5	-43.5dBm
18	QPSK 3/4	-74	10.8	-41.2dBm
24	16-QAM 1/2	-71	12.6	-42.4dBm
36	16-QAM 3/4	-67	17.35	-41.65dBm
48	64-QAM 1/2	-63	18.15	-44.85dBm
54	64-QAM 3/4	-62	23.31	-40.69dBm

D. SFDR

Dynamic range(DR) is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit provides a reasonable signal quality. This definition is quantified in different applications differently. In RF design, we base the definition of the upper end of the dynamic range on the intermodulation behavior and the lower end on the sensitivity.

Such a definition is called the “spurious-free dynamic range” (SFDR), shown in Eq. (2-6).

$$SFDR = \frac{2(P_{IIP3} - F)}{3} - SNR_{\min} \qquad (2\text{-}6)$$
$$= P_{in,\max} - P_{in,\min}$$



E. 1 dB compression point

The “1-dB compression point”, is defined as the input signal level that causes the small-signal gain to drop by 1 dB. The P1dB specification is approximately 10 dB below the IIP3 specification listed in Table 2-4.

In a manner similar to the definition of the 802.11a standard, the 802.11b/g system specification can be derived. Fig. 2-7~10 shows the specification of interference, out-of-band emission, out-of-band blocking and intermodulation in 802.11b. Table 2-6 makes a summarization of the 802.11a/b/g system specification. Compared with what’s derived in the preceding paragraphs, the following specification is revised for design margin consideration.

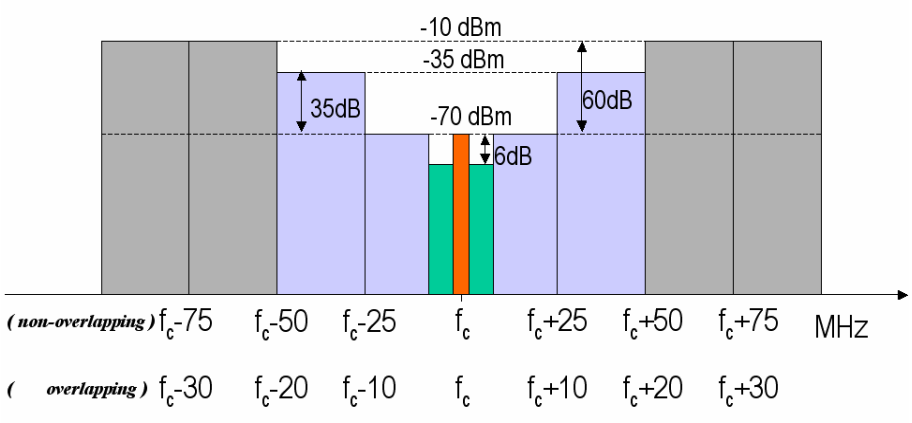


Fig. 2-7 Interference specification in WLAN 802.11b receiver

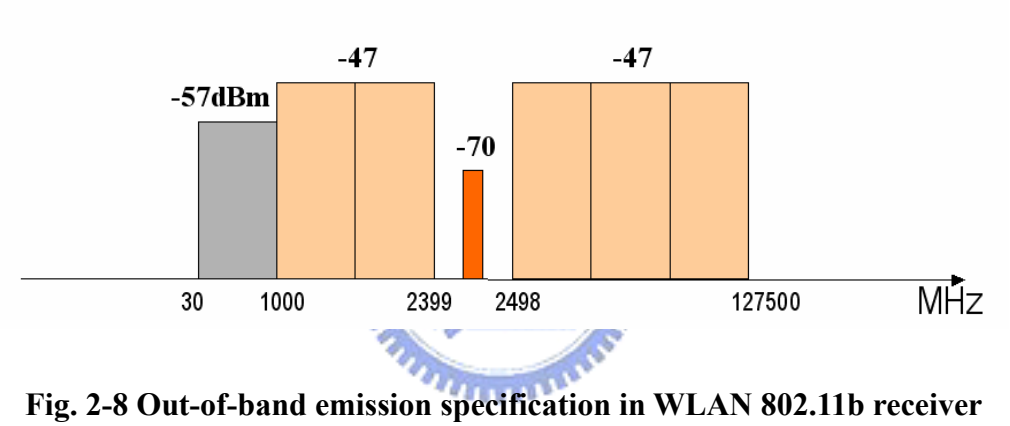


Fig. 2-8 Out-of-band emission specification in WLAN 802.11b receiver

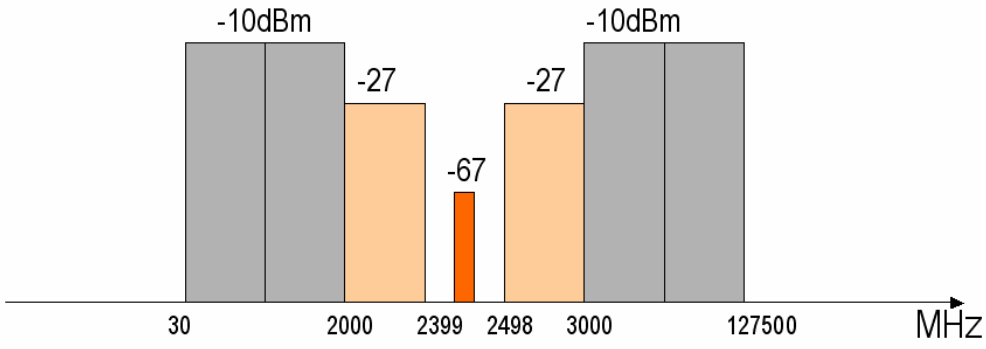


Fig. 2-9 Out-of-band blocking specification in WLAN 802.11b receiver

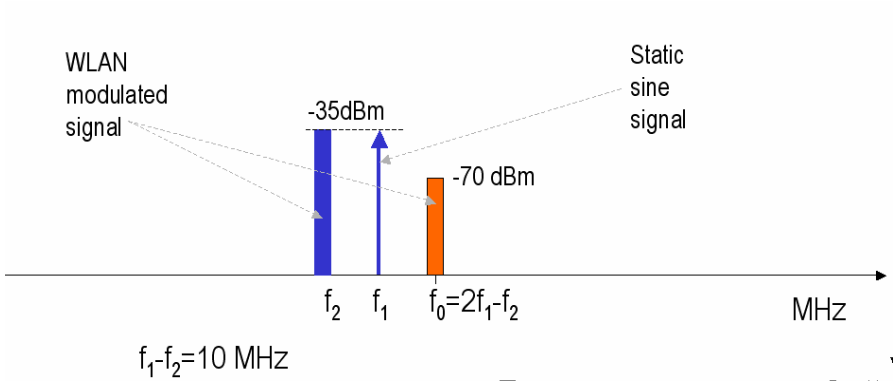


Fig. 2-10 Intermodulation specification in WLAN 802.11b receiver

Table 2-6 System specification summaries

Stand. / Spec.	802.11a	802.11b/g
Noise Figure	10dB	9dB
IIP3	-40dBm	-20dBm
IIP2	-30dBm	-10dBm
P1dB	-50dBm	-30dBm

2.3 From Receiver Specification to Circuit Specification

In this section, it is shown how the receiver specifications are assigned to the different building blocks according to link budget analysis. Link budget analysis ensures that the system composed of individual circuit blocks fits the system specification and consequently, each circuit has to be designed based on these circuit specifications. Prior to behavior simulations, the key design concepts of individual blocks will be briefly explained.

A. Low Noise Amplifier

The LNA gain is set by two considerations:

1. The gain must be large enough in order to bring the smallest possible wanted signal sufficiently above the noise floor of the mixers.

2. The gain must be low enough in order to make sure that the down-converters are not saturated by the amplified blocking signal.

The LNA gain needs to be set carefully. Even when the input capability of the mixer is larger, it is not recommended to further increase the LNA gain. Achieving high gains requires either a lot of current in the LNA or a high-Q LC tank, which makes the LNA sensitive to process variations. In addition, a higher gain inevitable toughens the linearity requirements of the mixer.

B. Mixer

Conversion gain in excess of unity is often convenient since the mixer then provides amplification along with the frequency translation. However, it does not necessarily follow that sensitivity improves, because noise figure must also be considered. For this reason, passive mixers may offer superior performance in some cases despite their conversion loss. Dynamic range requirements in modern telecommunication systems are

quite severe, and especially for receiver front-end, the mixer plays an important role in overall linearity performance.

C. Filter & VGA

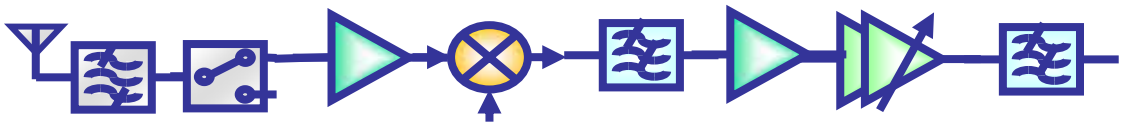
The main task of the low–pass filter consists in reducing the dynamic range requirements of the subsequent data converters by providing some filtering of the blocking signals. The VGA function must ensure that the wanted signal is maximally amplified to optimally exploit the dynamic range of the A/D converter.

D. A/D Converter

The presence of DC offset in direct conversion receiver does require some extra margin in the A/D converters. The reason is that the offset at the output of the VGA can be quite large (in the order of 500 mV) because of the large amplification factor.

When the building blocks topologies are known, the true impact of each specification can be determined and specifications can be traded against one another. The behavior simulation of 802.11a standard is performed. The sequence of the cascaded blocks is as follows, Antenna, BPF, LNA, mixer, HPF, baseband amplifier, variable gain amplifier, and LPF. The link budget analysis is listed in Table 2-7, and the simulation of gain, noise figure, SNR and the third order intercept point is shown

in Fig. 2-11. In the same way, the behavior simulation of 802.11b/g standard is shown in Fig. 2-12. After the system specifications and architecture are decided, the circuit specifications can be predicted according to the behavior simulation. General speaking, the receiver front-end is composed of the LNA and the mixer. The receiver front-end specifications of 802.11a/b/g are listed in Table 2-8.



BPF Switch LNA Mixer HPF IF Amp VGA LPF

Table 2-7 Receiver link budget calculation

Block	BPF	Switch	LNA	Mixer	HPF	IF Amp	VGA	LPF
NF (dB)	2	2	3.5	12	6	6	8	8
Gain (dB)	-2	-2	20	-6	-2	10	50	-1
IIP3(dBm)	40	40	-23	13	500Vrms	300Vrms	10Vrms	400Vrms
Cascade NF(dB)	2	4	7.5	7.9	8.2	8.4	8.9	*9.2*
Cascade Gain(dB)	-2	-4	16	10	8	18	68	*67*
Cascade IIP3(dBm)	-48	-37	-15	5	33Vrms	75Vrms	150Vrms	400Vrms

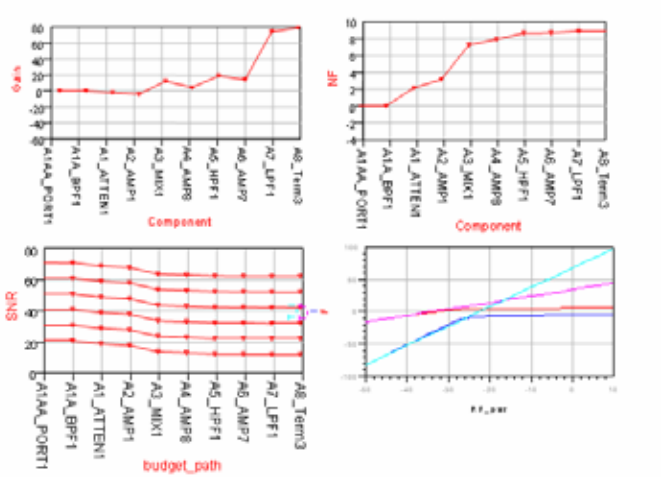
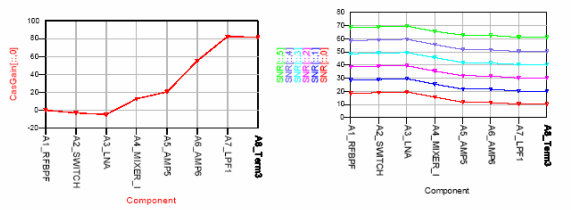


Fig. 2-11 Behavior simulation of 802.11a standard



Component	NFdegrade	SNR[:,0]
A1_RFBPF	0.000	20.327
A2_SWITCH	2.206	18.121
A3_LNA1	4.285	16.042
A4_MIXER_I	3.501	16.826
A5_AMP5	6.920	13.407
A6_AMP6	7.101	13.226
A7_LPF1	8.099	12.228
A8_Term3	8.099	12.228

Fig. 2-12 Behavior simulation of 802.11b/g standard

Table 2-8 802.11a/b/g receiver front-end specifications

	802.11a	802.11b/g
Input Return Loss (dB)	>10	
Gain (dB)	20	20
NF (dB)	7	6
IIP3 (dBm)	-20	-15
IIP2 (dBm)	-10	0
Input P_{1dB} (dBm)	-30	-25

Chapter 3
Receiver Architecture

Multistandard and multiband RF transceivers are becoming more and more popular. In the near future, as third-generation wireless systems are launched, there will be an increasing demand for multimode terminals, which will allow access to different systems providing various services. The coexistence of 3G cellular systems and wireless LAN is also not impossible and has taken some researchers's notice. The optimal multimode terminal should be as simple and small as possible. But the principal challenge in this task arises from the stringent cost and performance requirements, making it necessary to limit the additional hardware, particularly, filters, resonators, oscillators, and frequency synthesizer. Hence, it would be advantageous if the receiver could share as many of its building blocks as possible in all operation modes. Thus, both the architecture design and the frequency planning of a multistandard transceiver demand careful studies and numerous iterations. In this chapter, dual-band receiver architectures will be introduced, including "switched" and "concurrent" dual band.

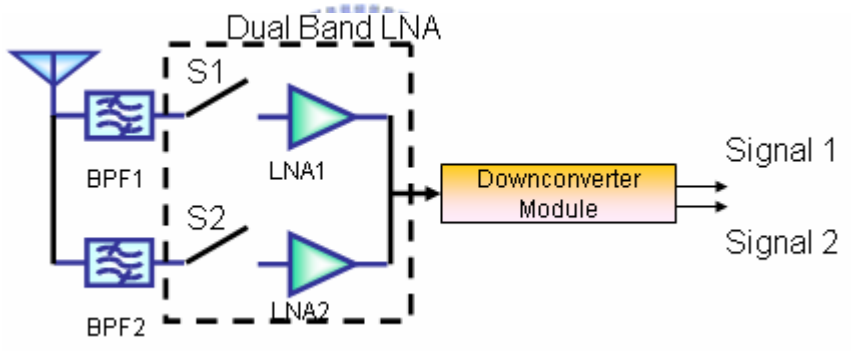
3.1 Switched Dual Band Architecture

There are a number of approaches for the design of dual-band receiver:

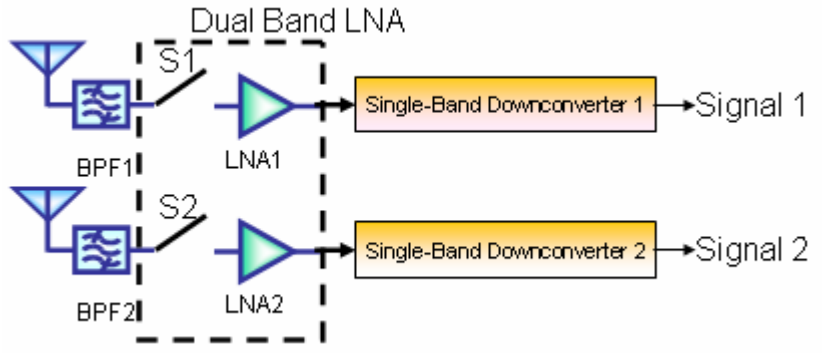
switched mode, parallel mode, concurrent mode and *wideband mode*. The first two modes are categorized in this section, and the last two will be classified in the next section, i.e., concurrent dual-band receiver.

Nowadays, most multi-band receivers use several sets of radio frequency circuits in switched or parallel mode and each set is optimized for a certain band. One of the key bottlenecks for the multiple-standard communication devices is to design a single LNA that can operate at different frequency bands, since the LNA is a very important building block of a single–chip RF receiver and locates at the first stage of the receiving path. But in switched dual-band architecture, the separate narrow-band LNA is easier to be designed in order to achieve optimal performance. The commonly used architectures are illustrated in Fig. 3-1. However, this kind of architecture will cause inevitable increase in the cost, footprint and power dissipation, because each LNA uses two single-band LNAs, either one of which is selected according to the instantaneous band of operation, or both of which are designed to work in parallel using two separate input matching circuits and two separate resonant loads. The former approach is non-concurrent while the latter consumes twice as much power. There are already many published works utilizing either one of the aforementioned architectures, including switched mode [14][15] and parallel mode [12][13]. In [15], it uses a single narrow-band LNA having dual input matching stages, which can save

chip area and cost, whereas by switching the two individual LNAs, the dual-band function is achieved [14]. There is another switched method that can be used in multiband receiver, that is, switching the resonant loading of the LNA, also called the tunable mode, but this technique is usually suited for dual band not far from each other in terms of frequency spacing, for example, within 1 GHz range, due to the limit of the relatively narrow band input matching. Thereby, tunable LNA is attractive but hard to design for a large tuning range.



(a) Switched mode



(b) Parallel mode

Fig. 3-1 Switched dual-band receiver

3.1.1 Comparisons of Receiver Architectures

In this section, several commonly used architectures suited to switched dual-band architecture are described.

A. Heterodyne receiver

Heterodyne receivers downconvert the input to an IF, perform band-pass filtering and amplification, and translate the spectrum to a lower frequency again (Fig. 3-2). Superheterodyne receiver is the most popular heterodyne receiver, and perhaps the most important feature of heterodyne receiver is its selectivity, i.e., the capability to process and select small signals in the presence of strong interferers. Heterodyning nonetheless entails a number of drawbacks. The trade-off between image rejection and channel selection typically requires a relatively high IF, making it difficult to integrate the IF filter monolithically. Furthermore, the image-reject filter is a passive, bulky device that must be placed off-chip and driven as a 50Ω load. This intensifies the trade-offs in the design of the low noise amplifier. The image problem and its solution is illustrated in Fig.3-3.

The choice of the noise figure (NF), the third intercept point (IP3), and the gain of each stage in the chain depends on those of the preceding and following stages, thereby demanding considerable iterations at the architecture and circuit levels to arrive at an acceptable distribution of gain in the receiver building blocks. Moreover,

each mixer generates many spurious components whose frequencies are related to those of the RF and IF signals and the oscillators. Thus, the frequency planning directly impacts the performance of the receiver. The switched dual-band architecture utilizing heterodyne is shown in Fig. 3-4.

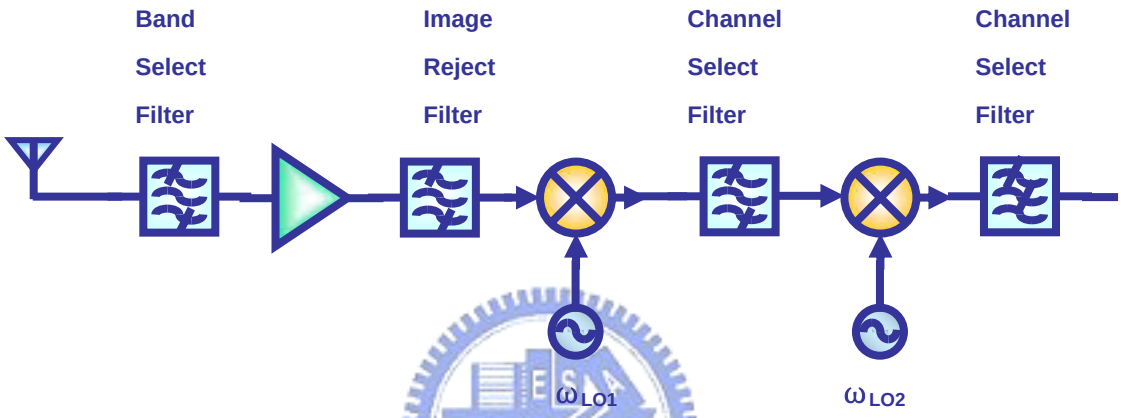


Fig. 3-2 Dual-IF heterodyne receiver

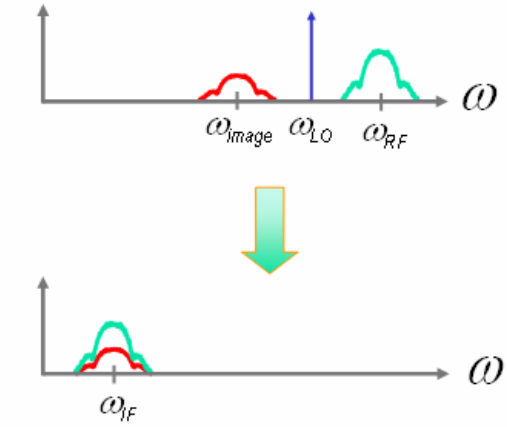
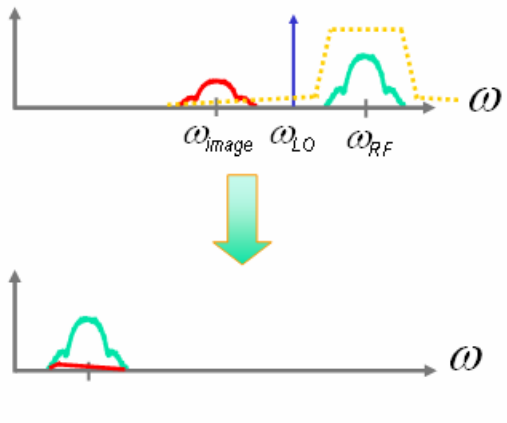


Fig. 3-3(a) Image problem



(b) The function of image reject filter

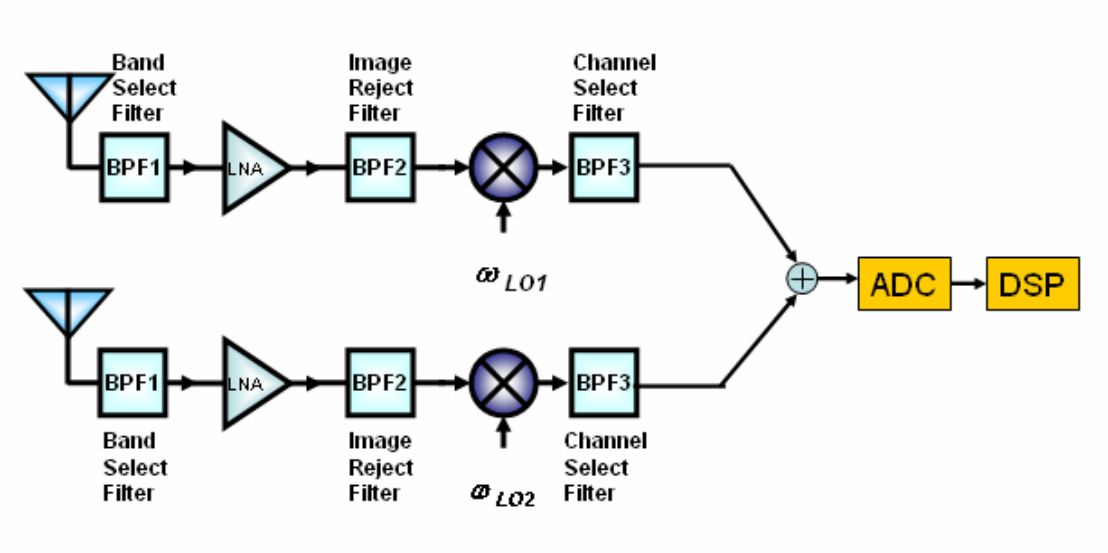
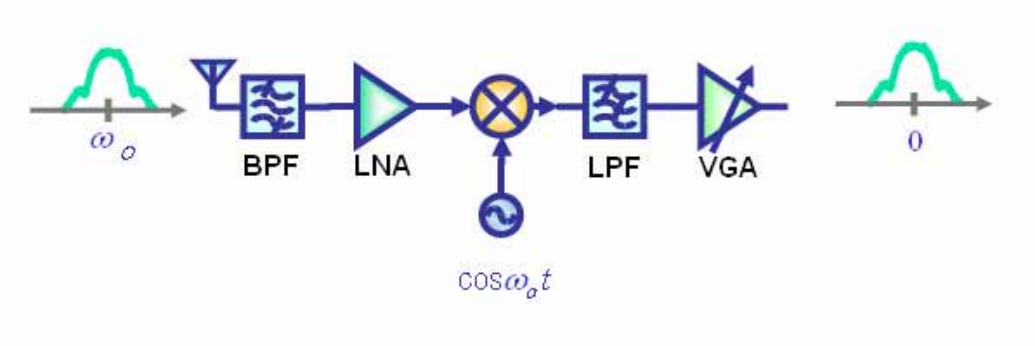


Fig. 3-4 Conceptual architecture of a switched dual-band receiver [16]

B. Direct conversion receiver

Direct-conversion receivers (DCR), also called zero IF receiver, translate the channel of interest directly to zero frequency (Fig.3-5(a)). For frequency- and phase-modulated signals, the downconversion must provide quadrature outputs so as to avoid loss of information (Fig.3-5(b)).

Direct conversion offers two important advantages over a heterodyne counterpart. First, the problem of image is circumvented because $\omega_{IF}=0$. As a result, no image filter is required and the LNA need not drive a 50Ω load. Second, the IF filters and subsequent downconversion stages are replaced with low-pass filters and baseband amplifiers that are amenable to monolithic integration.



(a) Simple direct-conversion receiver

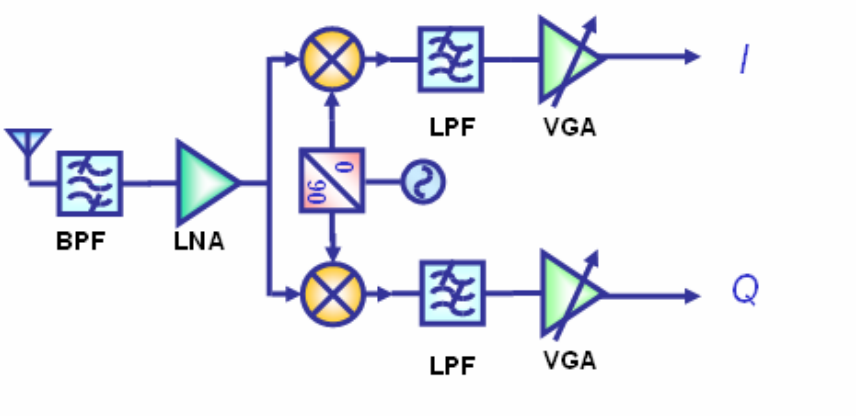


Fig. 3-5(b) Direct-conversion receiver with quadrature downconversion

(i) DC offset

The simplicity of direct conversion nevertheless comes with a number of design issues. First, as shown in Fig. 3-6, dc offsets due to mixing of the local oscillator (LO) leakage with itself corrupt the baseband signal and, more importantly, saturate the following gain stages. There are many DC offset cancellation techniques, such as digital calibration using DSP algorithms, auto-zeroing techniques, DC free coding in the transmitter, AC coupling requiring a large capacitor (Fig. 3-7(a)), high pass through utilizing servo loop, feedback or feed forward methods, TDMA burst mode(Fig. 3-7(b)), and so on.

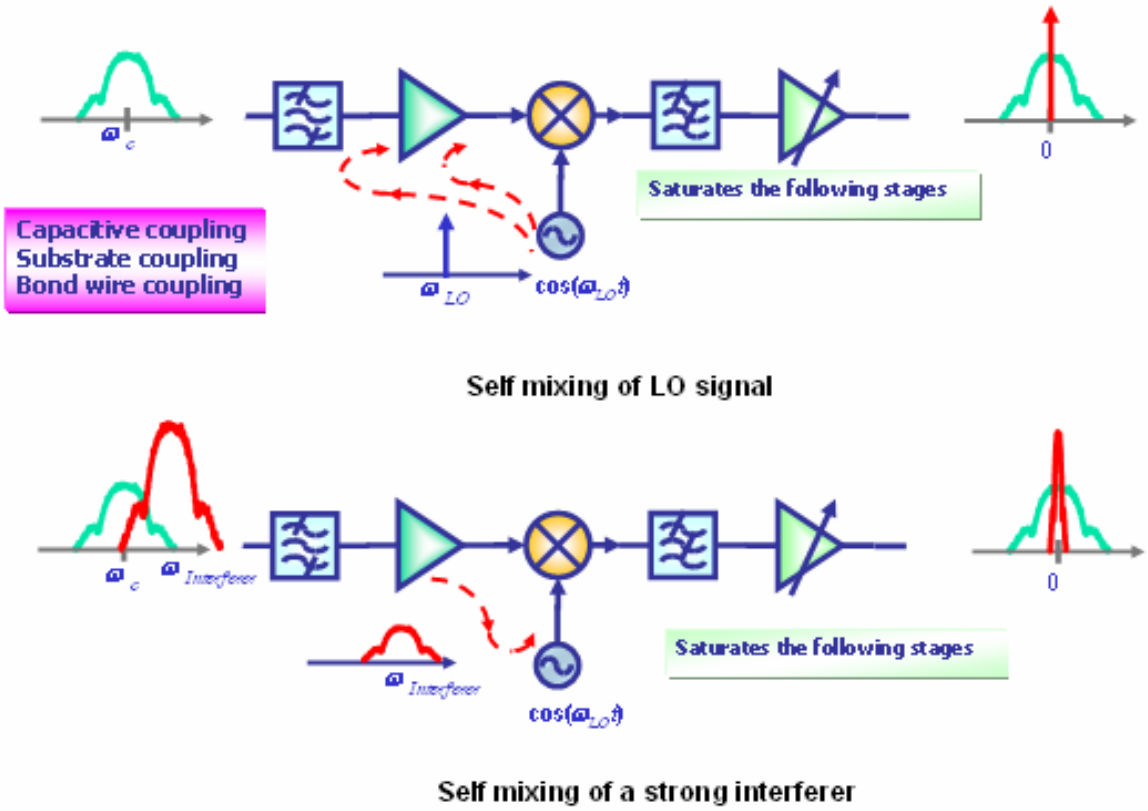
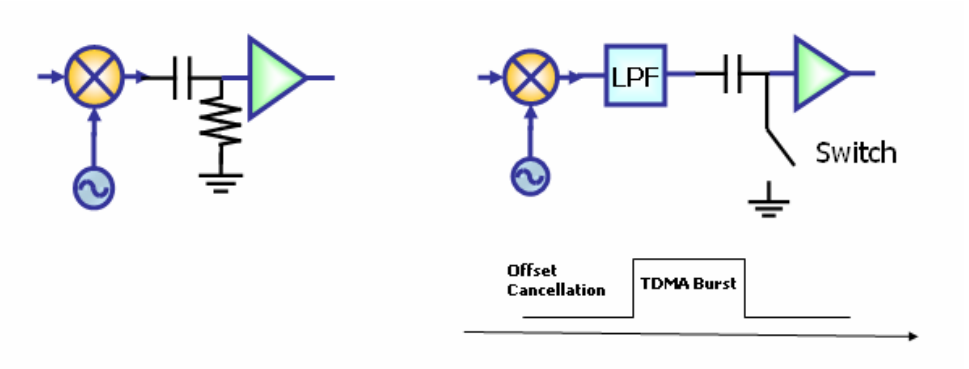


Fig. 3-6 DC offsets in direct conversion receiver



(a) AC coupling (b) TDMA burst mode

Fig. 3-7 DC offset cancellation techniques

(ii)Even-order distortion

As depicted in Fig. 3-8, even-order distortion in the RF signal path generates low-frequency beats from large interferers. In the presence of mismatches and asymmetry in the mixer, such components appear at the output, thus degrading the signal-to-noise ratio (SNR). This effect can be reduced by differential circuits or high pass filtering the beats before mixer.

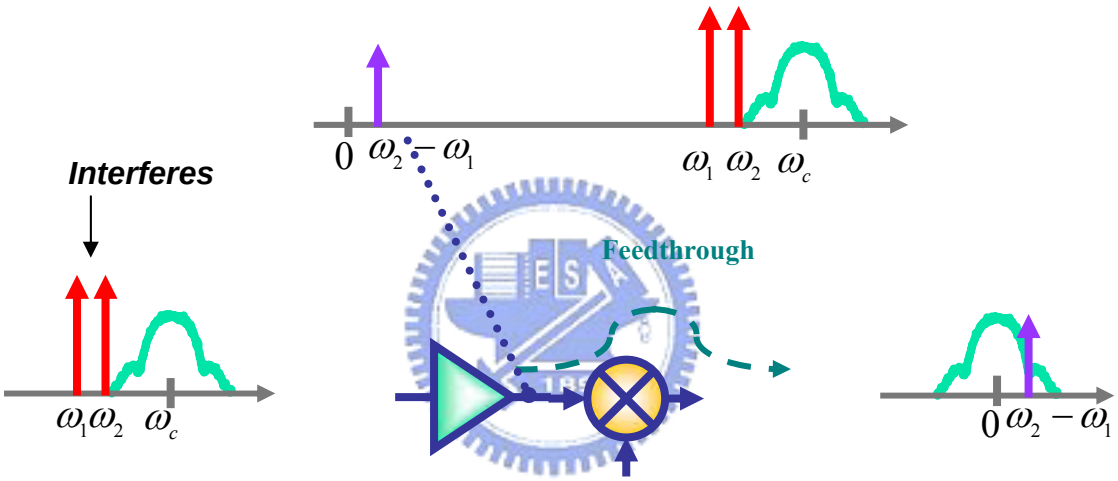


Fig. 3-8 Effect of even-order distortion

(iii) I/Q mismatch

Another issue in direct-conversion receivers is the phase and gain mismatch introduced by the mixers. Fig. 3-9 shows the signal constellation with finite gain and phase errors.

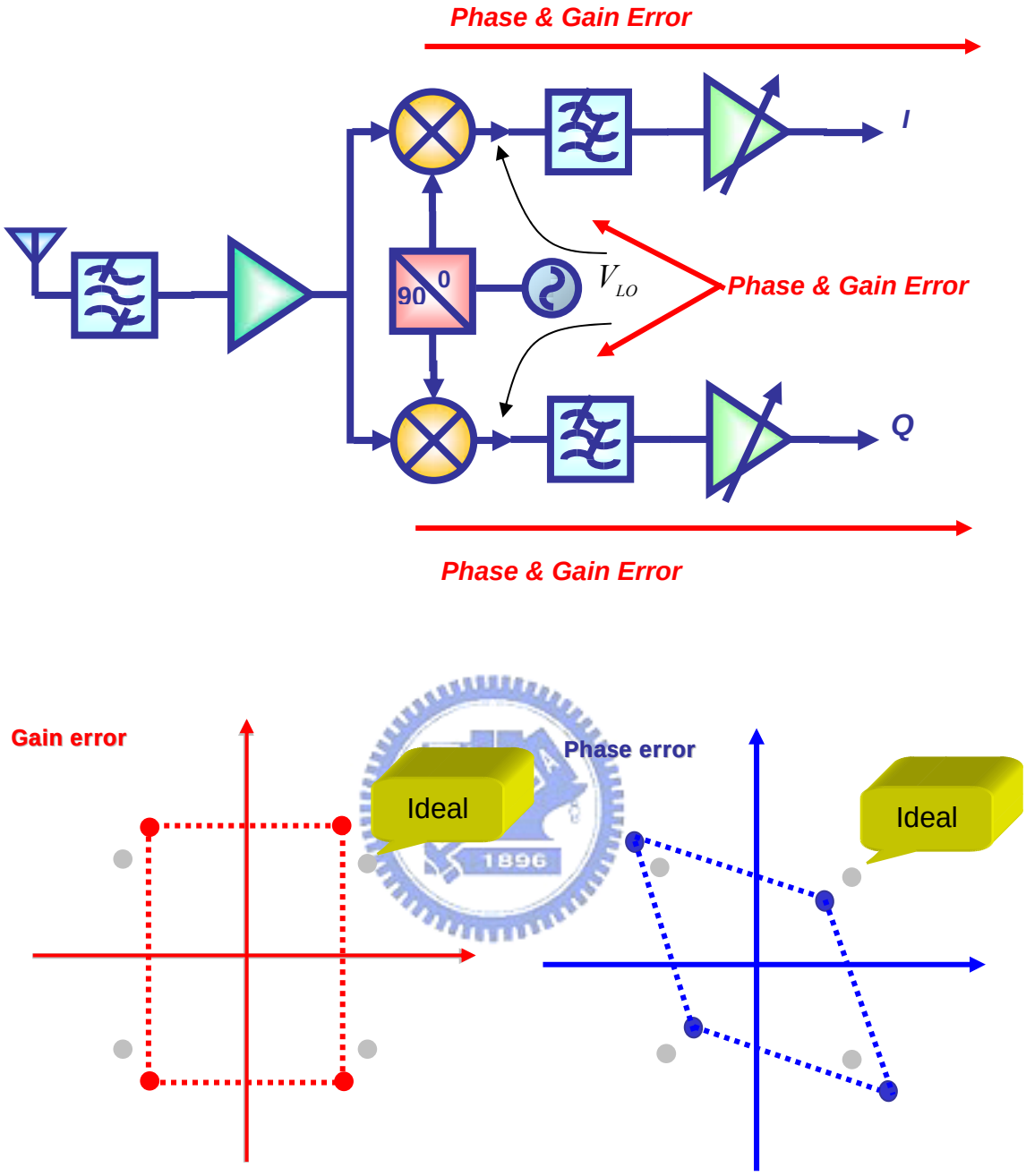


Fig. 3-9 Signal constellations due to gain and phase mismatch

As shown in Fig. 3-10, phase mismatch gives rise to cross-talk between demodulated quadrature waveforms, lowering the SNR because the I and Q data streams are usually uncorrelated. The key point, however, is that I/Q mismatch is

much less troublesome in DCR'S than in image-reject architectures.

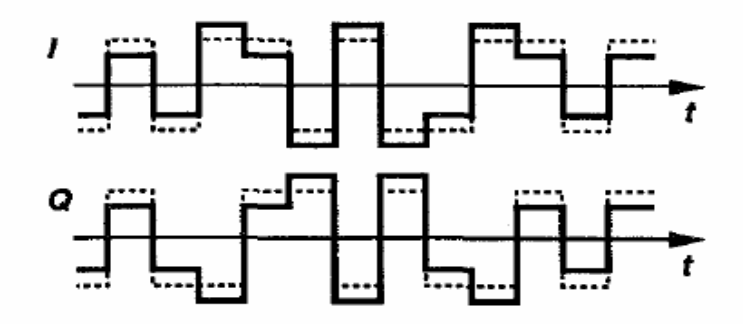


Fig. 3-10 Effect of I/Q phase imbalance on demodulated QPSK data

(iv) Flicker noise

The spectral density of the flicker noise is inversely proportional to frequency; therefore, it is commonly known as 1/f noise. Fig. 3-11 shows the illustration of flicker noise with a corner frequency of 200 kHz. With a typical gain of roughly 30 dB in the LNA/mixer combination, the downconverted signal usually falls in the range of tens of microvolts. The input noise of the following stage, for example, amplifiers and filters, is therefore still critical. In particular, since the downconverted spectrum is located around zero frequency, the 1/f noise of devices has a profound effect on the signal, a severe problem in MOS implementations.

The effect of flicker noise can be reduced by a combination of techniques. As the stages following the mixer operate at relatively low frequencies, they can incorporate very large devices (several thousand microns wide) to minimize the magnitude of the flicker noise. Moreover, periodic offset cancellation also suppresses low-frequency noise components though correlated double sampling.

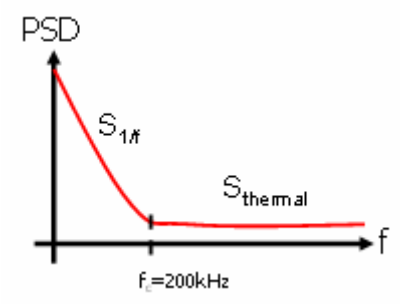


Fig. 3-11 Power spectral density of flicker noise

There are various receiver architectures which can be adopted in switched dual-band applications, depending on the frequency plan. In this thesis, the proposed switched dual-band receiver is based on the direct conversion architecture, as show in Fig. 3-12. We will focus on the shaded part, including 5 GHz and 2.4 GHz band receiver frontend.

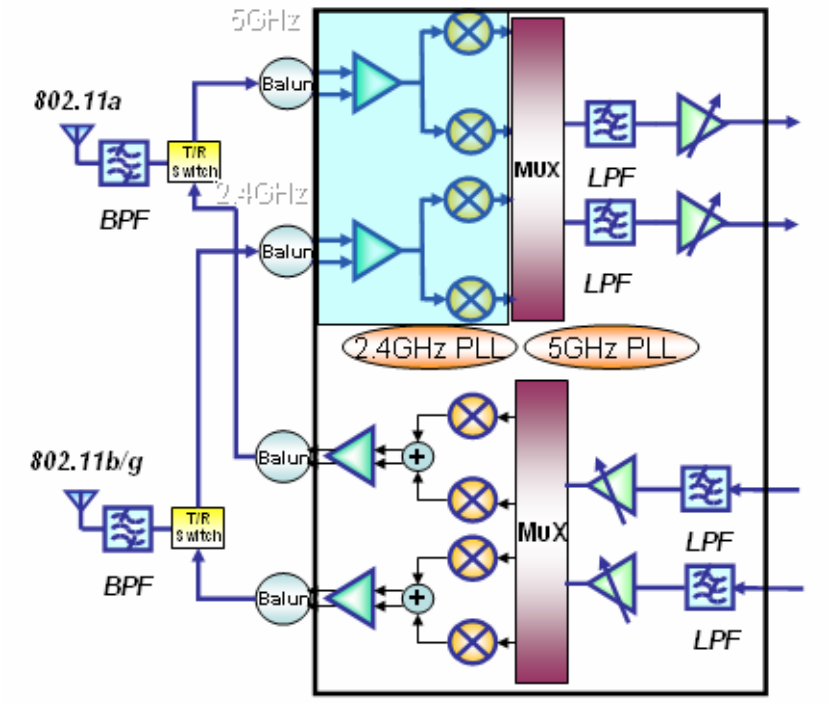


Fig. 3-12 The proposed switched dual-band architecture

C. Image-reject receiver

The issues related to the image-reject filter have motivated RF designers to seek other techniques of rejecting the image in a heterodyne receiver. One such technique originates a single-sideband modulator introduced by Hartley, illustrated in Fig. 3-13. Hartley's circuit mixes the RF input with the quadrature outputs of the local oscillator, low-pass filters and shifts the results by 90° before adding them together. The principal drawback of the Hartley architecture is its sensitivity to mismatches: with phase and gain imbalance, the image is only partially cancelled. The effect of I/Q mismatch is much more sever here than in direct-conversion receiver. Also, the loss and noise of the shift-by-90° stage and linearity of the adder are critical parameters. Furthermore, the variation of R and C introduces gain mismatch, limiting the image rejection ratio severely.

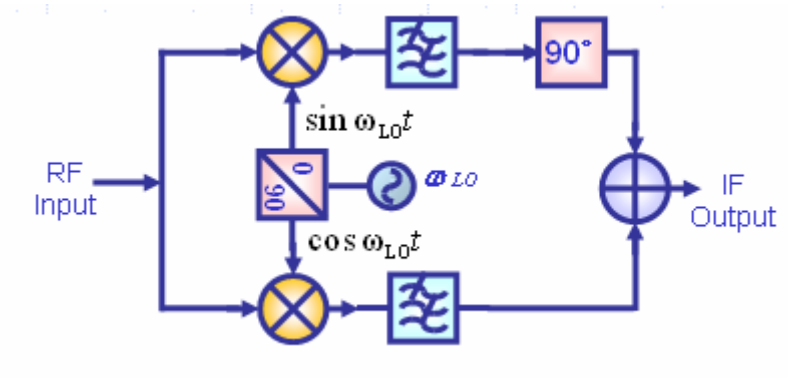


Fig. 3-13 Hartley image-reject receiver

Shown in Fig. 3-14 is the image-reject architecture introduced by Weaver. Replacing the 90˚ shift of Hartley's circuit with a second quadrature mixing operation, this technique provides an arbitrary translation of the signal band without image interference. The Weaver architecture is also sensitive to mismatch, but it avoids the use of an RC-CR network, thereby achieving greater image rejection despite process and temperature variations. The switched dual-band architecture employing image-reject receiver is shown in Fig. 3-15.

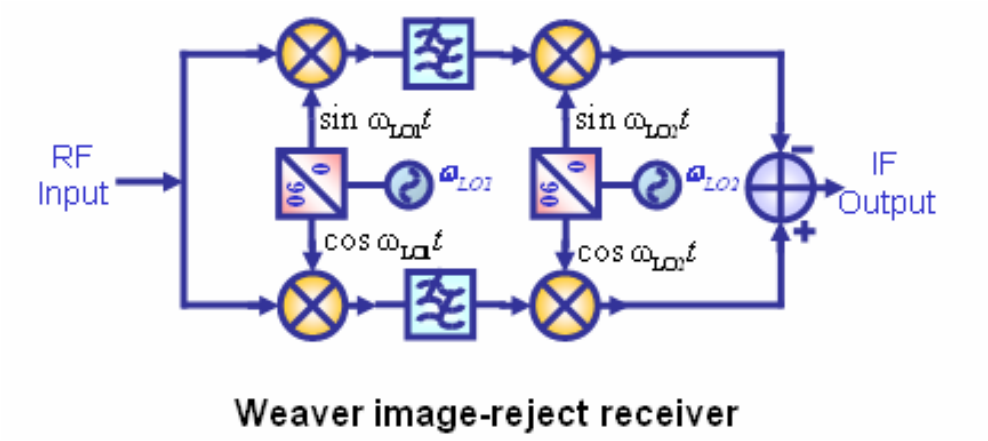


Fig. 3-14 Weaver image-reject receiver

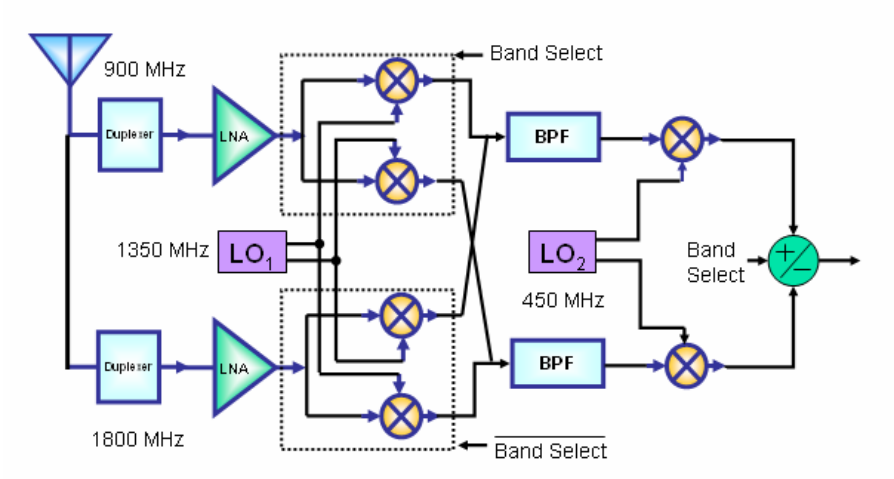


Fig. 3-15 Dual-band implementation of the Weaver architecture [13]

3.2 Concurrent Dual Band Architecture

This section will transfer the viewpoint from “switched” to “concurrent”. The extensive definition of concurrent dual band in this thesis includes both “concurrent mode” and “wideband mode”. Although the abovementioned “switched” mode is very popular, its principal drawback is that it’s very area inefficient. Another way is to use a wideband RF front-end that is capable of handling all the different carrier frequencies. Standard receiver architectures, such as superheterodyne and direct conversion, accomplish high selectivity and sensitivity by narrow-band operation at a single input frequency. These modes of operation limit the system’s available bandwidth and robustness to channel variations and thus its functionality. In addition to dual-band applications, wideband LNA can still be used for ultra wideband receiver and multiband applications more than two bands. Fig. 3-16 illustrates a wideband receiver employing direct-conversion architecture. It eliminates the complicated issue of choosing proper IF frequency in a dual or multiband radio, resulting in a compact, low cost receiver front end. On the other hand, wide-band modes of operation are more sensitive to out-of-band unwanted signals (blockers) due to transistor nonlinearity. These out-of-band blockers can severely degrade receiver’s sensitivity. Therefore, the dual-band function can be obtained by implementing dual-band antenna and filter while the front end ICs can be implemented with wideband

characteristics.

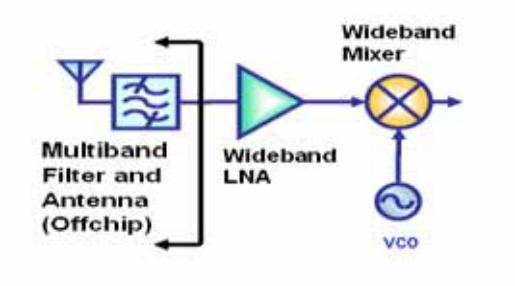


Fig. 3-16 Dual-band direct-conversion architecture (wideband mode)[5]

While switching between bands improves the receiver's versatility (e.g., in multiband cellular phones), it is not sufficient in the case of a multi-functionality transceiver where more than one band needs to be received simultaneously (e.g., a multiband cellular phone with a global positioning system (GPS)). Using conventional receiver architectures, simultaneous operation at different frequency bands can only be achieved by building multiple independent signal paths with an inevitable increase in the cost, footprint, and power dissipation. A very important observation is that the transconductance of the transistor is inherently wide-band and can be used to provide gain and matching at other frequencies without any penalty in the power dissipation. This observation leads to a compact and efficient front-end for a concurrent dual-band receiver which consists of a dual-band antenna, followed by a monolithic dual-band filter and a concurrent dual-band LNA that provides simultaneous gain and matching at two bands, as shown at the bottom of Fig.3-17. A detailed approach to the design of such a dual-band LNA will be described in the

subsequent chapter. It should be noted that the concurrent dual-band receiver does not need any dual-band switch or diplexer, because simultaneous reception at both bands is desired. Then a dual-band down-conversion scheme is needed to translate different information-carrying signals to baseband with as few local oscillators (LOs) and external filters as possible, while maintaining isolation between the two bands. This can be done in many different ways. For example, Fig. 3-18 shows a simplified block diagram of one such receiver employing image rejection.

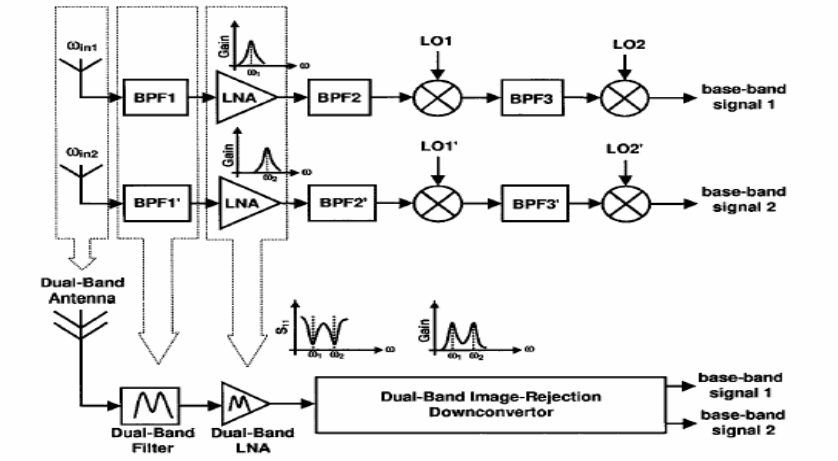


Fig. 3-17 Evolution process of two parallel receivers to a concurrent dual-band receiver [11]

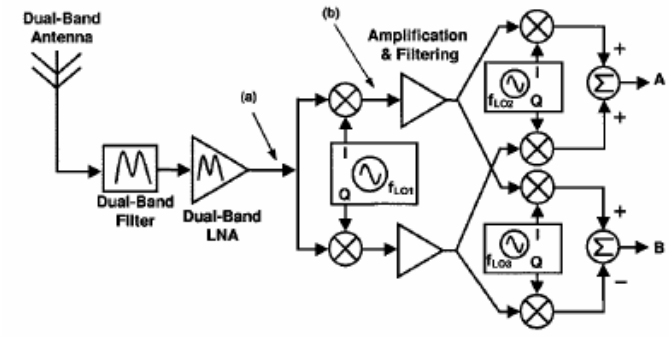


Fig. 3-18 An architecture for the concurrent dual-band receiver employing image rejection [11]

The frequency of the first LO that appears after the LNA and performs the first down conversion determines the image frequency and plays an important role in the performance of the system. For a *nonconcurrent* receiver, it has been proposed to choose the first LO frequency halfway between the two frequency bands and select the band of interest. However, for a *concurrent* receiver where the LNA amplifies the signal in both of the desired bands, it will suffer from some serious shortcomings. This is because one band is the image of the other and there is no attenuation of the image by either the antenna or the filter. The situation is exacerbated by the LNA gain in the image band.

An alternative approach that does not suffer from the above problem and, in fact, significantly improves the image rejection is to use an offset LO as shown Fig. 3-19. The LO frequency is offset from the midpoint of the two bands of interest ($\mathbf{f_A}$ and $\mathbf{f_B}$) in such a way that the image of the first band at $\mathbf{f_A}$ falls at the notch of the front-end transfer function at $\mathbf{f_{IA}}$. The attenuation at $\mathbf{f_{IA}}$ is determined by the compounded attenuation of the dual-band antenna, filter, and LNA. Similarly, the image of the second band at $\mathbf{f_B}$ will fall outside the passband of the front-end at $\mathbf{f_{IB}}$ and will be attenuated, accordingly. Using a quadrature first LO makes the stage fit to act as the first half of any single-sideband image-reject architecture, such as that proposed by Weaver. Since the receiver has to demodulate two bands concurrently and

independently, two separate paths must be used eventually. Each path comprises the second half of the image reject architecture, which provides further image rejection . This architecture eliminates an extra antenna, a front-end filter, an LNA, and a pair of high-frequency mixers, which in turn results in power, footprint, and area savings. At the same time, large image rejection in excess of that of the single-sideband receiver is achieved through diligent frequency planning and proper usage of stop-band attenuation.

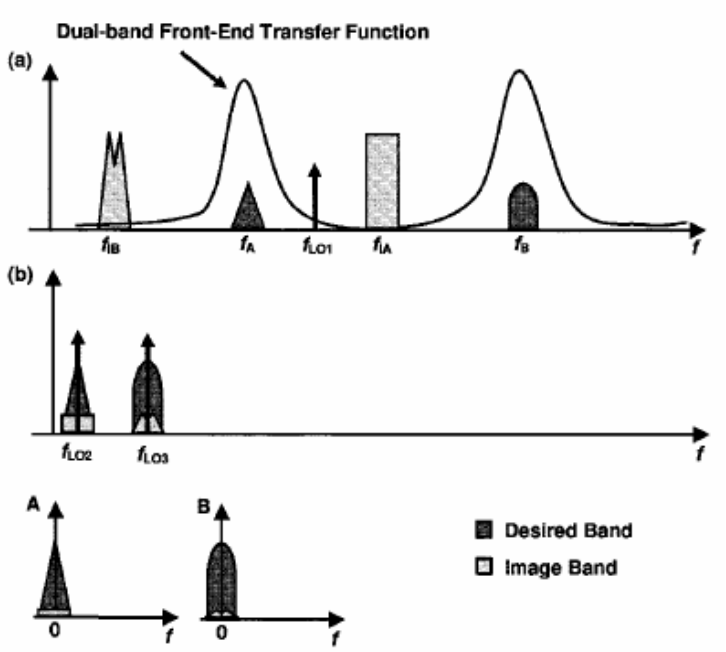


Fig. 3-19 Frequency-domain signal evolution of the concurrent dual-band receiver in Fig. 3-18 [11]

Thereby, the concurrent dual-band receiver based on the image rejection architecture (Fig. 3-18) needs a very careful frequency planning and a well-designed transfer function of dual-band BPF and LNA. Different from the image rejection architecture, the concurrent dual-band receiver based on direct conversion scheme is

proposed in this thesis, which is more suitable for integration and has no image problem. The evolution is illustrated in Fig. 3-20 and Fig. 3-21 depicts the block diagrams. Compared with the architecture in Fig.3-18, the frequency planning is simpler and the transfer function designs of dual-band LNA as well as BPF are not so stringent. Meanwhile, this architecture is not only for concurrent operation, but it can also substitute for the switched mode for nonconcurrent operation as mentioned in the preceding section. If we just need a nonconcurrent operation, the lower block represented by the dotted line can be eliminated. Take 2.4/5 GHz dual band for instance, a concurrent dual-band LNA is followed by single-band down conversion stage, and a 2.4/5 GHz switched dual-band VCO controls whichever band will be received in the baseband. If 5 GHz RF band needs to be received, then VCO outputs a 5 GHz signal as the LO input of the mixer. Both DC and RF (2.6 GHz = 5 GHz -2.4 GHz) signals are received after the mixer, but only DC signals can pass through low pass filter whereas RF signals carrying 2.4 GHz modulated information will be filtered out by LPF following the mixer. This operation is for 5 GHz RF signal, and vice versa for 2.4 GHz operation (just switching to 2.4 GHz VCO output signal). Take 2.4 GHz band operation for example, it is shown in Fig. 3-22. This principle is that only one band can be mixed down to baseband, whereas the other band is still held in RF.

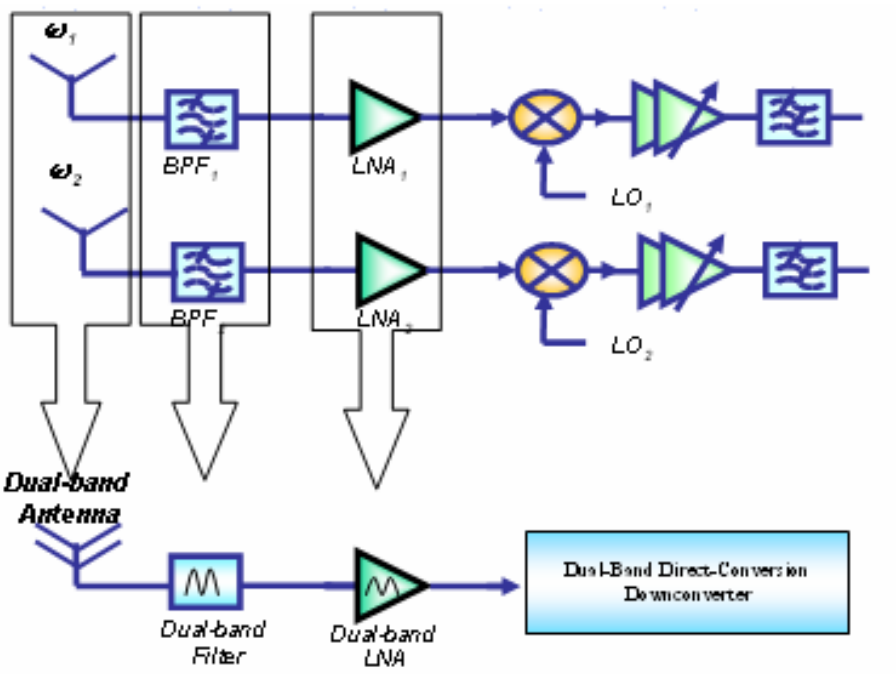


Fig. 3-20 Evolution process of concurrent dual-band direct-conversion receiver

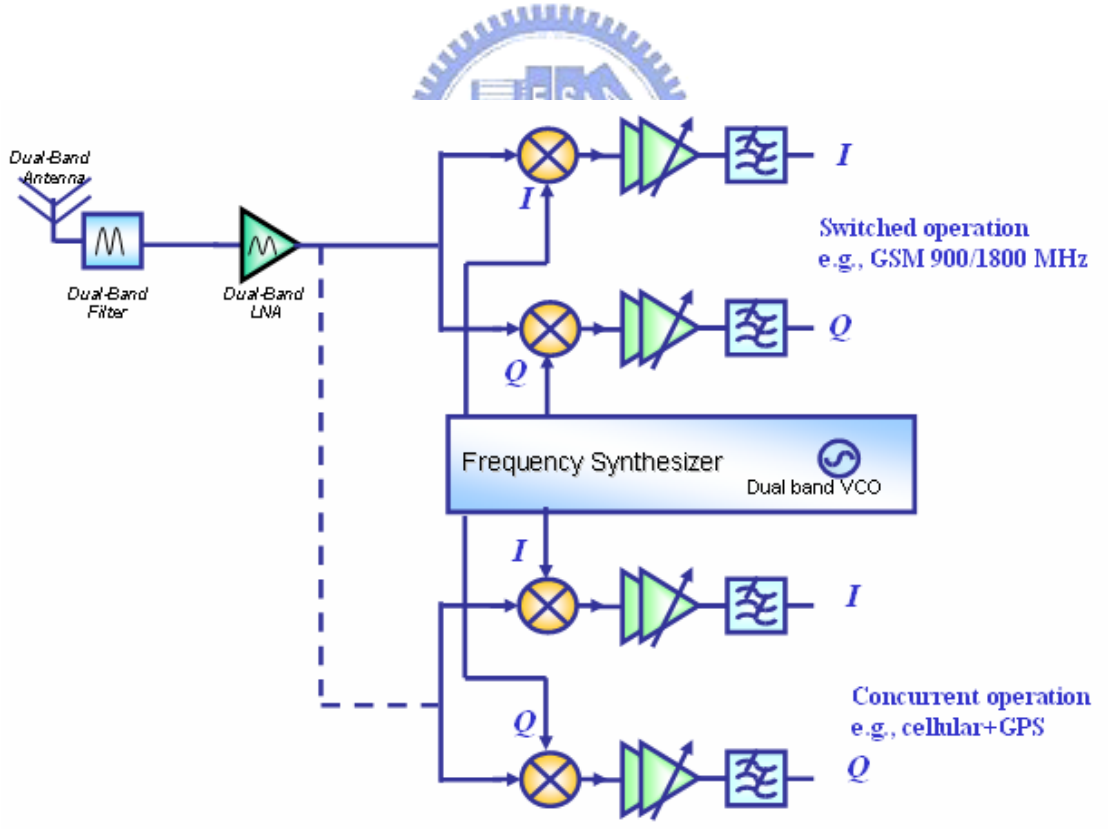


Fig. 3-21 Block diagrams of concurrent dual-band direct-conversion receiver (concurrent mode)

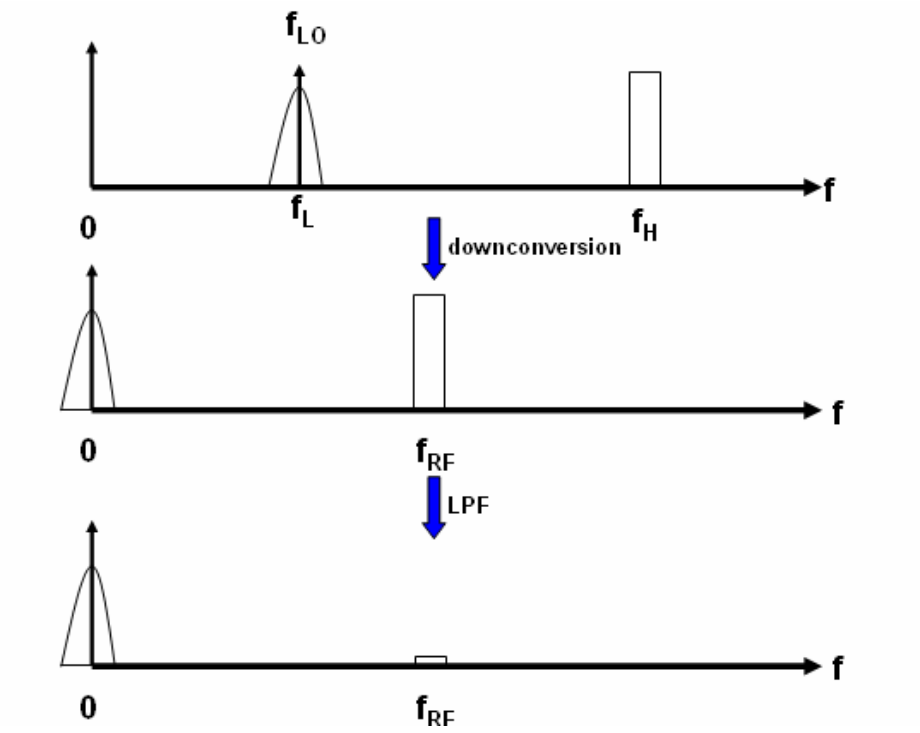


Fig. 3-22 Downconversion operation of concurrent dual-band direct-conversion receiver

Chapter 4

Device Characteristic and RF Modeling

CMOS technology continues to benefit from both scaling and the enormous momentum of the digital market, many high-speed and RF integrated circuits that were once considered the exclusive domain of III–V or SiGe bipolar technologies are likely to appear as CMOS implementations. As a result, CMOS technology becomes a prime choice for SOC applications where cost is a key driver and the noise and power consumption requirements are compatible.

Device modeling plays a critical role in the simulation of RF and analog circuits, but the importance is often neglected by circuit designers. This chapter describes the CMOS technology characterization that provides the basic information required in RF and analog design. It also reviews some relevant modeling difficulties, including the modeling of MOSFET, noise, and passive devices.

4.1 Device Characteristic

Drawing an analogy with digital integrated circuit technology, we would expect the optimum technology choice for RF IC applications to follow the same path that digital IC implementations followed, that is, towards CMOS. The principal difficulty in using a digital CMOS technology for analog design is that the process is

optimized and characterized for primarily one tradeoff: that between speed and power dissipation. By contrast, technical requirements for a transceiver function are considerably more complex than that of digital integrated circuits. Issues such as noise, linearity and gain are performance specifications that RF transceivers have to deal with. Even though the optimum integrated circuit technology choices for RF circuits are still evolving, CMOS technology is proved adequate for RF applications in the recent years.

4.1.1 Technology Comparisons

The two important figures of merit in comparing device characteristic are cut-off frequency f_t and maximum oscillation frequency f_{max}.

cut-off frequency

Defined as the frequency at which the short-circuit small-signal-current gain of a transistor drops to unity (Fig. 4-1), f_t is a measure of the speed of the intrinsic device excluding its junction parasitic. For a bipolar and MOS device, the cut-off frequency is defined as Eq. (4-1) and Eq.(4-2) respectively.

$$f_{t,BJT} = \frac{g_m}{2\pi\left(C_\mu + C_\pi\right)} \tag{4-1}$$

$$f_{t,MOS} = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4-2}$$

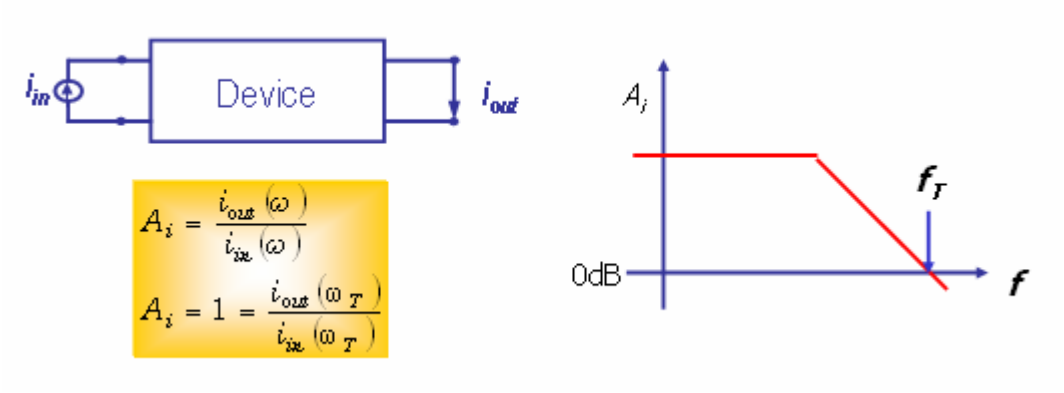


Fig. 4-1 The definition of f_t

Maximum oscillation frequency

The maximum oscillation frequency f_{max} has been defined to include the effect of the base resistance for bipolar transistors and similarly the gate, source and channel resistance for MOS devices. At this frequency, the maximum available power gain, i.e. G_{max}, becomes unity (Fig.4-2). The maximum oscillation frequency of both BJT and MOS is defined as Eq. (4-3) and (4-4) respectively.

$$f_{\max,BJT} = \sqrt{\frac{f_{t,BJT}}{8\pi r_b C_\mu}} \tag{4-3}$$

$$f_{\max,MOS} = \frac{f_{t,MOS}}{2\sqrt{2\pi f_{t,MOS} R_g C_{gd} + G_{ds} R_{in}}} \tag{4-4}$$

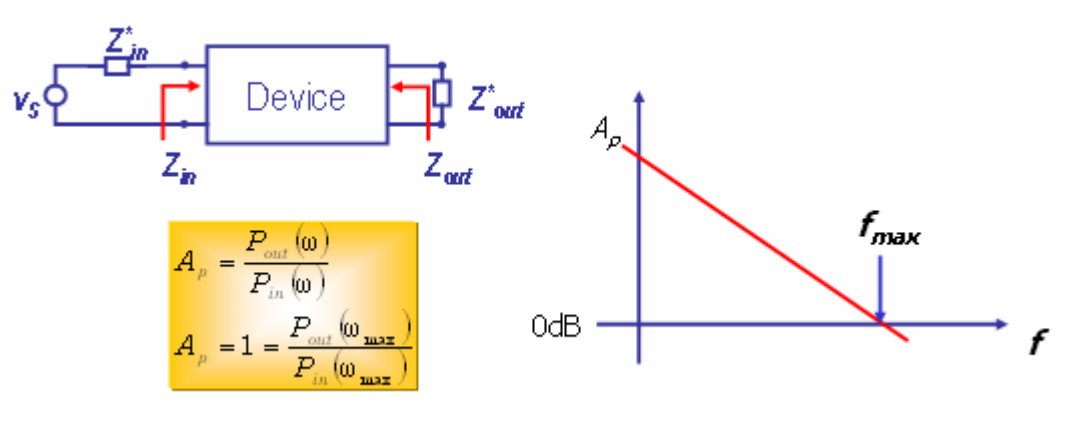


Fig. 4-2 The definition of f_{max}

Fig. 4-3 shows the high-frequency performance of Si BJT and NMOS devices. MOS devices exhibit a substantial speed advantage at low currents compared to bipolar devices, but bipolar transistors exhibit better performance at low voltages.

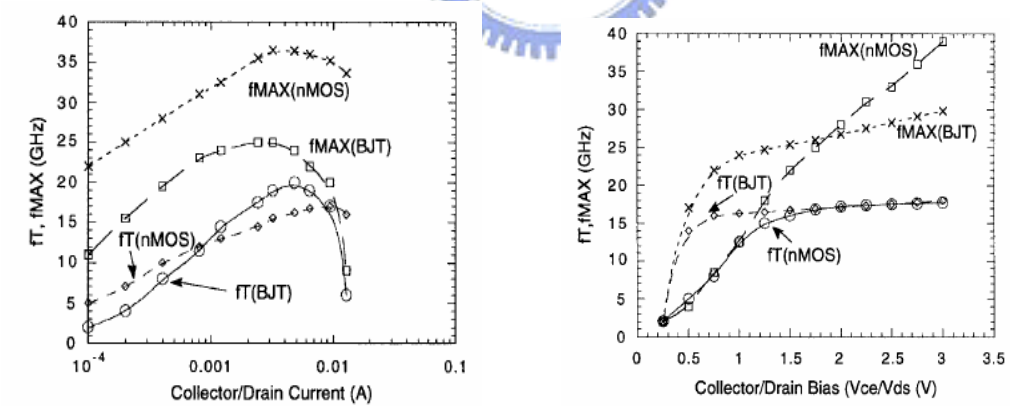


Fig. 4-3 Comparison of f_t and f_{max} versus Collector/Drain current and voltage [29]

In addition to frequency characteristic, the RF/microwave performance of a transistor can be quantified in terms of noise parameters.

A. Thermal Noise

Thermally agitated charge carriers in a conductor give rise to a random voltage due to their Brownian (random) motion. The noise voltage has a zero average value, but a nonzero mean-square value (Fig.4-4). Thermal noise can be regarded as independent white noise, i.e. noise power is additive. Thermal noise of a resistor can be modeled as a noise voltage source in series with the resistor (Thevenin), or a noise current source in parallel with the resistor (Norton), as shown in Fig. 4-5.

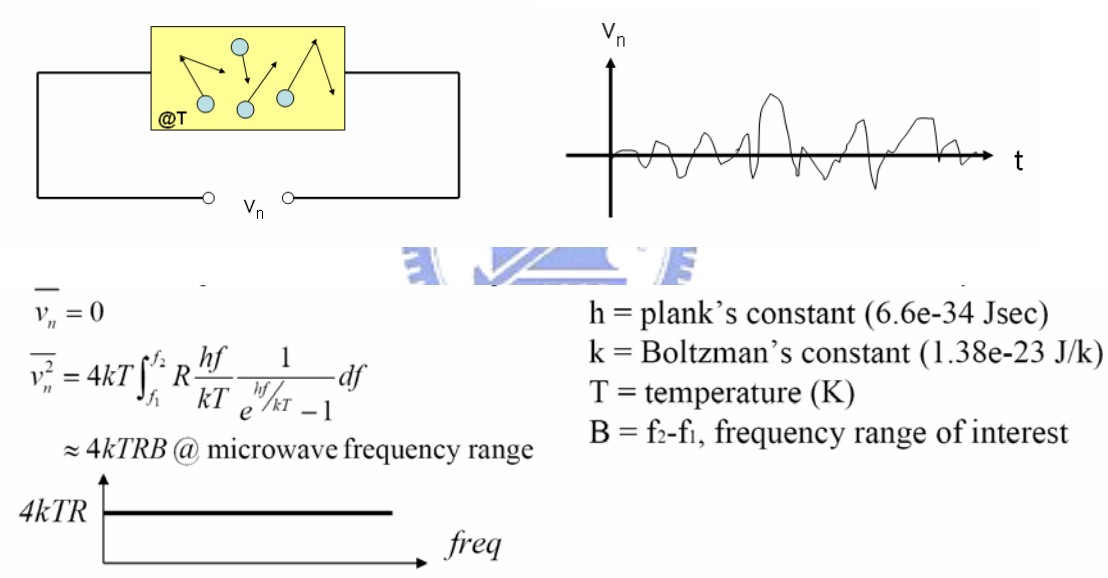


Fig.4-4 The illustration of thermal noise

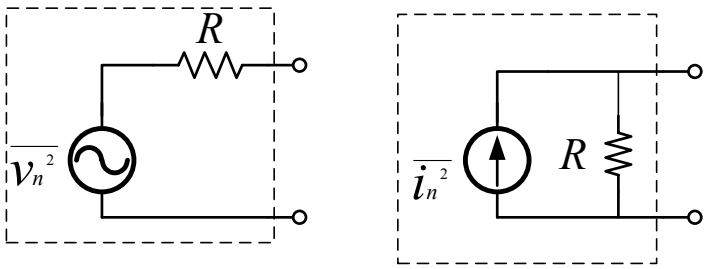


Fig.4-5 The model of thermal noise

B. Shot Noise

Shot noise occurs in PN junctions, and there are two conditions for shot noise to occur: direct current flow and energy barrier over which a charge carrier hops. Fig. 4-6 illustrates the phenomenon of shot noise. Shot noise of the diode can be represented by a noise current source in parallel with the diode. Fig. 4-7 depicts the equivalent model.

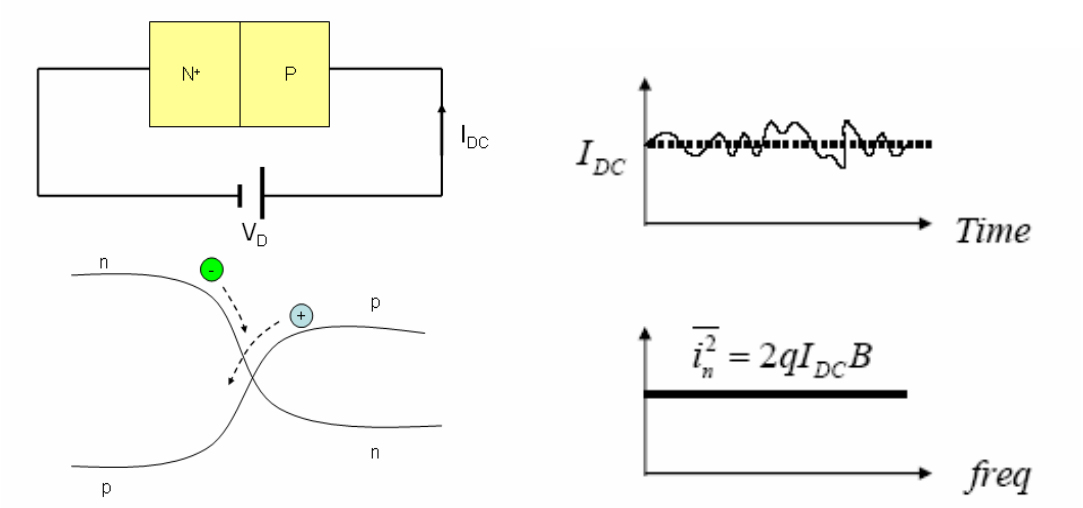


Fig. 4-6 The illustration of shot noise

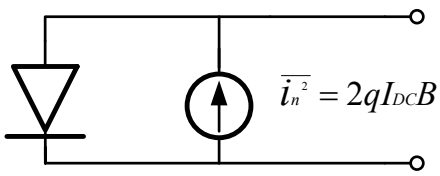


Fig. 4-7 The illustration of shot noise

C. Flicker Noise

In BJTs, flicker noise is caused by traps associated with contamination and crystal defects in the depletion regions. The traps capture and release carriers in a random fashion and the time constants associated with the process give rise to the 1/f nature of the noise power density. It has been established experimentally that only the base current exhibits 1/f noise. The characteristic is shown in Fig.4-8.

Flicker noise in MOSFETs is due to trapping of charges on the interface between the gate oxide and the silicon substrate. The trapping time leads to the 1/f character. Larger MOSFETs exhibit less 1/f noise because their larger gate capacitance smoothes the fluctuations in channel charge. Thinner dielectric layer is also preferred.

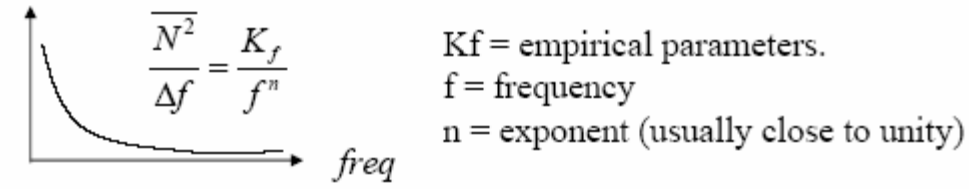
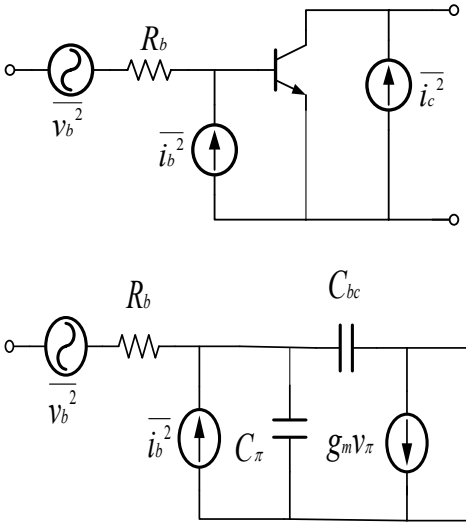


Fig. 4-8 The characteristic of flicker noise

Combining with the above-mentioned noise source, the noise models of BJT and MOSFET are demonstrated in Fig. 4-9.



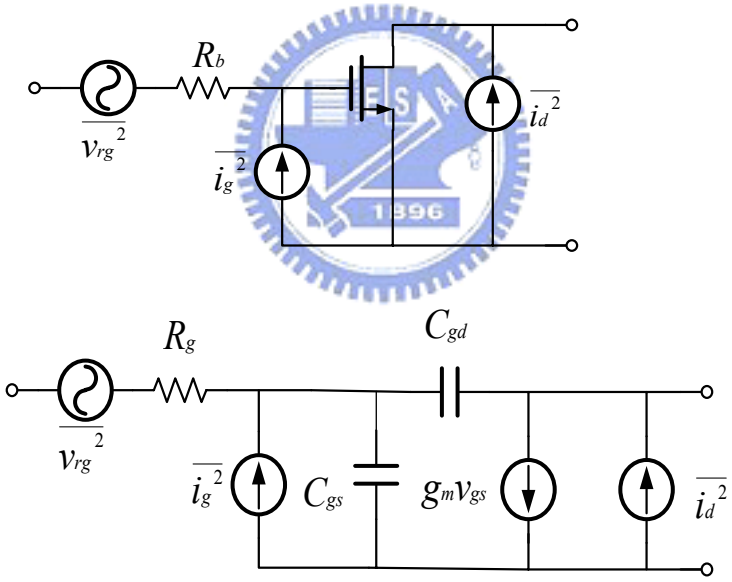
$$\overline{v_b^2} = 4kTR_b\Delta f$$

$$\overline{i_b^2} = 2qI_{BQ}\Delta f + K_f\frac{I_{BQ}}{f}\Delta f$$

$$\overline{i_c^2} = 2qI_{CQ}\Delta f$$

(a) Noise model of BJT

(b)



$$\overline{v_{rg}^2} = 4kTR_g\Delta f$$

$$\overline{i_g^2} = 4kT\delta R_{ch}\Delta f \qquad R_{ch} = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$$

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f + K_1\frac{\Delta f}{f}$$

$$g_{d0} = \text{drain} - \text{source conductance}\ @\ V_{DS} = 0$$

Fig. 4-9 (b) Noise model of MOSFET

Take LNA for example, several technologies are compared based on the figure-of-merits: gain, DC power dissipation, and noise figure. Care must be taken in comparing circuit performance, since it represents an intermingling of intrinsic device performance, process features, and circuit design. From Fig. 4-10, GaAs and SiGe show superior performance if dc power dissipation is a major consideration.

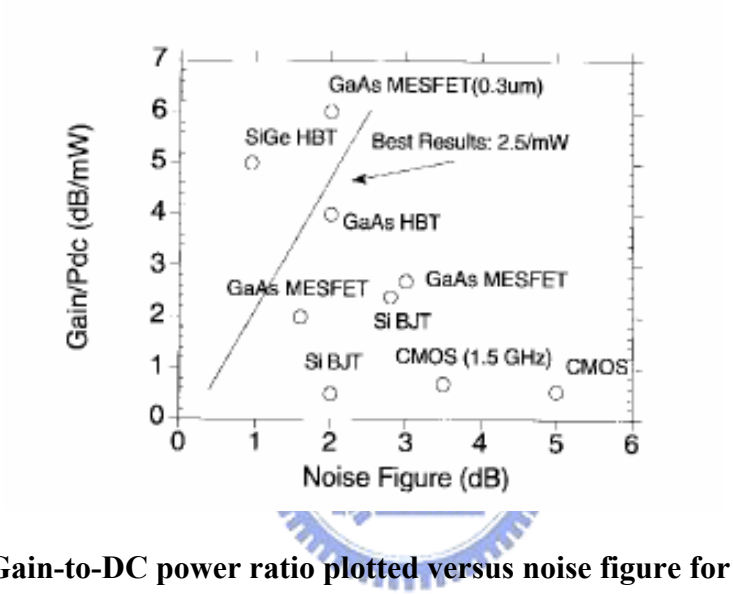


Fig. 4-10 Gain-to-DC power ratio plotted versus noise figure for 2-GHz LNA [29]

Because of the extreme dynamic range considerations of the low-noise front end, linearity is an equally important figure-of-merit for LNA's. In this case, a linearity figure-of-merit is the ratio of the input third-order intercept point (IP3) to the dc power dissipation. Fig. 4-11 illustrates that bipolar transistor amplifiers have demonstrated outstanding linearity performance compared to field-effect transistors. As with the case of noise figure, the performance advantages of SiGe and GaAs technologies are significant if dc power dissipation is a critical parameter, although the improvement is less dramatic.

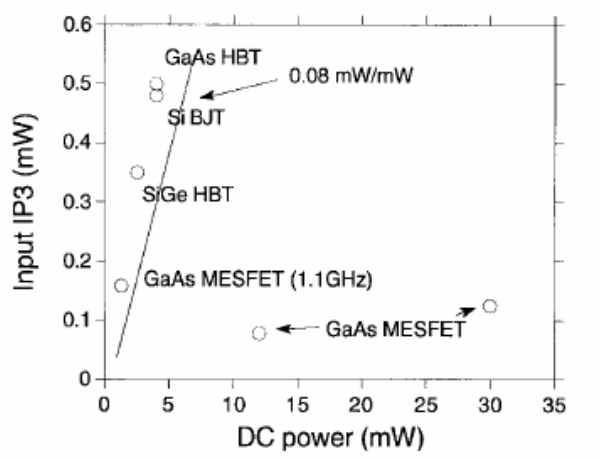


Fig. 4-11 Linearity versus DC power for 2-GHz LNA [29]

From the aforementioned discussions, CMOS technology is expected to possess a significant edge in production costs. However, time-to-market and performance issues are also important for RF applications, and it is in these areas that traditional Si bipolar and GaAs technologies possess an edge at this time. Nevertheless, in the long run, CMOS technology will acquire many of these desirable qualities, and Si Bipolar and GaAs technologies will find themselves increasingly pressed by competition with CMOS.

4.2 RF Modeling

Modeling of devices is as important as characterization. Without good models, it becomes difficult to analyze and predict circuit behavior on transistor level. Bipolar devices have a long history in modeling, even for radio frequencies. We will therefore not focus on bipolar device modeling, but will concentrate on MOS device modeling, where this accuracy is still lacking.

4.2.1 MOSFET Modeling

For the past few years, intensive research has been going on in the field of RF MOS modeling. Studies have shown that the "standard" (digital-oriented) MOS models do not allow for RF modeling. Three major effects play an important role at high frequencies: the terminal resistances, bulk effects, and non-quasi static effects. Each of these effects will be discussed briefly.

A. terminal resistances

At DC or low frequency, the gate resistance consists of poly-silicon sheet resistance and can be approximated by Eq. (4-5)

$$R_g = \frac{1}{3}\frac{W}{L}R_{\square,\,poly} \tag{4-5}$$

But, at high frequency, two additionally effects appear:

- Distributed transmission line effect on the gate (Fig. 4-12(a))
- Channel induced gate resistance(Fig. 4-12(b))

$$R_g = R_{g,poly} + R_{g,nqs}$$

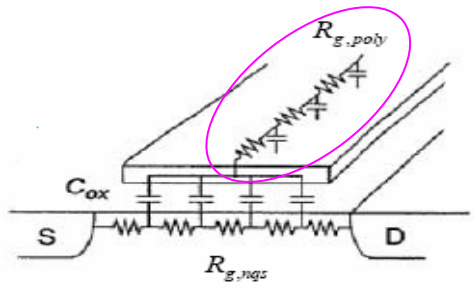


Fig. 4-12(a)

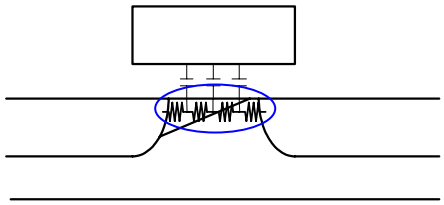


Fig. 4-12(b)

Besides, resistances in series with the drain and source degrade the drain

current and transconductance of the MOSFET. The source resistance will degrade the noise performance and the maximum oscillation frequency. The drain resistance will reduce the output impedance of the device.

B. bulk effects

Device operations are influenced by signals on the bulk node as a result of the body effect. A proper bulk resistance network is therefore mandatory in the intrinsic device model. The values of these resistors are highly dependent on the substrate used, i.e., a high-ohmic or low-ohmic substrate.

C. non-quasi static effects(NQS)

When signal frequencies are in the same order of the maximum operating frequencies as the MOS device, non-quasi static effects can occur. At low frequencies, the thickness of the channel will change due to the gate modulation, but the change will be the same everywhere in the channel. Hence, there will be no phase differences in the channel. However, this effect is no longer true at high frequency, as the channel thickness will be modulated. This effect results in an extra real contribution to the input impedance, the NQS model of which is shown in Fig. 4-13. The MOSFET model of UMC 0.18μm mixed-mode/RF CMOS process is shown in Fig.4-14.

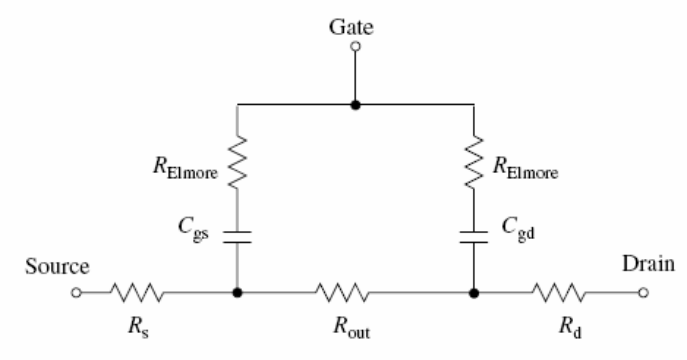


Fig. 4-13 Elmore non-quasi-static equivalent circuit

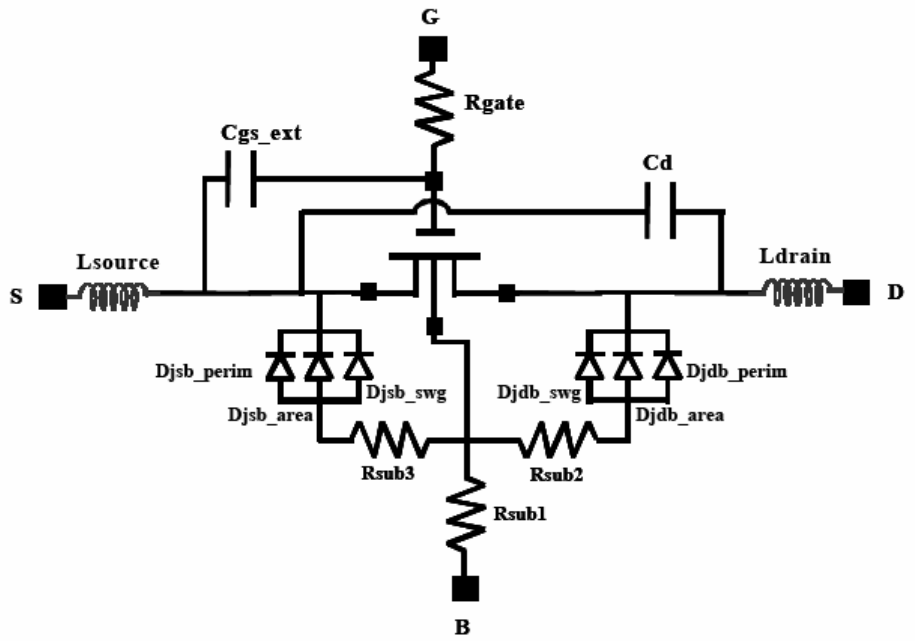


Fig. 4-14 RF N/P MOSFET extension model of UMC 0.18μm mixed-mode/RF CMOS process

(1) Rgate is used to model the equivalent gate resistance.

(2) Rsub1, Rsub2 & Rsub3 represent the substrate loss.

(3) Djdb_area and Djdb_perim are used to model source/drain bottom junction and sidewall junction capacitance.

(4) Djdb_swg and Djsb_swg are used to model source/drain sidewall junction capacitance per unit length at gate sidewall.

(5) Cd & Cgs_ext represent the total equivalent capacitance between drain, source and gate.

(6) Disable the junction diode in standard BSIM3v3 by setting AD=AS=PD=PS=0.

(7) Lsouce and Ldrain are used to model the parasitic inductance effect.

4.2.2 Noise Modeling

Both passive and active components in a circuit will generate various types of noise. In order to perform accurate noise simulation, an appropriate physics-based noise model that can predict accurately the noise performance of transistors is required. This model should be valid over a wide range of operating conditions of frequencies, currents and device geometries.

Different noise sources exist in a MOS transistor as shown in Fig. 4-15[26]. They include terminal resistance thermal noise at the gate/drain/source, thermal noise and flicker noise in the channel, substrate resistance thermal noise and induced gate noise.

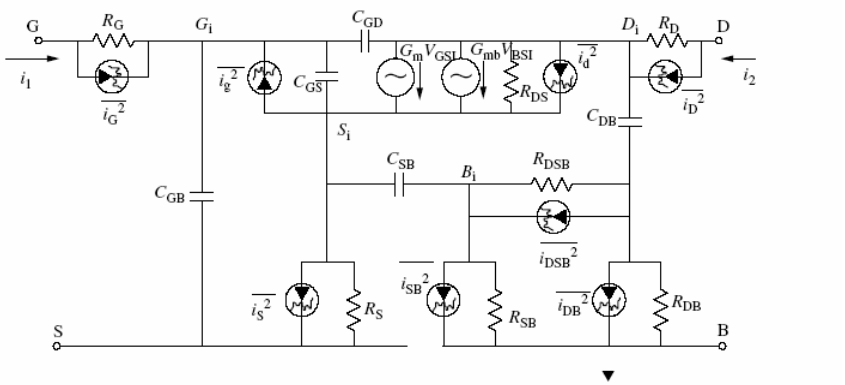


Fig. 4-15 An equivalent circuit to illustrate the noise sources in a MOSFET. i_G^2, i_S^2, and i_D^2 are the noise contributions by the terminal resistances at the gate, at the source, and at the drain; i_d^2 is the noise contribution in the channel, including the flicker noise portion; i_{DB}^2, i_{SB}^2, and i_{DSB}^2 are the noise contributions by substrate resistances; and i_g^2 is the induced gate noise

In principle, flicker noise is low-frequency noise and it mainly affects the low-frequency performance of the device, so it can be ignored at very high frequency. However, the contribution of flicker noise should be considered in designing some RF circuits such as mixers, oscillators, or frequency dividers that up-convert the

low-frequency noise to higher frequency and deteriorate the phase noise or the signal-to- noise ratio. Channel resistance and all terminal resistances contribute to the thermal noise at high frequency, but typically channel resistance dominates in the contributions of the thermal noise from the resistances in the device. Induced gate noise is generated by the capacitive coupling of local noise sources within the channel to the gate, and usually it plays a more important role as the operation frequency goes much higher than the frequency at which channel thermal noise dominates.

4.2.3 Modeling of Passive Devices

Most RF circuits do not only consist of active devices, but also use passive components such as resistors, capacitors and particularly at high frequencies, planar inductors. In many situations, the overall performance of the circuits is determined by the (parasitic) behavior of the passives. This means that the choice of technology should also be based upon the performance of the passive components. In this section, we will discuss some issues related to the design of passive devices, and describe how to model them.

A. Resistors

To have large resistance values, the resistor should be made from a material with a high resistance per unit area. The parasitic capacitances should also be as small as possible.

Well Resistor

In digital CMOS processes, where there is no high sheet resistance poly available, we may use one or more wells to implement resistors. In conventional CMOS processes, there is usually only one type of well available, either *n*-well or *p*-well. However, in state-of-the-art scaled down processes (as of this writing, 0.18-μm CMOS and newer), it becomes more and more common to have several well types. The most important feature of well resistors is the relative high sheet resistance, on the order of 1 to 10 kilo-ohms per square. The disadvantages of well resistors are high temperature coefficients (TCs) (may be as high as 6000 ppm/◦C), voltage dependency, and large parasitic capacitances to ground since the well is located close to the substrate. A π equivalent circuit of a well resistor valid up to moderate frequencies (about 100 MHz) is shown in Figure 4-16

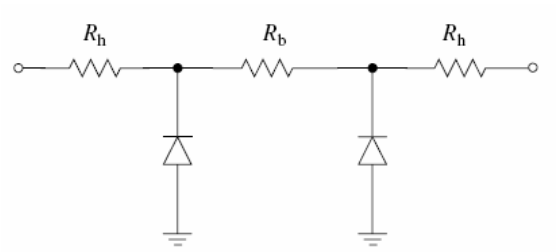


Fig. 4-16 Equivalent circuit of a well resistor

Metal Resistors

When small resistances are desired, maybe the best choice is to use one of the metal layers. Sheet resistance of the different metal layers is typically in the range 20

to 40Ω/sq. The advantages of metal resistors are low parasitic coupling to the substrate, low-voltage dependency, and low TCs.

Diffused Resistors

Diffused resistors can be realized in a CMOS process by making contacts to each side of an implanted region (the same type of region that is used for the drain and source of MOS transistors). Resistors made this way exhibit sheet resistance in the range 20 to50 Ω/sq if silicide blocks are used. Hence, using this resistor type may add extra cost to the manufacturing. This resistor type is not often used, since most CMOS processes offer poly resistors that have equal or greater sheet resistances.

Poly Resistors

Polysilicon is used in all modern CMOS processes for producing the gate of the MOS transistors. After deposition, the poly is heavily doped to improve conductivity for obtaining high-speed operation of the MOS transistors. The sheet resistance of heavily doped poly lies in the range of 1 to 20Ω/sq. At an extra cost, a mask can be manufactured that stops heavy poly doping at regions where resistors are desired. As a result, lightly doped poly can be produced with sheet resistance varying between 20 to 1000Ω/sq. The TC of poly resistors can have both positive and negative values depending on the doping density and the type of doping atoms used. In general, the absolute value of the TC increases with the sheet resistance.

Similar to well resistors, the equivalent circuit of poly resistors also includes parasitic capacitances to ground. However, since the poly layer is located further from the substrate compared to wells, the capacitance per unit resistor area is smaller for poly resistors compared to well resistors. Poly resistors may have unit-area parasitic capacitances on the order of 0.1 fF/μm2. The layout and equivalent circuit of a poly resistor in UMC 0.18 μm mixed-mode/RF CMOS process valid up to about 10 GHz is shown in Figure 4-17. A variety of resistors fabricated by CMOS process are listed in Table 4-1.

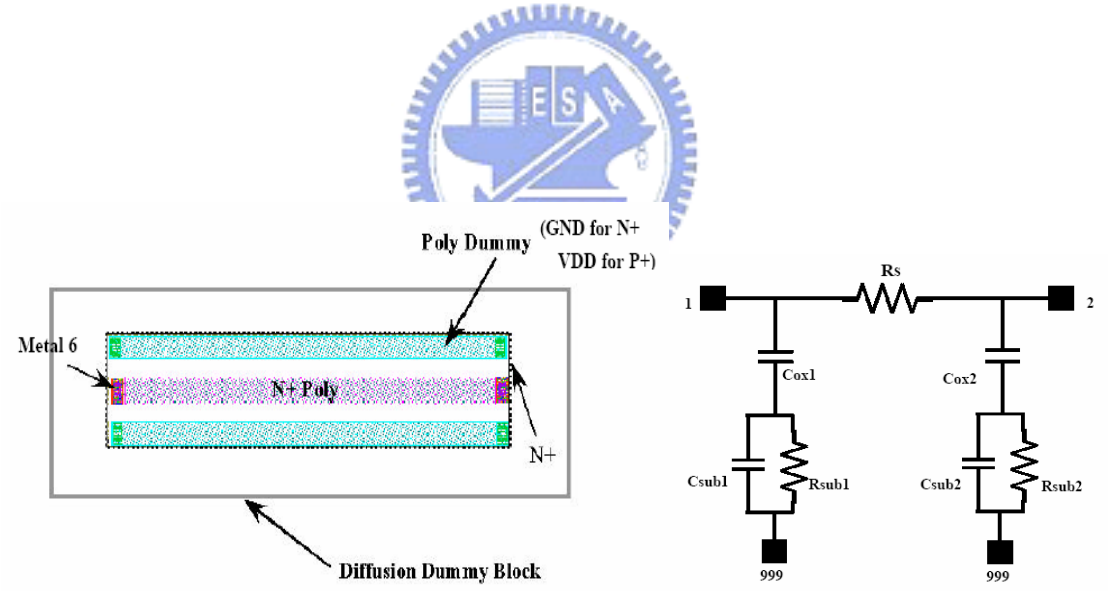


Fig. 4-17 Layout and equivalent circuit of N+/P+ non-salicided poly resistor in UMC 0.18 μm mixed-mode/RF CMOS process

Table 4-1 CMOS Resistor [28]

Type	*Sheet resistance (Ω/square)*	*Temperature coefficient (TC) (ppm/C)*	*Tolerance*	*Note*
Polysilicon - Silicided - Unsilcided	 5 – 10 Higher	 ~ 1000 Vary widely	 35% 50%	Low parasitic capacitance, low voltage coefficient
Source-drain diffusion	Similar to silicided poly	Similar to silicided poly		Significant parasitic cap., noticeable volt. coeff.
Well	1K – 10K	Large (3000 – 5000)	Poor (50 – 80%)	Substantial parasitic cap., large volt. coeff.
MOS transistor	Nonlinear to Vds voltage	High		
Metal interconnect	Order of 50m			Small resistor

Resistors is not just resistors in high frequency applications, and it has a few non-ideal parasitic effect, including series inductance, shunt capacitance, and substrate effect. The model is depicted in Fig. 4-18. The self-inductance of the metal or the poly resistor is modeled by inductor Ls, which is not included in the model of UMC CMOS process.

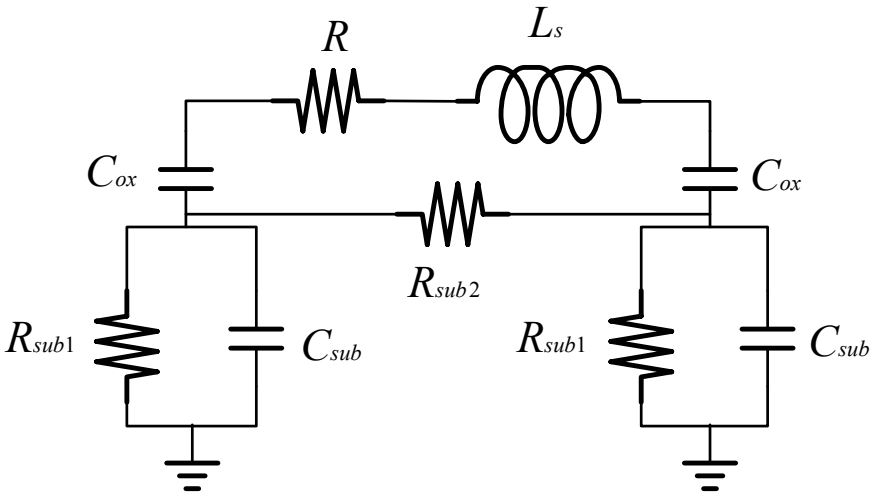


Fig. 4-18 Circuit model of resistors

B. Capacitors

Capacitors have become ubiquitous in analog-integrated circuits particularly owing to the switched capacitor technique for realization of analog-to-digital and digital-to-analog data converters and discrete-time filters. Other applications include continuous-time filters, RF building blocs, and for compensation in feedback amplifiers.

Poly–poly Capacitors

As the name indicates, both plates of a poly-insulator-poly (or simply poly-poly) capacitor are made of deposited polysilicon that is doped to keep the resistivity low. The bottom plate is usually implemented using the same layer as the poly gate of MOSFETs. The other plate must be supported by a second poly layer. There are extra processing steps involved in poly-poly capacitors since the insulator is unique to this structure. An example vertical cross section of a poly-poly structure is shown in Fig. 4-19.

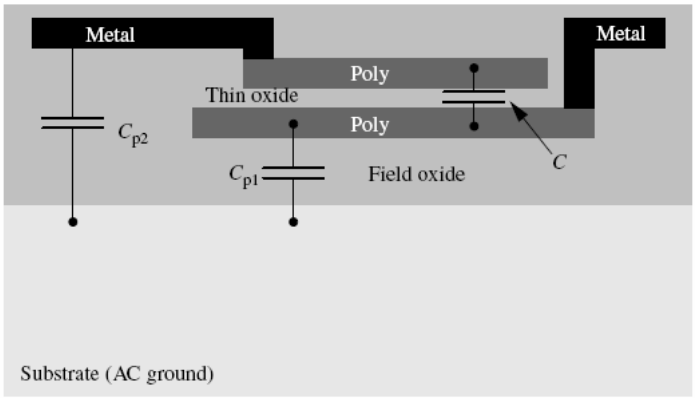


Fig. 4-19 Vertical cross section of a poly-poly capacitor structure

Metal–insulator–metal Capacitors

In RF designs larger capacitance values are very often needed. These large values can be realized by fringe capacitors (Fig.4-20(a)). When designing fringe capacitors, the device is laid out in such a manner that a maximum number of parasitic capacitances are created to increase the value of the capacitor, and the cross section is depicted in Fig.4-20(b). Another option to realize large capacitance values is to make use of metal-insulator-metal (MIM) structure (Fig. 4-21). MIM capacitors are rapidly becoming very popular owing to their high linearity and high unit-area capacitance. In modern state-of-the-art processes, MIM capacitors are replacing poly-poly capacitors owing to their improved linearity and mismatch characteristics since the conductivity of the metal plates is higher than that for the corresponding polysilicon plate, which reduces the effect of depletion. The drawback, however, is the special process option needed for this structure, making the technology more expensive. The structure and model of MIM capacitor used by UMC 0.18 μm CMOS process is shown in Fig. 4-22.

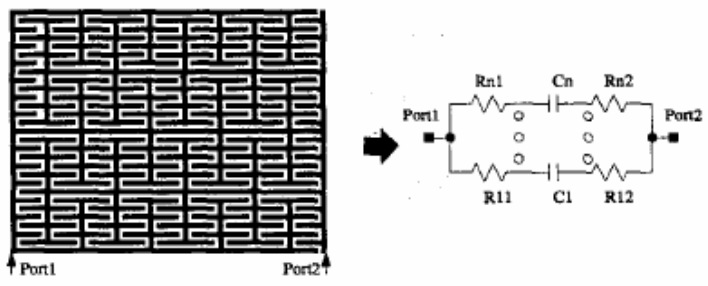


Fig. 4-20 (a) Top view of a fringe capacitor with fractal geometry and equivalent lumped circuit model

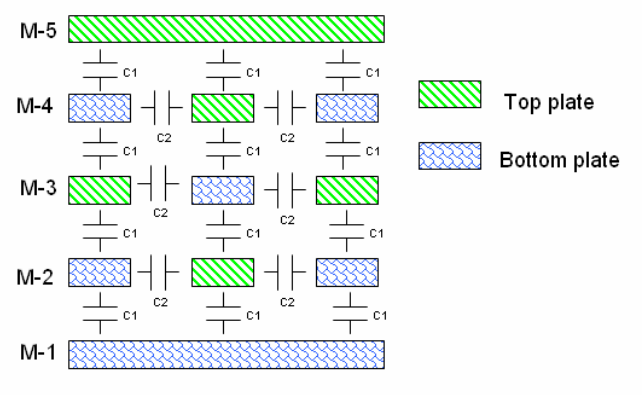


Fig. 4-20 (b) Cross-section view of fringe capacitor using five metal layers

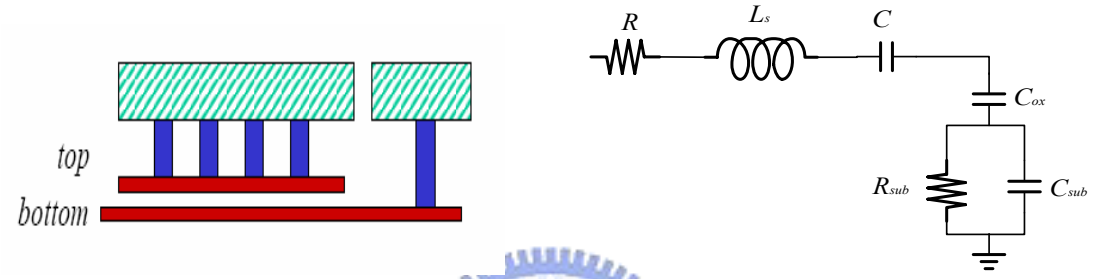


Fig. 4-21 Cross section view of general MIM capacitor with equivalent circuit model

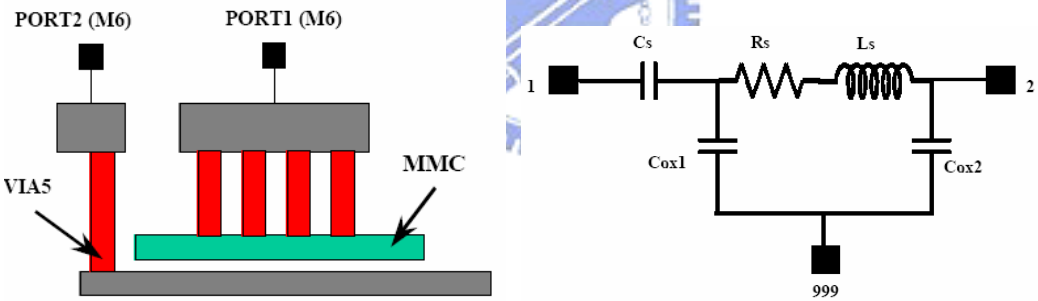


Fig. 4-22 Cross section view of MIM capacitor with equivalent circuit model by UMC 0.18 μm CMOS process

MOSFET Capacitors

MOS transistors can be used as capacitors (Fig.4-23). It is called MOS or gate capacitor which operates in accumulation mode. Their advantage is the high unit-area capacitance due to the thin oxide. High density, nonlinear, bias voltage required and medium Q are its characteristics.

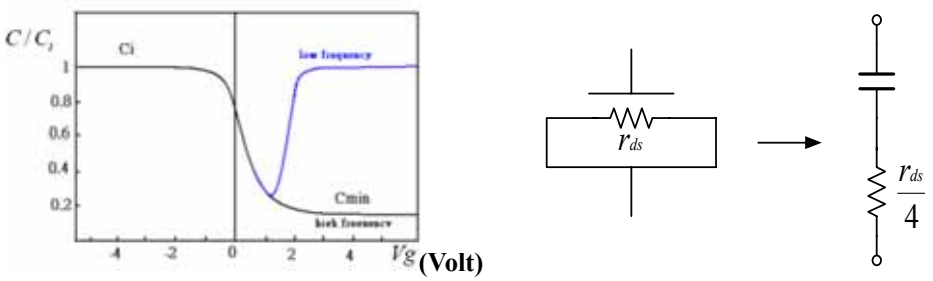


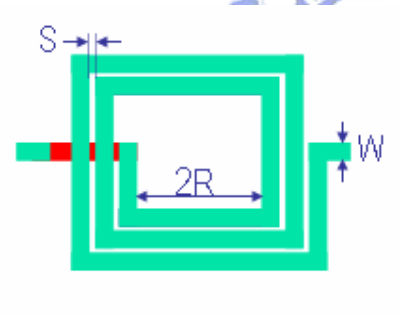
Fig. 4-23 Capacitance-voltage characteristics and circuit model of MOS capacitor

C. Inductors

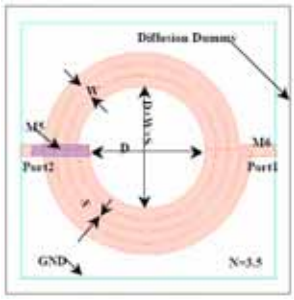
With continuing reduction of the gate length, the unity-current-gain frequency of the active devices in CMOS technology has exceeded 10 GHz. In addition, CMOS possesses the capability to integrate with the baseband circuits. Thus, CMOS technology seems to be an attractive candidate for low-gigahertz (5 GHz) RF applications. Currently, there are several integrated resistor and capacitor options and most of these implementations are easy to model. However, the poor characteristics of the on-chip inductors and transformers become the greatest obstacles to realize the fully integrated transceiver in CMOS technology. Considerable effort has also gone into the design and modeling of inductor implementations, of which the only practical options are bond wires and planar spiral geometries. Although bond wires permit a high quality factor (Q) to be achieved, with typical Q's in the 20–50 range, their inductance values are constrained and can be rather sensitive to production fluctuations. On the other hand, planar spiral inductors have limited Q's, but have inductances that are well-defined over a broad range of process variations. Thus,

planar spiral inductors have become essential elements of communication circuit blocks such as voltage controlled oscillators, low-noise amplifiers, mixers, and intermediate frequency filters.

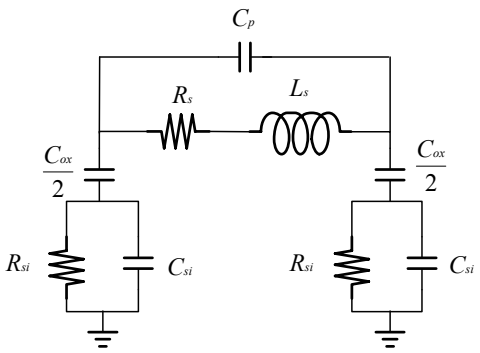
Square spirals are popular because of the ease of their layout. Fig. 4.24 shows the typical layout and device model of the on-chip spiral inductors including square and circular shapes. L_s and R_s represent the inductance and series resistance, respectively. C_p models the parasitic capacitance consisting of the overlap capacitance between the spiral inductor and the underpass metal, and the fringing capacitances between metal wires. The oxide capacitance between the metal wire and the substrate is modeled by C_{ox}. R_{si} and C_{si} are used to model the loss of the silicon substrate.



Spiral square inductor layout



Spiral circular inductor layout (N = 3.5) by UMC 0.18μm CMOS process



$$R_s = \frac{l}{w\sigma\delta(1-e^{-t/\delta})} \quad \text{where } \delta = \sqrt{\frac{2}{\omega\mu_o\sigma}}$$

$$C_p = nw^2\frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{ox} = wl\frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{si} = \frac{1}{2}w \cdot l \cdot C_{sub}$$

$$R_{si} = \frac{2}{wlG_{sub}}$$

Csub and Gsub are fitting parameters.

Fig. 4-24 Layout and equivalent model of spiral inductor

In CMOS technology, the on-chip inductor suffers from some main loss mechanisms:

- Conductor ohmic loss
- Cross-over capacitance
- Oxide capacitance
- Substrate loss
- Magnetically induced Eddy current (Fig. 4-25)

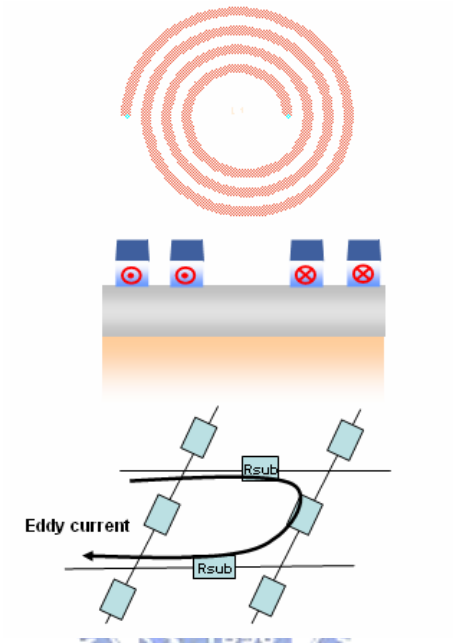
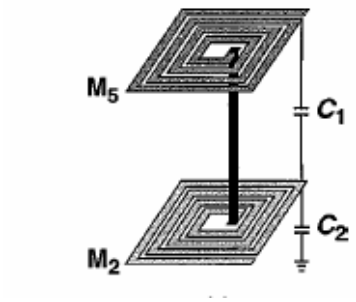


Fig. 4-25 The illustration of eddy current

There are some minor refinements to enhance Q of an inductor, such as thick metallization for lower ohmic loss, High-resistivity silicon substrate, stacking of metal layer to form stacked inductor (Fig. 4-26), patterned ground shield (Fig. 4-27), and so on.



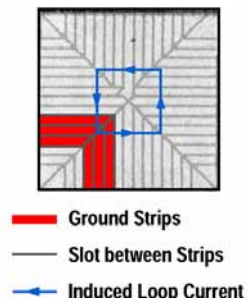


Fig. 4-26 Two-layer stacked inductor[16] Fig. 4-27 Patterned ground shield

D. Transformers

Monolithic spiral transformers have been used in monolithic microwave integrated circuit and silicon radio-frequency integrated circuit designs to perform impedance matching, signal coupling, phase splitting, etc. Specific applications include low-loss feedback and single-ended-to-differential signal conversion, matching, and coupling. Fig. 4-28 shows the layout and schematic symbol.

The operation of a passive transformer is based upon the mutual inductance between two or more conductors, or windings. A monolithic transformer can be realized either by tapping into a series of turns of coupled microstrip lines or by interwinding two identical spiral inductors, as shown in Fig. 4-29(a). The tapped structure can provide an arbitrary turns ratio, but it is not perfectly symmetrical for the 1 : 1 turns ratio case. One approach to transformer modeling follows the inductor modeling approach. Fig. 4-29(b) shows a circuit model for the transformer in Fig.4-29(a). In addition to planar transformer, stacked transformer can be applied to more layers of metal to achieve higher voltage gains, shown in Fig. 4-30.

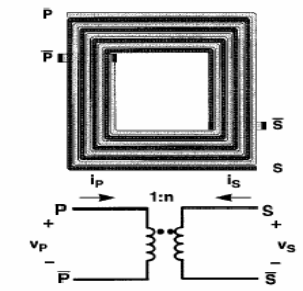


Fig. 4-28 Monolithic transformer (a) Physical layout (b) Schematic symbol

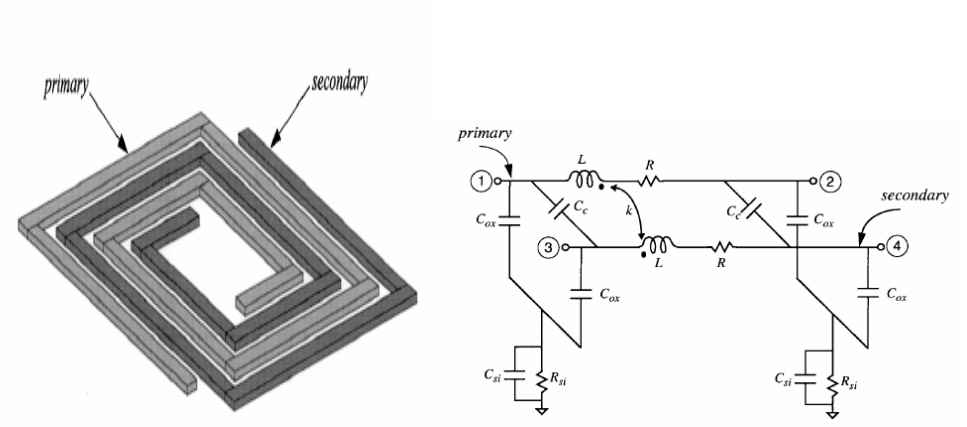


Fig. 4-29(a) Planar transformer layout (b) Transformer model

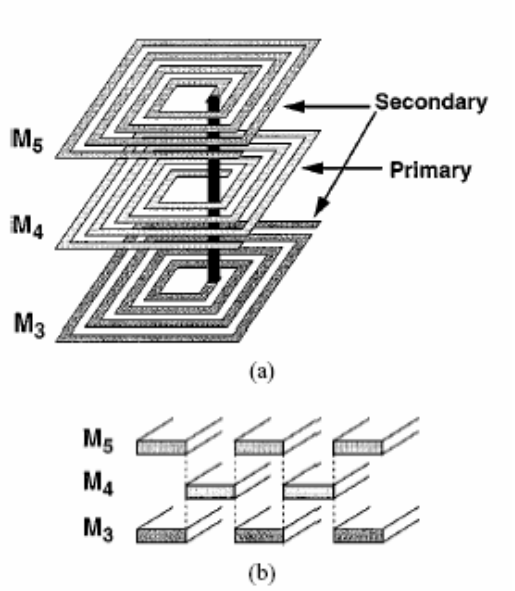


Fig. 4-30 Stacked transformer [17]

Chapter 5
Circuit Design

Based on the dual-band receiver architectures presented in chapter 3, this chapter deals with circuit designs of the receiver frontend, including 2.4/5 GHz receivers for switched dual-band architecture and concurrent dual-band receiver as well as wideband LNA for concurrent dual-band scheme. All those circuits employs the same core circuit, i.e., inductively degenerated low noise amplifier and passive mixer. Hence, the analysis of LNA and mixer will be carried out first before simulating the individual circuit blocks.

5.1 Low Noise Amplifier

The design of LNAs presents considerable challenge due to its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. Although gain, noise figure, stability, linearity and input and output match are all equally important, they are interdependent and do not always work in each other's favor. Minimum noise figure and maximum power gain are nearly impossible to be obtained simultaneously if feedback techniques are not used. In addition, stability is also the desired goal of LNA design. Stability issue is becoming more critical, especially if the LNA is preceded by a filter. Unconditional stability means that with

any load present at the output of the amplifier, the circuit will not become unstable, i.e., will not oscillate. According to the design issues, we will demonstrate how to trade off between those parameters in the next subsections.

5.1.1 Topologies

Although several different topologies have been proposed to implement LNAs, we will only focus on two most common single-stage LNAs in CMOS processes, namely, the common-gate topology and inductively degenerated common-source stage, shown in Fig. 5-1. The common-gate configuration uses the resistive part looking into the source of the transistor to match the input to a well-defined source impedance (e.g., 50Ω). This impedance is $1/(g_m + g_{mb})$ in the case of a MOSFET, where g_m and g_{mb} are transconductance of the top-gate and back-gate transistors, respectively. Thereby, common gate amplifier is suitable for wide-band applications. The minimum noise figure of common gate amplifier is derived as

$$F = 1 + \frac{4kT\gamma / g_m}{4kTR_S} = 1 + \frac{\gamma}{g_m R_S} = 1 + \gamma \tag{5-1}$$

γ is typically 2~3 in short channel device, and thus the NF is lower bounded to 3dB, which is unacceptable in many applications.

In a common-source LNA, inductive degeneration is used to generate the real part needed to match the LNA input to the preceding antenna or filter. The ideal lossless inductive feedback moves the source impedance for optimum NF toward the

optimum power match with a minor increase in the minimum NF. Unfortunately, in silicon implementations, the loss associated with inductors will degrade the NF. Table 5-1 compares the pros and cons of the two topologies.

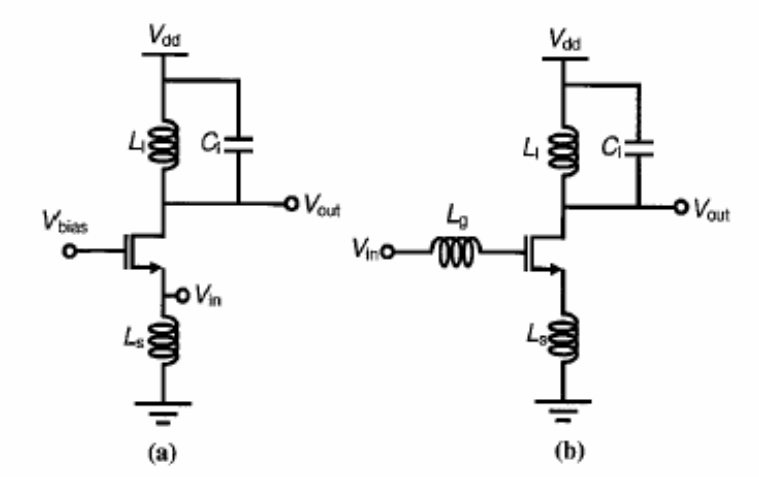


Fig. 5-1 Commonly used single-band CMOS LNAs (a) Common-gate. (b) Common-source with inductive degeneration

TABLE 5-1
The comparisons between common source and common gate topologies

	Common Source	Common Gate
Noise Figure	Lower	Higher
Gain	Higher	Lower
Impedance Matching	Narrower	Broader
Linearity	Better	Worse

5.1.2 Power matching

The input of the LNA is either fed directly by the antenna or is connected to the antenna through a bandpass filter, a diplexer/duplexer, or both. In any case, the impedance looking into the input of the LNA should be power matched (i.e., complex

conjugate matched) to the impedance of the preceding stage for maximum signal power transfer. As shown in Fig. 5-2, it is an inductively degenerated LNA with cascode configuration which can enhance the stability and reverse-isolation of the LNA. The LNA employed in this thesis is also based on that. This LNA incorporates L_s and L_g to create conjugate matching at the input. Eq.5-2 is used to generalize this power match concept. If both input and output are simultaneously conjugate matched to source and load impedance, then, the maximum power gain can be achieved.

$$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} \cdot L_s \approx \omega_T L_s \tag{5-2}$$

$$\omega_T = \frac{g_m}{C_{gs}} \approx \frac{3}{4}\frac{v_{sat}}{L} \quad \text{for short-channel device}$$

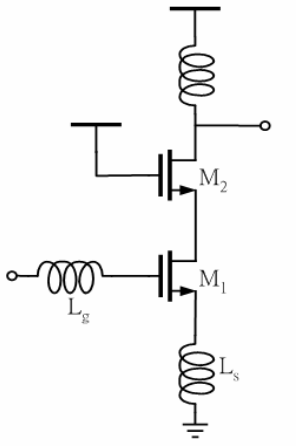


Fig. 5-2 Inductively degenerated LNA

5.1.3 Noise matching

Only the design concepts about noise figure are explained here, and the complex mathematical derivation is referred to [24]. An LNA is a design that minimizes the

NF of the system by matching the device to its noise matching impedance, or Γ_{opt}. Γ_{opt} occurs at impedance where the noise of the device is terminated. All devices exhibit noise energy. To minimize this noise as seen from the output port, one must match the input load (source impedance) to the conjugate noise impedance of the device. Otherwise the noise will be reflected back from the load to the device and amplified. While this gives a minimum noise figure, it often results in slightly reduced gain as well as possibility increasing the potential instabilities. Noise match often comes close to S11 conjugate (S11*) under non-feedback conditions. As a result, the input impedance to the amplifier will not be matched to 50Ω. Therefore, this is a design trade-off between gain and NF.

Except for the complex mathematical analysis, An practical approach is to use Smith charts to find the optimum impedance for noise and power matching at the input of the amplifier for given active devices. Although the Smith chart is a very convenient tool for seeing how close we are to the minimum NF and the maximum gain of a given device, it does not show the effect of individual noise sources on the total NF. This is particularly important for a concurrent multiband LNA, since the same noise sources behave differently at different frequencies. An example is illustrated in Fig. 5-3. We can find the optimum input impedance for complex conjugate matching and noise matching from gain circle and noise circle simulations.

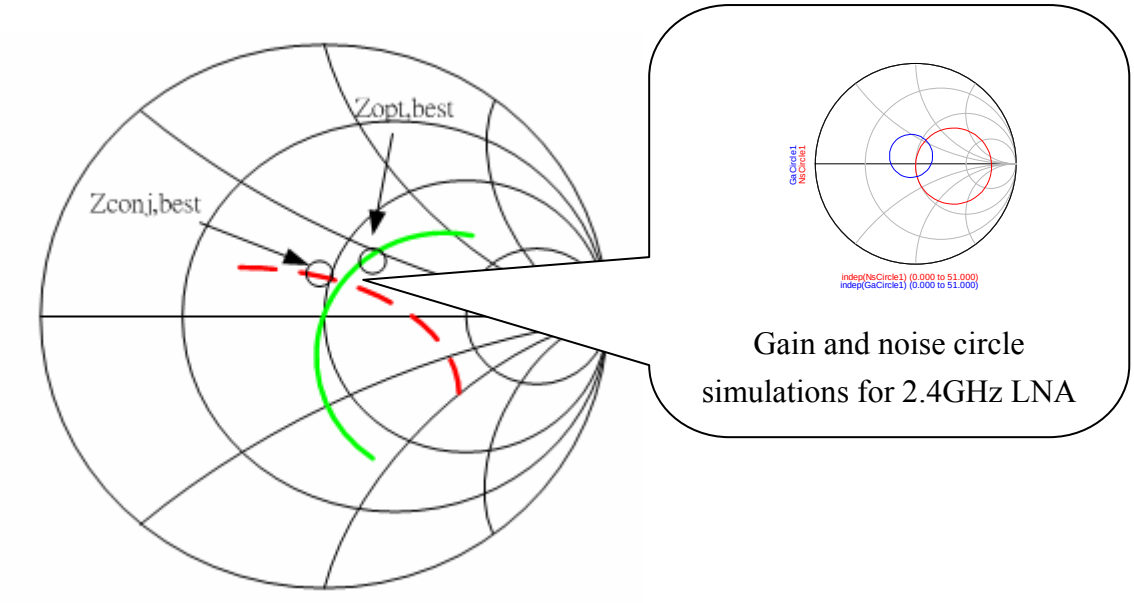


Fig. 5-3 Trade off between power matching and noise matching

5.1.4 Stability

Instabilities are primarily caused by three phenomena: internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess of gain at frequencies outside of the band of operation. The stability factor is often used to characterize the stability of circuits, shown in Eq. 5-3. A stability factor greater than unity and the Δ smaller than unity are required for unconditional stability.

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}||S_{21}|} > 1 \qquad (5\text{-}3)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} < 1$$

5.2 Mixer

In the receiver path, active CMOS mixers are more and more replaced by passive CMOS mixers due to power consumption restrictions. In contrast, the active mixer is still used in the transmit path to get more power gain. In this section, only the design concepts are described just like the preceding section, and the complicated mathematical analysis is referred to [22]. The trade-offs between gain, linearity, and now even the flicker noise in direct conversion receiver needs to be considered when designing a mixer.

5.2.1 Active Mixer

The simplest active CMOS mixer is the single balanced mixer presented in Fig. 5-4(a), and the double balanced one shown in Fig. 5-4(b). They all belong to Gilbert types. One of the most important design criteria is the noise produced by the mixer. Traditional Gilbert mixers focus on balancing high linearity and high voltage gain. However, for direct conversion receiver, additional design issue must be taken into account: the flicker noise. The bias selection of switching stage is restricted by flicker noise and linearity requirements. Thus, the separate bias is proposed to achieve both requirements simultaneously.

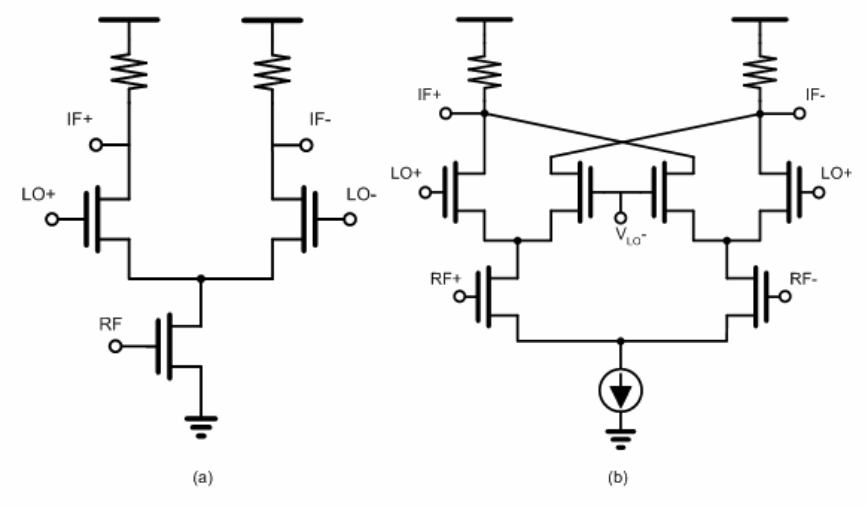


Fig. 5-4(a) Single balanced mixer (b) Double balanced mixer

5.2.2 Passive Mixer

The design of passive mixers seems trivial, because the transistors only act as switches; the larger the transistor sizes, the smaller the on-resistance of the transistor and the better the linearity. However, if the mixer is incorrectly designed, this can lead to an excessive amount of noise. In addition to noise, the major characteristic of passive mixer is the gain loss. But it is also the nature of lossy property that makes passive mixer own high linearity. The other advantage of passive mixers is the zero power consumption and therefore zero DC current leads to low flicker noise. Generally speaking, passive mixer is popular for low power applications.

For low power, low noise, and high linearity consideration, The passive mixer is chosen for this design. However, the loss of mixer must be compensated with additional amplifier; otherwise the noise figure of the latter stage is no longer

negligible, since the Friis equation in (2-1) implies that the noise in latter stage will arise for this reason.

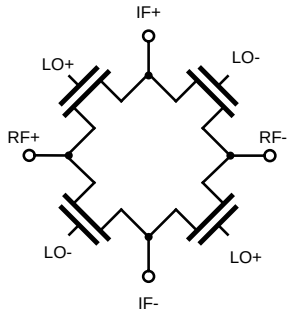


Fig. 5-5 Passive mixer

For a passive mixer shown in Fig. 5-5, the time varying conductance can be modeled as Fig. 5-6 (a), and Fig. 5-6 (b) is its Thevenin equivalent model where

$$v_T(t) = \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} v_{rf}(t) = m(t) v_{rf}(t) \tag{5-4}$$

$$g_T = \frac{g(t) + g(t - T_{LO}/2)}{2} \tag{5-5}$$

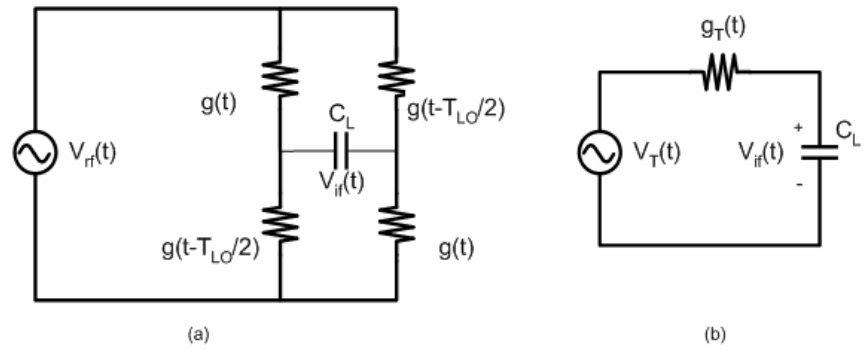


Fig. 5-6 (a) Time varying conductance model for passive mixer (b) Thevenin model of (a)

Note that $m(t)$ shows the frequency conversion behavior and depends on waveform of local oscillator.

$$m(t) = \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} \tag{5-6}$$

5.3 Switched Dual Band Receiver

Based on the above-mentioned inductively degeneration LNA and passive mixer, the 5GHz and 2.4 GHz receiver frontend (Fig. 5-7) are simulated to achieve the circuit specifications listed in Table 2-8. The differential topology is employed to overcome even-order distortion.

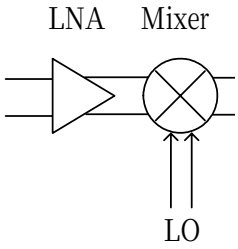


Fig. 5-7 Topologies of receiver frontend in this design

Combing with the individual receiver frontends, the switched dual-band function can be obtained. However, only the 5 GHz receiver frontend is fabricated into a chip due to the shuttle issue provided by UMC. Therefore, in order to justify that if 5 GHz receiver frontend can work, then 2.4 GHz circuit will also work, the 2.4 GHz use the same circuit as 5GHz. Only the component values (device size, bias condition, impedance matching point) are changed. Except for these procedures, the 2.4 GHz circuit employs noise matching to substitute for power matching used in 5 GHz circuit to get lower noise figure and power dissipation.

The power dissipation of the LNA circuit is shown in Fig. 5-8. The simulation of S-parameter and noise figure is shown in Fig. 5-9. Fig. 5-10 illustrates the good

compromise between gain and NF while both power matching and noise matching attain balance. From stability factor and stability measure shown in Fig. 5-11, it follows that the LNAs is unconditionally stable. Fig. 5-12 is the results of P1dB and IIP3. From the simulation results, the 2.4 GHz LNA has a comparable performance compared with the 5 GHz LNA. Table 5-2 lists comparison of some published LNAs at 5 GHz ranges.

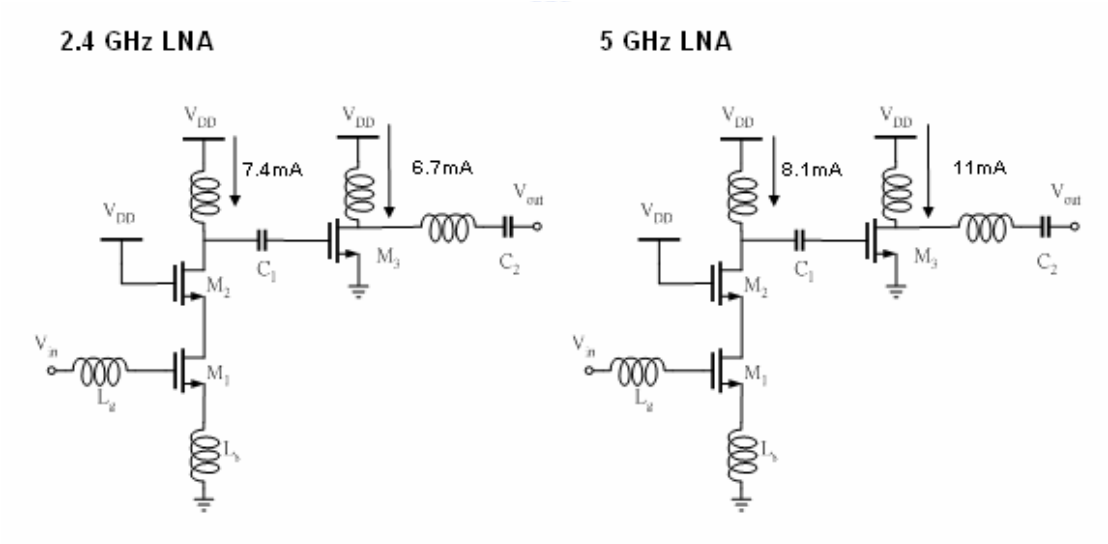


Fig. 5-8 2.4 and 5 GHz LNA circuits

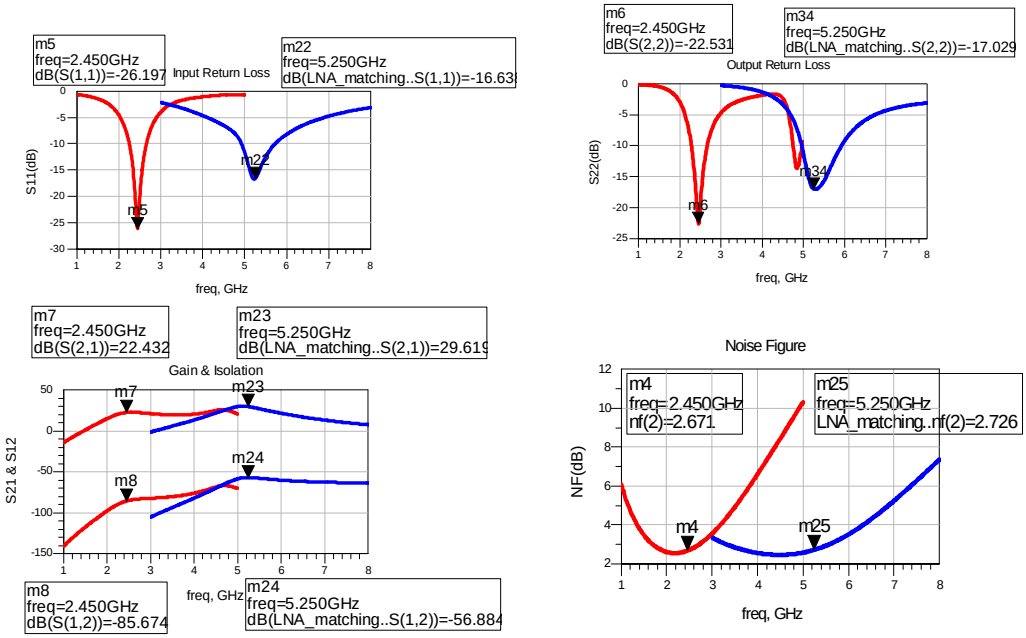


Fig. 5-9 S-parameter and noise figure simulation of switched dual-band LNA

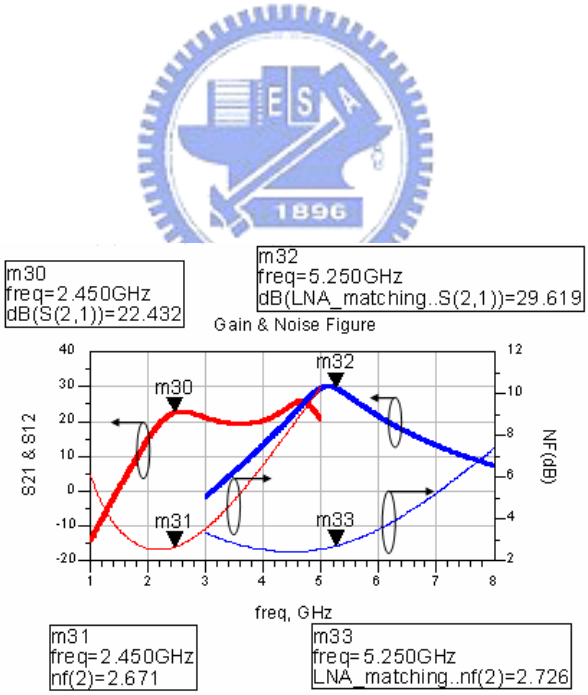


Fig. 5-10 Compromise between gain and NF of switched dual-band LNA

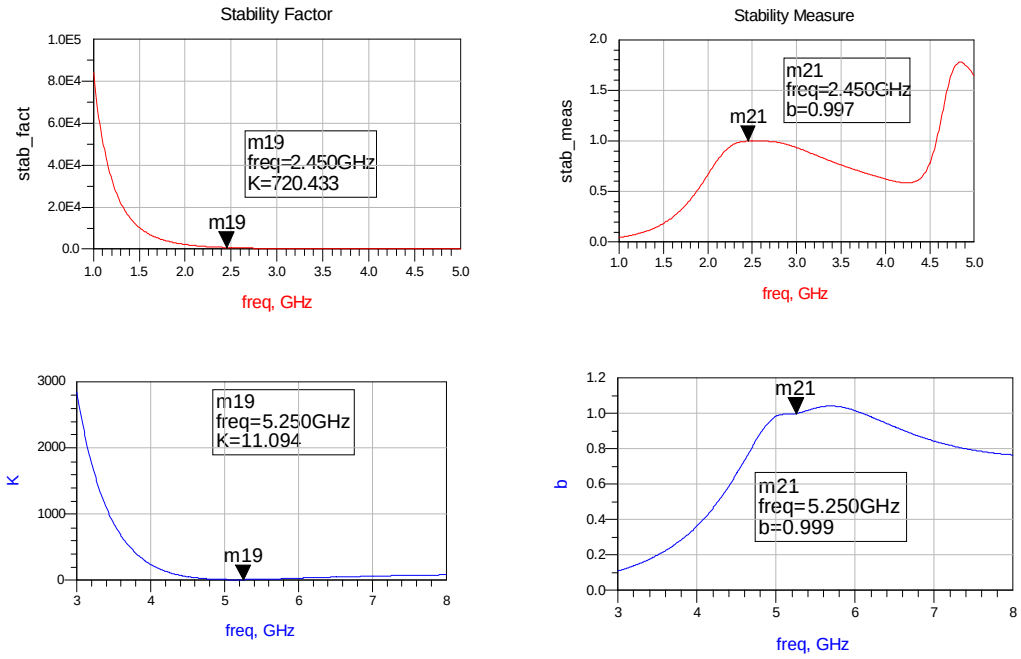


Fig. 5-11 Stability factor of switched dual-band LNA

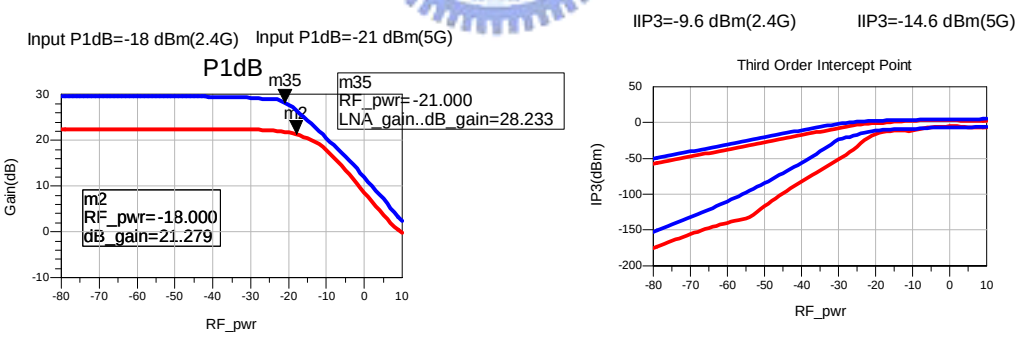


Fig. 5-12 Linearity simulation of switched dual-band LNA

Table 5-2 Comparisons of some published LNAs at 5 GHz ranges

Paper	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	This Work (Simulation)
Freq.(GHz)	5~6	5.2~5.6	5~6	5~5.5	5.25	5.8	5.1	5.1~5.9	5.25
Technology	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS	0.25μm CMOS	0.25μm CMOS	0.18μm CMOS	0.25μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply(V)	1.3	3	2.9	2	3	1	2	1.5	1.8
S11(dB)	-6 ~ -12	N/A	-4 ~ -5	-45 ~ -15	-12.3	-5.3	-12	-19 ~ -13	-16.5
S12(dB)	N/A	N/A	-48 ~ -50	-35 ~ -38	-26.4	N/A	N/A	-113 ~ -110	-56
S21(dB)	8 ~ 4	12 ~ 8	15 ~ 12	11.2~11.7	14	13.2	18(Av)	14.7~14.6	29.6
S22(dB)	-15 ~ -17	N/A	-8 ~ -10	N/A	-11.9	-10.3	N/A	-9.4 ~ -10	-17
IIP3(dBm)	+6.7	-1.5	-6.5	+0.3	-1.5	N/A	N/A	-9.1	-14.6
P1-dB(dBm)	-3.7	-8.7	-19	-8.3	-11.7	-14	N/A	-17.12	-21
NF(dB)	3 ~ 3.2	3.5 ~ 4	2.8 ~ 3.1	2.3 ~ 2.2	2.5	2.5	4.8	2.8 ~3.4	2.7
Power(mW)	20	12	23.2	10	48	22.2	7.2	12.4	34

Both 2.4 and 5 GHz receiver use the same mixer, and only the matching point of LO input is different. The simulation of a 5 GHz mixer is shown in Fig. 5-13. It tells that the passive mixer has a very good linearity, but the price is some gain loss.

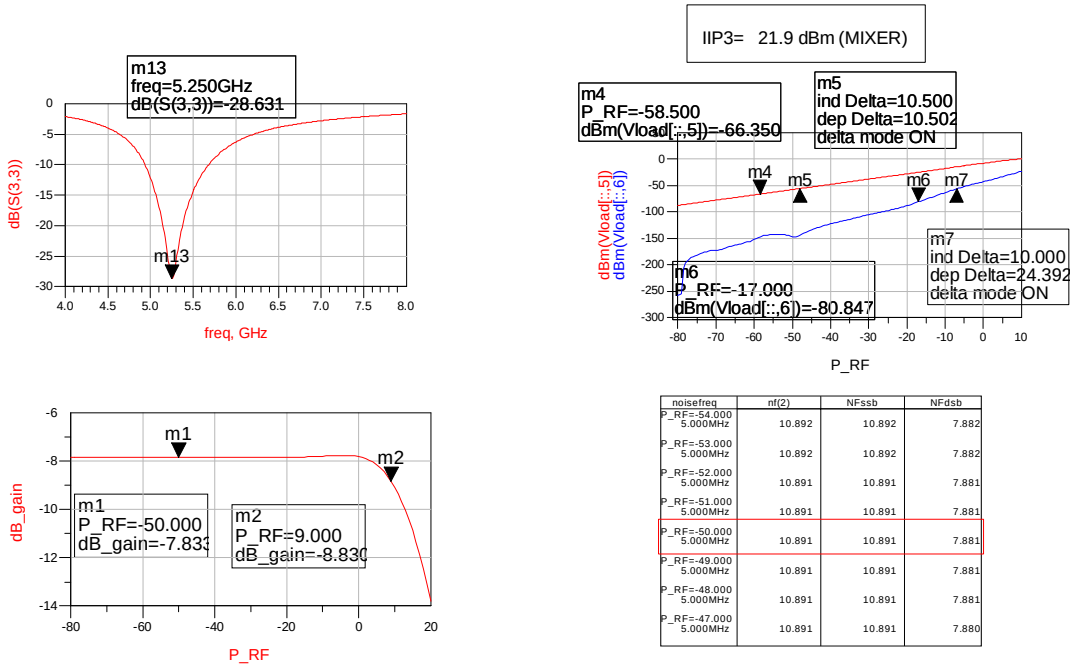


Fig. 5-13 The simulation of 5 GHz mixer

Next, the switched dual-band receiver frontend will be simulated. Again, both 2.4 and 5 GHz receivers use the same circuits. The simplified receiver circuit is drawn in Fig. 5-14. The simulation results of gain, P1dB, IP2, IP3, and input matching of mixer are shown in Fig. 5-15. The matching of the RF input port is the same as LNA, not shown here again. The NF simulation is shown in Fig. 5-16.

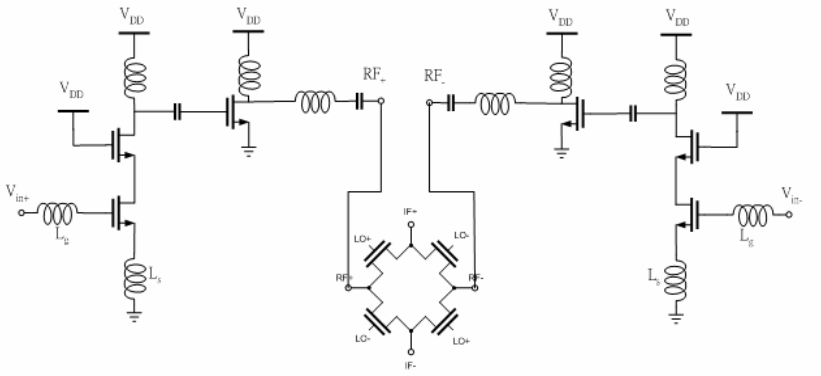


Fig. 5-14 Simplified receiver circuit

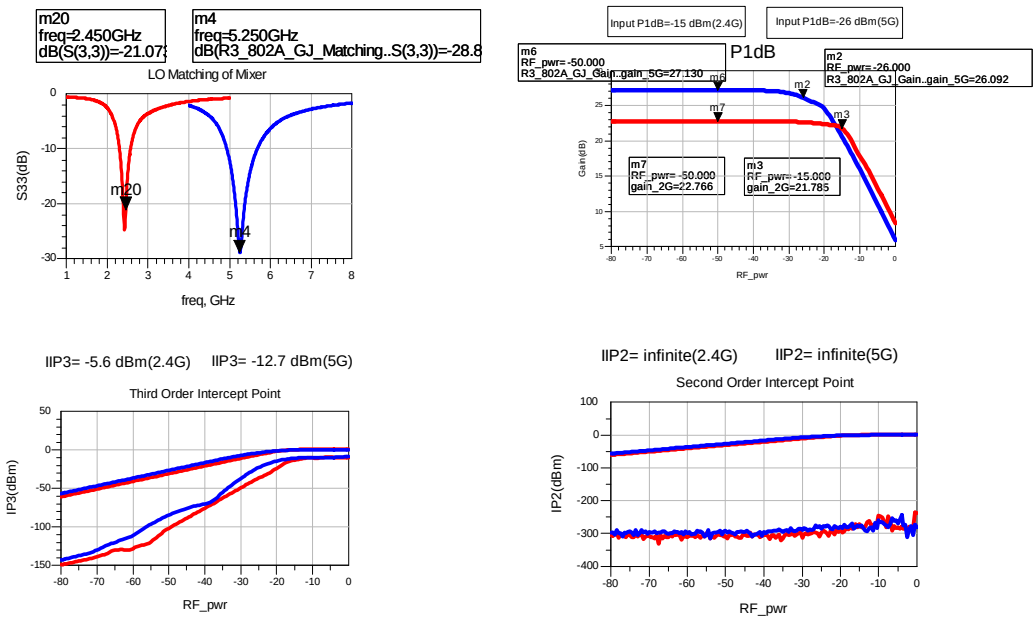


Fig. 5-15 The simulation of switched dual-band receiver circuit

noisefreq	nf(2)	NFssb	NFdsb
RF_pwr=-51.000 5.000MHz	5.767	5.767	2.769
RF_pwr=-50.000 5.000MHz	5.769	5.769	2.770
RF_pwr=-49.000 5.000MHz	5.770	5.770	2.772
RF_pwr=-48.000 5.000MHz	5.773	5.773	2.774
RF_pwr=-47.000 5.000MHz	5.775	5.775	2.777

noisefreq	nf(2)	NFssb	NFdsb
RF_pwr=-51.000 5.000MHz	5.807	5.807	2.737
RF_pwr=-50.000 5.000MHz	5.808	5.808	2.738
RF_pwr=-49.000 5.000MHz	5.809	5.809	2.740
RF_pwr=-48.000 5.000MHz	5.812	5.812	2.742
RF_pwr=-47.000 5.000MHz	5.814	5.814	2.745

Fig. 5-16 NF simulation of switched dual-band receiver circuit at IF = 5 MHz

5.4 Concurrent Dual Band Receiver

A dual-band LNA that can simultaneously provide gains and matching at 2.4 and 5 GHz is designed. The concurrent dual-band LNA can be revised from the single-band LNA shown in Fig. 5-8 and the circuit is depicted in Fig. 5-17. The source inductor provides wideband impedance of 50Ω, and the series and parallel resonator

circuits resonate at 2.4 and 5 GHz simultaneously. Therefore, a concurrent function is achieved. In addition to 5 GHz receiver frontend, another circuit fabricated in this thesis is the packaged concurrent dual-band LNA. The simulation of S-parameter and NF is shown in Fig. 5.18. The comparisons with the published papers are listed in Table 5-3.

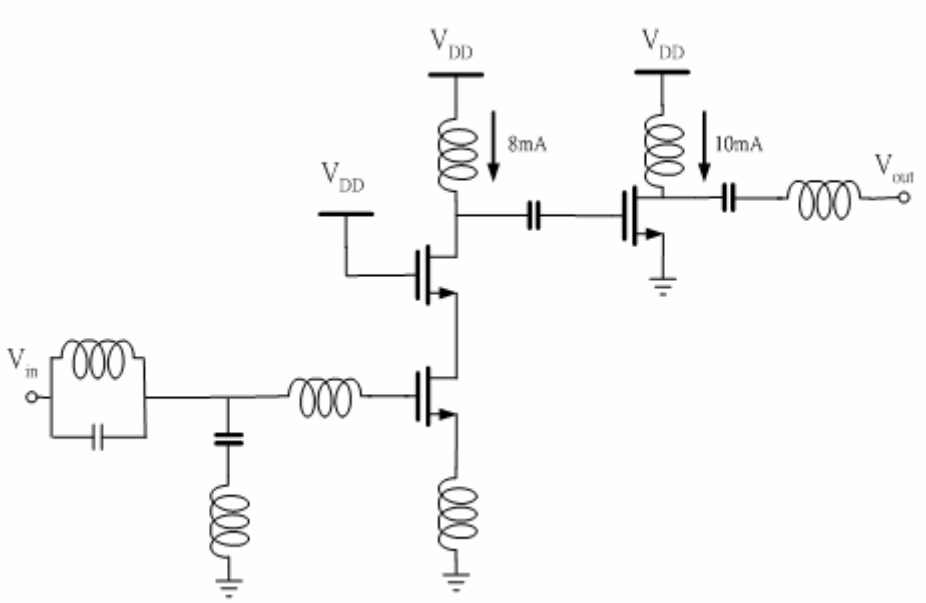


Fig. 5-17 Simplified concurrent dual-band LNA

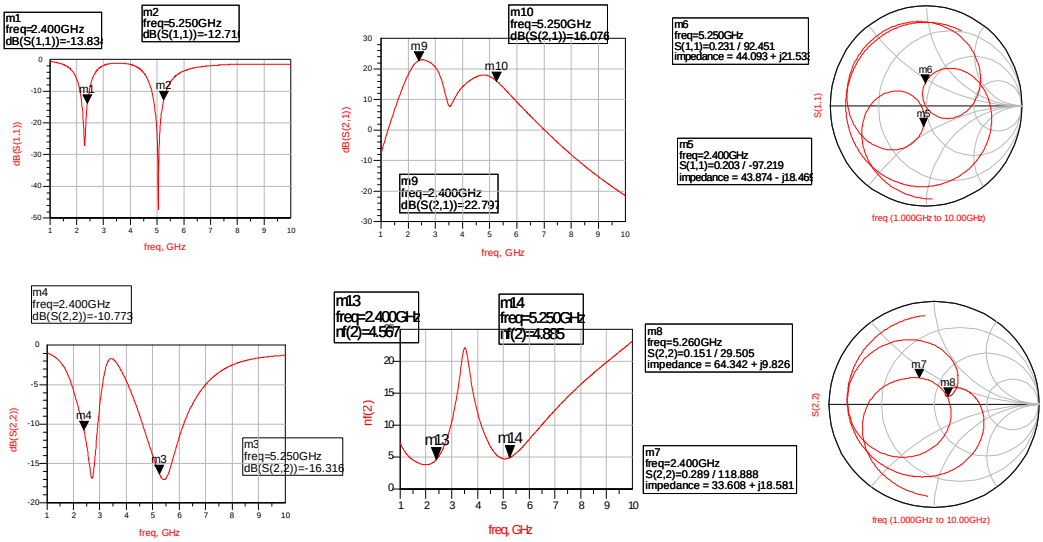


Fig. 5-18 The S-parameter and NF simulation (concurrent dual-band LNA)

Table 5-3 Comparisons between published papers and concurrent dual-band LNA

Paper	[10]		[11]		This work (Simulation)	
Technology	0.18μm CMOS		0.35μm CMOS		0.18μm CMOS	
Power Consumption	14.2mW@1V 6.2mW@0.7V		10mW@2.5V		32mW@1.8V	
Center Frequency	2.4 GHz	5 GHz	2.45 GHz	5.25 GHz	2.4 GHz	5.25 GHz
Power Gain (S21)	11.6dB@1V 8.5dB@0.7V	10.8dB@1V 5.5dB@0.7V	14dB@2.5V	15.5dB@2.5V	22.8	16.1
Input Matching (S11)	-5.1dB (on-chip)	-26.3dB (on-chip)	-25dB (off-chip)	-15dB (off-chip)	-13.8dB (off-chip)	-12.7dB (off-chip)
Noise Figure	2.3dB	2.9dB	2.3dB	4.5dB	4.5dB	4.8dB
Input P1dB	-7.9dBm	-7.1dBm	-8.5dBm	-1.5dBm	-12dBm	-8dBm

Combining the concurrent dual-band LNA with the same passive mixer which has concurrent input matching of LO port, the simulation of the concurrent dual-band receiver is shown from Fig. 5-19~5-22.

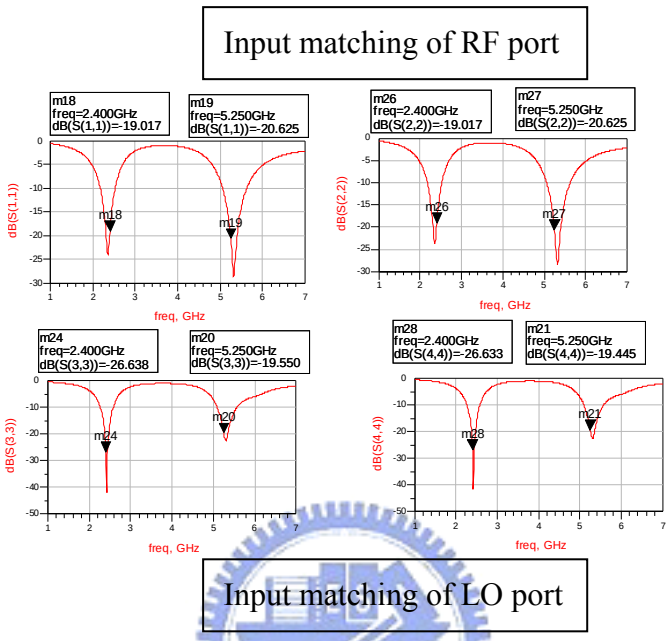
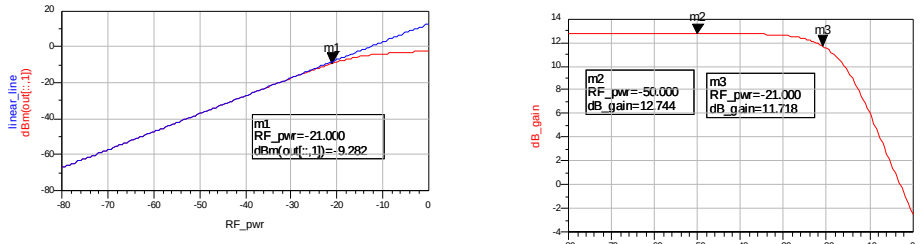
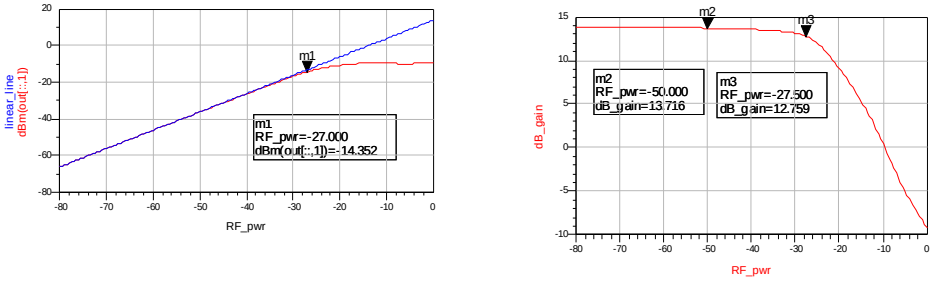


Fig. 5-19 The input matching of differential RF and LO port (concurrent dual-band receiver)



(a) 5 GHz Rx



(b) 2.4 GHz Rx

Fig. 5-20 The gain and P1dB simulation (concurrent dual-band receiver)

noisefreq	nf(2)	NFssb	NFdsb
RF_pwr=-52.000 5.000MHz	7.620	7.620	4.627
RF_pwr=-51.000 5.000MHz	7.624	7.624	4.630
RF_pwr=-50.000 5.000MHz	7.628	7.628	4.634
RF_pwr=-49.000 5.000MHz	7.632	7.632	4.639
RF_pwr=-48.000 5.000MHz	7.639	7.639	4.645

noisefreq	nf(2)	NFssb	NFdsb
RF_pwr=-52.000 5.000MHz	8.271	8.271	5.238
RF_pwr=-51.000 5.000MHz	8.271	8.271	5.238
RF_pwr=-50.000 5.000MHz	8.271	8.271	5.238
RF_pwr=-49.000 5.000MHz	8.271	8.271	5.239
RF_pwr=-48.000 5.000MHz	8.272	8.272	5.239

Fig. 5-21 NF simulation of concurrent dual-band receiver at IF = 5 MHz

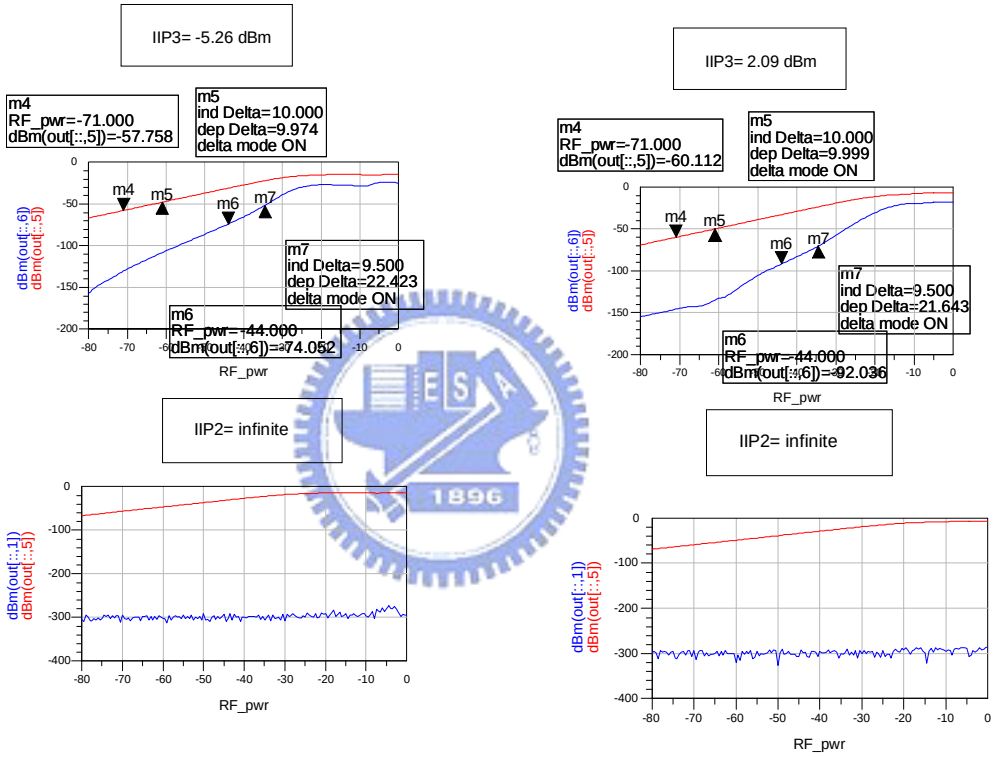


Fig. 5-22 IP3 and IP2 simulation of concurrent dual-band receiver

From the preceding simulation results, the switched dual-band receiver has better performance than the concurrent one. But the most important advantages of concurrent dual band consist in its accommodation for both switched and concurrent operation as well as its area-efficiency. The comparison of switched and concurrent dual-band receiver is listed in Table 5-4.

Table 5-4 The summaries of simulation between switched and concurrent dual-band receiver

	Switched		Concurrent	
	2.4 GHz	5.25 GHz	2.4 GHz	5.25 GHz
Voltage gain(dB)	22.8	26.1	13.7	12.7
P1dB(dBm)	-12	-26	-27	-21
IIP3(dBm)	-5.6	-12.7	-5.26	2.09
IIP2(dBm)	∞	∞	∞	∞
NF(dB)	5.77	5.81	7.63	8.27

5.5 Wideband LNA

In this section, a wideband LNA suited for the architecture shown in Fig. 3-16 is presented and simulated. The circuit is depicted in Fig. 5-23. But this design needs a transformer in both input and output, because the matching technique is different from the previous circuits (single-band LNA and dual-band LNA). It can be divided into two steps shown in Fig. 5-24 and described as follows:

Step-1: Move and compress wideband frequency sweep to real impedance axis of Smith Chart

Step-2: Use impedance transformation to shift the compressed region to the center of Smith Chart

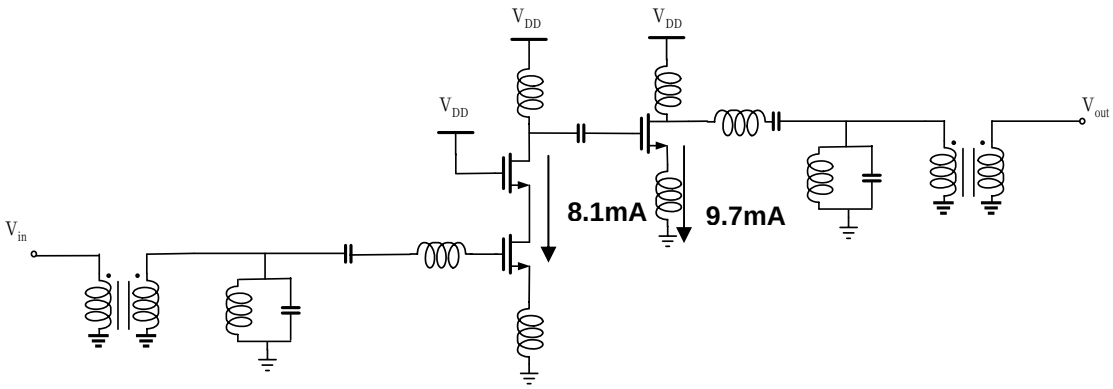


Fig. 5-23 The ideal wideband LNA covering 2.4 and 5 GHz band

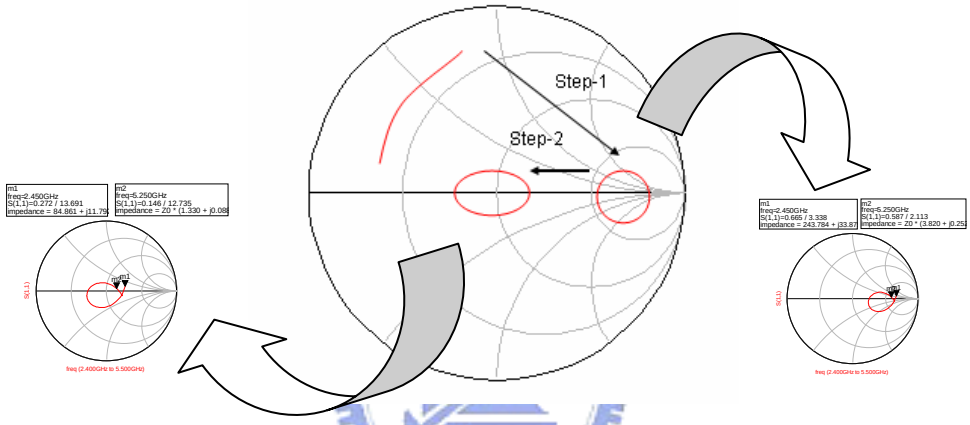


Fig. 5-24 Matching techniques of a wideband LNA

The planar or stacked monolithic transformer mentioned in chapter 3 can be used in this circuit to perform impedance transformation, but unfortunately the foundries cannot provide transformer device models. Hence, the ideal transformer model is employed to complete the simulation (other devices are still from UMC 0.18 μm CMOS process except for the transformers). From the simulations shown in Fig. 5-25~5-26, we can see the most ideal performance which this kind of wideband LNA can achieve. The real performance of the practical circuit is dependent on the Q value of the available monolithic transformers.

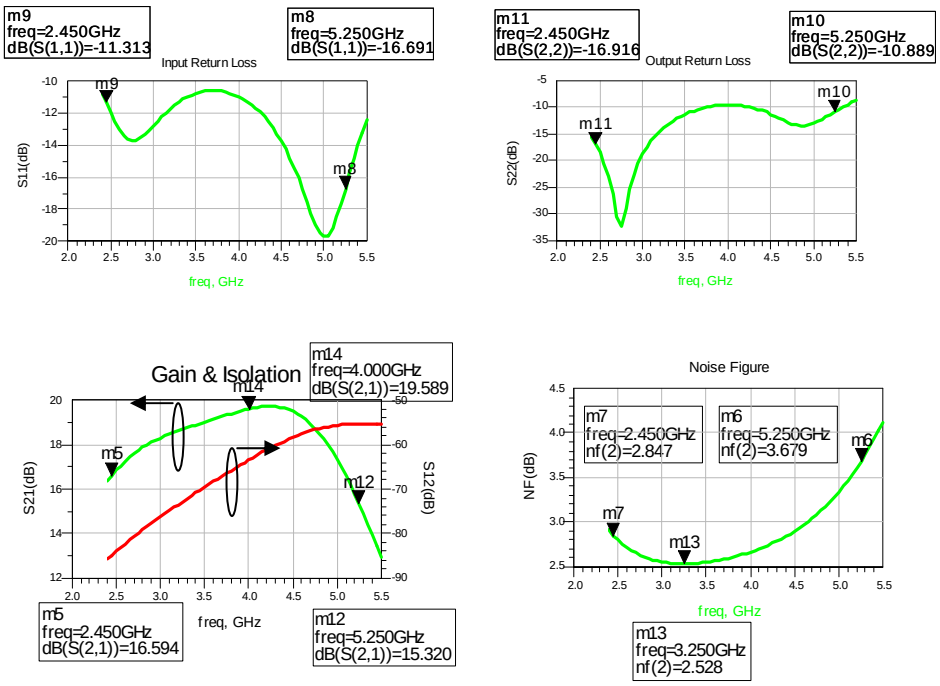


Fig. 5-25 The S-parameter and NF simulation of the ideal wideband LNA

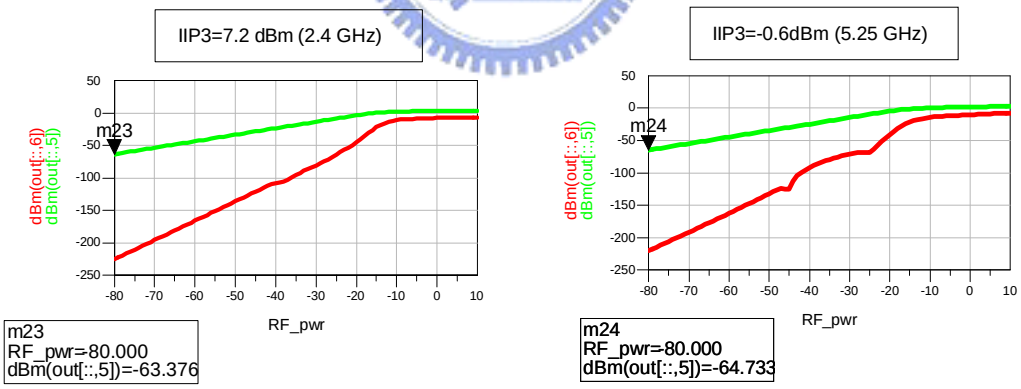


Fig. 5-26 IP3 simulation of the ideal wideband LNA

However, there is another approach that can attain the impedance transformation without transformers, which only utilizes the devices provided by UMC 0.18 μm CMOS process currently. It can be implemented by the capacitor-tapped impedance

transformation, shown in Fig. 5-27. The relation between C_1 and C_2 is determined by the ratio of R_S and R_L; meanwhile, the inductor is utilized to cancel the reactance produced by capacitors. The operation frequency decides the relation among C_1, C_2 and L, as shown in Eq. 5-7.

$$f = \frac{1}{2\pi\sqrt{LC_T}} \qquad C_T = \frac{C_1 C_2}{C_1 + C_2} \qquad \frac{C_1}{C_2} = \frac{R_S}{R_L} \tag{5-7}$$

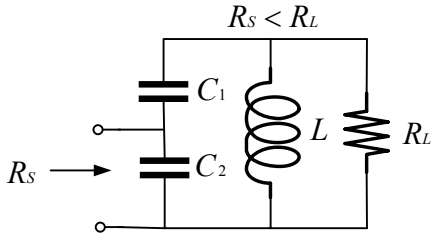


Fig. 5-27 Capacitor-tapped impedance transformation technique

Now we can simulate the practical wideband LNA (Fig. 5-28) in comparison with the one shown in Fig.5-23. The simulation of the circuit is shown in Fig. 5-29~5-30. Compared with the recently published papers relating to wideband LNA [18][19], this work is fairly acceptable.

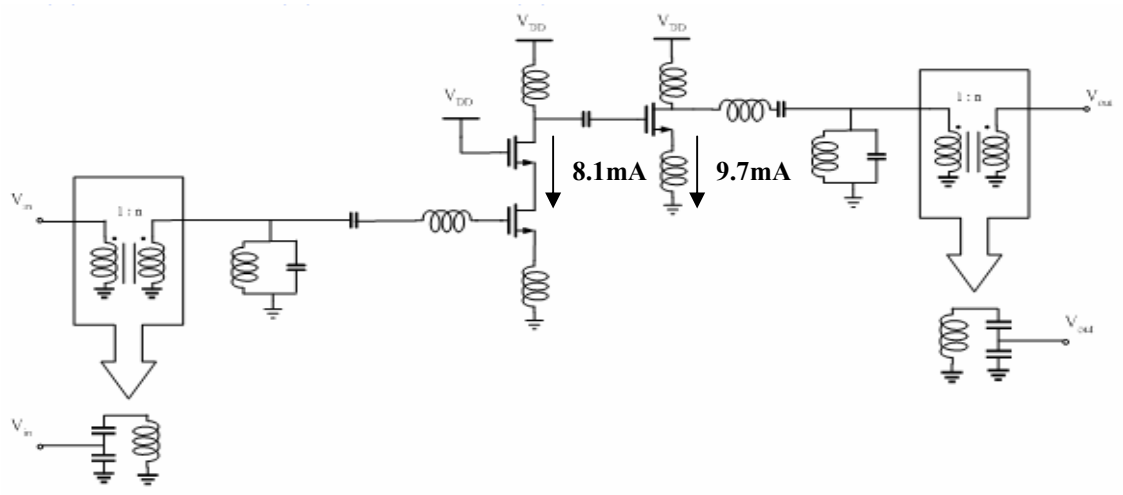


Fig. 5-28 The practical wideband LNA covering 2.4 and 5 GHz band

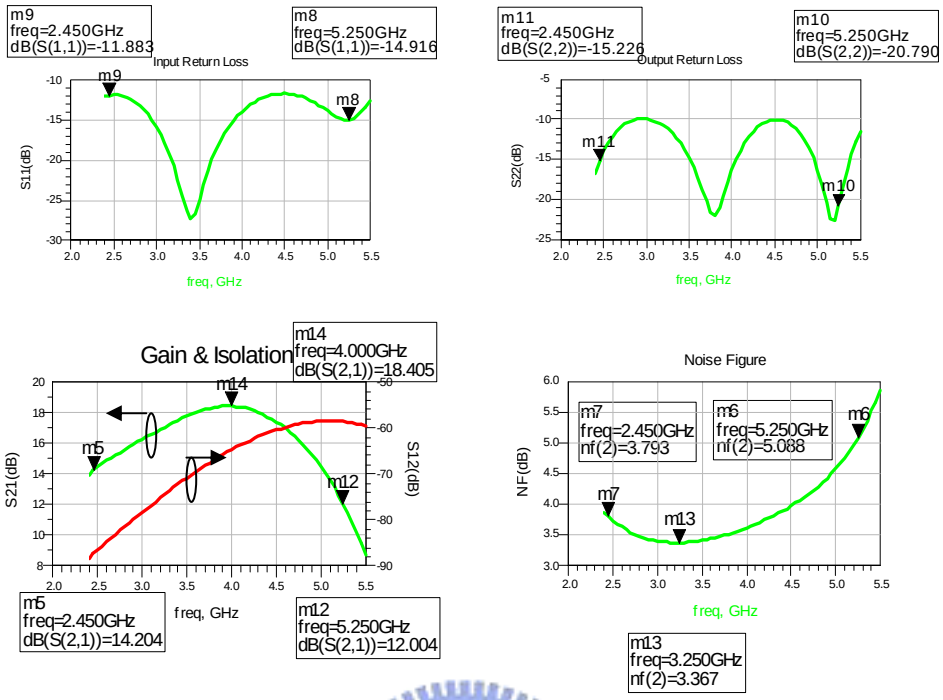


Fig. 5-29 S-parameter & NF simulation of the practical wideband LNA

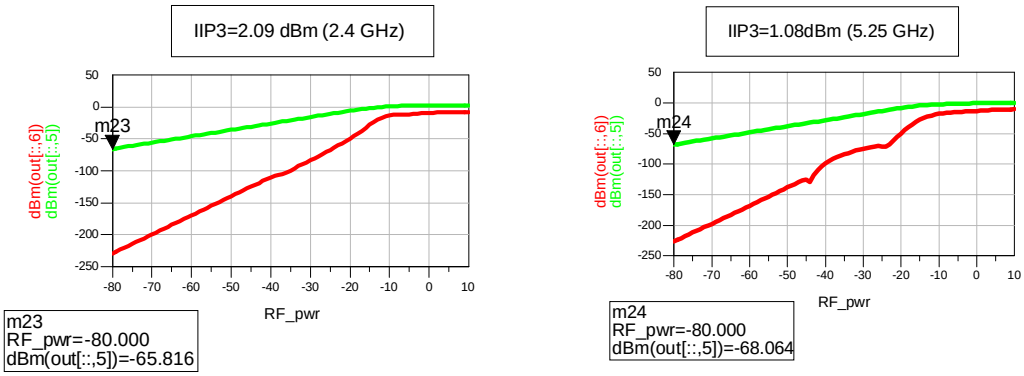


Fig. 5-30 IP3 simulation of the practical wideband LNA

The noise figure and gain of the practical wideband LNA has a little degradation compared with the ideal one, and this is duo to the passive impedance transformation circuits in input and output port. But it is still tolerant in comparison with the two papers [18] [19]. The summary between ideal and practical wideband LNA is listed in Table 5-5.

Table 5-5 Comparisons of the ideal and practical wideband LNAs

	Wideband LNA	
	Ideal	**Practical**
S11(dB)	-11@2.45GHz -17@5.25GHz	-12@2.45GHz -15@5.25GHz
S22(dB)	-17@2.45GHz -11@5.25GHz	-15@2.45GHz -20@5.25GHz
S21(dB)	16.6@2.45GHz 15.3@5.25GHz	14.2@2.45GHz 12@5.25GHz
S12(dB)	-86@2.45GHz -55@5.25GHz	-88@2.45GHz -58@5.25GHz
NF(dB)	2.8@2.45GHz NFmin=2.5@3.25GHz 3.7@5.25GHz	3.8@2.45GHz NFmin=3.37@3.25GHz 5.1@5.25GHz
IIP3(dBm)	7.2@2.45GHz -0.6@5.25GHz	2.09@2.45GHz 1.08@5.25GHz

Chapter 6
Chip Implementation

The two fabricated chips in this thesis are the 5 GHz receiver frontend and the concurrent dual-band LNA (Fig. 6-1). This chapter deals with the layout, ESD protection, package, testing plan issues.

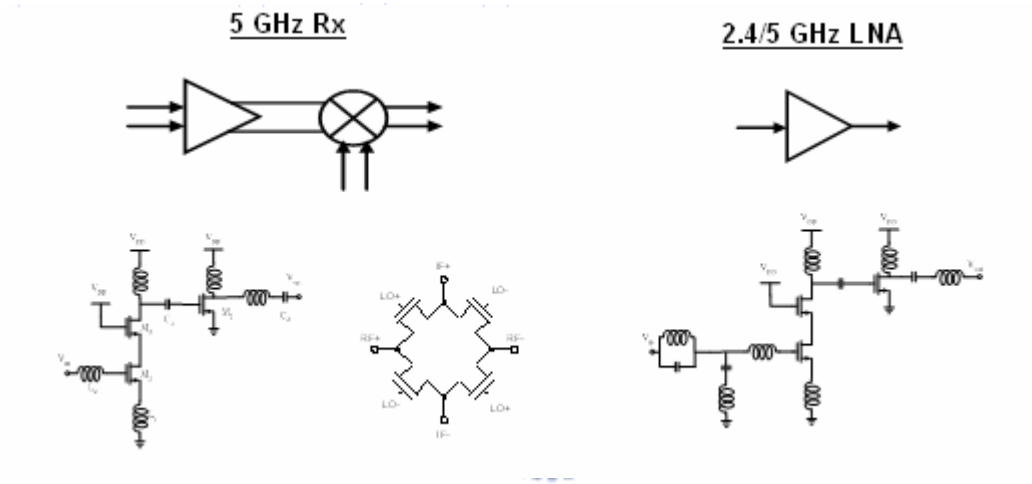


Fig. 6-1 Fabricated circuits in this thesis

6.1 Layout Consideration

Layout and process variation always dominate the performances in many kinds of analog circuits, especially in RF circuits. The layout principle is to decrease parasitic effects including capacitance and inductance. As the operation frequency is getting higher (e.g. over 10 GHz), the interconnect transmission effect cannot be neglected. Placing devices around a common central point is known as common centroid placement, adopted in the 5 GHz band receiver chips. The common centroid

technique (Fig. 6-2) is very good at reducing the effect of thermal or process linear gradients that may be present in an integrated circuit. A thermal gradient, for instance, is generated by a hot spot on the chip that can change the electrical characteristic of a device. Devices close to the hot spot will be affected more than devices that are further away. This technique distributes the gradient effect more evenly among the devices. The IC layout of the 5 GHz receiver and dual-band LNA is shown in Fig. 6-3.

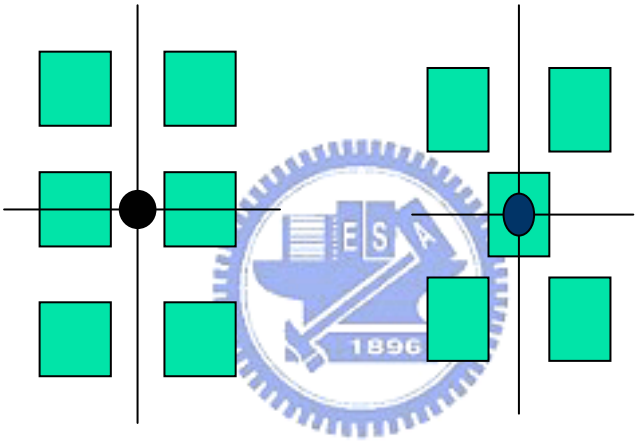


Fig. 6-2 Common centroid layout

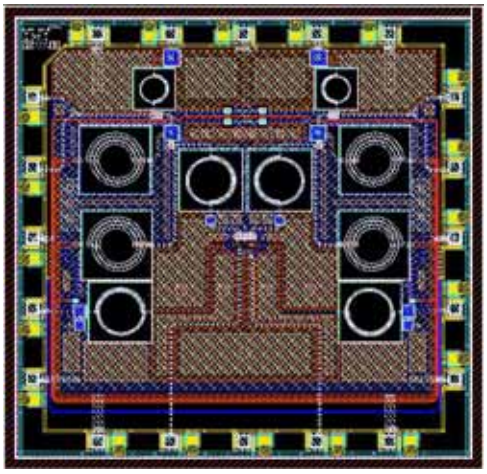
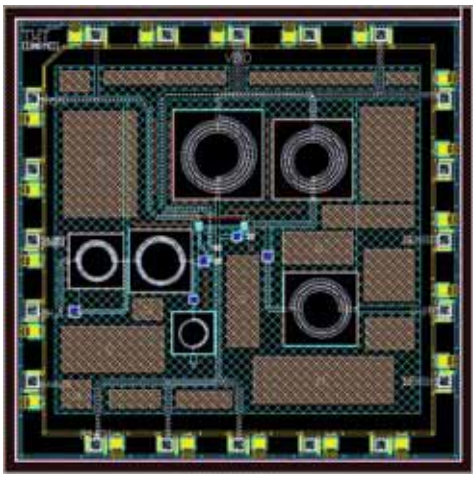


Fig. 6-3(a) 5GHz receiver frontend (packaged)
Die size: 2.5μm×2.5μm



(b)2.4/5GHz dual-band LNA (packaged)
Die size: 2.5μm×2.5μm

In addition to IC layout, the PCB layout is another important consideration. Since the RF circuits operate in several GHz, the wavelength is only in the order of centimeters. In the microwave viewpoint, the wave flows through the metal line, changing its phase according to both wave and wire length. In the electronics perspective, the phenomenon of phase change can be modeled as capacitance and inductance.

As mentioned above, since the wave length is short in RF frequency, the differential layout must be exactly fully symmetric to avoid phase difference and ensuring maximum CMRR. Overlapping of metal line is also prohibited. If they must be crossed, the influence must be taken into consideration. Besides the forementioned concerns, the step change in width should not be too abruptly because that would produce some parasitic effects, shown in Fig. 6-4. Avoiding perpendicular bending is also important, and hence, the turning used in Fig. 6-5(b) is better than Fig. 6-5(a).

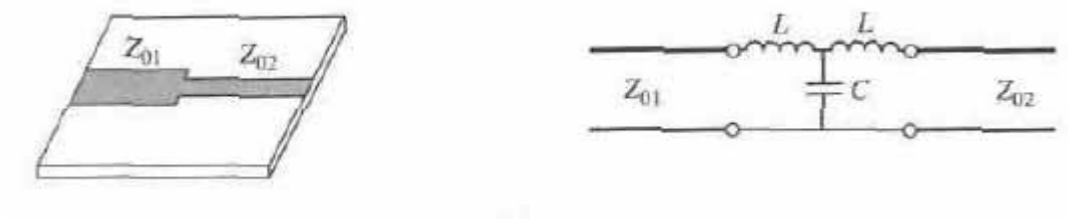


Fig. 6-4 Parasitic effects caused by microstrip discontinuities

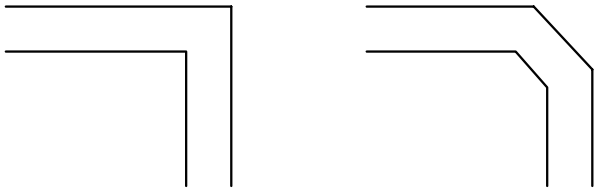


Fig. 6-5 The PCB layout technique

Because the 5 GHz receiver circuit employs differential topologies, both the RF port and LO port need a differential input signals. Therefore an accurate balun is needed to be placed in RF and LO input of the chip. The EM simulation of a 180° microstrip ring hybrid is shown in Fig. 6-6. The fabricated balun and its simulation are shown in Fig. 6-7. Its phase is very accurate and its impedance is also matched to 50Ω. The board design of the two chip is shown in Fig. 6-8.

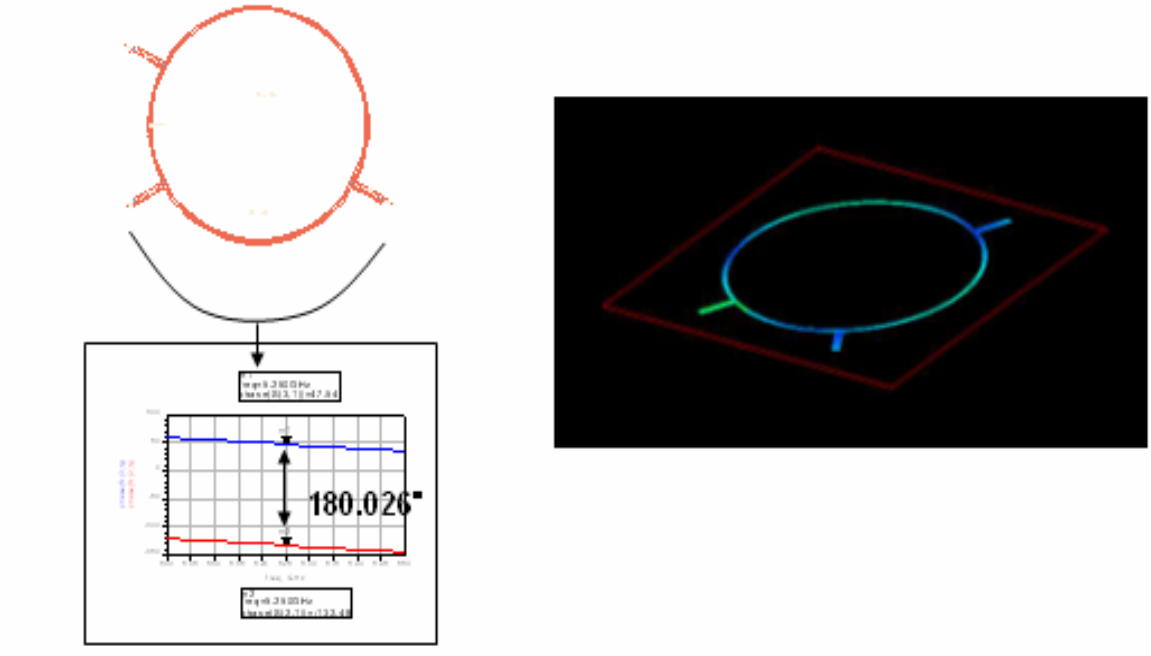
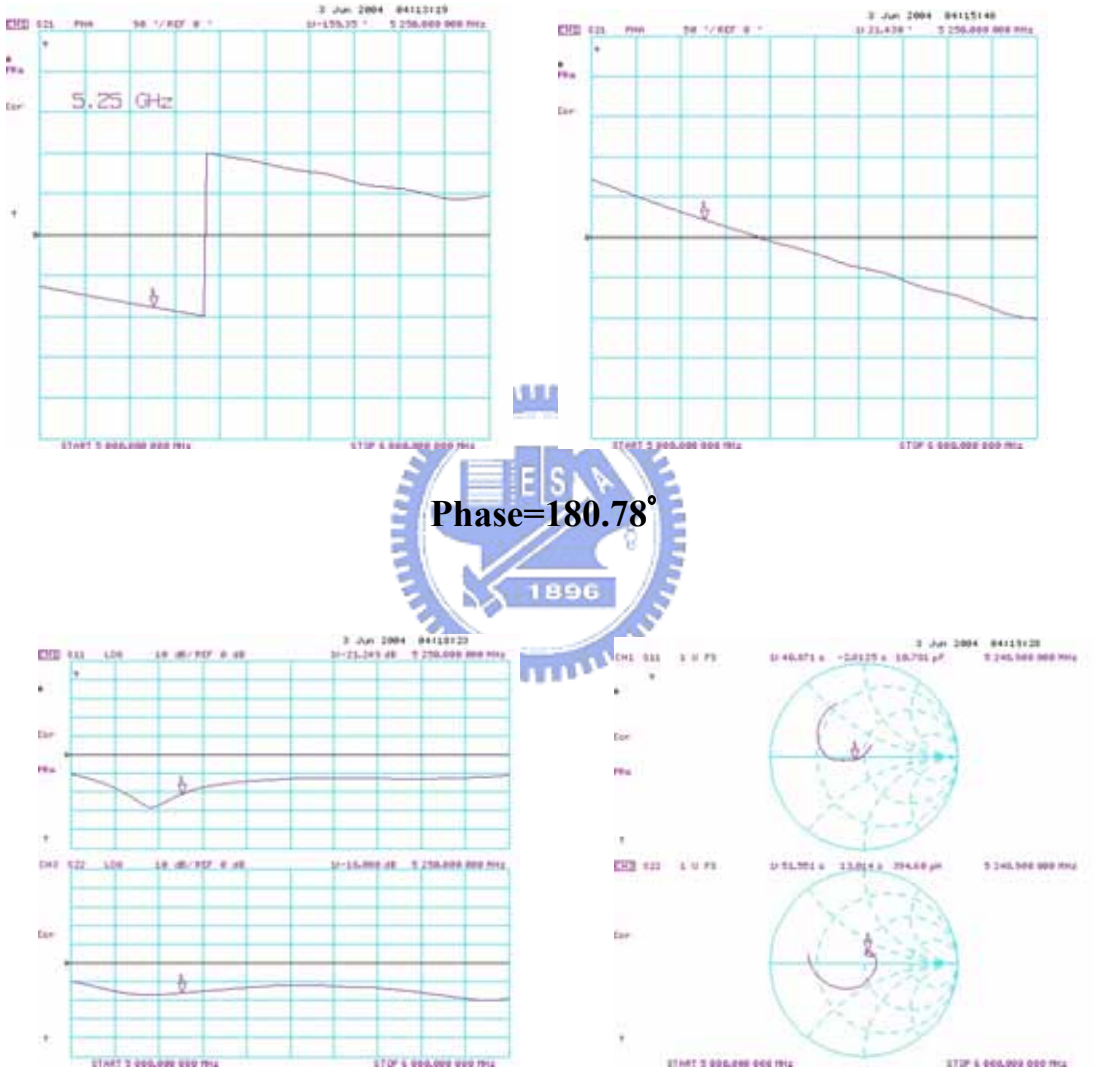


Fig. 6-6 The EM simulation of a 180° balun



Phase=180.78°

Impedance=~50Ω

Fig. 6-7 The phase and impedance measurements of a 180° balun

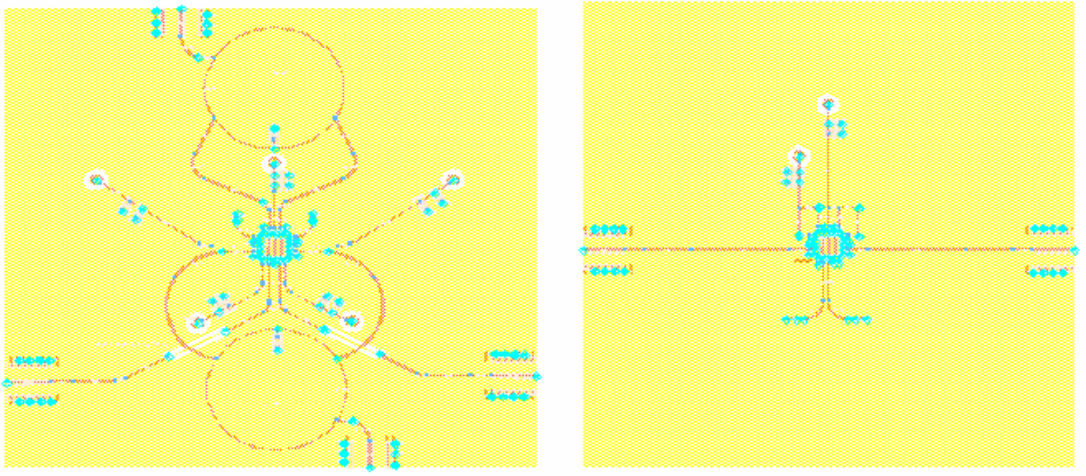


Fig. 6-8 Board design of (a) 5GHz receiver frontend (b) 2.4/5GHz dual-band LNA

6.2 ESD Protection

For 0.18μm process, the voltage limit that gate oxide can tolerate is only about 5V. Without any protection circuit, the MOSFET can be damaged permanently in about 10V potential applied to gate. Fig. 6-9 illustrates the most popular ESD protection circuits in commercial use. If a positive ESD pulse occurs at I/O pins, the upper diode chain will turn on to lead the ESD charge flow from ESDVDD to ESDGND through a gate-grounded NMOS, whereas a negative ESD pulse will forward bias the lower diode chain. The breakdown mechanism of the gate-grounded NMOS is that large ESD pulse makes the NMOS operate in snapback region to conduct a large current, shown in Fig 6-10. The ESD circuits provided by UMC ensure 3.6kV in human body mode (HBM) test but induce about 40fF nonlinear capacitance in each pad.

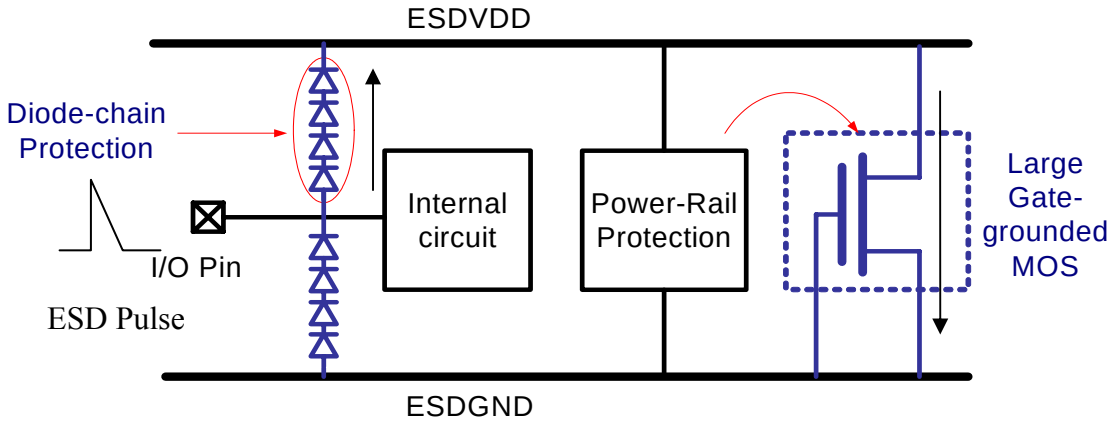


Fig. 6-9 ESD protection circuits

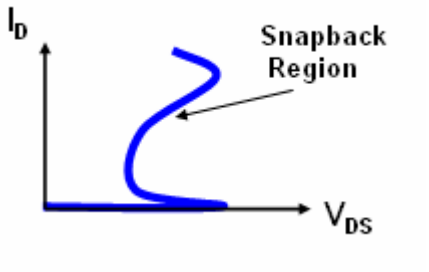


Fig. 6-10 I-V characteristic of gate-grounded NMOS

6.3 Package and Modeling

The package used for this design is QFN20D which is provided by SPIL™ and modeled in 5 GHz frequency. The package model for bond-wire is built as Fig 6-11.

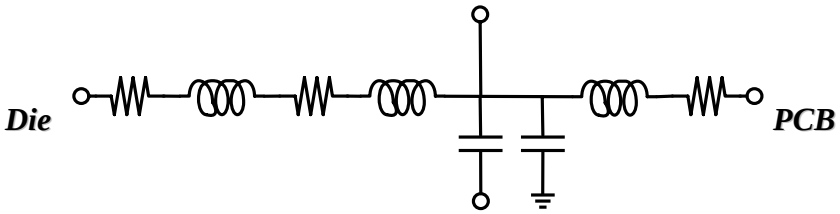


Fig. 6-11 Package model

The most important issue is serial inductance and parasitic capacitance between pads. The serial inductance results in a non-ideal ac ground in DC supply while the capacitance between pads causes adjacent pin coupling. This would make the ground of the chip not equal to that of the board. In some cases, it can even cause a feedback oscillation from output to input port. The bond-wire serial inductance is about 1nH/mm and has a high quality factor compared with on-chip inductors. Hence, if the bond wire inductor is properly used, it can enhance the circuit performance; otherwise, it would cause performance degradation. For adjacent pin coupling, a simulation result shown in Fig. 6-12 reveals about -14dB coupling between pads, which is critical to layout design. The signal pads shall be separated as far as possible, and some dc pads such as GND/VDD/Bias must be interleaved.

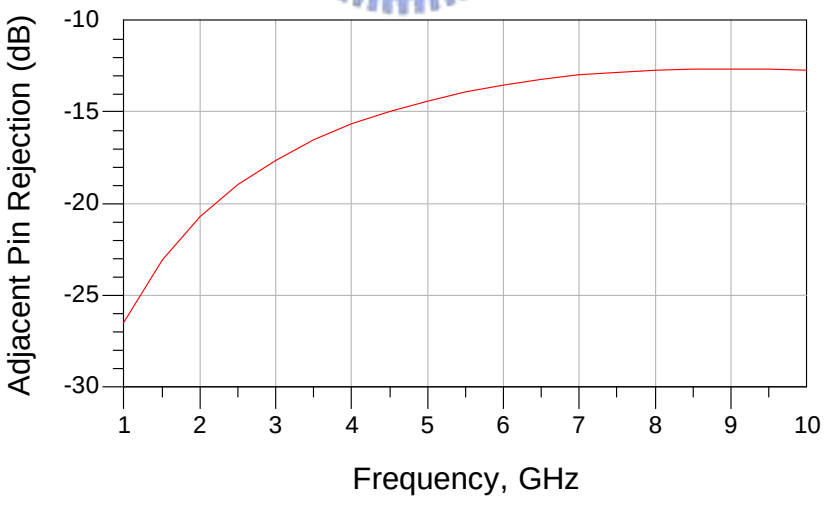


Fig. 6-12 Pin-to-Pin isolation for package model

Chapter 7

Measurement

This chapter will deal with the measurements of 5 GHz receiver frontend including packaged and on-wafer versions as well as 2.4/5 GHz dual-band LNA. Fig. 7-1 shows the measurement environment in this design.

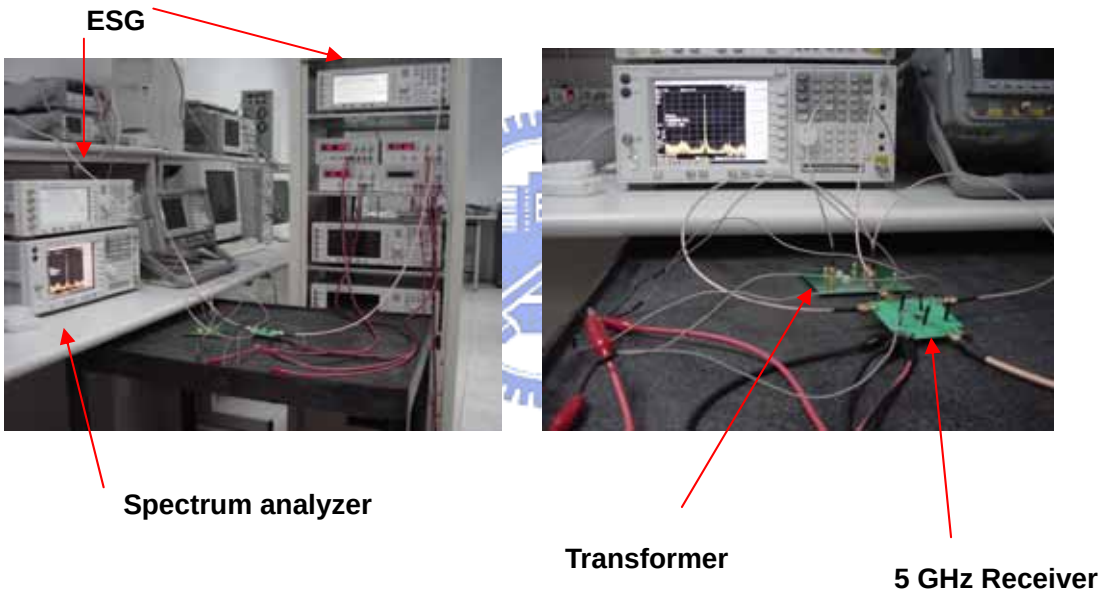


Fig. 7-1 Measurement environment

7.1 Testing Plan

The measurement setup requires three topologies to measure all performance. Matching testing setup is for impedance measurements. Power testing setup is for gain and linearity measurement. The last is noise testing setup utilized for noise figure measurement. The three kinds of setup is shown as follow:

7.1.1 Matching Measurement

For impedance matching measurement, 2-port network analyzer is connected at the RF terminal. It must be noted that LO terminals must be terminated with two 50Ω terminations to ensure the operating condition and stability. The IF terminal can be floating at this stage. The network analyzer used is Agilent 8753ES, and the operating frequency band covers 30 kHz~6GHz. The setup is shown in Fig. 7-2.

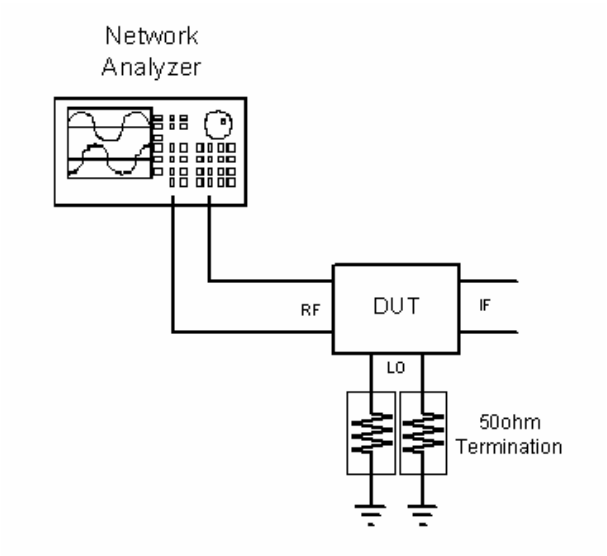


Fig. 7-2 Matching measurement setup

7.1.2 Power Measurement

Three signal generators supported up to 5GHz are required for one-tone testing and two-tone testing. A power combiner is needed for two-tone testing. The power combiner is 2way-0° (ZFSC-2-10G) combiner provided by Mini-Circuits. Low frequency transformer used for differential to single conversion is ADT4-6T (Mini-Circuits). The setup is shown in Fig. 7-3.

Because the output impedance of the mixer is comparable to 50Ω which is also the input impedance of spectrum analyzer, the voltage gain is degraded due to loading effect. The active probe which provides 1 MΩ input impedance is assumed to be available in order to measure the actual voltage gain of the mixer not affected by the loading of the following stage. But this measurement is under the condition without the active probe. The difference between the two conditions is shown in Fig. 7-4. That is, the simulation performance of voltage gain is degraded from 21dB to 17dB for packaged 5 GHz receiver frontend. The voltage gain degradation is from 27 to 21 dB for on-wafer 5 GHz receiver frontend.

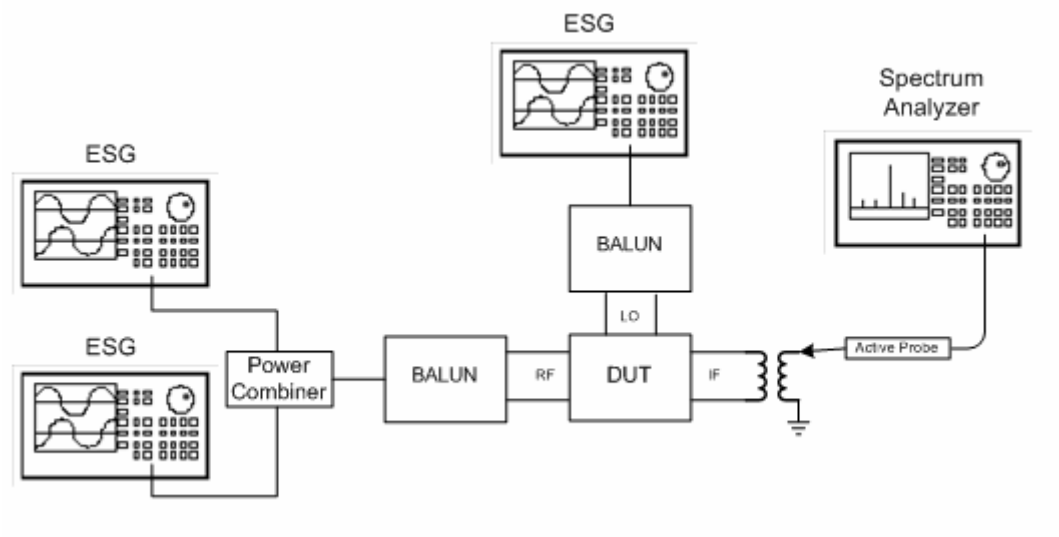


Fig. 7-3 Power measurement setup

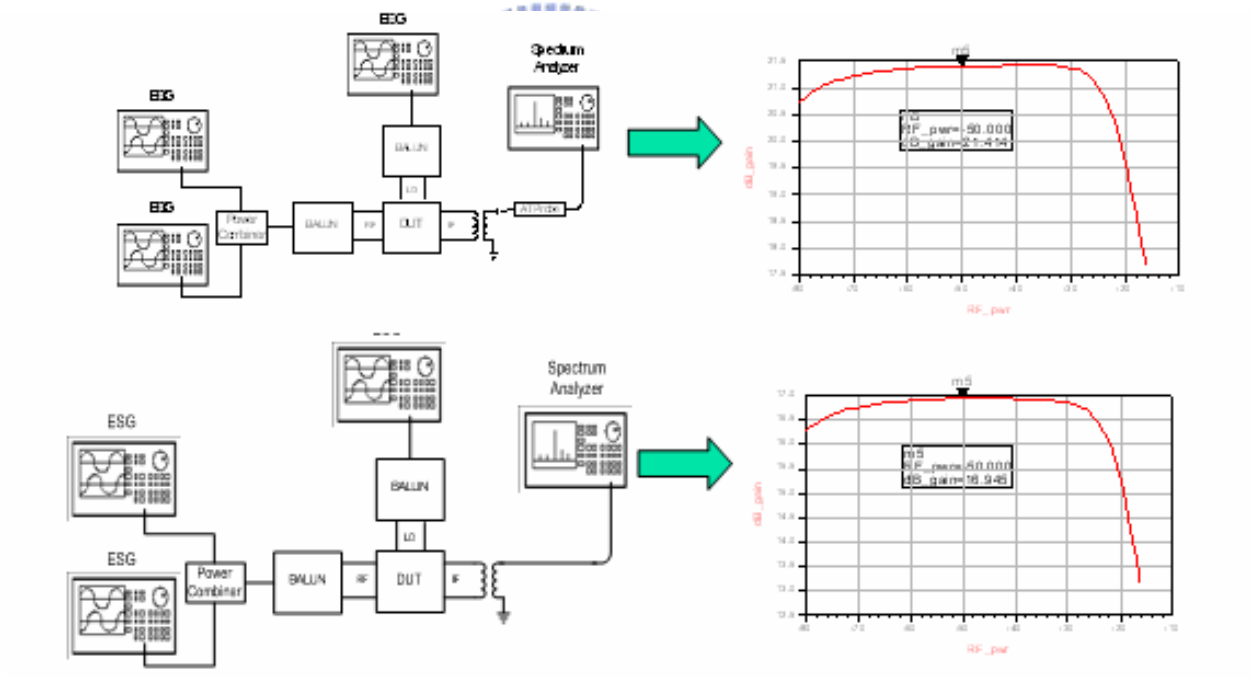


Fig. 7-4(a) The comparison between the two measurement condition for packaged 5 GHz Rx (Voltage gain: 21.4dB → 16.9dB)

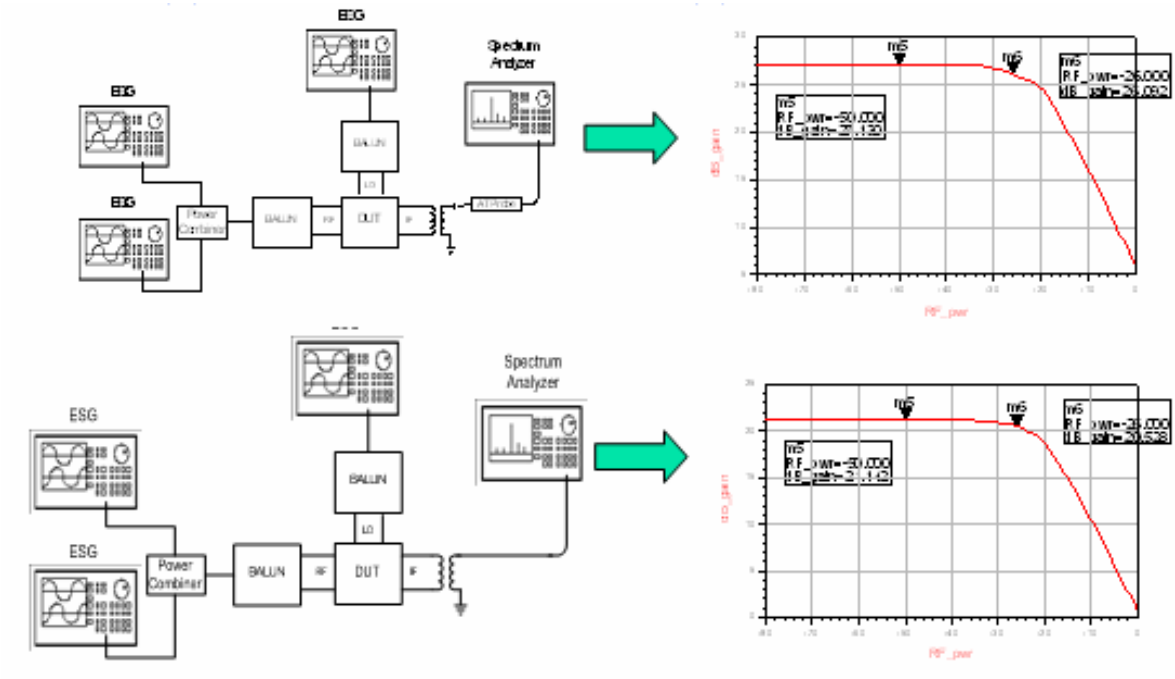


Fig. 7-4(b) The comparison between the two measurement condition for on-wafer 5 GHz Rx (Voltage gain: 27.1dB → 21.1dB)

7.1.3 Noise Measurement

The noise figure is measured by Agilent N8975A noise figure analyzer with Agilent 346A noise source, while ESG provides the LO signal to perform frequency downconversion. The balun at RF ports and transformer at IF ports can be de-embedded by the method proposed by [20]. The setup is shown in Fig. 7-5.

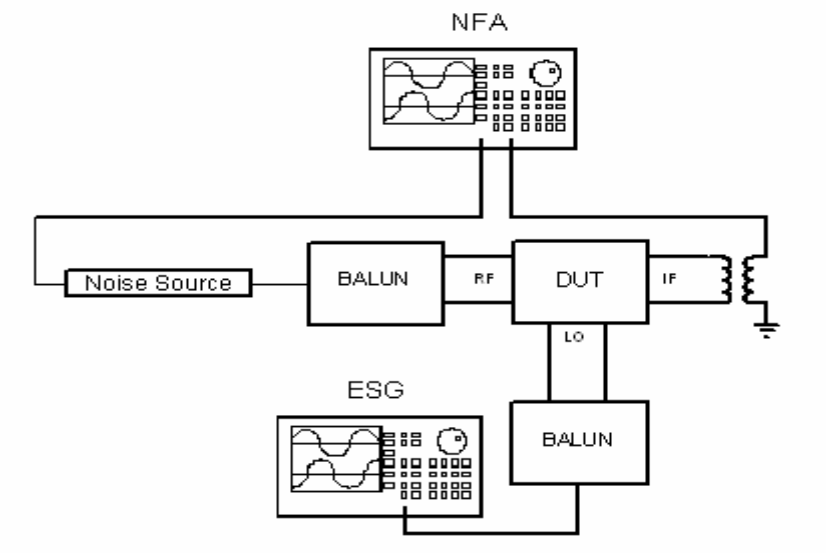
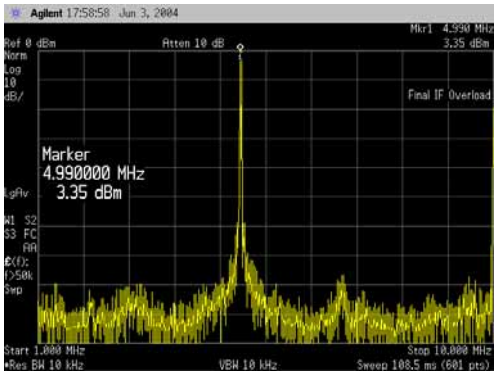


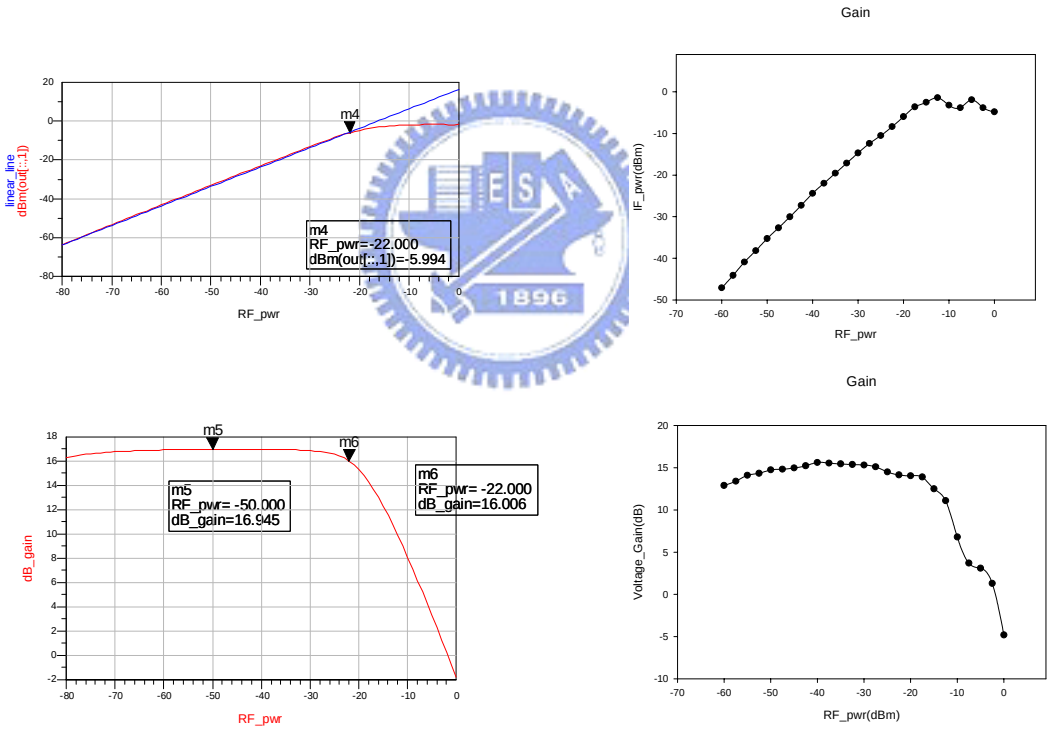
Fig. 7-5 Noise measurement setup

7.2 Experimental Results

7.2.1 Packaged 5 GHz Band Receiver

The one-tone and two-tone testing measurements of the packaged 5 GHz receiver is shown in Fig. 7-6 and Fig. 7-7. The left side in the figure shows the simulation and the right side illustrates the measurement. The NF measurement is shown in Fig.7-8.

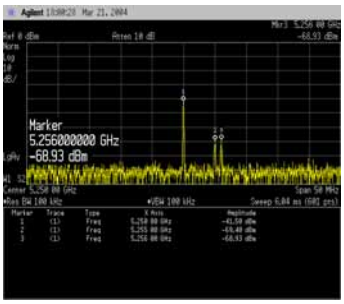




Simulation **Measurement**

One-tone testing---Gain=15 dB, P1dB=-23dBm

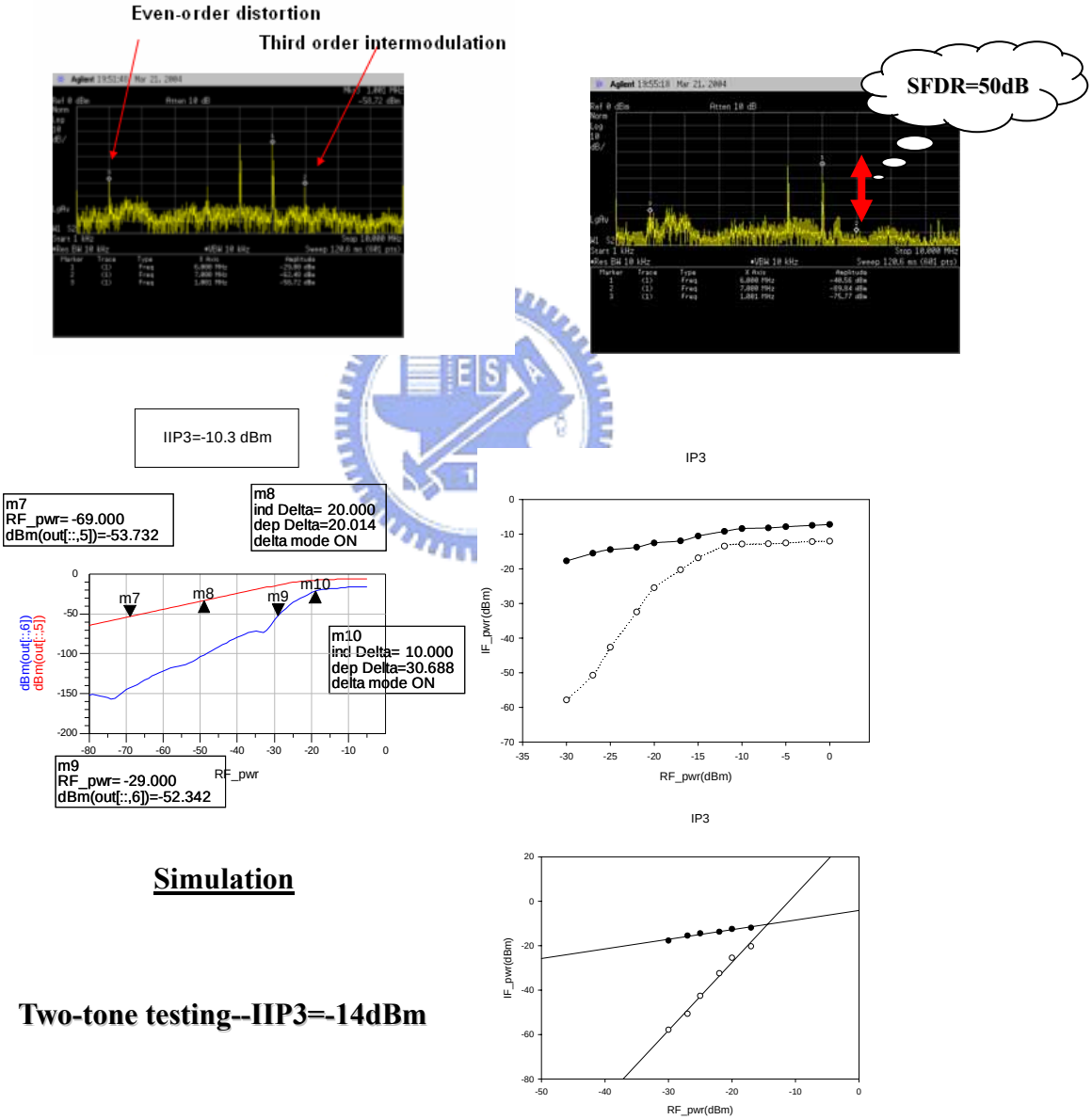
Fig. 7-6 Gain & P1dB measurement of packaged 5 GHz receiver



RF1 Frequency=5.255 GHz

RF2 Frequency=5.256 GHz

LO Frequency=5.25 GHz

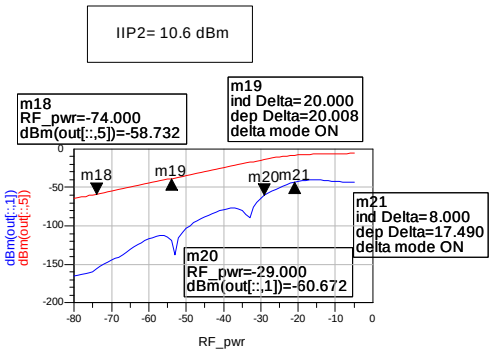


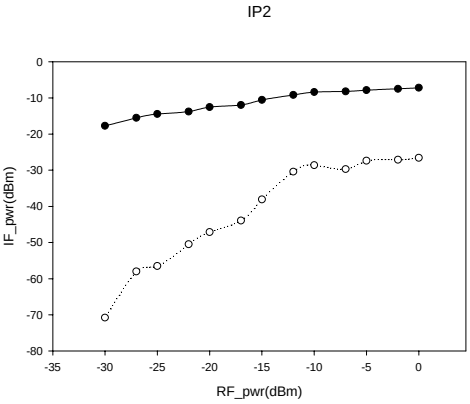
Simulation

Two-tone testing--IIP3=-14dBm

Measurement

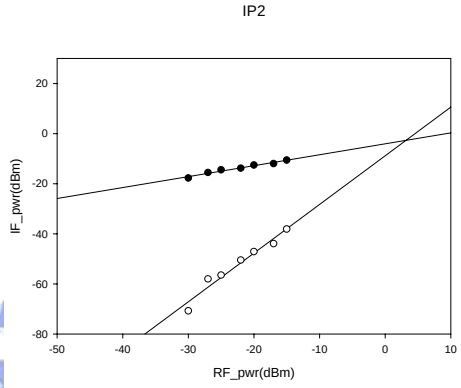
Fig. 7-7(a) IP3 measurement of packaged 5 GHz receiver





Simulation

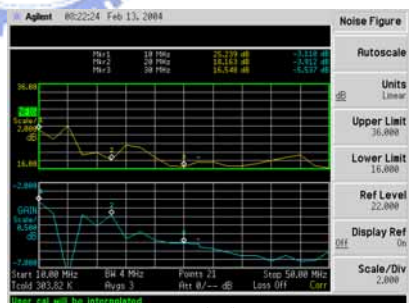
Two-tone testing---IIP2=4dBm



Measurement

Fig. 7-7(b) IP2 measurement of packaged 5 GHz receiver

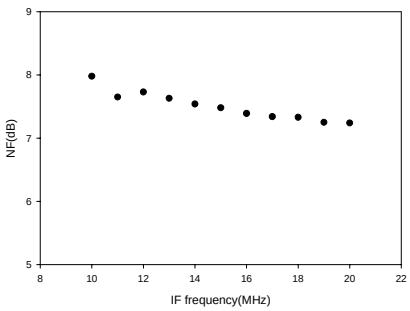
noisefreq	nf(2)	NFssb	NFdsb
RF_pwr=-52.000 10.00MHz	5.833	5.833	2.765
RF_pwr=-51.000 10.00MHz	5.833	5.833	2.765
RF_pwr=-50.000 10.00MHz	5.833	5.833	2.765
RF_pwr=-49.000 10.00MHz	5.833	5.833	2.765
RF_pwr=-48.000 10.00MHz	5.833	5.833	2.766



Noise figure

Simulation

NF =7.2 dB

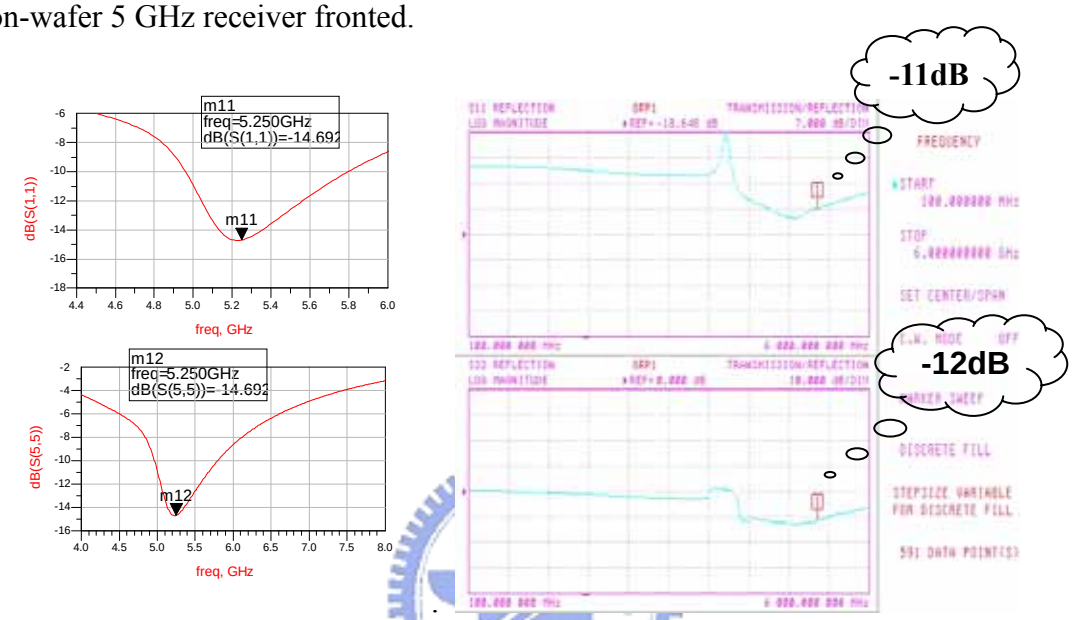


Measurement

Fig. 7-8 Noise figure measurement of packaged 5 GHz receiver

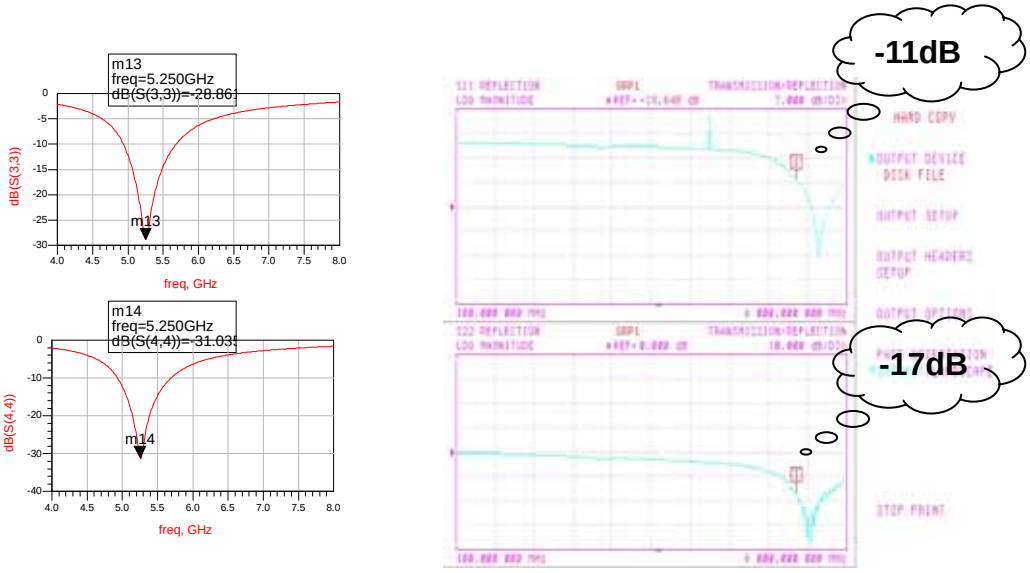
7.2.2 On-wafer 5 GHz Band Receiver

Fig. 7-9 shows matching measurements. One-tone testing is shown in Fig. 7-10 while two-tone testing is illustrated in Fig. 7-11. Fig. 7-12 shows the NF measurement. Table 7-1 lists the measurement summaries of both packaged and on-wafer 5 GHz receiver fronted.



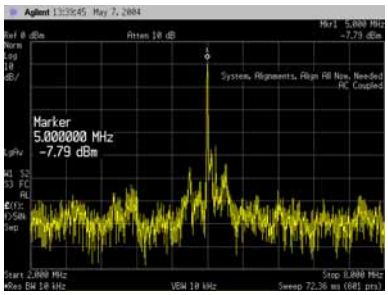
Simulation **Measurement**

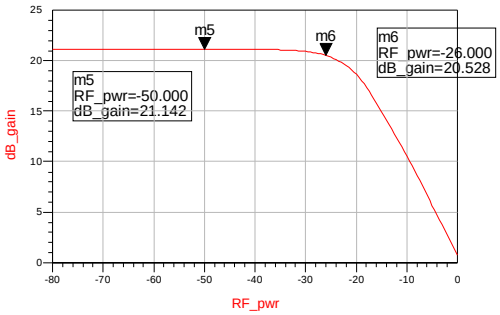
(a) RF port matching of differential 5 GHz receiver



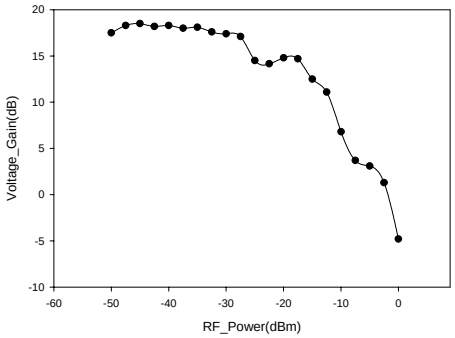
Simulation **Measurement**

Fig. 7-9 (b) LO port matching of differential 5 GHz receiver



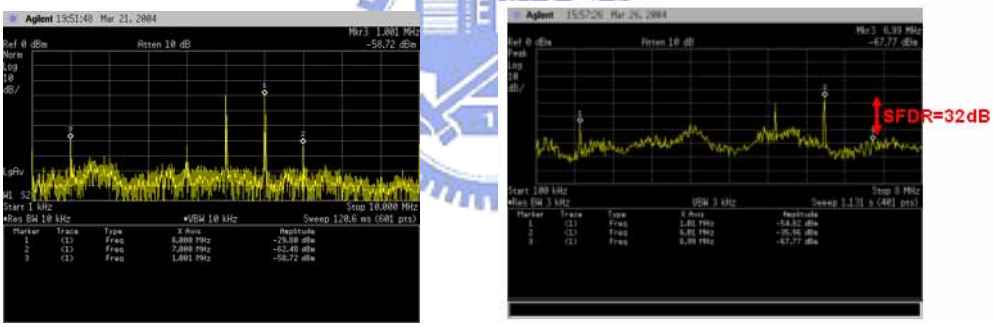


Gain

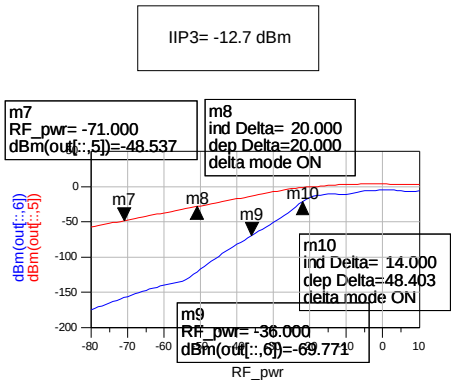


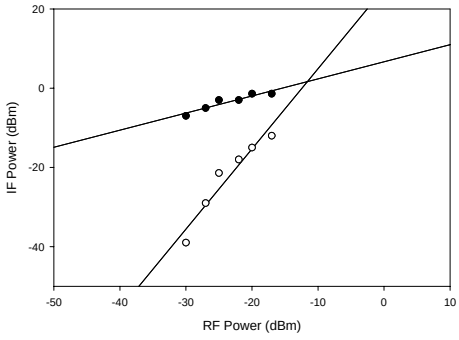
Simulation **Measurement**

Fig. 7-10 Gain & P1dB measurement of on-wafer 5 GHz receiver (Gain=18dB; P1dB=-27dBm)



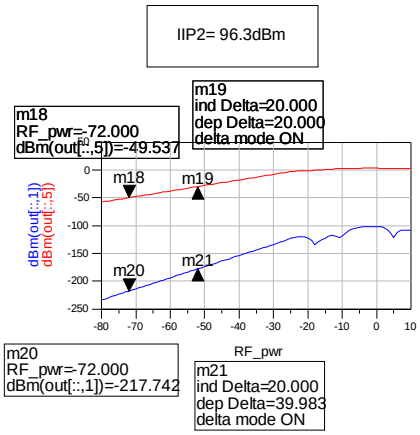
IP3

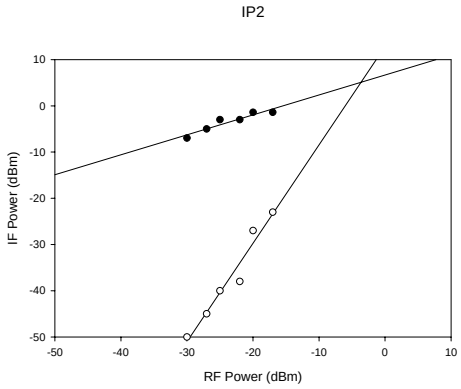




Simulation **Measurement**

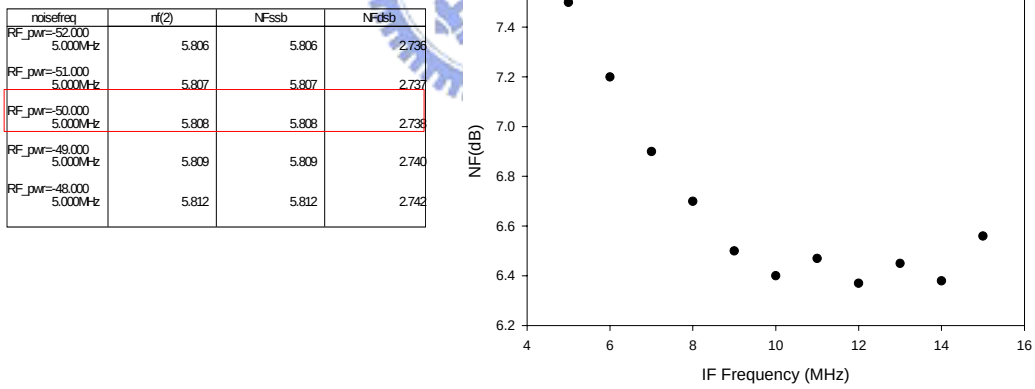
Fig. 7-11(a) IP3 measurement of on-wafer 5 GHz receiver (IIP3=-12dBm)





Simulation **Measurement**

Fig. 7-11(b) IP2 measurement of on-wafer 5 GHz receiver (IIP2=-3dBm)



noisefreq	nf(2)	NFssb	NFdsb
RF_pwr=-52.000 5.000MHz	5.806	5.806	2.736
RF_pwr=-51.000 5.000MHz	5.807	5.807	2.737
RF_pwr=-50.000 5.000MHz	5.808	5.808	2.738
RF_pwr=-49.000 5.000MHz	5.809	5.809	2.740
RF_pwr=-48.000 5.000MHz	5.812	5.812	2.742

Simulation **Measurement**

Fig. 7-12 Noise figure measurement of on-wafer 5 GHz receiver

Table 7-1 Comparisons between simulation and measurement of 5 GHz receiver frontend

	Packaged		On-wafer	
	Simulation	Measurement	Simulation	Measurement
Voltage gain(dB)	17	15	21	18
P1dB(dBm)	-22	-23	-26	-27
IIP3(dBm)	-10.3	-14	-12.7	-12
IIP2(dBm)	10.6	4	96.3	-3
NF(dB)	5.83	7.2	5.81	6.4

7.2.3 Concurrent 2.4/5 GHz Dual Band LNA

The measurement of the S-parameter and Smith Chart are shown in Fig. 7-13.

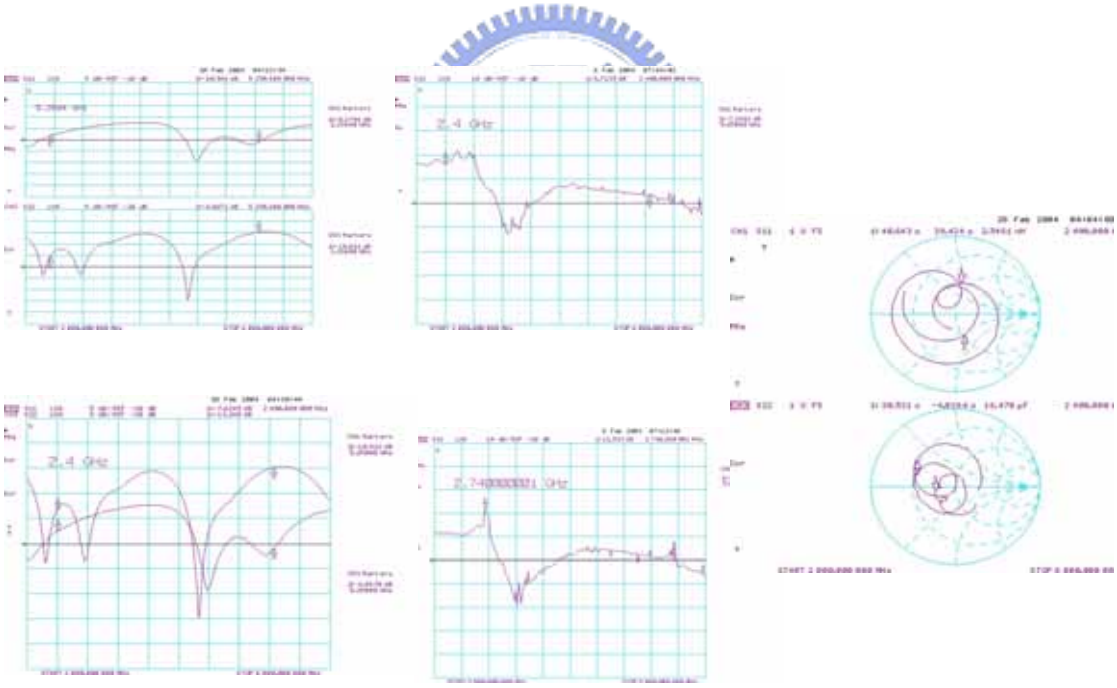


Fig. 7-13 S-parameter measurement of concurrent dual band LNA

S11=-8.3dB at 2.4 GHz; S11=-10.9dB at 5.25 GHz

S22=-15.8dB at 2.4 GHz; S22=-4.8dB at 5.25 GHz

S21=6.7dB at 2.4 GHz; S21=-7.2 dB at 5.25GHz or

S21=11.9dB at *2.74 GHz*; S21=-5.1 dB at 5.25GHz

7.3 Discussion

From the aforementioned measurements, the causes of a little mismatch between simulations and measurements is due to source inductors of LNAs. The two circuits (5 GHz receiver and dual-band LNA) utilize bond wire inductors in package model as source inductors, as shown in Fig. 7-14. Although the simulation shows this kind of configuration can work pretty well, the actual bonding angle or length will affect the inductance value. Furthermore, the mutual inductance between adjacent pins is complex (Fig.7-15), so it is not easy to control the required source inductance accurately. As for the on-wafer 5 GHz receiver, it is just a layout issue, since the IF output pins adjoin with DC pins, as shown in Fig. 7-16. This would cause measurement errors.

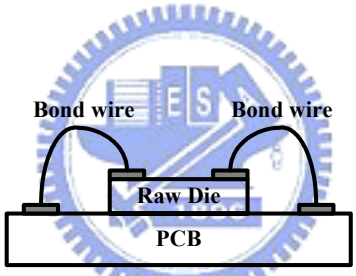


Fig. 7-14 Bond wire used as source inductor of LNA

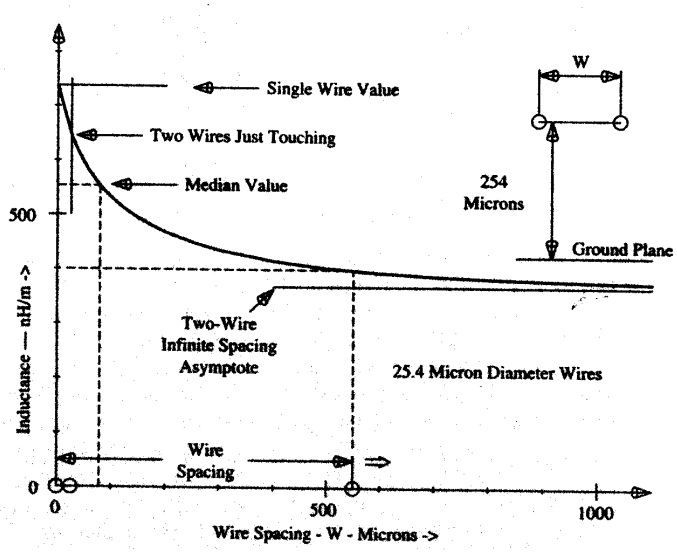


Fig. 7-15 Inductance of two wires as a function of spacing [30]

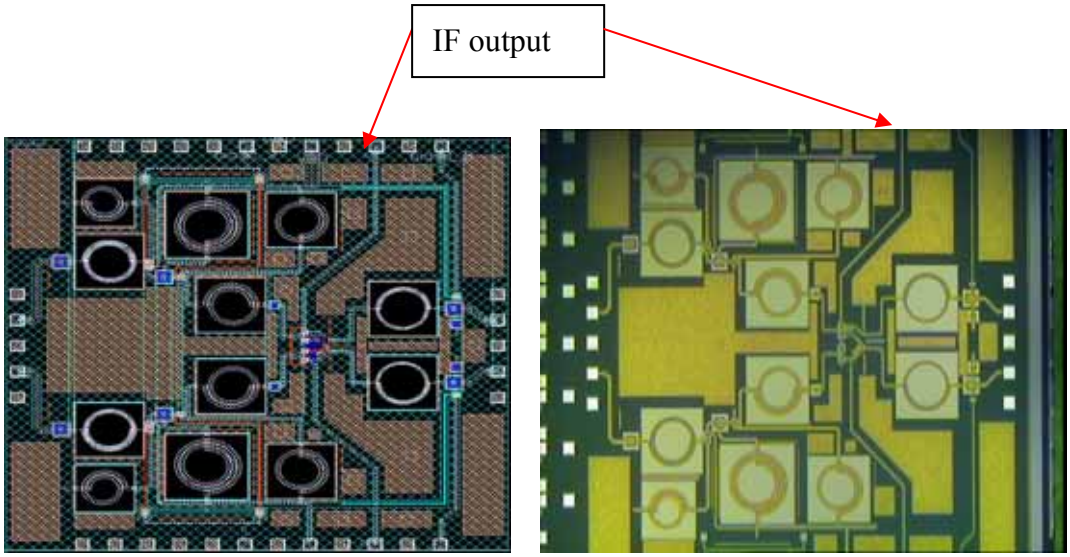
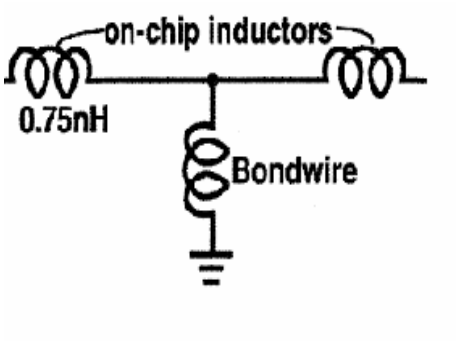


Fig. 7-16 Layout issues of on-wafer 5 GHz receiver

How to resolve the problems encountered in this thesis? There are two methods proposed. Using a 3-port inductor (Fig. 7-17(a)) to replace the source inductors of the differential LNA. In the deep submicrometer process and several GHz RF application, the source inductor often needs less than 1nH to obtain a narrow-band input matching of 50Ω. This is less than the inductance of a bondwire and a package lead. It may be difficult to realize this small inductor even with multiple bondwires and pins in parallel. Since the circuit is differential, the source degeneration inductors are integrated as small on-chip spirals and then center tapped to ground through the bondwire and package lead. As only the common-mode dc and even harmonics flow to ground, the bondwire and lead inductance do not affect the differential input impedance of the LNA.

Unfortunately, the 3-port inductor is not provided by UMC CMOS process. Therefore, we need to design a testkey for ourselves, following the modeling flow depicted in Fig. 7-18. Except for the inductor, the monolithic transformer employed in wideband LNA (Fig. 7-17(b)) also needs a testkey design and RF modeling to implement the circuit.



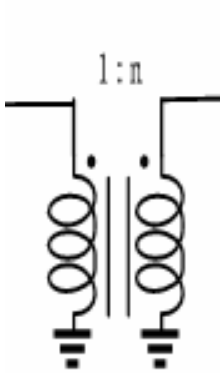


Fig. 7-17(a) 3-port inductor **(b) Monolithic transformer**

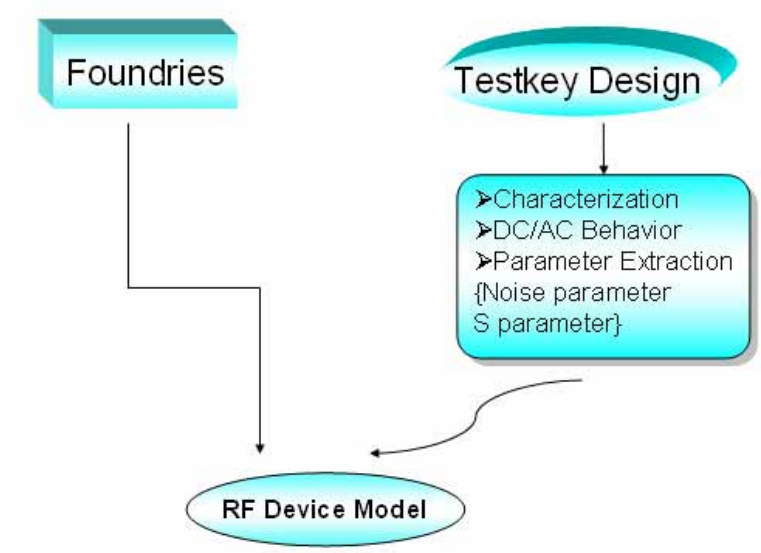


Fig. 7-18 Device modeling flow

Chapter 8
Conclusions

8.1 Conclusions

This thesis is divided into two major parts. In the first part, the commonly used dual band RF receiver architectures are analyzed and discussed. Both the switched and concurrent dual band architectures suited for this design are proposed. The second part deals with the circuit designs of switched and concurrent dual band receiver frontend operating in 2.4 GHz and 5 GHz bands based on direct conversion architectures. There are three chips fabricated in this design, including packaged and on-wafer 5 GHz receiver frontend as well as a concurrent dual band LNA. Besides, 2.4 GHz receiver is simulated to work with 5 GHz receiver in order to achieve the switched dual band function. The concurrent dual band LNA is combined with the passive mixer to realize the concurrent dual band receiver. In the end, a novel impedance matching technique is utilized to fulfill the wideband LNA, the performance of which is comparable to the recently published literature.

According to the experimental results, some mismatch between simulation and measurement exits. The cause is due to the implementation of bondwire used as source inductor for packaged chip including 5 GHz band receiver and dual band LNA.

Although the ADS simulation shows pretty good results, the actual inductance value is hard to be predicted. Therefore, the 5 GHz band receiver needs a 3-port inductor to realize the source inductor accurately and minimize the device or circuit mismatch due to process variation at the same time because it adopts the differential topologies. On the other hand, the dual band LNA should be transformed into on-wafer version to eliminate the bond wire effect. Since the inductance value of the source inductor is required to be less than 0.6nH, however, the bond wire inductance is about 1nH. Furthermore, the package QFN20D(Appendix-A) is modeled for 5 GHz band application, and it is not very suited for the dual band LNA even though the chip works at 2.4 GHz band, but fails at 5 GHz band.

8.2 Future Work

RF-SOC

The term system-on-chip (SOC) can be defined as a chip that has embedded multifunctional circuits, such as memory, analog circuits, and logic components. It can also mean a chip that integrates intellectual property (IP) cores. Thereby, IP reuse is an important factor for SoC because it shortens development turnaround time (TAT) and reduces cost.

"RF-SoC" means adding RF circuits to the "traditional" SoC. That is, RF/analog/digital circuits are all integrated with memory blocks and

microprocessors/DSP as a complex single-chip digital communication system. In the recent years, the integration level of RF ICs has exhibited dramatic progress during the last decade. It is not impossible to achieve this goal-“RF-SoC”. Nevertheless, it must face many trade-off between cost, size, performance (crosstalk), radio architecture, device technology, and time-to-market.

Design Methodology

What if IP cores provided by IP vendors cannot completely fit buyers’ requirements? Is it totally useless? Different from the IP-reuse methodology, a IP-revise design methology is proposed in this thesis. Fig. 8-1 demonstrates the design flow. This is based on two prerequisite, i.e., the characteristic of strong dependence on matching network in designing RF circuits, and the frequently-used inductively degeneration LNA in today’s RF circuits. Even though lots of innovative techniques are invented to improve the LNA performances, such as feedback, dual gain, linearity boosting, current-reuse, and so on, their impedance matching still relies on the source inductor. Hence, IP-revise methodology can reduce the design cycle in some special circuits.

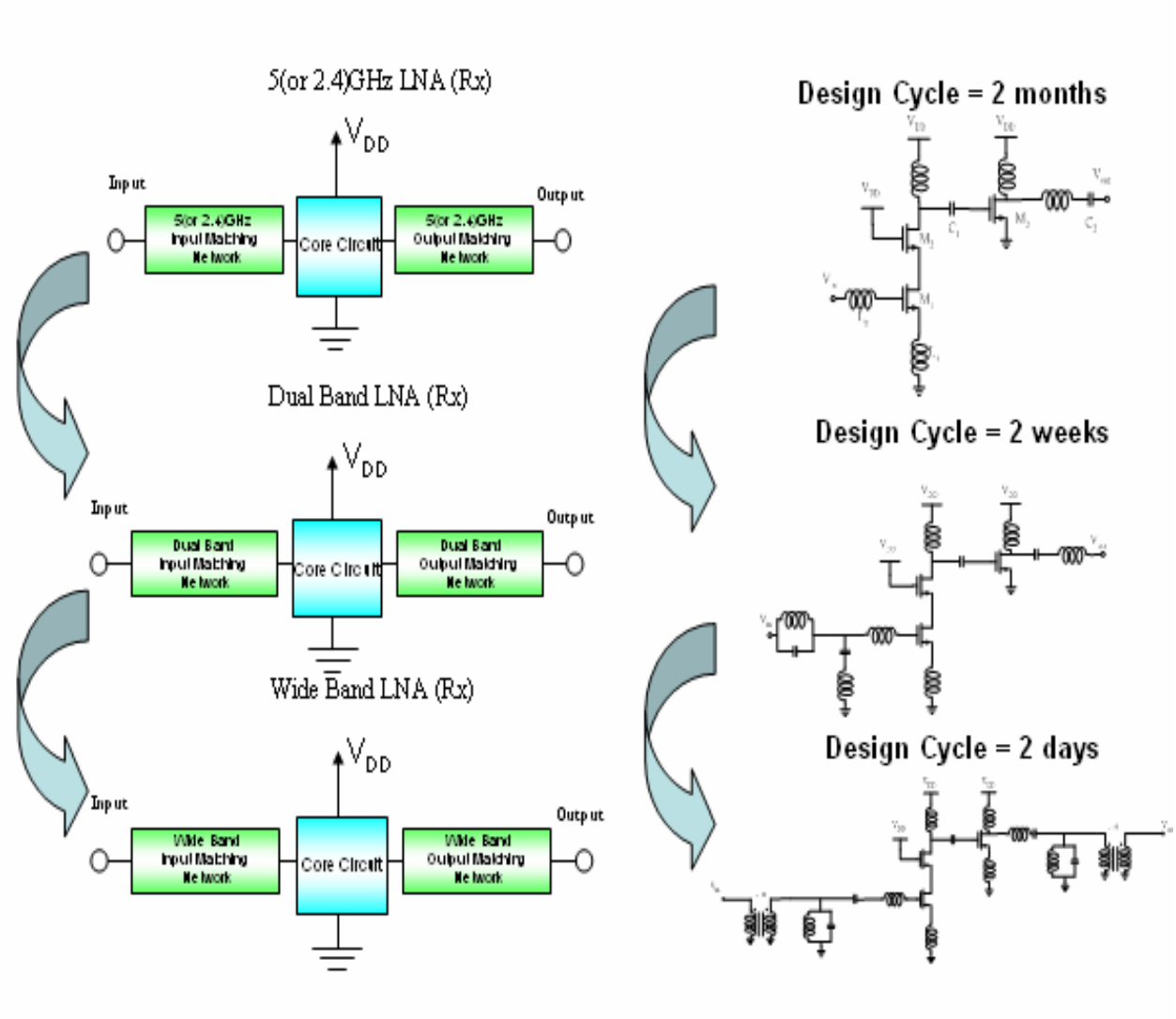


Fig. 8-1 IP-revise design mythology proposed in this thesis

Fig. 8-2 shows the interconnection between 5 GHz receiver and 5 GHz synthesizer designed by another group member. Fig. 8-3 is the measurement result showing the correct frequency downconversion function just like using ESG as LO input of the receiver. This reveals the feasibility of IP integration for RF circuits. In the future design, the VCO can be embedded into the receiver frontend to be fabricated (Fig. 8-4), and gradually integrate more and more circuit blocks into a transceiver in order to achieve the ultimate goal—"RF-SOC".

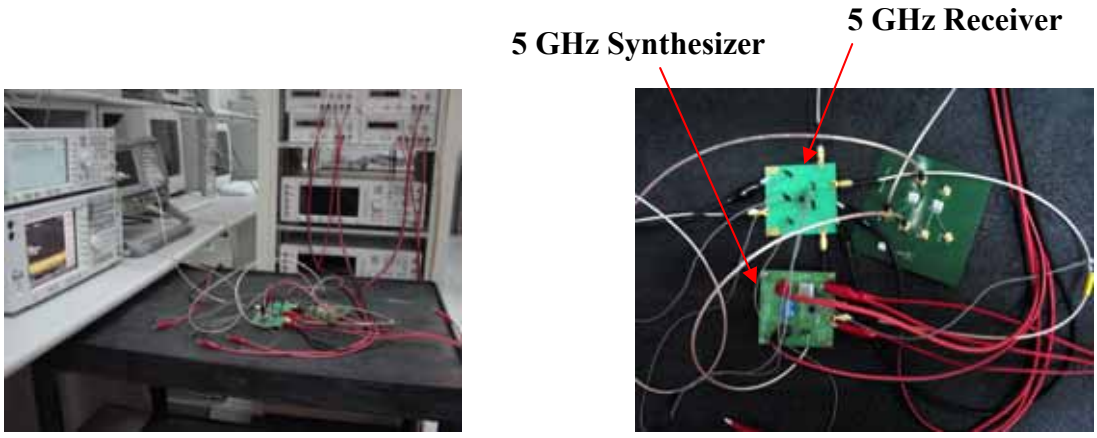


Fig. 8-2 The interconnection between 5 GHz receiver and 5 GHz synthesizer

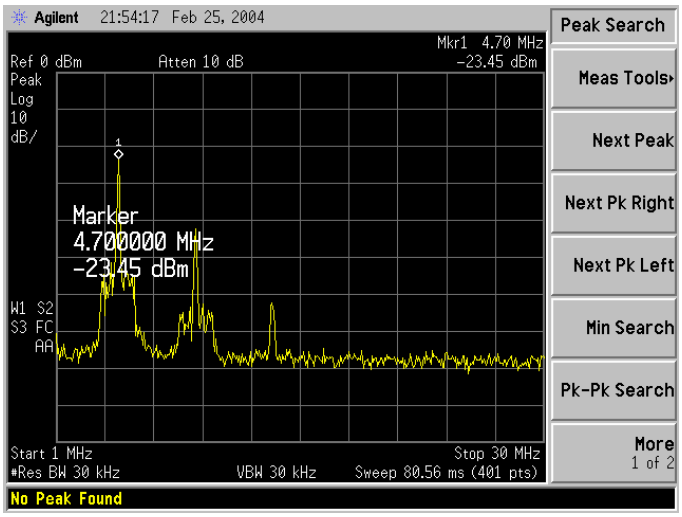


Fig. 8-3 The measurement of connecting 5 GHz receiver and 5 GHz synthesizer design

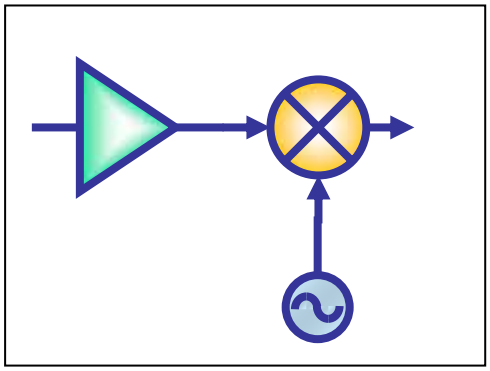


Fig. 8-4 Embed VCO into receiver frontend

Appendix-A
Package Data Sheet

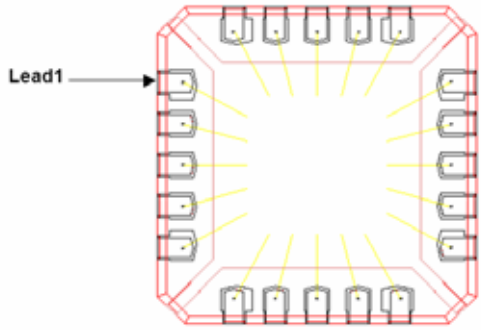


Figure 1: 2D Model for QFN20 Lead Frame Drawing.

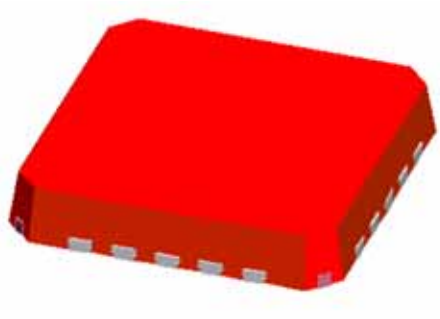
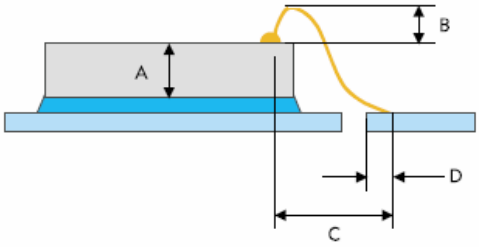


Figure 2: 3D Model for QFN20 Package.

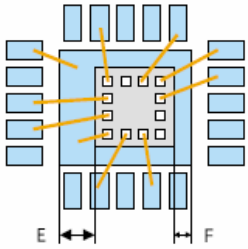
The following table showed the RLC parameter of all leads with bond wires.

Lead (i)	Label	Wire length (mm)	Wire			Lead				
			$Ls_{(i,i)}$ (nH)	$Lm_{(i,i+1)}$ (nH)	$R_{(i,i)}$ (mΩ)	$Ls_{(i,i)}$ (nH)	$Lm_{(i,i+1)}$ (nH)	$Cs_{(i,i)}$ (pF)	$Cm_{(i,i+1)}$ (pF)	$R_{(i,i)}$ (mΩ)
1	GND	1.150	1.058	0.188	53.08	0.013	0.002	0.114	0.031	1.06
2	5GHz	1.041	0.960	0.163	351.64	0.013	0.002	0.112	0.023	7.46
3	VDD	1.006	0.920	0.163	48.30	0.013	0.002	0.108	0.023	1.06
4	5GHz	1.043	0.962	0.191	352.18	0.013	0.002	0.113	0.031	7.52
5	GND	1.144	1.053	0.126	52.91	0.013	0.001	0.114	0.004	1.05
6	---	1.144	1.056	0.188	53.02	0.013	0.002	0.114	0.031	1.06
7	---	1.043	0.960	0.163	49.77	0.013	0.002	0.113	0.023	1.06
8	---	1.006	0.920	0.163	48.29	0.013	0.002	0.108	0.023	1.06
9	---	1.041	0.962	0.191	49.81	0.013	0.002	0.113	0.031	1.06
10	---	1.150	1.052	0.126	52.89	0.013	0.001	0.114	0.004	1.06
11	GND	1.144	1.057	0.188	53.06	0.013	0.002	0.115	0.031	1.06
12	5GHz	1.043	0.960	0.163	351.75	0.013	0.002	0.112	0.023	7.51
13	VDD	1.006	0.920	0.163	48.27	0.013	0.002	0.108	0.023	1.06
14	5GHz	1.041	0.962	0.191	352.14	0.013	0.002	0.113	0.031	7.52
15	GND	1.150	1.052	0.126	52.90	0.013	0.001	0.114	0.004	1.05
16	GND	1.150	1.058	0.188	53.11	0.013	0.002	0.115	0.031	1.05
17	5GHz	1.041	0.960	0.163	351.85	0.013	0.002	0.113	0.023	7.52
18	VDD	1.006	0.920	0.163	48.30	0.013	0.002	0.108	0.023	1.06
19	5GHz	1.043	0.961	0.191	351.87	0.013	0.002	0.112	0.031	7.52
20	GND	1.144	1.052	---	52.90	0.013	---	0.114	---	1.05

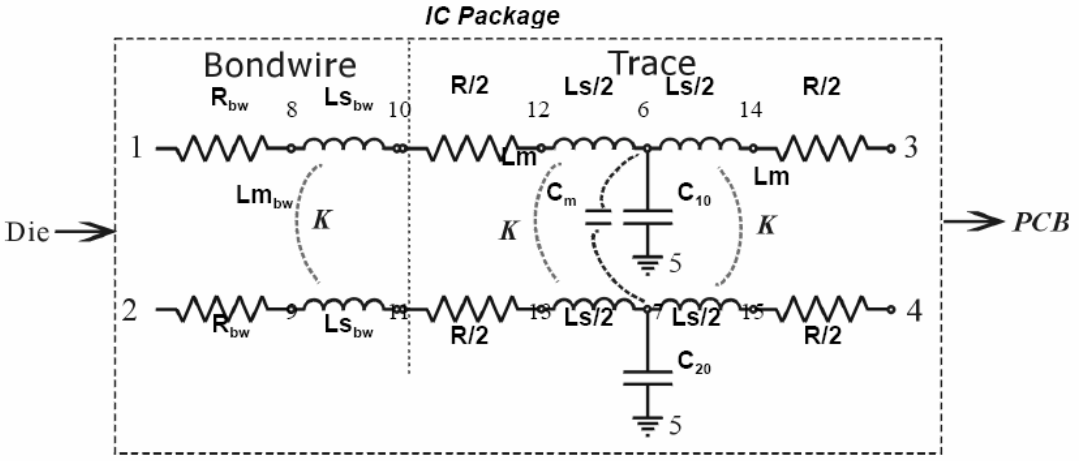
1. Die thickness after lapping: 12±0.5mil (A)
2. Wire loop height: 7.1±0.9mil (180±20μm) (B)
3. Min length: 30mil (C)
   Max length: 170mil (C)
4. 2nd bond to finger tip: 10mil (D)



5. Minimum distance between chip and L/F pad
   With ground bond: min. 30mil (E)
   Without ground bond: min. 10mil (F)
6. Minimum distance from die edge to bonding pad edge: 1.18mil (30μm) (G)
7. Minimum bond pad pitch: 2.76mil (70μm) (H)



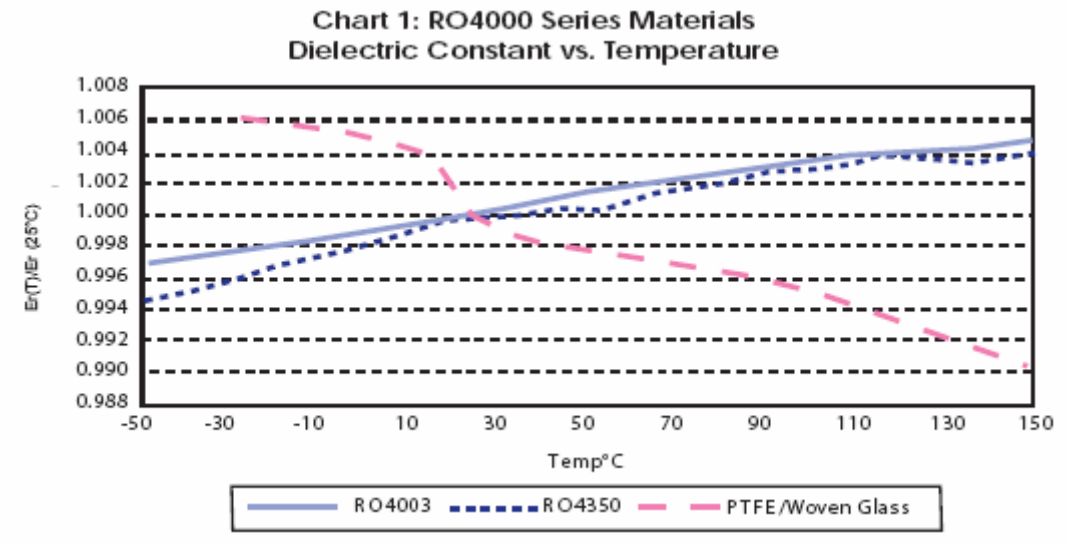
➢ Attachment 1: IC Package equivalent circuit graph

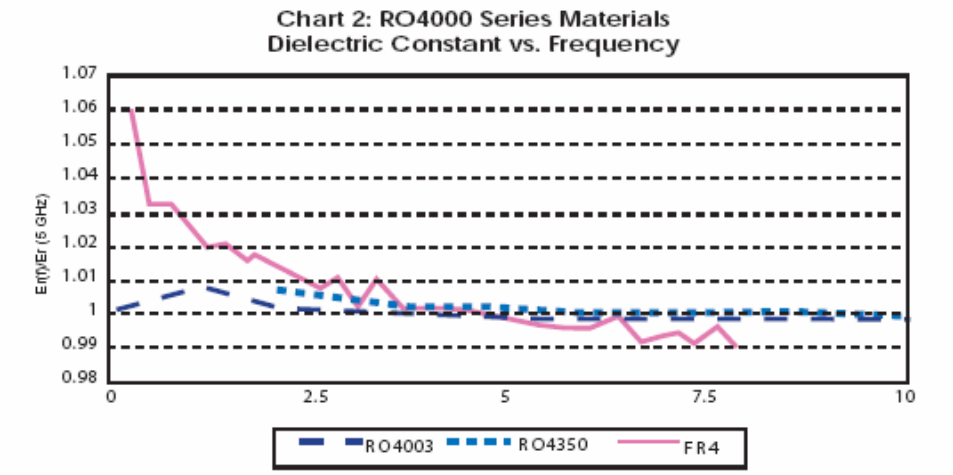


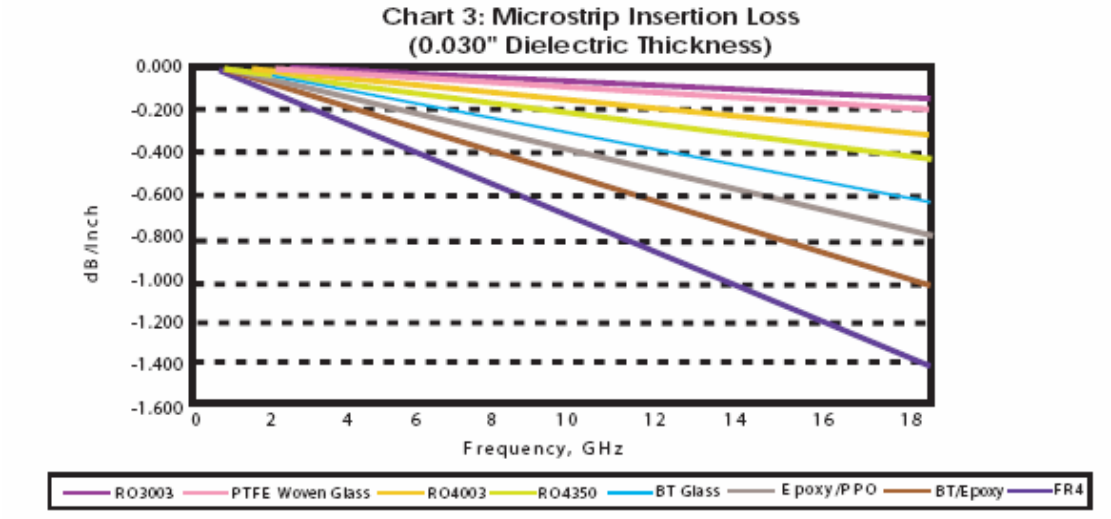
- R or R_{bw} : Self resistance of the lead or bondwire.
- Lm or Lm_{bw} : Mutual inductance between the lead (or bondwire) and its nearby lead (or bondwire).
  e.g.: L_{12}, L_{23}, ...
- Ls or L_{bw} : Self inductance of a lead (or bondwire) reduced by mutual inductance coupling with package and PCB ground planes.
  e.g. L_1, L_2, L_3, ...
- C_{i0} : Self capacitance between the lead to ground plane. i = 1, 2, 3, …
- Cm : Mutual capacitance between the lead and its nearby lead.
  e.g. C_{12}, C_{23}, ...
- Cs : Bulk capacitance (e.g. C_{11}, C_{22}, C_{33}, ...) from the lead under question to all other leads. All other leads and metal are ground potential.
  e.g. $C_{11} = C_{10} + C_{12} + C_{13} + \ldots$, $C_{10} =$ Cs − Cm

K : Inductive coupling coefficient. e.g. $K_1 = \frac{L_{12}}{\sqrt{L_1 \times L_2}}$

Appendix-B
PCB Data Sheet







PROPERTY	TYPICAL VALUE		DIRECTION	UNITS	CONDITION	TEST METHOD
	RO4003C™	RO4350B™[1]				
Dielectric Constant, ϵ_r	3.38±0.05	3.48±0.05[2]	Z	--	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Dissipation Factor tan, δ	0.0027 0.0021	0.0037 0.0031	Z	--	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ϵ_r	+40	+50	Z	ppm/ °C	-100°C to 250°C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7 X 10^{10}	1.2 X 10^{10}		MΩ•cm	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2 X 10^{9}	5.7 X 10^{9}		MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	31.2 (780)	31.2 (780)	Z	KV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	26,889 (3900)	11,473 (1664)	Y	MPa (kpsi)	RT	ASTM D638
Tensile Strength	141 (20.4)	175 (25.4)	Y	MPa (kpsi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)	-	MPa (kpsi)		IPC-TM-650 2.4.4
Dimensional Stability	<0.3	<0.5	X,Y	mm/m (mils/inch)	after etch +E2/150°	IPC-TM-650 2.4.39A
Coefficient of Thermal Expansion	11 14 46	14 16 50	X Y Z	ppm/°C	-55 to 288°C	IPC-TM-650 2.1.41
Tg	>280	>280	-	°C	A	IPC-TM-650 2.4.24
Thermal Conductivity	0.64	0.62	-	W/m/°K	100°C	ASTM F433
Moisture Absorption	0.04 •	0.04	-	%	48 hrs immersion 0.060" sample Temperature 50°C	ASTM D570
Density	1.79	1.86	-	gm/cm^3	23°C	ASTM D792
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)		N/mm (pli)	after solder float 1 oz. EDC Foil	IPC-TM-650 2.4.8
Flammability	N/A	94V-0				UL

Bibliography

[1] Ren-Chieh Liu; Chung-Rung Lee; Huei Wang; Chorng-Kuang Wang," *A 5.8-GHz two-stage high-linearity low-voltage low noise amplifier in a 0.35-μm CMOS technology [WLANs]",* Radio Frequency Integrated Circuits (RFIC) Symposium, 2002 IEEE , 2-4 June 2002 Pages:221 - 224

[2] Ting-Ping Liu; Westerwick, E.," *5-GHz CMOS radio transceiver front-end chipset*", Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 12 , Dec. 2000 Pages:1927 - 1933

[3] Madihian, M.; Fujii, H.; Yoshida, H.; Suzuki, H.; Tamazaki, T.," *A 1-10 GHz 0.18£gm-CMOS chipset for multi-mode wireless applications*", Microwave Symposium Digest, 2001 IEEE MTT-S International , Volume: 3 , 20-25 May 2001 Pages:1865 - 1868 vol.3

[4] Hong-Wei Chiu; Shey-Shi Lu," *A 2.17 dB NF, 5 GHz band monolithic CMOS LNA with 10 mW DC power consumption*", VLSI Circuits Digest of Technical Papers, 2002. Symposium on , 13-15 June 2002 Pages:226 - 229

[5] Mukherjee, D.; Bhattacharjee, J.; Chakraborty, S.; Laskar, J.," *A 5-6 GHz fully-integrated CMOS LNA for a dual-band WLAN receiver*", Radio and Wireless Conference, 2002. RAWCON 2002. IEEE , 11-14 Aug. 2002 Pages:213 - 215

[6] Westerwick, E.H.,” *A 5 GHz band CMOS low noise amplifier with a 2.5 dB noise figure*”, VLSI Technology, Systems, and Applications, 2001. Proceedings of Technical Papers. 2001 International Symposium on , 18-20 April 2001 Pages:224 - 227

[7] Tsang, T.K.K.; El-Gamal, M.N.,” *Gain and frequency controllable sub-1 V 5.8 GHz CMOS LNA*”, Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 4 , 26-29 May 2002 Pages:IV-795 - IV-798 vol.4

[8] Samavati, H.; Rategh, H.R.; Lee, T.H.,” *A 5-GHz CMOS wireless LAN receiver front end*”, Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 5 , May 2000 Pages:765 - 772

[9] Wei Meng Lim; Manh Anh Do; Jian Guo Ma; Kiat Seng Yeo,” *A broadband CMOS LNA for WLAN applications*”, Ultra Wideband Systems and Technologies, 2003 IEEE Conference on , Nov. 16-19, 2003 Pages:42 – 46

[10] Tsang, T.K.K.; El-Gamal, M.N.,” *Dual-band sub-1 V CMOS LNA for 802.11a/b WLAN applications*”, Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on , Volume: 1 , 25-28 May 2003 Pages:I-217 - I-220 vol.1

[11] Hashemi, H.; Hajimiri, A.,” *Concurrent multiband low-noise amplifiers-theory, design, and applications*”, Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue: 1 , Jan. 2002 Pages:288 - 301

[12] Masoud Zargari, Steve Jen, Brian Kaczynski, Meelan Lee, Michael Mack, Srenik Mehta, Sunetra Mendis, Keith Onodera, Hirad Samavati, Weimin Si, Kalwant Singh, Ali Tabatabaei, Manolis Terrovitis, David Weber, David Su, Bruce Wooley, ”*A single-chip dual band tri-mode CMOS transceiver for IEEE 802.11a/b/g WLAN*”, Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International , Feb. 2004 Pages:96 - 97

[13] L. Perraud, C. Pinatel, M. Recouly, J-L. Bonnot, N. Sornin, F. Benoist, M. Massei, O. Gibrat, ”*A dual band 802.11a/b/g Radio in 0.18µm CMOS*”, Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International , Feb. 2004 Pages:94 – 95

[14] Rami Ahola, Adem Aktas, James Wilson, Kishore Rama Rao, Fredrik Honsson, Isto Hyyrylainen, Anders Brolin, Timo Hakala, Aki Friman, Tuula Makiniemi, Jenny Hanza, Martin Sanden, Daniel Wallner, Yuxin Guo, Timo Lagerstam, Laurent Noguer, Timo KKnuuttila, Peter Olofsson, Mohammed Ismail, “ *A single Chip CMOS Transceiver for 802.11 a/b/g WLANs*”**,** Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International , Feb. 2004 Pages:92 – 93

[15] June-Ming Hsu; Yung-Hui Chen; Shin-Fu Chen; Ming-Ching Kuo; Peng-Un Su, “*A SiGe WCDMA/DCS dual-band RF front-end receiver*”, Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE , 8-10 June 2003 Pages:27 – 30

[16] Wu, S.; Razavi, B., "*A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications*", Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 12 , Dec. 1998 Pages:2178 - 2185

[17] Zolfaghari, A.; Chan, A.; Razavi, B.," *Stacked inductors and transformers in CMOS technology*", Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 4 , April 2001 Pages:620 - 628

[18] Andrea Bevilacqua, Ali M Niknejad, "*An Ultra-Wideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receivers*", Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International , Feb. 2004 Pages:382 – 383

[19] Andersson, S.; Svensson, C.; Drugge, O.; "*Wideband lna for a multistandard wireless receiver in 0.18 /spl mu/m cmos*", European Solid-State Circuits, 2003. ESSCIRC '03. Conference on , 16-18 Sept. 2003 Pages:655 - 658

[20] A. A. Abidi, J. C. Leete, "*De-embedding the noise figure of differential amplifiers*," *IEEE J. Solid-State Circuits*, vol. 34, pp. 882-885, June 1999.

[21] Sjoland, H.; Karimi-Sanjaani, A.; Abidi, A.A.," *A merged CMOS LNA and mixer for a WCDMA receiver*", Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 6 , June 2003 Pages:1045 – 1050

[22] A. R. Shahani, D. K. Shaeffer, and T.H. Lee, "*A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver*" *IEEE J. Solid-State Circuits*, vol. 32,

pp. 2061-2070, Dec. 1997.

[23] B. Razavi, "*Design considerations for direct-conversion receivers*", *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 428-435, June 1997.

[24] D. K. Shaeffer, T. H. Lee "*A 1.5-V, 1.5-GHz CMOS low noise amplifier*", *IEEE J. Solid-State Circuits*, vol. 32, pp. 745-759, May 1997.

[25] B. Leung, *VLSI for Wireless Communication*, Upper Saddle River, NJ: Prentice-Hall, 2002.

[26] Trond Ytterdal, Yuhua Cheng, Tor A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*, Chichester :John Wiley Sons Ltd,2003.

[27] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, New York: Cambridge University Press, 1998.

[28] Chiennan Kuo, "*RF-IC Design"* class note, Department of Electronics Engineering, National Chiao Tung University, fall 2003

[29] Huang, Q.; Piazza, F.; Orsatti, P.; Ohguro, T.," The impact of scaling down to deep submicron on CMOS RF circuits", Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 7 , July 1998 Pages:1023 – 1036

[30] R. J. Weber, *Introduction to microwave circuits*, New York: IEEE Press, 2001