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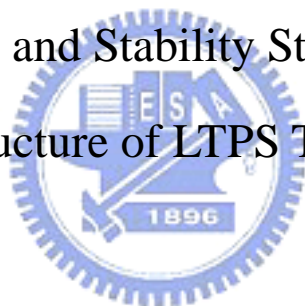
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碩 士 論 文

新穎低溫多晶矽薄膜電晶體之製程與穩定度分析

The Fabrication and Stability Study of the Novel
Structure of LTPS TFTs



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在本篇論文,一個含有較厚的源/汲極區和較薄的通道的新穎複晶矽薄膜電晶體被提出而加以研究。在提出的結構中,和傳統的堆疊式薄膜電晶體比較下,我們只需較少的4道光罩製程。提出的結構中,它有不錯的開/關電流比仍維持在良好的擺幅(約 1.51)。在開/關電流比上,在閘極電壓為 5V 下,仍維持在 1.85×10^7 左右。而更進一步地看,在閘極電壓加至 30V 時,提出的薄膜電晶體仍展現了一個較佳的飽和電流特性。同時在漏電流方面,也比傳統的降低了 2.96 倍。

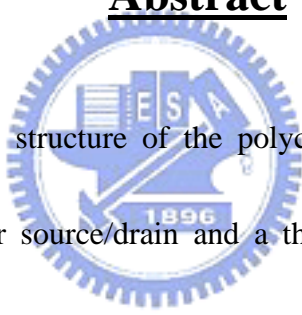
The Fabrication and Stability Study of the Novel Structure of LTPS TFTs

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Abstract



In this paper, a novel structure of the polycrystalline silicon thin-film transistors (Poly-Si TFT's) with a thicker source/drain and a thin channel have been developed and investigated. In the proposed structure, the thick source/drain and a thin active region could be achieved with only four mask steps, which are less than conventional stagger TFT. The proposed TFT has and higher Swing (~ 1.51). The on/off ratio is 1.85×10^7 for $V_{gs} = 5$ V. Moreover, the proposed TFT exhibits excellent current saturation characteristics at high bias ($V_{gs} = 30$ V) and has more than 2.96 times reduction in minimum off-state current compared to conventional TFT's.

Index Terms—stagger source/drain, On/Off current ratio, poly-Si TFT.

誌謝

~有人靠車，有人靠馬，但我們要提到耶和華我們神的名。
~

Psalms:20:7

三年的研究實是很不容易的過程，宛如從一個不懂研究的小 baby 到現在可以稍稍在這個深奧的研究世界站穩腳步。這些成果也不是一個人可以獨立完成，在這個過程中讓我體會到“彼此”幫忙和付出重要性，我想下面我會用感謝來對幫助我完成這個研究所有人去表達我心中最深的敬意。

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~我每逢想念你們，就感謝我的 神；每逢為你們眾人祈求的時候，常是歡歡喜喜地祈求。因為從頭一天直到如今，你們是同心合意的興旺福音。我深信，那在你們心裡動了善工的必成全這工，直到耶穌基督的日子。
腓立比：1：3-6

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究失敗，可以被你簡單的話語給打氣·欣娣，也謝謝你在台南請我吃很棒的大餐，讓我從原本落寞心情可以放鬆和期待·還有 Campus 姐妹，你們為我做的禱告書，讓我知道有一群家人陪我面對困境·

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～ 謹記於 2005 年 7 月

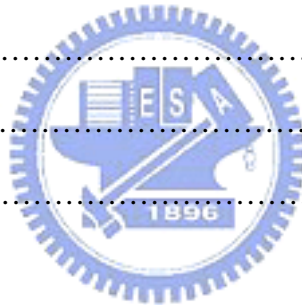
新竹風城～

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Table Captions

Table I. Major electrical parameters of the conventional and novel Poly-Si TFTs . The On/Off current ratio is measured at $V_{gs}=5$ V. The field-effect mobility (μ_{fe}) is measured in the linear region at a V_{ds} of 0.1 V. The threshold voltage is defined at a normalized drain current of (100 nA) x (W/L) at $V_{gs} = 5$ V; W/L = 50/50 ($\mu\text{m}/\mu\text{m}$)

Table II. Major electrical parameters of the conventional and novel Poly-Si TFTs . The On/Off current ratio is measured at $V_{gs}= 5$ V. The field-effect mobility (μ_{fe}) is measured in the linear region at a V_{ds} of 0.1 V. The threshold voltage is defined at a normalized drain current of (100 nA) x (W/L) at $V_{gs} = 5$ V; W/L = 50/20 ($\mu\text{m}/\mu\text{m}$)



Figure Captions

Chapter 1

Fig. 1-1. A process flow of the fabrication of Poly-Si MOSFET

Fig. 1-2. A cross sectional view of the self-aligned LDD poly-Si TFT

Fig. 1-3. Process flow (a) and cross sectional view (b) of offset poly-Si TFT using anodic oxidation (AO)(a) Fabrication flow of offset (b) A cross sectional view of offset poly-Si TFT. gate using anodic oxidation

Fig.1-4.A cross sectional view of the semi-staggered poly-Si TFT with RPCVD SiO₂ as a gate insulator

Fig. 1-5. A cross sectional view of an inverse staggered poly-Si TFT using PECVD SiN_x and n⁺ a-Si:H layer



Chapter 2

Fig.2-1 Process flow of fabricating the Novel Low-temperature Poly-Si TFTs

Fig. 2-2(a) The Top-View of the novel structures

Fig. 2-2(b) The A-A' cross section of the novel structures

Fig. 2-2(c) The B-B' cross section of the novel structures

Chapter 3

Fig. 3-1 the structure of the conventional TFTs

Fig. 3-2(a) I_{ds} - V_{gs} transfer characteristics of the conventional and the novel LTPS TFTs for $V_{ds}= 5$ V; $W/L= 50/20$ $\mu\text{m}/\mu\text{m}$

Fig. 3-2(b) I_{ds} - V_{gs} transfer characteristics of the conventional and the novel LTPS TFTs for $V_{ds}= 5$ V ; $W/L= 10/25$ $\mu\text{m}/\mu\text{m}$

Fig. 3-2(c) I_{ds} - V_{gs} transfer characteristics of the conventional and the novel LTPS TFTs for $V_{ds}= 5 \text{ V}$; $W/L= 50/50 \mu\text{m}/\mu\text{m}$

Figure. 3-3 The basic structure of an n-channel poly-Si TFT and its band diagram with the three kinds of leakage current mechanisms. G: The generation current, T1: the thermionic field emission current, T2: the field emission current, E_{fns} : quasi-Fermi level of electron at the source, E_{fp} : quasi-Fermi level of hole, E_{fnd} : quasi-Fermi level of electron at the drain.

Fig.3-4 (a) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs with different width for $V_{ds}= 5\text{V}$; $W/L=50/20\mu\text{m}/\mu\text{m}$, $W/L=10/20\mu\text{m}/\mu\text{m}$

Fig.3-4 (b) I_{ds} - V_{gs} transfer characteristics of the conventional LTPS TFTs with different width for $V_{ds}= 5\text{V}$; $W/L=50/20\mu\text{m}/\mu\text{m}$, $W/L=10/20 \mu\text{m}/\mu\text{m}$

Fig. 3-5 The current transmission mechanism of the novel LTPS TFTs

Fig.3-6 (a) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}= 5 \text{ V}$; $W/L=50/50 \mu\text{m}/\mu\text{m}$

Fig.3-6 (b) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}= 1 \text{ V}$; $W/L= 50/50 \mu\text{m}/\mu\text{m}$

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Fig.3-6 (e) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}= 5 \text{ V}$; $W/L= 50/25 \mu\text{m}/\mu\text{m}$

Fig.3-6 (f) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus

overlapped length for $V_{ds}= 5 \text{ V}$; $W/L= 10/50 \mu\text{m}/\mu\text{m}$

Fig.3-7(a) The minimum off-state current versus the gate overlapped length for different W/L .

Fig.3-7(b) The On/Off current ratio versus the gate overlapped length for different W/L .

Fig. 3-8(a) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}= 5 \text{ V}$; $W/L= 50/20 \mu\text{m}/\mu\text{m}$

Fig. 3-8(b) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}= 5 \text{ V}$; $W/L= 50/50\mu\text{m}/\mu\text{m}$

Fig. 3-8(c) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}= 5 \text{ V}$; $W/L= 10/50 \mu\text{m}/\mu\text{m}$

Fig. 3-8(d) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}= 5 \text{ V}$; $W/L= 10/20 \mu\text{m}/\mu\text{m}$

Fig. 3-9(a) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L= 50/20\mu\text{m}/\mu\text{m}$

Fig. 3-9(b) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L= 50/20\mu\text{m}/\mu\text{m}$

Fig. 3-9(c) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L= 50/50 \mu\text{m}/\mu\text{m}$

Fig. 3-9(d) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L= 50/50\mu\text{m}/\mu\text{m}$

Chapter 1

Introduction

1.1 Overview of Polycrystalline Silicon Thin-Film Transistors Technology

In 1966, the first polycrystalline silicon thin-film transistors (Poly-Si TFTs) were fabricated by Fa et al. [1]. Since then, many research reports have been proposed to study their conduction mechanisms, fabrication processes and device structure to improve the performance. In 1970s, the conduction mechanism and the electrical properties of polysilicon films, which are determined by the properties of grain-boundaries, were clarified [2],[3]. In 1983, the first practical application of poly-Si TFT's to liquid-crystal displays (LCDs) was announced for full-color pocket TVs [4], and then commercialized in 1984 as the world's first. To date, Poly-Si TFT's have been expanding in applications to linear image sensors[5], thermal printer heads[6], liquid-crystal shutter arrays for printers[7], photodetector amplifier[8], high-density static random access memories (SRAMs)[9],[10], nonvolatile memories[11],[12], and active-matrix LCDs(AMLCDs)[13]-[16].

The dominant leakage current mechanism in poly-Si TFTs is the field emission via grain boundary traps by a high electric field near the drain [17]. Thus, reducing the electric

field near the drain junction is required. Today, many device structures have been proposed to improve poly-Si TFTs performance. For example, Offset Gated Structure (Offset TFTs) [18]-[19] and Lightly Doped Drain Structure (LDD TFTs) [20]-[21] are two kinds of new TFT structures. Both of them were proposed due to suppress the off-state leakage current, but the on-state current is lowered at the same time. Besides, an extra mask in LDD structures and misalignment in Offset TFTs are two major problems. Thus, how to reduce off-state current without degrade on-state current too much is a trade-off.

1.2 Several Novel High Performance Structures for TFTs



To realize large-area LCDs with peripheral circuits, it is essential to develop a low-temperature fabrication process for high-mobility poly-Si TFTs. Such a process would reduce fabrication costs by allowing use of a low-cost glass substrate [22-24].

Generally speaking, Poly-Si TFTs have two different structures : top-gate coplanar structure and bottom-gate structure. The top-gate TFTs have mainly used in AMLCD applications because their self-aligned source/drain regions provide low parasitic capacitances and is suitable for device scaling down. On the other hand, though bottom-gate TFTs have better interface and higher plasma hydrogenation rate than top-gate TFTs, They have lower

current and need extra process steps for backside exposure.

Kamins et al. reported CW Kr laser annealed poly-Si MOSFET with a mobility of $320 \text{ cm}^2/\text{Vs}$ by using quartz as a substrate [25]. This poly-Si MOSFET was an initial poly-Si TFT using laser annealing. The fabrication process was based on that used in silicon IC fabrication in order to retain the transistor stability associated with the thermally grown silicon/silicon-dioxide interface. Figure 1-1 shows process flow of the fabrication of the laser-annealed poly-Si MOSFET. Troxell et al. also reported the laser-annealed poly-Si MOSFET with a field effect mobility of $270 \text{ cm}^2/\text{Vs}$ using thermal SiO_2 by similar process with that of Kamins [26].



On the other hand, Seki et al. reported high performance CW Ar laser annealed poly-Si TFT with a high mobility of $200 \text{ cm}^2/\text{Vs}$ by using thermally grown SiO_2 as a gate insulator [27]. Their poly-Si TFT with lightly doped drain (LDD) structure exhibited a low leakage current of $6 \times 10^{-13} \text{ A}$ and a high on/off current ratio of 10^8 . Figure 1-2 shows a cross sectional view of the self-aligned LDD structure poly-Si TFT.

Itoh et al. has developed an offset structure poly-Si TFT using anodic oxidation (AO) of Al gate [28]. Figure 1-3 shows a fabrication flow and a cross sectional view of the offset poly-Si TFT. An aluminum layer of 400 nm thickness is deposited for a gate electrode by sputtering at room temperature. A thin aluminum oxide is formed on the surface of Al by AO (anodic oxidation) to prevent the hillock formation during the following steps. After

patterning the gate electrode, AO is performed again, at which step the offset length is precisely determined because of its fine controllability of the oxide thickness (Fig 1-3 a). Offset gate structure using AO technology was adopted to decrease both the off-state leakage current and photomask number, respectively. As well as the offset poly-Si TFT can be fabricated with only 4 photo-mask steps.

Kohno and Sameshima et al. reported the high performance semi-staggered poly-Si TFT with the highest mobility of $640 \text{ cm}^2/\text{Vs}$ using remote plasma (RP) CVD SiO_2 . Figure 1-4 shows a cross sectional view of semi-staggered poly-Si TFT. Recently, Okabe et al. reported the offset structure poly-Si TFT with a TEOS SiO_2 as a gate insulator. The TEOS SiO_2 has advantages of good step coverage and low ion damage. Therefore, the large area high performance poly-Si TFT-LCD using TEOS SiO_2 can be available due to these merits.

Aoyama et al. has developed the inverse staggered poly-Si TFT using n^+ a-Si:H ohmic contact in which the active layer is poly-Si/a-Si:H stacked on gate insulator [29]. They proposed the simultaneous process of a-Si:H TFT in the pixel area and of poly-Si TFT in the driver circuits area. Figure 1-5 shows the inverse staggered poly-Si TFT using PECVD SiN_x and n^+ a-Si:H ohmic layer. Field effect mobilities of 10 and $0.5 \text{ cm}^2/\text{Vs}$ were obtained for the laser annealed poly-Si and a-Si:H (without laser annealing) TFTs, respectively. The leakage currents of the both TFTs were good comparable to those of the conventional a-Si:H TFT.

1.3 Main Issues in LTPS TFTs

Although it is useful to use the Poly-Si TFTs instead of the amorphous TFTs by high mobility, the Poly-Si TFTs suffer from high leakage currents in the off-state operations and high kink effect in on-state operations, which can be attributed to the grain boundary traps in the channel region. Besides, the long-term stability is also an important issue for Poly-Si TFTs. It has been reported that the devices' degradation is mainly related to channel carrier density under the stressing and unlike the hot carrier effects in the-crystal Si devices. After the stressing on the Poly-Si TFTs, the devices' parameters such as the threshold voltage, the sub-threshold swing, the mobility, the channel trap density, the off-state current, and on-state current will be degraded. Self-heating effect is also reported as another degradation mechanism especially occurred in the wide-channel Poly-Si TFTs.

1.4 Motivation

The high driving current as well as the mobility are the reasons to use the Poly-Si TFTs instead of the amorphous TFTs. However, the undesired off-state leakage current for a Poly-Si TFT is much higher than that of an amorphous TFT. It is well known that off-state

leakage current mechanism is the field emission via grain boundary traps due to high electric field in the drain depletion region [30]. Thus, suppressing the off-state leakage current by reducing the drain electric field is required. Several methods have been proposed to achieve this purpose, such as offset gated structure [31], lightly doped drain structure [32] and field induced drain structure [33], [34]. In the lightly doped offset drain structure, the implant damage can cause an undesired degradation in the drain junction, especially for low-temperature processed poly-Si TFT's [35]. In the field induced drain structure, an additional photo masking step is required and unavoidable photo masking misalignment error will occur [33], [34].

In this paper, we proposed a new fabrication process of the low-temperature Poly-Si (LTPS) TFT with a thick source/drain region and a thin channel which has lower minimum off-state current and higher on/off current ratio than those of a conventional structure. The process also does not require any additional mask step.

1.5 Thesis Organization

In chapter 1, a brief overview of LTPS TFT technology and related applications were introduced.

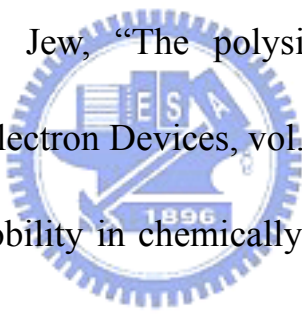
In chapter 2, the fabrication process flow of the new TFT device, experimental

recipes, and device parameter extraction methods will be described.

In chapter 3, we will show the electrical property of the novel TFT device, includes transfer characterization, output characterization.

Finally, conclusions and future work as well as suggestion for further research and given in chapter 5.

1.6 References

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Chapter 2

Experimental of the Novel Structure of LTPS TFTs

2.1 The Fabrication Process flow of the Novel Low-temperature Poly-Si TFTs

The poly-Si TFTs were fabricated on 4-inch-diameter p-type silicon wafer. Fig.2-1 shows the process flow of the proposed poly-Si TFTs. The device has a thick source/drain region (300 nm) and a thin channel region (50nm). The thick source/drain region could be used to obtain good source/drain contact and reduced series resistance. And the thin channel region could be used to obtain high on-state current and low off-state current [1].

The 300nm undoped amorphous silicon (a-Si) films were initially deposited on 500nm thermally oxidized silicon (100) wafers by low-pressure chemical vapor deposition (LPCVD) system with silane (SiH_4) gas at 550°C . The deposition pressure was 100 mtorr and the silane flow rate was 40 sccm. After the active region was patterned using reactive ion etching (RIE), thin channel (50 nm) region was formed at this mask step. Then the deposited a-Si film was annealed in nitrogen ambient at 600°C for 24 h to become the Poly-Si film as shown Fig.2-1(c). A 50 nm-thick TEOS oxide film was deposited at 350°C to serve as the gate dielectric by PECVD. Then, a 300 nm thick Poly-Si was deposited by LPCVD at 600°C with

SiH₄ for the gate electrode.

After patterned the gate region as, the remnant 50-nm oxide film and 50-nm poly-Si film were also removed using the RIE system. In this step, the isolation region, the thick undoped source/drain region (300 nm) and gate overlap region were formed. After the photoresist was removed, Gate, Source and Drain regions were formed by ion implantation of Phosphorous (Dose= $5 \times 10^{15} \text{ cm}^{-2}$ at 60 keV). The dopant were activated at 600°C in N₂ ambient for 24 hr. Next, a 500 nm TEOS oxide was deposited by PECVD at 350°C as a passivation layer, and contact lithography was carried out. After opening contact holes, a 600 nm Al was deposited by evaporation and the metal layer was patterned. Finally, the samples were sintered at 400°C for 30min in N₂ gas ambient. No hydrogenation step was performed on these devices.

The total masks of our fabrication process are four masks, which are less than those of conventional process in staggered Poly-Si TFTs. For comparison, the conventional Poly-Si TFT's with 50-nm channel thickness were also fabricated at the same time.

The detailed fabrication process flow is listed as follows.

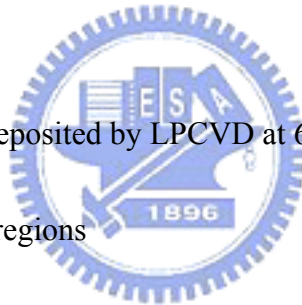
1. (100) orientation Si wafer
2. Initial cleaning
3. Thermal wet oxidation at 1050°C to grow 5000Å thermal SiO₂ in furnace

4. 3000 Å a-Si was deposited by LPCVD at 550° C in SiH₄ gas
- 5.. Mask#1 : define active regions

(a-Si dry etch by Poly-RIE system)
6. RCA cleaning
7. 500 Å a-Si deposition by LPVCD at 550°C in SiH₄ gas
8. RCA cleaning
- 9.. 500 Å gate dielectric deposition by PECVD at 350°C
10. The deposited a-Si film was annealed in nitrogen ambient 600°C for 24h
11. RCA cleaning
12. 3000 Å poly-Si was deposited by LPCVD at 620°C in SiH₄ gas
13. Mask#2: Define gate regions

(Poly-Si dry etch by Poly-RIE system)
14. Ion implantation: P³¹ , 60KeV, 5x10¹⁵ ions/cm²
15. Dopant activation in N₂ ambient at 600°C for 24h in furnace
16. 5000 Å TEOS oxide was deposited by PECVD as passivation layer
17. Mask#3: Open contact holes

(wet etch by B.O.E)
- 18.. 5000 Å Al thermal evaporation
19. Mask#4: Al pattern defined

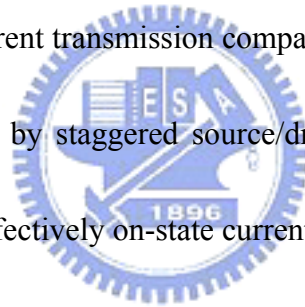


20. Etching Al and removing photoresist
21. Al sintering at 400°C in N₂ ambient for 30 min

2.2 The Cross-Section of Novel Structures

In Fig. 2-2(a), we could see clearly the top-view of the proposed structures.

L_{MC} , $L_{o,d}$ and $L_{o,s}$ represent the length of main channel, gate-overlap in the drain and gate-overlap in the source, respectively. We suggest that the current transmission mechanism might have another path of current transmission compared with conventional sample. Because its width would be increased by staggered source/drain regions ($W' > W$), the novel TFTs appear to be promoted more effectively on-state current.



In Fig. 2-2(c), we see that the B-B' cross section of the novel structures compared to the conventional would increase additional poly channel.

2.3 Methods of Device Parameter Extraction

Many methods have been proposed to extract the characteristic parameter of Poly-Si TFT. In this section, the methods of parameter extraction used in this research are described.

2.3.1 Determination of Threshold Voltage (V_{th})

The threshold voltage V_{th} is an important MOSFET parameter required for the channel length-width and series resistance measurement. However, V_{th} is a voltage that is not uniquely defined. Various definitions exist and the reason for this can be found in the I_D - V_{GS} curves. One of the most common threshold voltage measurement techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of typically 50-100 mV to ensure operation in the linear MOSFET region [2]. But the drain current is not zero below threshold and approaches zero only asymptotically. Hence the I_D versus V_{GS} curve is extrapolated to $I_D=0$, and the threshold voltage is determined from the extrapolated or intercept gate voltage V_{GSi} by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \quad (\text{Eq. 2.1})$$

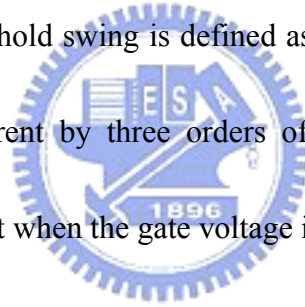
Equation (2.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain currents where threshold voltage measurements are made. The I_D - V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to subthreshold currents and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope on the I_D - V_{GS} curve by maximum in the transconductance fit a straight line to the I_D - V_{GS} curve at that point and extrapolate to $I_D=0$.

2.3.2 Determination of Subthreshold Swing

Subthreshold swing S.S (V/dec) is a typical parameter to describe the control ability of gate toward channel. That is the turn on/off speed of a device. It is defined as the amount of gate voltage requires to increase/decrease drain current by one order of magnitude.

The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short channel effect such as charge sharing, avalanche multiplication, and punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as serial resistance and interface state.

In my thesis, the subthreshold swing is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.



2.3.3 Determination of Field Effect Mobility (μ_{FE})

Usually, μ_{FE} is extracted from the maximum value of transconductance (g_m) at low drain bias ($V_{DS}=1V$). The drain current in linear region ($V_{DS}<V_{GS}-V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right) [(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2] \quad (\text{Eq. 2.2})$$

where W and L are width and length, respectively. C_{ox} is the gate oxide capacitance. Thus, g_m is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right) V_{DS} \quad (\text{Eq. 2.3})$$

Therefore,

$$\mu_{FE} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)} \Big|_{V_{DS} \rightarrow 0} \quad (\text{Eq. 2.4})$$

2.3.4 Determination of On/Off Current Ratio

On/Off current ratio is one of the most important parameters of poly-Si TFTs. Since a good performance means not only large On current but also small Off (leakage) current. The leakage current mechanism in poly-Si TFTs is not like it in MOSFET. In MOSFET, the channel is composed of single crystalline and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel layer region. However, in poly-Si TFTs, the channel is composed of poly crystalline. A large amount of trap densities in grain structure attribute a lot of defect state in energy band gap to enhance the tunneling effect. Therefore, the leakage current due to the tunneling effect is much larger in poly-Si TFTs than in single crystalline devices. When the voltage drops between gate voltage and drain voltage increase, the band gap width decrease and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFT I_D - V_G characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decrease/increase for n/p-channel TFTs.

There are a lot of ways to specify the On and Off current. In my thesis, take n-channel poly-Si TFTs for examples, the On current and Off current is defined as the drain current when gate voltage equal to 15V and drain voltage is 1 V(linear operation mode). The Off

current is specified as the minimum leakage current in linear operation mode for usual cases.

$$\frac{I_{ON}}{I_{OFF}} = \frac{\text{Maximum current of } I_{DS} - V_{GS} \text{ plot at } V_{DS} = 1V}{\text{Minimum current of } I_{DS} - V_{GS} \text{ plot at } V_{DS} = 1V} \quad (\text{Eq. 2.5})$$

2.4 References

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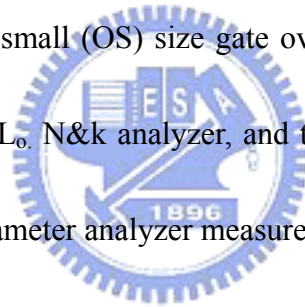
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Chapter 3

The Characteristics of Novel Gate-Overlapped Low-Temperature Poly-Si TFTs with Stagger Source/Drain Regions

In this paper, we will discuss the device performances of Poly-Si TFTs with different structures including traditional TFTs as shown Fig 3.1 and Novel TFTs we proposed. In addition, we make three different ranges in overlapped gap about novel TFTs we proposed. In later sections, Long (OL) and small (OS) size gate overlap length have been compared. We define gate-overlapped length L_o . N&k analyzer, and the I-V characteristics of Poly-Si TFTs by HP4156 semiconductor parameter analyzer measured the thicknesses of the films.



3.1 The Electrical Properties of Novel TFTs and Conventional TFTs

Conventional Poly-Si TFTs suffer from an anomalous off-state leakage current which increases with drain voltage and voltage [1]. This undesirable off-state leakage current less than 1 pA per pixel is needed for a gray-scale active matrix LCD [2]. In order to lower the leakage current in Poly-Si TFTs that occurs by field emission via grain boundary traps due to

the high electrical field near the drain junction [3]. Many efferots have been introduced to improve drain electrical field [4]-[5]. Because of gate-overlapp and thick S/D regions [6]-[7], We believe it will lower effectively drain electrical field.

Fig. 3.2(a), Fig. 3.2(b) and Fig. 3-3(c) show the gate transfer characteristics of the novel TFTs compared to the conventional TFTs. Obviously, the novel TFTs exhibit the best off-state leakage compared to the conventional devices. It is well known that thicker drain would result in the lower maximum lateral electrical field. The well-known El-Mansy/Ko model [4] and [5] describes the maximum channel field for bulk MOSFET's as

$E_{\max} = (V_{ds} - V_{d,sat})/l$, where the characteristic length l is given as

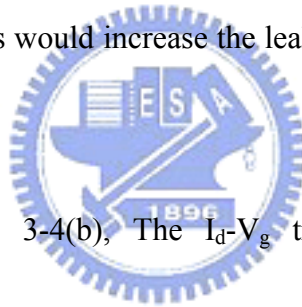
$$l = [(\epsilon_{Si} \epsilon_{ox}) * t_{ox} x_j]^{1/2}$$

and ϵ_{Si} and ϵ_{ox} are the permittivities for Si and SiO₂, respectively; t_{ox} is the gate oxide thickness, and x_j is the drain junction depth. Hence, it can be concluded that for a given oxideness, the E_{\max} can be reduced by increasing the junction depth.

In order to explain the different phenomenon of the leakage current when the gate bias is very low ($V_g = 0 \sim -10$ V) and very high ($V_g < -10$ V), we would study these results using the model for the leakage current mechanisms. Chul Ha Kim and Ki-Soo Sohm proposed the model in 1997[8]. The three kinds of leakage current for a Poly-Si TFT for the model can be considered. First, when the drain voltage is very low ($V_d < 5$ V), the leakage current is governed by thermally generated carriers via trap states, which is denoted by G in Fig.3-3.

The leakage current therefore is dependent on the drain voltage. While the gate bias is high enough ($V_g < -10V$), the leakage current is generated by the field tunneling which is denoted by T2 and T1 in Fig. 3-3. So, the leakage current is dependent on the lateral electric field and the grain-boundary traps. Obviously, the lower drain electric field decreases the leakage current which is governed by G mechanisms in Fig. 3-3. We suggest that leakage current of the novel TFTs are lower compared to the conventional. when the drain bias is low ($V_d=5 V$) because of the lower drain electric field by thicker drain junction. In the condition of $V_g < -10V$, the leakage current of the novel TFT are higher because of more traps generated from overlapped regions. These traps would increase the leakage current paths governed by T1 and T2

Fig. 3-3.



In Fig. 3-4(a) and Fig. 3-4(b), The I_d-V_g transfer characteristics of novel and conventional TFTs with different widths were compared. Obviously, in Fig. 3-4(a), at $V_{gs}=30V$, the ratio $I_{on}(W=50)/I_{on}(W=10)$ is about 13. But in Fig. 3-4(b), at $V_{gs}=30V$, the ratio $I_{on}(W=50)/I_{on}(W=10)$ is about 6.36. The former is two times larger than the latter. So, we believe that our novel structure will promote effectively on-state current as width increasing. We also proposed a model to explain the better on-state current improvement. In Fig. 3-5, the current transmission mechanism for the novel TFTs had been proposed. We suggested that it might have another path of current transmission compared with conventional sample. The active region under the whole of gate region was defined using gate mask.

Therefore, the width of active region would be equal to that of gate region (W'). The carriers could be transferred in this large-width active region. So, the proposed structure exhibits a better on-state current improvement.

In Fig. 3-6(a), (b), (c), (d), (e) and (f), we show the characteristics of novel TFTs with different gate-overlapped length. Several reports have demonstrated that an offset structure has been widely used to reduced the leakage current and enhance device reliability by suppressing the electric field near the drain junction [9],[10]. However it might degrade the driving capability due to the large series resistance. We proposed a novel four-mask steps poly-Si TFT with thick S/D and thin channel regions. The basic concept of the structure is that the thin channel region is used to achieve high on-state current [11], and the thick drain region is used to reduce the lateral electric field, thereby suppressing the kink current and minimizing the leakage current. In Fig. 3-6(a), obviously, both the On/Off current ratio (measured at maximum on-state current/minimum off-state current) and the field effect mobility (measured at $V_{dS} = 0.1V$) for $L_o = 4.5 \mu m$ is slightly higher than those of $L_o = 2.5 \mu m$. It is because that the channel thickness of the gate overlap region is thicker than that of the main channel region, and the thicker channel thickness could be used to obtain the lower on-state current and higher off-state current .Therefore, the On/Off current ratio would be decreased with increasing of the gate overlap length.

We summarize the above-mentioned results in Fig. 3-7(a) and (b).

3.2 The Stability Study of Novel Gate-Overlapped Low-Temperature Poly-Si TFTs with Stagger Source/Drain Regions

Fig. 3-8(a), Fig. 3-8(b), Fig. 3-8(c), and Fig. 3-8(d) show that in two mode measurements, forward and reverse, these results would examine symmetry of novel TFTs. In Fig. 3-8(b), for on-state current, the result of forward measurement consists with the result of reverse measurement. However, for off-state current, the off-state current of the reverse measurement is higher than the forward measurement. We suggest that it is due to misalignment in gate-overlapped regions. Therefore, the device has larger overlap length near the source side in reverse measurement. So the drain electrical field of forward measurement would be higher than reverse measurement. It is well known that higher lateral electric field would cause a higher leakage current. Previous results would cause devices serious stability. Although misalignment error makes stability to be worse, we could solve the problem of the gate overlap misalignment using more accurate and full-automatic mask aligner. In the device of $L=10\mu\text{m}$, it also show similar result, as shown Fig. 3-8(b) and (b)

Fig. 3-9(a), (b), (c) and (d) both show I_{ds} - V_{ds} output characteristics of novel TFTs and conventional TFTs. Super-thin channel polysilicon TFTs are reported to have higher

current drive compared to their thicker film counterparts [12]. However, they experience a high electric field at the channel/drain junction region when the device is operated in the saturation region. The high drain electrical field would lead to hole accumulation in the floating body of the device [13],[14]. The hole accumulation causes a serious kink effect [15]. In Fig. 3-9(a), the kink effect doesn't occur at $V_{gs}=15V$ in the proposed structure; however, it happened at $V_{gs}=10V$, $V_{ds}=35V$ in the conventional structure. We could find that the elimination of the kink effect is obtained due to reduction in lateral electric field at the channel/drain junction region of the proposed TFTs even if higher on-state current density compared to conventional TFTs. In Fig. 3-9(b), both the proposed and conventional TFTs have almost the same drain current I_{ds} . We can find that the kink effect occurred at $V_{ds}=16V$ in the proposed structures. However, it had occurred at $V_{ds}=12V$ in the conventional structures. We appear to obtain results of suppressing the kink effect for the novel structures. We suggest the drain electrical field should be lowered as a result of thicker drain junction depth. By lowering drain electrical field, the effect of hole accumulation will be suppressed. Although we get the lower on-state current in Fig.3-9, it is worthy for us to get trade-off between the stability and high on-state current.

3.3 REFERENCE

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Chapter 4 Conclusions and Future Work

4.1 conclusions

In this letter, a novel n-channel gate-overlapped low-temperature Poly-Si TFT with a thicker source/drain region and thin channel was proposed and investigated. The results shows that excellent current saturation characteristics at high bias are obtain in the proposed device, and exhibits kink-free I-V characteristics, low leakage current compared to conventional TFTs . Moreover, the total masks of our fabrication process are four masks, which are less than those of conventional process in staggered Poly-Si TFT. Therefore, the new process is simple, inexpensive, requires fewer steps than conventional methods, and appears to be quite promising for fabricating Poly-Si TFT's in future high-performance large-area liquid crystal displays.

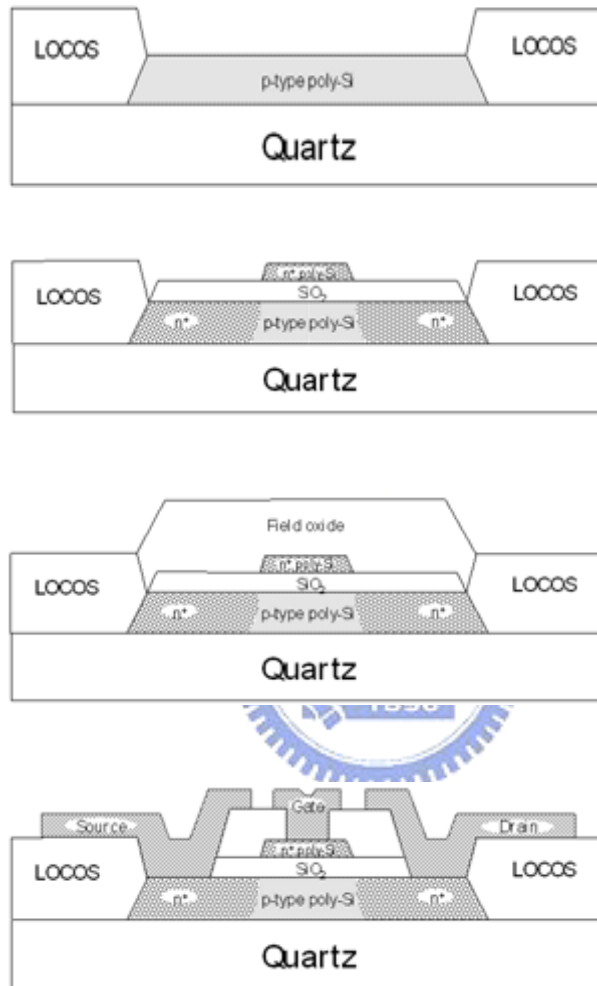
4.2 Future Work

We have proposed a gate-overlapped low-temperature Poly-Si TFTs with a thicker source/drain region and thin channel to improve conventional low-temperature Poly-Si TFTs performance. However, in order to further improve device electrical characteristics and apply to glass substrates, there are still some works worthy of being investigated.

We could adopt LDD structures to improve limited on-state current by gate-overlap and

we can use RTA process instead of furnace thermal annealing to further confirm optimal condition. Moreover, in the study topic of reliability, we could study degradation mechanism by analyzing the evolution of device parameters including transconductance, threshold voltage, and sub-threshold slope by dynamic stress and static stress.





**Fig. 1-1. A process flow of the fabrication of Poly-Si
MOSFET**

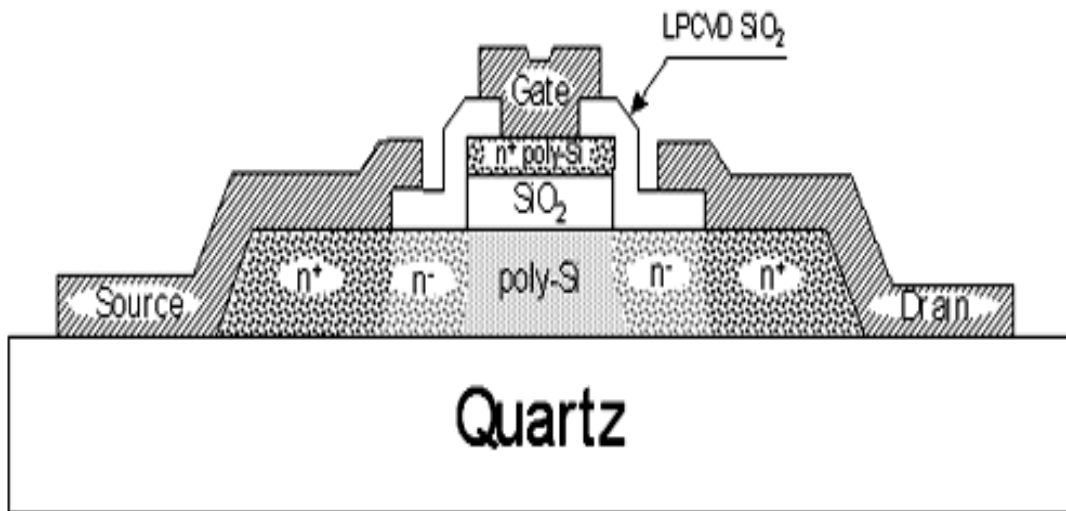
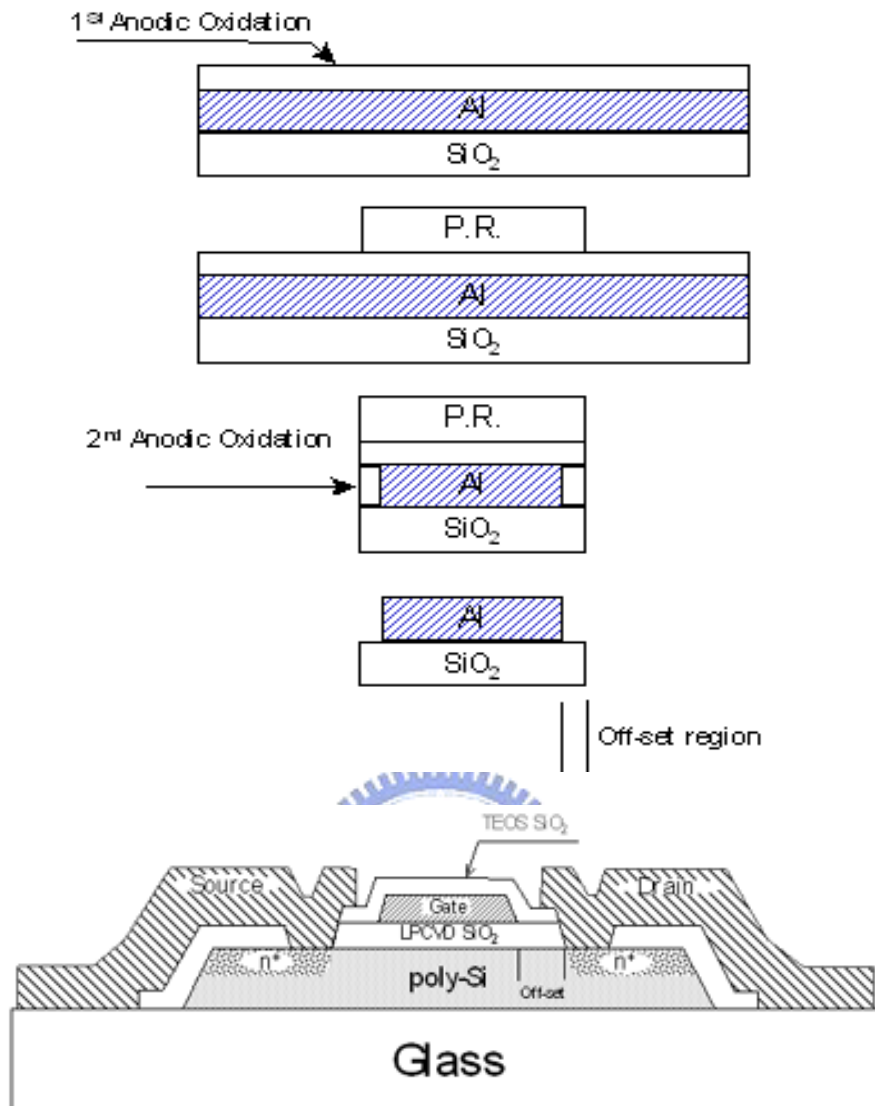
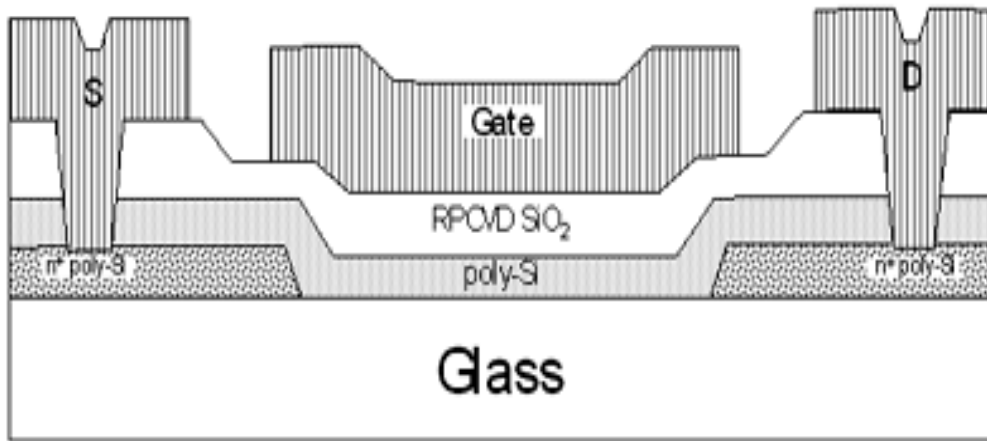


Fig. 1-2. A cross sectional view of the self-aligned LDD poly-Si TFT

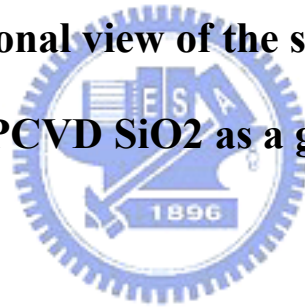


(a) Fabrication flow of offset gate using anodic oxidation (b) A cross sectional view of offset poly-Si TFT. gate using anodic oxidation

Fig. 1-3. Process flow (a) and cross sectional view (b) of offset poly-Si TFT using anodic oxidation (AO)



**Fig. 1-4. A cross sectional view of the semi-staggered poly-Si TFT
with RPCVD SiO₂ as a gate insulator**



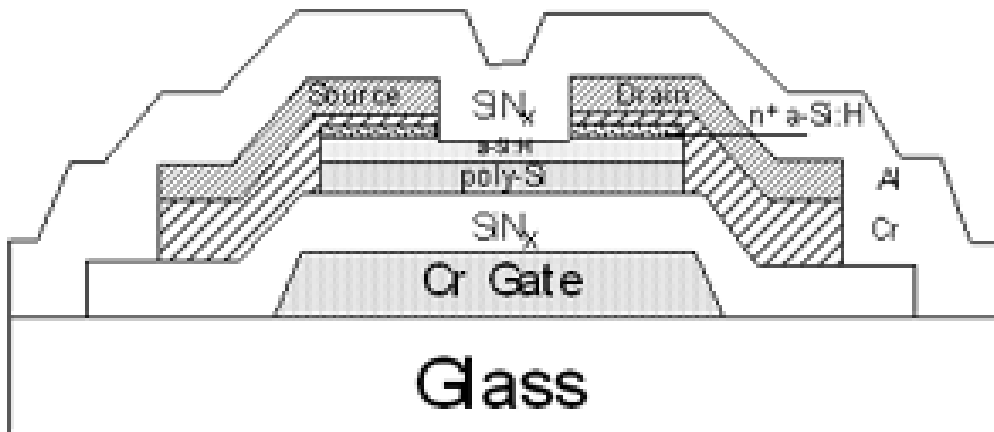
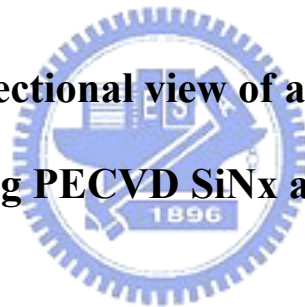
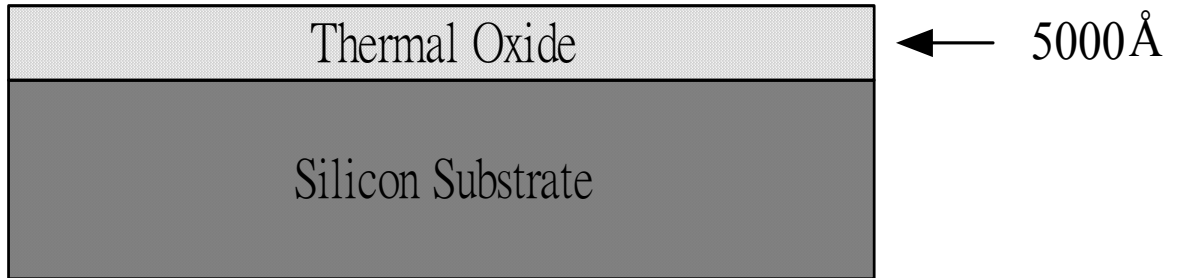
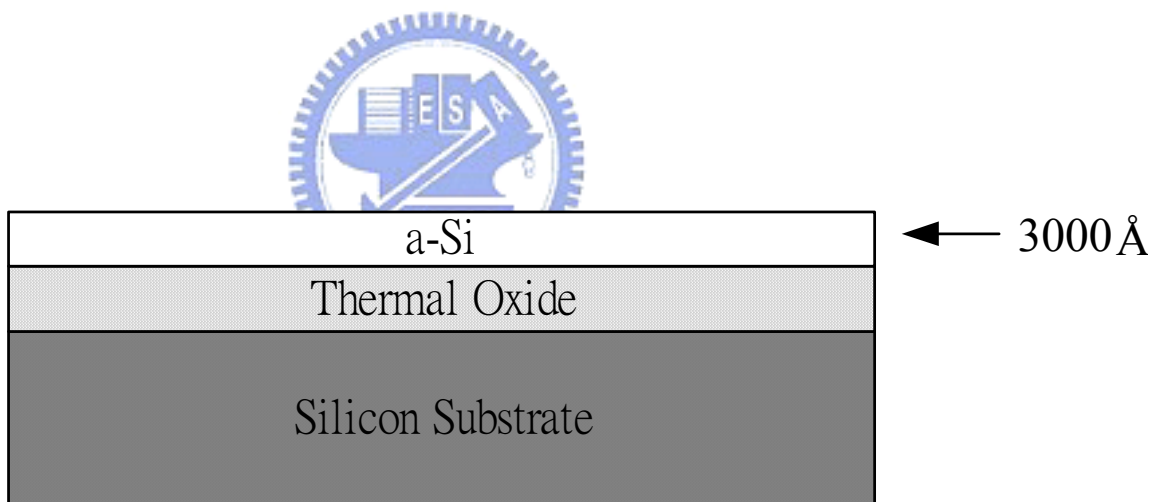


Fig. 1-5. A cross sectional view of an inverse staggered poly-Si TFT using PECVD SiNx and n⁺ a-Si:H layer



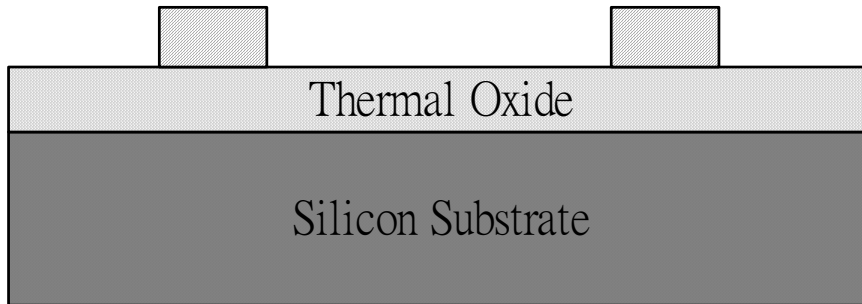


(a) Thermal oxidation

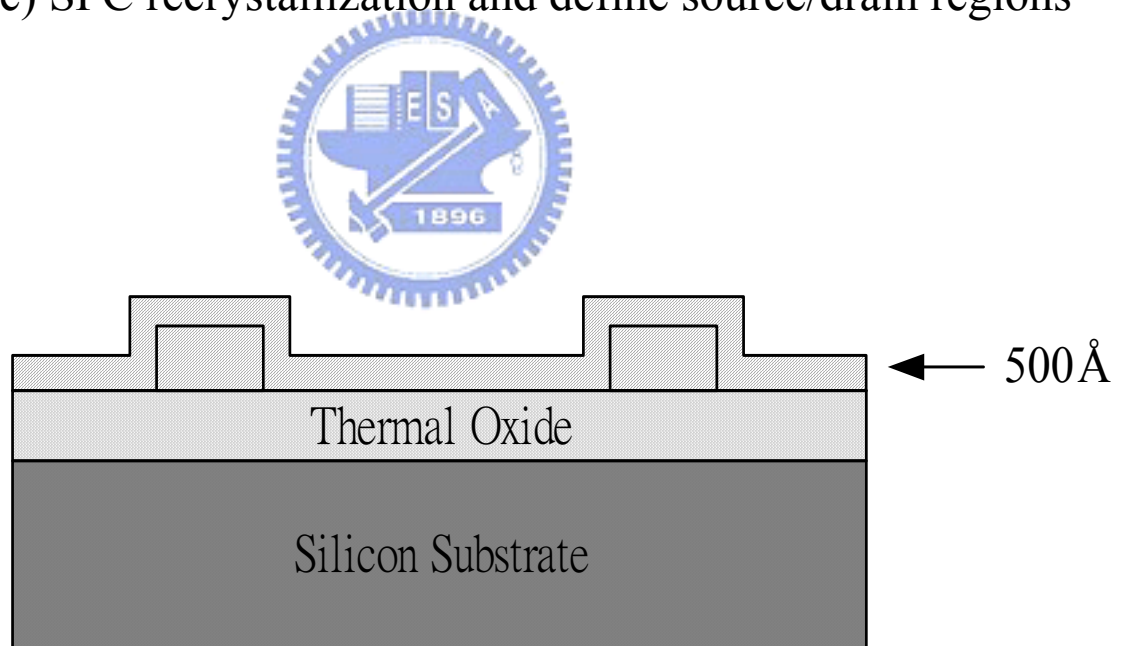


(b) Deposit a-Si by LPCVD

 undoped Poly-Si



(c) SPC recrystallization and define source/drain regions

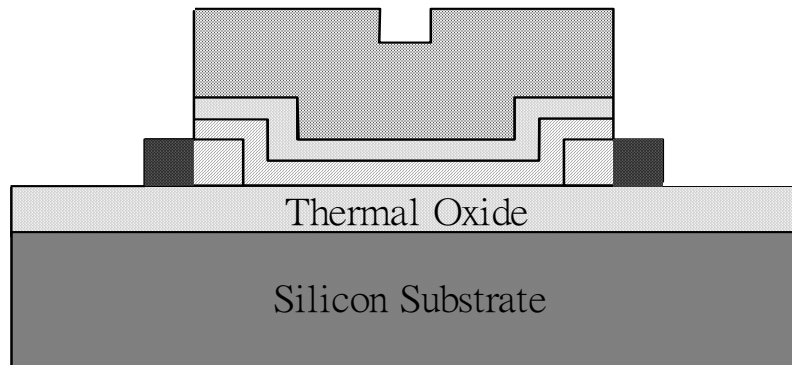
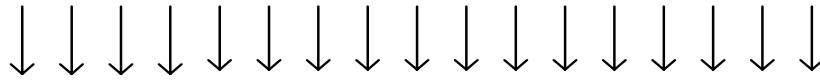


(d) Deposit a-Si by LPCVD and SPC recrystallization
as channel



n+ Poly-Si

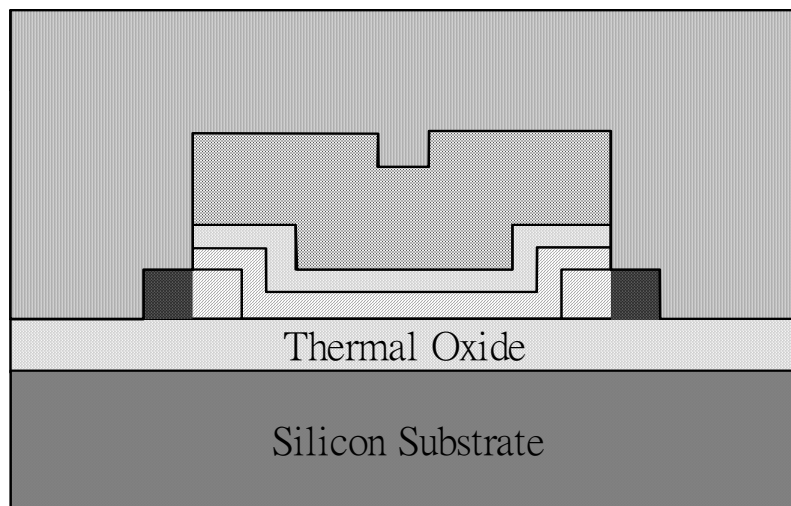
P^{31}



(g) Ion implantation and dopant activation

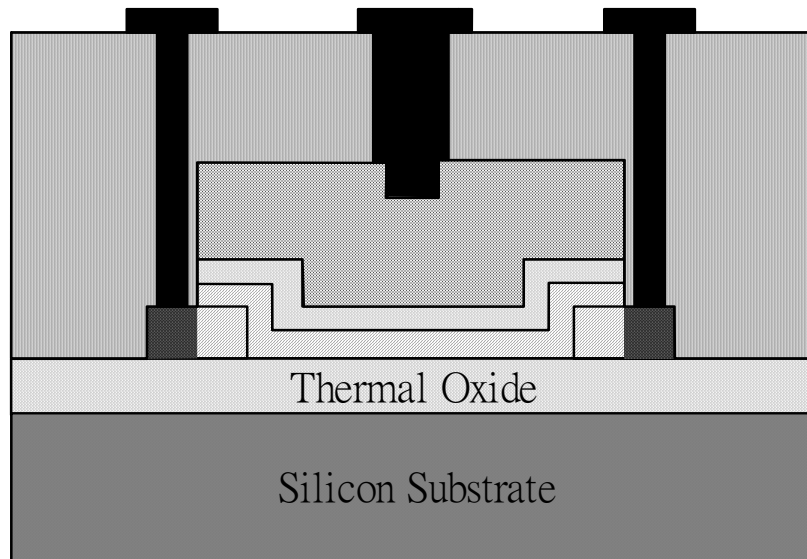


TEOS oxide



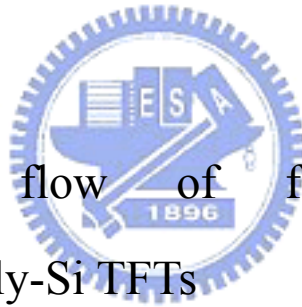
← 5000Å

(h) Deposit PECVD TEOS oxide as passivation layer



(i) Define contact holes and Al electrodes

Fig.2-1 Process flow of fabricating the Novel Low-temperature Poly-Si TFTs



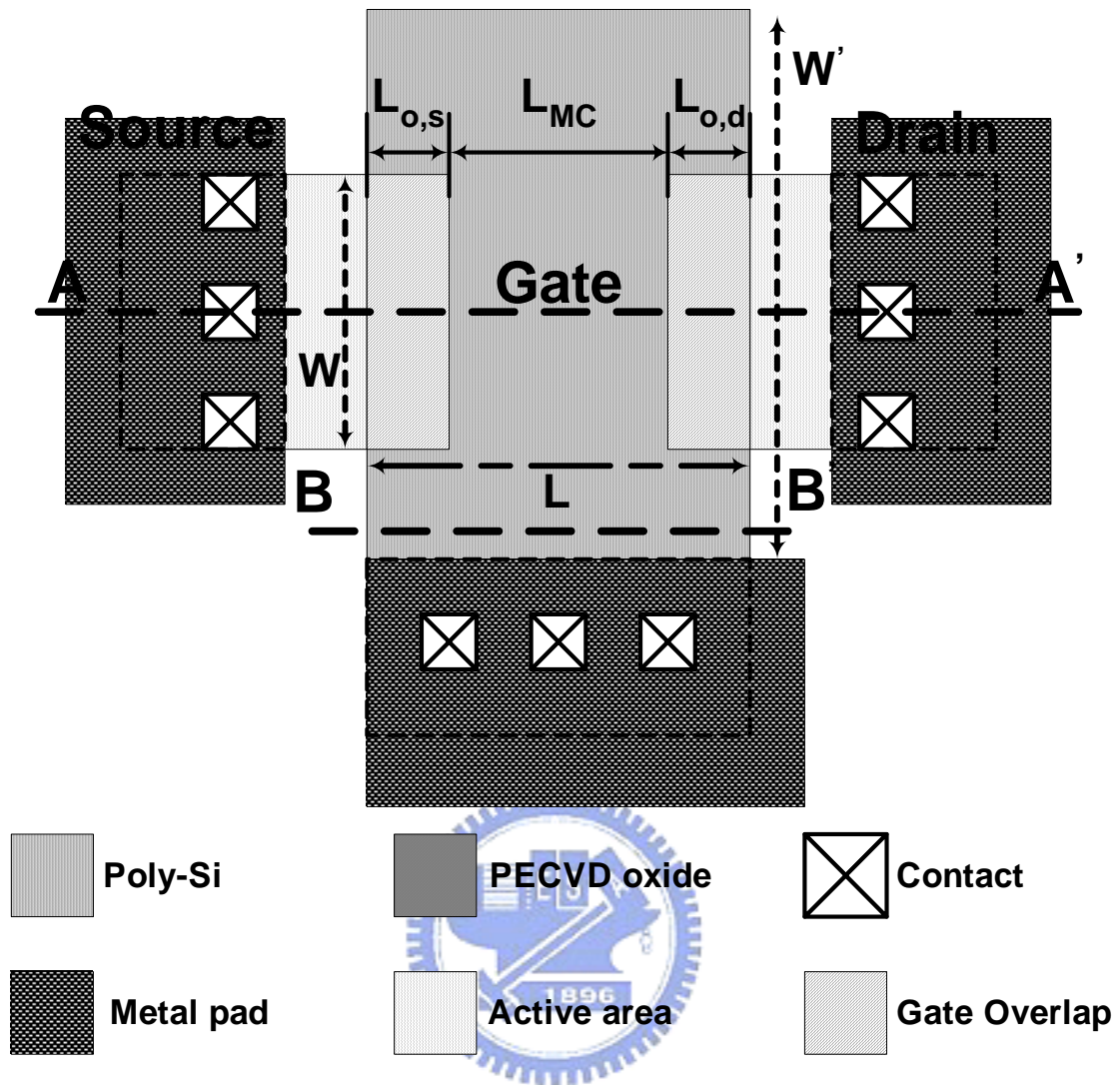


Fig. 2-2(a) The Top-View of the novel structures

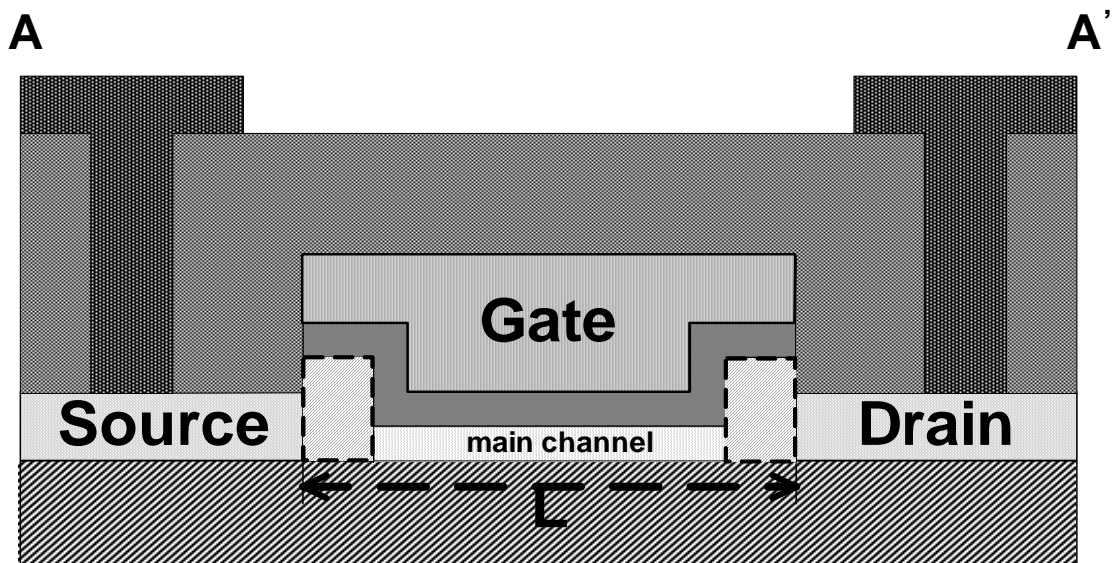


Fig. 2-2(b) The A-A' cross section of the novel structures



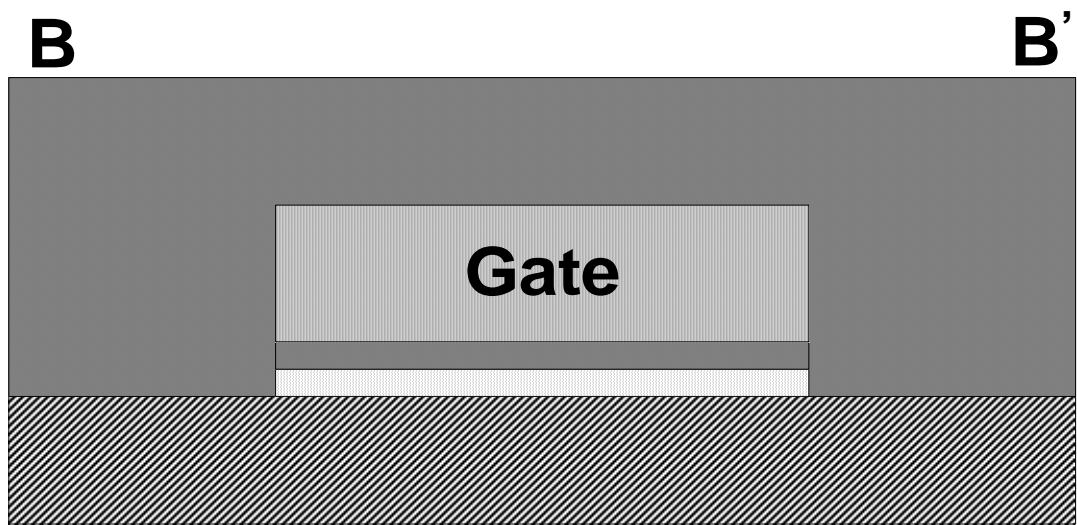


Fig. 2-2(c) The B-B' cross section of the novel structures



Table I

Conventional/Novel TFTs	On/off current ratio($V_{gs}=5V$)	V_{th} (V)	S (V/dec)	μ_{fe} (cm ² /VS)
Conventional	7.78×10^6	10.4687	1.816901	11.91304
Novel	1.85×10^7	11.97333	1.516875	10.6087

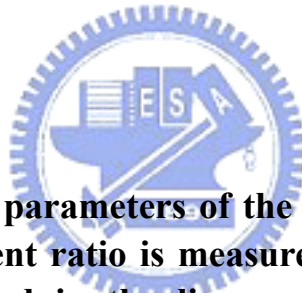


Table I. Major electrical parameters of the conventional and novel Poly-Si TFTs . The On/Off current ratio is measured at $V_{gs}= 5$ V. The field-effect mobility (μ_{fe}) is measured in the linear region at a V_{ds} of 0.1 V. The threshold voltage is defined at a normalized drain current of (100 nA) x (W/L) at $V_{gs} = 5$ V; W/L = 50/50 ($\mu\text{m}/\mu\text{m}$)

Table II

Conventional/Novel TFTs	On/off current ratio($V_{gs}=5V$)	V_{th} (V)	S (V/dec)	μ_{fe} (cm/VS)
Conventional	1.67×10^6	9.424227	1.793857	9.33333
Novel	8.19×10^6	13.56097	1.945159	6.89855

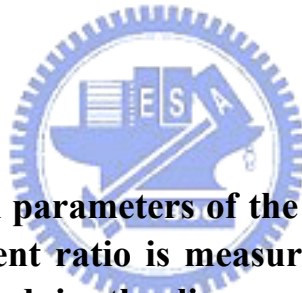


Table II. Major electrical parameters of the conventional and novel Poly-Si TFTs . The On/Off current ratio is measured at $V_{gs}= 5$ V. The field-effect mobility (μ_{fe}) is measured in the linear region at a V_{ds} of 0.1 V. The threshold voltage is defined at a normalized drain current of (100 nA) x (W/L) at $V_{gs} = 5$ V; W/L = 50/20 ($\mu\text{m}/\mu\text{m}$)

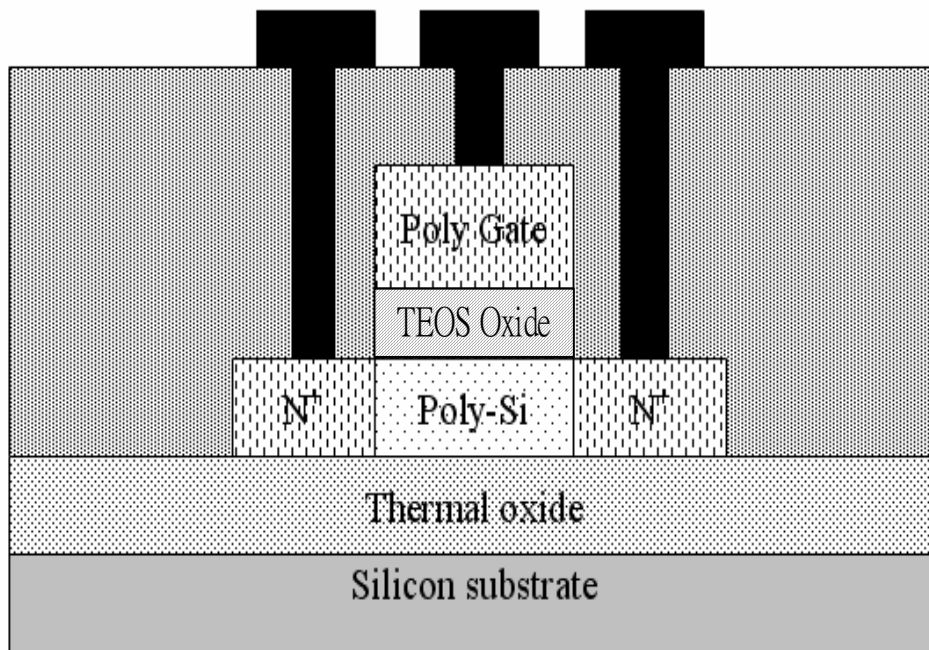


Fig. 3-1 the structure of the conventional TFTs

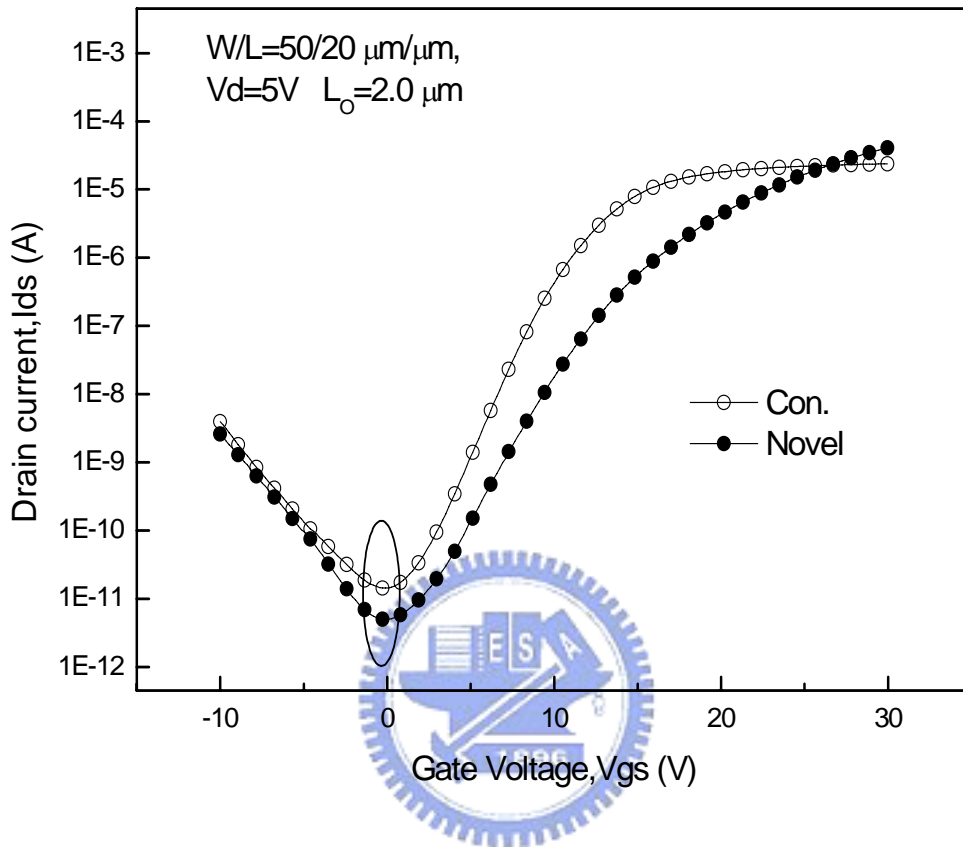


Fig. 3-2(a) I_{ds} - V_{gs} transfer characteristics of the conventional and the novel LTPS TFTs for V_{ds}

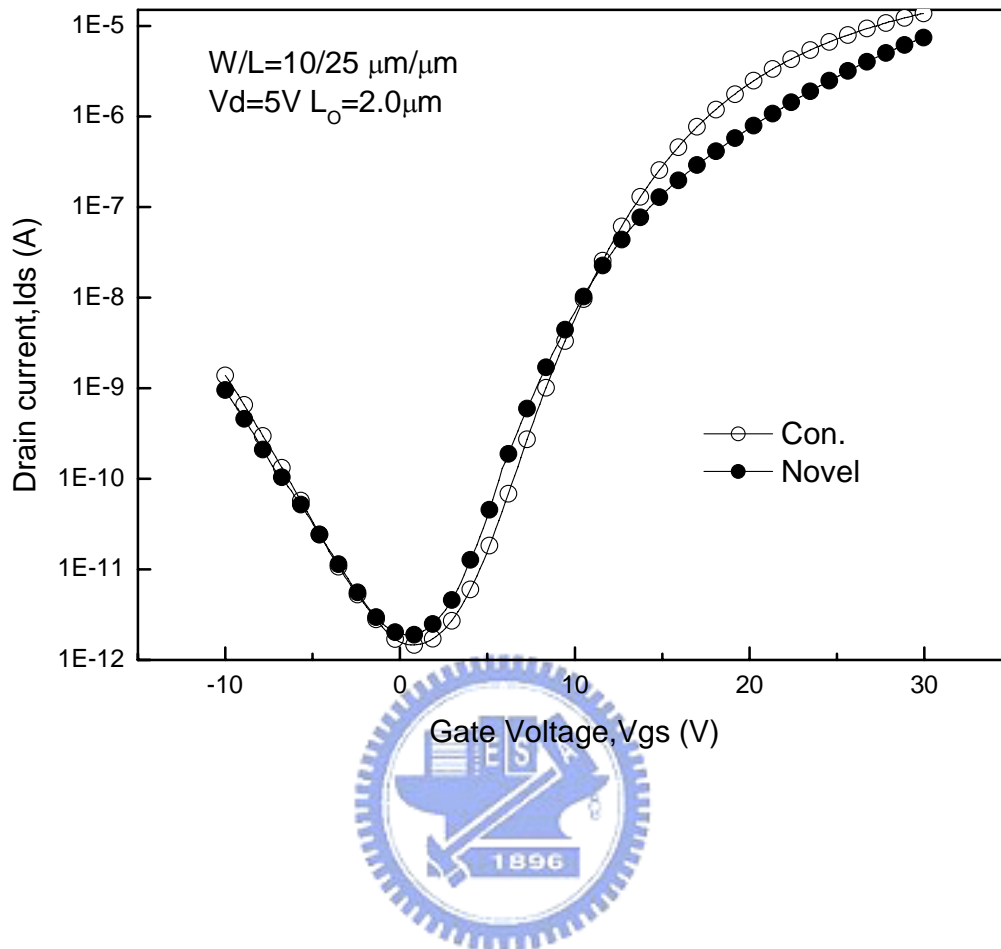


Fig. 3-2(b) I_{ds} - V_{gs} transfer characteristics of the conventional and the novel LTPS TFTs for $V_{ds}=5\text{ V}$; $W/L=10/25\ \mu\text{m}/\mu\text{m}$

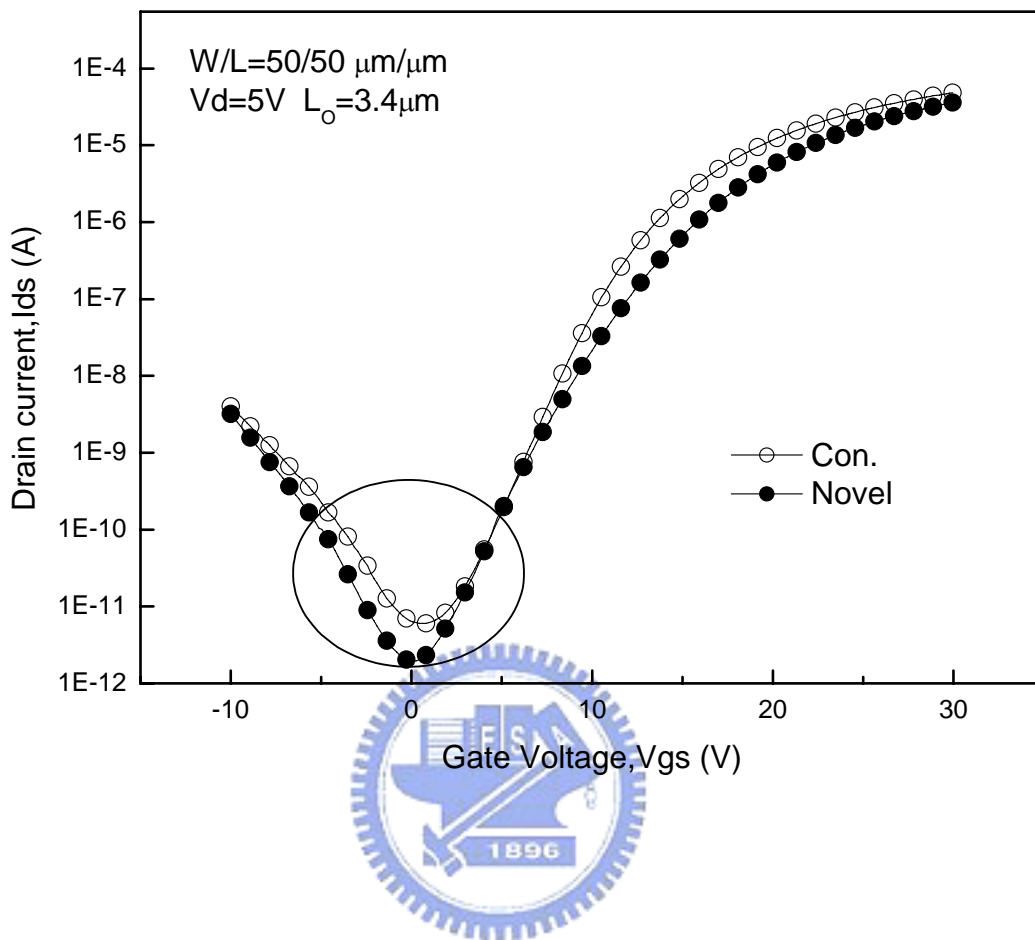


Fig. 3-2(c) I_{ds} - V_{gs} transfer characteristics of the conventional and the novel LTPS TFTs for $V_{ds}=5\text{ V}$; $W/L=50/50\ \mu\text{m}/\mu\text{m}$

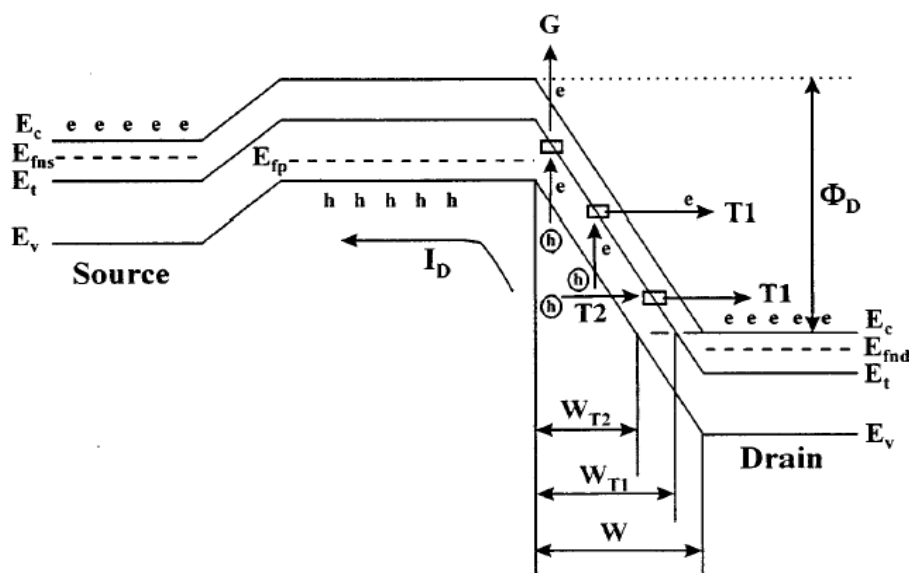
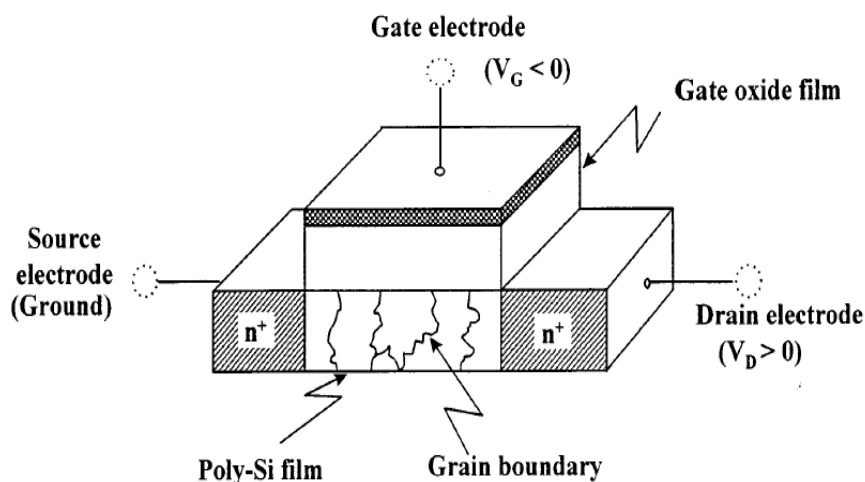


Figure. 3-3 The basic structure of an n-channel poly-Si TFT and its band diagram with the three kinds of leakage current mechanisms. G: The generation current, T1: the thermionic field emission current, T2: the field emission current, E_{fns} : quasi-Fermi level of electron at the source, E_{fp} : quasi-Fermi level of hole, E_{fnd} : quasi-Fermi level of electron at the drain.

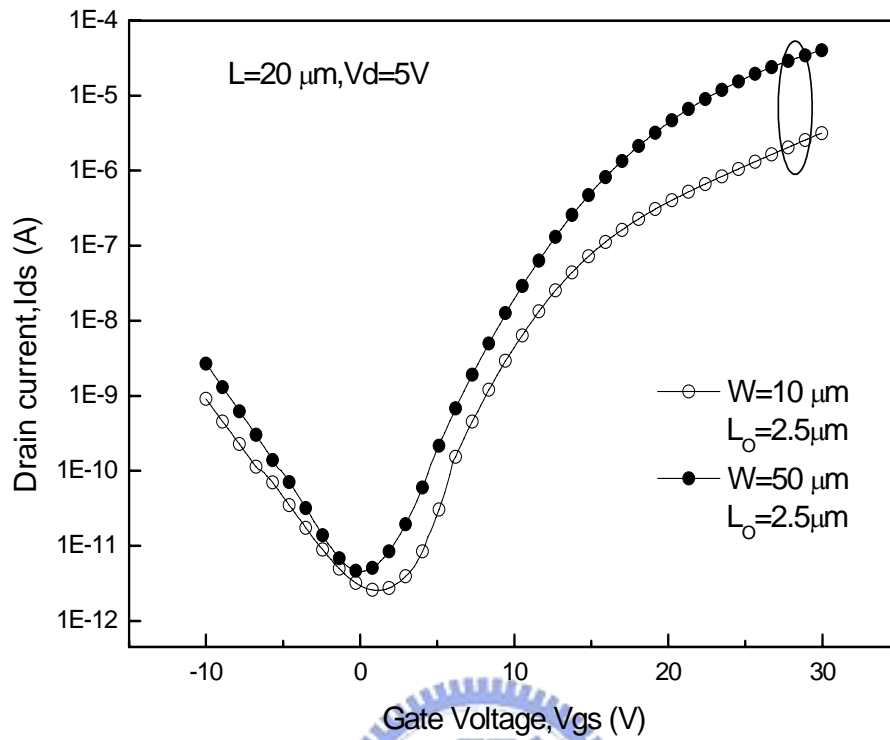


Fig.3-4 (a) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs with different width for $V_{ds}= 5V$; $W/L=50/20\mu m/\mu m$, $W/L=10/20\mu m/\mu m$

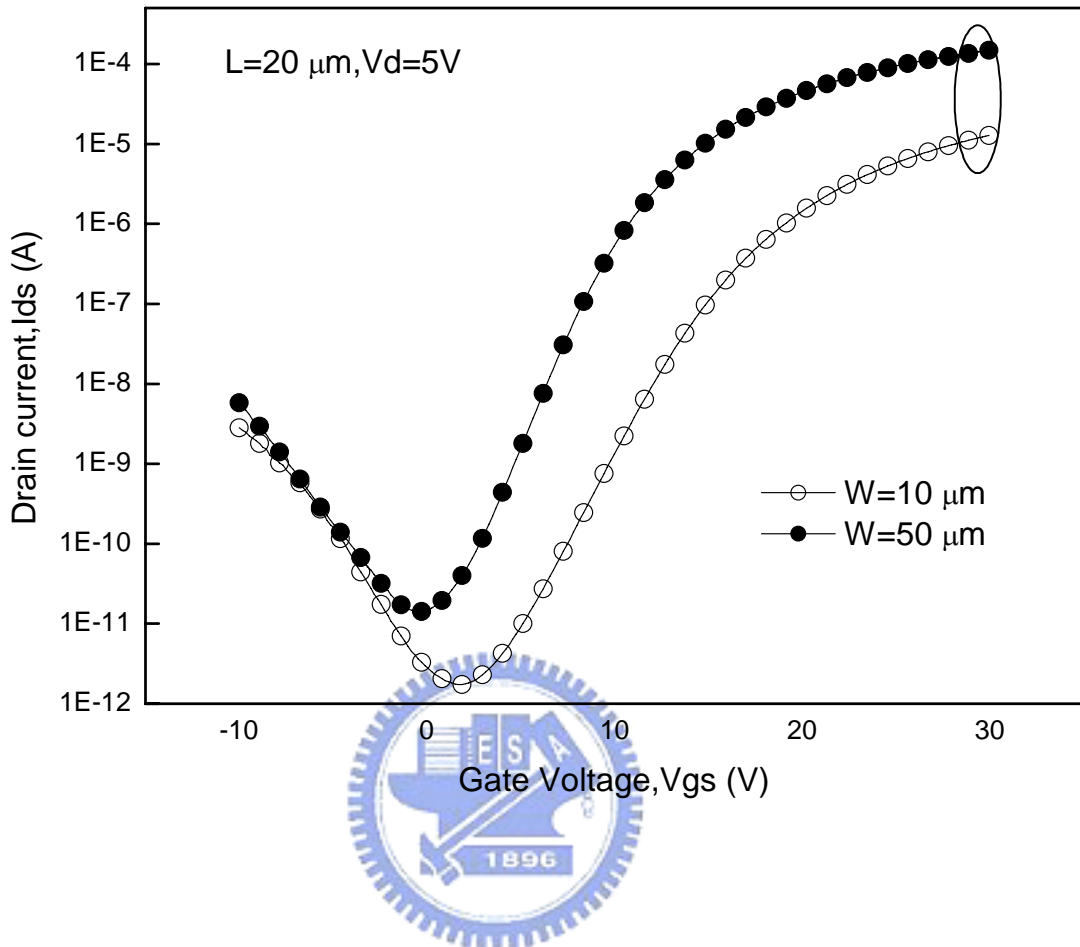


Fig.3-4 (b) I_{ds} - V_{gs} transfer characteristics of the conventional LTPS TFTs with different width for $V_{ds}= 5V$; $W/L=50/20\mu\text{m}/\mu\text{m}$, $W/L=10/20 \mu\text{m}/$

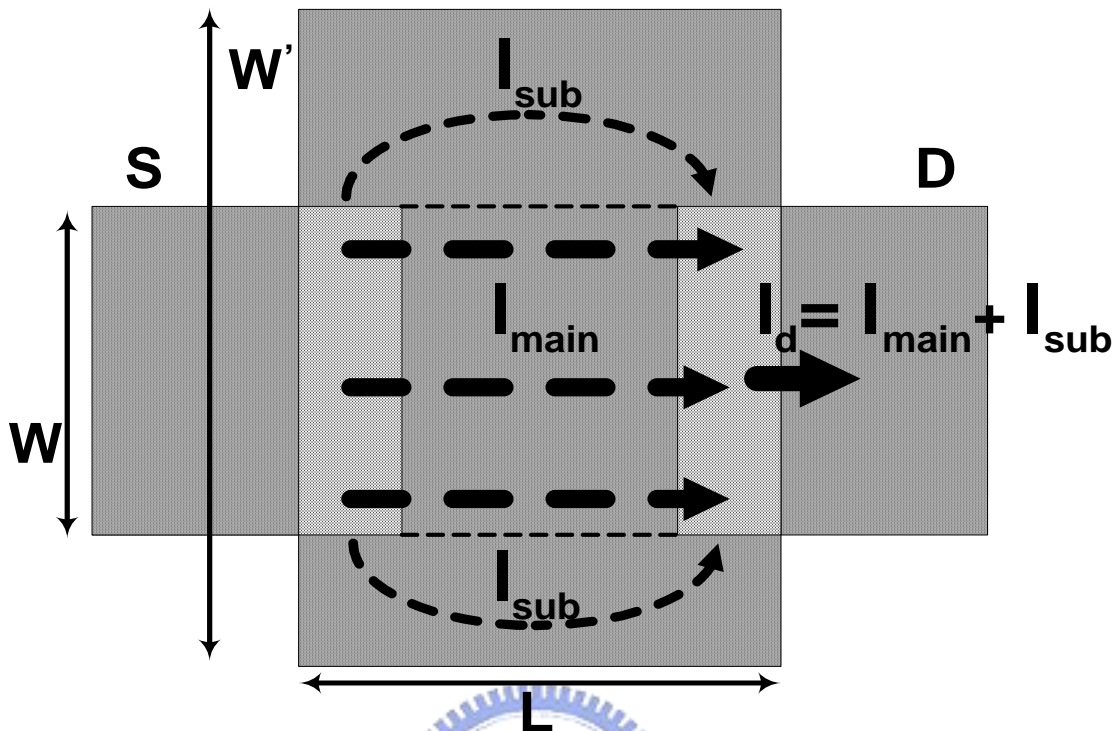


Fig. 3-5 The current transmission mechanism of the novel LTPS TFTs

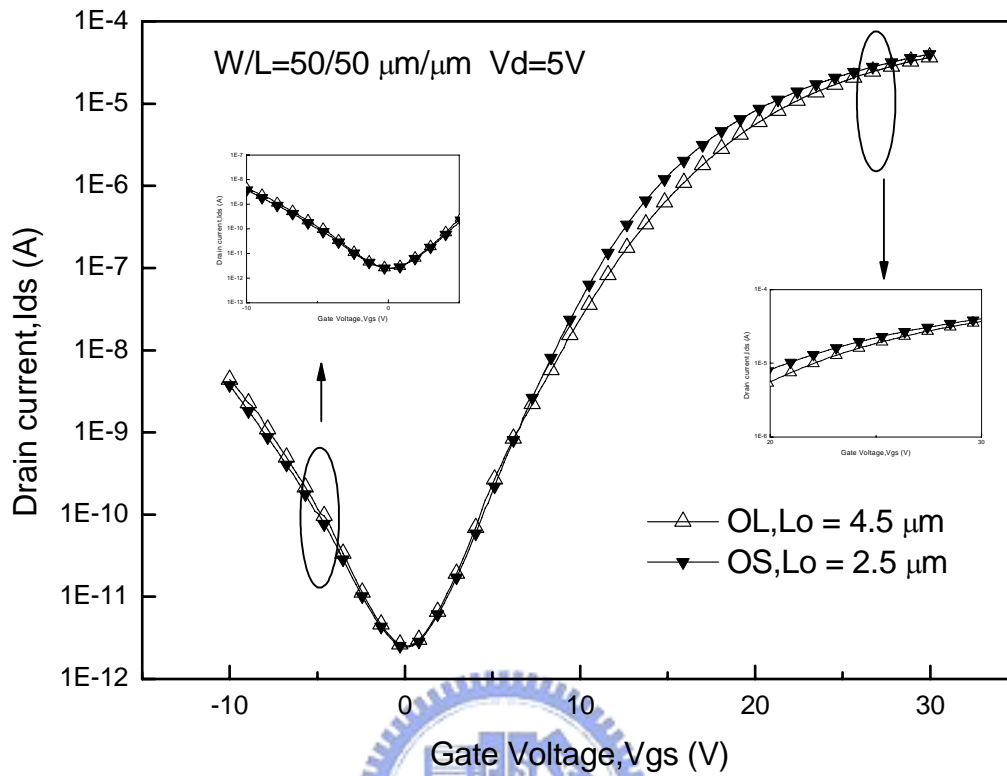


Fig.3-6 (a) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_d=5\text{V}$; $W/L=50/50 \mu\text{m}/\mu\text{m}$

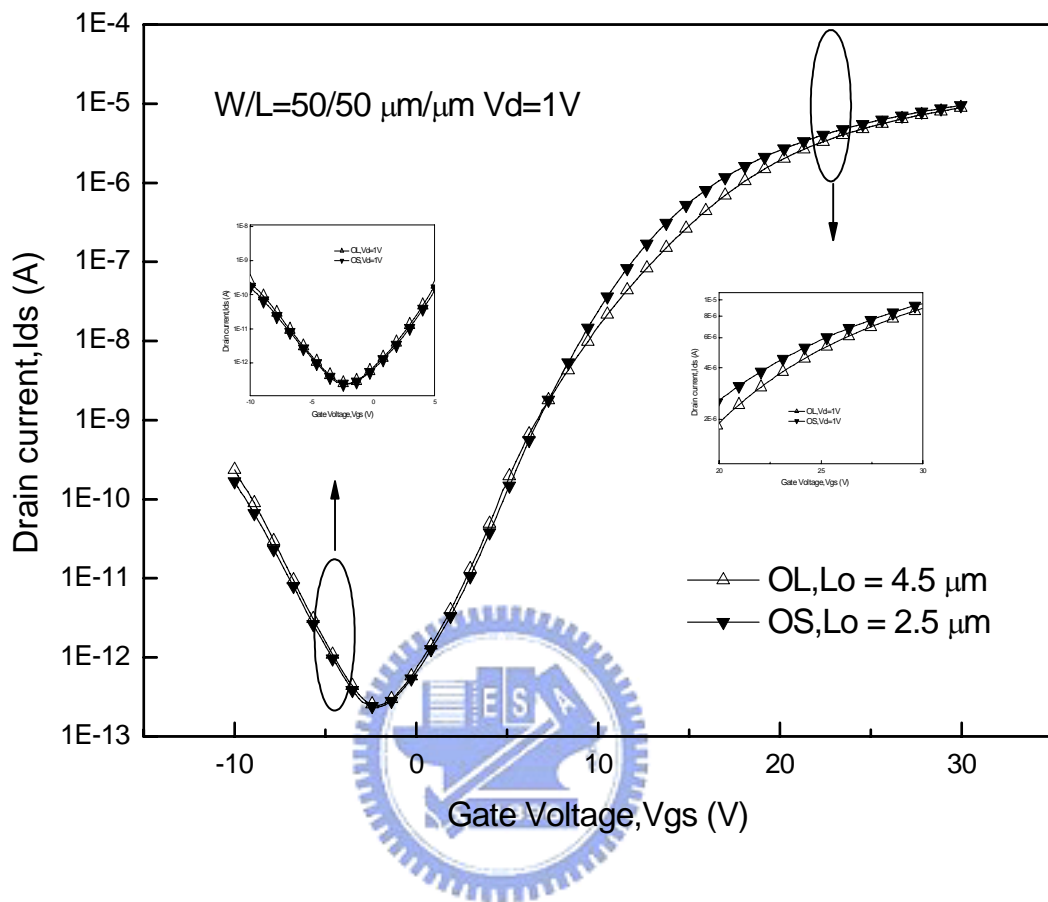


Fig.3-6 (b) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}=1\text{V}$; $W/L=50/50 \mu\text{m}/\mu\text{m}$

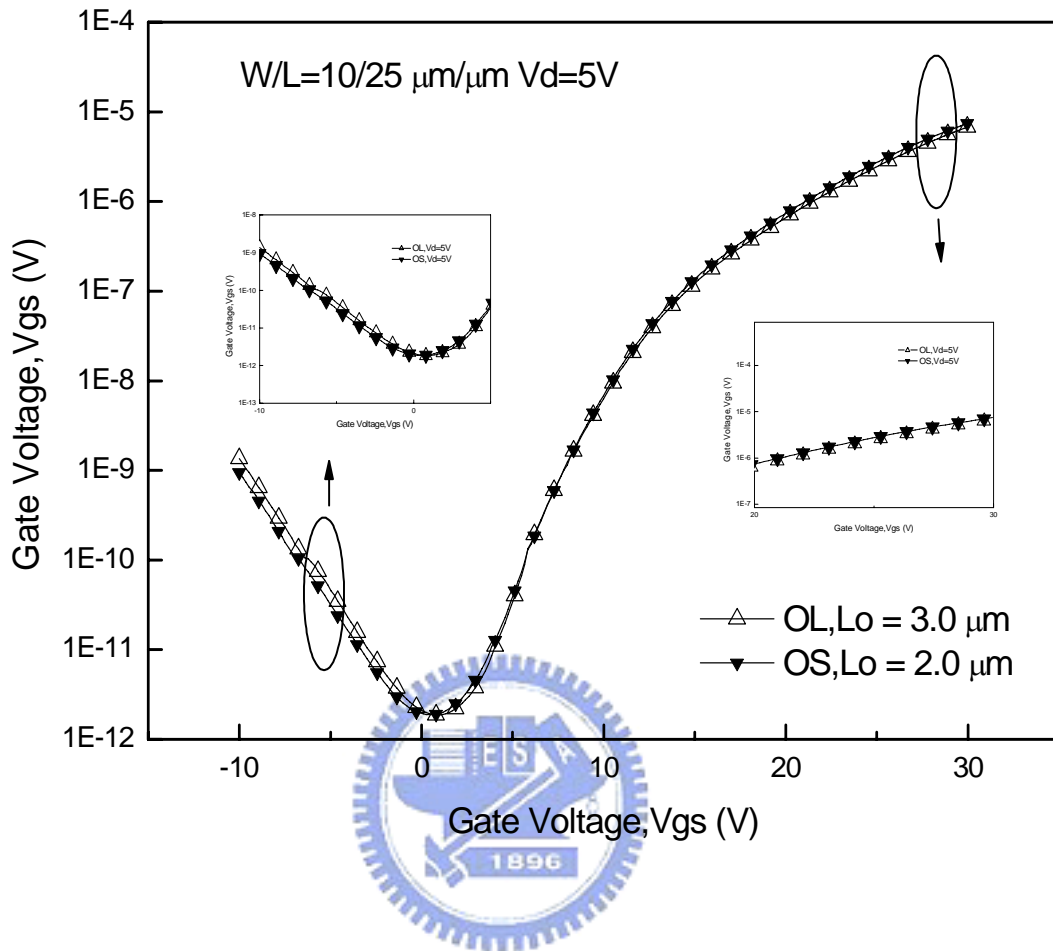


Fig.3-6 (c) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}= 5 \text{ V}$; $W/L= 10/25 \mu\text{m}/\mu\text{m}$

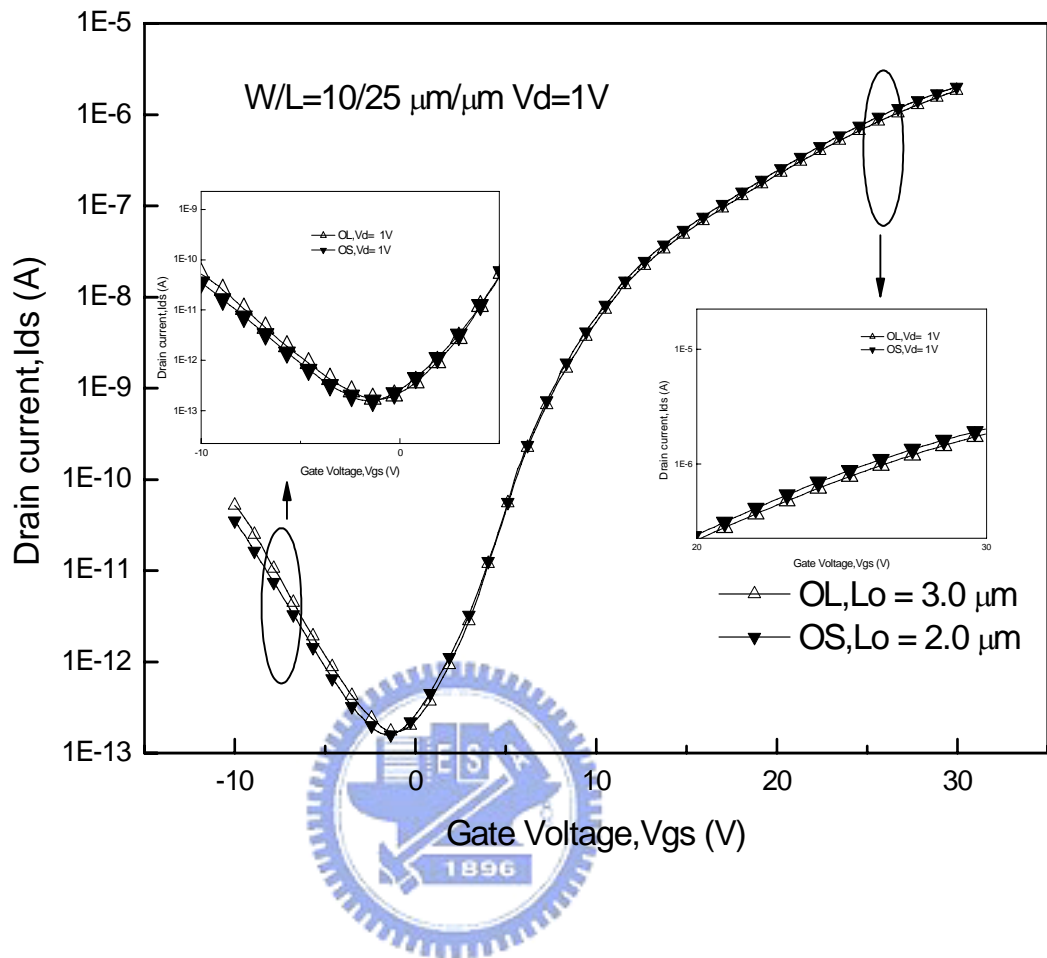


Fig.3-6 (d) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}= 1 \text{ V}$; $W/L= 10/25 \mu\text{m}/\mu\text{m}$

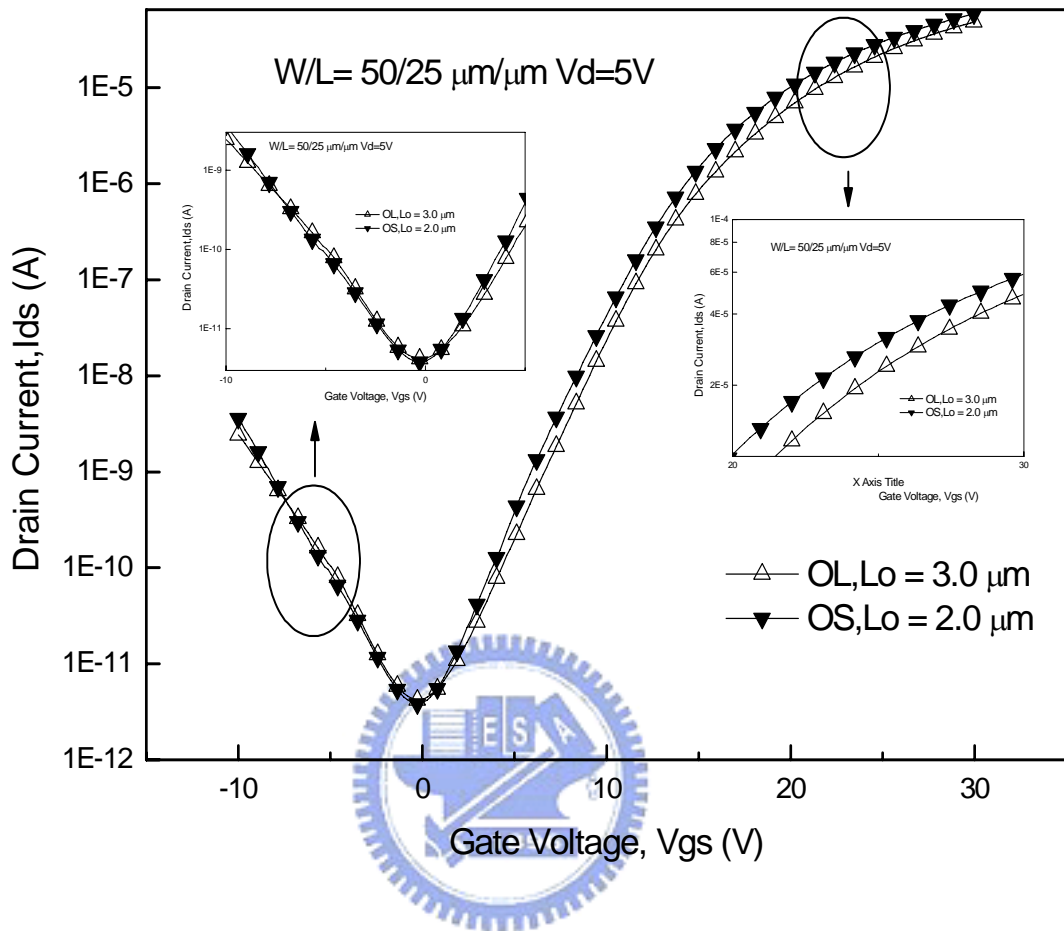


Fig.3-6 (e) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds}= 5 \text{ V}$; $W/L= 50/25 \mu\text{m}/\mu\text{m}$

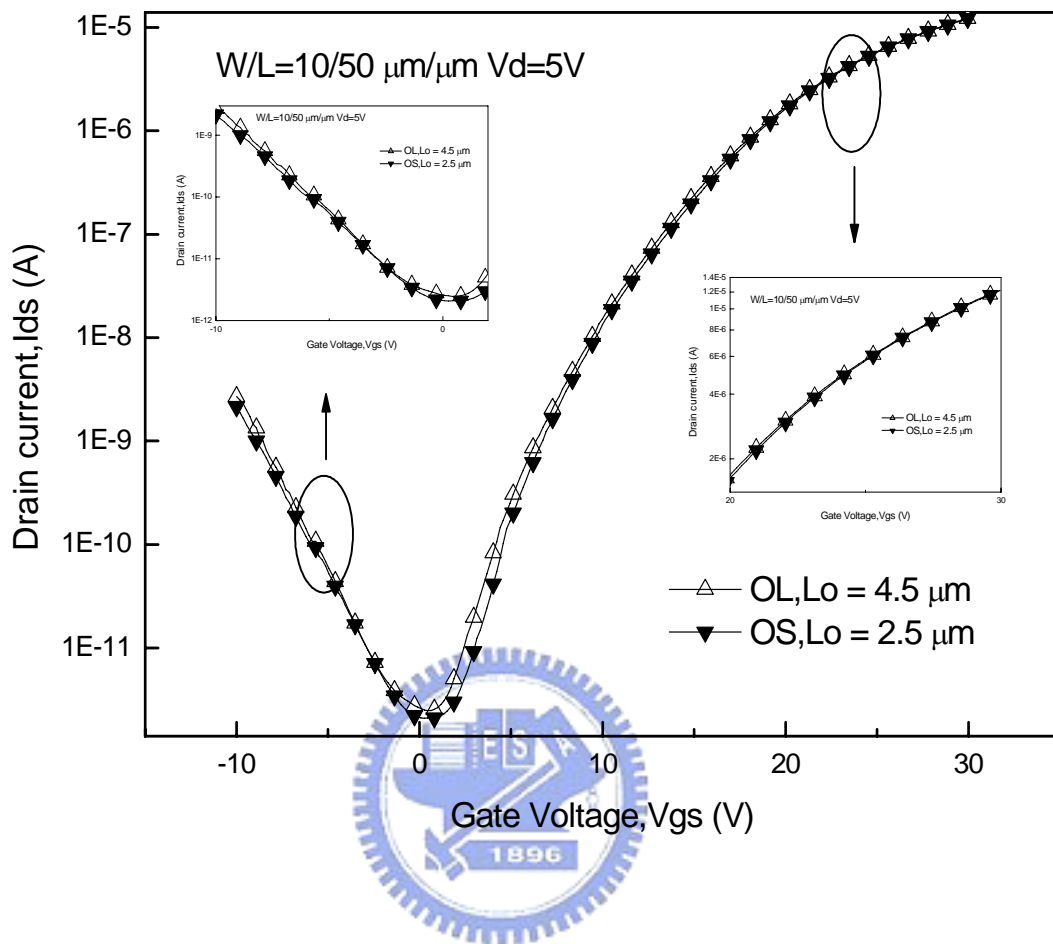


Fig.3-6 (f) I_{ds} - V_{gs} transfer characteristics of the novel LTPS TFTs versus overlapped length for $V_{ds} = 5\text{V}$; $W/L = 10/50 \mu\text{m}/\mu\text{m}$

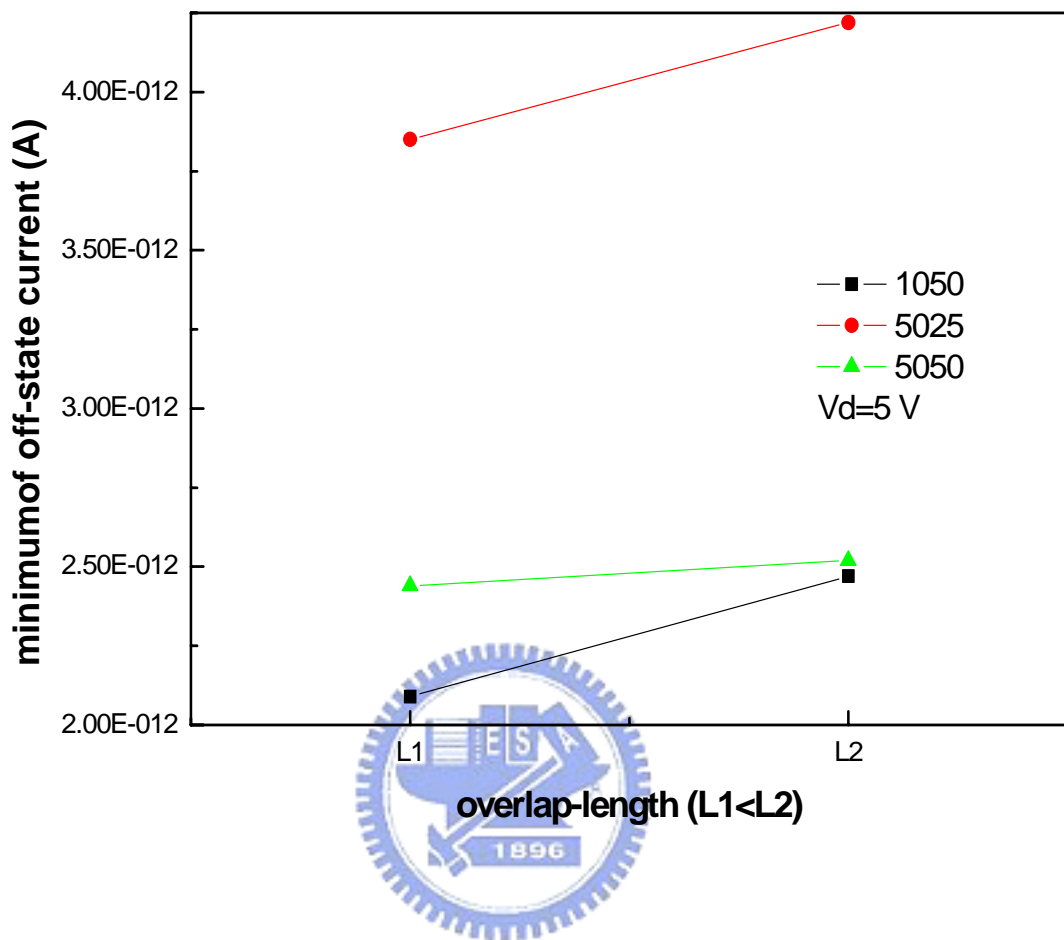


Fig.3-7(a) The minimum off-state current versus the gate overlapped length for different W/L .

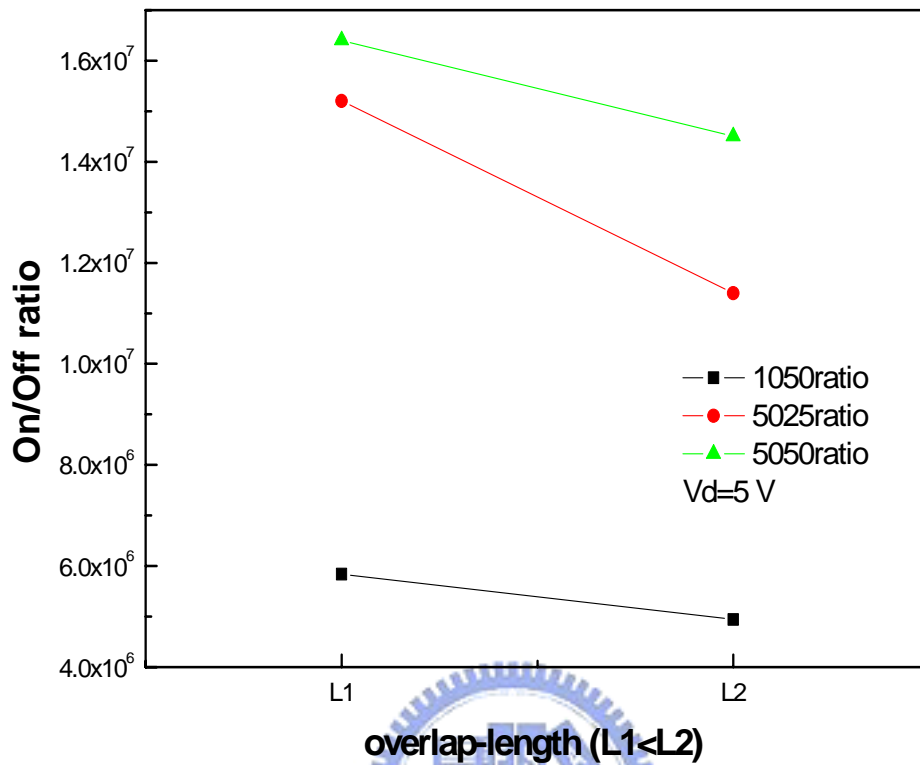


Fig.3-7(b) The On/Off current ratio versus the gate overlapped length for different W/L.

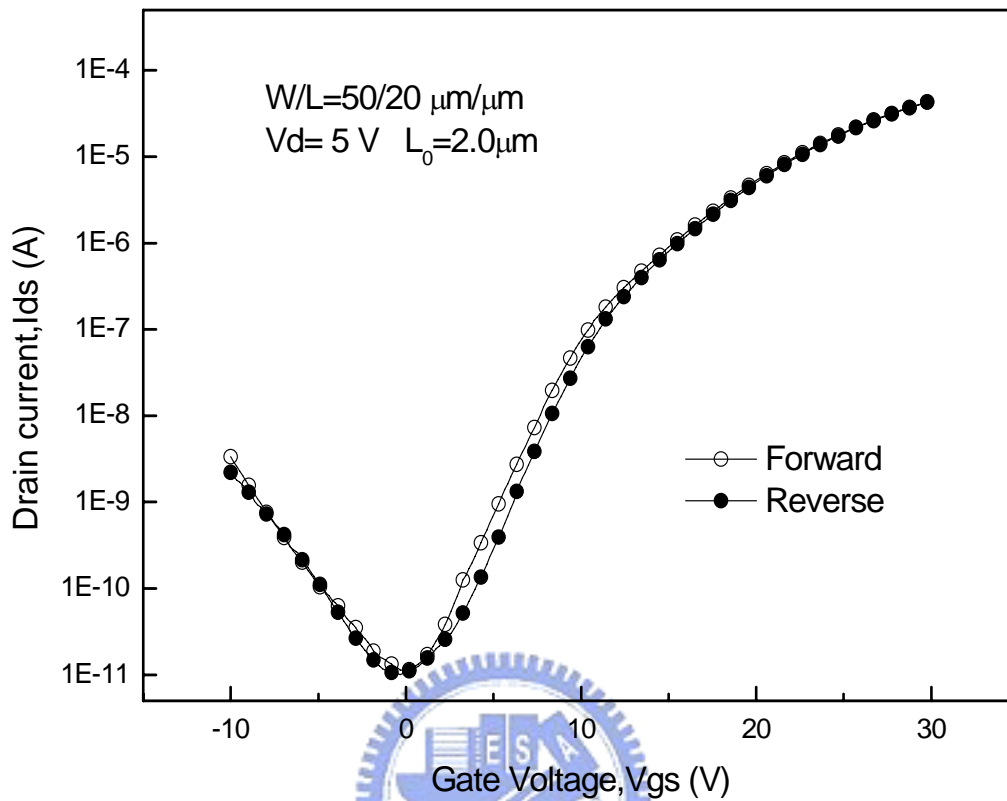


Fig. 3-8(a) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}=5\text{ V}$; $W/L=50/20\ \mu\text{m}/\mu\text{m}$

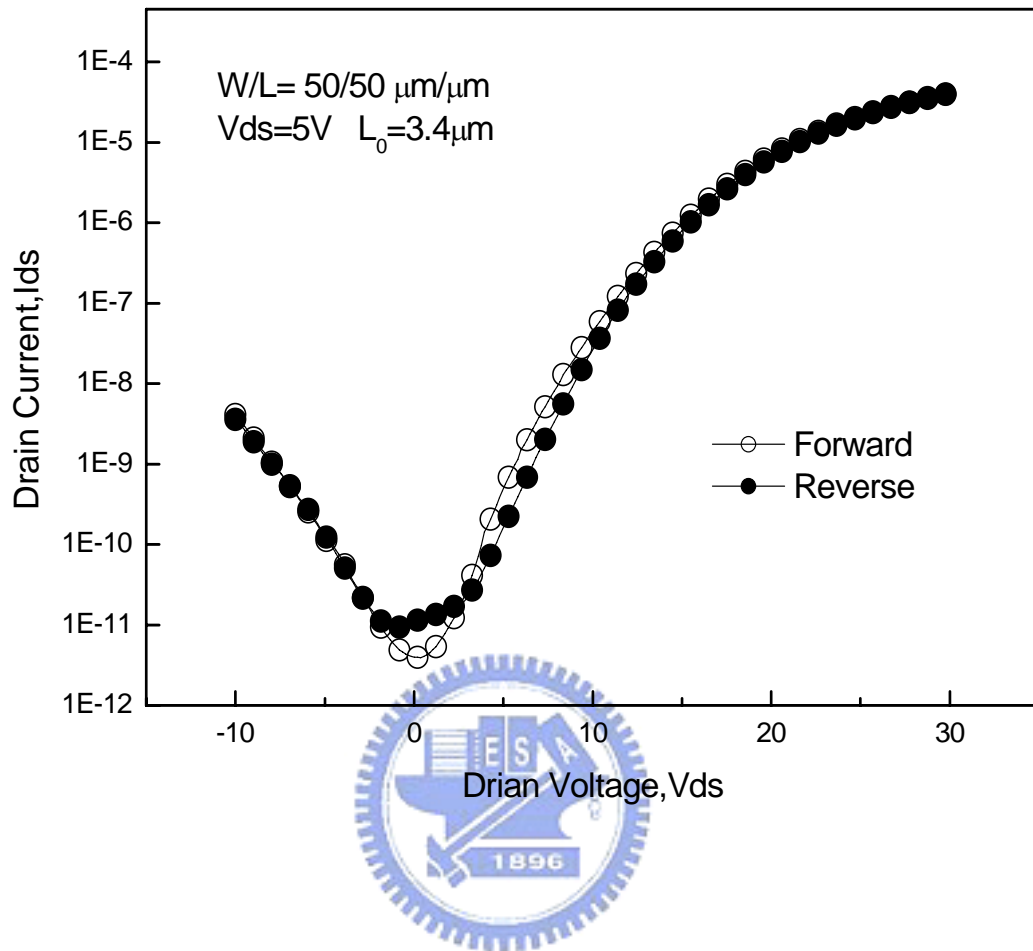


Fig. 3-8(b) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds} = 5\text{ V}$; $W/L = 50/50\ \mu\text{m}/\mu\text{m}$

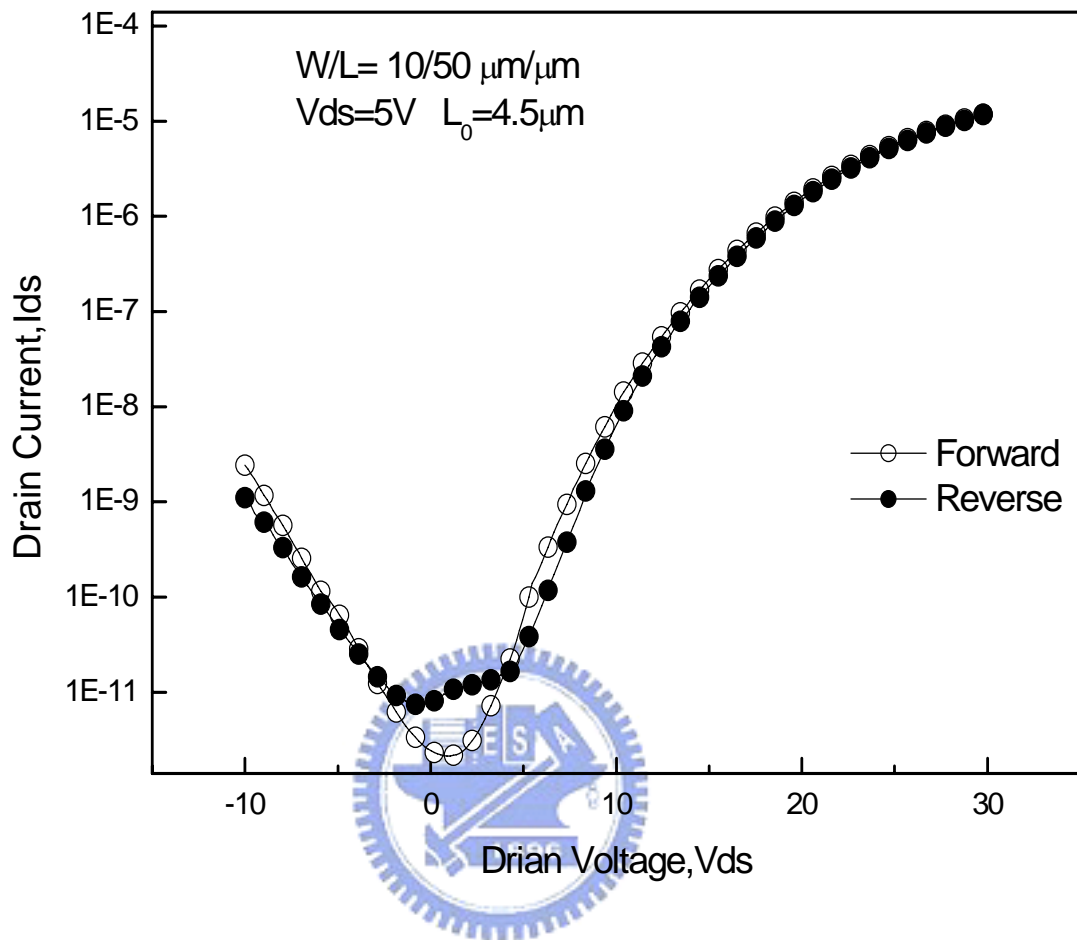


Fig. 3-8(c) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}=5\text{ V}$; $W/L=10/50\ \mu\text{m}/\mu\text{m}$

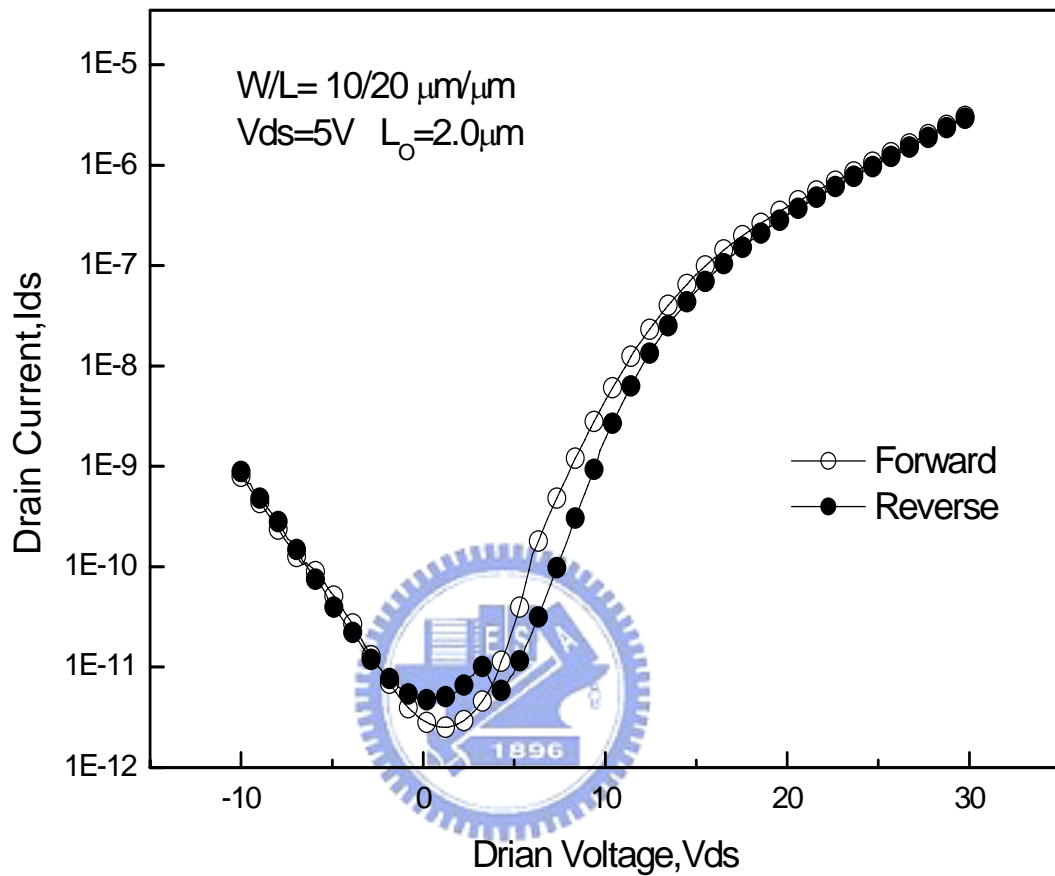


Fig. 3-8(d) The symmetry study of the novel LTPS TFTs in forward and reverse measurement for $V_{ds}=5\text{ V}$; $W/L=10/20\ \mu\text{m}/\mu\text{m}$

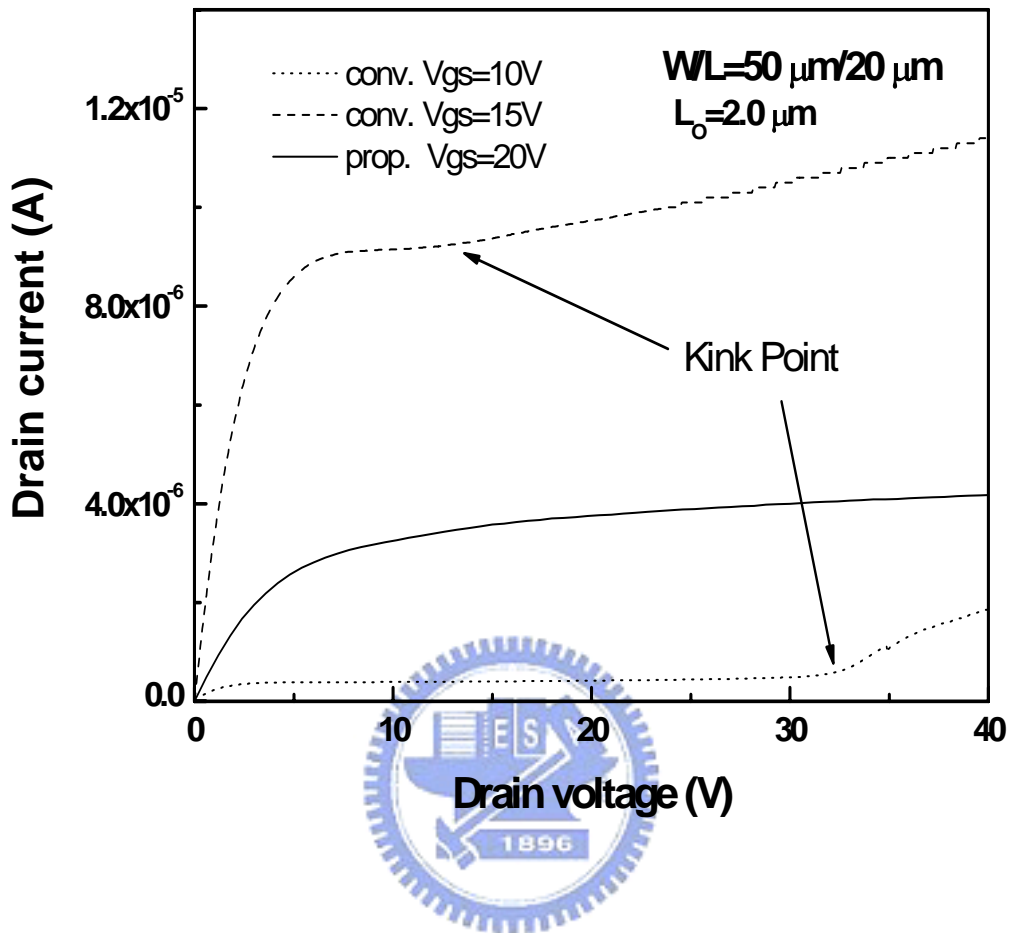


Fig. 3-9(a) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L= 50/20\mu\text{m}/\mu\text{m}$

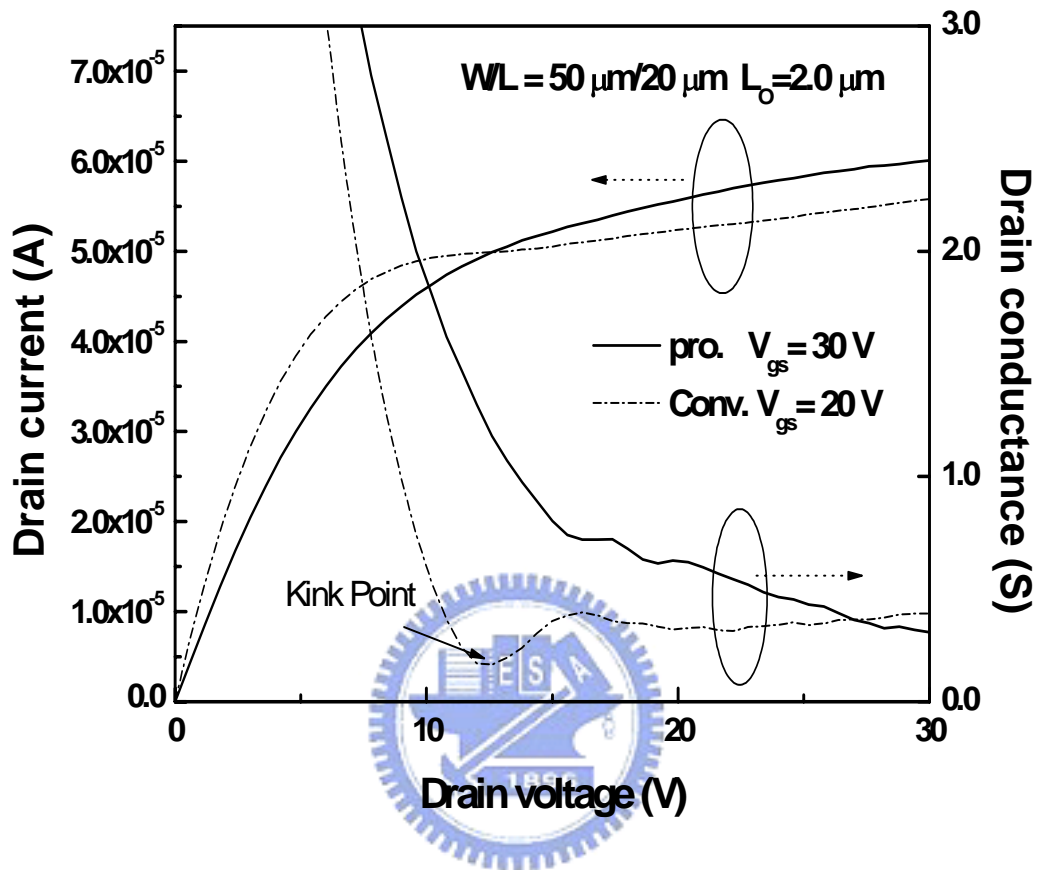


Fig. 3-9(b) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L = 50/20 \mu\text{m}/\mu\text{m}$

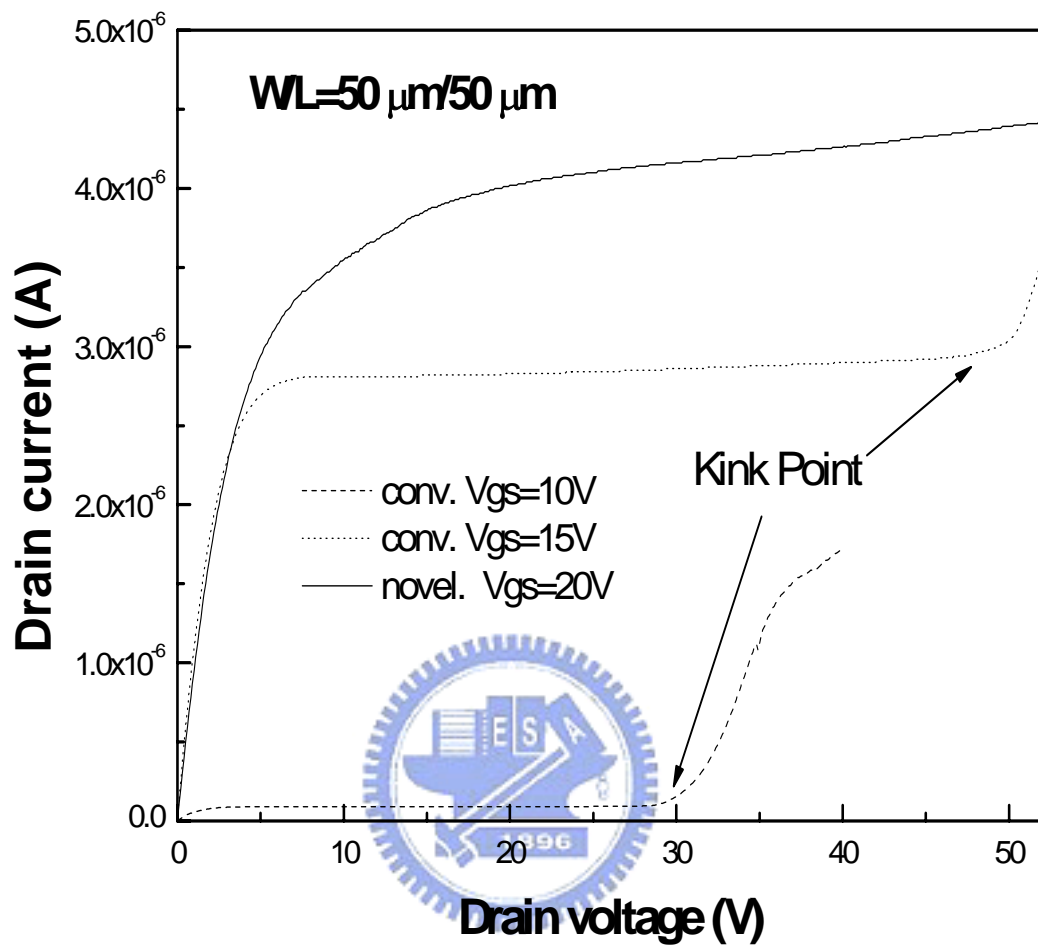


Fig. 3-9(c) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L= 50/50 \mu\text{m}/\mu\text{m}$

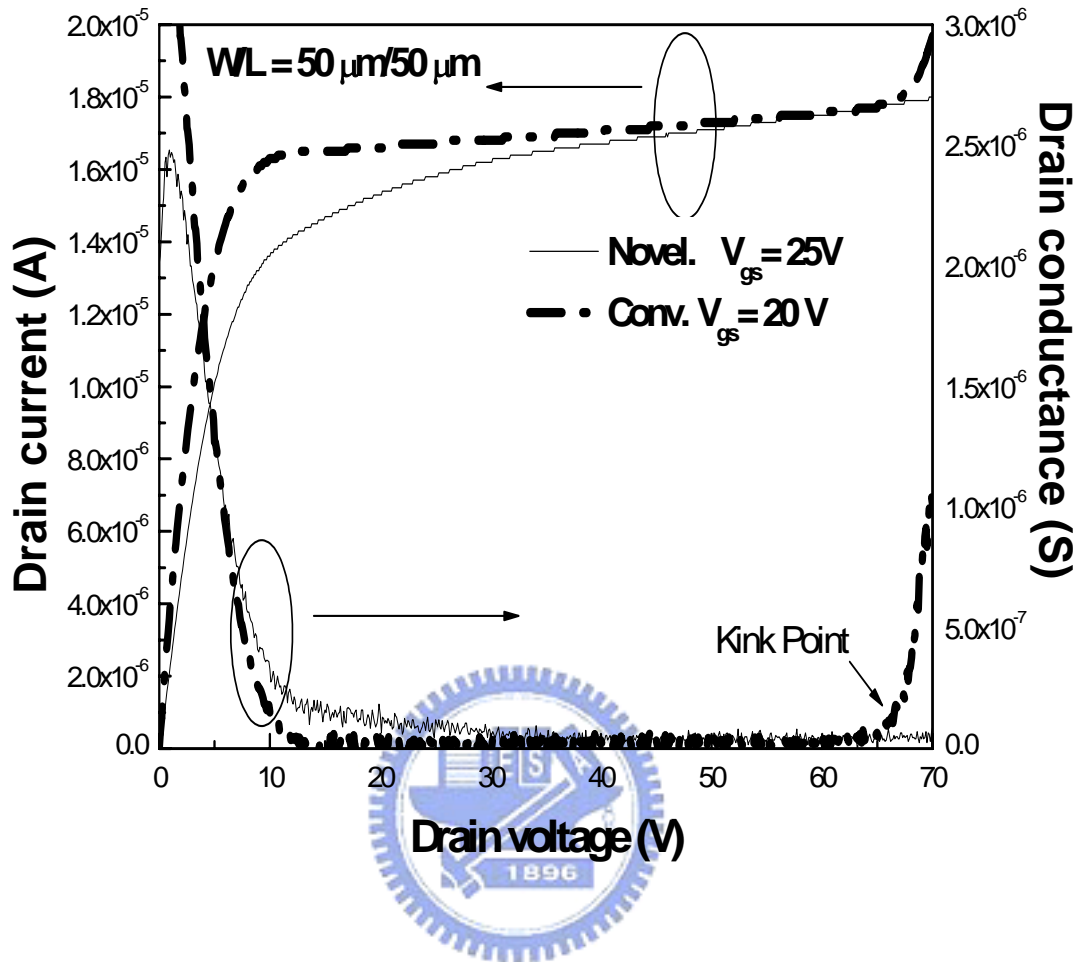


Fig. 3-9(d) I_{ds} - V_{ds} output characteristics of the novel and the conventional TFTs for $W/L = 50/50\mu\text{m}/\mu\text{m}$

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TFTs