Chapter 1

Introduction

The low frequency flicker (1/f) noise is becoming a major concern for continuously scaled down devices, since the 1/f noise increases with the shrinkage of device area. The 1/f noise could lead to serious limitation of the functionality of the analog and digital circuits. The 1/f noise is also of paramount importance in RF circuit applications where it gives rise to phase noise in oscillators or multiplexors [1].

Although the research of low frequency noise started many decades ago, the physically based 1/f noise model for MOSFET is still incapable to predict noise behavior in scaled CMOS [2]. Besides, the noise model developed for large area device based on the large-number-electron averaging theories break down. Since noise has important implications to the reliability and performance of devices, it becomes impossible without accurate models to predict the noise performance of an individual transistor, especially for a small area MOSFET [3]. In small area MOSFETs, the observed noise is basically a single electron phenomenon. It is well known that small area MOSFETs suffer from random telegraph signals (RTS) due to the trapping and detrapping process of a single electron by defects at or near Si-SiO$_2$ interface [4][5]. So, we measure RTS to investigate noise sources in ultra-thin gate oxide MOSFETs with small area.

In addition, the excess noise behavior in PD silicon-On-Insulator (SOI) MOSFETs is also explored. SOI CMOS has emerged as an attractive technology for high-speed, low power, fully integrated RF and mixed-signal circuits. SOI has been shown to exhibit improved performance over bulk-silicon technologies due to decreased parasitic junction capacitance, enhanced drive current, improved

subthreshold slope, and so on [6]. However, the troublesome floating-body effect (FBE) in PD SOI MOSFET's leads to a kink in drain current characteristics as well as some undesirable transient effect. FBE also gives rise to excess low-frequency noise in floating-body PD devices, posing a serious problem for baseband signal processing system [7]-[8].

Chapter 2 deals with the fundamental low frequency noise theory in MOSFET devices. In the beginning, the unified flicker noise model will be reviewed briefly. After that, RTS theory is discussed. Finally, measurement setups of noise power spectrum density and RTS will be shown.

Chapter 3 deals with excess generation/recombination noise mechanism in ultra-thin gate oxide (14Å) n-MOSFETs. First, an abnormal increase of flicker noise is observed in ultra-thin oxide n-MOSFETs. Then, the electron trapping/de-trapping times are measured from RTS traces. Finally, a new generation/recombination noise mechanism based on valence electron tunneling will be proposed to explain the abnormal noise behavior.

Chapter 4 shows the investigation of excess low-frequency noise in ultra-thin oxide n-MOSFETs with floating body. We verify that ultra-thin gate oxide n-MOSFET's with floating body show similar noise behaviors to PD SOI MOSFET's. After that, the impact of soft breakdown location on drain current noise in ultra-thin gate oxide n-MOSFETs is investigated. Finally, we will give a conclusion in chapter 5.

Chapter 2

Fundamentals of Low-Frequency Noise in

MOSFET Devices

2.1 Introduction

At present, Chenming Hu's unified flicker noise model is still the main stream to elucidate the origin of flicker noise. Nevertheless, the model cannot explain clearly the noise source and the noise behaviors in ultra-thin gate oxide MOSFETs where oxide trap density is low. The possibility of the unified flicker noise model breakdown in ultra-thin gate oxide MOSFETs is explored. [3] Random telegraph signal (RTS) noise can explain the noise behaviors in ultra-thin gate oxide MOSFETs with very small area. In the beginning, the unified flicker noise model will be reviewed briefly. After that, RTS theory is discussed. Finally, measurement setups of noise power spectrum density and RTS will be shown.

2.2 Unified Flicker Noise Model

Flicker noise in drain current has a power spectral density proportional to 1/f, so that it is often referred to as 1/f noise. In the past, there is no consensus to the origin of 1/f noise; it is very likely that there exist more than one mechanism giving rise to the same noise characteristics. According to McWhorter's number fluctuation theory [9], 1/f noise is attributed to the trapping and de-trapping processes of the charges in oxide traps close to the $Si\text{-}SiO_2$ interface. Hooge's empirical model [10], however, consider the 1/f noise as a result of carrier mobility fluctuation due to lattice scattering.

More recently, C. Hu proposed a unified noise model. According to his theory, both carrier number fluctuation and mobility fluctuation are possible mechanisms, which lead to the 1/f noise in MOSFET's [11]. The developed noise model incorporates both carrier number fluctuation theory and carrier mobility fluctuations theory as follows:

$$S_{Id}(f) = \frac{kTI_d^2}{rfWL^2} \int_0^L N_t(E_{fn}) \left[\frac{1}{N(x)} \pm \alpha\mu \right]^2 dx \qquad (2.1)$$

where **r** is the attenuation coefficient of the electron wave function in the oxide $N_t(E_{fn})$ is the oxide trap concentration around the Fermi level along the channel   N is the carrier concentration along channel and   is lattice scattering coefficient.

S_{id}/Id^2 is generally used as index of noise, which is in line with the physically based model and has a special meaning in circuit design. It also can be used to analyze the noise behaviors without considering current level.

2.2 Random Telegraph Signal Theory

A discrete switching of the current between two (or more) levels at a constant bias is sometimes observed (Fig. 2.1) [4]. This phenomenon is attributed to a carrier trapping or de-trapping, which is referred to as RTS, and is generally believed to be caused by a single trap or scattering center in the vicinity of the channel of MOSFET devices. Normally, the trap energy level should be within a few kT from the Fermi level to produce noise. k and T are the Boltzmann's constant and equilibrium temperature, respectively. Traps with energy levels several kT below the Fermi level would be permanently filled while traps with energy levels several kT above the Fermi level would be permanently empty, resulting in negligible noise power. A simple two-level RTS is defined by three parameters: the time spent in the high current state τ_H, the time spent in the low current state τ_L and the amplitude ΔI, as illustrated in Fig. 2.1. For the case of Fig. 2.1(a), the RTS has been measured in the
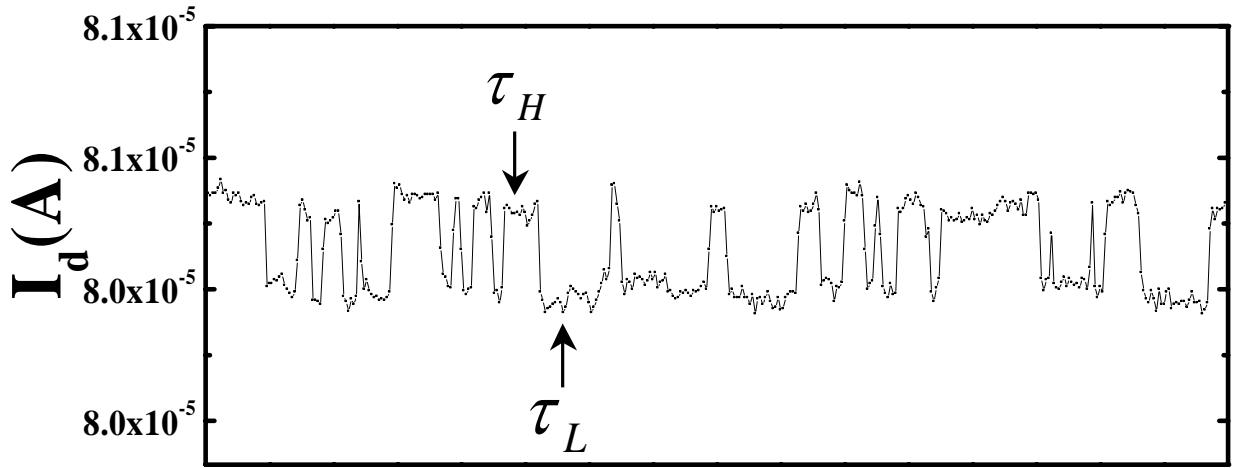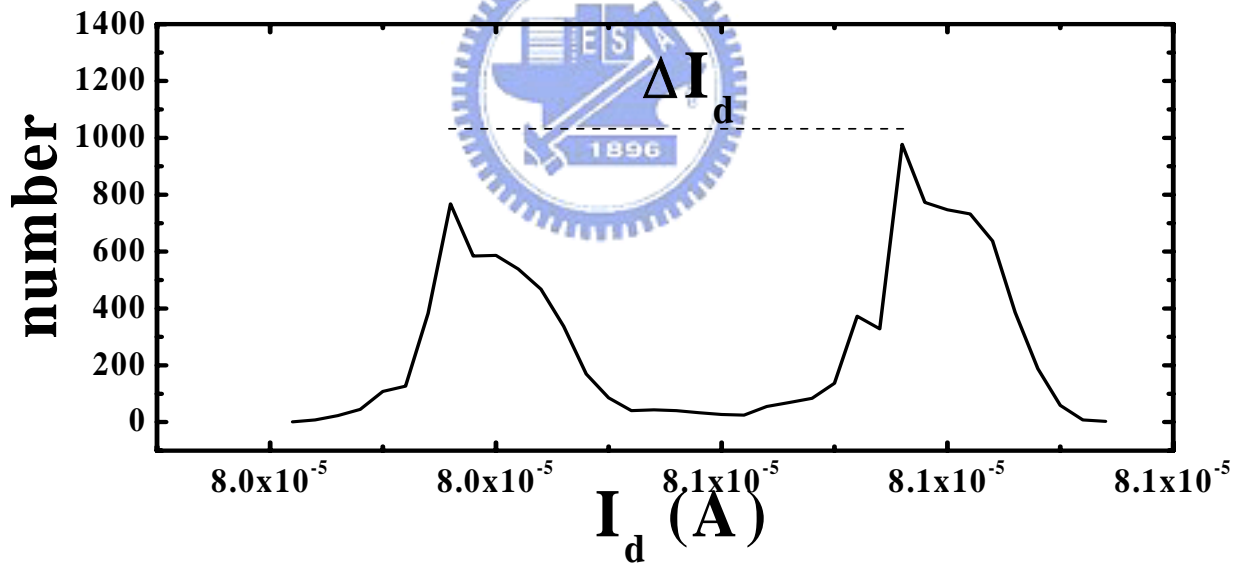
Fig 2.1 (a) Sample RTS in the drain current of a NMOS with W/L=0.32μ m /0.12 μ mV$_g$=0.9V, V$_d$=0.2V. **(b)** the current interval between two max numbers of the drain current can extract Δ I and the two peaks of the drain current can symbolize clearly two-level RTS.

drain current I_d of a small-area that the high and low times follow a Poisson distribution [4][5], given by:

$$p_{H,L}(t) = \frac{1}{\tau_{H,L}}\exp\left(-\frac{t}{\tau_{H,L}}\right)$$

(2.2)

The average values of t_H and t_L are given by τ_H and τ_L, and are defined as high and low time constants. They usually correspond to a trap site empty or occupied, in other words, to the average carrier capture or emission time. Fig. 2.1(b) shows the sampling number versus the drain current, while the total sampling number for a given time is 50000. Moreover, the current interval between the two max numbers of the drain current can be used to extract ΔI and the two peaks of the drain current represents clearly two-level RTS.

The mean time for capturing an electron, τ_c (t_H) follows the Shockley-Read-Hall statistics:

$$\tau_c = \frac{1}{n\upsilon_{th}\sigma}$$

(2.3)

where n is the density of electrons in the vicinity of the trap, υ_{th} is the average thermal velocity of the electrons, and σ is the electron capture cross-section of the trap. The characteristic time for electron emission, τ_e (t_L), depends on the activation energy, ΔE_{ct}, defined as the energy difference between the conduction-band edge and the trap energy level [5]:

$$\tau_e = \frac{\exp(\Delta E_{ct}/kT)}{N_c\upsilon_{th}\sigma}$$

(2.4)

where N_c is the density of states in the conduction band. The capture cross-section can be expressed in terms of barrier energy for capture, ΔE_B, used as a fitting parameter in the model [5]:

$$\sigma = \sigma_0\exp\left(-\frac{\Delta E_B}{kT}\right)$$

(2.5)

where σ_0 is the capture cross-section pre-factor. The activation energy ΔE_B is the lattice energy needed for a crossing of the conduction band with the bound state.

In frequency domain, the noise with two-level RTS switching shows a clear Lorentzian power spectrum, which is characterized by a constant plateau at low frequencies and a $1/f^2$ roll-off at higher frequencies. As an example, the current power spectrum is shown in Fig. 2.2 with a Lorentzian fitting, for the time domain RTS. The current power spectrum density of an RTS can be given by [5][12]:

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_L + \tau_H) \cdot [(1/\tau_L + 1/\tau_H)^2 + (2\pi f)^2]} \tag{2.6}$$

$$\frac{1}{\tau} = \frac{1}{\tau_H} + \frac{1}{\tau_L} \qquad \text{and} \qquad f_c = \frac{1}{2\pi\tau}$$

where f_c is the corner frequency of Lorentzian spectrum corresponding to the 3 dB point of the spectrum. For the uniform interface trap distribution in the band-gap, the sum of each Lorentzian component can yield $1/f$ noise power spectrum.
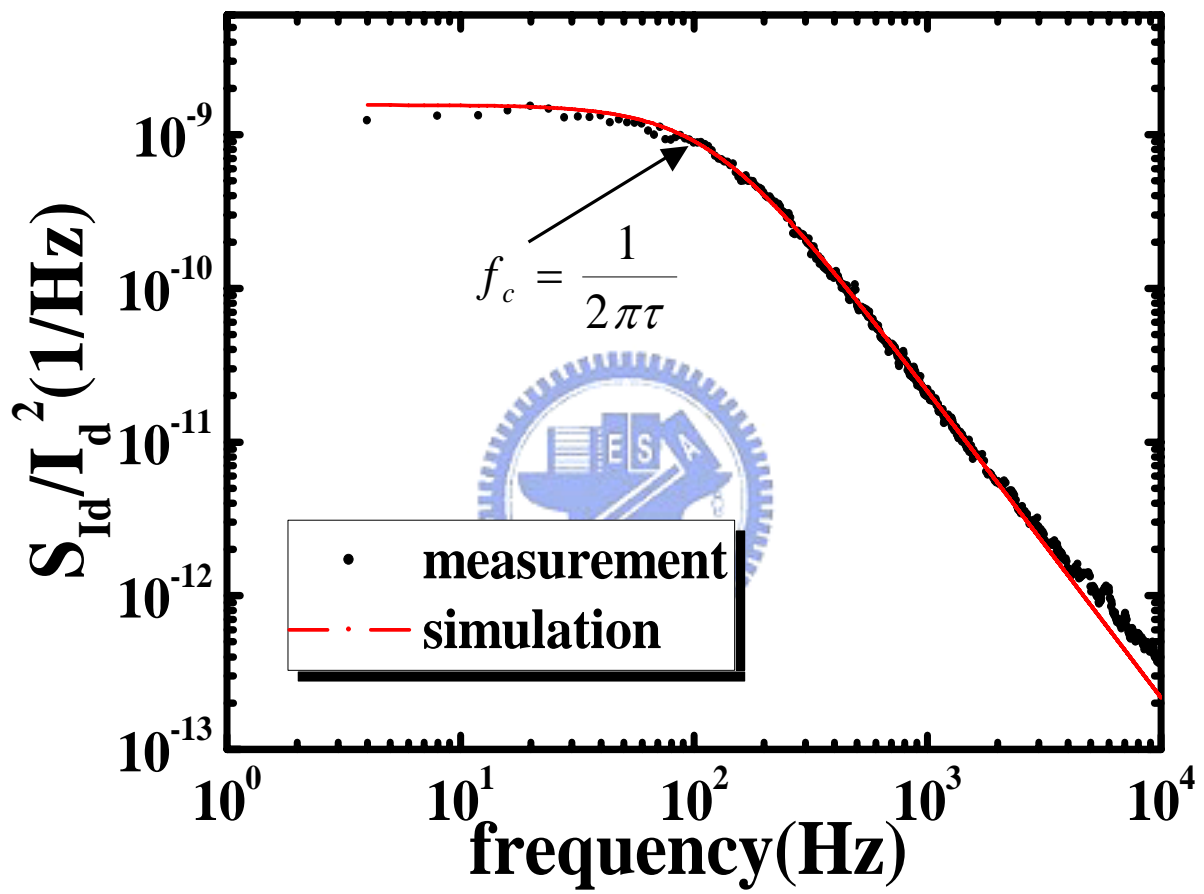
$$f_c = \frac{1}{2\pi\tau}$$

Fig 2.2 Normalized current noise power spectral density for RTS with a Lorentzian fitting.
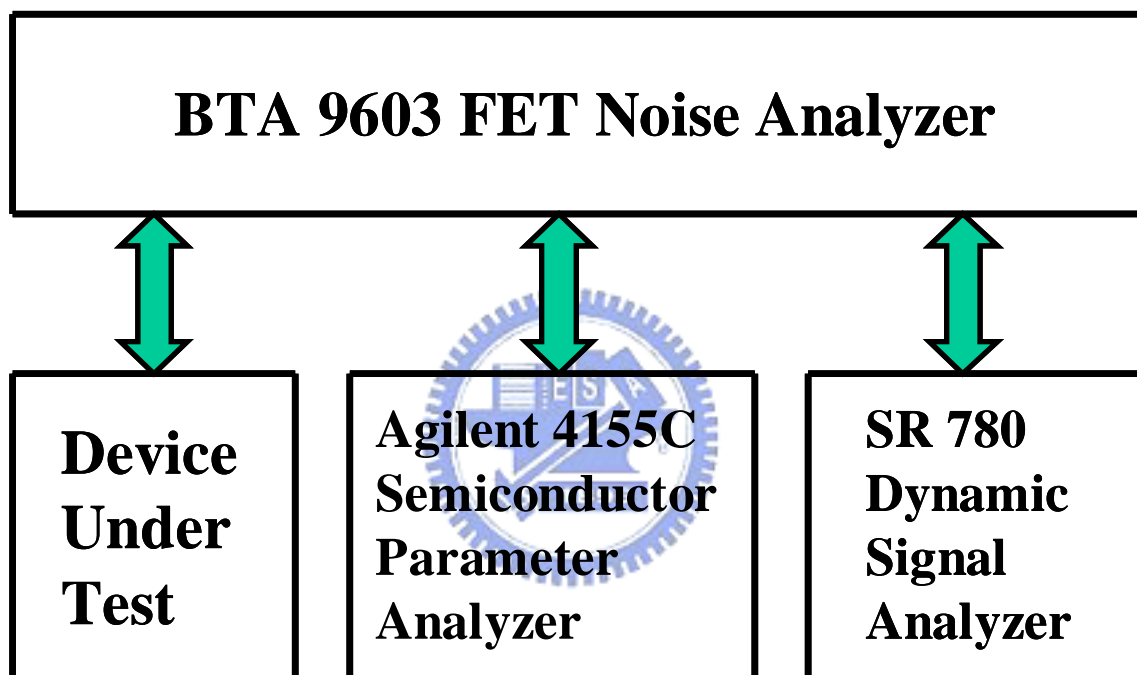
2.3 Measurements of Noise Power Spectrum Density and RTS

2.3.1 Noise Power Spectrum Density Measurement

Low frequency measurement (1Hz-100KHz) can be considered as a practical tool for the evaluation of quality near the Si-SiO$_2$ of MOS devices. A Low-frequency noise measurement setup is shown in Fig. 2.3. The **dc** bias applied to the DUT is supplied by the Berkeley Technology Associate BTA9603 Noise Analyzer, which eliminates the residual noise in the bias voltages generated by Agilent-4155C Semiconductor Parameter Analyzer. The measured device noise is amplified by BTA9603 and then connected to SR780 Network Signal Analyzer for FFT (fast Fourier transform). All measurements are controlled and analyzed automatically through GPIB cards by a computer program named NoisePro.

2.3.2 RTS Measurement

RTS noise is characterized by three parameters: the averages of the high and low time constants and magnitude of the RTS. The range of the time constant is from milli-seconds to seconds. Therefore, a micro-second measurement system is necessary. Fig. 2.4 shows the setup we used for our measurements of small MOSFETs at room temperature. Fig. 2.5 shows the photograph of our micro-second RTS measurement system. The MOSFET bias voltages (**V_D, V_G,** and **V_{SUB}**) are all controlled by Agilent-4155C Semiconductor Parameter Analyzer. The source current is measured with a virtual-ground amplifier, with a 10k   feedback resistor. To obtain a reasonable estimate of high and low times of RTS, a time record containing 100 transitions is stored. Similarly, in order not to miss transitions, the sampling rate must be 50 times the switching rate.

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│        BTA 9603 FET Noise Analyzer                  │
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│           │   │ Agilent 4155C     │   │ SR 780        │
│ Device    │   │ Semiconductor     │   │ Dynamic       │
│ Under     │   │ Parameter         │   │ Signal        │
│ Test      │   │ Analyzer          │   │ Analyzer      │
│           │   │                   │   │               │
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Fig 2.3　A Low-frequency noise measurement setup.
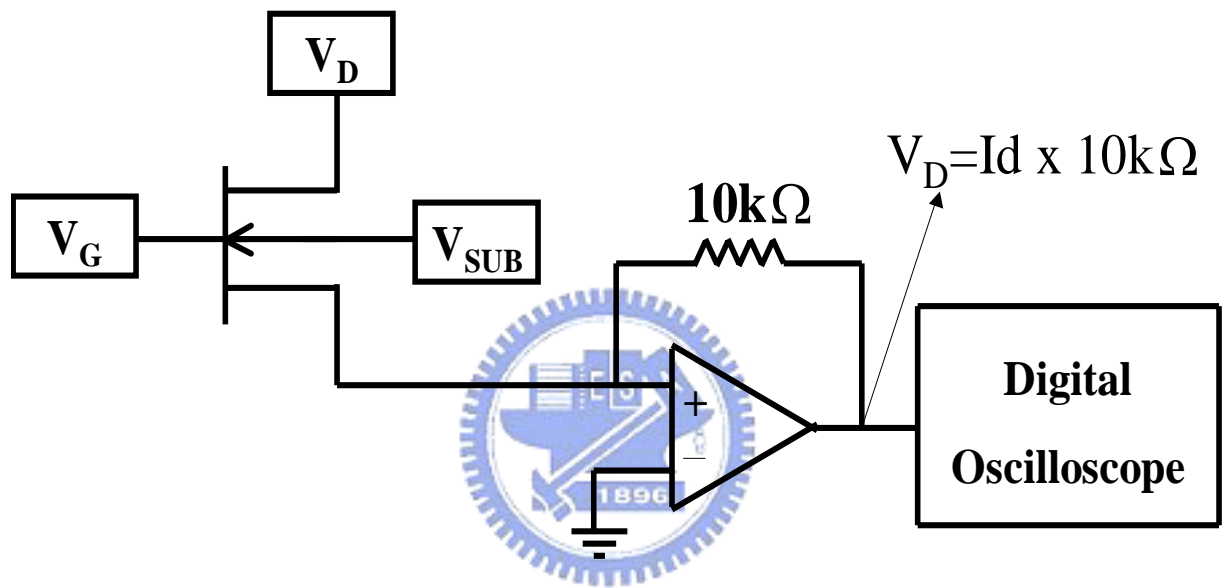
Fig 2.4 Block diagram of experimental setup used for the measurement of RTS in MOSFETs.

Fig 2.5 The photograph of our micro-second measurement system.

Chapter3

Observation of Excess Generation/Recombination Noise in Ultra-Thin Oxide (14Å) n-MOSFETs

3.1 Introduction

The need to understand the noise sources in new generation MOSFETs becomes more and more important in order to design and fabricate devices with acceptable performance characteristics. According to the unified noise model, the low frequency noise in n-MOSFETs under strong inversion condition is attributed to oxide charge tunnel trapping/de-trapping induced channel electron number fluctuation [11]. As the gate oxide thickness is scaled into direct tunneling domain, oxide trap density is much reduced. In addition, channel electrons would likely tunnel through an ultra-thin gate oxide directly without being captured by oxide traps. However, the low frequency noise in ultra-thin oxide CMOS devices still exhibits a noticeable level compared with that in thick oxide ones [13]. Furthermore, some researchers found that the low frequency noise shows an abnormal increase in ultra-thin oxide (15Å) n-MOSFETs [14]. Therefore, this unified flicker model may break down for ultra-thin gate oxide devices [3]. Although noise has important implications to the reliability and performance of the devices, it becomes impossible to predict the noise performance of ultra-thin oxide MOSFETs with the existing model.

In this work, n-MOSFETs with gate oxide thickness from 65Å to 14Å are used. The normalized noise power spectral density (S_{id}/I_d^2) is measured as a monitor of drain current noise, which is considered as a fair index because of the normalization

to the drain current. In addition, the electron trapping/de-trapping times are measured from a RTS in a small area n-MOSFET. Finally, a new generation/recombination noise mechanism based on valence electron tunneling will be proposed to explain the abnormal noise behavior.

3.2 Observation of an abnormal increase of flicker noise

Fig. 3.1 shows the gate oxide thickness (t_{ox}) dependence of the normalized noise power spectral density at f=100Hz. Due to the statistical nature of flicker noise, devices with too small area may exhibit a large fluctuation range in noise [15]. Therefore, the measured devices have a large area (W/L=10μm/1μm) and each noise measurement data point represents an average of 5 devices. The noise is measured in the linear operation region (Vd=0.2V, Vg-overdrive=0.7V) to make sure the carrier distribution along the channel is uniform. As shown in Fig. 3.1, the normalized noise power spectral density decreases as the gate oxide thickness reduces from 65Å to 22Å. This result agrees with the published unified flicker noise model [11] because oxide trap density is reduced in thinner oxides. However, as gate oxide thickness continuously scales down, an abnormal increase in noise level is observed.

Fig. 3.2 shows the normalized noise power spectral density in a small n-MOSFET (W/L=0.16μ m/0.12μ m) with 14 Å gate oxide. The device is biased in the linear region, while the gate overdrive voltage is varied from 0.4 to 0.9 V. The measured noise exhibits obviously a Lorentzian spectrum density as follows:

$$\frac{S_{id}}{I_d^{\,2}} \propto \frac{\tau}{1 + (2\pi f \tau)^2} \tag{3.1}$$

The Lorentzian spectral density was generally attributed to the single electron trapping/de-trapping. In Fig. 3.3(a), the gate overdrive voltage dependence of the normalized noise power spectral density at f=100Hz is shown. It is interesting to note
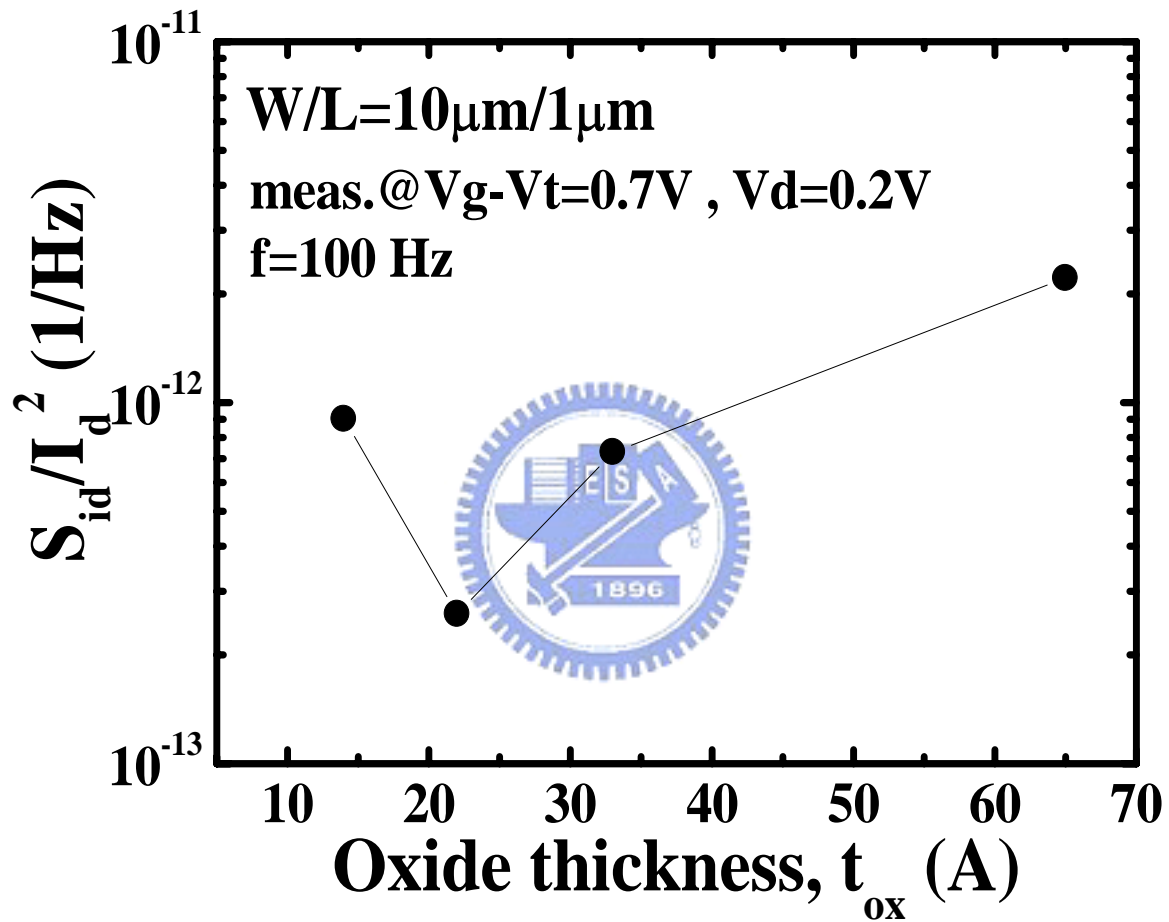
Fig. 3.1 Normalized noise power spectral density (measured at Vd=0.2V, Vg-overdrive=0.7V, f=100Hz) versus gate oxide thickness in n-MOSFETs. There is an abnormal increase in noise level for the 14Å gate oxide device.
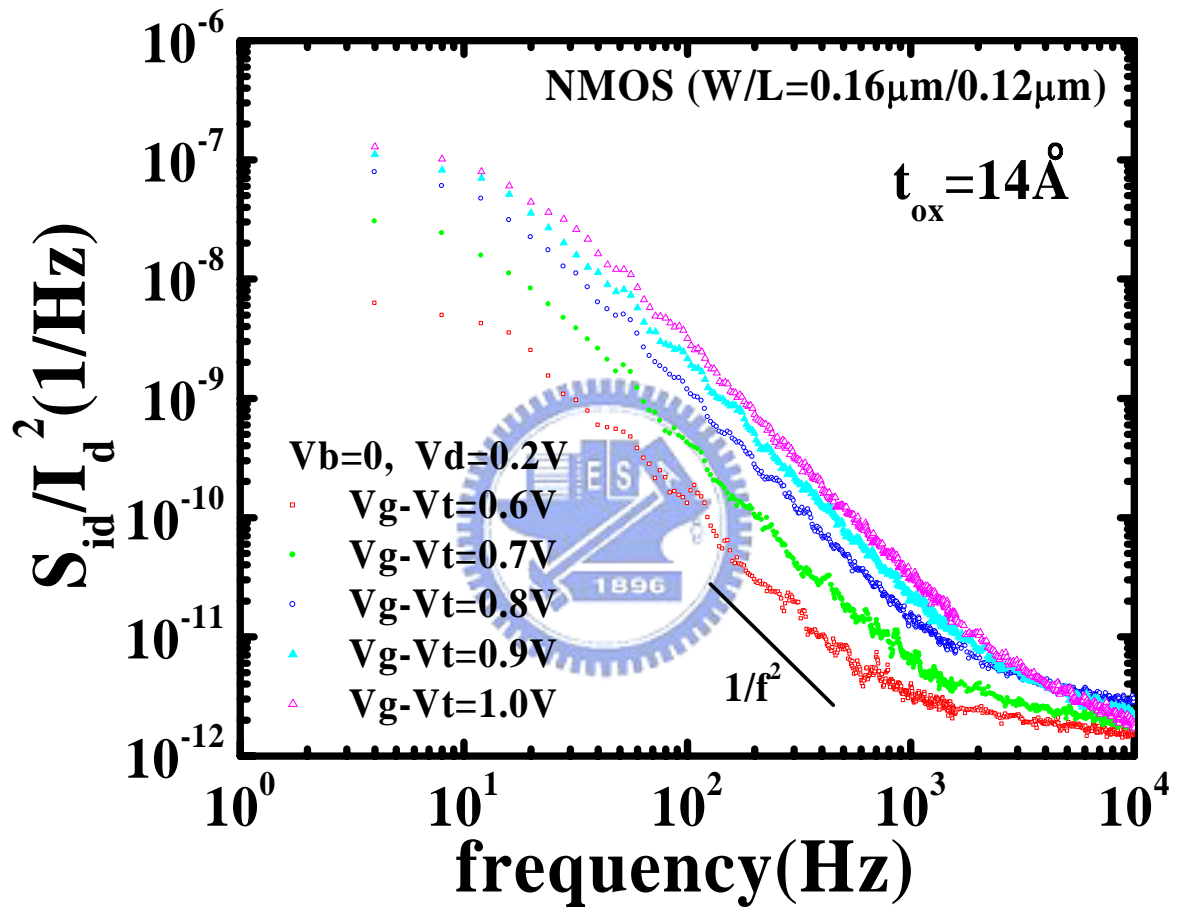
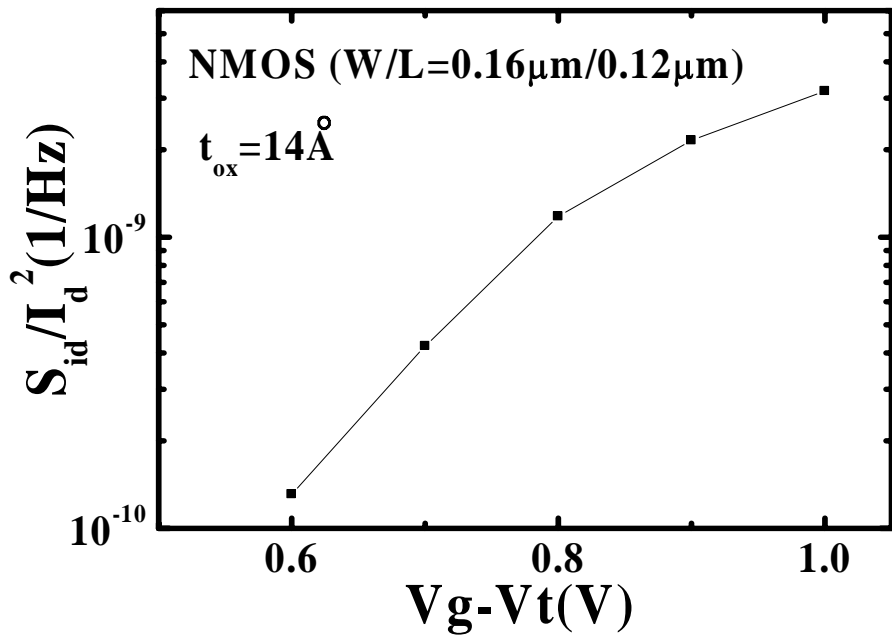**Fig. 3.2** Lorentzian power spectral density with the Vg-overdrive in a small n-MOSFET with 14 Å gate oxide

that normalized noise power spectral density shows an abnormal increase in ultra-thin gate oxide (14Å) n-MOSFET. The unified noise model based on large number of electron averaging theory cannot explain such a noise behavior. In order to explore the origin of the abnormal noise increase, we measure the normalized noise power density in a small n-MOSFET (W/L=0.16μ m/0.24μ m) with 65 Å gate oxide, as shown in Fig. 3.3 (b). The device was also biased in the linear region, while the gate overdrive voltage was varied from 0.5 to 1.7 V. The higher gate overdrive voltage is, the smaller the normalized noise power spectral density is. This trend consists with the published unified flicker noise model because electron number fluctuation decreases with gate voltage, thus causing a lower S_{id}/I_d^2.

In order to investigate the abnormal noise source in the 14Å gate oxide n-MOSFETs, the temperature dependence of the noise characteristic in a small area device (W/L=0.36μm/0.12μm) with a single trap is analyzed. Fig. 3.4(a) shows the temperature dependence of S_{id}/I_d^2 versus frequency. The temperature varies from 25℃ to 125℃. We can distinguish easily that the time constant $\tau = 1/2\pi f_c$ has strong temperature dependence. More clearly, the temperature dependence of τ is noticed in Fig. 3.4(a) where the individual normalized spectral density times the frequency $((S_{id}/I_d^2)*f)$ versus frequency is plotted in Fig. 3.4(b) using the same data as in Fig. 3.4(a). Obviously, as temperature increases, the trap time constant decreases, resulting in a higher corner frequency. According to the Shockley-Read-Hall theory, the carrier capture time (τ) can be described by

$$\tau = \frac{1}{N\sigma_0 \upsilon_{th}} \cdot \exp\left(\frac{\Delta E_b}{kT}\right) \tag{3.2}$$

where E_b is the energy barrier for the capture of a carrier and **N** is the carrier density in the vicinity of the trap. σ_o is the pre-factor of the capture cross-section. The linear behavior of the Arrhenius plot shown in Fig. 3.5 reveals that the source of the.
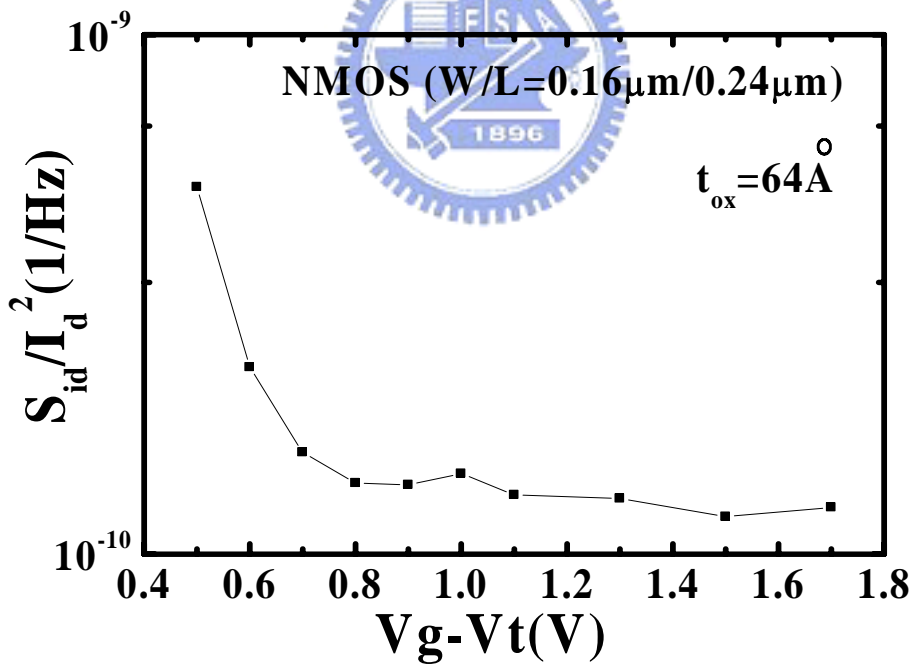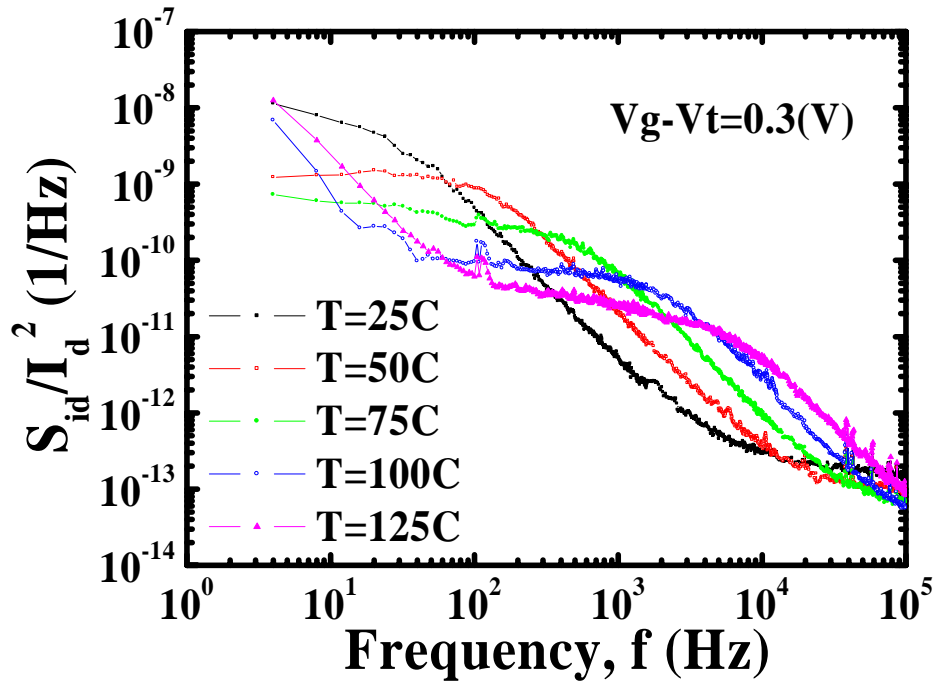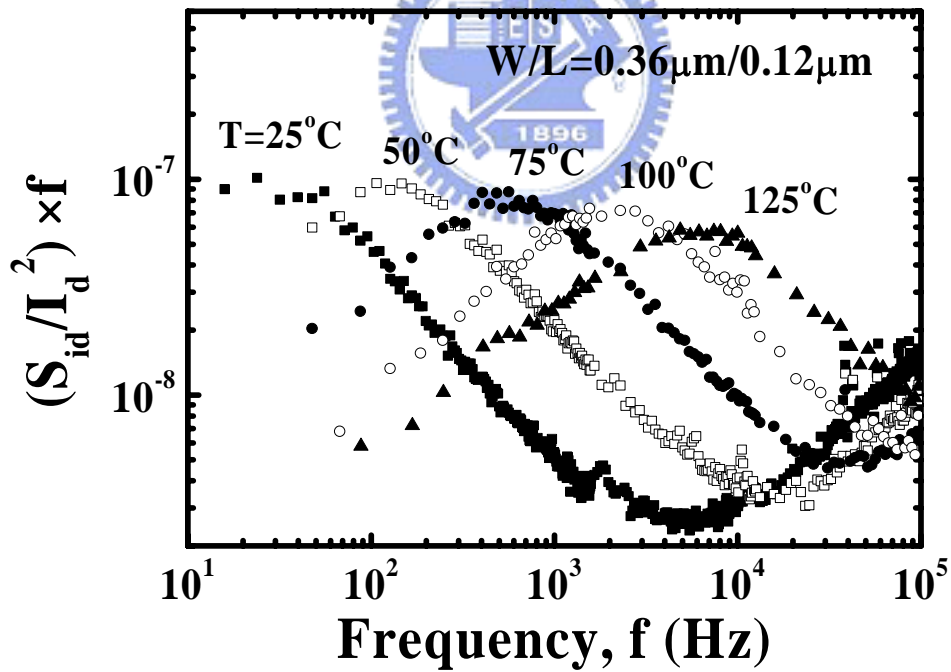
Fig. 3.3 Normalized noise power spectral density versus Vg-overdrive at f=100Hz in small n-MOSFETs with **(a)14** Å gate oxide **(b) 64** Å gate oxide
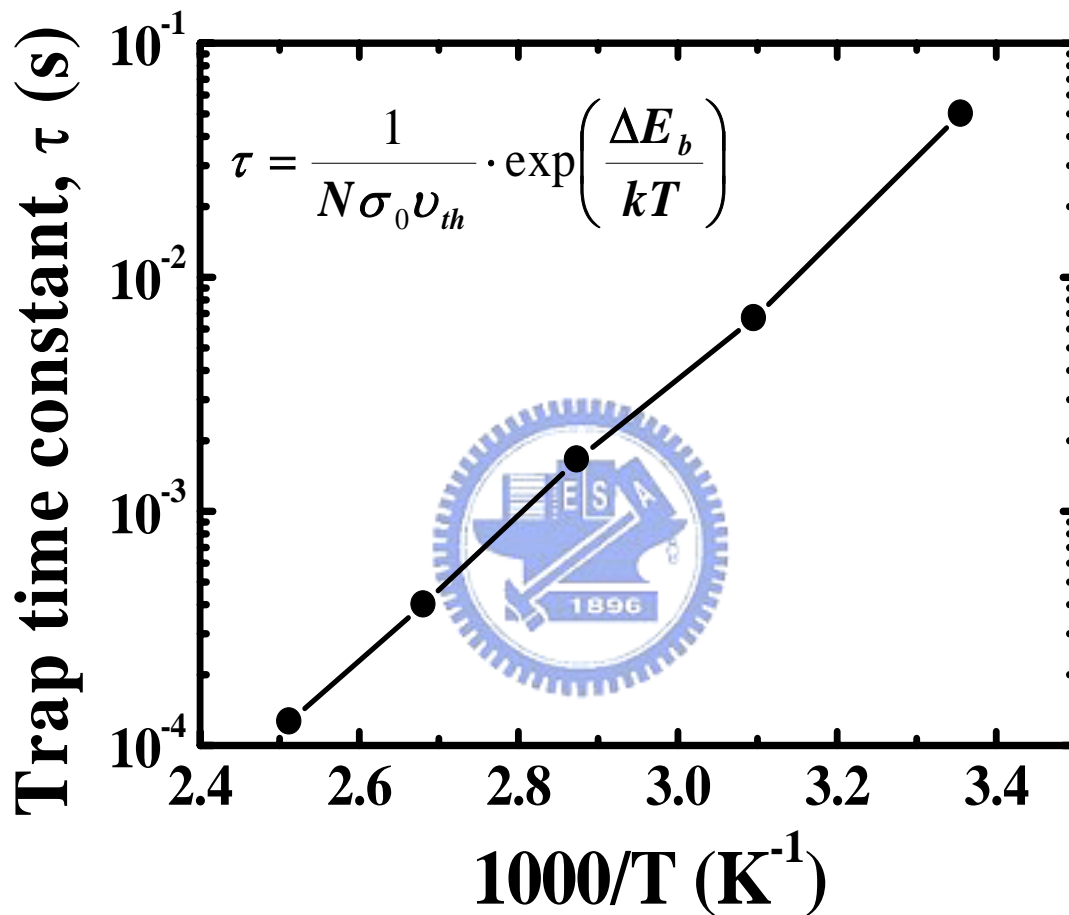
Fig. 3.4 (a) Temperature dependence for the Lorentzian noise in a small area nMOSFET with an oxide thickness of 14Å **(b)** Temperature dependence for $((S_{id}/I_d^2)*f)$

Fig. 3.5 Arrhenius plot of τ versus 1000/T. The carrier capture time (τ) according to the Shockly-Read-Hall theory is also shown. The linear behavior of the Arrhenius plot reveals that the source of the noise is related to carrier capture/emission by an interface trap.

noise is related to carrier capture/emission by an interface trap.

3.2   Analysis of RTS Noise Behavior

In Fig. 3.6, two Lorentzian spectrums in a small n-MOSFET (W/L=0.16μ m/0.12μ m) with 14 Å gate oxide are measured at low gate bias and high gate bias. A decrease in the plateau level and an increase in the corner frequency are observed as operation gate bias increases from low to high. The Lorentzian spectrum is associated with a single trapping center that has a unique RTS noise signature. So, the characteristic time constant of RTS is short in weak inversion region and long in strong inversion region, as can be predicted from Fig. 3.6.

Therefore, the corresponding RTS in a small area device is characterized. In Fig. 3.7, a RTS in a small n-MOSFET (W/L=0.16μ m/0.12μ m) with 14 Å gate oxide is measured in weak inversion region (Vg=0.65 V   0.7 V   0.8 V   0.9 V) with a time interval of 20ms. In contrast, RTS in the strong inversion region (Vg=1.1 V   1.2 V   1.4 V   1.6 V) was also measured (Fig. 3.8) with a time interval of 5s. Under different operation region, the associated time constants are quite different. Moreover, Fig. 3.7 shows that as the gate bias increases, the time in the high-current state is decreased drastically, while the time in the low-current state is increased. However, it is interesting to note that the trend of the time in the weak inversion region is opposite to the trend of the time in the strong inversion region. That is, Fig. 3.8 shows that as the gate bias increases, the time in the high-current state is increased, while the time in the low-current state is opposite.

The measured RTS exhibits two levels. The upper level corresponds to an empty interface trap, i.e., no electron occupation, and the duration of time is denoted by τ_H. The lower level corresponds to an electron occupied trap and its duration is denoted
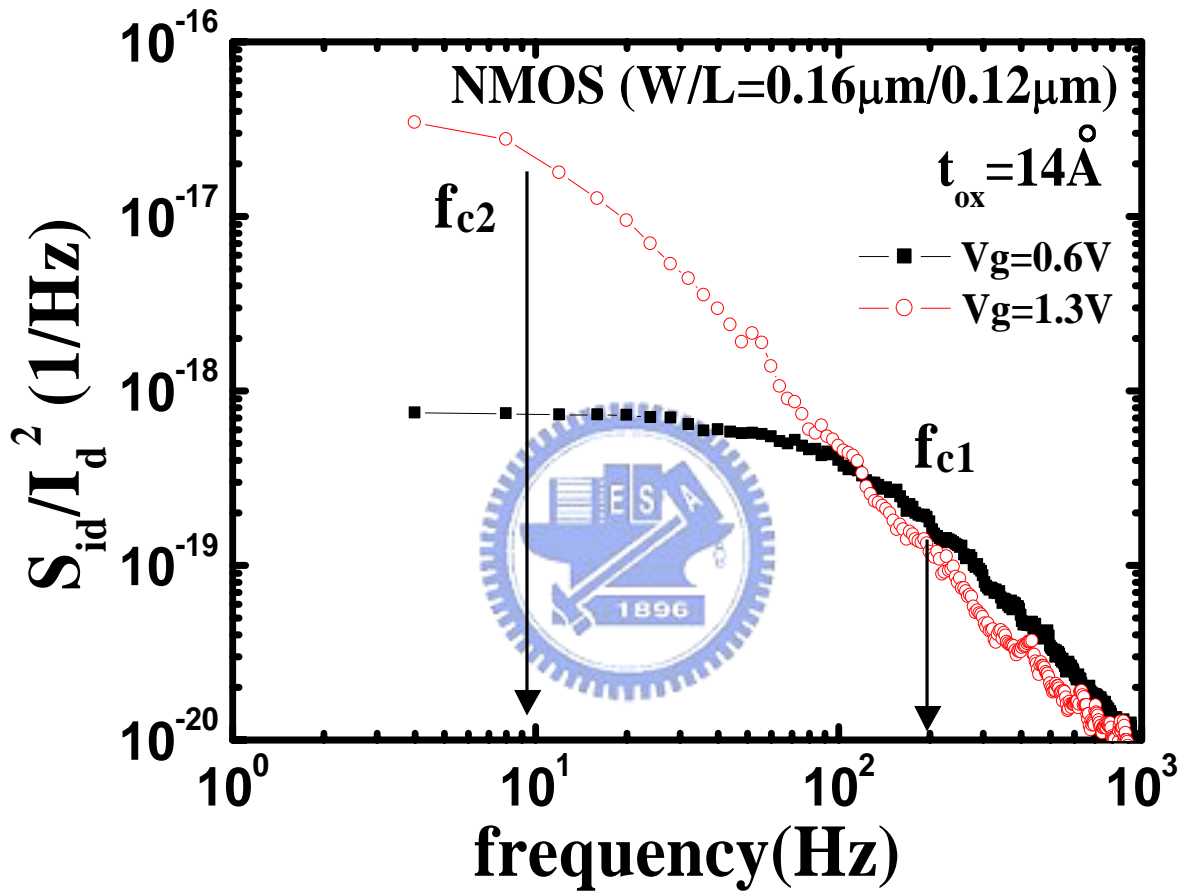
Fig. 3.6 Measured Lorentzian noise power spectral density characteristics of a small area n-MOSFET for two gate voltages (Vg=0.6V, 1.3V). The corner frequency (f_c), which reflects the trap time constant (τ), changes to a lower value as the Vg increases.
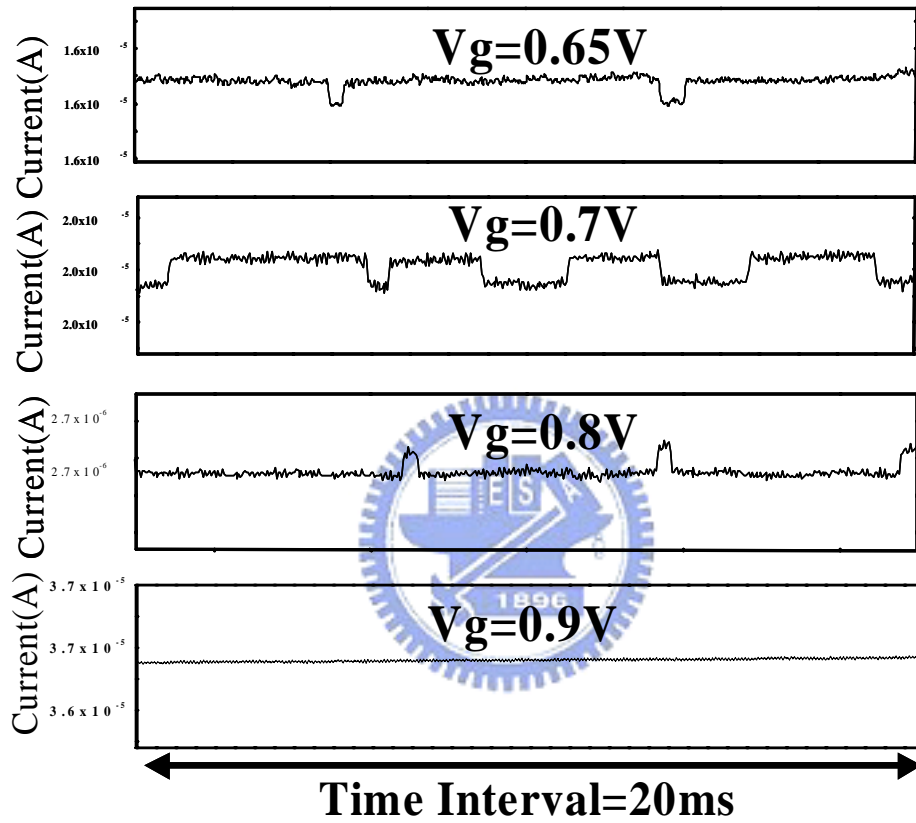
Fig. 3.7 RTS in a small n-MOSFET (W/L=0.16μ m/0.12μ m) with 14 Å gate oxide is measured in the weak inversion region (Vg=0.65 V 0.7 V 0.8 V 0.9 V) at the time interval = 20(ms) .
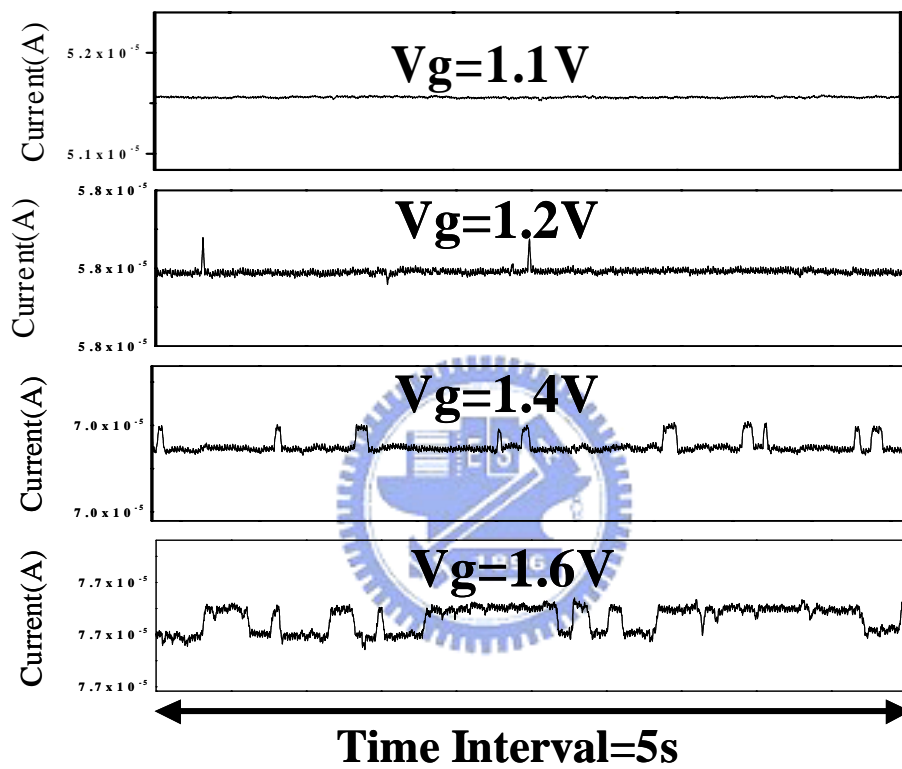
Fig. 3.8 RTS in a small n-MOSFET (W/L=0.16μ m/0.12μ m) with 14 Å gate oxide is measured in the strong inversion region (Vg=1.1V   1.2 V 1.4 V   1.6 V) at the time interval = 5(s).

by τ_L. Fig. 3.9 shows the gate bias dependence of average τ_H and τ_L in weak inversion.Fig. 3.10 shows the gate bias dependence of average τ_H and τ_L in strong inversion. Note that the gate bias dependence of time constant in strong inversion is opposite to that in weak inversion. In order to realize the unusual phenomenon, the electron occupation factor of the interface trap (f_t) is evaluated as $f_t= \tau_L/(\tau_L + \tau_H)$ shown in Fig. 3.11. Without gate oxide tunneling, as the gate bias is increased, the trap occupancy should increase and f_t should show an increase. Nevertheless, it is interesting to note that f_t decreases as Vg increases in strong inversion region. In other words, at a larger Vg, although the energy level of the interface trap moves deeper with respect to the electron Fermi level, the chance of the trap being occupied by an electron becomes smaller. The gate bias dependence of the normalized noise power density in a small n-MOSFET (W/L=0.16μ m/0.12μ m) with 14 Å gate oxide is measured at f=100Hz, as shown in Fig. 3.12. We can observe clearly that there are two peaks that are in line with the f_t behavior as the gate is biased from the weak inversion region to strong inversion region. The noise level has maximum values at Vg=0.7V and 1.5V.

3.4　A New G-R Noise Mechanism

An abnormal increase of the flicker noise in ultra-thin oxide n-MOSFETs is observed in strong inversion condition. The traditional flicker noise model of oxide charge tunnel trapping/de-trapping cannot account for the observed noise behavior. The possible explanation is illustrated in Fig. 3.13. To investigate the correlation between the abnormal noise increase and valence band tunneling, the valence band tunneling current is measured in n-MOSFETs with 14 Å gate oxide, as shown in Fig. 3.13(a). The substrate current with grounded drain and source is contributed by
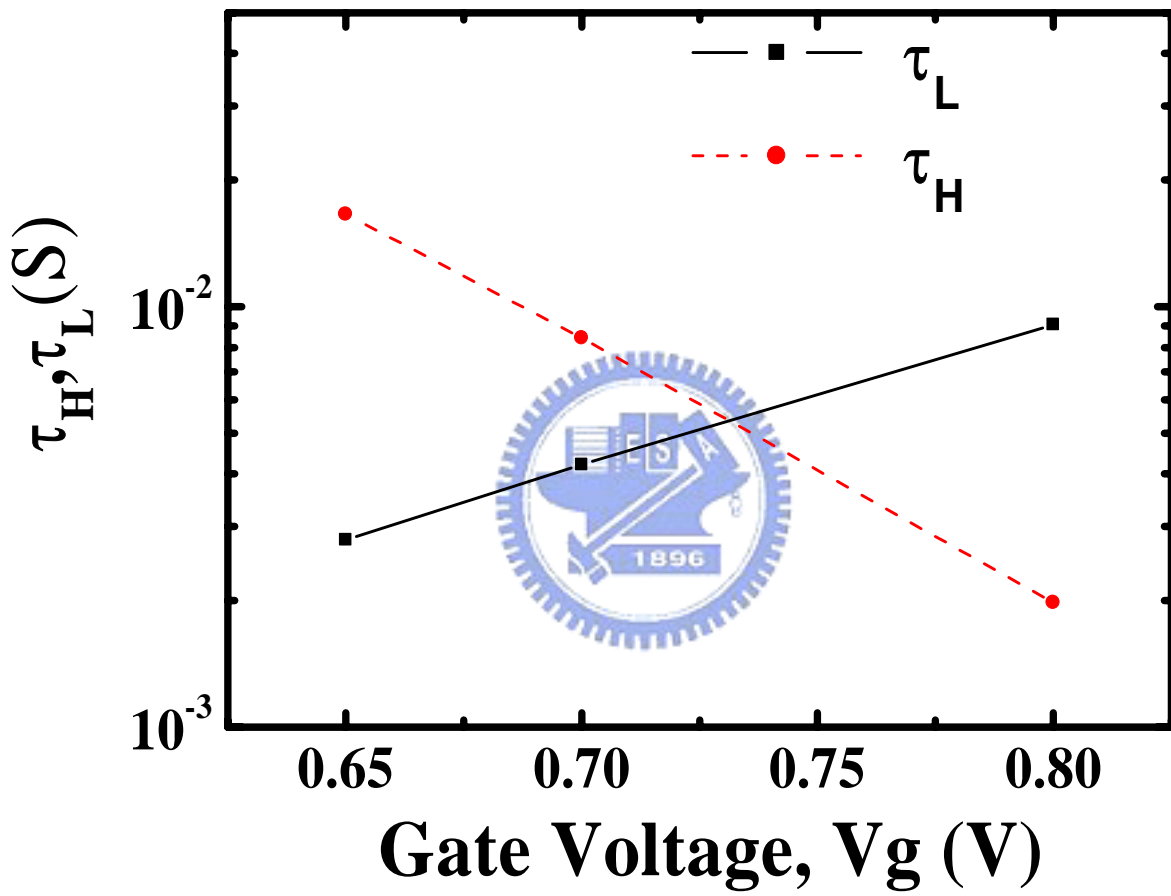
**Fig. 3.9** Average τ_L and τ_H versus gate voltage in a small area (W/L=0.16μm/0.12μm) n-MOSFET for the weak inversion .
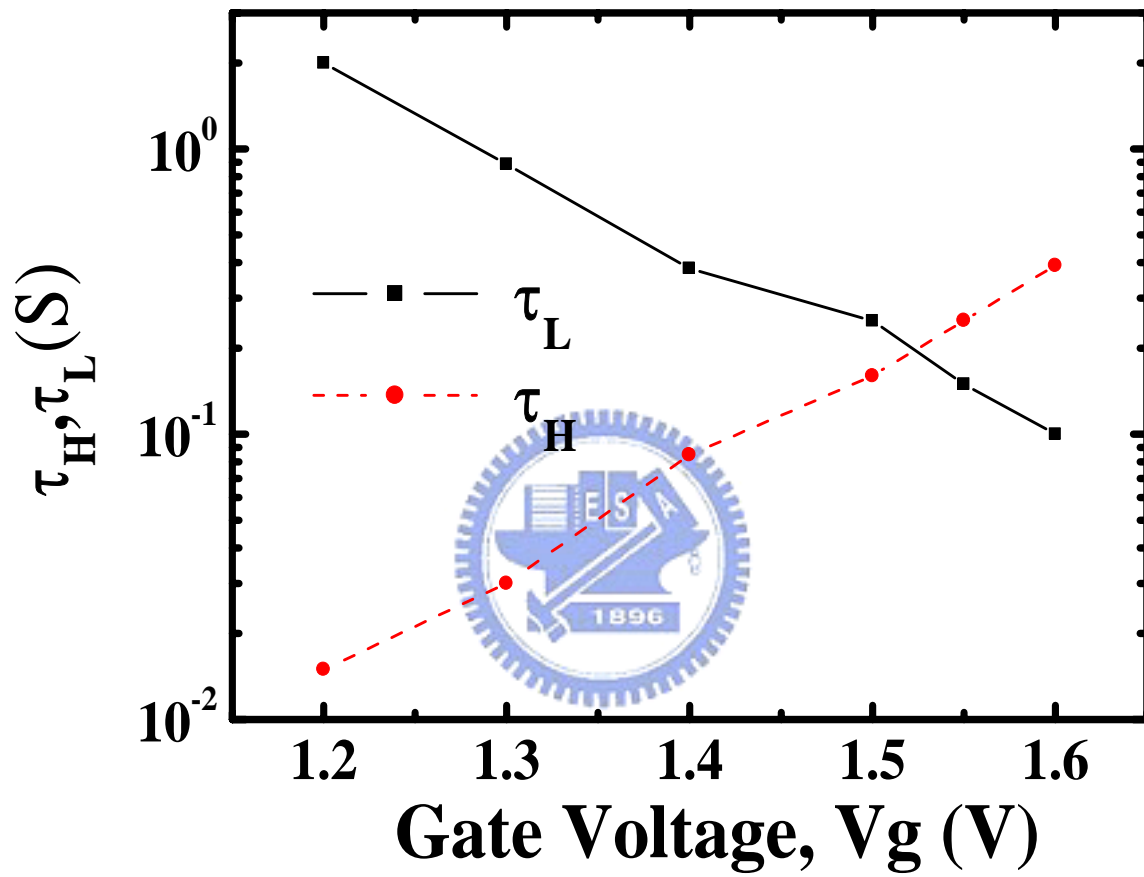
Fig. 3.10 Average τ_L and τ_H versus gate voltage in a small area (W/L=0.16μm/0.12μm) n-MOSFET for the strong inversion .
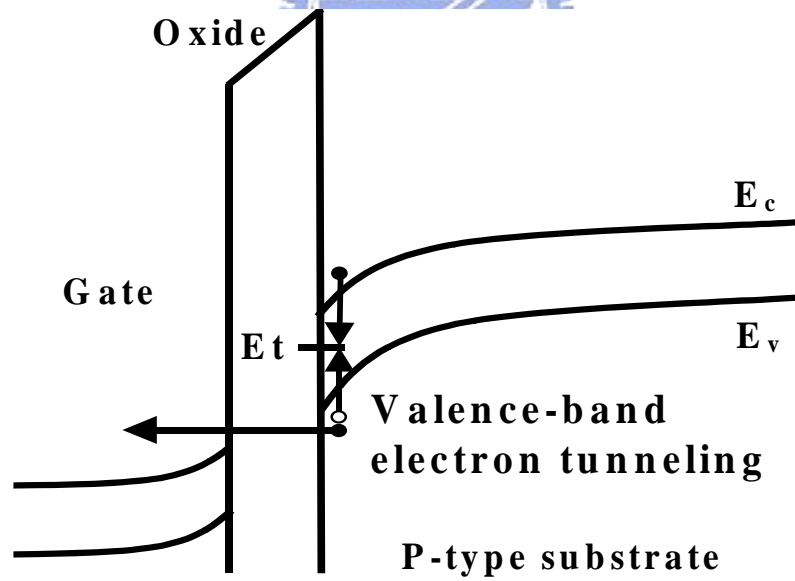
$$f_t = \frac{\tau_L}{\tau_H + \tau_L}$$
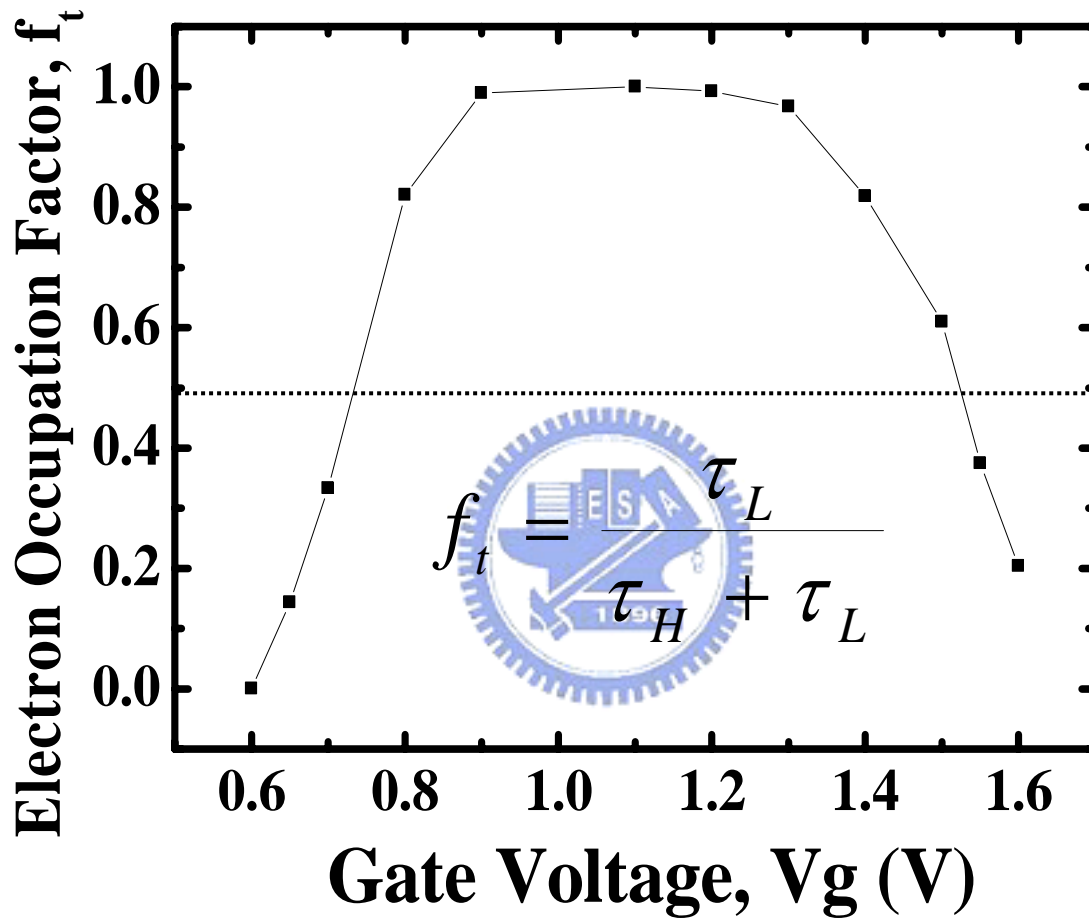
Fig. 3.11 The corresponding electron occupation factor (f_t) versus the entire range of Vg. When ft is equal to 0.5, gate voltages are equal to 0.7V and 1.5V, respectively.
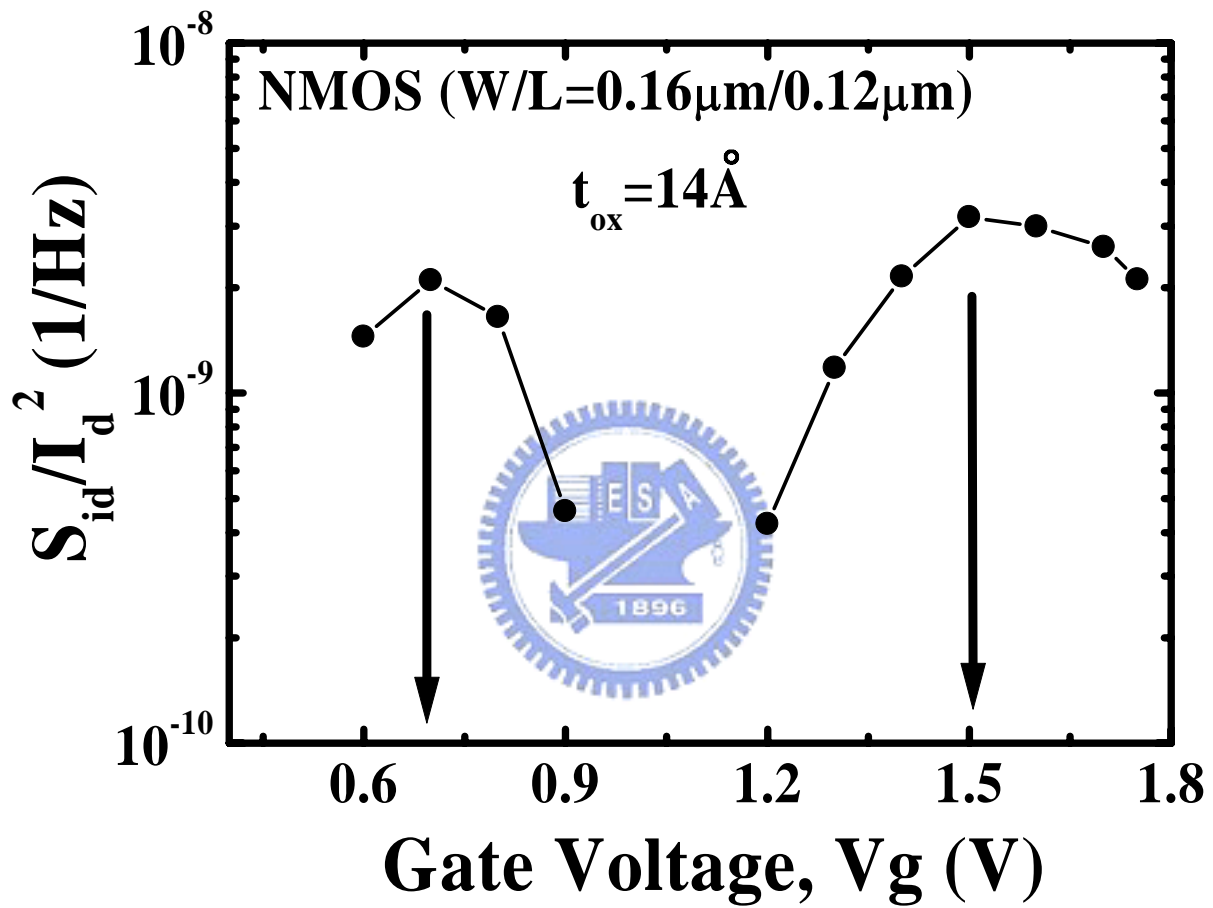
Fig. 3.12 The corresponding normalized noise power spectral density versus the entire range of Vg at f = 100 (Hz). The noise level has maximum values at Vg=0.7V and 1.5V.
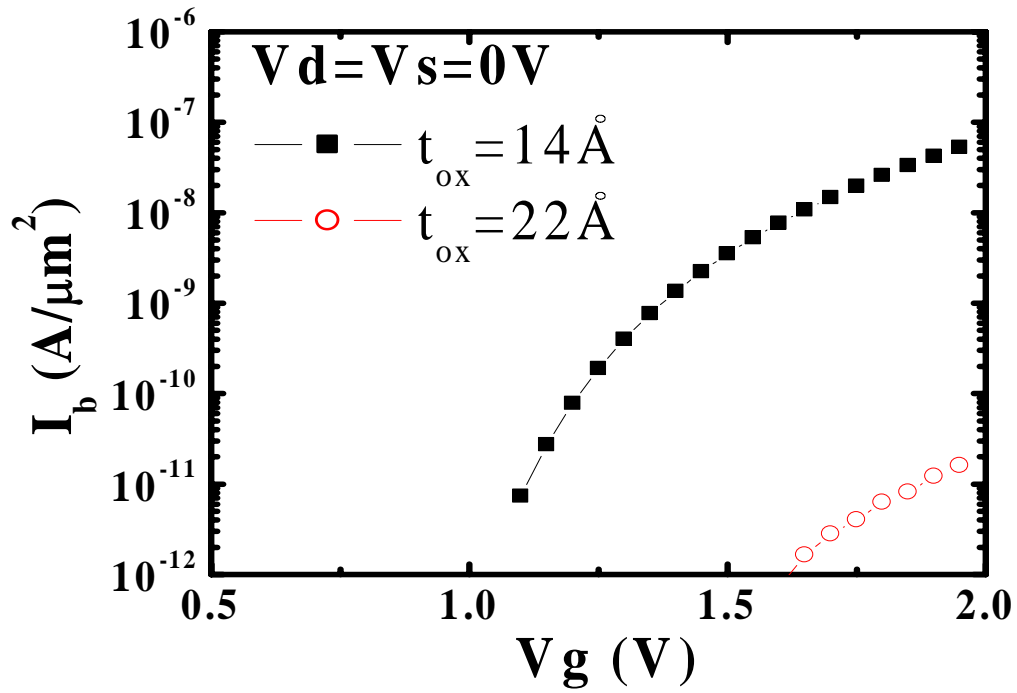
Fig. 3.13 (a) Substrate current versus gate bias with Vd=Vs=0V (b) Illustration of valence-band electron tunneling and electron and hole recombination at an interface trap.

tunneling of valence-band electrons from the p-type substrate into the conduction band of the poly gate. After the 1V gate bias, the substrate current becomes larger in n-MOSFETs with 14 Å gate oxide. And, in ultra-thin oxide n-MOSFETs, valence electron tunneling is more significant at a larger gate voltage and holes are left behind in the channel. Because of the increased hole concentration at a larger Vg, the hole capture at the interface trap becomes more probable, thus resulting in a reduction of f_t. In other words, the interface trap serves as electron and hole recombination center and the increase of low frequency noise can be well understood.

Chapter 4

Excess Low-Frequency Noise in Ultra-Thin Oxide

n-MOSFETs with Floating Body

4.1 Introduction

Excess low-frequency noise in ultra-thin oxide n-MOSFETs with floating body configuration is investigated. We show that ultra-thin gate oxide n-MOSFETs with floating body exhibit similar noise behaviors to PD SOI MOSFET's. In the beginning, the excess noise model in PD SOI MOSFETs is introduced. Then, the kink effect in ultra-thin gate oxide n-MOSFETs with floating body is studied, which would induce excess low frequency noise. After that, the impact of soft breakdown location on drain current noise in ultra-thin gate oxide n-MOSFETs (1.6nm) is investigated. In a channel breakdown device, a noise overshoot phenomenon is observed in the ohmic regime. It is characterized by a peak in current noise spectral density versus the operation gate voltage, whereby the peak amplitude can be about one order of magnitude higher than the background 1/f noise. The origin of this excess noise is believed due to soft breakdown (SBD) enhanced valance-band electron tunneling and thus induced floating body effect. The findings indicate that channel SBD enhanced drain current noise can be a reliability issue in PD analog SOI CMOS circuit.

4.2 Excess Low-Frequency Noise Model in SOI MOSFETs

The excess low-frequency noise is specific to PD SOI MOSFET's associated with the floating-body effect (FBE). Fig. 4.1(a) shows the shot noise sources in an

SOI MOSFET operating in strong inversion. Although the shot noises are small in magnitude compared with flicker noise, they are amplified by FBE and give rise to the excess low-frequency noise in PD SOI MOSFET.

The noise small-signal equivalent circuit shown in Fig. 4.1(b) can explain the mechanism underlying the excess low-frequency noise [16]. The shot noise results from the impact ionization current (I_{ii}):

$$S_{ib1} = M \cdot 2qI_{ii} \tag{4.1}$$

where **M** is a multiplication factor [17]. Impact ionization current exhibits shot noise because only the carriers with sufficient kinetic energy can generate electron-hole pairs. The second noise source is associated with the body-source diode current (**I_{bs}**) where carriers have to overcome the built-in potential barrier:

$$S_{ib2} = 2qI_{bs} \tag{4.2}$$

The two noise current flow through the body-ground impedance (c_{eq} and r_{eq}), leading to a fluctuation in body potential:

$$S_{vb} = S_{ib} \cdot \frac{r_{eq}^2}{1 + (\frac{f}{f_c})^2} \tag{4.3}$$

where

$$S_{ib} = S_{ib1} + S_{ib2} \qquad \text{and} \qquad f_c = \frac{1}{2\pi \cdot r_{eq} c_{eq}}$$

The equivalent body-ground resistance r_{eq} is equal to the small-signal resistance of the body-source junction. The equivalent body-ground capacitance c_{eq} can be modeled as the sum of all the capacitance seen from the body. And, the fluctuation in the body potential modulates the threshold voltage of the device:

$$S_{vth} = S_{vb} \cdot (\frac{\partial V_{th}}{\partial V_{bs}})^2 \tag{4.4}$$
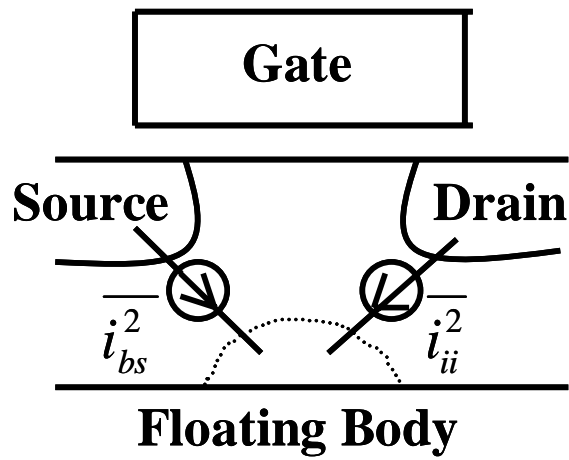
$\overline{i_{ii}^2}$:Shot noise due to impact ionization current

$\overline{i_{bs}^2}$:Shot noise due to body-source diode current

(a)

(b)
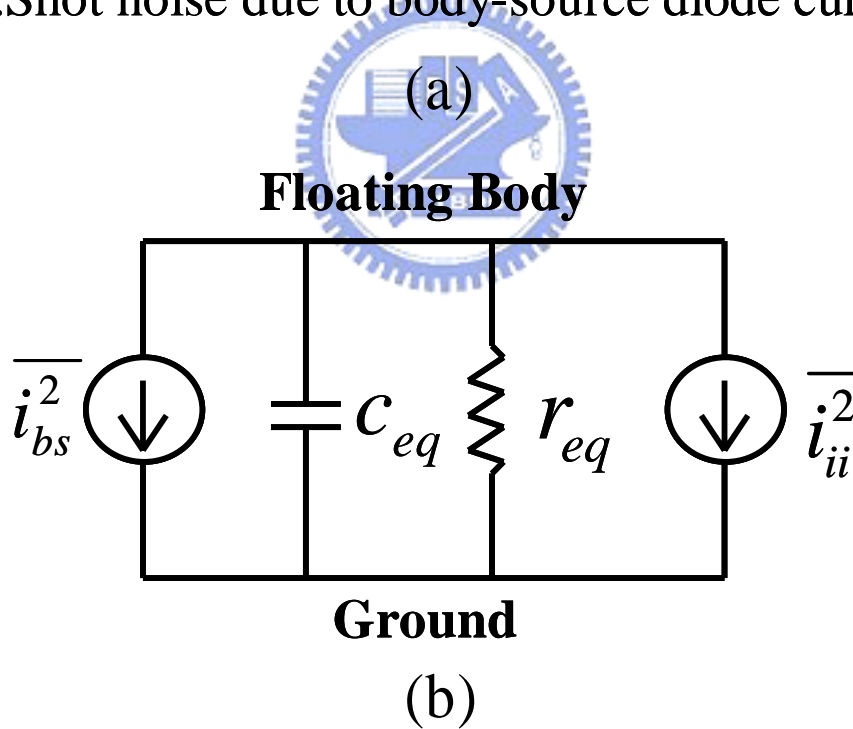
Fig 4.1 **(a)** Shot noise sources in an SOI MOSFET operating in strong inversion
(b) The noise small-signal equivalent circuit for the floating body

Due to the fluctuation in V_{th}, the excess drain current noise is given by:

$$S_{id-excess} = S_{vth} \cdot (\frac{\partial I_{ds}}{\partial V_{th}})^2$$

$$= \frac{(M+1) \cdot 2qI_{ii}g_{mb}^2 r_{eq}^2}{1 + (\frac{f}{f_c})^2} \qquad (4.5)$$

where g_{mb} is the body transconductance. Since 1/f noise and excess noise are uncorrelated, the total spectrum density of low-frequency drain current noise is the sum of the two components:

$$S_{id-total} = S_{id-1/f} + S_{id-excess}$$

4.3 Kink Effect Induced Excess Low-Frequency Noise in Ultra-Thin Oxide n-MOSFETs with Floating Body

Fig. 4.2 shows ours measured I_d-V_d characteristics of n-MOSFETs (W/L=1μ m/1μ m) with floating body and grounded body. Gate is biased at 0.9V. The kink effect is obviously observed in a floating body n-MOSFET and not in a n-MOSFET with body grounded. Due to the impact ionization current, electron-hole pairs are created at the drain end. Then, the holes go to the floating body, which induce the variation of body potential. At the kink point where the body potential sufficiently increases, threshold voltage (V_{th}) drops and thus causes an increase of the drain current. The phenomenon in the floating body n-MOSFET consists with others' result in PD SOI MOSFETs. The excess noise is firstly found in floating body PD SOI MOSFET as the drain bias is above the kink voltage [18]. In Fig. 4.3, normalized noise power spectrum density in an n-MOSFET with floating body is measured at gate biased 0.9 V, and drain biased 0.5V 1.2V 1.4V. The device has 1μ m gate width and 1μ m length. Fig. 4.3 shows that the excess noise is not observable in the curve
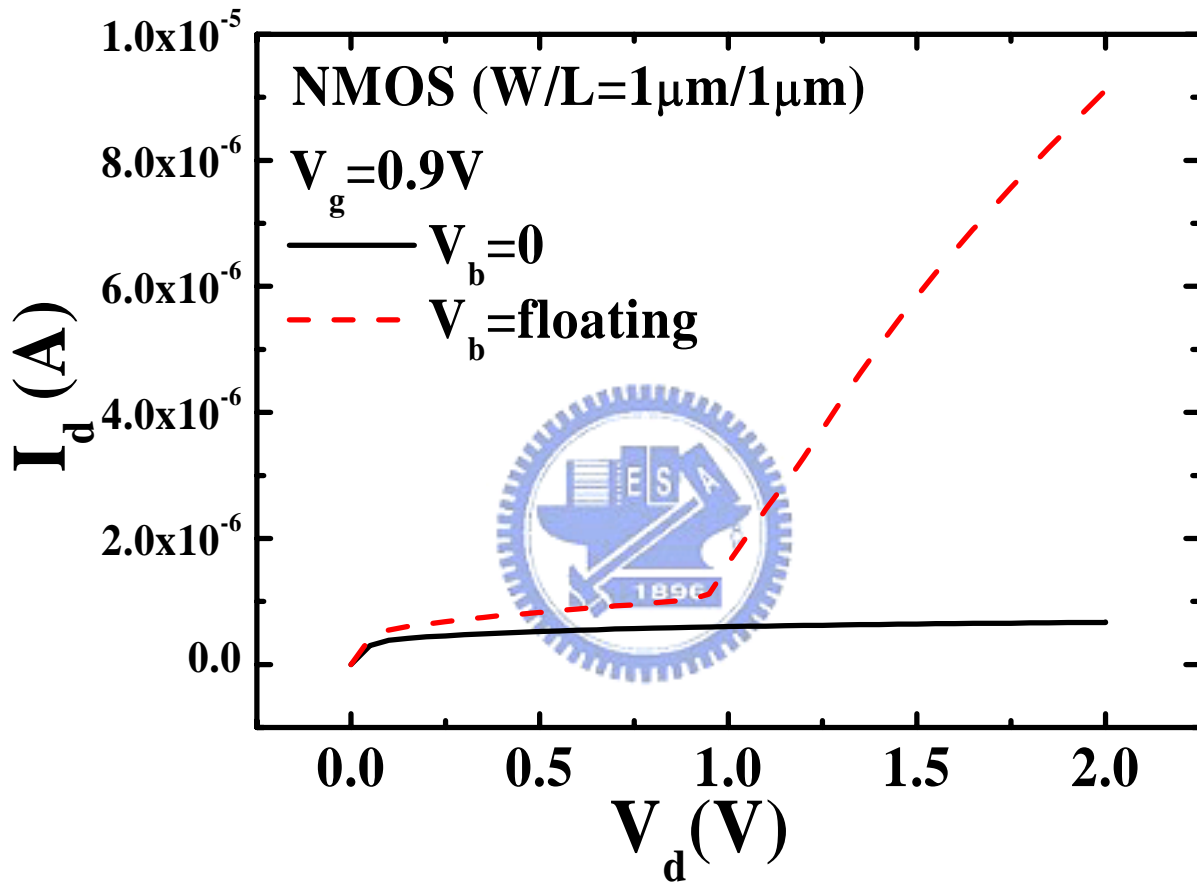
Fig. 4.2 The I_d-V_d characteristics in NMOS devices with floating body and grounded body when gate is biased at 0.9V
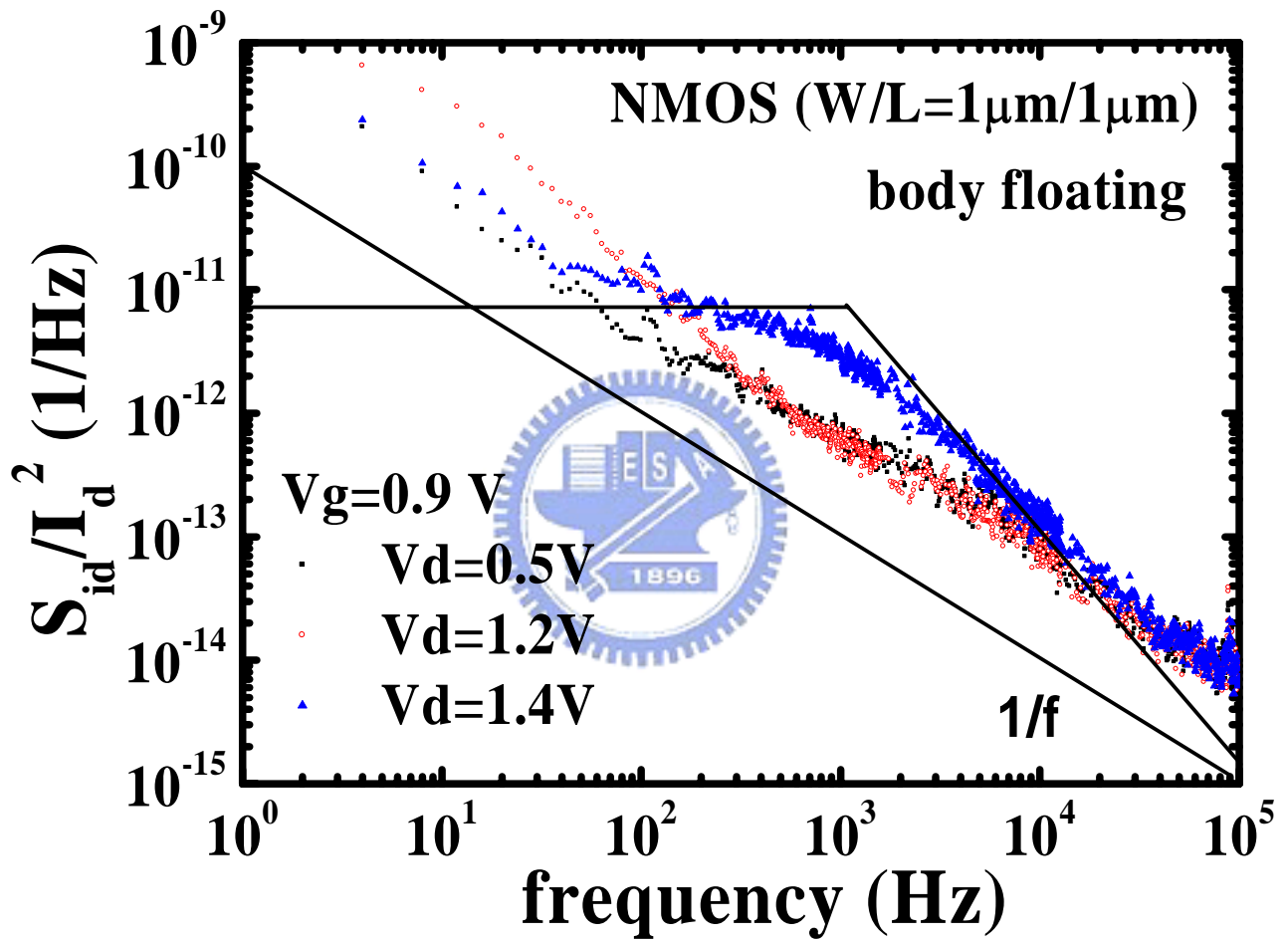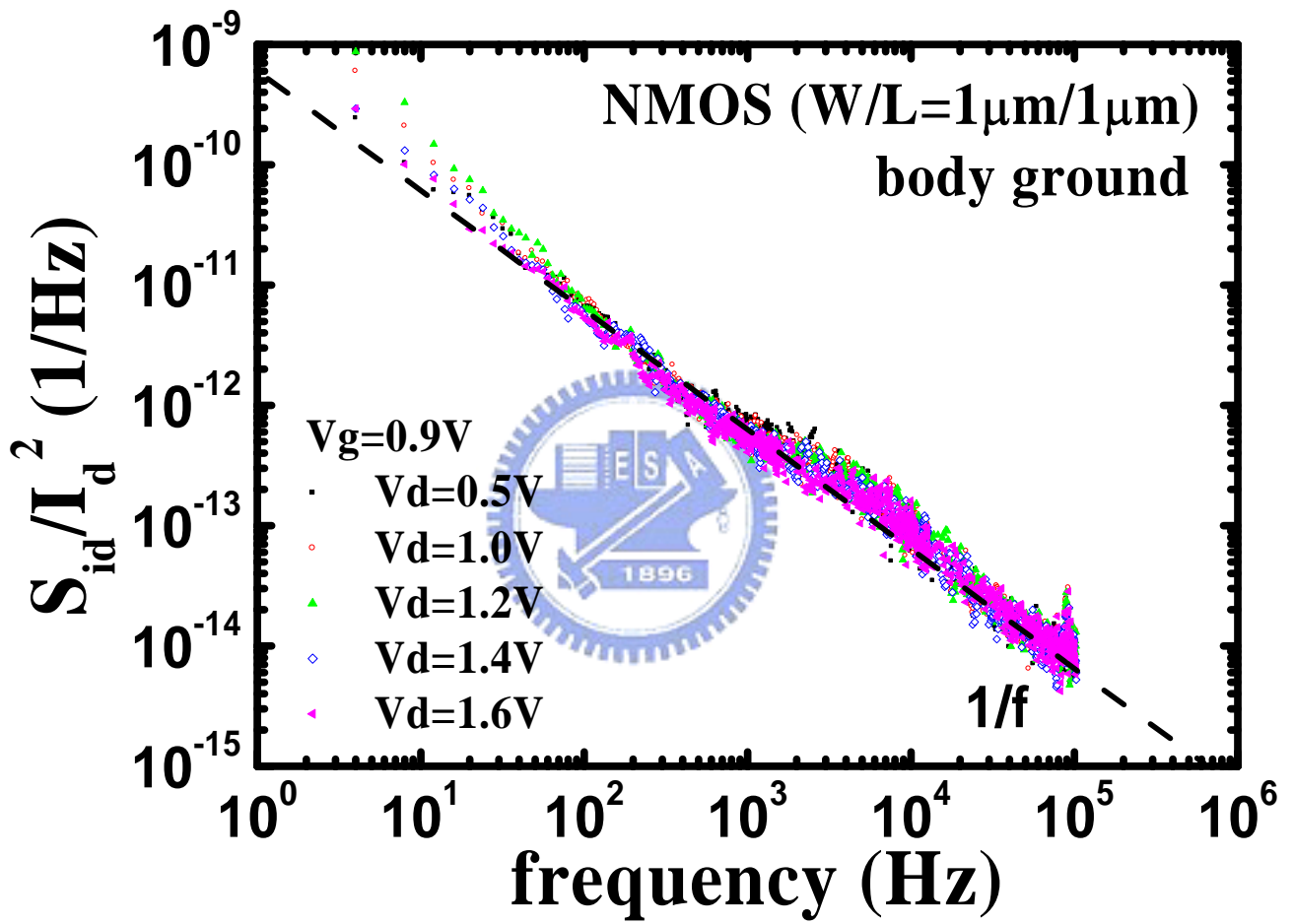
Fig. 4.3 Normalization noise power spectral density in a floating body NMOS under different drain voltages when gate is bias at 0.9V

corresponding to the linear regime operation. The Lorentzian-like excess noise is significant only when the drain bias is above the kink voltage. The reason is that the origin of the excess noises could be related to high drain bias induced impact ionization current.

In Fig 4.4, normalized noise power spectrum density in an n-MOSFET with body grounded is measured at V_g=0.9 V, V_d=0.5V, 1V, 1.2V, 1.4V, and 1.6V, The device has 1μ m gate width and 1μ m length. Fig. 4.4 manifests that only flicker noise is exhibited at drain biased from linear regime to saturation regime. That is, the excess noise can be effectively eliminated, as body contact is grounded.

Fig. 4.5 shows the normalized noise spectrum of an n-MOSFET with floating body under different drain biases, as is above the kink onset voltage. The normalized noise power spectrum exhibits a plateau up to the characteristic frequency $f_c = 1/(2\pi \cdot r_{eq} c_{eq})$ before a $1/f^2$ roll-ff sets in. Furthermore, a typical Lorentzian shift to lower plateau and higher cut-off frequency is observed due to the increase of impact ionization current with the drain bias. Because the r_{eq} decreases with increasing drain voltage, a larger drain bias gives rise to a higher f_c but a smaller noise magnitude.

Fig. 4.6 illustrates that the normalized drain current noise initially increases with the drain voltage and reaches a peak when the kink point appears for a given frequency. This is when the device switches from linear operation regime to the regime around the kink point with the increase of the drain voltage.

Fig. 4.4 Normalization noise power spectral density in grounded body NMOS under different drain voltage when gate is bias at 0.9V
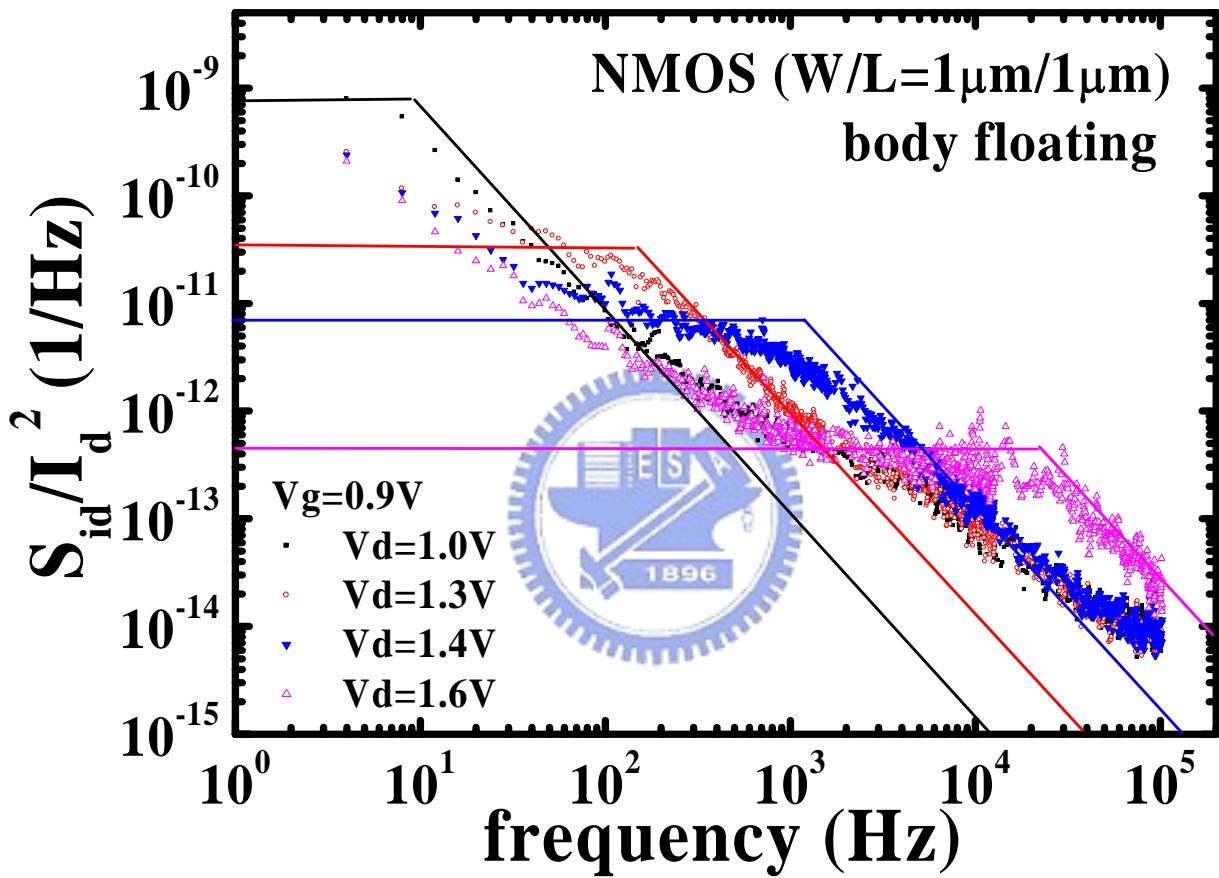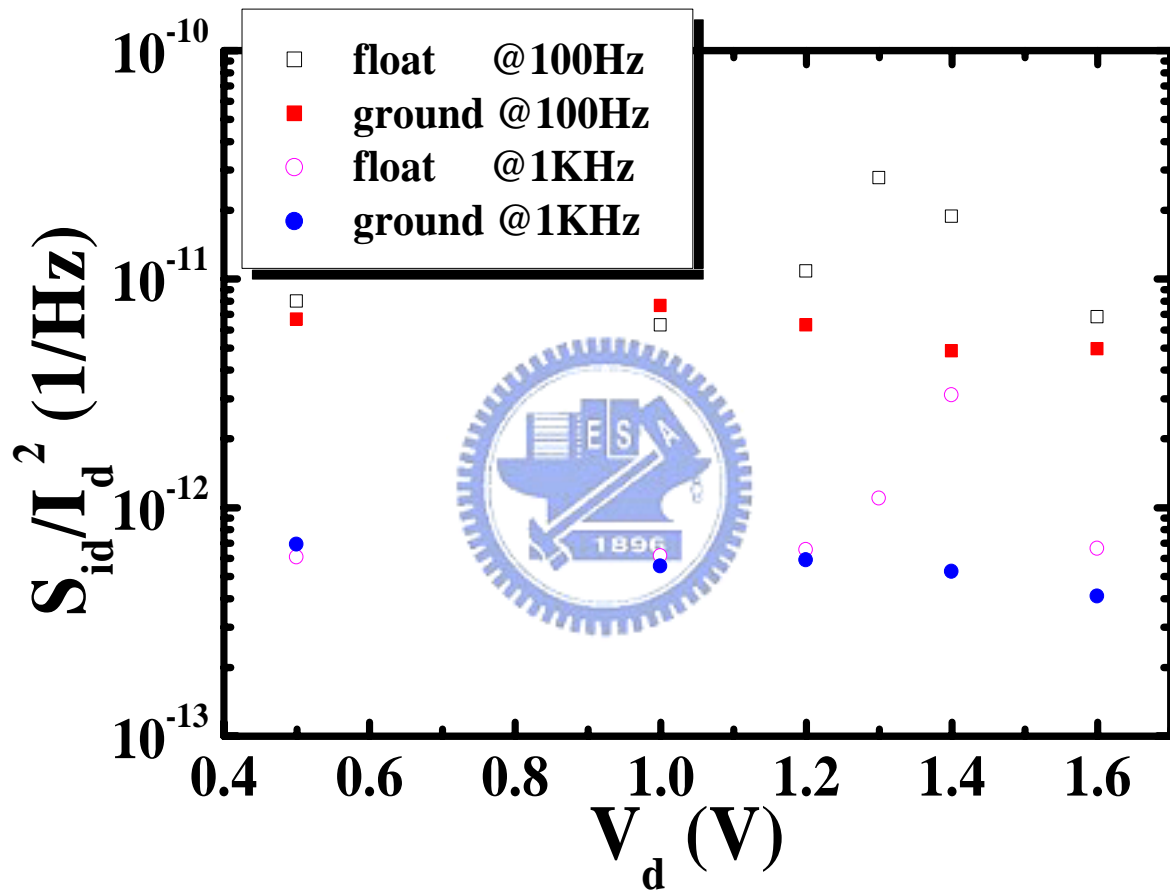
Fig. 4.5 Normalization noise power spectral density in floating body NMOS under different drain voltage when gate is bias at 0.9V

Fig. 4.6 Comparison of normalization noise power spectral density under different drain bias in floating body NMOS and grounded body NMOS for given frequency

4.3 Channel Soft Breakdown Enhanced Excess Low-Frequency Noise in Ultra-Thin Oxide n-MOSFETs with Floating Body

The devices in this work were made with a 0.13μm standard CMOS process on p-type silicon substrate. The gate length is 0.13μm, the gate width is 10μm and the oxide thickness is 1.6nm. In this paragraph, all devices were stressed at high constant gate voltages with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10μA. After breakdown, the device on-state characteristics were checked and no difference was observed. Similarly, from others' study, [19]-[23] the impact of the gate oxide SBD is only a noticeable increase in leakage current without degrading any on-state device performance in operation.

The breakdown position was examined by using the method given in reference [24]. Table 1 shows the ratio of I_d/I_s+I_d before and after SBD in the two n-MOSFETs. The measurement gate bias is $|V_g|=1.5V$ and $V_d=V_s=0V$ in the accumulation region. A significant increase of I_d/I_s+I_d in device B indicates that breakdown is located at the drain edge, while the moderate change of I_d/I_s+I_d in device A implies that SBD position is in the channel. Aside from I_d/I_s+I_d, I_b/I_s+I_d was measured (also shown in Table 1). In the c-SBD devices, the tunneling leakage current in the channel region was enhanced, thus resulting in a larger I_b/I_s+I_d. In the case of e-SBD, the breakdown was above the drain edge. As a result, the tunneling leakage current in the channel region remained almost the same as pre-SBD, and the increased edge leakage current made I_s+I_d larger and led to a smaller I_b/I_s+I_d. That is, the results in Table 1 show that the breakdown location can be determined by I_d/I_s+I_d or by the change of I_b/I_{sd} in the accumulation region. In Fig. 4.7, the gate current and substrate current as a function of Vg in fresh, channel SBD, and edge SBD n-MOSFETs were compared.

acc. region	nMOSFET	
	device A (c-SBD)	device B (e-SBD)
I_d/I_s+I_d before SBD	0.5078	0.5297
I_d/I_s+I_d after SBD	**0.4482**	**0.9957**
I_b/I_s+I_d before SBD	0.0287	0.0178
I_b/I_s+I_d after SBD	**0.1426**	**0.0001**

Table. 1 The ratio of I_d/I_s+I_d and I_b/I_s+I_d before and after SBD in two n-MOSFETs are shown.

This comparison indicates that the substrate current increased drastically in channel-SBD devices, but the change in edge-SBD devices was negligible. The substrate current at a positive gate bias is attributed to channel hole creation resulting from valence-band electron tunneling from Si substrate to the conduction band of the poly gate. The tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the bandgap of the n^+ poly-gate. Thus, these findings support the viewpoint that the post c-SBD I_b is enhanced largely at a positive gate bias due to a localized effective oxide thinning [25] while I_b is nearly unchanged after e-SBD. The results presented provide direct experimental evidence that channel soft breakdown may induce a substrate leakage current increase in device operation, especially at a high gate bias.

Fig. 4.8 illustrates two floating-body charging processes in channel breakdown and drain-edge breakdown n-MOSFETs. In a c-SBD device with a positive gate bias (Fig. 4.8(a)), valence band electron tunneling from the substrate to the gate is increased after SBD. The excess holes left behind in the valence band flow to the body and raise the body potential. Fig. 4.8(b) presents the drain-induced floating-body charging in an e-SBD n-MOSFET. If the breakdown path is in the drain edge, the band-to-band tunneling current increases due to a stronger band bending in the n^+ drain region, thus raising the body potential at a high drain bias. According to the above results, c-SBD enhanced floating body effect in PD SOI MOSFETs is proposed as a new body-charging mode [26][27]. Fig. 4.9 shows the low frequency drain noise spectrums of an n-MOSFET before and after both SBD modes. The measurement drain bias is 0.1V and the gate bias is 1.2V. The pre-BD noise characteristics of n-MOSFETs are dominated by a 1/f-like flicker noise component. An additional Lorentizian-like spectrum appears only when both channel soft breakdown occurs and body contact is floating. As body contact is grounded, the excess noise can be
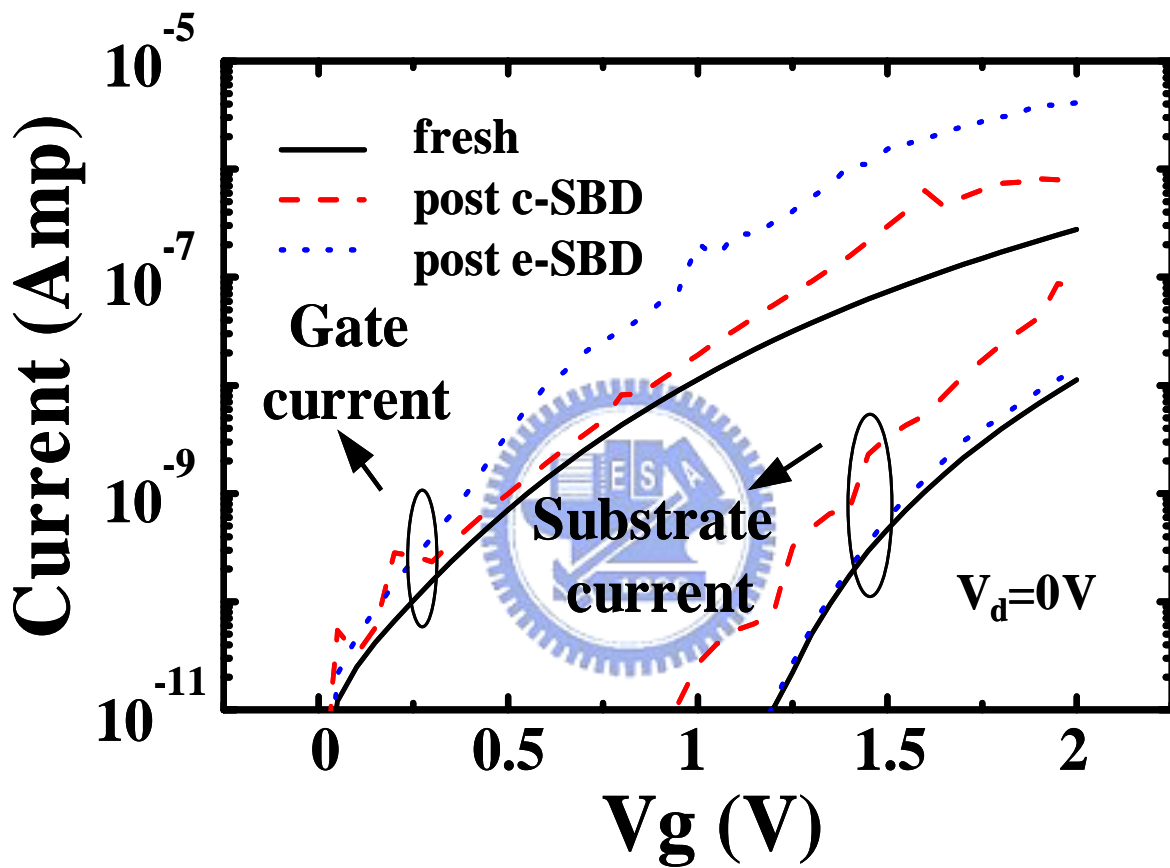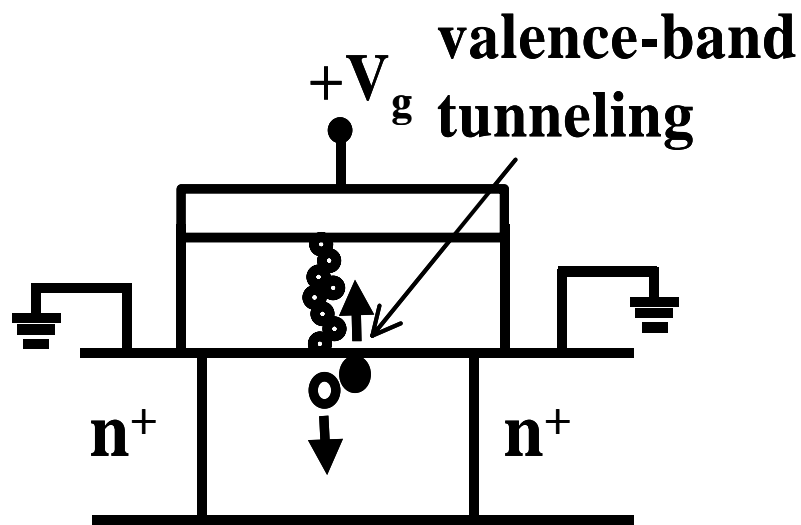
Fig. 4.7 The gate current and substrate current as a function of Vg in fresh, channel SBD, and edge SBD n-MOSFETs were compared.

valence-band tunneling

+V$_g$

n$^+$ **n$^+$**

(a)

band-to-band current

+V$_d$

n$^+$ **n$^+$**
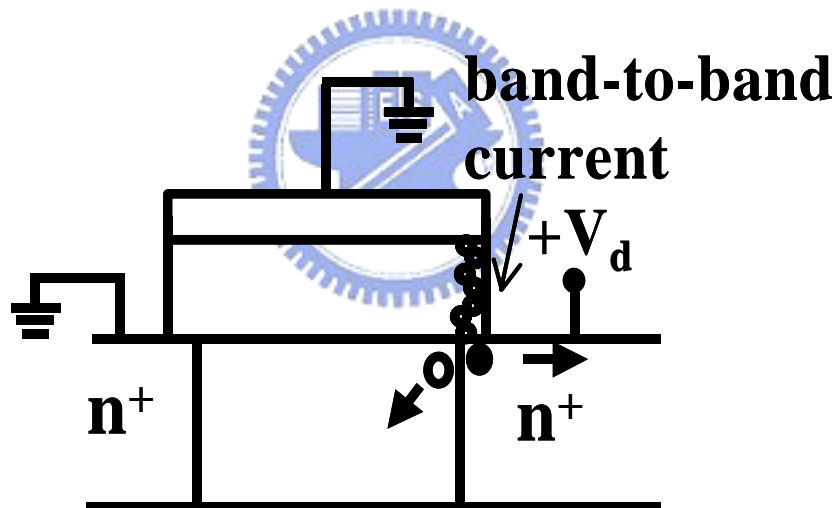
(b)

Fig. 4.8 (a) Valence band electron tunneling induced floating-body charging in a c-SBD n-MOSFET **(b)** The drain-current induced floating-body charging in an e-SBD n-MOSFET

Fig. 4.9 The low frequency drain noise spectrums of n-MOSFET before and after both SBD modes are shown .The measurement drain bias is 0.1V and the gate bias is 1.2V.
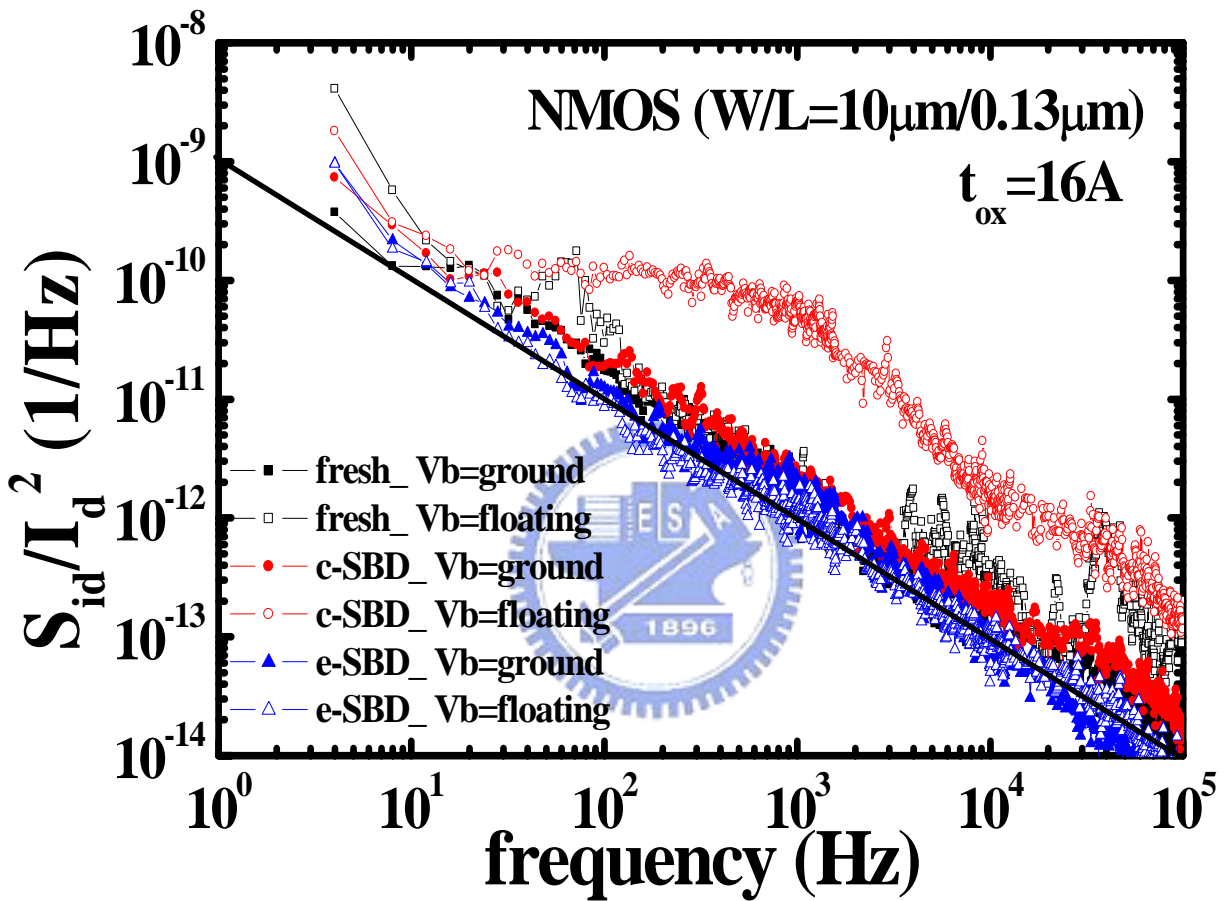
effectively eliminated. The excess noise is also not observable in e-SBD devices. It indicates that the additional body charge injection in c-SBD devices not only enhances the floating body effect but also degrades the low frequency noise power spectrum.

Fig. 4.10 shows the normalized noise power spectrum density of a c-SBD n-MOSFET with floating body under different gate biases. We observed a typical Lorentzian shift to lower plateau and higher cut-off frequency due to the substrate leakage current increase with the gate bias. At Vg=1.6V, only 1/f noise is observed. In fact, we believe there is still a Lorentzian in this case but shifted to a lower frequency, below our measurement limit. The excess noise of a c-SBD nMOSFET with floating body shows similar behaviors to the excess noise induced by the kink effect in SOI nMOSFETs.

Fig. 11 illustrates that for a given frequency, the normalized drain current noise of c-SBD n-MOSFETs with floating body initially increases with Vg and reaches a peak when gate bias is 1V. This phenomenon is consistent with other research claiming that the RC network of the body in floating-body PD SOI n-MOSFET's amplifies and filters the shot noise of substrate current, giving rise to a Lorentzian-like spectral density in noise [28][29]. It can be explained that with an increase in gate voltage, c-SBD induces more substrate current as a result of valence band electron tunneling. Further increase in gate bias leads to a low amplification gain, because the equivalent substrate resistance decreases with the substrate current increase, and thus the noise magnitude decreases. The significance of soft breakdown position to the low frequency drain current noise in PD SOI NMOS devices has been evaluated. The excess floating body noise would be enhanced if a breakdown path occurs at the channel of n-MOSFETs. The enhanced noise originates from channel soft breakdown enhanced valance band electron tunneling. This noise source correlates well with the

amplification by small white noise of substrate currents in floating body devices. The c-SBD enhanced excess noise may occur even with supply voltage less than 1.0V and would be a serious reliability concern in ultra-thin gate oxide analog SOI devices.
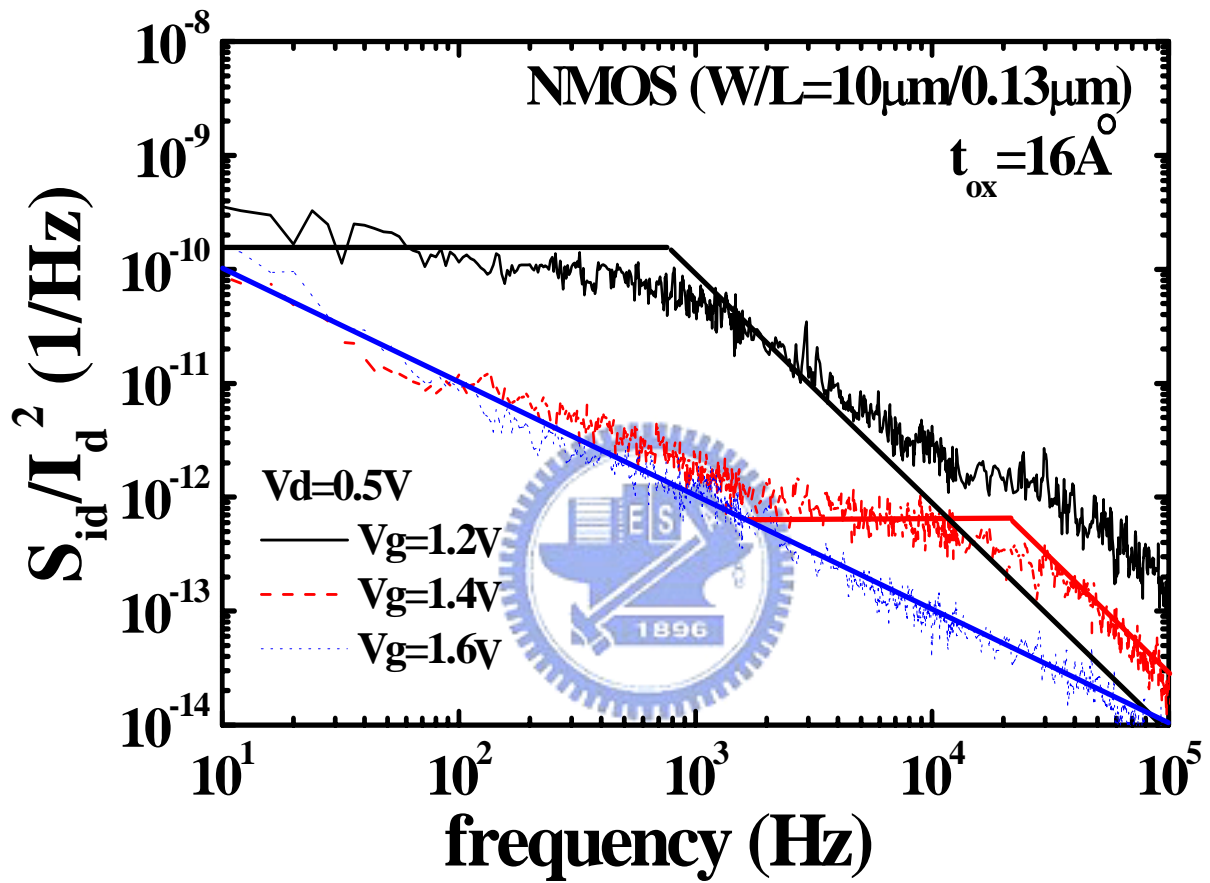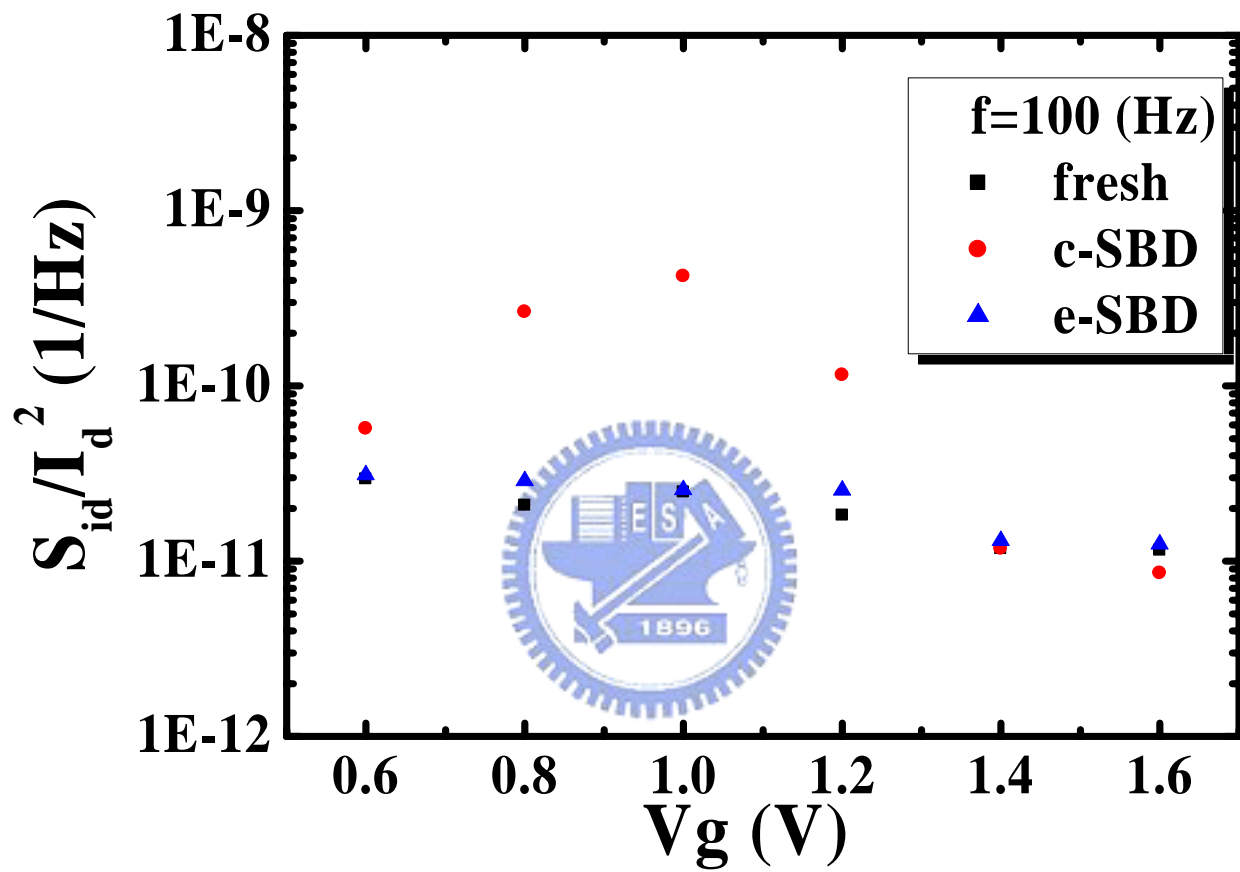
Fig. 4.10 The normalized noise power spectrum of a c-SBD n-MOSFETs with floating body under different gate biases is shown.

Fig. 4.11 Comparison of normalization noise power spectral density under different gate bias in the flesh device, c-SBD device and e-SBD device at f=100(Hz).

Chapter5
Conclusion

A new G-R noise mechanism in ultra-thin gate oxide (14Å) n-MOSFETs has been proposed in this thesis. The traditional flicker noise model of oxide charge tunnel trapping/de-trapping cannot account for the observed noise behavior. The analysis of RTS reveals that the low-frequency excess noise is attributed to electron and hole capture at interface traps. The increased channel hole concentration is due to valence-band electron tunneling. The increase of flicker noise would be a serious reliability issue in ultra-thin gate oxide n-MOSFETs.

The excess low-frequency noise in ultra-thin oxide n-MOSFETs with floating body has also been investigated. Ultra-thin gate oxide n-MOSFETs with floating body configuratoin exhibit similar noise behavior to PD SOI MOSFET's. Moreover, the significance of soft breakdown position to the low-frequency noise in ultra-thin oxide n-MOSFETs with floating body has been evaluated. The excess floating body noise would be enhanced if a breakdown path occurs at the channel of n-MOSFETs. The enhanced noise originates from channel soft breakdown induced large substrate current. This noise source correlates well with the amplification by small white noise of substrate currents in floating body devices. The c-SBD would be a serious reliability concern in ultra-thin gate oxide analog SOI devices.

References

[1] Ali Hajimiri and Thomas H. Lee, "A general theory of phase noise in electrical oscillators" *IEEE J. Solid-State Circuits,* vol. 33, pp. 179-194, 1998.

[2] Ewout P. Vandamme et al. "Critical Discussion on Unified 1/f Noise Models for MOSFETs,' *IEEE TED*, Vol. 47, pp. 2146, 2000

[3] Z. Celik-Butler, "Low-frequency noise in deep-submicron metal-oxide-semiconductor field-effect transistors," *IEE Proc.-Circuits Devices Syst.,* Vol. 149, No.1, February 2002.

[4] M.J. Kirton, M.J. Uren, Adv. Phys. (1989); 38: 367

[5] M.J. Kirton, M.J. Uren, S. Collins, M. Schulz, A. Karmann, K. Scheffer, Semicond. Sci. Technol. 4 (1989) 1116

[6] J. Chen, P. Fang, P. K. Ko, C Hu, R. Solomon, T. Y. Chan, and C. G. Sodini, "Noise overshoot at drain current kink in SOI MOSFET," *in IEEE SOS/SOI Conf. Proc.,* 1990, pp. 40-41

[7] E. Simoen, U. Magnusson, A. L. P. Rotondaro, and C. Claeys, "The kink-related excess low-frequency noise in silicon-on-insulator MOST's and frequency," *IEEE Trans. Electron Devices*, vol. 41, pp. 330-339, Mar. 1994.

[8] Y. C. Tseng, W. M. Huang, J. A. Babcock, J. M. Ford, and J. C. S. Woo, "Correlation between low-frequency noise overshoot in SOI MOSFET's and frequency dependence of floating body effect," in *Symp. VLSI Technol.*, 1997, pp. 99-100.

[9] A. L. McWhorter, "1/f noise and germanium surface properties," in Semiconductor Surface Physics. Philadelphia, PA: Univ. of Pennsylvania Press, 1957, p. 207.

[10] F. N. Hooge, "1/f noise," Physics, vol. 83B, p. 14,1976

[11] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 654-665, 1990.

[12] Machlup S. Spectrum of two-parameter random signal. *J Appl Phys* 1954*; 25:341-3*

[13] M. J. Knitel, P. H. Woerlee, A. J. Scholten and A. T. A. Zegers-Van Duijnhoven, "Impact of process scaling on 1/f noise in advanced CMOS technologies," in *IEDM Tech. Dig.*, pp. 463-466, 2000.

[14] Hisayo sasaki Momose, Hideki Kimijima, Shin-ichiro Ishizuka, Yasunori Miyahara, Tatsuya Ohguro, Takashi Yoshitomi, Eiji Morifuji, Shin-ichi Nakamura, Toyota Morimoto, Yasuhiro Katsumata and Hiroshi Iwai, "A study of flicker noise in n- and p-MOSFETs with ultra-thin gate oxide in the direct-tunneling regime," in *IEDM Tech. Dig.*, pp. 923-926, 1998.

[15] R. Brederlow, W. Weber, D. S.-Landsiedel, and R. Thewes, "Fluctuations of the low frequency noise of MOS transistors and their modeling in analog and RF-circuits," in *IEDM Tech. Dig.*, pp. 159-162, 1999.

[16] Wei Jin, "Shot-Noise-Induced Excess Low-Frequency Noise in Floating-Body Partially Depleted SOI MOSFET's," *IEEE Trans. Electron Devices,* vol. 46, pp. 1180-1185 No.6, June 1999

[17] R. P. Jindal, "Noise associated with substrate current in fine-line NMOS field-effect transistors," *IEEE SOI Conf.,* 1996, pp. 146-147

[18] J. Chen, P. K. Ko, C. Hu, R. Solomon, T. Y. Chan, and C. G. Sodini, "Noise overshoot at drain current kink in SOI MOSFET," in *IEEE SOS/SOI Conf. Proc.,* 1990, pp. 40-41

[19] Eli Harari, J. of Appl. Phys. **49**, 2478 (1978)

[20] I.C. Chen, S. Holland, K.K. Young, C. Chang and C. Hu, *Appl. Phys. Lett.* **49**, 669 (1986).

[21] M. Houssa, T. Nigam, P.W. Mertens and M.M. Heyns, *J. of Appl. Phys.* **84**, 4351 (1998)

[22] E. Miranda, J. Sune, R. Rodriguez, M. Nafria and X. Aymerich, *Appl. Phys. Lett.* **73**, 490 (1998)

[23] B.E. Weir, P.L. Silverman, D. Monroe, K.S. Krisch, M.A. Alam, G.B. Alers, T.W. Sorsch, G.L. Timp, F. Baumann, C.T. Liu, Y. Ma, and D. Hwang, Tech. Dig. Int. Electron Devices Meet. 73 (1997)

[24] Robin Degraeve, Ben Kaczer, An De Keersgieter, and Guido Groeseneken, "Relation between breakdown mode and breakdown location in short channel NMOSFETs and its impact on reliability specifications", in 2001 *IRPS Proc.*, p.360 2001.

[25] Felice Crupi, Giuseppe Iannaccone, Isodiana Crupi, Robin Degraeve, Guido Groeseneken, and Herman E. Mase, "Characterization of Soft Breakdown in Thin Oxide NMOSFETs Based on the Analysis of the Substrate Current", in *IEEE Transaction on Electron Devices*, vol. 48, no. 6, p. 1109 2001.

[26] S.K.H. Fung, N. Zamdmer, P.J. Oldiges, J. Sleight, A. Mocuta, M. Sherony, S-H. Lo, R. Joshi, C.T. Chuang, I. Yang, S. Crowder, T.C. Chen, F. Assaderaghi, and G. Shahidi, "Controlling floating-body effects for 0.13 μm and 0.1 μm SOI CMOS", in 2000 *IEDM Techn. Digest*, p.231 2001.

[27] M.C. Chen, C.W. Tsai, S.H. Gu, Tahui Wang, S. Huang Lu, S.W. Lin, G.S. Yang, J.K. Chen, S.C. Chien, Y.T. Loh, and F.T. Liu, *Proc. Int. Reliab. Phys. Symp*. 404 (2002).

[28] V. Dessard, B. Iniguez, S. Adriaensen and D. Flandre, IEEE Trans. Electron Devices **49** 1289 (2002).

[29] A. Mercha, J. M. Rafi, E. Simoen, E. Augendre and C. Claeys, IEEE Trans. Electron Devices **50** 1675 (2003).