CMOS Nonthreshold Logic (NTL) and Cascode Nonthreshold Logic (CNTL) for High-Speed Applications

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Abstract — **Two new high-speed CMOS logic circuits are proposed and analyzed. One is called the CMOS nonthreshold logic (CMOS NTL), the other the CMOS cascode nonthreshold logic (CMOS CNTL). The CMOS NTL is derived from its bipolar counterpart, which is the fastest bipolar logic, and takes the NOR gate as its basic building gate. It is shown that by applying the nonthreshold principle to CMOS circuits the resultant speed performance can also be highly promoted, but with a sacrifice of dc power consumption. From transient analyses the speed of CMOS NTL is found quite comparable to that of I^2L or even ECL and is about 20–60 percent better than that of the conventional CMOS. Meanwhile, the power–delay product of CMOS NTL is smaller than those of I^2L and ECL and is nearly the same as that of conventional CMOS operated at high frequency. The CMOS NTL was fabricated and measured, and experimental results have verified its performance.**

The nonthreshold principle is then applied to the CMOS cascode structure to form the CMOS CNTL, in which there is a trade-off between speed performance and power dissipation. It is shown from the design of full adders that the CMOS NTL is the fastest of all the static CMOS logic circuits. The speed of the CNTL circuit, although slower than that of the NTL circuit, is still higher than that of the differential split-level logic (DSL) circuit, which is the fastest static circuit proposed so far. The CNTL circuit also has a smaller power–delay product than the DSL circuit.

The CMOS NTL and CNTL circuits can be used along with conventional CMOS circuits, and they are expected to increase the design flexibility and extend the application regime of digital CMOS IC's.

NOMENCLATURE

C_{ox}	Gate oxide capacitance per unit area of a MOS device.
C_S	Shunting capacitor used in an NTL gate.
L	Mask channel length.
$t_{phl(plh)}$	Delay time of a fall (rise) waveform.
$V_{H(L)}$	The logic high (low) output voltage.
$V_{SH(SL)}$	The voltage of the node S when the output of the NTL gate is logic low (high).
$V_{TN(P)0}$	The device threshold voltage of a NMOS (PMOS) device with zero substrate bias.
$V_{TN(P)}$	The device threshold voltage of a NMOS (PMOS) device with nonzero substrate bias.
W	Mask channel width.
$\mu_{n(p)}$	The surface mobility of a NMOS (PMOS) device.
$K_{P(N)}$	$= \frac{\mu_{p(n)}C_{ox}}{2}\left(\frac{W}{L}\right)_{P(N)}$.

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I. INTRODUCTION

CMOS CIRCUITS have played a dominant role in digital VLSI/ULSI circuits, mainly due to low dc power consumption. However, conventional static CMOS circuits suffer from low speed and low packing density. Recently, several new static and dynamic CMOS circuits have been proposed to deal with these problems [1]–[5]. Cascoding the differential NMOS logic trees while using only two cross-coupled PMOS devices as loads is the main approach to saving chip area in those new static circuits [1]–[3]. In new dynamic circuits, however, the domino principle is widely used [4], [5]. Of the various new static logic circuits, the differential split-level logic, DSL [3], derived from cascoded logic [1], has been used in high-speed CMOS complex-gate applications, and has been shown [6] to be the fastest static CMOS logic so far developed. In this study, two new CMOS logic circuits, one called the CMOS nonthreshold logic (CMOS NTL) and the other the CMOS cascode nonthreshold logic (CMOS CNTL), are proposed and shown also to have high speed characteristics. They are compatible in process with conventional CMOS circuits, and are expected to extend the application field of CMOS circuits to higher speed regimes.

The basic circuit structure of the CMOS NTL is derived from its bipolar counterpart [7], [8] as shown in Fig. 1. In the bipolar NTL gate, there are two resistors R_E and R_C which can split the power supply voltage to reduce the output voltage swing. The resistor R_E in the negative feedback path results in a nonthreshold-like dc transfer characteristic. The shunting capacitor C_S is used to reduce the negative feedback effect caused by resistor R_E and

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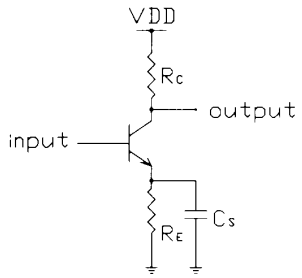

Fig. 1. Bipolar nonthreshold logic gate.

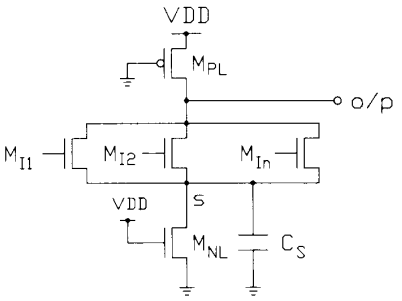

Fig. 2. CMOS NTL multi-input NOR gate.

thus to enhance the operation speed [7]. It is shown that by applying such a nonthreshold principle to CMOS circuits, the resultant speed performance can also be highly promoted, but at the cost of dc power dissipation.

The nonthreshold principle is then applied to a CMOS cascode structure to form CMOS cascode nonthreshold logic (CNTL), in which there is a trade-off between speed performance and power dissipation. However, it is shown that the speed performance of the CNTL circuit is still comparable to that of the DSL circuit. In addition, the power–delay product of the CNTL circuit is shown to be superior to that of the DSL circuit.

In the succeeding sections, basic analyses of CMOS NTL circuits will be performed first. Then, the C_S effect on the switching speed and performance evaluations for the NTL circuits will be discussed. Next, the principle of CNTL and its application will be described. Finally, experimental results will be shown to verify part of the theoretical predictions.

II. Basic Analyses of CMOS NTL Circuits

Fig. 2 shows the circuit configuration of a CMOS NTL NOR gate, which is employed as the basic building gate in CMOS NTL. The input signals are applied to the gates of parallel-connected NMOS transistors M_{NI}'s. The PMOS M_{PL} and the NMOS M_{NL} serve as resistors to split the power supply voltage to reduce the output voltage swing. Nonetheless, the NMOS M_{NL} introduces a negative feedback effect, which will reduce the switching speed. In order to enhance the operational speed, a capacitor C_S can be shunted with M_{NL} between node S and the ac ground node to reduce this effect during switching. Because NOR is a complete logic function, the CMOS NTL circuit can have a straightforward logic construction style and is especially suitable for design automation. It is also possible to obtain NAND structures in NTL forms by stacking several M_{NI}'s. However, it will be shown later that since such NTL NAND circuits have no obvious speed advantages, they are not adopted as the basic NTL circuits.

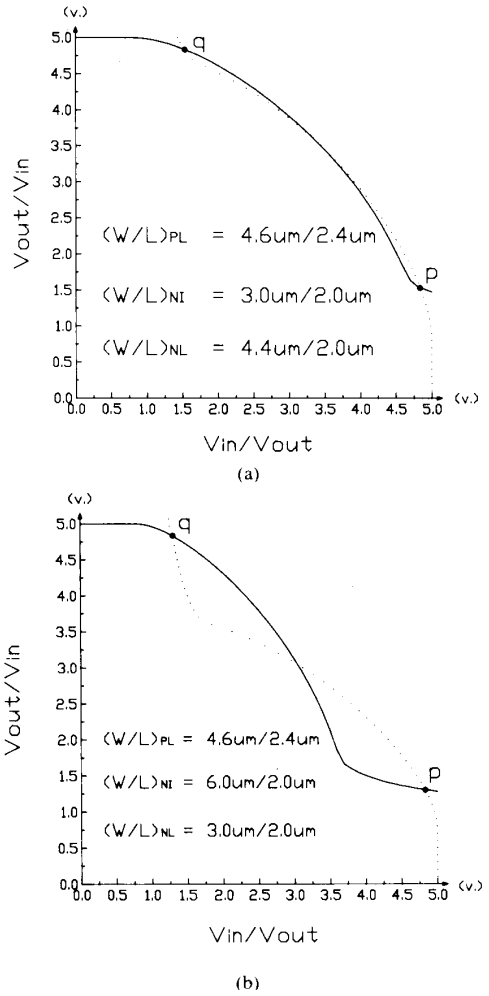

Fig. 3. The dc transfer characteristics of CMOS NTL inverter with device dimensions of (a) $(W/L)_{PL} = 4.6\ \mu m/2.4\ \mu m$, $(W/L)_{NI} = 3.0\ \mu m/2.0\ \mu m$, and $(W/L)_{NL} = 4.4\ \mu m/2.0\ \mu m$; and (b) $(W/L)_{PL} = 4.6\ \mu m/2.4\ \mu m$, $(W/L)_{NI} = 6.0\ \mu m/2.0\ \mu m$, and $(W/L)_{NL} = 3.0\ \mu m/2.0\ \mu m$.

Typical dc voltage transfer characteristics of CMOS NTL inverters are shown in Fig. 3(a) and (b) for two different dimension designs. For the solid lines in these figures, the abscissa stands for the input voltage, and the ordinate for the output voltage, and vice versa for the dotted lines. As may be seen from these figures, the transfer curves are quite smooth. This implies no clear cut at the logic threshold. However, the two cross points p and q guarantee a correct logic operation. This is why the

TABLE I
DEVICE DIMENSIONS AND SPICE-SIMULATED DC CHARACTERISTICS OF VARIOUS CMOS NTL INVERTERS

Cases	M_{PL} (μm)	M_{NI} (μm)	M_{NL} (μm)	V_H (v)	V_L (v)	V_{SH} (v)	V_{SL} (v)	I_H (μA)	I_L (μA)
a	$\frac{4.6}{2.4}$	$\frac{3.0}{2.0}$	$\frac{4.4}{2.0}$	4.83	1.54	0.46	0.04	333.	29.3
b	$\frac{4.6}{2.4}$	$\frac{3.6}{2.0}$	$\frac{2.0}{2.0}$	4.69	1.78	0.81	0.12	325.	52.7
c	$\frac{4.6}{2.4}$	$\frac{5.2}{2.0}$	$\frac{3.0}{2.5}$	4.45	2.05	1.24	0.30	317.	90.6
d	$\frac{4.6}{2.4}$	$\frac{6.0}{2.0}$	$\frac{3.0}{2.0}$	4.83	1.30	0.85	0.07	339.	30.0

name *nonthreshold logic* is adopted. The output voltage swing of the NTL gate is designed to be about 3.5 V for a 5-V power supply, so that good noise immunity can still be retained.

It is seen that the transfer curves of Fig. 3(b) have larger open eyes than those of Fig. 3(a); thus the design of the former has higher noise immunity than that of the latter. Through several simulations, it is found that the dimension design of Fig. 3(b) for the CMOS NTL inverter is stable for a typical process fluctuation range in that there are always two cross points, p and q, in the transfer characteristics.

The first-order current equations are applied to analyze the dc characteristics of CMOS NTL gates and to obtain an approximate dimension design guideline. For a CMOS NTL inverter, the following equations can be obtained:

$$I_H = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{PL}\left[2(V_{DD}-V_{TP0})(V_{DD}-V_L) - (V_{DD}-V_L)^2\right] \quad (1a)$$

$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{NI}\left[2(V_H - V_{SH} - V_{TN})(V_L - V_{SH}) - (V_L - V_{SH})^2\right] \quad (1b)$$

$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{NL}\left[2(V_{DD}-V_{TN0})\cdot V_{SH} - V_{SH}^2\right] \quad (1c)$$

$$I_L = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{PL}\left[2(V_{DD}-V_{TP0})(V_{DD}-V_H) - (V_{DD}-V_H)^2\right] \quad (2a)$$

$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{NI}(V_L - V_{TN} - V_{SL})^2 \quad (2b)$$

$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{NL}\left[2(V_{DD}-V_{TN0})\cdot V_{SL} - V_{SL}^2\right] \quad (2c)$$

where $I_{H(L)}$ is the dc gate current when the output voltage is low (high). Given $(W/L)_{PL}$, $(W/L)_{NI}$, and V_L, and making some approximations, the dc characteristics of the CMOS NTL inverter can be formulated. Detailed derivations are performed in the Appendix.

Table I lists the SPICE-simulated dc characteristics of several CMOS NTL inverters with different dimension ratios among M_{PL}, M_{NI}, and M_{NL}. The transfer characteristics of Fig. 3(a) and (b) correspond to cases *a* and *d*, respectively, of Table I. The device parameters adopted in the simulations are of a 2-μm p-well CMOS process. As compared with the SPICE simulation results, hand calculations using the derived equations have an error within 20 percent if the mobility degradation due to the electric field is considered. Thus, these equations can be used as good design guidelines.

The CMOS NTL can receive the conventional CMOS signal directly, and vice versa. When a conventional CMOS gate comes after a CMOS NTL gate, the dimension design of the conventional CMOS gate is similar to the case where it is connected after a TTL gate, except that the logic transfer voltage should be adjusted to be equal to that of the NTL gate. On the other hand, because the voltage swing of a conventional CMOS gate fully covers that of a CMOS NTL gate, the CMOS NTL can then be connected immediately after the CMOS gate.

III. PERFORMANCE EVALUATIONS FOR CMOS NTL GATES

A. Speed and Power

Because the NMOS M_{NL} results in a negative feedback effect, the switching speed will degrade. By shunting M_{NL} with a capacitor C_S, the negative feedback effect can be reduced during switching, and the speed is improved without an increment of power dissipation. To evaluate the extent of the improvement by increasing the value of C_S, transient simulations on NTL inverters were performed. Since the characteristic waveform [15], [16] is the actual internal voltage waveform within an IC chip, it is more adequate to evaluate the speed performance from the characteristic waveform timing. To obtain the characteristic waveforms and their signal timing, a string of identical gates is excited and the output waveforms at the nodes of intermediate stages are observed. In the following descriptions, the average delay time of a gate is defined as half of the pair delay in the characteristic waveform case. For the characteristic timing, the average delay time of each stage gate is identical, and the delay time through N gates in series will be proportional to N [15], [16].

The simulated rise delay time t_{plh}, the fall delay time t_{phl}, and the pair delay time t_p versus the C_S value are plotted in Fig. 4. The curves are monotonic decreasing. It is seen that the fall delay time t_{phl} is greatly improved by increasing the C_S value slightly from zero because the main effect of C_S is to reduce the negative feedback effect on the series resistance in the discharging path from the output to the ground. On the other hand, the delay rise time t_{plh} is also improved because a faster falling input waveform results in a faster rising output waveform. All the improvements become saturated as the C_S value increases further. It is found that a 0.2–0.25 pF C_S is suitable for the 2-μm CMOS process.

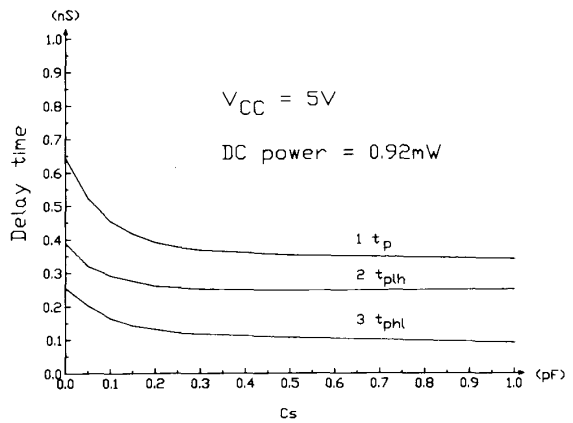

Fig. 4. The effect of reducing the switching delays by increasing the capacitance value of C_S in a CMOS NTL gate.

TABLE II
NORMALIZED DELAY TIMES OF CMOS NTL INVERTERS, NOR GATES, AND NAND GATES WITH DIFFERENT SHUNTING CAPACITANCE VALUES

C_S(pF)	INV_a	INV_d	$NOR2_d$	$NOR3_d$	$NAND2_d$	$NAND3_d$
0	0.72	0.76	0.52	0.44	1.03	1.25
0.2	0.61	0.46	0.31	0.26	0.73	1.06
0.25	0.59	0.44	0.29	0.24	0.69	1.00

From Fig. 4, it is seen that the speed of CMOS NTL is quite comparable to that of I^2L [9] or even ECL [10]. Moreover, the minimum power–delay product of a CMOS NTL gate can be as small as 0.15 pJ for the 2-μm CMOS process. This value is smaller than the typical values of 1.0–1.8 pJ in ECL [10] and 0.6–1.0 pJ in I^2L [9] and is nearly the same as that of 1-μm standard CMOS logic [11] under high-frequency operations. However, unlike the conventional CMOS logic, the CMOS NTL has dc power dissipation.

By using the same CMOS device parameters, the SPICE-simulated delay times of CMOS NTL inverters, NOR gates, and NAND gates are shown in Table II, where all the delay times are normalized to those of conventional CMOS inverters, NOR gates, and NAND gates, respectively. In this comparison, the device dimensions of conventional CMOS circuits are optimally designed so that in a CMOS inverter gate the ratio of the device dimension of the PMOS device to that of the NMOS device has a value near $\sqrt{\mu_n/\mu_p}$ according to [12]. The inverters with a subscript a (or d) in Table II denote that their device dimensions follow the design in case a (or d) in Table I. For both types of NTL inverters with a C_S of 0.25 pF, their delay times are found to be 0.59–0.44 times as small as those of conventional CMOS inverters. It is also found that the efficiency of C_S in enhancing switching speed in case d is higher than that in case a. Besides this, the noise immunity of case d is better than that of case a, as described in the previous section; thus only case d is considered in simulating NTL NOR and NAND gates. In Table II, the number after the gate name denotes the fan-in number, e.g., the two-input NOR gate is denoted by NOR2. It is seen that the speed advantage can still be kept in NTL NOR gates. However, in multi-input NAND cases, NTL circuits do not have a better speed performance than the conventional CMOS NAND gates unless the shunted capacitance is larger than 0.25 pF. This is why only NOR gates are adopted as the basic gates in the developed CMOS nonthreshold logic.

TABLE III
NORMALIZED DELAY TIMES OF CONVENTIONAL CMOS AND CMOS NTL CIRCUITS WITH DIFFERENT FAN-OUT NUMBERS

# of F.O.	Inverters			NOR2 gates		NOR3 gates	
	CMOS	NTLa	NTLd	CMOS	NTLd	CMOS	NTLd
1	1.00	0.59	0.44	1.00	0.29	1.00	0.24
2	1.00	0.50	0.42	1.00	0.32	1.00	0.29
3	1.00	0.43	0.40	1.00	0.35	1.00	0.33
4	1.00	0.40	0.40	1.00	0.38	1.00	0.36

* C_S = 0.25pF in the NTL gates.

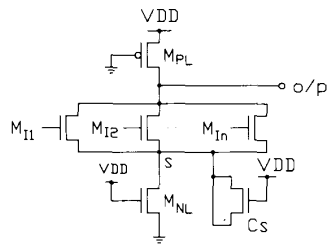

Fig. 5. Circuit diagram of the CMOS NTL multi-input NOR gate, showing that the shunting capacitor C_S is implemented by a MOS transistor.

The fan-out effects of NTL gates are shown in Table III. Here again, the delay times of NTL gates are normalized to those of CMOS gates. Because of smaller input capacitance, the speed advantage can also be found in multi-input, multi-fan-out NTL NOR gates.

B. C_S Realization and Area Comparisons

Two problems are encountered in realizing the shunting capacitor C_S. One is how to realize it; the other is the implementation area. The method to implement it is technology dependent. In a single-metal p-well CMOS process, the method shown in Fig. 5 is found to be the most suitable. In Fig. 5, the C_S is implemented by a MOS transistor. The gate of the MOS transistor is connected to V_{DD}, and its source and drain nodes are tied together and connected to node S in the NTL gate. A large voltage difference between the gate of the MOS transistor and node S makes the transistor work in the linear region to provide a large gate-to-source/drain capacitance, and the very low node voltage swing at node S makes the capacitance stable. In the 2-μm CMOS process, the nominal gate oxide thickness t_{ox} is 250 Å, so an area of about 144 μm^2 is needed to implement a 0.2-pF C_S. It is expected that if an advanced technology such as the trench technology [13] can be used in realizing C_S, the area needed can be greatly

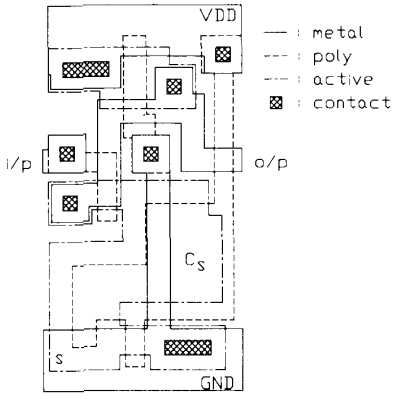

Fig. 6. Layout diagram of a CMOS NTL inverter using 2-μm design rules.

TABLE IV
NORMALIZED LAYOUT AREAS OF CONVENTIONAL CMOS AND CMOS NTL GATES

gates / logic	INV	NOR2	NOR3	NOR4
CMOS	1.00	1.00	1.00	1.00
NTL	1.91	1.04	0.81	0.69

reduced. A layout diagram of an NTL inverter using 2-μm single-metal CMOS design rules with the C_S realized by a MOSFET is given in Fig. 6.

Based upon the same design rules, layout diagrams of various conventional CMOS gates and CMOS NTL gates with C_S equal to 0.25 pF were generated. Layout-area comparisons are shown in Table IV, where the area of each conventional CMOS gate is normalized to unity. It is seen from this table that the layout area of an NTL inverter gate is really larger than that of a conventional CMOS inverter because of the extra area needed for C_S. However, for all gates more complex than a two-input NOR gate, the areas of the NTL gates become compatible to or even less than those of the corresponding conventional CMOS gates, due to the redundant device usage in conventional CMOS gates. Therefore it is realized that the extra area needed for C_S is tolerable for those complex gates.

IV. CNTL AND ITS APPLICATION

From the results in the previous sections, we have seen that CMOS NTL circuits can have a very high speed performance. They are therefore especially suitable for applications requiring high speed. The penalty paid is the high static power consumption. In some applications, there can be a trade-off between speed and power. To achieve such a trade-off, another logic circuit, called the CMOS cascode nonthreshold logic (CNTL) circuit, is developed. The basic idea in implementing the logic is to apply the nonthreshold logic to the recently developed cascode structures [1]–[3] where complex cascoded AOI circuits are permitted.

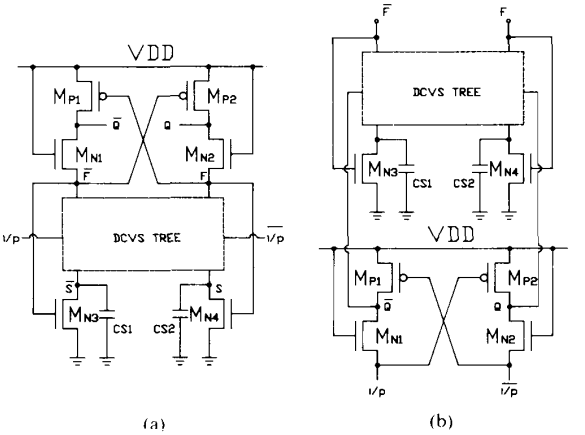

Fig. 7. (a) The basic CNTL circuit and (b) a reconfigurated CMOS CNTL gate.

The CNTL principle is shown in Fig. 7(a), and the basic CNTL gate can be reconfigured as in Fig. 7(b), just as the DSL circuit [3]. The circuit structure is similar to the differential split-level logic (DSL), but the electrical behavior is essentially different. Like all cascode logic circuits, the CNTL has a differential cascode voltage switch (DCVS) tree [1], [3] constructed by NMOS devices. Similar to the DSL circuit, two cross-coupled PMOS devices are used as loads, and two NMOS devices, M_{N1} and M_{N2}, are inserted between the PMOS loads and the NMOS logic tree to split the supply voltage to reduce the output voltage swing. However, the gates of the two NMOS devices M_{N1} and M_{N2} are connected together to V_{DD}, not to a reference voltage V_{ref} as in the DSL circuits. So the voltage reference circuit and the routing area needed for V_{ref} are eliminated. Q and $\overline{Q}$ are two true output nodes, and F and $\overline{F}$ are two pseudo-output nodes which have smaller voltage swings and can be used for wire routing among different gates as in the DSL circuit. The main difference between the CMOS CNTL and the DSL circuit is that the two NMOS devices, M_{N3} and M_{N4}, and the two shunting capacitors, C_{S1} and C_{S2}, are added below the DCVS tree to form the nonthreshold circuit. The shunting capacitors can be implemented by using MOS transistors as in the NTL case. Unlike the basic NTL circuit, which connects the gate terminal of M_{NL} to V_{DD}, the gate terminals of M_{N3} and M_{N4} in the CNTL gate are connected to the nodes F and $\overline{F}$, respectively, to make the layout of Fig. 7(b) more compact. It is found that this connection does not affect the negative feedback effects of M_{N3} and M_{N4}. As expected, the NMOS M_{N3} and M_{N4} can further reduce the output voltage swing, and their negative feedback effects can be reduced by C_{S1} and C_{S2}.

The DCVS trees for the sum and carry outputs of a CNTL full adder are shown in Fig. 8. The device dimensions of the MOS's, M_{P1}, M_{P2}, M_{N1}, M_{N2}, M_{N3}, and M_{N4}, and the simulated dc characteristics are shown in Table V. As shown in this table, the output voltage swings at the nodes Q and $\overline{Q}$ of the CNTL gate are about from 1.5 to

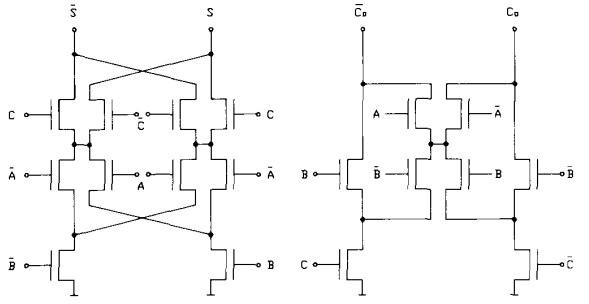

Fig. 8. The DCVS trees required to implement the sum and carry functions of a full adder.

TABLE V
SIMULATED DC CHARACTERISTICS OF A CMOS CNTL FULL ADDER

$(\frac{W}{L})_{P1/2}$ (μm)	$(\frac{W}{L})_{N1/2}$ (μm)	$(\frac{W}{L})_{N\text{-logic}}$ (μm)	$(\frac{W}{L})_{N3/4}$ (μm)
13.2/2.4	7.0/2.0	7.0/2.0	21.0/2.0

V_H (v)	V_L (v)	$V_{F/\bar{F}}$ (v)	$V_{S/\bar{S}}$ (v)	I_H (μA)	I_L (μA)
4.83	1.50	1.3-3.0	0.0-0.9	139	72

TABLE VI
PERFORMANCE COMPARISONS OF THE SUM CIRCUITS OF THE FULL ADDERS IMPLEMENTED BY THE CONVENTIONAL CMOS, THE DSL, THE NTL, AND THE CNTL CIRCUITS

Gates / Performance	CMOS	DSL	NTL	CNTL
Power (mW)	0.3	2.3	8.1	1.3
Delay (ns)	2.5	2.0	1.2	1.7
p·τ (pJ)	0.8	4.6	9.7	2.2

4.8 V, and those at the nodes F and $\bar{F}$ are about from 1.3 to 3.0 V. Just as with the DSL gates, the nodes F and $\bar{F}$ with smaller voltage swings can be used for connection among different gates. Because the maximum voltage drop between the drain and source nodes of all PMOS and NMOS devices is below 3.5 V, for the same processing technology shorter channel length can be used in CNTL gates than in other types of logic gates to improve the switching speed without serious hot carrier effects [3], [14]. Due to the lower voltage swings at the output nodes F and $\bar{F}$, and the nonthreshold technique applied, the speed of the CNTL circuit is expected to be faster than that of the DSL circuits under the same power consumption.

The SPICE-simulated transient results at the sum circuits of the full adders implemented by conventional static CMOS, DSL, NTL, and CNTL are compared in Table VI with all C_S's = 0.25 pF in CMOS NTL and CNTL gates. The sum circuit implemented by the CMOS NTL is a three-level logic circuit. From Table VI, the speed of the CMOS NTL adder is seen to be the fastest of all the implemented adders, and that of the conventional CMOS adder is the slowest. The speed of the CNTL adder, although slower than that of the NTL adder, is still higher than that of the DSL adder. Moreover, the power dissipation of the CNTL circuit is nearly half that of the DSL circuit. Thus, the CNTL circuit has a smaller power–delay product than the DSL circuit.

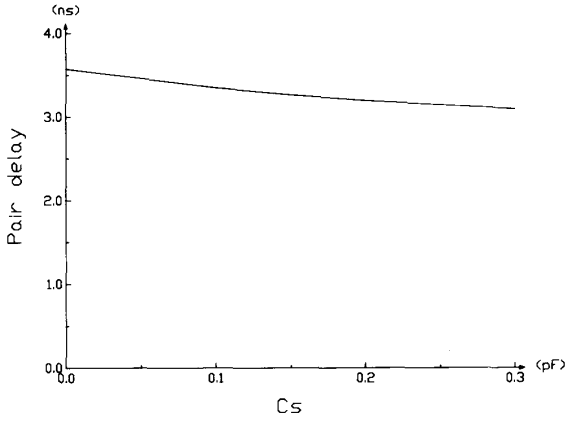

Fig. 9. The effect of an increasing C_S value on the speed performance of the CMOS CNTL gate.

It can be seen from Table VI that the NTL circuit is faster than the CNTL circuit. However, the CNTL circuit has a much smaller dc power dissipation due to the use of the cross-coupled loads and the complex cascode AOI circuits. Generally, the NTL circuits and the CNTL circuits have different features to meet different requirements or specifications.

The C_S effect on the speed of CNTL gates is shown in Fig. 9. The shunting capacitor can also reduce the negative feedback effect and improve the speed. However, its effect is not so significant as in NTL gates because of the NAND/AND circuit structure used in CNTL gates. A capacitance value of 0.2–0.25 pF is selected for the 2-μm CMOS technology as in the NTL gates.

V. EXPERIMENTAL RESULTS

Some experiments were performed to verify part of the simulated results. Several strings of 71-stage ring oscillators were designed and fabricated to measure the average delay time of NTL inverters and two-input NTL NOR gates using a standard 2-μm single-metal p-well CMOS process. For comparisons, similar test structures were also designed and fabricated for conventional CMOS inverters and two-input NOR gates. The C_S values in the fabricated NTL gates are all chosen to be 0.25 pF. A chip photomicrograph is shown in Fig. 10. The measured dc transfer characteristic of the fabricated NTL inverter is shown in Fig. 11, which is very close to the simulation results. The measured output waveforms of the fabricated ring oscillators with two-input NTL NOR gates are shown in Fig. 12, and the measured timing data are listed in Table VII. It is seen

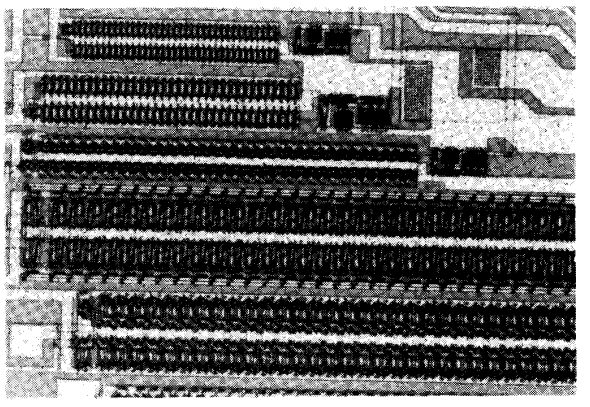

Fig. 10. Photomicrograph of the fabricated ring oscillators made of CMOS NTL inverters or NOR gates.

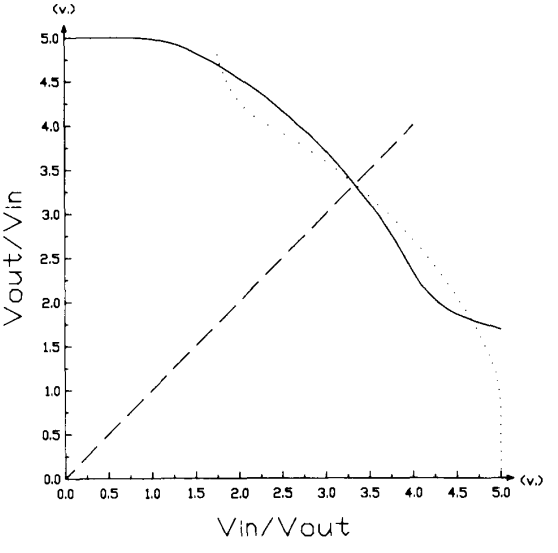

Fig. 11. The measured dc transfer characteristics of the fabricated CMOS NTL inverter.

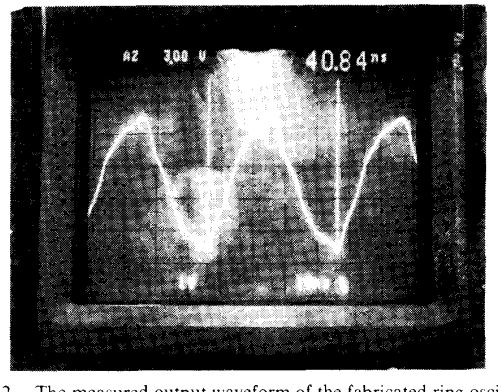

Fig. 12. The measured output waveform of the fabricated ring oscillator made of two-input CMOS NTL NOR gates.

TABLE VII
MEASURED DELAY TIMES OF FABRICATED CONVENTIONAL CMOS GATES AND OF CMOS NTL GATES FOR COMPARISON

Gates / Performance	INV		NOR	
	CMOS	NTL	CMOS	NTL
Delay time (ns)	0.63	0.19	0.91	0.25
NTL/CMOS	30%		27%	

that the measured delay time of the NTL inverter is about one-third that of the conventional CMOS inverter, and the delay time of the NTL NOR gate is about one-fourth that of the conventional CMOS NOR gate. These experimental observations are all consistent with the theoretical predictions described in Section III.

VI. CONCLUSIONS

In this paper, two novel static CMOS logic circuits are proposed, analyzed, and partly chip-tested. First, the CMOS nonthreshold logic (CMOS NTL) is shown to be the fastest logic of the various static CMOS logic circuits. It has a simple logic construction style. The other new CMOS logic, the CMOS cascode nonthreshold logic (CMOS CNTL), is also shown to have a high speed performance. It offers a suitable trade-off between the high speed characteristics of the NTL circuits and the low power characteristics of the cascode CMOS circuits. We believe that these two new high-speed logic circuits will extend the application regime of digital CMOS IC's.

APPENDIX

Given K_{PL}, K_{NI}, and V_L, K_{NL}, V_H, V_{SH}, and V_{SL} can be solved from the dc current equations in (1) and (2). Making a reasonable assumption that $(V_{DD}-V_H)^2 \to 0$ in (2), then

$$V_H = V_{DD} - \frac{K_{NI}(V_L - V_{TN})^2}{2\cdot K_{PL}(V_{DD}-V_{TP})}. \tag{A1}$$

Substituting (A1) into (1) and solving for I_H and I_L, we have

$$I_H = K_{PL}\cdot\left[2(V_{DD}-V_{TP})(V_{DD}-V_L)-(V_{DD}-V_L)^2\right] \tag{A2}$$

$$I_L = K_{NI}\cdot(V_L - V_{TN})^2 - \frac{K_{NI}^2(V_L-V_{TN})^4}{4\cdot K_{PL}(V_{DD}-V_{TP})^2}. \tag{A3}$$

From (2) and (A3), we have

$$V_{SL} = V_L - V_{TN} - \sqrt{(V_L-V_{TN})^2 - \frac{K_{NI}(V_L-V_{TN})^4}{4\cdot K_{PL}(V_{DD}-V_{TP})^2}}. \tag{A4}$$

Substituting (A3) and (A4) into (2c) and assuming $V_{SL}^2 \to$

0, K_{NL} can be solved as

$$K_{NL} = \frac{I_L}{2V_{SL}(V_{DD} - V_{TN})}. \quad \text{(A5)}$$

Then, substituting (A2) and (A5) into (1c) and solving for V_{SH}, we have

$$V_{SH} = V_{DD} - V_{TN} - \sqrt{(V_{DD} - V_{TN})^2 - (I_H/K_{NL})}.$$

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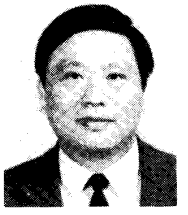

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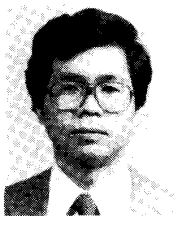

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