國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

一個具正交相位和增益誤差校準之 5-GHz 直接降頻射頻接收器

A 5-GHz Direct Conversion Receiver with I/Q Phase and Gain Error Calibration

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中華民國九十三年十月

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摘要

近年來無線區域網路如 IEEE 802.11a 和 HIPER LAN 的發展，吸引許多相關方面研究其傳送接收器。隨著系統晶片整合的時代來到，對低成本射頻傳送接收器的需求更為強烈。而採用直接降頻架構的寬頻無線傳送接收器具有需求較少外部元件的優勢，因此能達到低成本的目標。這架構因此吸引本篇論文研究。本篇論文描述設計一個適用於無線區域網路應用之 5GHz，具可變增益直接降頻接收器。而本地振盪器之頻率定為所欲接收射頻頻率之三分之二來避免功率放大器所造成的拉起現象以及本地振盪器和射頻信號接收端的交互作用。此外，還提出增益和相位誤差校準技巧來補償正交信號路徑上的不匹配情形。測量到用來評估正交誤差之鏡像排拒比為 28.25 分貝。射頻前端電路之轉換增益根據輸入信號功率具可切換高低來配合下一級之動態操作範圍。它可達到在高增益模式下具有轉換增益 28.2 分貝而在低增益模式下具有轉換增益 11.6 分貝。整體雜訊指收為 9.4 分貝而線性度為-6.8dBm(在有輸出緩衝器情況下)。籍由所提出正交校準方法，所測量到的相位誤差小於 0.6 度以及增益誤差小於 0.2 分貝。晶片面積為 1.64mm^2 和在 1.8V 的供應電壓下功率消耗 37.25mW。

此外，還實現一個操作在所欲接收頻帶三分之二的頻率合成器。設計之重點主要在於最佳化相位雜訊效能，和利用所提出的具電流匹配之電荷充放器有效地降低參考信號雜頻。晶片面積為 1.06㎜^{2} 以及在 1.8V 的供應電壓下功率消耗 14.4mW。

A 5-GHz Direct Conversion Receiver with I/Q Phase and Gain Error Calibration

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Abstract

Wireless Local Area Networks (WLANs) based on IEEE 802.11a and HIPER LAN have drawn transceiver research efforts and turn widely deployed in recent years. With the coming of soc era, a low cost RF transceiver is in strong demand. For wide band wireless transceiver direct conversion architecture is a superior candidate for fewer external required components, thus low cost design goal can be achieved. This activates the research of this work. This thesis describes the design of a 5GHz, variable gain, and direct conversion receiver for wireless LNA application. The LO frequency is set to be 2/3 of required RF frequency to avoid PA pulling and LO-RF interaction. Furthermore, gain and phase error calibration techniques are proposed to compensate mismatches in the I/Q signal path. Measured image-rejection ratio for evaluating I/Q error is about 28.2dB. The conversion gain of the RF front-end is variable to slide the available dynamic range of the following stages based on the input power level. It performs a conversion gain of 28.2 dB in the high gain mode and

11.6 dB in the low gain mode. The overall noise figure (SSB) is 9.4dB and IIP3 is about -6.8dBm (with output buffer). By means of I/Q calibration techniques, the measured phase error is less than 0.6° and gain error is less than 0.2 dB. It consumes chip area of 1.64mm^2 and power of 37.25mW at 1.8V supply voltage.

Additionally, a frequency synthesizer operating at 2/3 of required RF frequency has been implemented. The design issue is to optimize the phase noise performance and effectively reduce reference spur from mismatches by employing proposed current-match charge pump. It consumes chip area of 1.06mm^2 and power of 14.4mW at 1.8V supply voltage.

誌謝

回顧快兩年的碩士求學生涯，在這段時光裡充滿了許多回憶，一點一滴在心中，將是我這生中最珍貴的寶藏。

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李宗霖

九十三年十月

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Chapter 1

Introduction

1.1 Background

As increasing demand for high-speed wireless communication and high-quality multimedia application, wireless local-area network (WLAN) market has grown fast. The IEEE 802.11a standard [1], which operates in the 5-GHz unlicensed national infrastructure (UNII) band, supports higher data rates up to 54Mb/s compared with maximum data 11Mb/s offered by the 802.11b standard. It provides for orthogonal multiplexing (OFDM) modulation with 52 subcarriers in a channel bandwidth of 16.6MHz (channel spacing of 20MHz). The data is modulated with BPSK, QPSK, 16QAM, or 64QAM, and further mapped into 48 subcarriers (4 subcarriers are for pilot signals).

These advantages come at a cost, as OFDM-based systems pose significant implementation challenges requiring low in-band noise, high linearity, and accurate quadrature matching [2]. Besides, the use of 64QAM modulation requires a high SNR of 26dB, which is substantially greater than that required by the FSK modulation in Bluetooth and the QPSK modulation in 802.11b. This high SNR translates to more stringent phase noise requirement for the synthesizer and tight quadrature signal matching constraints for both the transmitter and receiver [3]. To realize the low-cost

implementation, the CMOS integrated receiver is desirable for its inexpensive price.

Implementation CMOS RF receiver using direct-conversion architecture has many advantages, such as fewer external filters (cost down), less internal components (reduce power dissipation), and highly integration (small form factor). However, this architecture accompanies with some problems, such as dc offset, I/Q mismatch, even-order distortion, flicker noise, and LO leakage , which described in detail in ref [4]. Therefore, in the past years, design issues in this architecture become popular and active researches.

1.2 Motivation

The drawbacks in direct conversion receiver architecture mentioned before can be alleviated and improved by the following design techniques.

1.2.1 Optimum between gain, noise figure, and linearity

In the RF frond-end design (LNA + Mixer), providing high conversion gain will get better overall noise figure, but degrade whole linearity. Contrarily, providing low conversion gain will promote whole linearity, but increase overall noise figure. Therefore, if conversion gain of the frond-end is programmable, as shown in Fig1.1, it is able to alleviate tradeoff between gain, noise figure, and linearity performance.

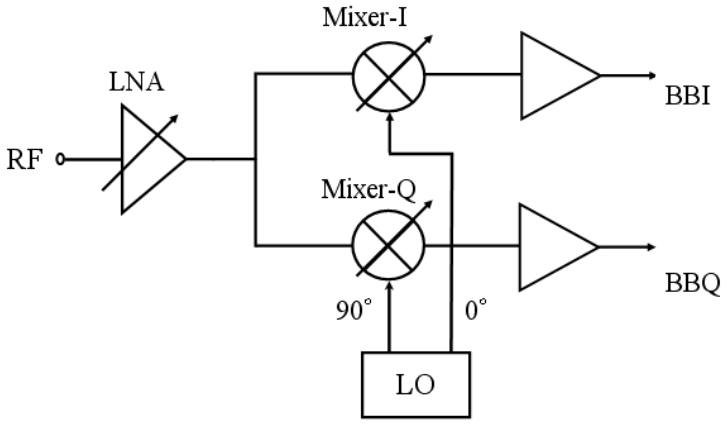


Fig. 1.1 Programmable conversion gain in the front-end design

1.2.2 Avoid VCO pulling for transceiver integration

Combining direct-conversion receiver with direct-conversion transmitter accompanies some impairment, such as pulling effects by the on-chip PA, and large in-band LO leakage. Thus, design challenge in the direct conversion architecture is minimization of VCO pulling from on-chip PA and LO leakage. In order to alleviate these impairments, the VCO is operated at two-thirds of the required LO frequency to avoid VCO-pulling and reduce LO-RF interaction. The required LO generation is shown in Fig1.2 [5].

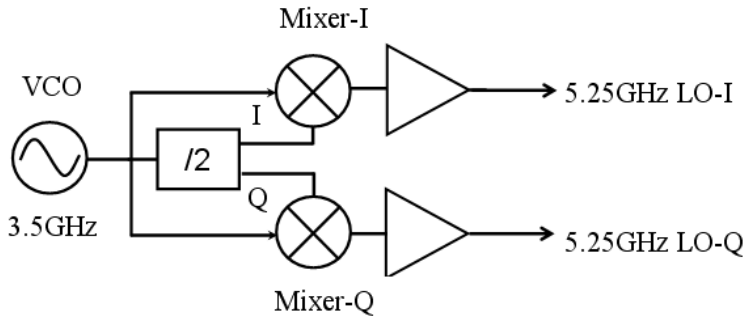


Fig. 1.2 LO generation architecture [5]

1.2.3 Provide precise I/Q output

As shown in Fig1.1, for phase and frequency modulation schemes, a homodyne receiver has to incorporate quadrature mixing. The phase errors in qradrature LO generation, and mismatches between the amplitudes of the I/Q signals corrupt the down converted signal constellation, thereby raising the bit error rate. As shown in Fig1.3, all stages in the I/Q paths contribute gain and phase errors.

High order QAM-OFDM modulation requires tightly matched phase and gain in I/Q signal path to avoid degradation of the overall EVM. Thus, in order to get higher SNR in the receiving signals and better EVM (error vector magnitude) for transmitter, I/Q mismatch problem in the implementation of CMOS RF receiver must be

overcome. It comes from the process, voltage, temperature variations and transistors, passive components (L, C) mismatch. To compensate I/Q mismatch, some analog and digital calibration have been proposed [4]. Recently, a LC oscillator with poly-phase filter employing self-calibrated technique [6] and a quadrature LC oscillator using tail current source control for phase error calibration [7] have been presented. However, the calibrated I/Q phase error by their proposed mechanism is about less than 2°. However, system simulation shows that an I/Q mismatch of 1.5° / 0.2 dB and an integrated phase error of 1°rms are required [8]. Thus, phase and gain error calibration techniques are proposed to compensate gain and phase error in the receiving I/Q signal paths. By means of these techniques, the phase mismatched is reduced to less than 0.8° and gain error less than 0.2dB. Table 1.1 lists the design target of our receiver design.

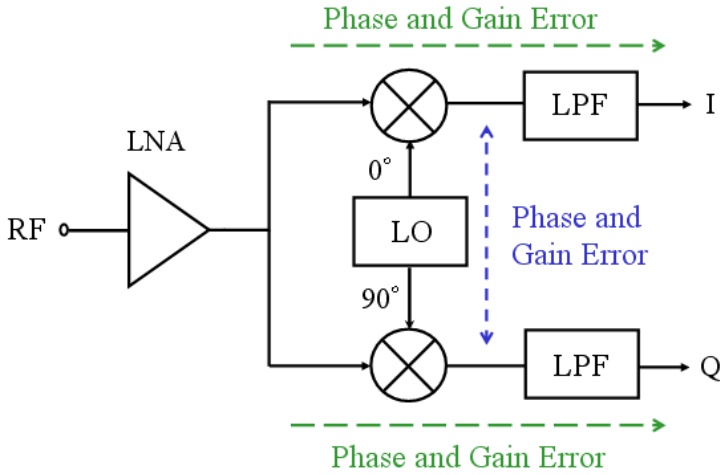


Fig. 1.3 I/Q mismatch contributions by various stages

Table 1.1 Design target

Technology	TSMC 0.18 um CMOS
Modulation / Data rates	64QAM / 54Mbps
Supply Voltage	1.8 V
LNA gain	10 ~ 22 dB
LNA NF	< 2.5dB
Mixer gain	6 ~ 12 dB
Mixer NF	< 15 dB
Total noise figure	< 7dB
Max. gain	34 dB
1dB point	-26dBm
IIP3	- 16dBm
I-Q path amplitude / phase error	< 0.2dB / < 0.8°
Phase noise	-113 dBc/Hz @ 1MHz

1.3 Organization

In this thesis, chapter 2 describes how to realize the proposed I/Q calibration generator and LO generation architecture. The detail operation theory and improved performance are presented, and verified by chip implementation. Chapter 3 describes the direct-conversion front-end receiver design. The components employed in the receiver, such as LNA (low noise amplifier), down-conversion mixer, VCO, are also discussed. Chapter 4 describes the implementation of a frequency synthesizer chip with low phase noise and low reference spur. The design flow and performance optimum are presented. Finally, Chapter 5 describes the conclusions and future works.

Chapter 2

Quadrature LO Generator with I/Q Mismatch Calibration

Direct down-conversion from 5GHz requires quadrature LO generation at the RF carrier frequency, which may result in large gain and phase mismatches. Other significant problems include sensitivity to flicker noise and pulling of the VCO by the external or on-chip PA. In addition to these architecture-related nonidealities, higher order QAM-OFDM modulation requires tightly matched I/Q signal path on both transmit and receive side to avoid degradation of the overall EVM.

2.1 Phase-calibrated LO Generator

In this section, we present the phase-calibrated LO generator. In our frequency planning, a “fractional VCO” is adopted in which the desired RF frequency is 1.5 times higher than the VCO frequency [5]. Fig 2.1 reports an LO generation scheme that consists of a VCO operating at two-thirds of the LO frequency and a divide-by-2 divider generating quadrature outputs at one-third LO frequency. Besides, additional phase-calibrated LO generators are employed and combined with up-conversion mixers in LO I/Q path for phase error calibration.

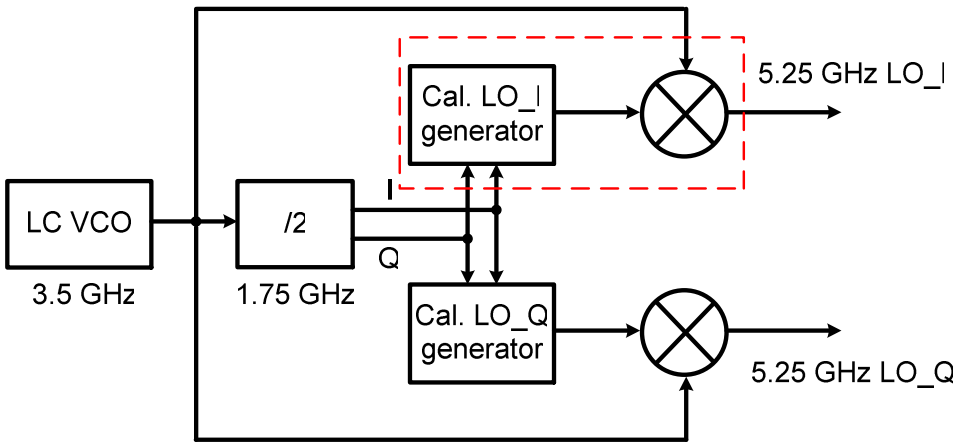


Fig. 2.1 Calibrated LO generator architecture

As the VCO operates at two-thirds of the LO frequency (3.5GHz), this scheme can effectively avoid pulling and reduce LO-RF interaction. However, the generated LO signal has strong lower sideband at one-third of LO frequency, which is roughly 1.75GHz, a highly populated frequency band where high-power transmitters exist. To suppress the lower side band image at the LO I/Q output, the up conversion mixer utilizes LC tanks as the output load.

Assume vector I and Q are not orthogonal, as is illustrated in Fig 2.2, a modified quadrature phase Q' can be generated by summing up Q with a compensated vector –I. Once the polarity and weighting factor of the compensation can be digitally controlled, a precise I/Q signal can be generated by eliminating their phase error. Fig 2.3 depicts the phase-calibrated LO generator, which performs as an up conversion mixer with phase compensation capability. The divider output I/Q signals at 1/3 f_{LO} are applied to the transconductance stages (M1-M6) of the mixer, while the VCO output at 1/3 f_{LO} are applied to commutating stages (M7-M10) of the mixer. The vector compensation is achieved by I/Q phase current mixing.

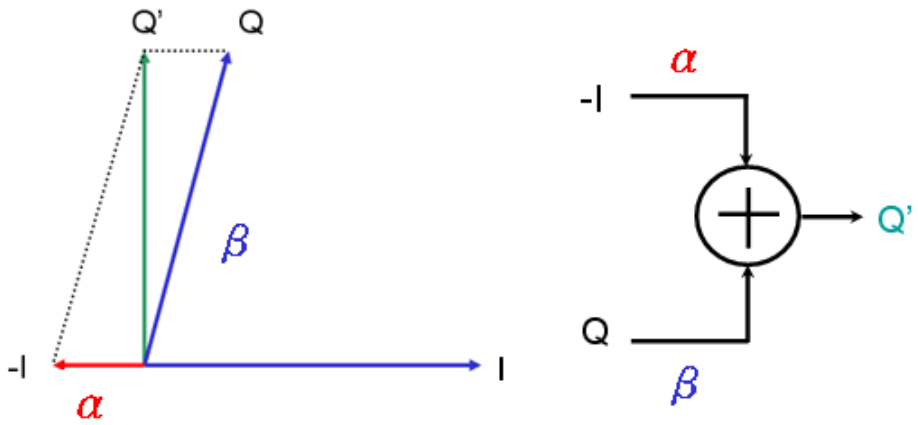


Fig. 2.2 Phase compensation concept

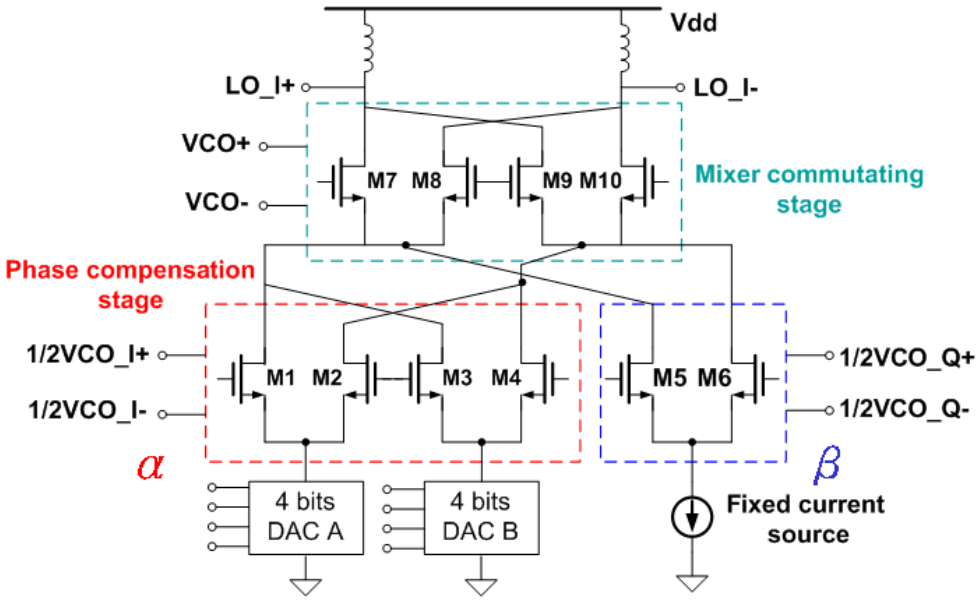


Fig. 2.3 Phase-calibrated LO generator

Assume

$$\alpha \mathrm{I} = (\alpha 1)\mathrm{I} - (a2)\,\mathrm{I}$$

The compensated quadrature vector (Q') can be derived as

$$\mathrm{Q}' = \alpha \mathrm{I} + \beta \mathrm{Q}$$

Here α1 and α2 are controlled by 4 bits DAC A and B respectively. Thus the

polarity and magnitude of the compensated current can be digitally programmed to null out the phase error.

2.2 Phase Calibration Verification

To evaluate the performance of the calibration LO I/Q generator, we must measure the phase and gain errors. But it is very hard to measure those parameters of quadrature phase outputs at such high frequency. To get information about phase error, we can use the image rejection down-conversion mixers to mix down LO I/Q signals with accurate quadrature RF I/Q signals and measure the image rejection ratio (IRR). Specific relations exist between gain error, phase error, and image rejection ratio.

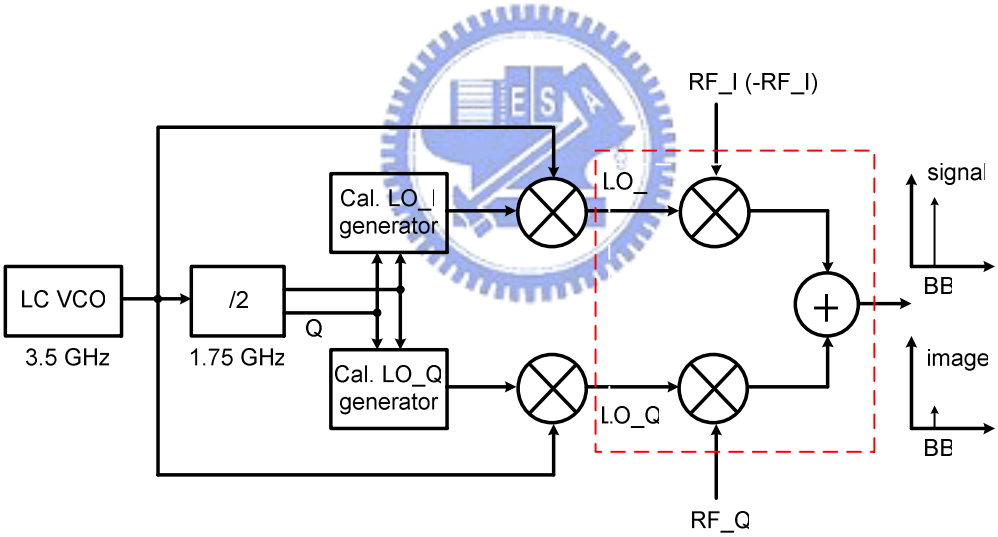


Fig. 2.4 Phase compensation concept

Assume we generate and inject signals at two frequencies: ω_{LO}, ω_{RF} respectively, then mix them together. Parameter ε represents the magnitude error of LO I/Q signals and θ represents phase error of them.

$RFI \times LOI + RFQ \times LOQ$:

$$\cos(\omega_{RF}t)\times\cos(\omega_{LO}t)+\sin(\omega_{RF}t)\times(1+\varepsilon)\sin(\omega_{LO}t+\theta) \tag{2.1}$$

$$\approx \frac{1}{2}[1+(1+\varepsilon)\cos\theta]\times\cos(\omega_{RF}-\omega_{LO})t+\frac{1}{2}[1-(1+\varepsilon)\cos\theta]\times\cos(\omega_{RF}+\omega_{LO})t$$

wanted signal

$-RFI \times LOI + RFQ \times LOQ$: (2.2)

$$-\cos(\omega_{RF}t)\times\cos(\omega_{LO}t)+\sin(\omega_{RF}t)\times(1+\varepsilon)\sin(\omega_{LO}t+\theta)$$

$$\approx -\frac{1}{2}(1-(1+\varepsilon)\cos\theta)\times\cos(\omega_{RF}-\omega_{LO})t+\frac{1}{2}(1+(1+\varepsilon)\cos\theta)\times\cos(\omega_{RF}+\omega_{LO})t$$

image signal

When we mix RFI and RFQ with LOI and LOQ respectively, we get down-conversion wanted signal at frequency of ω_{RF} - ω_{RF}, as indicated in equation (2.1). Inversely, when we mix –RFI and RFQ with LOI and LOQ respectively, we get down-conversion image signal at frequency of ω_{RF} - ω_{RF}, as indicated in equation (2.2). However, up-conversion signals at frequency of ω_{RF} + ω_{RF} after mixing will be filtered by the band-limited circuits, such as down conversion mixers, output buffers, and low pass filters. Image rejection ratio (IRR) is magnitude ratio between them, which is listed in equation (2.3).

$$IRR = 20Log\sqrt{\frac{(1+\varepsilon)^2+1+2\varepsilon\times\cos\theta}{(1+\varepsilon)^2+1-2\varepsilon\times\cos\theta}} \tag{2.3}$$

By using MATLAB, we can show relations between gain error, phase error, and image rejection ratio in Fig 2.5 and Fig 2.6.

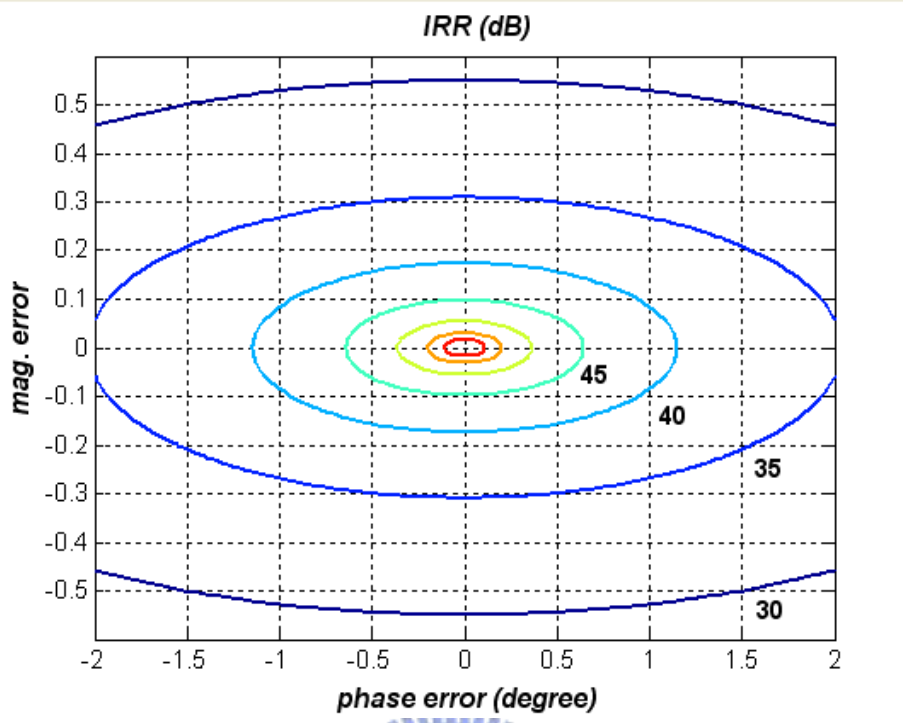


Fig. 2.5 Relations between IRR, phase error, and magnitude error

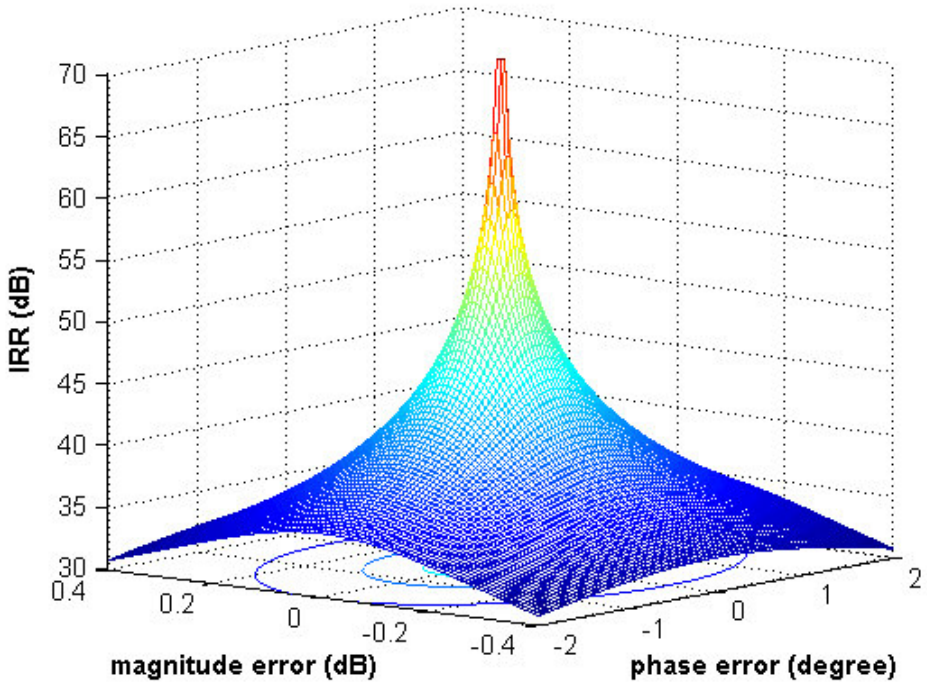


Fig. 2.6 Relations between IRR, phase error, and magnitude error (3D)

From IEEE 802.11a specification, we get that EVM has to be less than -25dB for good data constellations. From hand calculation, EVM can be expressed as:

$$EVM \approx 20Log\frac{\sqrt{(1+\varepsilon)^2+1-2\varepsilon\times\cos\theta}}{\sqrt{2}} < -25dB \tag{2.4}$$

According to equation (2.3) and (2.4), it reveals that IRR has to be greater than 28dB to achieve specification. If I/Q mismatch of 0.8˚ and 0.2dB can be achieved by our proposed phase -calibrated mechanism, IRR will be greater than 37.4dB and EVM will be less than -34.3dB. By MATLAB, we can show relations between magnitude error, phase error, and EVM as shown in Fig 2.7.

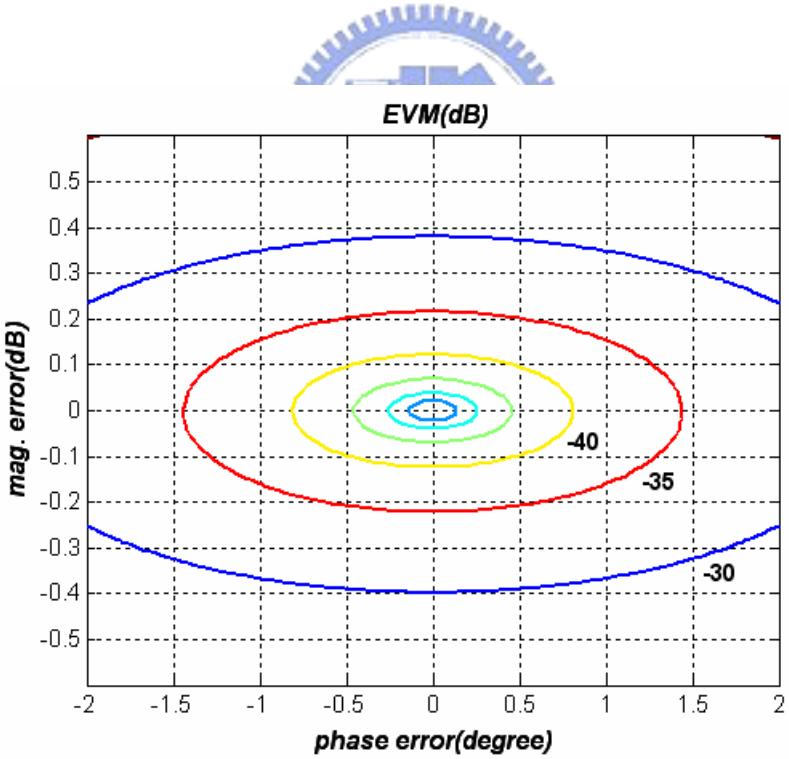


Fig. 2.7 Relations between EVM, phase error, and magnitude error

In order to determine the maximum phase compensation, Monte Carlo simulations have been employed for analyzing the maximum I/Q phase error from component mismatches. As shown in Fig 2.8, Monte Carlo simulations (50 times) using Gaussian distribution show that maximum phase error would achieve about 2.2˚ in the presence of 10% and 6-sigma device channel length mismatches. Furthermore, as shown in Fig 2.9, under more serious conditions, Monte Carlo simulations (50 times) using uniform distribution show that maximum phase error would achieve about 5.9˚ in the presence of 10% and 6-sigma device channel length mismatches. Thus, according to mention before, the calibrated LO I/Q generators have to be designed to have capability of compensating maximum phase error about 6˚. In our phase compensation plan, I/Q phase error less than 10˚ can be compensated to less than 0.8˚.

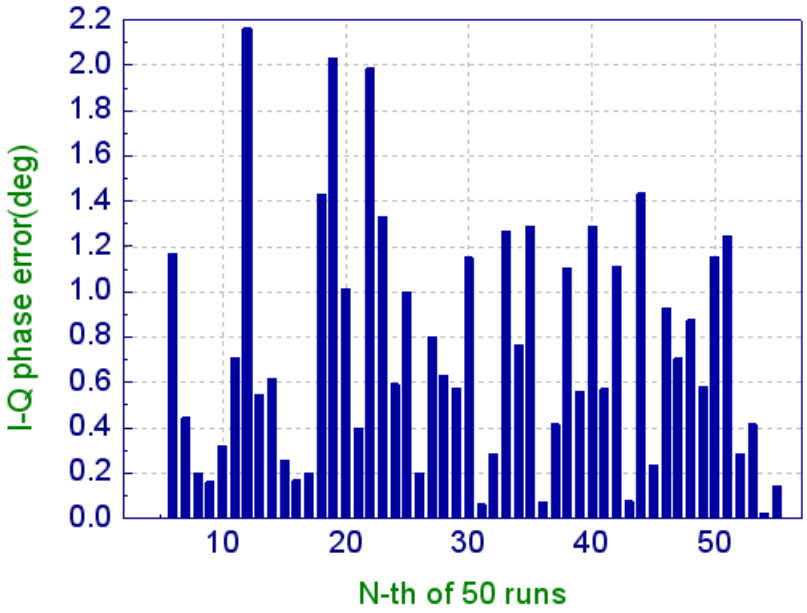


Fig. 2.8 Monte Carlo simulations using Gaussian distribution

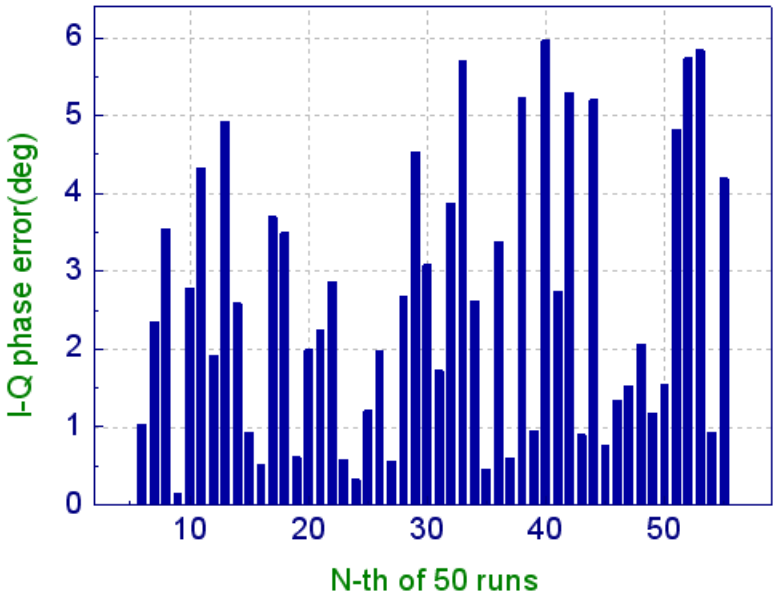


Fig. 2.9 Monte Carlo simulations using uniform distribution

The DAC_A and DAC_B in Fig 2.3 are current-mode D/A converters and controlled by 4-bit binary-weighted current sources, as shown in Fig 2.10. The currents through DAC_A and DAC_B are proportional to their bit numbers respectively and total current through them are constant. In this work, the sum of bit numbers of DAC_A and DAC_B is a constant value, 16. By assigning bit number of DAC_A and DAC_B, I/Q phase compensation polarity and magnitude can be digitally controlled. As I/Q phase error is zero, DAC_A and DAC_B have the same current and

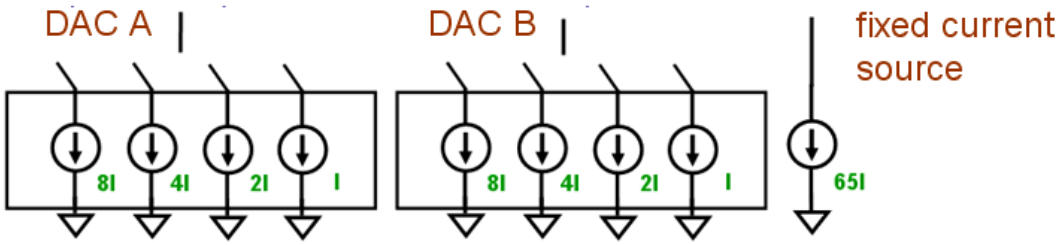


Fig. 2.10 Monte Carlo simulations using Gaussian function

bit number, 8, so phase-I signals for compensation in Fig. 2.3 are canceled through cross couple pairs, M1-M4. And from roughly hand calculation and simulation result, current ratio under minimum DAC control is (2I / 65I), which results in I/Q phase variation about 1.54°. And current ratio under maximum DAC control is (15I / 65I) , which results in I/Q phase variation about 9.58°. I/Q phase change versus DAC control step (the difference between bit number of DAC_A and DAC_B) is shown in Fig. 2.11.

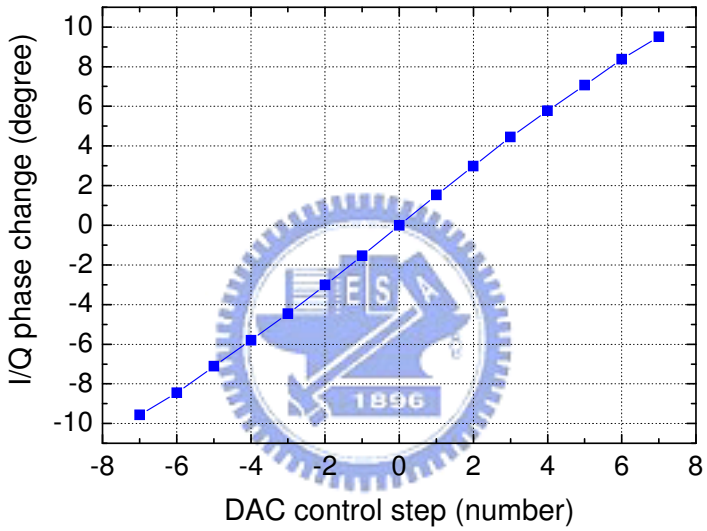


Fig. 2.11 I/Q phase change versus DAC control step

2.3 Gain-calibrated Down-conversion Mixer

To compensate the gain error at signal I/Q path, receiver frond-end (LNA + Mixer) is designed to provide fine gain control in I/Q paths conversion gain. However, the gain of LNA is the same for signal I/Q path. Therefore, the down-conversion mixers at signal I/Q path are suit to provide this function. The simplest way is to make changes in resistor load of mixers. Fig 2.12 shows that resistor load adjusted by switching sw4 and sw5. As sw4 and sw5 turn on, resistor load is “R + 5R”. As sw4

turns off and sw5 turns on (or inversely), resistor load is "(5R/4) + 5R", mixer gain increases 0.4dB. As sw4 and sw5 turn off, resistor load is "(5R/3) + 5R", mixer gain increases about 0.7dB. Therefore, if signal I/Q path exists gain error less than 1dB, after gain error calibration, gain error will be less than 0.2dB.

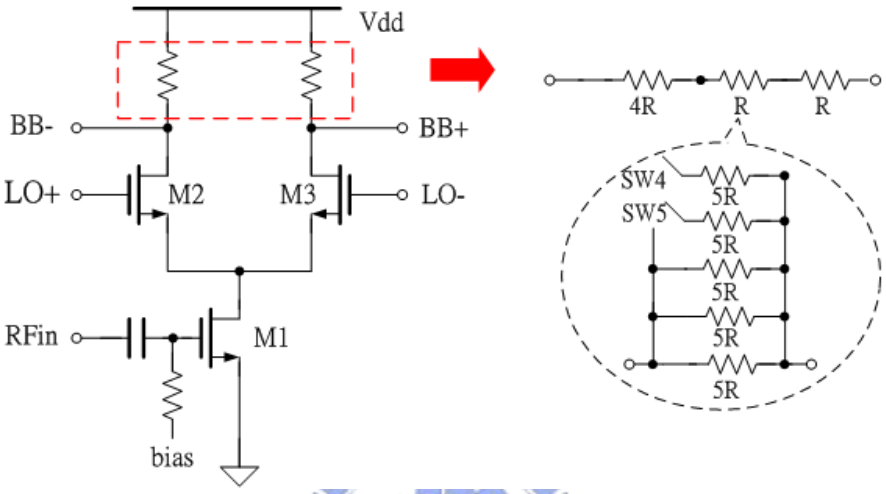


Fig. 2.12 Resistor Load is fine controlled by sw4 and sw5

2.4 Circuit Realizations

In this section, we will discuss other block designs in Fig 2.4, such as complementary VCO, divide-by-2 divider, and source couple pair adder.

2.4.1 Complementary VCO

In this work, our VCO design adopted differential complementary cross-coupled LC oscillator architecture, as shown in Fig 2.13. Symmetric inductor and accumulation-mode varactor is used for inductor and capacitance of VCO. Complementary cross-coupled architecture saves more power than only nmos or pmos cross-coupled architecture because negative resistance becomes double. Also, its phase noise performance can be further improved by means of the complementary architecture thanks to symmetric output waveform [9].

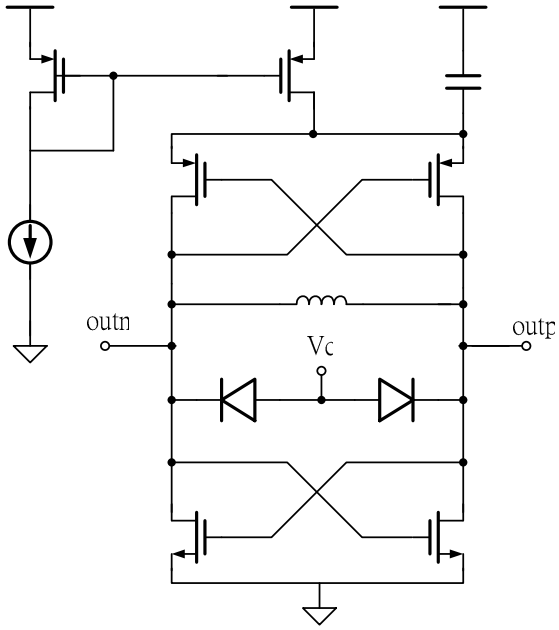


Fig 2.13 Complementary cross-coupled VCO

2.4.2 Divide-by-2 divider

Fig 2.14 shows a divide-by-two divider schematic utilized to generate the quadrature LO signals. The circuit is realized as two master-slave D flip-flops configured in a negative feedback loop. Each flip-flop consists of a differential amplifier followed by a regenerative cross coupled pair. Thus dividing signals with I/Q phases can be derived at the divider outputs. The detailed schematic of MS-D-FF is shown in Fig 2.15. Typical device mismatches result in phase imbalances as large as 5° [10].

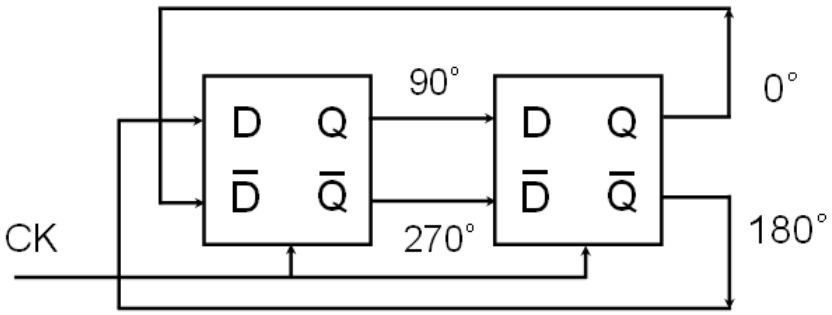


Fig. 2.14 Divide-by-2 divider configuration

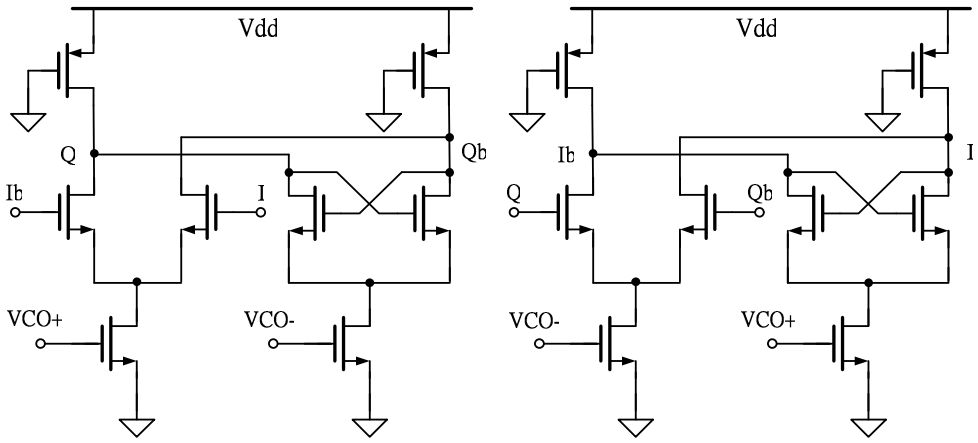


Fig. 2.15 Divide-by-2 divider

2.4.3 Source Couple Pair Adder

Fig 2.16 shows a source couple pair adder schematic. Since RF I/Q signals mix with LO I/Q signals respectively, then down convert to baseband signals (150k ~ 8.3MHz) and added up through source couple pair adder. If down-conversion signals were wanted signals, they would be sum up. However, if down-conversion signals were image signals, they would be canceled out.

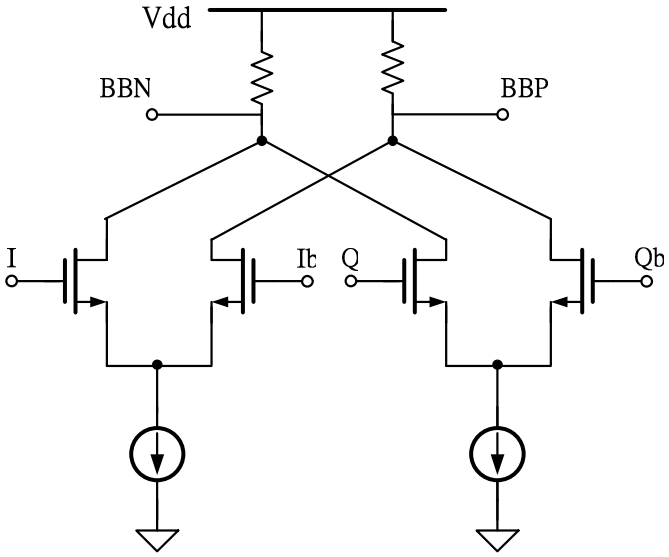


Fig. 2.16 Source couple pair adder

2.5 Simulation result

Transient response of each circuit block is shown in the following. The simulation results of VCO differential output waveforms are shown in Fig 2.17. Quadrature outputs of divide-by-2 divider are shown in Fig 2.18. The mixing up-conversion quadrature LO waveforms through phase-calibrated LO generator are shown in Fig 2.19. Fig 2.20 shows that simulation result of down-conversion wanted signal at 20MHz. On the other hand, Fig 2.21 shows that simulation result of down-conversion image signal at 20MHz.

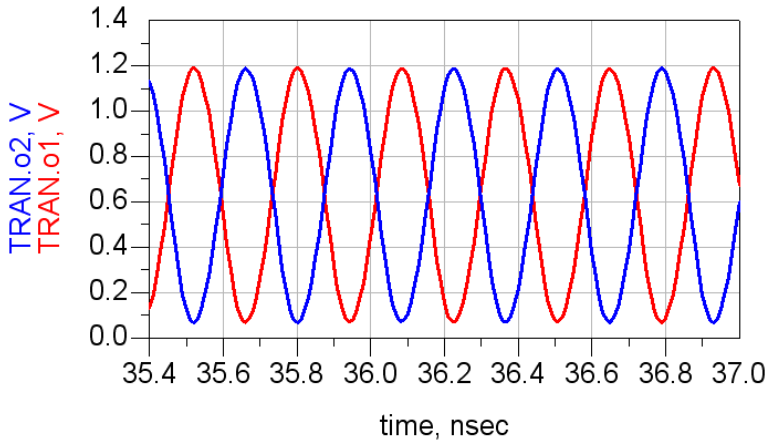


Fig. 2.17 VCO differential output waveforms

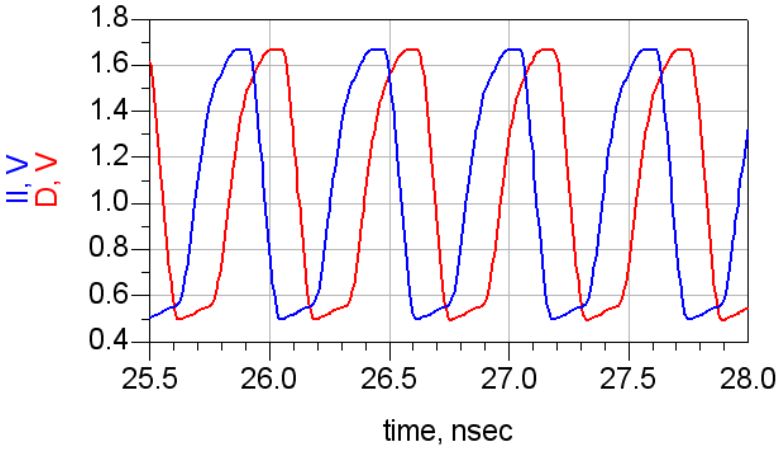


Fig. 2.18 Quadrature outputs of divide-by-2 divider

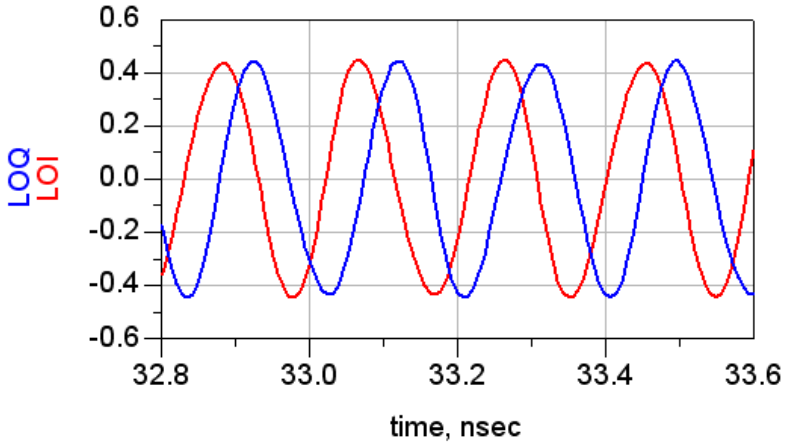


Fig. 2.19 Quadrature LO waveforms

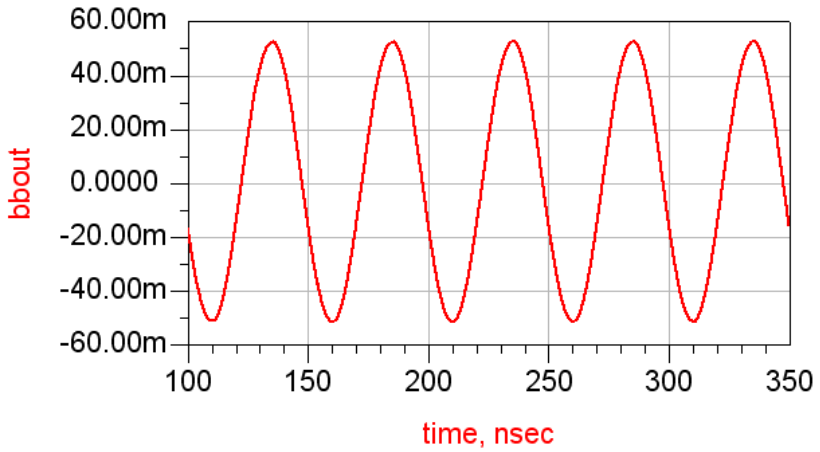


Fig. 2.20 Down-conversion wanted signal

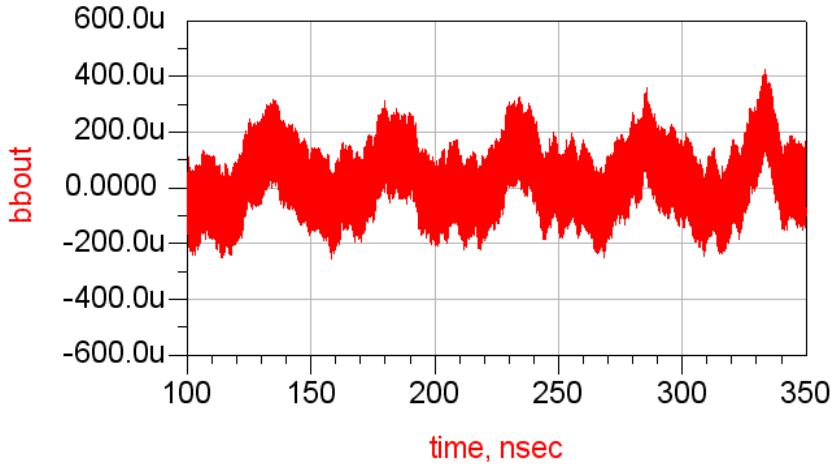


Fig. 2.21 Down-conversion image signal

The spectrum of quadrature outputs of divide-by-2 divider is shown in Fig 2.22. As can be seen in Fig 2.21, LO signal power at 5.25GHz is higher than that of lower side band about 27dB. Fig 2.23 shows that spectrum of down-conversion wanted signal in Fig 2.20 and Fig 2.24 shows that spectrum of down-conversion image signal in Fig 2.21. As can be seen in Fig 2.23 and Fig 2.24, the simulated IRR is greater than 50dB under I/Q matching situation. In Table 2.1, it lists the performance summary of quadrature LO generator with I/Q mismatch calibration.

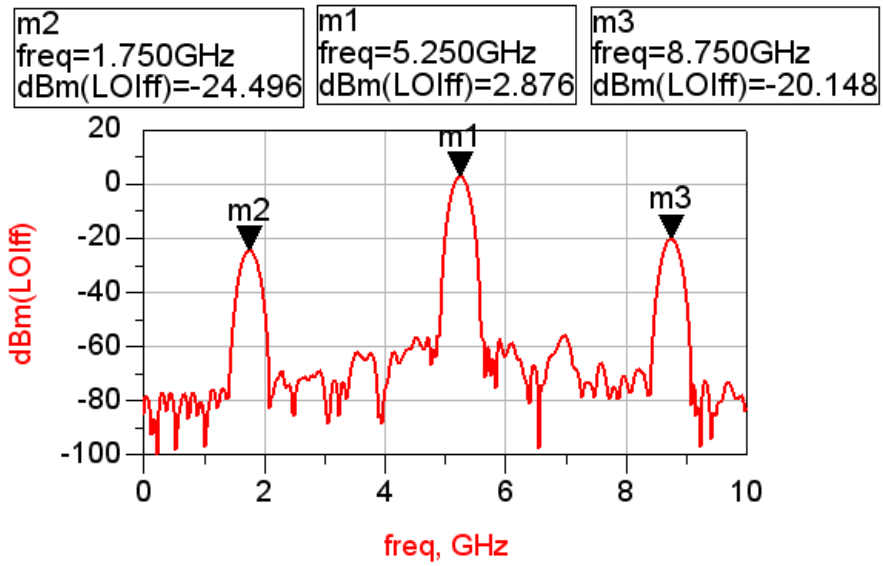


Fig. 2.22 Spectrum of quadrature outputs of divide-by-2 divider

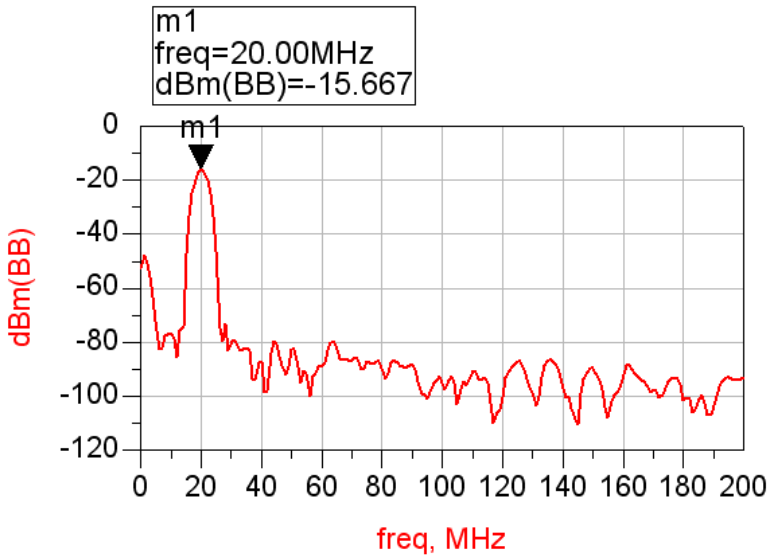


Fig. 2.23 Spectrum of down-conversion wanted signal

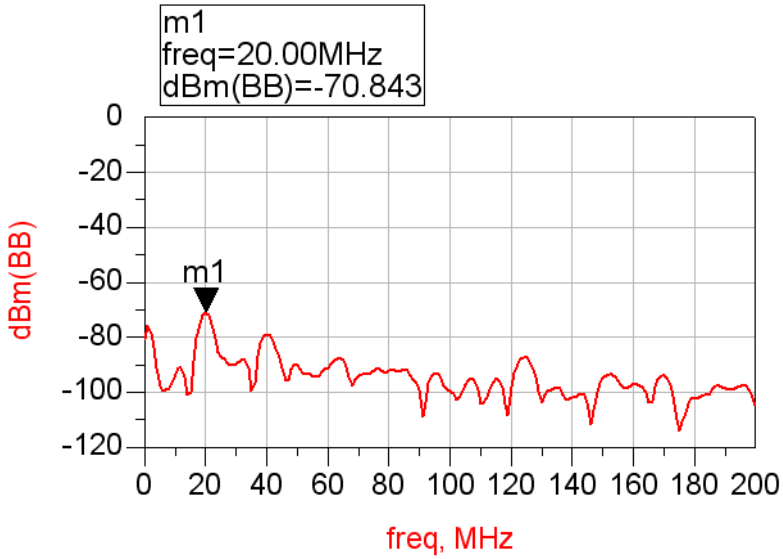


Fig. 2.24 Spectrum of down-conversion image signal

Table 2.1 Performance summary

Technology	TSMC 0.18 um CMOS	
Supply Voltage	1.8 V	
I/Q phase error	< 0.8°	
I/Q gain error	< 0.2dB	
Max. phase compensation	± 9.58°	
IRR	> 37.4 dB	
VCO tuning range	3.18GHz ~ 3.74GHz	
Power Consumptions	VCO	3.56 mW
	I/Q divider	5.94 mW
	LO generator	5.86 mW
	Mixer	9.42 mW
	Adder	20.63 mW
	Overall	45.41 mW

2.6 Measurements

A Quadrature LO generator with I/Q mismatch calibration is designed and fabricated in TSMC 0.18 μm technology. This section includes chip photograph, measurement setup and experimental results. Measured performances are taken into discussions.

2.6.1 Measurement Setup

Dies for measurement are bare and required to be bonded on PCB board. Packages are excluded for complicated parasites. The chip microphotograph and bonding board for measurement test are shown in Fig 2.25 and Fig 2.26. The chip need quadrature RF inputs, and thereby quadrature generator is necessary.

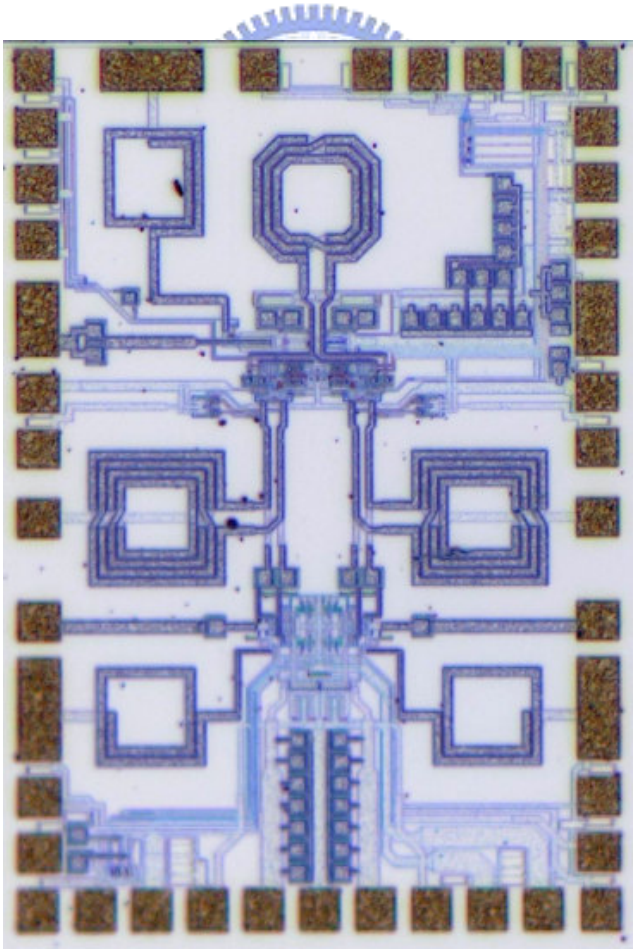


Fig. 2.25 Chip microphotograph of quadrature LO generator

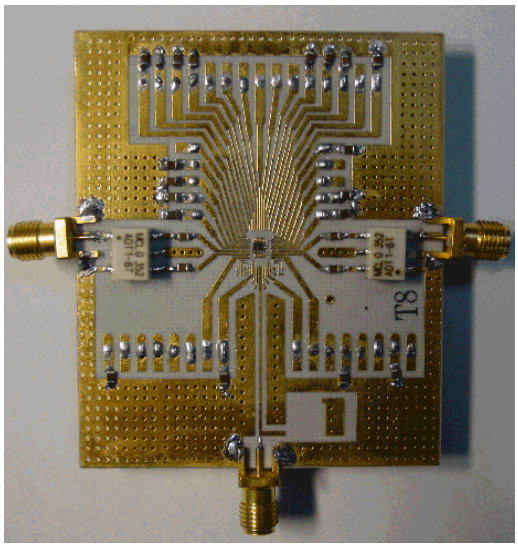


Fig. 2.26 Bonding board

DC board is used to provide the supply voltage, bias, and ground for bonding board. After plugging the DC board with the bonding board, test platform is completed as shown in Fig 2.27. SMD bypass capacitors are connected on the bonding board to filter out the high-frequency noise from supply and external components. The transformers with module number ADT1-6T are made by Mini-circuits. Signal attenuations caused by the matching network, transmission line,

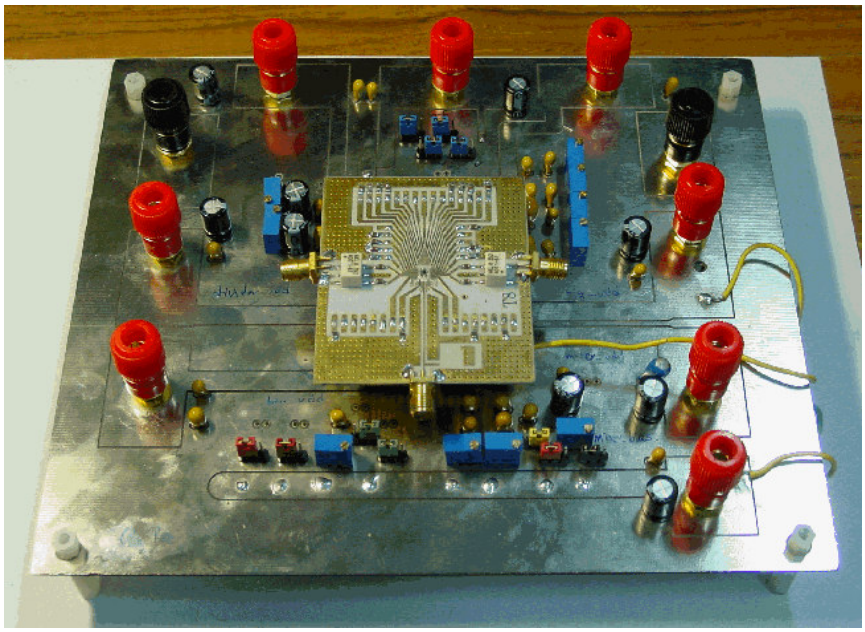


Fig. 2.27 Plugging DC board with bonding board

coaxial line and transformer network are measured and compensated back to measurement results.

In Fig 2.28, it shows the measurement setup diagram of quadrature phase-calibrated LO generator with image rejection mixers. Input signal is provided from external signal generator and quadrature signals are generated through quadrature hybrid. By adjusting frequency control voltage of the VCO, we can down convert RF signals to frequency band of 150k ~ 8.3MHz. At the output terminals, a transformer converts differential outputs to single output and feeds this output to spectrum analyzer. By spectrum analyzer, we can measure image signal and wanted signal, thus IRR can be get.

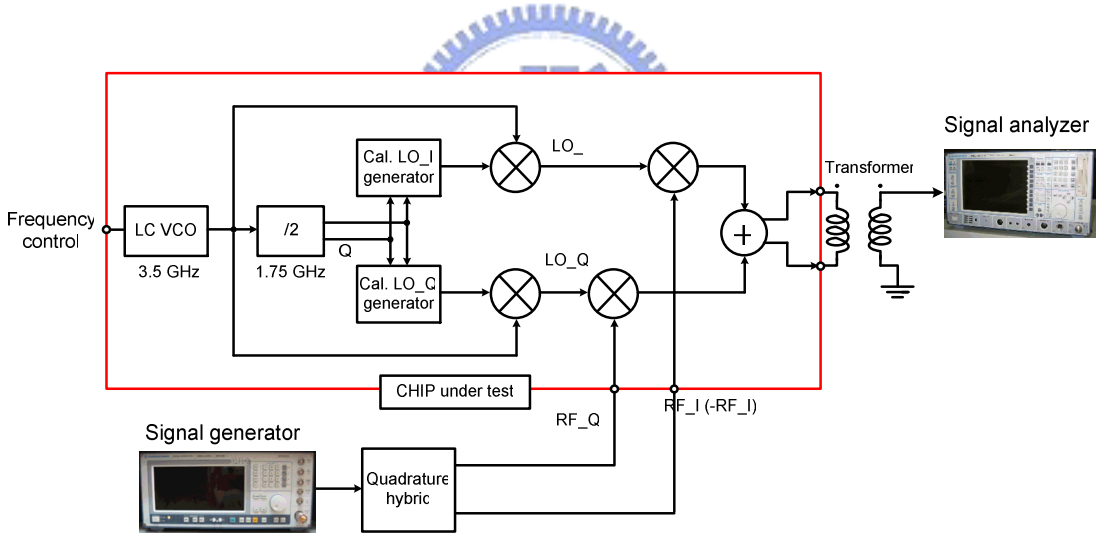


Fig. 2.28 Measurement setup diagram of quadrature phase-calibrated LO generator with image rejection mixers

2.6.2 Measurement Results

In Fig 2.28(a), it shows that photograph of quadrature hybrid. It is a four-port component. As RF signal inputs from one port, other two ports will generator RF I/Q signals at some frequency and the other port is isolated, i.e., the signal is cancelled at this port. In Fig 2.28(b), it shows that precise quadrature phase is at frequency of 5.335GHz. Fig 2.28(c), it shows that difference of S21 at 5.335GHz is about 0.7dB, a significant magnitude mismatch between port of RF_I and port of RF_Q.

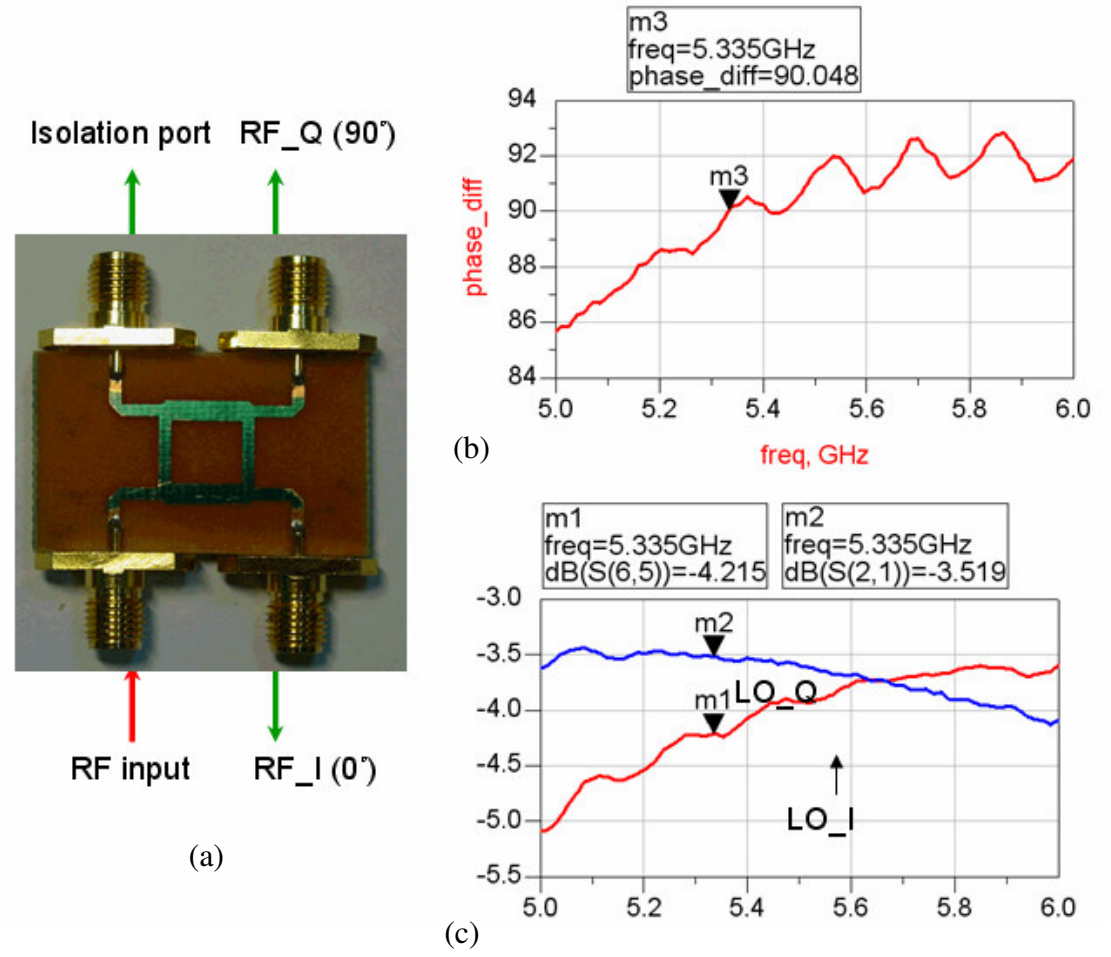


Fig. 2.28 Quadrature hybrid (a) photograph (b) phase difference between port of RF_I and RFQ (c) gain error between port of RF_I and RF_Q

In Fig 2.29, it shows input matching condition at RF I/Q input ports. At frequency of 5.335GHz, I/Q input matching is similar, thus it is suitable for injecting RF test signal at 5.335GHz. In Fig 2.30, it shows operating frequency of VCO versus control voltage and reveals that desired frequency of 5.335GHz is achievable.

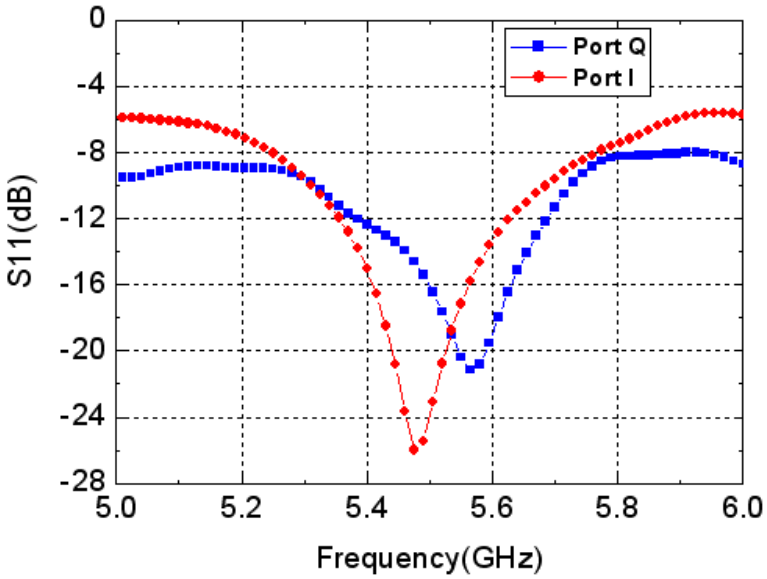


Fig. 2.29 I/Q port input matching

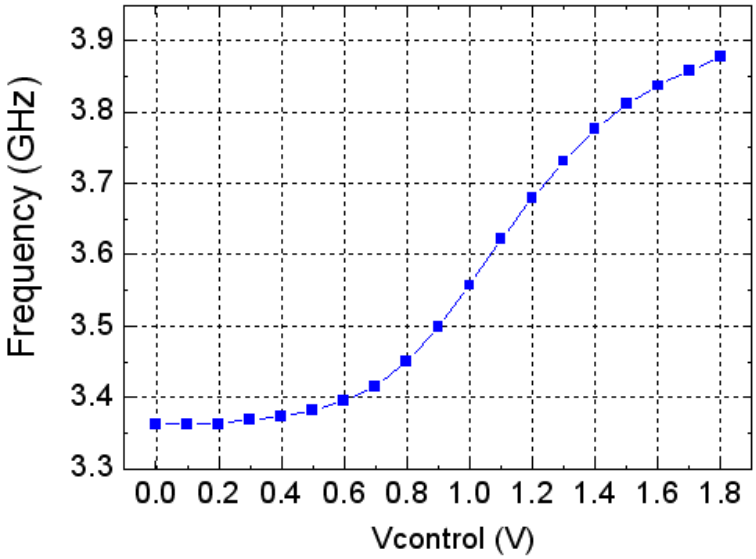


Fig. 2.30 Down-conversion signal from Q path

In Fig 2.31, it shows down-conversion signal by mixing of RFI and LOI. In Fig 2.32, it shows down-conversion signal by mixing of RFQ and LOQ. From Fig 2.31 and 2.32, it reveals that gain error about 2dB exists in I/Q path. However, our design is only able to calibrate gain error less than 1dB. This gain error exceeds our estimate.

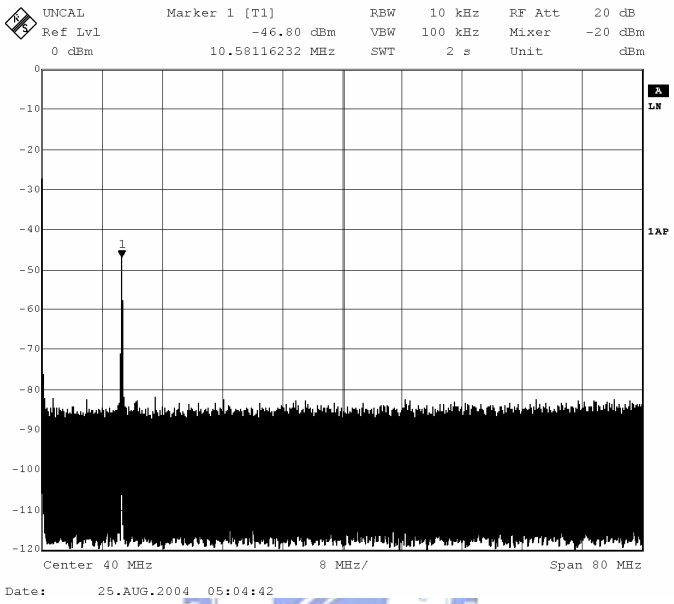


Fig. 2.31 Down-conversion signal from I path

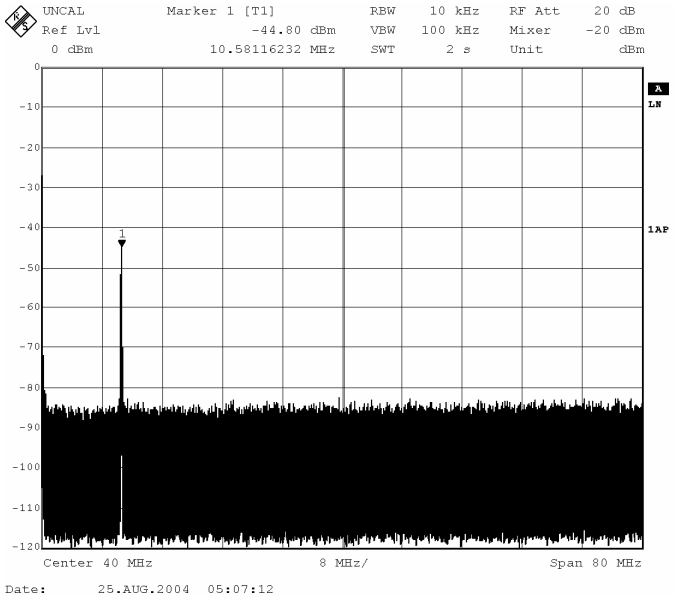


Fig. 2.32 Down-conversion signal from Q path

In Fig 2.33, it shows down-conversion signal is about -45.3dBm. In Fig 2.34, it shows down-conversion image is about -62.35dBm. From Fig 2.33 and 2.34, it reveals that IRR is about 17.05dB before calibration. And we can estimate that gain error is about 2dB and phase error is about 6°.

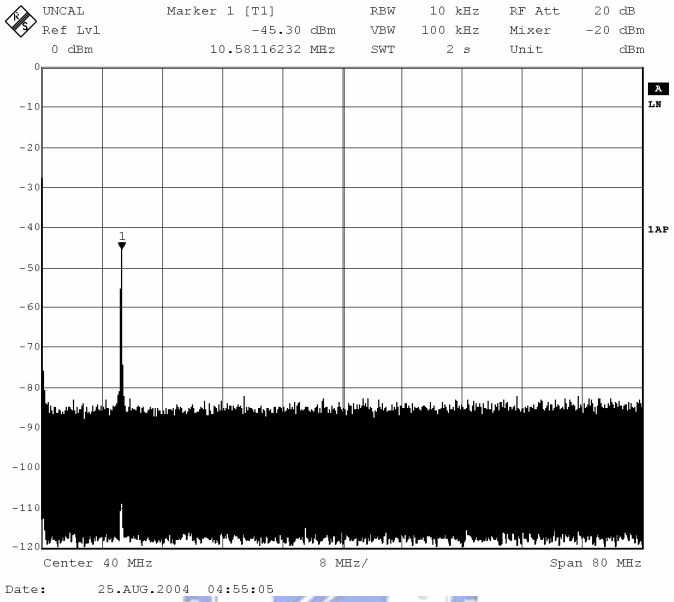


Fig. 2.33 Down-conversion signal (before calibration)

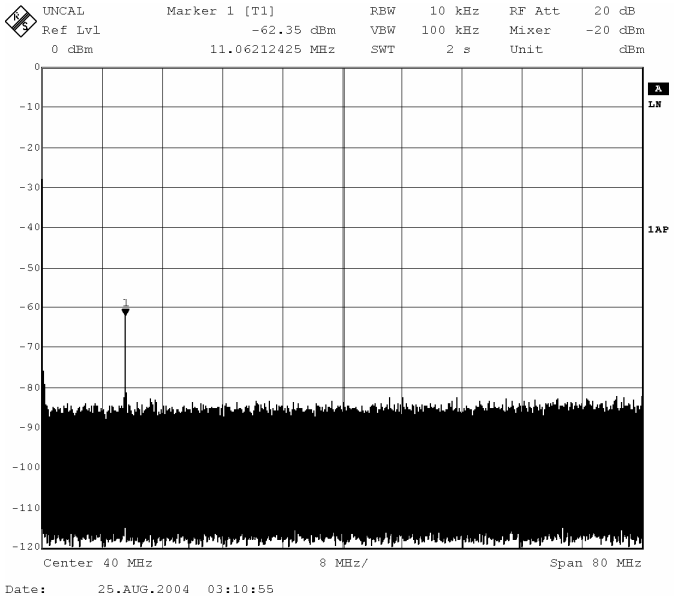


Fig. 2.34 Down-conversion image (before calibration)

In Fig 2.35, it shows down-conversion signal is about -43.86dBm. In Fig 2.36, it shows down-conversion image is about -72.11dBm. From Fig 2.35 and 2.36, it reveals that IRR is about 28.25dB after calibration. And we can estimate that gain error is about 0.66dB and phase error is less than 1°.

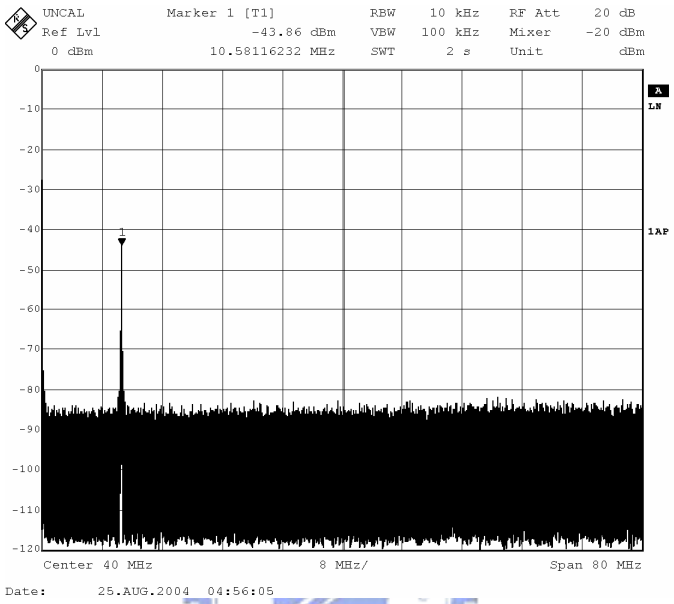


Fig. 2.35 Down-conversion signal (after calibration)

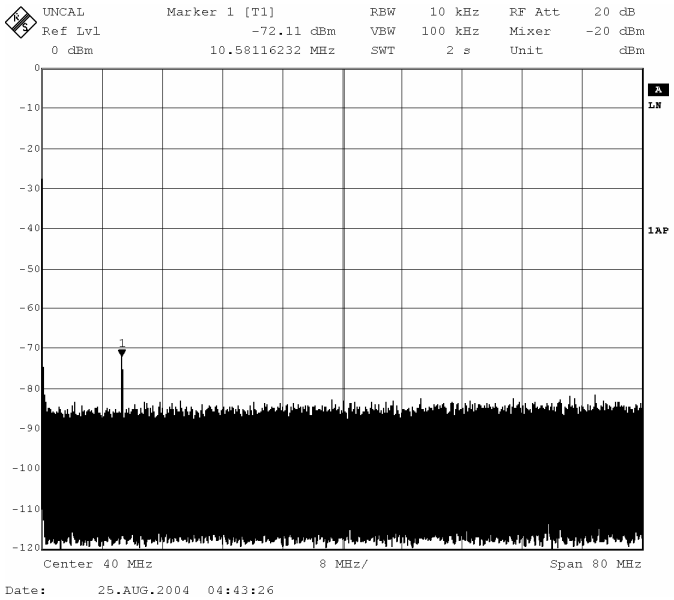


Fig. 2.36 Down-conversion image (after calibration)

In Table 2.2, it lists the performance summary of quadrature LO generator with I/Q mismatch calibration. Measured IRR is underestimated because of gain mismatch in quadrature hybrid and devices mismatch in I/Q signal path.

Table 2.2 Measured performance summary

Technology	TSMC 0.18 um CMOS	
Supply Voltage	1.8 V	
I/Q phase error	$< 1^{\circ}$	
I/Q gain error	≈ 0.66dB	
IRR	28.25 dB	
VCO tuning range	3.36GHz ~ 3.87GHz	
Power Consumptions	VCO	3.64 mW
	I/Q divider	5.56 mW
	LO generator	6.97 mW
	Mixer	9.05 mW
	Adder	14.89 mW
	Overall	40.11 mW

Chapter 3

Front-End Receiver with I/Q Mismatch Calibration

The function of our direct-conversion receiver is introduced in Chapter 1. In addition to the quadrature LO generator, the receiver requires the programmable front-end, including a variable-gain type LNA and a pair of gain-switch down-conversion mixer. Fig 3.1 gives an overall view of receiver block diagram. The quadrature LO generator is implemented by that mentioned in chapter 2. The LNA and mixer design will be introduced in the following.

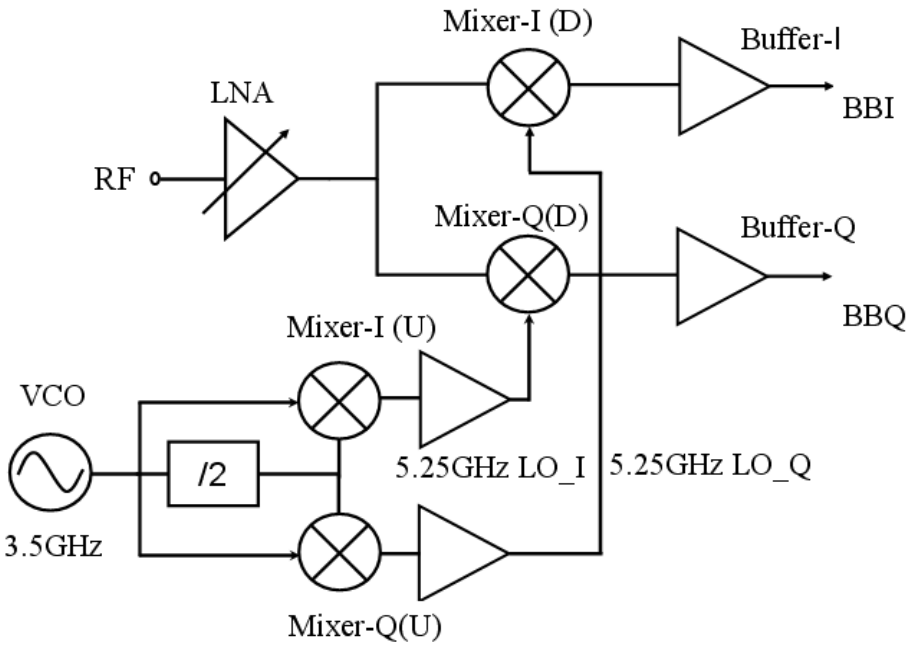


Fig. 3.1 Receiver block diagram

3.1 Front-End Link Budget

The IEEE 802.11a standard specifies over a generous 300-MHz allocation of spectrum for unlicensed operation in the 5-GHz block. Of that 300-MHz allowance, there is a contiguous 200-MHz portion extending from 5.15 to 5.35 GHz, and a separate 100-MHz segment from 5.725 to 5.825 GHz, whereas the output power cannot exceed 40 mW for channels from 5.15 to 5.25 GHz or 200 mW for channels from 5.25 to 5.35 GHz. Fig 3.2 shows a lower frequency band of the channel allocation [1]. To determine the precise target value, the specification sets frequency range, noise figure, maximum input signal level (input-referred 1-dB compression point). For frequency range, it is often acceptable to cover only the lower 200-MHz band. The upper 100-MHz domain is not contiguous with that allocation, so its coverage would complicate somewhat the design of the synthesizer. Furthermore, that upper 100-MHZ spectrum is not universally available, such as HIPERLAN. Hence,

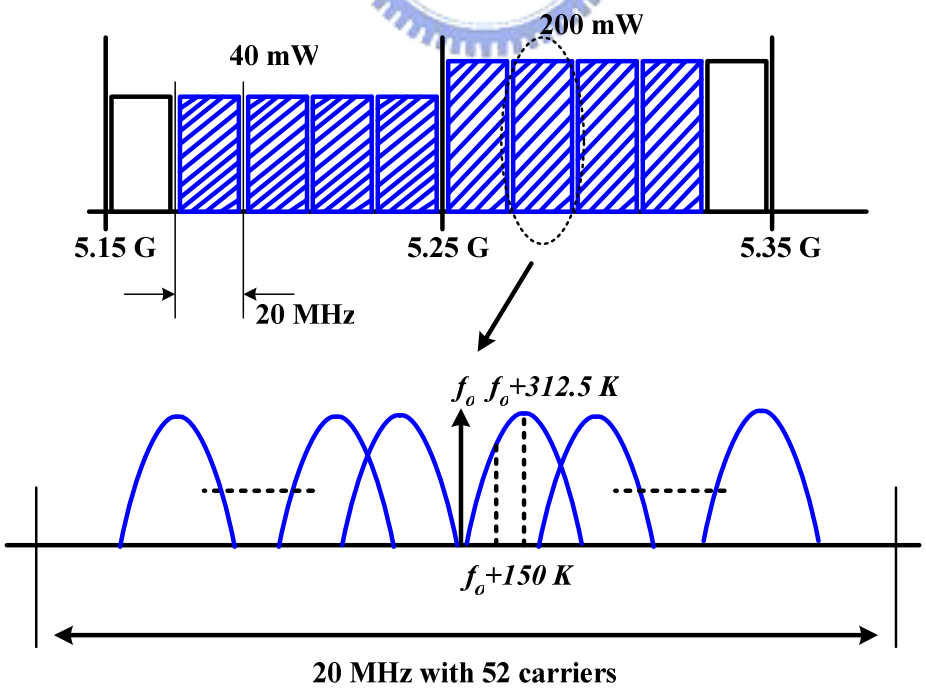


Fig. 3.2 IEEE 802.11a lower frequency band of the channel allocation

the receiver at the frequency band of 5.15-5.35GHz is our design goal. The specification simply recommends a noise figure of 10dB, with a 5-dB implementation margin. In order to accommodate the worst-case situation and gain more margins, maximum noise figure of 7dB is the design target for this receiver. The standard also specifies a value of –30 dBm as maximum input signal that a receiver must accommodate (for a 10% packet error rate). Converting this specification into a precise IIP3 target or 1-dB compression requirement is nontrivial. However, as a conservative rule of thumb, the 1-dB compression point of receiver should be about 4 dB above the maximum input signal power level that must be tolerated successfully. Based on this approximation, the target of input-referred 1-dB compression point has to be better than –26 dBm [11]. Furthermore, the IIP3 is about 9.6dB higher than the 1-dB compression point; therefore, the target of IIP3 is set to -16dBm.

According to the Friis equation, we can calculate the effect of each stage in a cascade upon the signal, noise, and IIP3. For the noise figure of cascaded stages, the total NF can be written as equation (3.1). For the linearity of a general expression for cascaded stages, the overall IIP3 can be equation (3.2). Table 3.1 lists the receiver front-end link budget under different gain modes and shows the overall performances.

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{p1}} \tag{3.1}$$

$$\frac{1}{A^2_{IP3,total}} \approx \frac{1}{A^2_{IP3,1}} + \frac{A_{P1}{}^2}{A^2_{IP3,2}} \tag{3.2}$$

Table 3.1 Estimated front-end link budget (High gain mode / Low gain mode)

	LNA	Mixer	Overall
Conversion Gain	22 / 8	12 / 6	34 / 14
Noise Figure	2 / 6	14 / 15	6 / 12
IIP3	-12 / -4	6 / 12	-24 / -10

3.2 Low Noise Amplifier Design

In RF system, the LNA, one of front-end circuits, locates on the receiving path of transceiver. The main functions are amplifying RF signal received from the antenna, providing input impedance matching and contributing as minimal noise as possible for the system working well.

3.2.1 Principle of the circuit design

Low Noise Amplifier, which constitutes the front-end of RF receivers, should have enough power gain to suppress the noise characteristic for the latter stages. However, when the signals with about -30dBm, the maximum input power of the IEEE 802.11a specification, are amplified by such high gain LNA, the output of the LNA exceeds the input dynamic range of the following stages. This would then result in undesired distortion of the mixer output, i.e. intermodulation. Therefore, in order to achieve high sensitivity and high linearity, the LNA should have a variable gain control function. At the time of a weak signal input, the LNA is set at a high gain mode to achieve the required high sensitivity, while at the time of a strong signal input the LNA is set at a low gain mode in order to keep the signal within the input dynamic range of the following mixer.

Fig 3.3 shows the schematic of the adopted current switch gain control amplifier [12]. The MOS transistors M1 and M2 form a conventional common-source-cascode single ended LNA with inductive degeneration. The source of M3 is connected to transconductance stage, M1, which converts the RF input power into current, and the drain of it is connected to the supply Vdd, which provides a leakage path for RF signal current. The current determined by the transconductance stage flows into the M2 and M3. The current ratio of M2 and M3 is determined by the gate bias of them. In the high gain mode, both sw1 and sw2 are turned on, such that M3 is biased at the

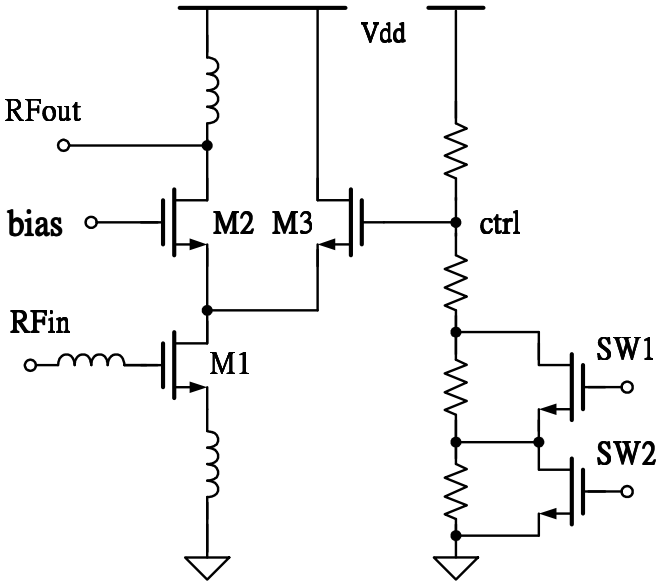


Fig. 3.3 Current switch gain control LNA

cut-off region, it acts as an usual cascode LNA and has a high gain. In the medium gain mode, sw1 is turned on and sw2 is off, thus part of the RF current produced by the transconductance input stage is bypassed to VDD and results in a lower gain. It stands to the reason that if both switches are turned off, the LNA gain would be further reduced and operated in the low gain mode. The variable gain function is realized by switching sw1 and sw2 to control the gate bias of M3.

3.2.2 Input matching

Input matching is an important consideration for connection with external components. Described by microwave theoretic, signal is partially reflected if passing through the interface between two different mediums. The meaning in circuit design is unequal input/output impedances between two stages. To minimize the reflection, input impedance of an LNA has to be designed to match 50Ω characteristic impedance.

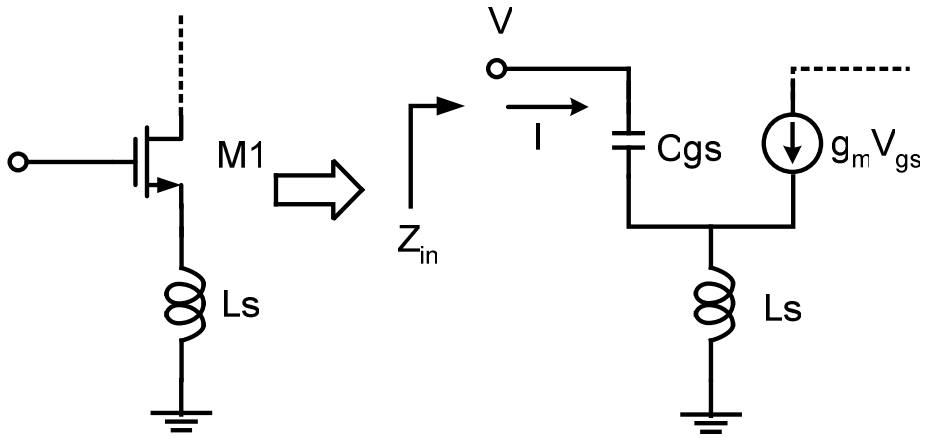


Fig. 3.4 LNA Input matching

As passive device, an active device such as MOS or BJT contributes impedance. In the design with CMOS process, MOS device is applied with inductor in matching strategy. To analysis the input matching network of LNA, the equivalent small-signal model in LNA input port is shown in Fig 3.4. The *Zin* can be got from the simple small signal analysis in the following. The input impedance

$$V = j\omega \cdot L_S \cdot \left(I + g_m \cdot V_{gs}\right) + \frac{I}{j\omega \cdot C_{gs}}$$

$$\Rightarrow Zin = \frac{V}{I} = \frac{g_m}{C_{gs}} \cdot L_S + j\omega \cdot L_S + \frac{1}{j\omega \cdot C_{gs}}$$

$$= \frac{g_m}{C_{gs}} \cdot L_S + j\left(\omega \cdot L_S - \frac{1}{\omega \cdot C_{gs}}\right) \tag{3.3}$$

As described in equation (3.3), the source inductor can be designed to eliminate the reactance; the transconductance g_m, parasitical capacitance C_{gs} and source inductance L_S can be designed to achieve 50Ω resistance.

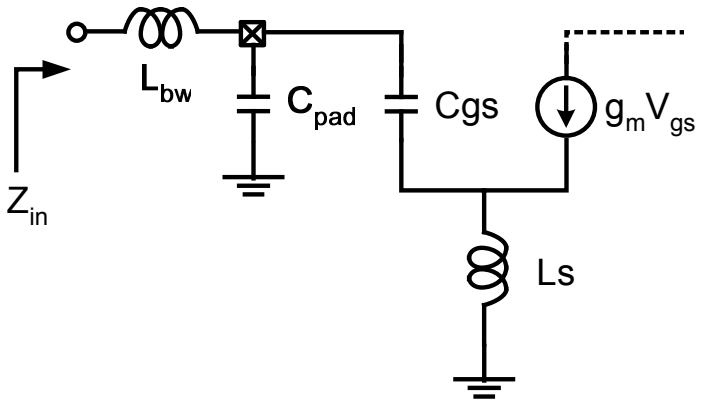


Fig. 3.5 LNA input matching using pad and bondwire

Actually, input matching is also affected by other inevitable factors. There exists parasitical capacitance on input/output pads. If a chip under test is bonded on a board for measurement, bond-wires contribute parasitical inductance. The parasitic can be practically treated as a part of matching network(L network), thus the impedance *Zin* in Fig 3.4 cannot be designed as 50Ω. Fig 3.5 depicts a modified input matching with parasitic of a pad and a bond-wire. Smith chart is useful for designing proper capacitance for pad and inductance for bondwire to achieve *Zin* of 50Ω.

3.2.3 Optimum Noise Figure Analysis [13]

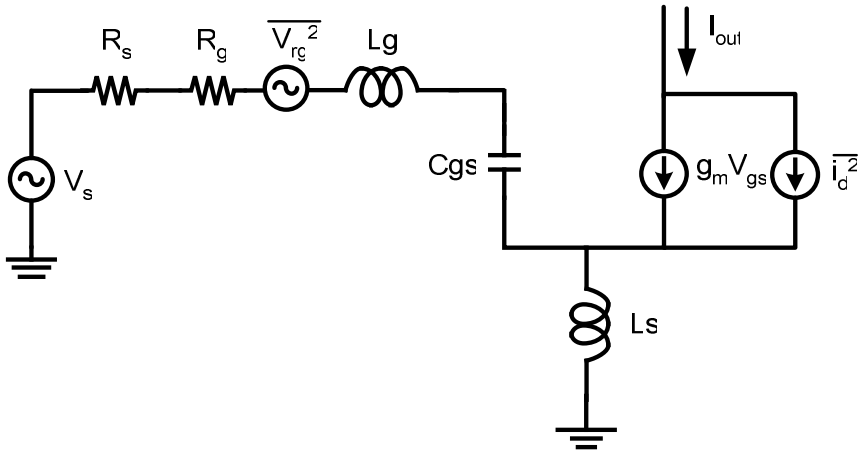


Fig. 3.6 LNA input matching using pad and bondwire

The noise figure of the LNA can be computed by analyzing the input noise model shown in Fig 3.6. In this circuit, R_s represents the voltage source impedance of V_s, R_g is the gate resistance of the MOS device, and $\overline{i_d^2}$ is the channel thermal noise of the device. For the simply analysis, the noise distribution of the cascode device M2 in Fig 3.6 is neglected. Another type noise source in MOS is "induced gate noise". This noise is generated because the fluctuations in the channel charge will induce a physical current in gate due to capacitive coupling. At frequency approaching w_T, the gate impedance is not pure capacitive, but it include a real conductance g_g. Be careful that the "induced gate noise" is different from the noise generated by the gate polysilicon resistance. The mathematical expressions for these sources are:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \tag{3.4}$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{3.5}$$

Based on the model represented from ref [13], theoretically minimal noise figure formulates considering the effect of the gate induced noise can be expressed as:

$$NF = 1 + \frac{\gamma\omega_0 L}{3v_{sat}} p(\rho, P_D) \tag{3.6}$$

$$p(\rho, P_D) \approx \frac{\frac{P_D}{P_0}(1+\frac{\delta}{5\gamma}) + 2|c|\sqrt{\frac{\delta}{5\gamma}\rho^2 + \frac{P_o}{P_D}\frac{\delta}{5\gamma}\rho^4}}{\rho^3} \tag{3.7}$$

$$\rho = \frac{V_{od}}{L\varepsilon_{sat}} \tag{3.8}$$

$$P_o = \frac{3}{2}\frac{V_{dd}v_{sat}\varepsilon_{sat}}{\omega_o R_s} \tag{3.9}$$

$$P_D = V_{dd}I_d = V_{dd}WC_{ox}v_{sat}\frac{V_{od}^2}{V_{od} + L\varepsilon_{sat}} \tag{3.10}$$

, where γ is a bias-dependent factor, L is channel length, v_{sat} is saturation velocity, V_{od} is overdrive voltage, ε_{sat} is velocity saturation field strength, c is the correlation coefficient between the gate noise and drain noise and P_D is power consumption.

From the above equations, it is known that the noise figure is a function of P_D, thus, it is defined as a variable

$$Q_L = \frac{1}{\omega_o R_s C_{gs}} \quad , \quad C_{gs} = \frac{2}{3} WLC_{ox} \quad \Rightarrow \quad Q_L = \frac{P_0}{P_D} \frac{\rho^2}{1+\rho} \tag{3.11}$$

For designer, decidable parameters are V_{dd}, W, L and P_D. Since minimal L is generally used for minimum NF_{min} and standard operation supply for 0.18 μm process is 1.8V. The designed LNA optimizes the noise performance only by choosing proper W and P_D. From equation (3.6) ~ (3.11), we can use the MATLAB simulation to find the minimum NF at a specific value of Q_L. After the Q_L value has been found, the optimal device size of input stage can be determined from equation (3.11). Fig 3.7 plots NF versus finger number (transfer from Q_L and W) curves under different power consumptions by MATLAB. It exhibits that choosing the finger number of input stage equal to 32 (device size = 2.5×32 = 80 μm) will derive the minimum NF. And according to ref [14], it has good performance at NF if the size of M2 is the same as M1 in Fig 3.3.

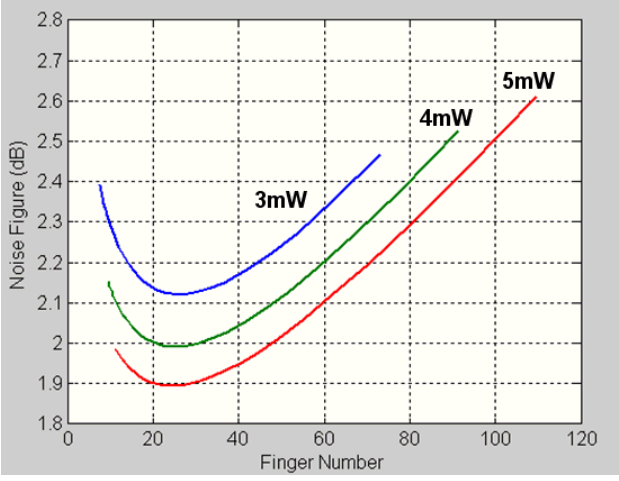


Fig. 3.7 NF versus finger number of input stage

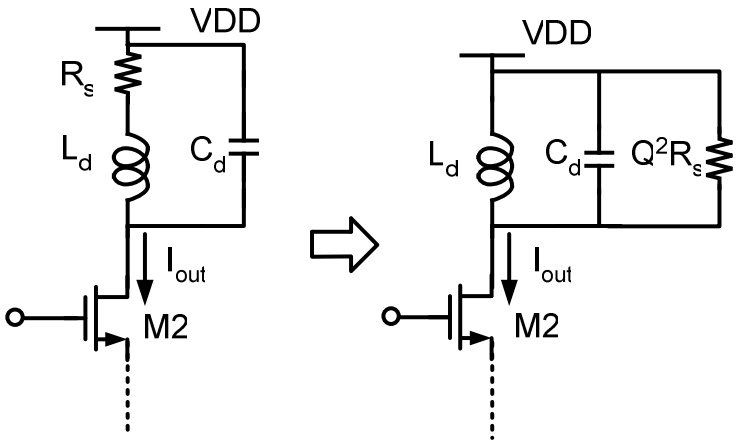


Fig. 3.8 Impedance transformation

3.2.4 Gain

In this LNA design, the power gain and voltage gain can be derived as

$$A_V = g_{m,M1} Q_{in} R_{out} = G_{eff} R_L \tag{3.12}$$

As shown in Fig 3.8, the combination that forms the R_L in LNA is the parallel of a capacitor and an inductor series with a resistor. The parallel capacitor plays a role to tune out the inductor load, and the series resistor is modeled as the parasitic resistor of the inductor. The value of the load can be derived:

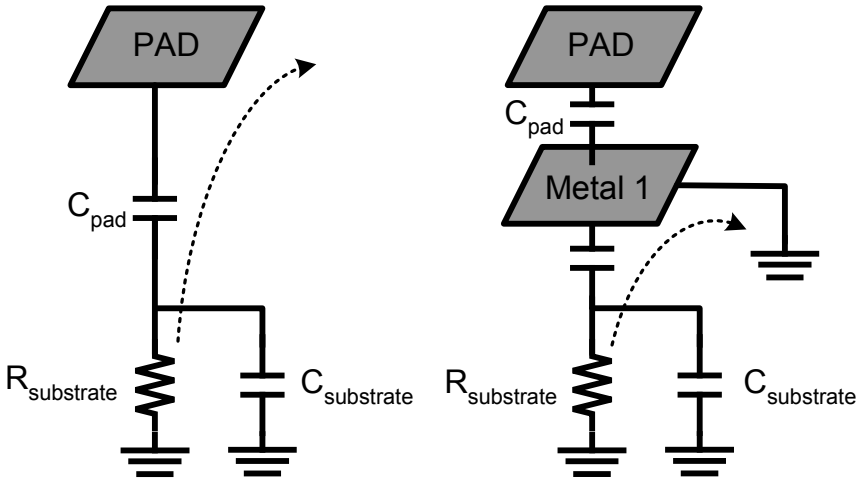
$$R_L(j\omega) = \frac{1}{j\omega C} \| (j\omega L + R) \tag{3.13}$$

Using the passive impedance transformation [10], the series L-R circuit is transformed to the equivalent parallel L-R circuit.

$$R_L(j\omega) = \frac{1}{j\omega C} \| j\omega L_p \| R_p = \frac{1}{j\omega C} \| j\omega L \| Q^2 R \tag{3.14}$$

where Q is the quality factor of the inductor, defined as the impedance of the inductor divider by the series resistor. At the resonance frequency, i.e. $\omega = \frac{1}{2\pi\sqrt{LC}}$, the voltage gain of the LNA

$$A_V = G_{eff} R_L = G_{eff} \cdot Q^2 R \tag{3.15}$$



(a) Normal pad (b) Shielded pad

Fig. 3.9 Normal pad and shielded pad

3.2.5 Shielded PAD (RF PAD)

The comparison between normal pad and shielded pad is shown in Fig 3.8. Fig 3.8(a) shows that the normal pad has capacitive characteristic with resistivity. This is the cause to make input signals noisy, because the parasitic resistance of substrate is a significant thermal noise source and the noise couples into the signal path through the metal to substrate capacitance, as shown in Fig 3.9(a). This will degrades noise characteristics of the LNA. To avoid such degradation, the shielded pad is used for input pad of the LNA. The shielded pad, shown in Fig 3.8(b), acts as a shield and leads the coupled substrate noise to ground. Thus, the shielded pad will alleviate the noise from substrate.

3.2.6 LNA Simulation

The simulation of LAN is completed by ADS simulator with process parameters of TSMC 0.18-μm mixed signal 1P6M RF SPICE models. In Fig 3.10, it reveals that the simulated S11 is lower than -12dB from 5.15GHz to 5.35GHz at different gain

modes. Therefore, the input matching is good at operation frequency band. Fig 3.11 is the simulation result of noise figure at high gain mode and it achieves NF_{min} at the desired band. Fig 3.12 shows that voltage gain about 23dB, 16dB, and 9dB at high, medium, and low gain mode respectively. In Fig 3.13, it evaluates the linearity performance, i.e. IIP3, by two-tone test and it reveals that IIP3 can improve about 16dB at low gain mode than at high gain mode. A summary of the LNA is listed in Table 3.2.

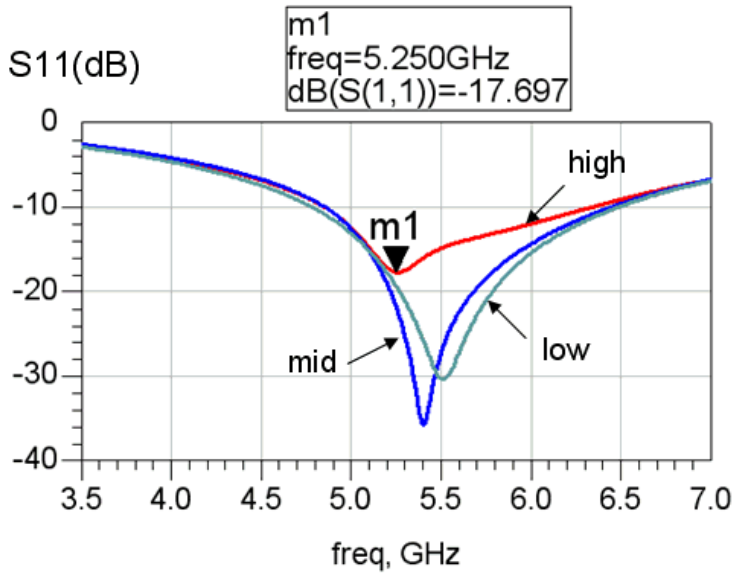


Fig. 3.10 S11 of the LNA at different gain mode

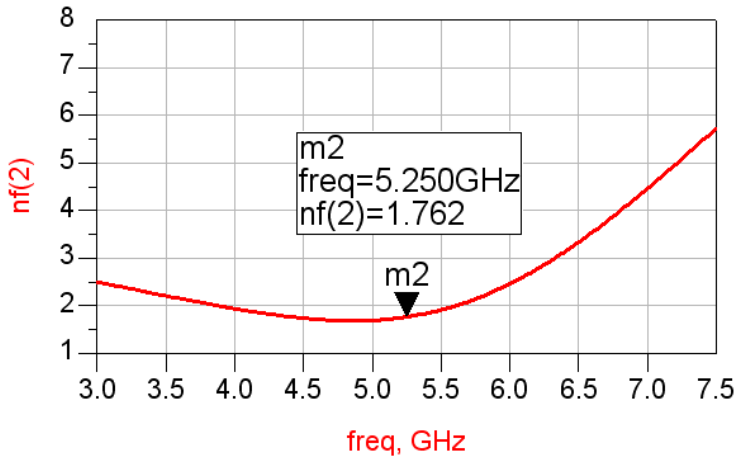


Fig. 3.11 Noise figure of the LNA at high gain mode

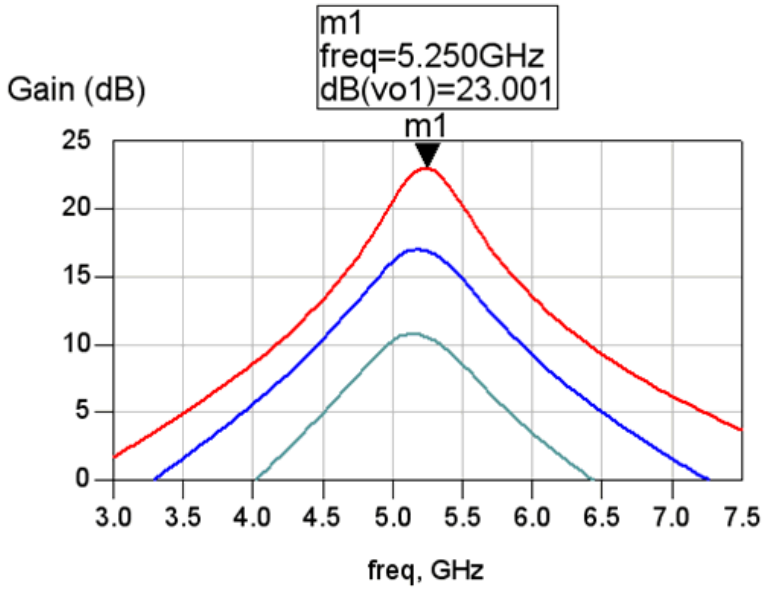


Fig. 3.12 Voltage gain of the LNA at different gain mode

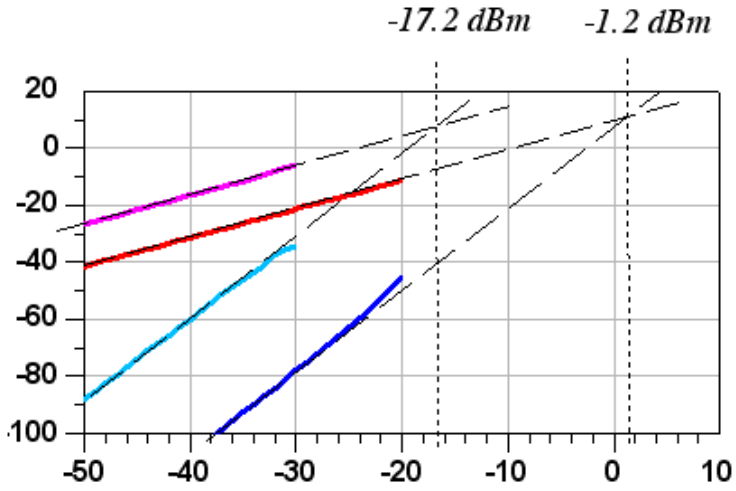


Fig. 3.13 IIP3 of the LNA at high and low gain mode

Table 3.2 Summary of the LNA

	Con. Gain (dB)	NF (dB)	IIP3 (dBm)
High Gain	23	1.8	-17.2
Medium Gain	16	3.5	-4.6
Low Gain	9	6.1	1.2

3.3 Down-Conversion Mixer

The amplified RF signal by LNA is converted down to mixers for further amplification and frequency transfer. However, the behavior of down conversion will imply some unwanted spurious signals to interfere with the desired signal, thus the linearity is the most important issue of the mixer design. Usually the mixer dominates the linearity performance of the overall receiver.

3.3.1 Principle of the circuit design

The mixer is the most critical stage in the receiver chain in combating the flicker noise. In a conventional single balanced mixer (Fig 3.14(a)), one faces a difficult trade-off in choosing the proper biasing of I1. The switching quad M2 and M3 exhibits lower flicker noise if I1 can be reduced [15], while the V/I converter M1 requires a high biasing current to achieve a decent conversion gain and good linearity.

In this work, a current injection mixer is used (Fig 3.14(b)) [16]. By means of the current-injection technique, it reduces the voltage drops across the resistor load for low voltage operations. Furthermore, it alleviates the LO power for current switches,

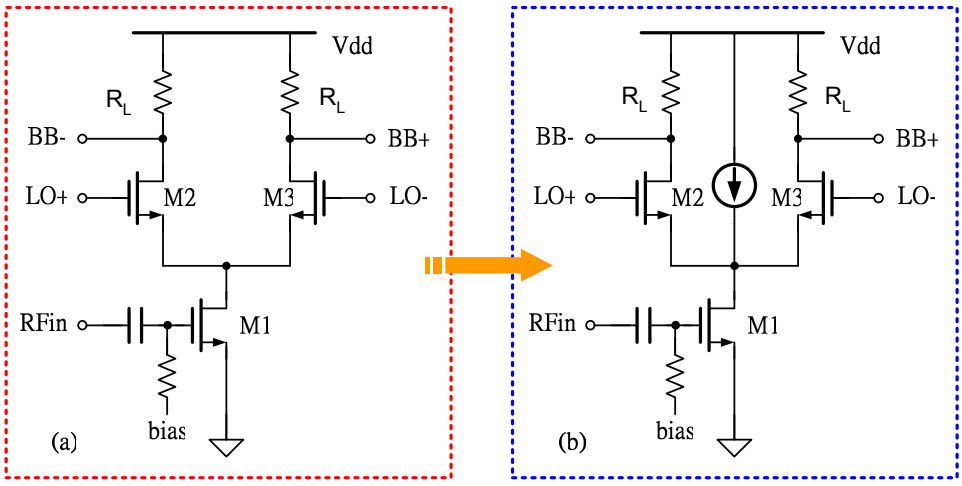


Fig. 3.14 Mixer design

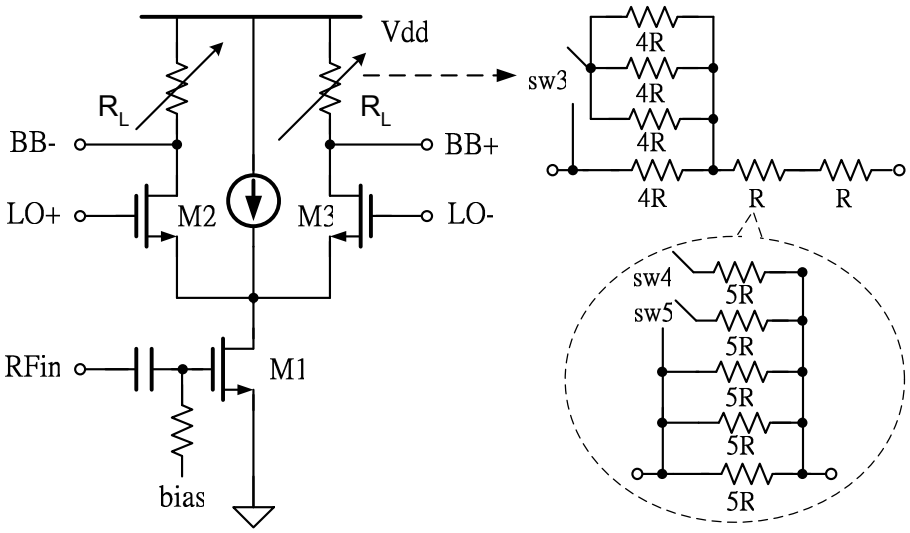


Fig. 3.15 Mixer design and comparison

accelerates the switching speed, and suppresses flicker noise up-conversion thanks to sharp transitions of the current switches [15]. Some mixer solving the above problem is provided in [17].On the other hand, the linearity of the mixer can be maintained at a higher DC current level. For digital gain control, a resistor ladder is utilized as the output load. Fig 3.15 shows the detailed resistor ladder load. For coarse tuning, the resistive load is switched between 6R and 3R by sw3 for high (6R) and low gain (3R) operations. Besides, the gain can be fine tuned by switching sw4 and sw5. They correspond to switch a fine gain step of 0.4dB. By this approach, the gain error of I/Q signal paths less than 1dB can be calibrated less than 0.2dB.

3.3.2 Noise Analysis

The mixer or frequency converter is a significant noise contributor in most communication systems. Its function is inherently noisy because noise is transferred from multiple frequency bands to the output. Since the circuit performs frequency translation, it is not linear time-variant and its noise behavior cannot be analyzed with conventional circuit techniques. Therefore the presented noise analysis [18] and noise

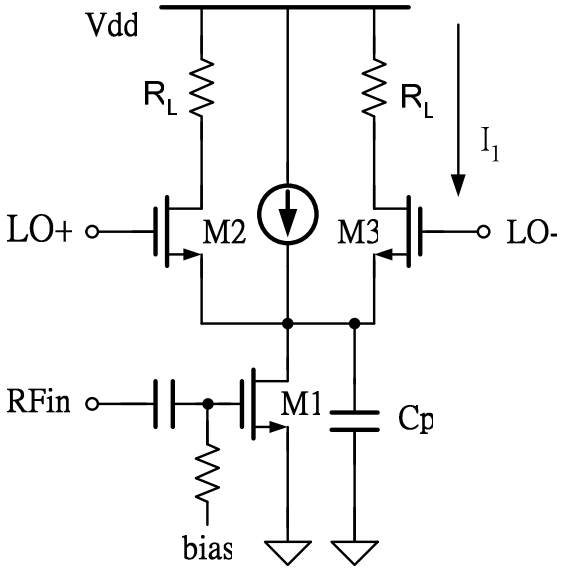


Fig. 3.16 Noise analysis of used mixer

model [15] are employed to optimize the noise performance. According to ref [15], the overall noise sources in Fig 3.16 are expressed as:

$$\overline{V_{n1}^2} = \frac{1}{\pi}\cdot\frac{I_1}{A}\cdot\overline{V_n^2} \tag{3.16}$$

$$\overline{V_{n2}^2} = (2\cdot f_{LO}\cdot Cp)^2\cdot\overline{V_n^2} \tag{3.17}$$

$$\overline{V_{n3}^2} = (\frac{1}{\pi}\cdot\frac{g_m\cdot Vos}{A})^2\cdot\overline{V_{ni}^2} \tag{3.18}$$

$$\overline{V_{n4}^2} = 8kT\cdot R_L\cdot(1+\gamma\cdot\frac{1}{\pi}\cdot\frac{I_1\cdot R_L}{\pi\cdot A}+\gamma\cdot\frac{g_m\cdot R_L}{2}) \tag{3.19}$$

$$A_m \approx \frac{2}{\pi}\cdot g_m\cdot R_L\cdot(1-\frac{\sqrt{2}\cdot(V_{gs}-V_{th})_{M2}}{\pi\cdot V_{LO}}) \tag{3.20}$$

$$\overline{V_{total}^2} = \frac{\overline{V_{n1}^2}+\overline{V_{n2}^2}+\overline{V_{n3}^2}+\overline{V_{n4}^2}}{A_m{}^2} \tag{3.21}$$

, where $\overline{V_n^2}$ is flicker noise of the switch pair, $\overline{V_{ni}^2}$ is flicker noise of input stage, and g_m is transconductance of the switch pair. Equation (3.16) reveals direct induced flicker noise of the switch pair. Equation (3.17) reveals the indirect induced flicker noise of switch from parasitic capacitance, Cp. Equation (3.18) reveals that flicker noise originating from the transconductance devices leaks through switch FET's

unbalanced by an offset. Equation (3.19) reveals white noise of the mixer, where the first term is due to the two load resistor s R_L, the second term is the output noise due to the two switches, and the last term shows the noise of the transconductance stage transferred to the mixer output. In Fig 3.17, it shows the calculation result compares with ADS simulation. It reveals that the value and trend of them are similar.

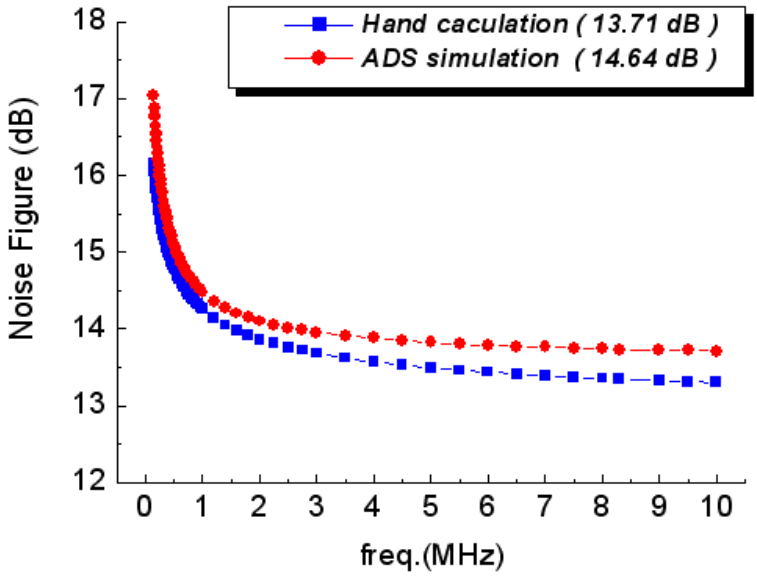


Fig. 3.17 Mixer noise figure

3.3.2 Mixer Simulation

In Fig 3.18, it shows the simulated IIP3 at high and low gain mode. IIP3 at high gain mode is 1dBm and at low gain mode is 3dBm. IIP3 is improved by 2dB at low gain mode. Table 3.3 lists summary of the mixer.

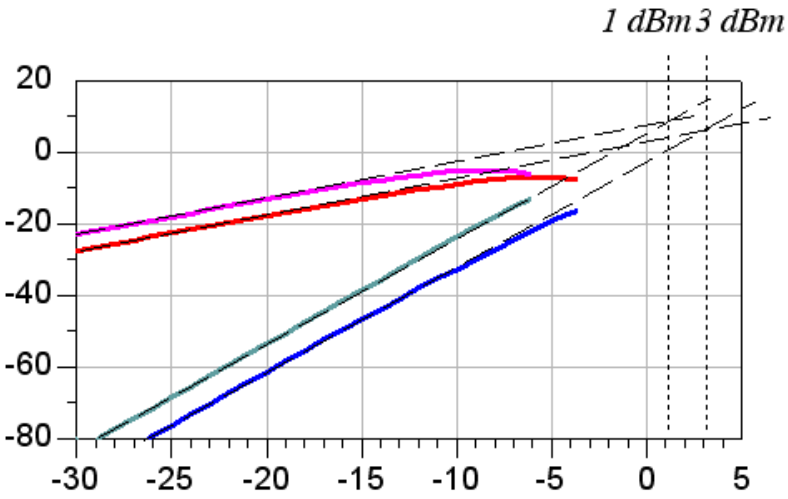


Fig. 3.18 IIP3 of the mixer at high and low gain mode

Table 3.3 Summary of the mixer

	Con. Gain (dB)	NF (dB)	IIP3 (dBm)
High Gain	11.6	14.64	1
Low Gain	6.1	14.89	3

3.4 Adaptive Biasing VCO

In a high-performance VCO design, it trends toward whether power can be traded off for phase noise system in such way that performance is not unduly compromised. The VCO in ref [19] is to architect circuit techniques that allow for scaling back performance to save power in times of reduced demand but which do not detract from the ultimate level of phase noise performance realized in a full integrated VCO. A tunable oscillator and on-chip biasing provide a wide linear control range over the bias current. Therefore adaptive biasing VCO is used in this receiver design.

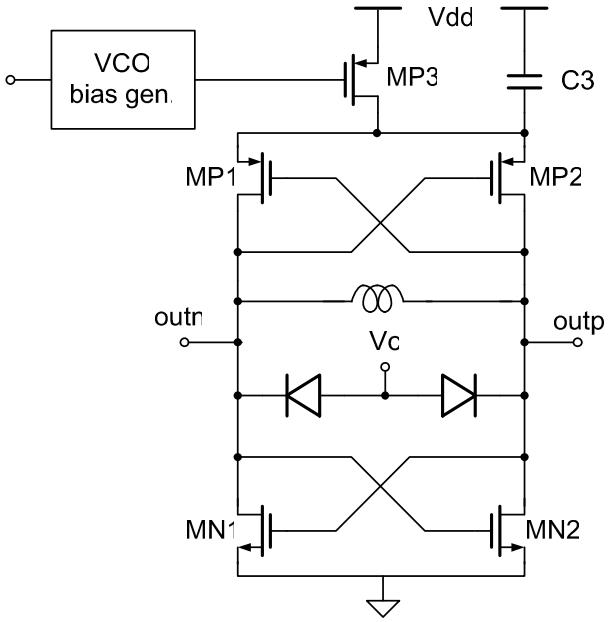


Fig. 3.19 Differential CMOS VCO [19]

3.4.1 Principle of the circuit design

A recent CMOS oscillator topology is depicted in Fig 3.19, where the cross-coupled nMOS and pMOS pairs provide regenerative gain and balanced drive strengths to lower flicker noise up-conversion [9]. Capacitor C3 filters the bias current sourced by MP3 [20], a tail current source ideally operated with a minimal voltage drop so the oscillation can swing over the full range afforded by the supply. However, making MP3 arbitrarily wide increases its transconductance, magnifying the effect of bias circuitry noise on the gate potential of MP3. The desired solution is to use a small tail transistor with a low V_{DS} but a large gate overdrive to support the bias current. While optimal for reducing phase noise, these conditions leave the tail device in triode where it ceases to function as a current source, and a diode-tied mirror transistor no longer suffices for accurately controlling the oscillator current from an established reference.

For the VCO current to track an input current reference, the reference must flow

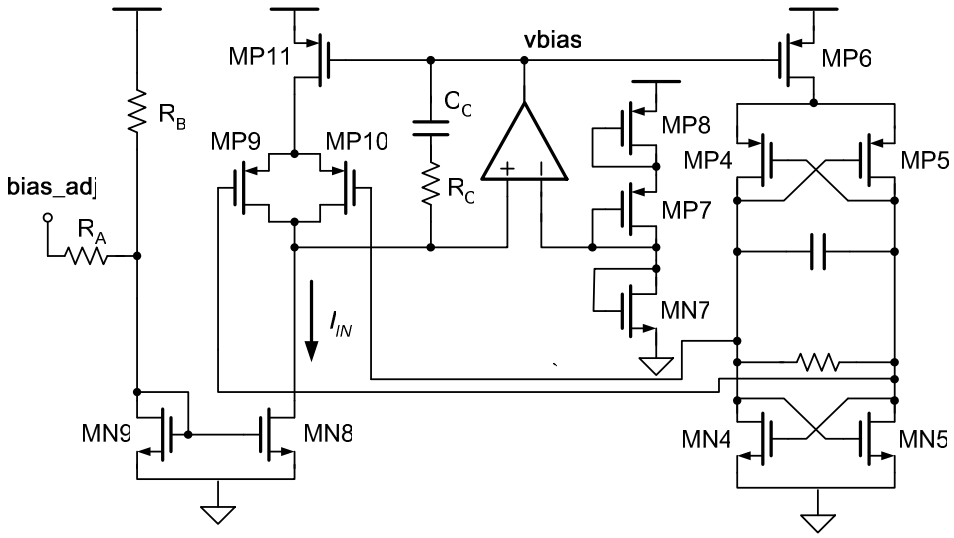


Fig. 3.20 Adaptive linear bias generation circuit [19]

into a transistor that is matched to the VCO tail current source and which has the same V_{GS} and V_{DS} potentials. The circuit that implements this is shown in Fig 3.20. Transistors MN4-5 combines with MP4-6 to form a non-oscillating replica of the VCO in which the resonant load is replaced with an RC network. MP9-11 duplicates the p-channel half of the replica. Provided that the Mp9010 transistor pair is maintained in saturation, the gate-to-source potentials of MP9-10 match those of MP4-5 in the replica, and thus the drain-to-source voltages ─ and hence the drain current ─ of the p-channel tail devices (MP11 and MP6) also match. An op-amp holds the drains of MP9-10 to a potential set by a reference chain that approximates the VCO common-mode output voltage, and also drives the gate bias on the tail transistors to the level required to support the input current (I_{IN}). The same current flows in the DD replica of the VCO and thus appears in the oscillator core itself (multiplied by a scale factor of size ratio of MP3 to MP6). Two resistors and the current mirror MN8-9 set I_{IN}, although a more elaborate reference could be substituted. For feedback loop stabilization, R_C and C_C are used to provide enough phase margins.

3.4.2 Phase Noise Analysis

In 1996, Leeson proposed a model to describe the phase noise of the LC oscillator. In Leeson's model [21], phase noise spectrum is first determined by three regions, i.e.,$1/f^3$, $1/f^2$, and noise floor. And an equation is proposed to express phase noise as:

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_S}\cdot\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{3.22}$$

, where P_s is the power of the oscillation swing, Q is effective quality factor of the tank, ω_0 and $\Delta\omega$ mean oscillation frequency and offset frequency, $\Delta\omega_{1/f^3}$ is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions, and F is an empirical fitting parameter for device noise and must be determined from measurements.

Recently, phase noise of LC VCO has been analyzed by different models and theories [22][23]. A popular model for phase noise analysis presented in [23] is suitable for our VCO and is expressed as

$$L(\Delta\omega) = 10\log\left(\frac{\overline{v_{noise}^2}}{v_{signal}^2}\right) = 10\log\left[\frac{2FkT}{P_S}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{3.23}$$

$$F = 2+\frac{4\gamma RI_T}{\pi Vo}+\gamma\frac{8}{9}g_{mbias}R \tag{3.24}$$

, where R is the resonator resistor, V_O is the swing amplitude, γ is the noise factor of a single FET, classically 8/3 for short channel device, g_m is the conductance of tail current source, and I_T is tail current flowing through VCO core. From devices in our VCO design, it shows that R equal to 13.27, g_m equal to 7.64 mA/V, V_o equal to 0.55V, and I_T equal to 2mA, and evaluation of PN by equation (3.24) shown in the following.

$$L(\Delta\omega) = 10\log\left(\frac{\overline{v_{noise}^2}}{v_{signal}^2}\right) = 10\log\left[\frac{2FkT}{P_S}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] = -121.8dBc/Hz \tag{3.25}$$

3.4.3 VCO Simulation

Fig 3.21 shows the simulated behavior with a 1.8V supply and a 5:1 range of input currents. The current in the VCO core matches core matches the input setting to within 3% of the expected 5. In Fig 3.21, it shows the simulated differential outputs of VCO at time domain. In Fig 3.22, phase noise simulation using ADS simulator shows that output noise exhibits -121.8dBc/Hz at 1MHz offset. It reveals that the simulator result is similar to noise model calculation shown in equation (3.25). Table 3.4 lists summary of the VCO.

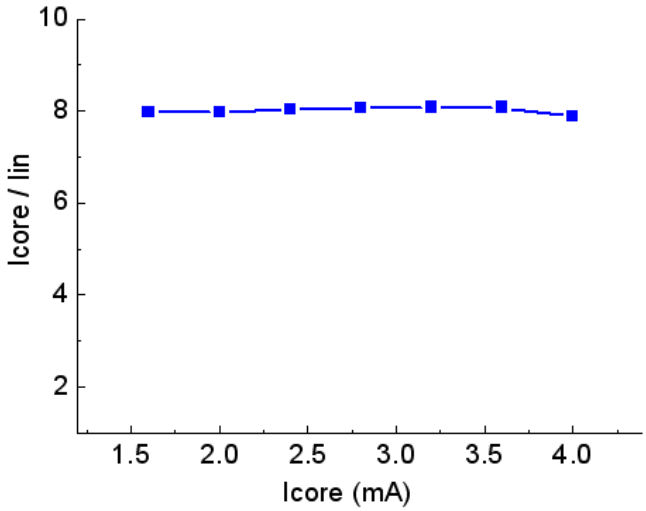


Fig. 3.21 DC simulation of VCO bias circuit

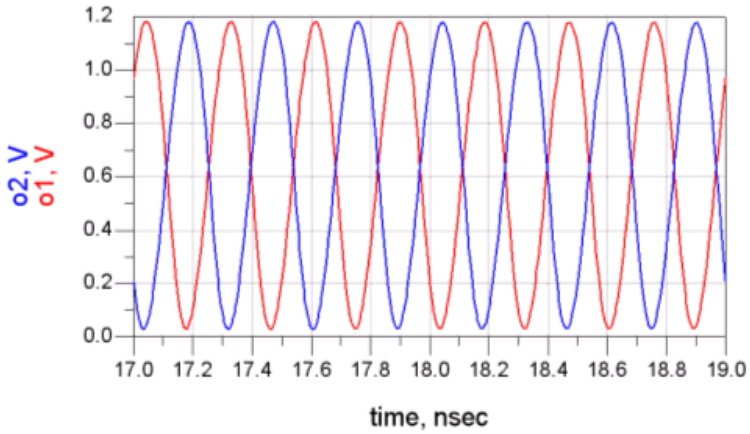


Fig. 3.22 Differential outputs of VCO at time domain

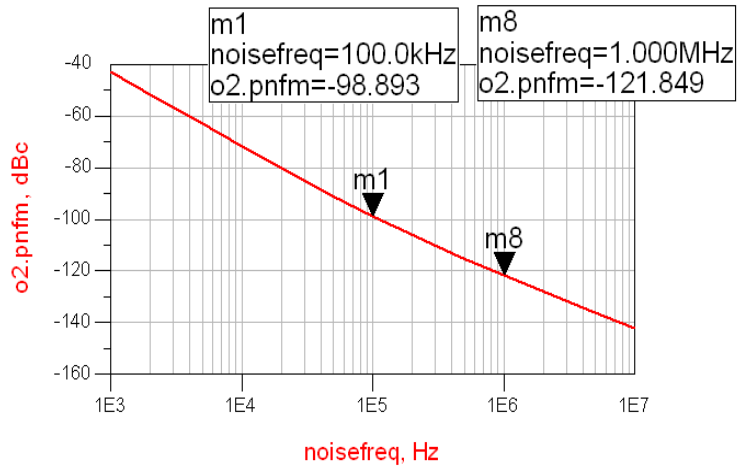


Fig. 3.23 Phase noise simulation using ADS simulator

Table 3.4 Summary of the VCO

Phase noise @ 1MHz	-121.8dBc/Hz
Tuning range	23
Dissipation power	16
FOM	9

3.5 Receiver Simulation

Fig 3.24 shows the simulated noise figure of overall receiver and conversion gain under maximum gain mode. It reveals that the integrated noise figure from 150kHz to 8.3MHz is about 5.5dB. In Fig 3.25, it shows the simulated IIP3 at maximum and minimum gain mode. IIP3 at maximum gain mode is -23.8dBm and at minimum gain mode is -7dBm. IIP3 is improved by 16.8dB at minimum gain mode. Fig 3.26 shows the simulated down-conversion quadrature signals. Table 3.5 lists simulated summary of the receiver.

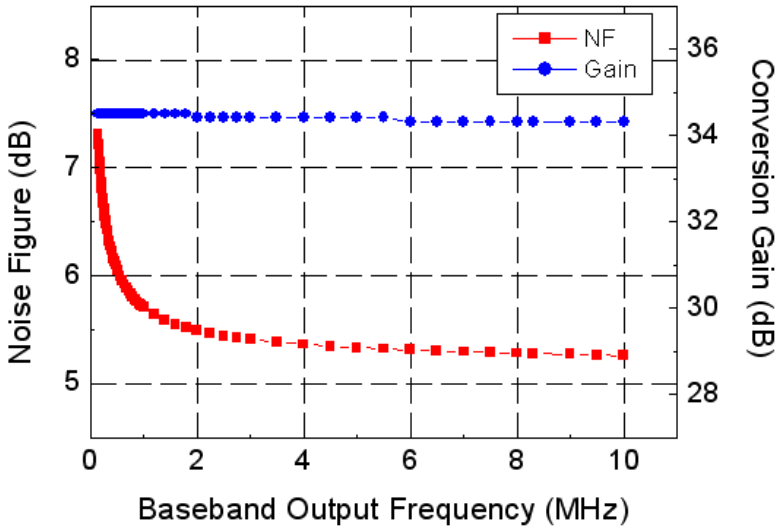


Fig. 3.24 Phase noise simulation using ADS simulator

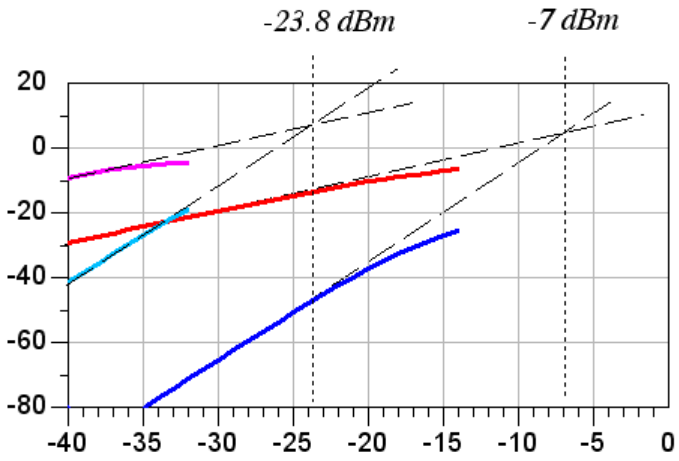


Fig. 3.25 Phase noise simulation using ADS simulator

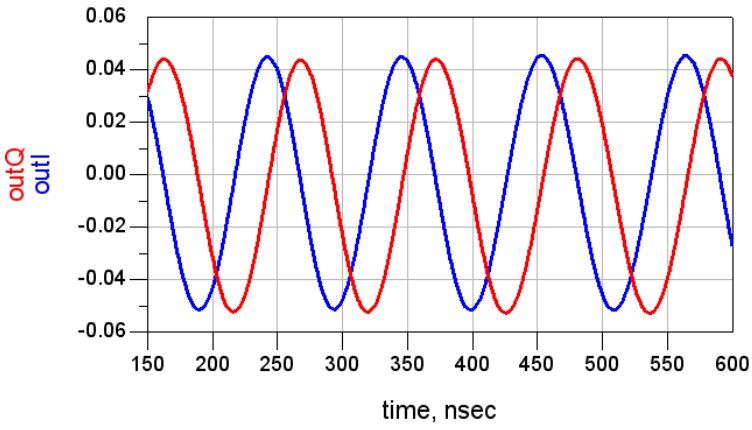


Fig. 3.26 Down-conversion quadrature signals

Table 3.5 Simulated summary of the receiver

Technology / Supply	TSMC 0.18 um CMOS	
Frequency band	5.15 ~ 5.35GHz	
Down-conv. frequency	150k ~ 8.2MHz	
S11	< -12dB	
Gain max / mini	34dB / 16dB	
LNA gain switch	7dB / 14dB	
Mixer gain switch	5.5dB	
Noise Figure(SSB)	5.5dB	
IIP3	-23.8dBm/-7dBm	
I/Q phase mismatch	< 0.8°	
I/Q gain mismatch	< 0.2dB	
Power Consumptions	LNA	4.86mW
	Mixer	9.82mW
	VCO	3.59mW
	I/Q divider	6.12 mW
	LO generator	5.86 mW
	Overall	30.25 mW

3.6 Measurements

A front-end receiver is designed and fabricated in TSMC 0.18 μm technology. This section includes chip photograph, measurement setup and experimental results. Measured performances are taken into discussions and comparison with the state-of-the-art publications.

3.6.1 Measurement setup

Dies for measurement are bare and required to be bonded on PCB board. Packages are excluded for complicated parasitic. The chip microphotograph and the bonding board for measurement test are shown in Fig 3.27 and Fig 3.28. Total chip area is 1.64 mm^2. External balun is not necessary because of single-ended RF input.

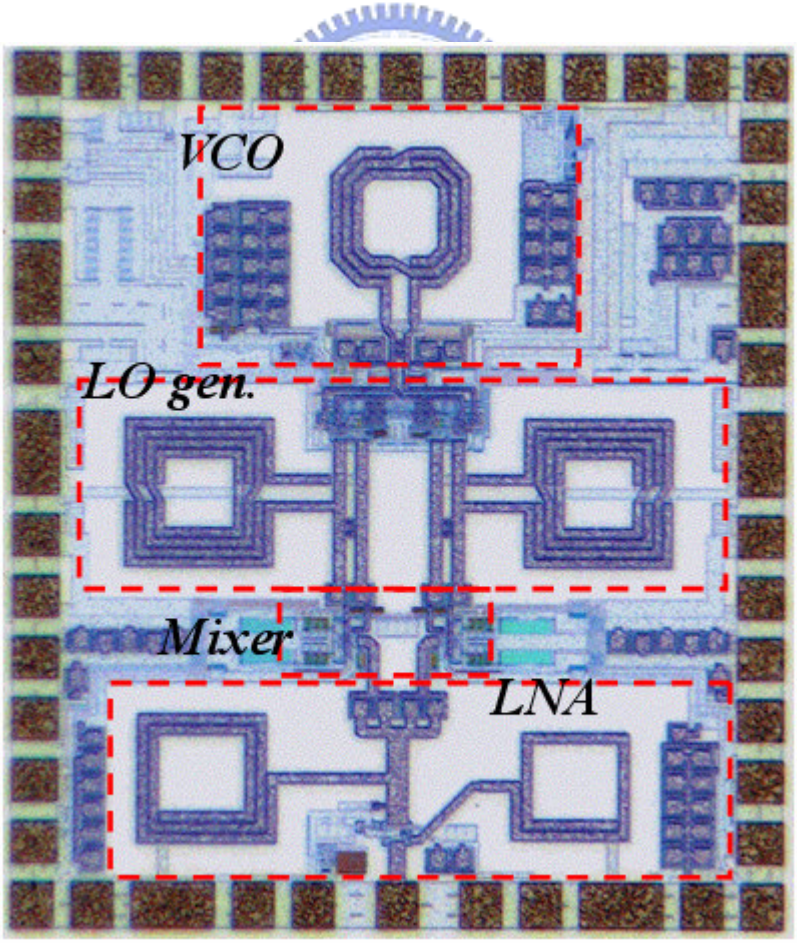


Fig. 3.27 Chip microphotograph of the receiver

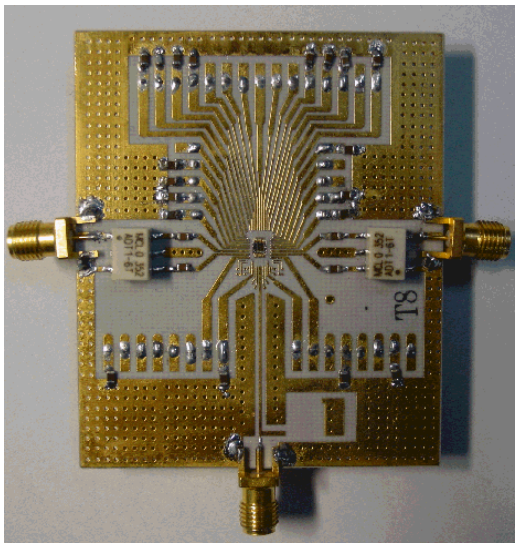


Fig. 3.28 Bonding board

DC board is used for providing the supply voltage, bias, and ground to bonding board. After plugging the DC board with the bonding board, test platform is completed as shown in Fig 3.29. SMD bypass capacitors are connected on the bonding board to filter out the high-frequency noise from supply and external components. The transformers with module number ADT1-6T are made by Mini-circuits. Signal attenuation caused by the matching network, transmission line,

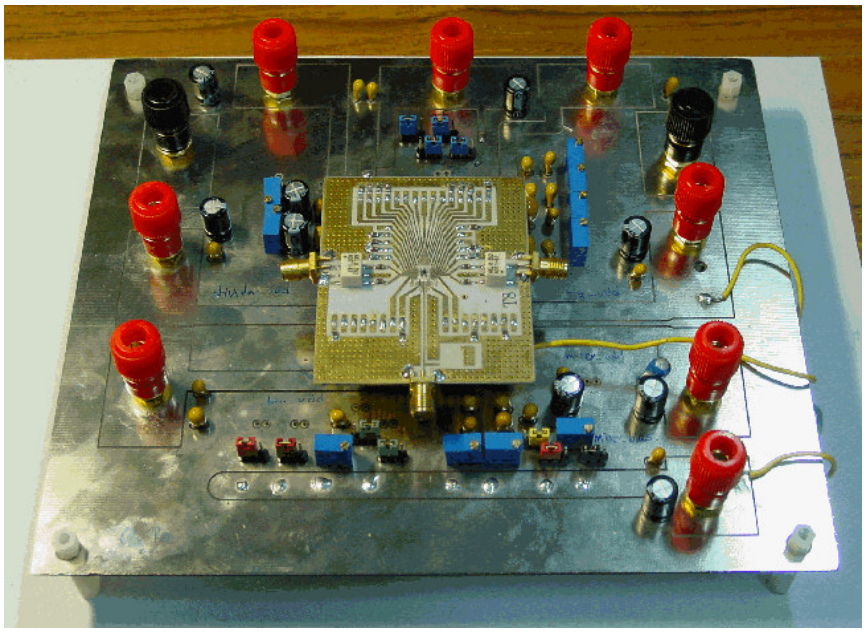


Fig. 3.29 Plugging DC board with bonding board

coaxial line and transformer network are measured and compensated back to measurement results.

In Fig 3.30, it shows the measurement setup diagram of receiver. Input signal is provided by external signal generator. By adjusting frequency control voltage of the VCO, we can down convert RF signals to frequency band of 150k ~ 8.3MHz. At the output terminals, a transformer converts differential outputs to single output and feeds this output to spectrum analyzer. Besides, each kind of measurements depends on using suitable instruments. S-parameter measurement for input matching condition requires a network analyzer; spectrum analysis requires a signal generator (input 5GHz RF signals) and a spectrum analyzer; noise analysis requires a noise source and a noise analyzer; waveform analysis requires a signal generator (input 5GHz RF signals) and an oscilloscope.

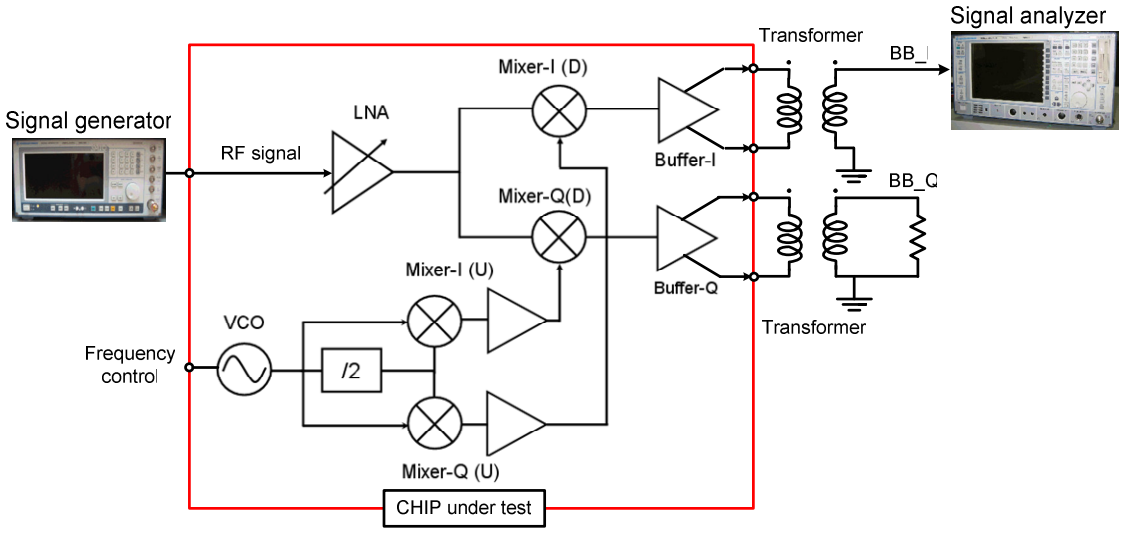


Fig. 3.30 Measurement setup diagram of receiver

3.6.2 Measurement Results

In Fig 3.31, it shows the measured down-conversion signal with -37dBm at 3.8MHz as input RF power of -65dBm. It reveals that conversion gain is about 28dB at the interesting band. In Fig 3.32, it plots that LNA gain (roughly estimated from power of down-conversion signal) and input matching (S11) versus frequency. It reveals that estimated gain is about 21dB and the desired frequency band (5.15GHz ~

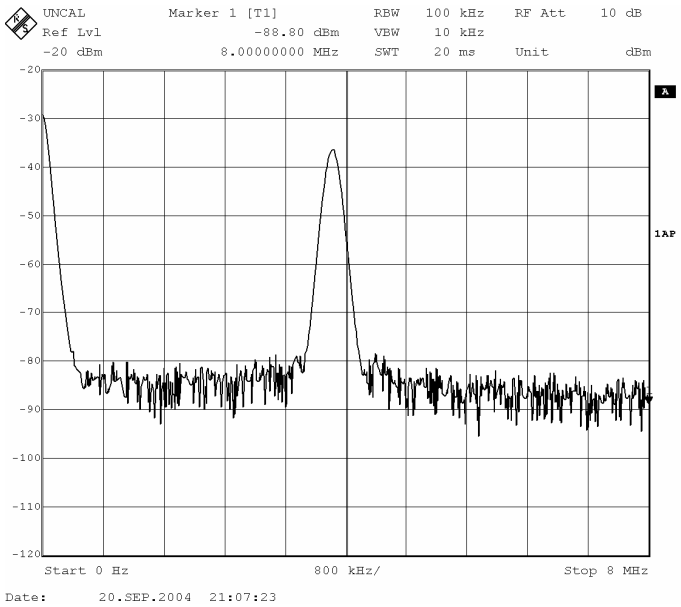


Fig. 3.31 Measured down-conversion signal

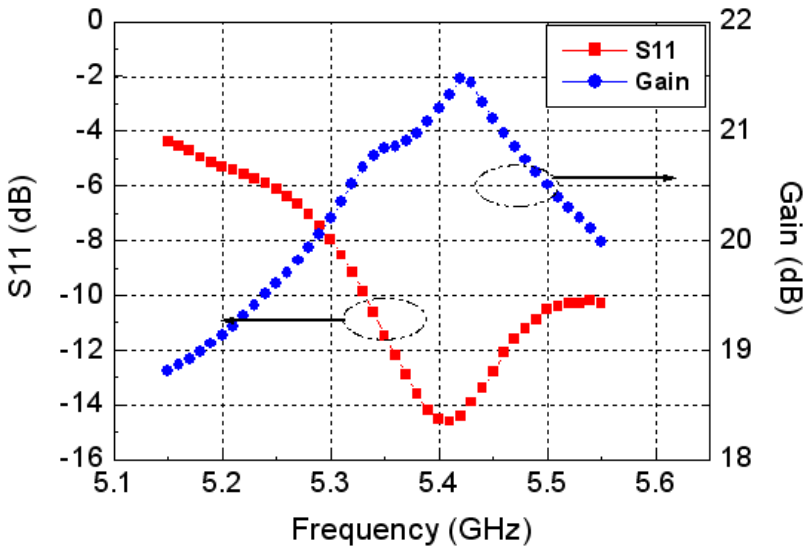


Fig. 3.32 LNA gain and input matching (S11)

5.35GHz) shifts to higher frequency band (5.31GHz ~ 5.51GHz). Fig 3.33 shows the receiver gain and noise figure versus down-conversion output frequency. It reveals that the conversion gain is about 28.2dB at high gain mode and integrated SSB noise figure from 150 kHz to 8.3MHz is about 9.4dB. It shows that frequency tuning range versus frequency control voltage of VCO in Fig 3.34 and it covers from 3.32GHz to 3.79GHz, i.e., it covers from 4.98GHz to 5.49GHz through LO generation.

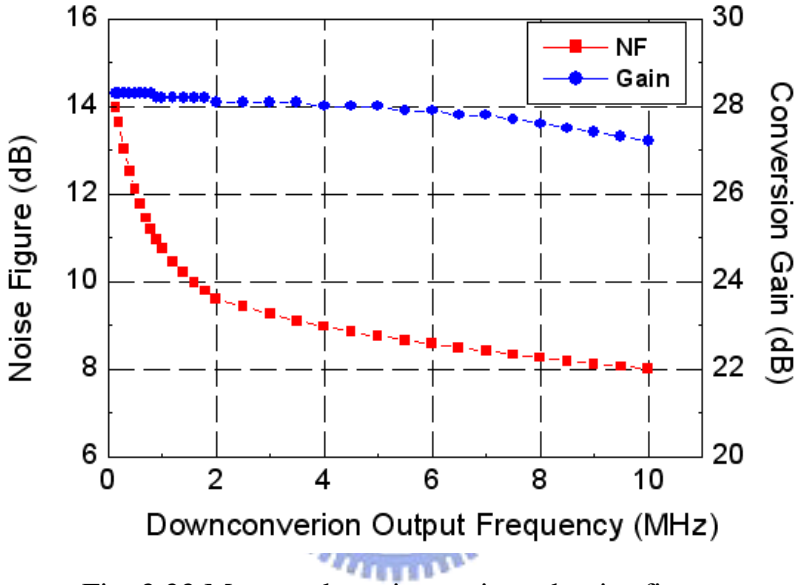


Fig. 3.33 Measured receiver gain and noise figure

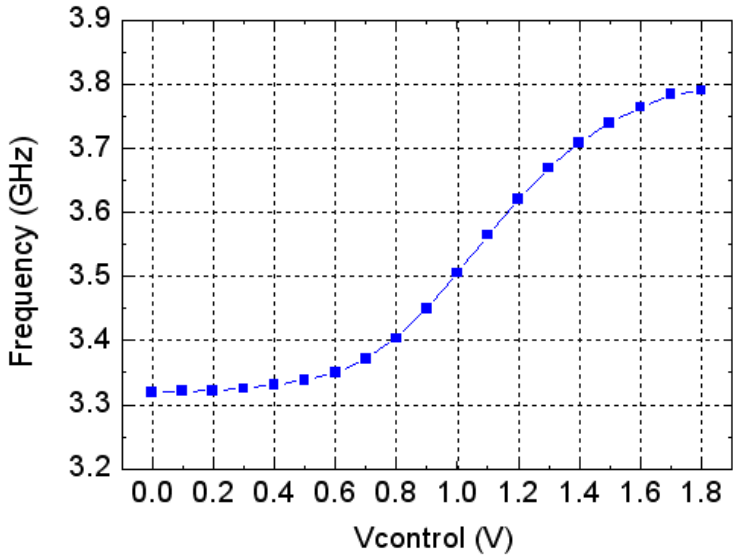


Fig. 3.34 Frequency tuning range versus frequency control voltage of VCO

Two-tone test is applied to measure linearity of the receiver. In Fig 3.35, it shows the measured down-conversion two-tone signals with third-order intermodulation products at high gain mode under input RF power of -36dBm. It reveals that overall receiver is nonlinear. However, in Fig 3.36, it shows that under the same condition the intermodulation tones are much weaker than the amplified signal at low gain mode, thus the linearity of overall receiver will be improved significantly.

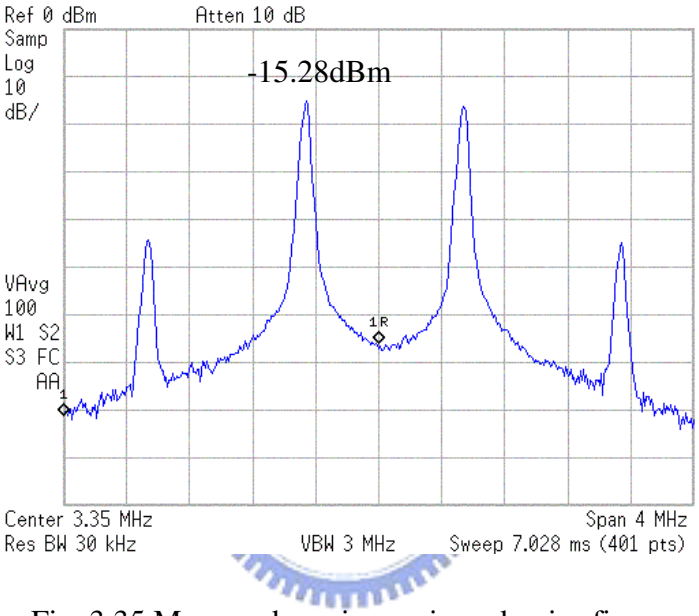


Fig. 3.35 Measured receiver gain and noise figure

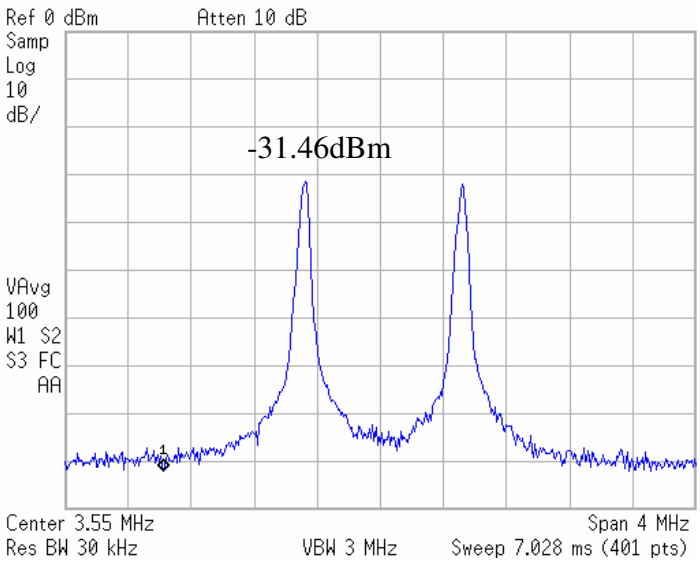


Fig. 3.36 Measured receiver gain and noise figure

By two-tone test, output power of the fundamentals and IM_3 products versus input power at high and low gain modes are plotted in Fig 3.37. It shows that IIP3 is -21.5dBm at high gain mode and -6.8dBm at low gain mode. The low gain mode can improve IIP3 about 15.7dB. In Fig 3.38, it shows the measured I/Q down-conversion waveforms at 3.2MHz before calibration. It reveals that gain error is about 0.4dB and phase error about 2.3°.

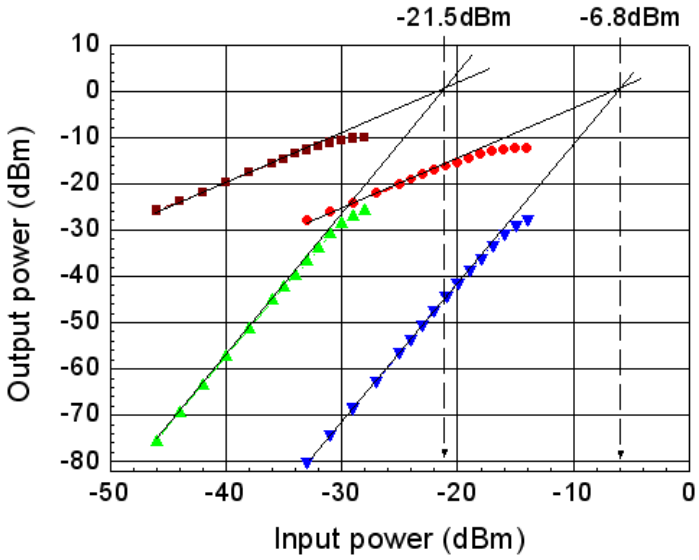


Fig. 3.37 Two-tone test for IIP3 measurement at high/low gain mode

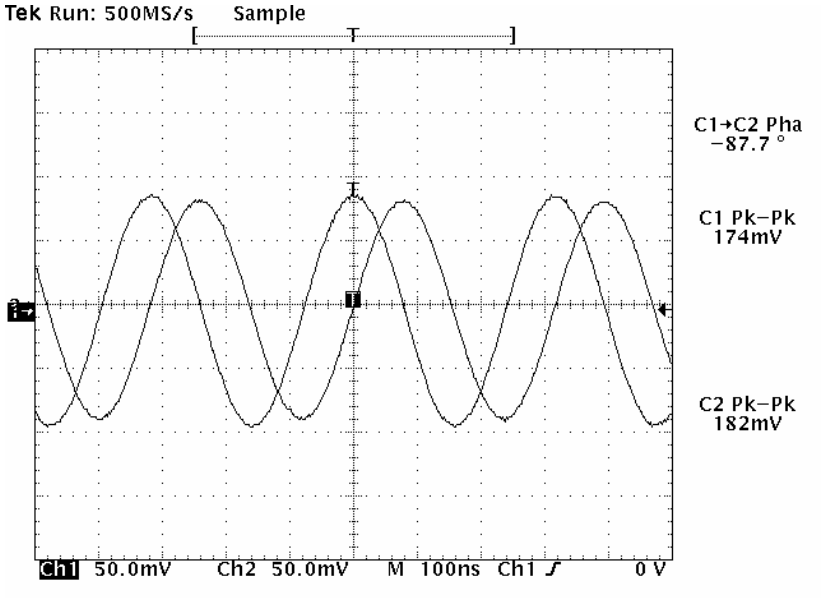


Fig. 3.38 Measured I/Q down-conversion waveforms before calibration

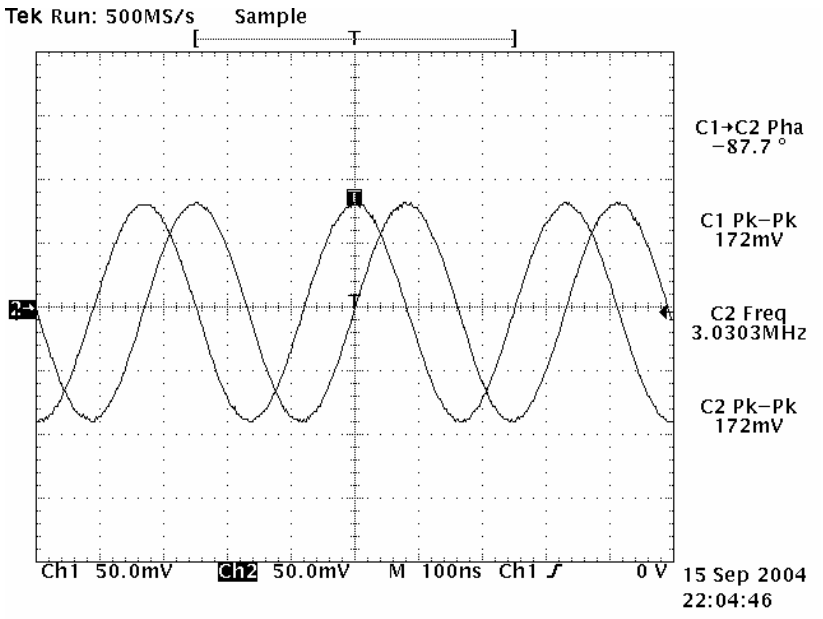


Fig. 3.39 Measured I/Q down-conversion waveforms after gain calibration

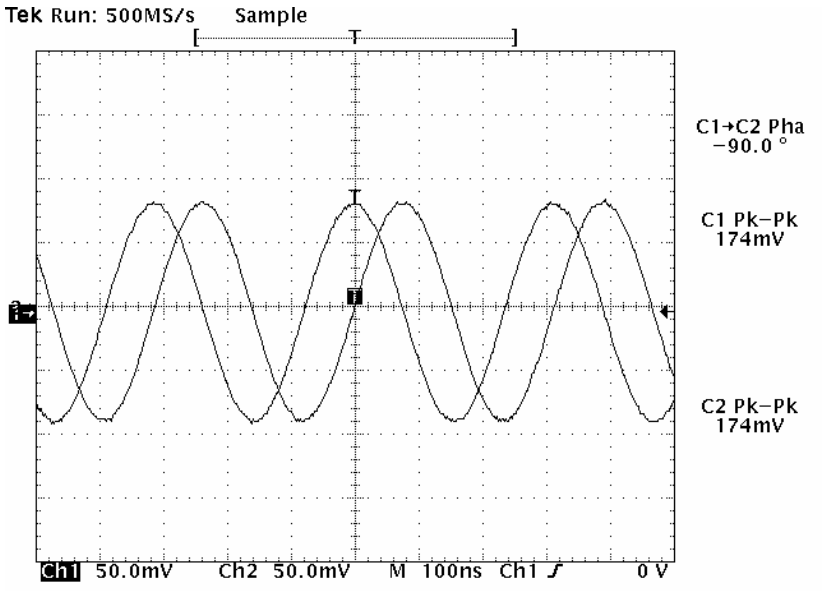


Fig. 3.40 Measured I/Q down-conversion waveforms after gain and phase calibrations

In Fig 3.39, it shows the measured I/Q down-conversion waveforms at 3.1MHz after gain calibration. It reveals that magnitude error is less than 0.2dB after gain calibration but phase error is still 2.3°. In Fig 3.40, it shows the measured I/Q down-conversion waveforms at 3.1MHz after gain calibration. It reveals that gain is error less than 0.2dB and phase error is less than 0.6° after gain and phase calibration.

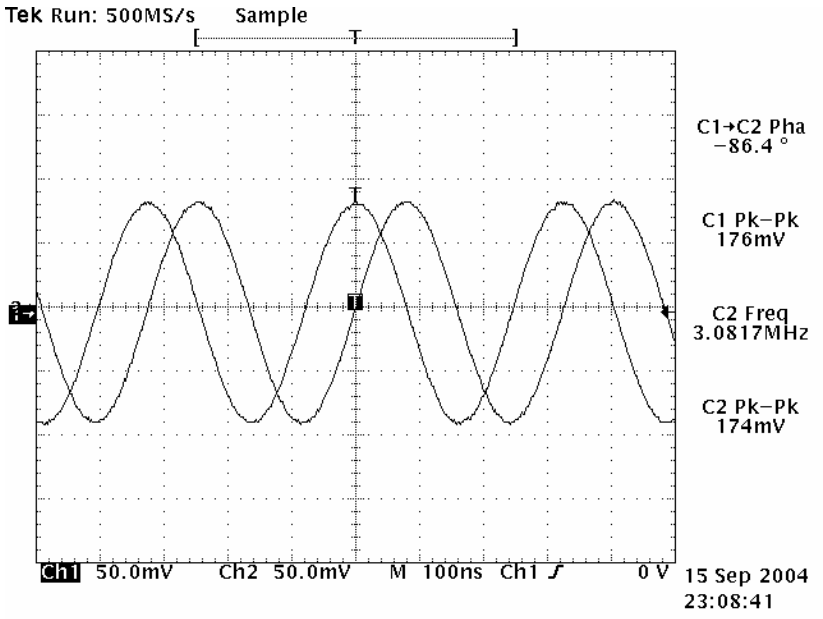


Fig. 3.41 I/Q phase change of first positive step DAC

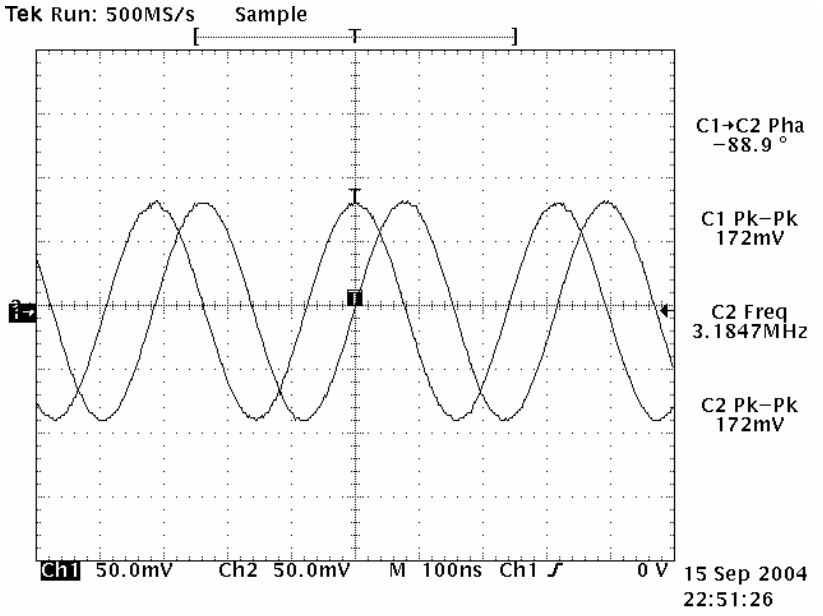


Fig. 3.42 I/Q phase change of first negative step DAC

In Fig 3.41, it shows that I/Q phase change of first positive step DAC is about 1.3° (comparison with I/Q phase shown in Fig 3.39). In Fig 3.42, it shows that I/Q phase change of first negative step DAC is about -1.2° (comparison with I/Q phase shown in Fig 3.39). It reveals that phase resolution per step is about half of 1.2°, i.e. , 0.6°.

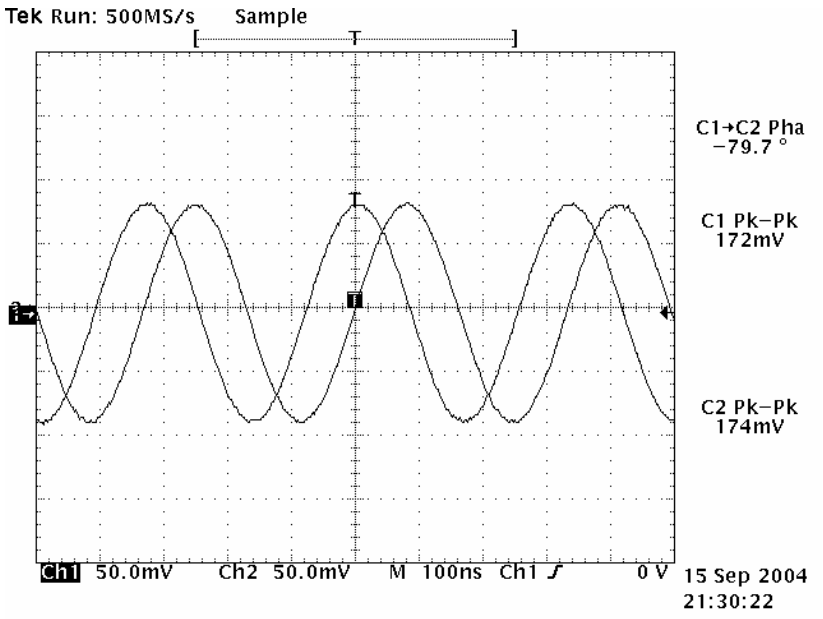


Fig. 3.43 Measured maximum positive change of I/Q phase

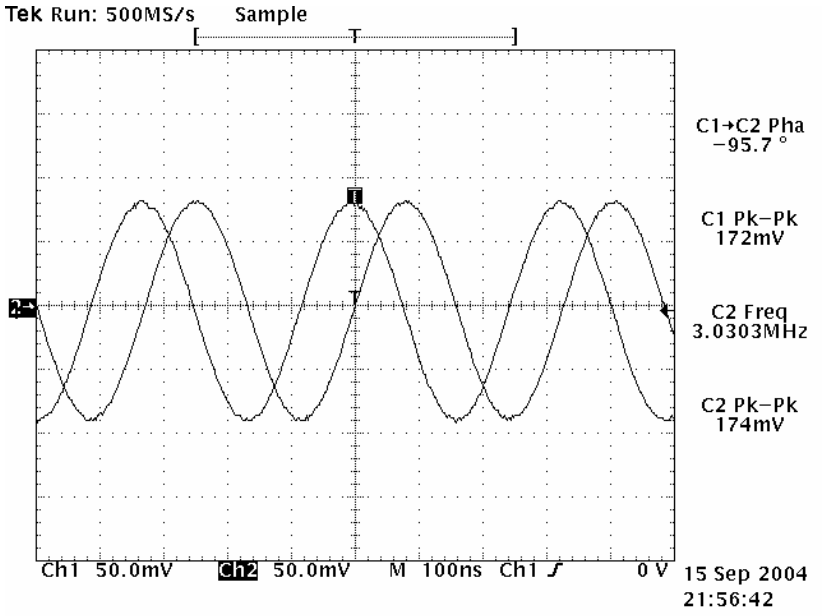


Fig. 3.44 Measured maximum negative change of I/Q phase

In Fig 3.43, it shows that measured maximum positive change of I/Q phase is about 8° (comparison with I/Q phase shown in Fig 3.38). In Fig 3.44, it shows that measured maximum negative change of I/Q phase is about 8° (comparison with I/Q phase shown in Fig 3.39). It reveals that maximum phase error of 8.6° can be calibrated to less than 0.6°.

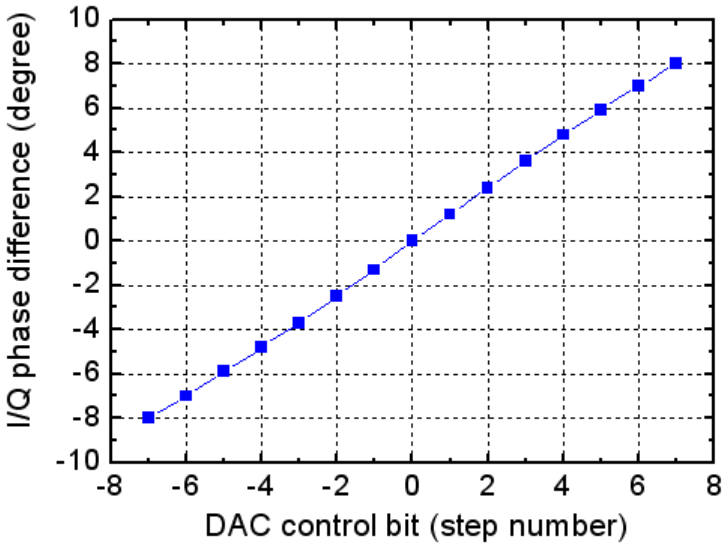


Fig. 3.45 I/Q phase change through DAC control bit

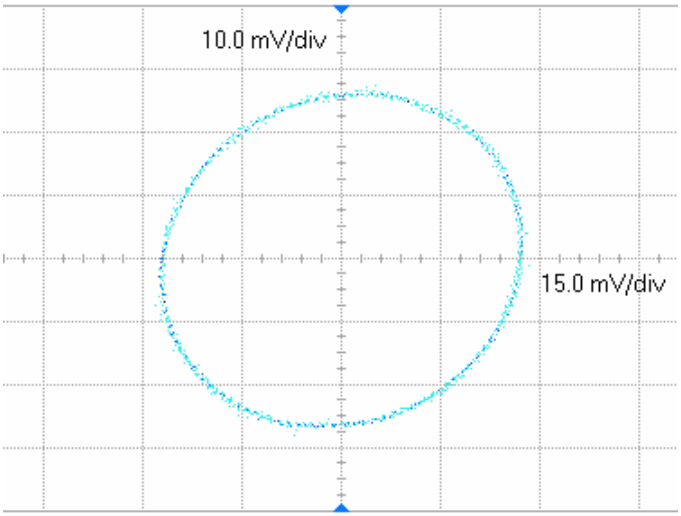


Fig. 3.46 I-Q diagram (before calibration)

It shows that I/Q phase change through DAC control bit in Fig 3.44. It reveals that maximum phase change is 8°, which is less than 9.58° of simulated change shown in Fig 2.11 and minimum phase change is 1.2° , which is less than 1.54° of simulated change shown in Fig 2.11. Fig 3.46 shows the I-Q diagram before calibration and it is like an ellipse because of phase and gain mismatch in signal I/Q path.

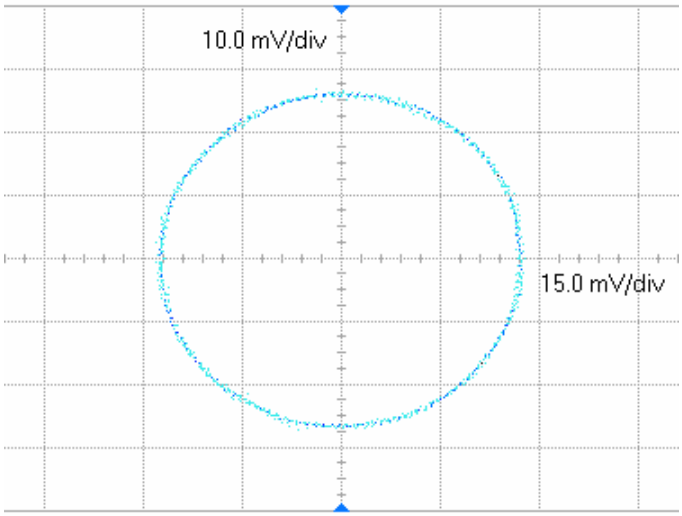


Fig. 3.47 I-Q diagram (after calibration)

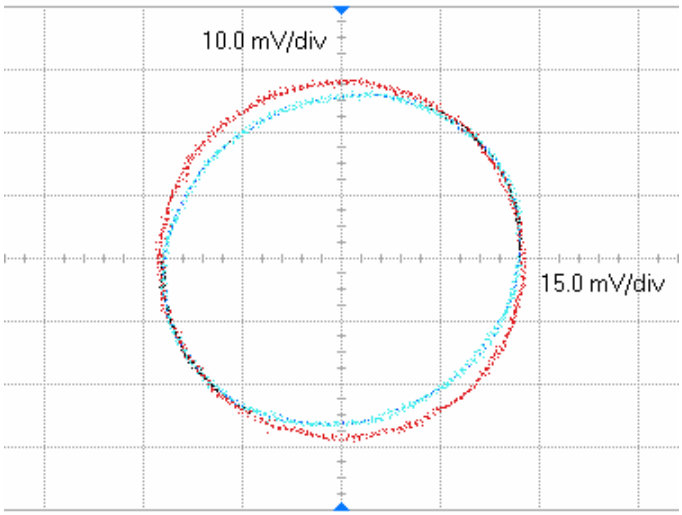


Fig. 3.48 I-Q diagram comparison (calibration or not)

Fig 3.47 shows the I-Q diagram after calibration and it is like a circle because of phase and gain match in signal I/Q path. Fig 3.48 shows the I-Q diagram comparison and it reveals that after phase and gain calibration the I/Q matching considiton is improved.

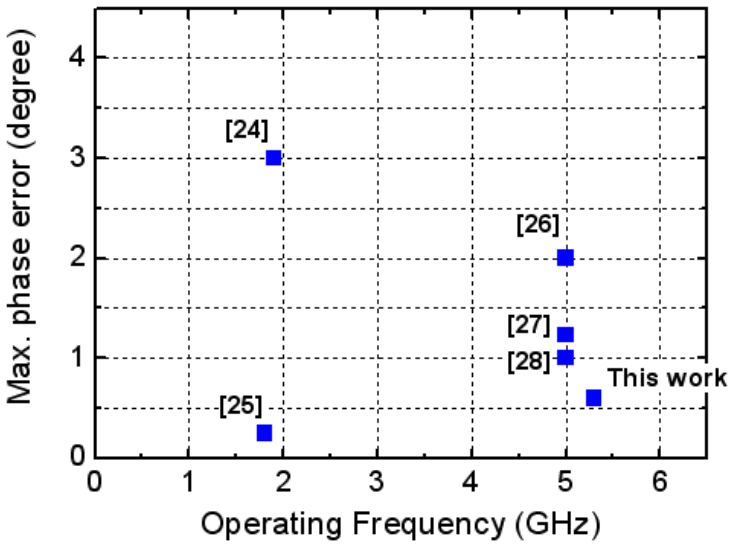


Fig. 3.49 I/Q phase change through DAC control bit

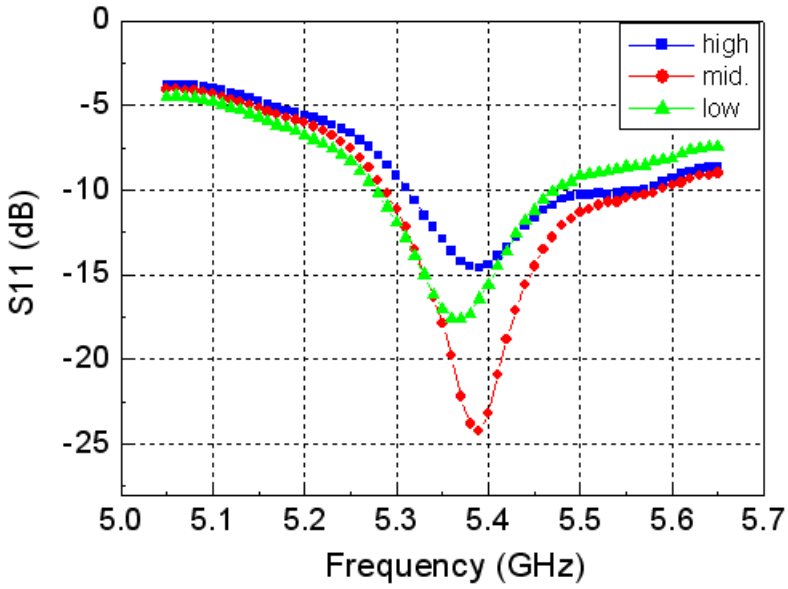


Fig. 3.50 Measured input matching (S11) at different gain modes

Fig 3.49 lists the phase accuracy comparison with the state-of-the-art publications. It reveals that proposed phase error calibration has good performance in this research topic. In Fig 3.50, it shows that measured input matching (S11) at different gain modes and exhibits that measured S11 is less than -10dB at 5.31GHz ~ 5.51GHz.

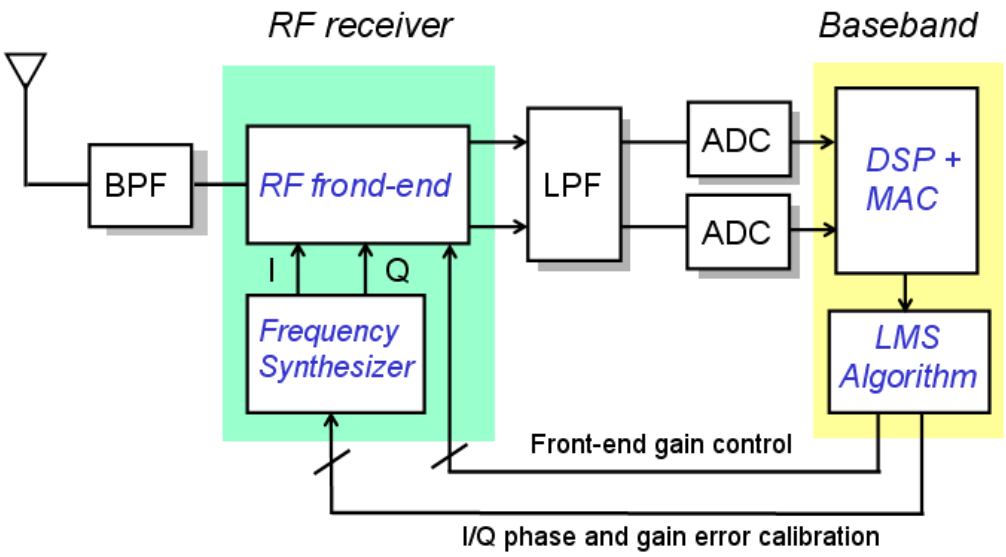


Fig. 3.51 I/Q calibration and gain adjustment controlled by base band DSP using LMS algorithm

Fig 3.51 presents the receiver system suitable for our RF receiver design. First, testing signals are received by RF receiver and then processed by DSP to judge the I/Q mismatch conditions. Then I/Q calibration and gain adjustment are controlled by base band DSP using LMS algorithm to reduce I/Q mismatch and improve overall performance.

Table 3.6 Measurement summary of the receiver

Technology / Supply	TSMC 0.18 um / 1.8V	
Frequency band	5.31 ~ 5.51GHz	
Down-conv. frequency	150k ~ 8.2MHz	
S11	< -10dB	
Gain max / mini	28.2dB / 11.6dB	
LNA gain switch	5.7dB / 11.8dB	
Mixer gain switch	4.8dB	
Noise Figure(SSB)	9.4dB (< 10dB)	
IIP3	-21.5dBm / -6.8dBm (> -16dBm)	
I/Q phase mismatch	< 0.6˚ (< 1.5˚)	
I/Q gain mismatch	< 0.2dB (< 0.2dB)	
Power Consumptions	LNA	5.52mW
	Mixer	9.86mW
	VCO	3.54mW
	I/Q divider	6.34 mW
	LO generator	12.06 mW
	Overall	37.32 mW

Chapter 4

Low Spur Frequency Synthesizer

4.1 Architecture and specification

Fig 4.1 shows the block diagram of integer-N frequency synthesizer and Fig 4.2 shows that output frequency of synthesizer is 2/3 of 802.11a band in this work.

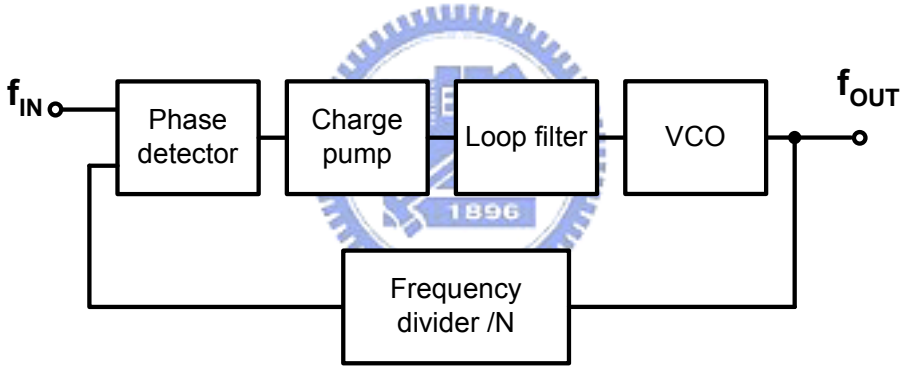


Fig. 4.1 Block diagram of the integer-N frequency synthesizer

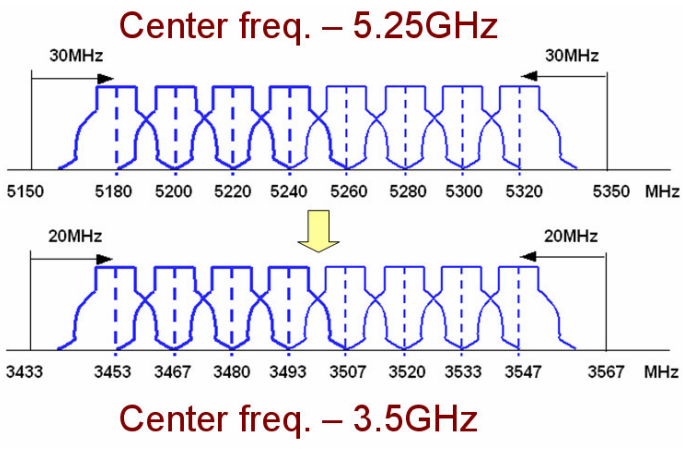


Fig. 4.2 Synthesizer operation frequency transformation

Table 4.1 list the specification and design target in this work.

Table 4.1 Specification and design target

Process / Supply	Gain (dB)
f_{out}	3.44 ~ 3.56 GHz
Channel spacing (f_{ref})	13.33 MHz
Channel number	8
Division number	259 ~ 266
Lock time	< 20us
Phase noise@1MHz	< -113 dBc/Hz

4.2 Phase Noise Consideration

Consider the noise sources of synthesizer, which come from VCO, PFD, charge pump, loop filter, and find the optimum selection of bandwidth for minimum output phase noise. The expressions of noise sources mentioned above are listed in the following:.

$$\frac{\overline{i^2}}{\Delta f} = 4KTgm + \frac{KF_n \cdot gm_n^2}{W_n L_n C_{OX} \cdot f^{AF_n}} + \frac{KF_p \cdot gm_p^2}{W_p L_p C_{OX} \cdot f^{AF_p}} \tag{4.1}$$

$$\frac{\overline{i^2}}{\Delta f} = \frac{4kT}{Rz} \tag{4.2}$$

, where first term from PFD and charge pump, and second term from loop filter.

$$\frac{\theta o, vco}{\theta vco} = \frac{s}{s + KZ(s)Kv/N} = 1 - H(s) \tag{4.3}$$

$$\frac{\theta o, pfd}{\theta pfd} = \frac{F(s)Kv}{s + KdF(s)Kv/N} = \frac{1}{Kd} \cdot H(s) \tag{4.4}$$

$$\frac{\theta o, lf}{\theta lf} = \frac{Kv}{s + KZ(s)Kv/N} = \frac{1}{KZ(s)} \cdot H(s) \tag{4.5}$$

, where first term from VCO, second term from charge pump, and third term from loop filter. Overall noise phase noise can be expressed:

$$\begin{aligned}\Phi o &= \Phi o, pfd + \Phi o, lf + \Phi o, vco \\ &= \left|\frac{1}{Kd}H(s)\right|^2 \Phi pfd + \left|\frac{1}{KdF(s)}H(s)\right|^2 \Phi lf + \left|1-H(s)\right|^2 \Phi vco\end{aligned} \tag{4.6}$$

, where phase noise of VCO is set to -110dBc/Hz at 1MHz offset frequency in initial calculation for phase noise optimum.

From device parameter and equations mentioned above, we can express the overall phase noise by MATLAB simulation as shown in Fig 4.3. In Fig 4.3(a), it shows the in-band phase noise such as charge pump and loop filter and overall phase noise. Here, charge pump current is set to 60uA. In Fig 4.3(b), it shows the out-band phase noise such as VCO and overall phase noise. It reveals that under selection bandwidth of synthesizer equal to 160kHz, we can get the best noise performance of -116dBc/Hz at 1MHz offset frequency.

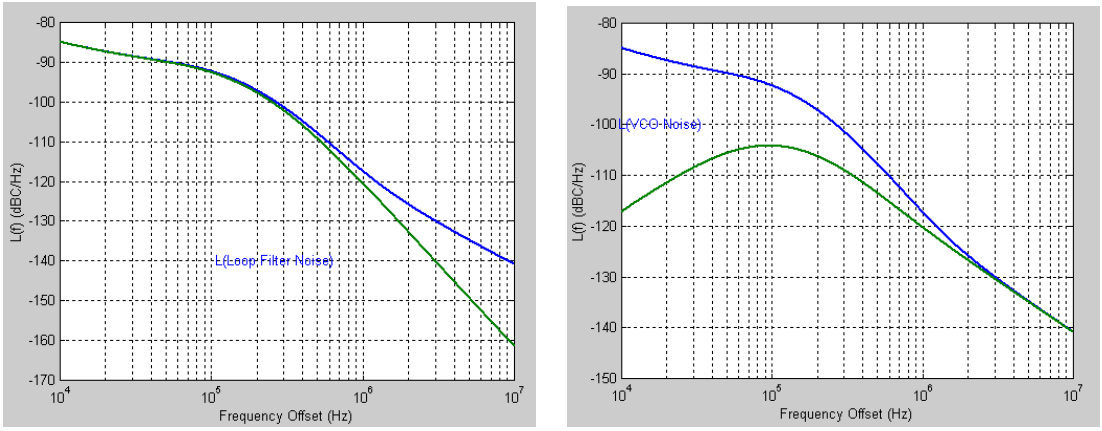


Fig. 4.3 (a) Phase noise of charge pump and loop filter compares with overall phase noise

(b) VCO phase noise compares with overall phase noise

4.3 Circuit implementations

4.3.1 VCO

The VCO employed for synthesizer is mentioned in chapter 3. Thus it is not introduced here. However, comparison with VCO shown in Fig 3.18, this work has extra function, i.e., switchable band (C1 and C2), which is shown in Fig 4.4. Its main function is to cover wider frequency band to overcome process variation and reduce Kvco to improve phase noise and reference spur performance.

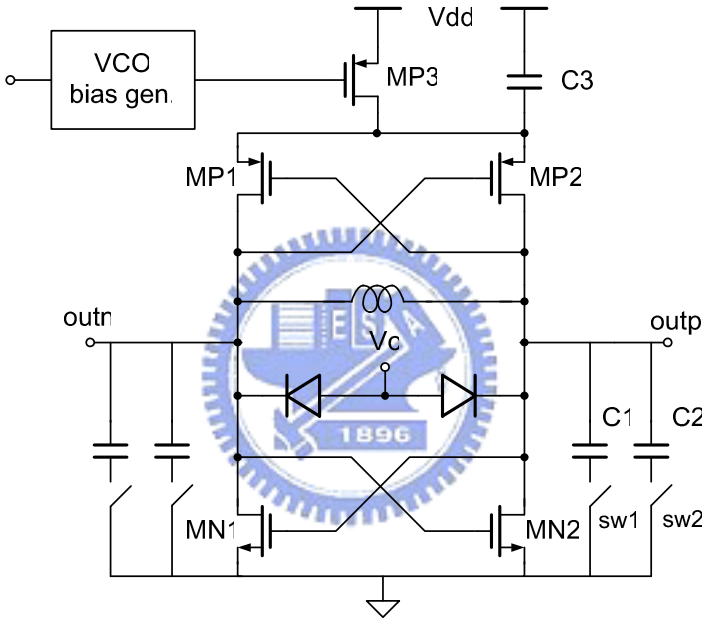
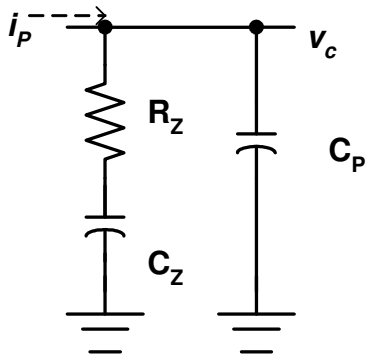


Fig. 4.4 Adaptive biasing VCO with switchable band

4.3.2 Loop filter

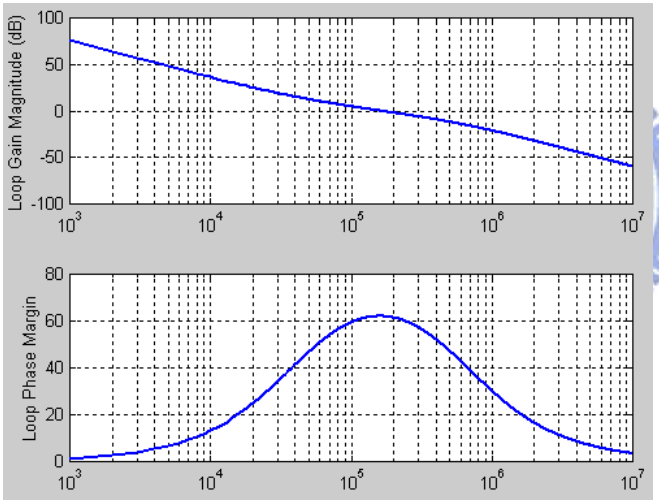
In this work, Kvco is set to 200MHz/V, an adequate selection for phase noise and reference spur consideration. We select a second-order R-C loop filter in our synthesizer. Because of division number, charge pump tail current, bandwidth has determined, it will naturally set the value of R-C if we determine the phase margin of overall loop. In Fig 4.5, it shows the loop filter selection.



Parameter	Value
Rz	23.67 kΩ
Cz	168.54 pF
Cp	11.17 pF

Fig. 4.5 Second-order loop filter

In order to ensure stability of PLL, phase margin of 62° is selected and open-loop analysis is done by MATLAB simulation as shown in Fig 4.6.



Parameter	Value
BW	160 kHz
PM	62°

Fig. 4.6 Open-loop analysis

4.3.3 Programmable frequency divider

For integer-N frequency synthesizer, a pulse swallow counter is needed. In Fig 4.7, it shows the block diagram of frequency divider include a prescaler (/N, /N+1), a 6-bits programmable counter, and a 3-bits swallow counter. The function of pulse swallow counter is to implement the division factors. By changing the division factors, we can choose different channels. Initially, prescaler divides the input frequency by

N+1. The swallow counter counts the prescaler output pulses, until number S is reached. Then the prescaler modulus control is changed, which starts dividing by N. The prescaler output pulses also counted in the programmable counter. If programmable counter has counted P pulses, it reset itself and the swallow counter. The output generates one complete cycle for $(N+1)\cdot S + N\cdot(P-S) = N\cdot P + S$ cycles at the input The operation repeats after the swallow counter is reset. The allocated division number is listed in Table 4.2. The prescalar, program counter and pulse swallow counter block schematic are shown in Fig 4.8, Fig 4.9, and Fig 4.10.

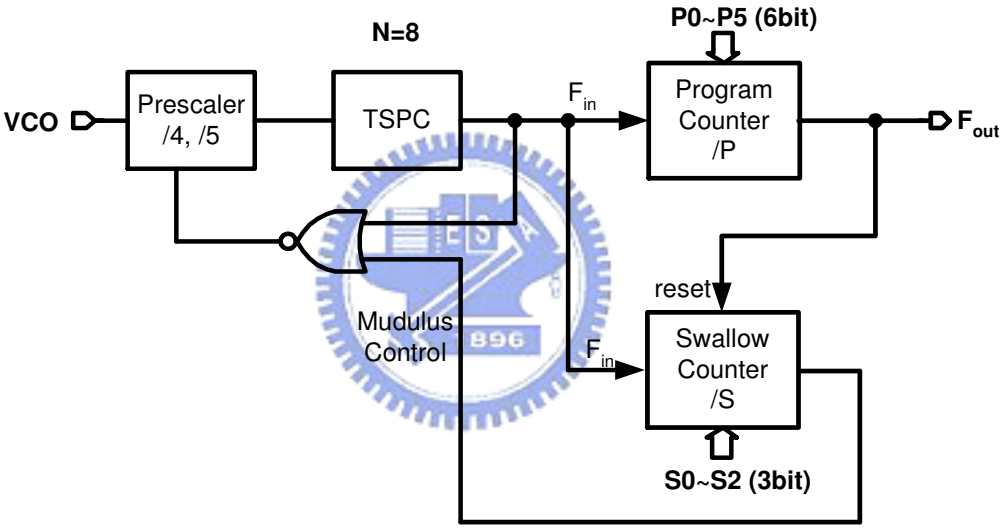


Fig. 4.7 Block diagram of frequency divider

Table 4.2 Allocated division number

Parameter	Value
N	8
P	32 ~ 33
S	0 ~7
Division ratio	259 ~ 266

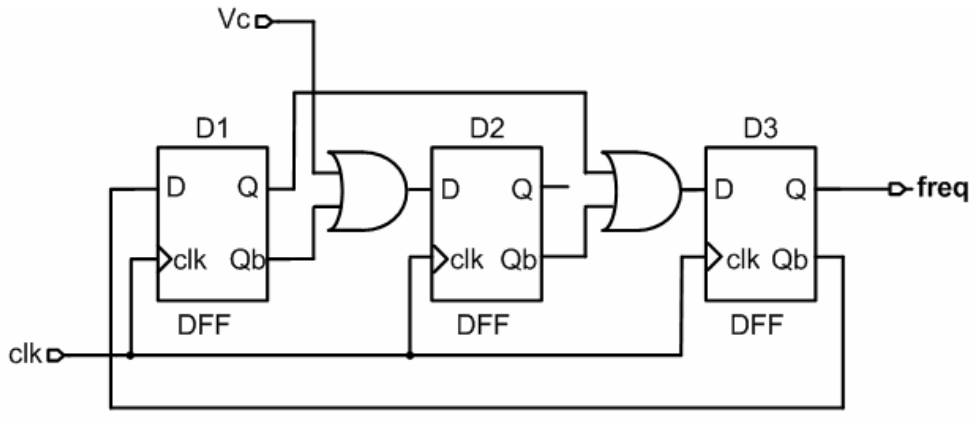


Fig. 4.8 prescalar (/4 , /5)

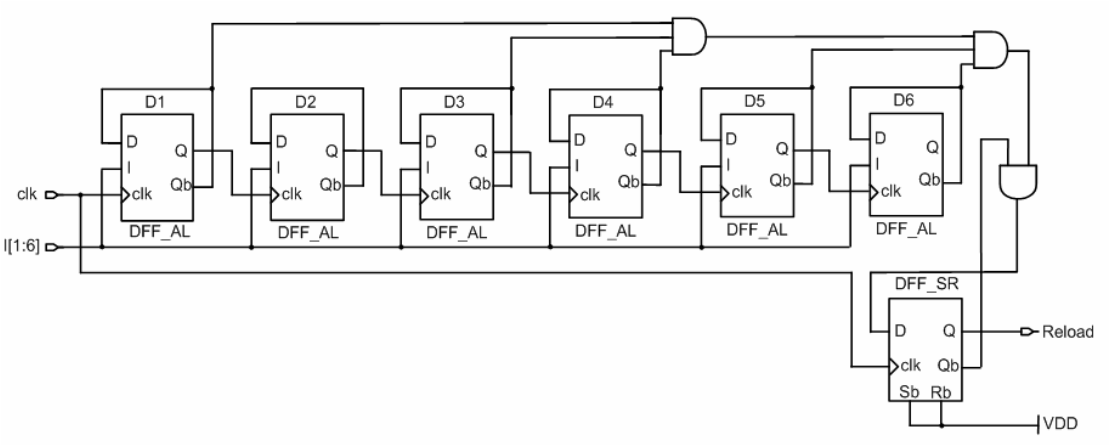


Fig. 4.9 Program counter

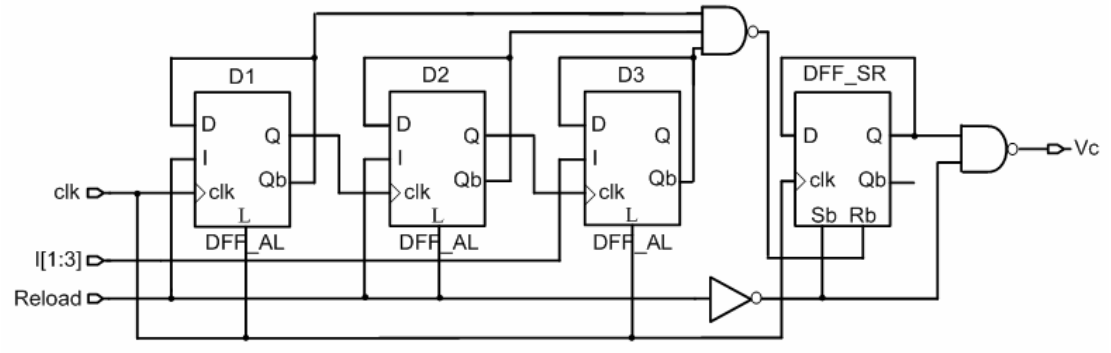


Fig. 4.10 Pulse swallow counter

4.3.4 PFD

Phase frequency detector can detect both phase and frequency difference between the reference signal and the output signal of the frequency divider. The block diagram of employed PFD is shown in Fig 4.11. It can operate at high speed detection because of using simplified TSPC (Fig 4.12) as D-flipflop. The inverters in the reset path generate enough delay to eliminate the dead zone of the charge pump.

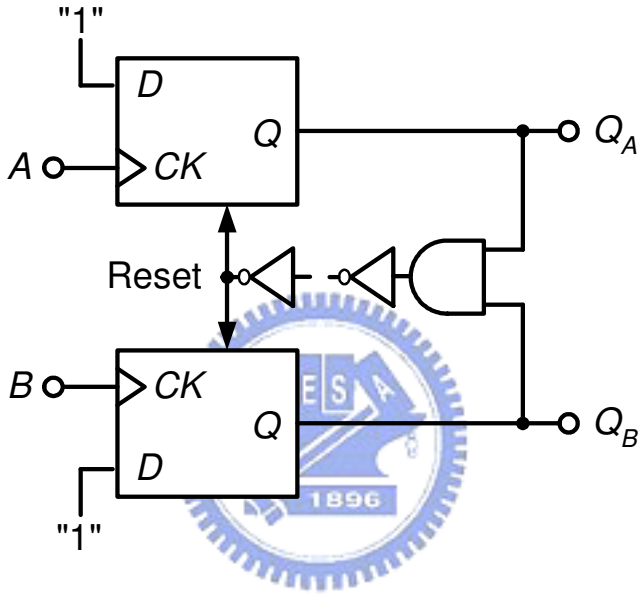


Fig. 4.11 PFD schematic

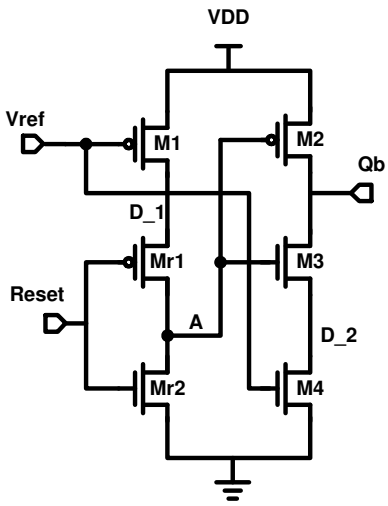


Fig. 4.12 Simplified TSPC

4.3.5 Charge pump

Fig 4.13 [11] shows the circuit diagram of the charge pump and loop filter. In this charge pump the up and down current sources are always on and transistors Mc1-Mc4 are used as switches to steer the current from one branch of the charge pump to the other. The charge pump has a differential architecture, but only a single output node Q_p, drives the loop filter. To prevent node Q_n from drifting to the rail to rail unity gain buffer of the kind shown in Fig 4.14 is placed between the two output nodes. This buffer keeps the two output nodes has the same potential and thus reduces the systematic charge pump offset. The replica switching pair prevents the current sources of charge pump from operating at triode region, thus reduces charge sharing. The power of the synthesizer spurious sidebands is thereby reduced.

To compensate the fine output impedance of the up and down current sources and match their currents more precisely over all output voltages, the up and down currents are monitored in a replica circuit. A feedback network measures the output voltage, Vo, and the voltage of the replica circuit, Vr, and thereby equates the up and down currents at every output voltage.

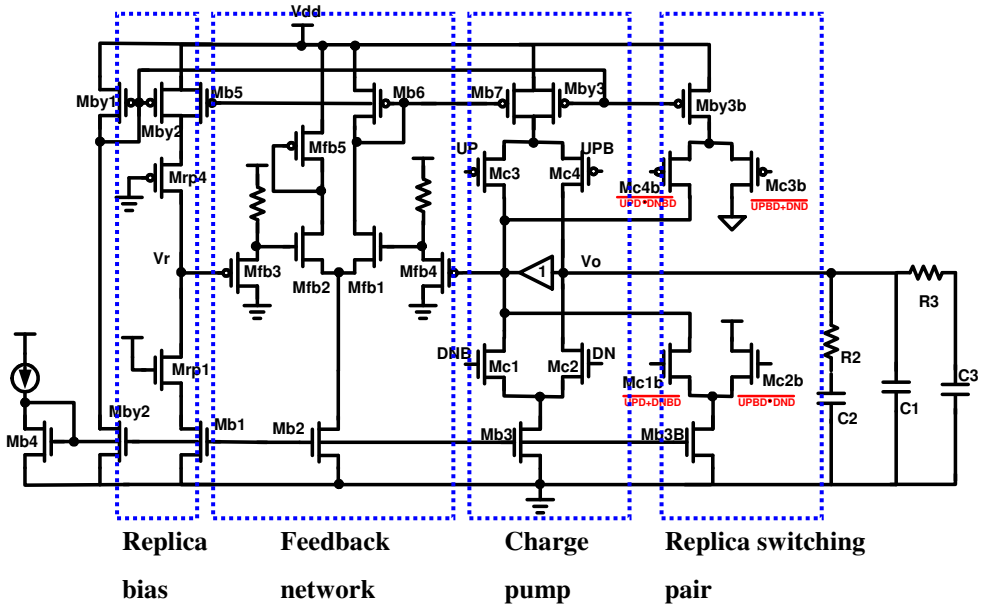


Fig. 4.13 Schematic of charge pump

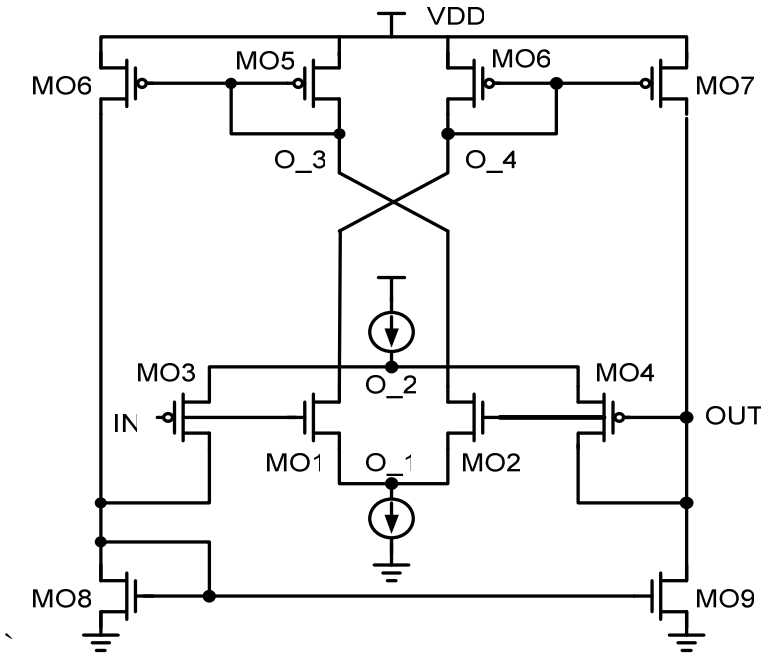


Fig. 4.14 Schematic of the unity gain buffer used in the charge pump

4.4 Simulation Results

Fig 4.15 shows that output frequency of VCO versus control voltage with switching band and reveals that 3.32GHz ~ 3.69GHz is covered. Fig 4.16 and Fig 4.17 show that prescalar output waveforms at different modules. Fig 4.18 shows that Current pump current matching condition and reveals that current mismatch is less than 3% between 0.4V and 1.4V of control voltage. Fig 4.19 shows that replica switching pair avoids charge sharing effect. Fig 4.20 shows that PFD dead zone simulation and reveals the operating is very linear and zero dead zone. Fig 4.21 shows that close-loop response simulation and reveals that lock time is about 18us. Table 4.3 lists the synthesizer performance summary.

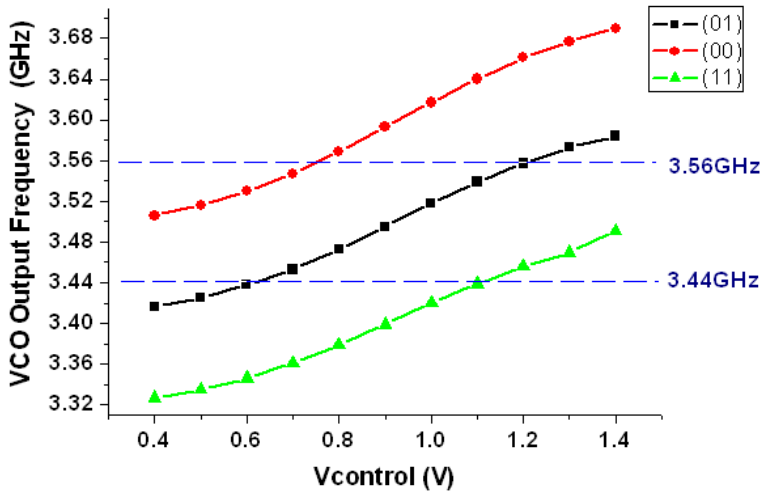


Fig. 4.15 Output frequency versus control voltage with switching band

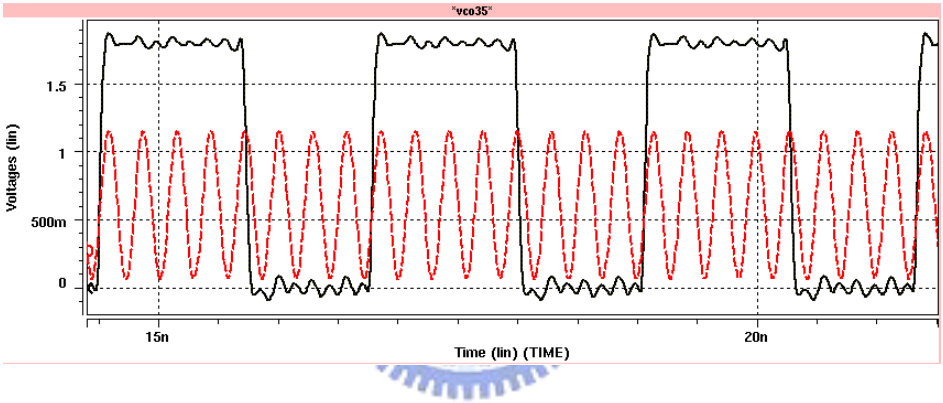


Fig. 4.16 Output waveform of dividing by 8

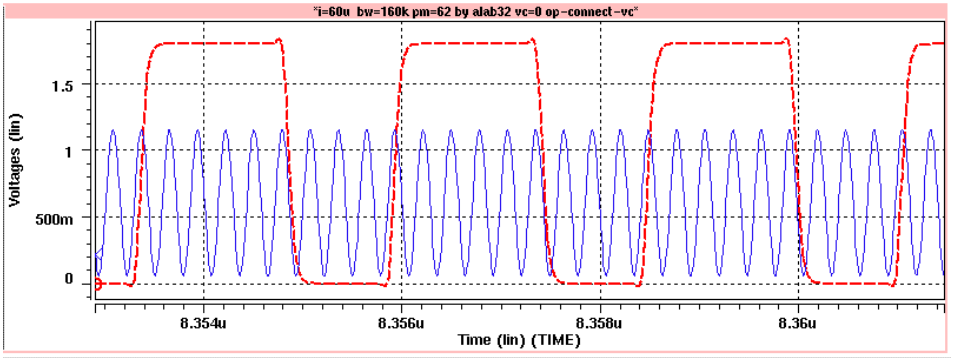


Fig. 4.17 Output waveform of dividing by 9

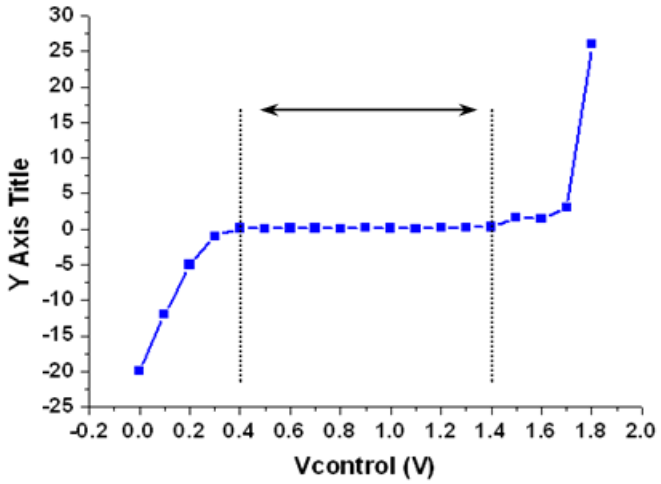


Fig. 4.18 Current pump current matching condition

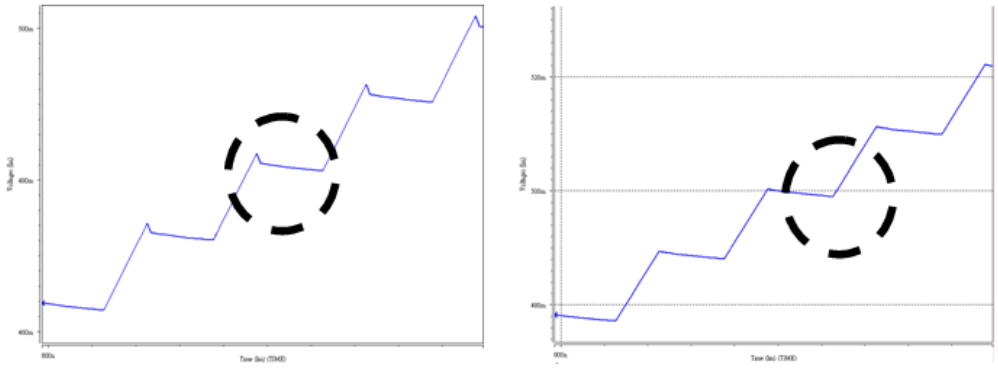


Fig. 4.19 Replica switching pair avoids charge sharing effect

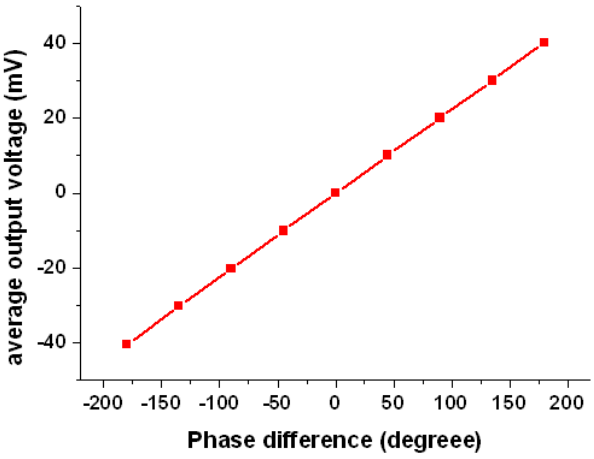


Fig. 4.20 PFD dead zone simulation

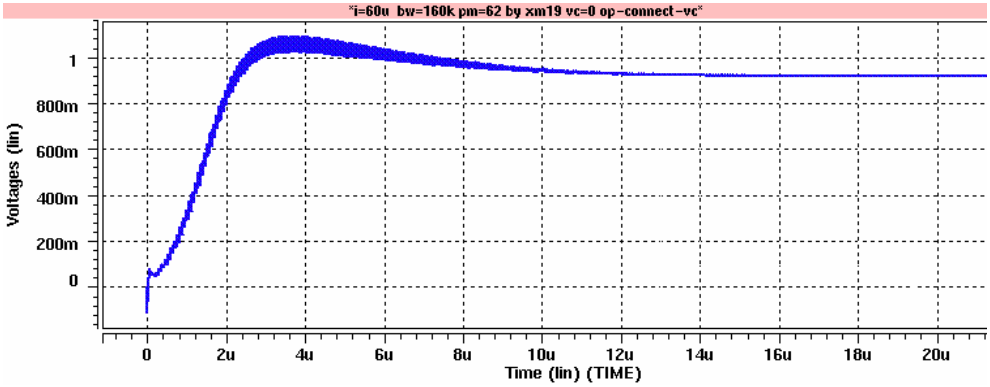


Fig. 4.21 Close-loop response simulation

Table 4.3 Synthesizer performance summary

Process / Supply		TSMC 0.18-μm / 1.8V
Frequency range		(3.362~3.474GHz) (11) (3.437~3.557GHz) (01) (3.529~3.660GHz) (00)
Reference frequency		13.33 MHz
Lock time		18us (< 20us)
Loop bandwidth		160 kHz
Phase noise @1MHz		-117 dBc/Hz (< -113 dBc/Hz)
Division ratio		259 ~ 266
Power	VCO	3.2 mW
	Frequency divider	8.8 mW
	Rest of synthesizer	1.4 mW
	Output buffer	20.6 mW

Chapter 5

Conclusions

In chapter 2, the proposed I/Q mismatch calibration techniques has been implemented using TSMC 0.18um CMOS technology. Frequency plan of the LO generation avoids VOO-pulling and reduce LO-RF interaction. And calibration performance is evaluated by measuring the image-rejection ratio (IRR). The measured IRR after calibration is 28.25dB. According to measured IRR, we estimated that gain error is about 0.66dB and phase error is less than 1°.

In chapter 3, a 1.8V, 5-GHz direct conversion front-end receiver using TSMC 0.18um CMOS technology is proposed. By calibrated techniques mentioned in chapter 2, measured results show that I/Q phase error less than 0.6° and gain error less than 0.2dB can be achieved, thus I/Q phase and gain calibrations were implemented successfully. In addition, adaptive gain control of both LNA and mixer provides the feasibility for optimizing its gain, noise, and linearity performance. This I/Q calibration technique facilitates the realization of high performance and high yield RF receiver in a generic CMOS process. It consumes chip area of $1.64mm^2$ and power of 37.25mW at 1.8V supply voltage.

In chapter 4, a frequency synthesizer operating at 2/3 of required RF frequency has been implemented. A novel charge pump with improved current matching is

proposed to effectively reduce reference spurs. And low phase noise frequency synthesizer design methodology is proposed. It consumes chip area of 1.06mm^2 and power of 14.4mW at 1.8V supply voltage.

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