具有 LVDS 與 RSDS 低電壓差動訊號傳輸規格之平面顯示器高速輸入輸出緩衝器設計

學生: 莊 凱 嵐　　指導教授: 柯 明 道 博士

國立交通大學

電子工程學系　電子研究所碩士班

摘要

今日平面顯示器持續在提供其色彩濃度與解析度的增加。很多面板製造業者都已經可以量產解析度超過 SVGA (800 × 600 像素) 和 XGA (1024 × 768 像素) 的平面顯示器。隨著平面顯示器解析度的快速增加，位於平面顯示器系統裡直接連接顯示卡到液晶顯示時脈控制器以及液晶顯示時脈控制器到面板驅動電路的介面應該操作於更高的資料傳輸速度。因此，位於平面顯示器系統介面的高速輸入輸出緩衝器設計是有其必要的。本論文共包含三個設計子項，透過三個獨立下線的晶片來驗證這些設計。

第一個設計為採用 0.25-μm 1P5M CMOS 製程技術所實現的一個相位鎖相迴路，其電源電壓為 2.5 V。其所設計的輸出時脈頻率為 200 MHz 而由於使用一個除八的除頻器故輸入參考時脈頻率為 25 MHz。

第二個設計為採用 0.25-μm 1P5M CMOS 製程技術所實現的三個輸入輸出緩衝器，其電源電壓為 3.3 V。這些輸入輸出緩衝器可跟低電壓差動訊號傳輸規格和更小擺幅差動訊號傳輸規格完全相容。此兩種低電壓差動訊號傳輸規格和更小擺幅差動訊號傳輸規格都是用來定義平面顯示器系統裡的介面傳輸。這些輸入輸出緩衝器的資料傳輸速度可以到達每秒 1.2 十億位元 (1.2 Gb/s)，其可以支援解析度為 UXGA (1600 × 1200 像素) 的平面顯示器。

第三個設計為一個可以將 28 位元的大擺幅 (3.3 V) 並列資料轉換成四條

低電壓差動訊號傳輸資料流或更小擺幅差動訊號傳輸資料流的傳送器，其採用 0.25-μm 1P5M CMOS 製程技術而其電源電壓為 3.3 V。位於傳送器的相位鎖相迴路擁有七個不同的時脈相位以便將輸入的資料做並列轉串列的轉換。傳送器的資料操作速度可以到達每秒 1.05 十億位元 (1.05 Gb/s)，其可以支援解析度為 SXGA (1280 × 1024 像素) 的平面顯示器。

Co-Design on High-Speed I/O Buffers With Both LVDS and RSDS Standards for Flat Panel Display Applications

Student: Kai-Lan Chuang Advisor: Prof. Ming-Dou Ker

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT

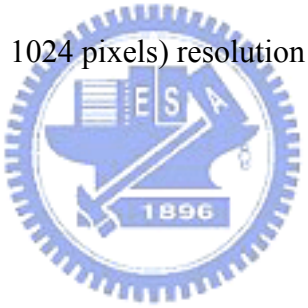
Flat panel displays (FPDs) continue to offer an increase in color depth and resolution, today. Beyond the SVGA (800 × 600 pixels) and XGA (1024 × 768 pixels) resolutions of flat panel displays are ready for production by many flat panel manufacturers. As the resolution of FPDs is increasing rapidly, the interfaces that directly connect a graphics card to a liquid crystal display (LCD) timing controller and a LCD timing controller to flat panel column drivers in FPD systems should be operated at a higher data rate. Therefore, high-speed I/O buffers designed for interfaces in FPD systems are necessary. This thesis includes three topics, which were verified through 3 individual chips.

In the first topic, a phase-locked loop (PLL) has been implemented in a 0.25-μm 1P5M CMOS process and the power supply is 2.5 V. The designed output clock frequency is 200 MHz and the input reference clock frequency is 25 MHz due to the divided by eight divider.

In the second topic, three I/O buffers have been fabricated in a 0.25-μm 1P5M

CMOS process and the power supply is 3.3 V. These I/O buffers are fully compatible with both low-voltage differential signaling (LVDS) standard and reduced-swing differential signaling (RSDS) standard. Both LVDS and RSDS standards are defined for interface transmission in FPD systems. The data rates of these I/O buffers are up to 1.2 Gb/s which can support the UXGA (1600 × 1200 pixels) resolution of flat panel displays.

In the third topic, a transmitter which converts 28 bits of full-swing (3.3 V) parallel data into four LVDS or RSDS data streams has been implemented in a 0.25-μm 1P5M CMOS process and the power supply is 3.3 V. The PLL in the transmitter has seven different clock phases in order to perform parallel-to-serial conversion of incoming data. The data rate of the transmitter is up to 1.05 Gb/s which can support the SXGA (1280 × 1024 pixels) resolution of flat panel displays.



誌謝

回顧快兩年的碩士求學生涯，這過程真可以酸甜苦辣、五味雜陳來形容。這其中最苦的時期在於碩一剛入學時，由於當時心態尚未調適過來以至於在修課方面充滿著極大的挫折感與無力感。幸而在實驗室周千譯學長適時的精神鼓勵讓我能在幾乎要放棄的情況下咬緊牙根撐過最苦的日子，這不但讓我對日後的修課不再畏懼也對未來所面臨到更困難的挑戰具有更高的抗壓性。回顧這段往事真使我覺得自己何其幸運，能在最無助的時候得到實驗室師長最正面的幫助，這也使我懷著最真誠的心，深深感謝生活中每一個貴人。

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莊凱嵐

九十三年六月

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Chapter 1
Introduction

1.1 MOTIVATION

With the rapid technology scaling and increasing operation frequencies, the internal clock frequency in microprocessors is up to gigabits-per-second range. However, unlike internal clocks, chip-to-chip or chip-to-board signaling gains little benefit in terms of operating frequency from the increased silicon integration. It means that the biggest bottleneck for designing the ever-increasing processing speed of microprocessor motherboards, optical transmission links, flat panel display systems, intelligent hubs and routers, etc., is the I/O interface transmission between chips to chips or chips to boards.

In the last decade, high-speed I/O interfaces were achieved by massive parallelism with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). However, such method also consumes huge power and induces unavoidable electro-magnetic interference (EMI) during signal transmission [1]. In order to save power, area and cost, the number of I/O pads in systems should be reduced. Therefore, parallel-based technologies need to be changed to serial-based technologies.

The serial link technology can lower the numbers of transmission lines to decrease power, volumes, cost and EMI. The population applications are optical communication, USB, IEEE-1394, TMDS, PECL, LVDS and RSDS. Some industrial standards of high-speed serial link are listed in Table 1.1.

1.2 BASIC SERIAL-LINK TRANSCEIVER ARCHITECTURE

The components of basic serial-link transceiver architecture, as shown in Fig. 1.1, are a parallel-to-serial conversion circuit, a transmitter, a channel, a receiver, and a serial-to-parallel conversion circuit. The data before transmitted are usually parallel data stream in order to increase the bandwidth of the link. Therefore, a parallel-to-serial conversion circuit is needed before sending data to the transmitter. The transmitter converts digital information to analog signal on the transmission medium. This medium which signals travel on is commonly called the communication channel such as the coaxial cable or the twisted pair cable. The receiver on the other end of the channel recovers the signal to the original digital information by amplifying and sampling the signal. The termination resistors which match the impedance of the channel could minimize signal reflection in order to have better signal quality. The clock recovery circuit at the receiver is used to adjust the receiver clock based on the received data to let the sampling point at the middle of the received data. Then, a serial-to-parallel conversion circuit is used to convert the serial data back to N parallel bits in order to be processed by following digital circuits.

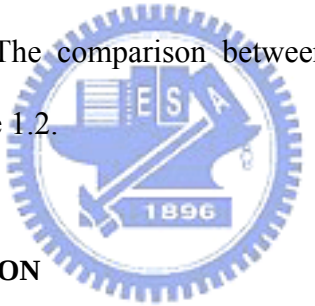
1.3 HIGH-SPEED AND LOW-POWER TRANSCEIVER CIRCUITS DESIGN

A high performance transceiver circuit must consider speed, power consumption, cost and noise. However, the four factors are trade-off to each other. On balance, the low output signal swing and differential data transmission are the good choice for designing a high performance transceiver circuit. Signals transmitted with low voltage swing can minimize power dissipation and enable operation at very high speed. The differential transmission can provide adequate noise margin in practical systems since

signals are transmitted with low voltage swing.

The controversial point is to use the differential transmission. It costs twice of connectors and transmission lines. However, reliable single-ended signals require many ground pins (many high-speed chips and/or backplanes provide one ground pin for every two signal pins) and run significantly slower. And for noise concern, any noise that is coupled into both transmission lines of the signal path will be rejected at node 1 and node 2 in receiver, as shown in Fig. 1.2, due to the common-mode rejection of the differential amplifier. Besides, for EMI aspect, differential signals tend to radiate less EMI than single-ended signals due to the canceling of magnetic fields.

There are currently many different transmission technologies that are applied for different I/O interfaces [2]. The comparison between these different transmission technologies is shown in Table 1.2.



1.4 THESIS ORGANIZATION

The chapter 2 of the thesis discusses the low-voltage differential signaling (LVDS) standard and the reduced-swing differential signaling (RSDS) standard. The detail DC specifications and applications of both standards are presented. In the chapter 3, a phase-locked loop (PLL) is described and the simulation results are in the final section. In the chapter 4 and 5, three I/O buffers and the complete transmitter for flat panel display applications are implemented. The new proposed I/O buffers with both LVDS and RSDS standards are presented and detail circuit functions of the transmitter are discussed. The last chapter recapitulates the major consideration of this thesis and concludes with suggestion for future investigation.

Table 1.1

Industrial standards for high-speed serial link.

Standard	Speed
USB 2.0 (High Speed)	480 Mb/s
RAM Bus	800 Mb/s
IEEE 802.3	1 Gb/s
IEEE 1394b	1.6 Gb/s ~ 3.2 Gb/s
SONET OC-48	2.4883 Gb/s

Table 1.2

Comparison between different transmission technologies

that are applied for different I/O interfaces.

	RS-422	PECL	LVDS	RSDS	Optics	GTL	TTL
Signaling type	Diff.	Diff.	Diff.	Diff.	Single-ended	Single-ended	Single-ended
Transmitter output voltage swing (mV)	+/- 2000 ~ +/- 5000 (typical +/-2000)	+/- 600 ~ +/-1000 (typical +/- 800)	+/- 250 ~ +/- 450 (typical +/- 350)	+/- 100 ~ +/- 400 (typical +/- 200)	n/a	1200	2400
Receiver input threshold voltage (mV)	+/- 200	+/- 200 ~ +/-300	+/- 100	+/- 100	n/a	100	1200
Speed (Mb/s)	< 30	> 400	> 400	> 400	> 1000	< 200	< 100
Dynamic Power	Low	High	Low	Low	Low	High	High
Noise	Low	Low	Low	Low	Low	Med	High
Cost	Low	High	Low	Low	High	Low	Low

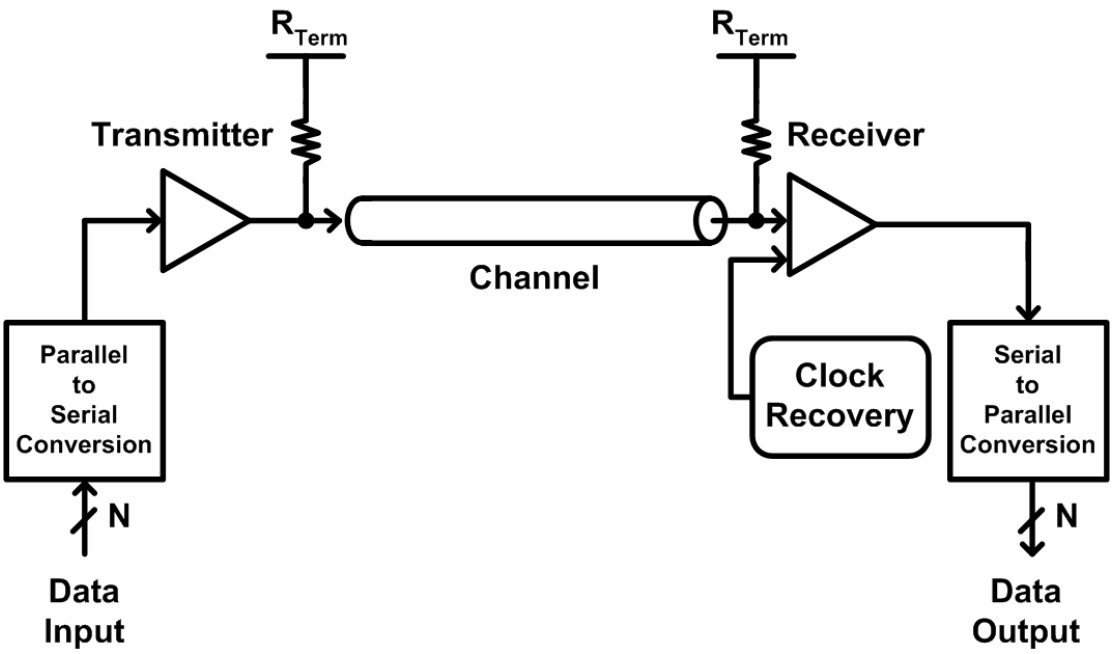


Fig. 1.1 Basic serial-link transceiver architecture.

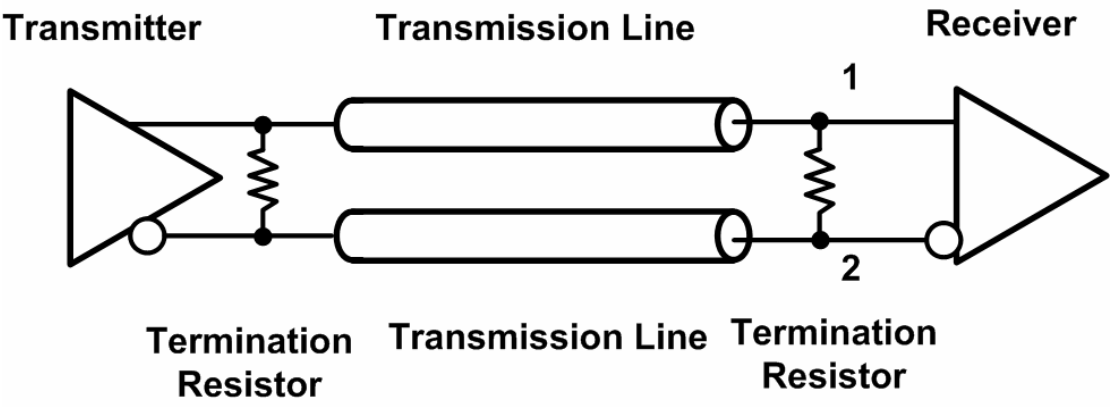


Fig. 1.2 Reduce noise and suppress EMI effect by using the differential transmission technology.

Chapter 2

Specifications of Low-Voltage Differential Signaling (LVDS) Standard and Reduced-Swing Differential Signaling (RSDS) Standard

2.1 BACKGROUND

Recent growth in high-end processors, multi-media, virtual reality and networking have demanded more bandwidth than ever before. But the point-to-point physical layer interfaces have not been able to deal with moving information at the data rates required. Some of today's biggest challenges that remain to be solved include the ability to transfer data fast, lower power systems than currently available, and economical solutions to overcome the physical layer bottleneck. Data transmission standards such as RS-422, RS-485, SCSI and others all have their own limitations most notably in transferring raw data across a medium. Therefore, low-voltage differential signaling (LVDS) is a high-speed (> 400 Mb/s), low-power general purpose interface standard that solves the bottleneck problems while servicing a wide range of application areas.

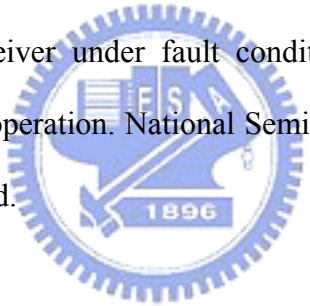
2.2 TWO STANDARDS OF LVDS

There are two industry standards that define LVDS [3]. The more common of the two is the generic electrical layer standard defined by the TIA (Telecommunications Industry Association) [4]. This standard is known as ANSI/TIA/EIA-644. The other

application specific standard is the IEEE (Institute for Electrical and Electronics Engineering) standard which is titled SCI (Scalable Coherent Interface).

2.2.1 ANSI/TIA/EIA-644

This standard defines driver output and receiver input characteristics. Functional specifications and/or protocols are not within the scope of the TIA standard. It notes a recommended maximum data rate of 655 Mb/s and a theoretical maximum of 1.923 Gb/s based on a loss-less medium. However, maximum data rate is application (desired signal quality), and device specific (transition time). It is feasible that LVDS based interface will operate in the 500 Mb/s to 1.5 Gb/s range in the near future. Minimum media specifications are also defined within the standard. It also discusses failsafe operation of the receiver under fault conditions and other configurations issues such as multi-receiver operation. National Semiconductor Corporation held the editor position for this standard.



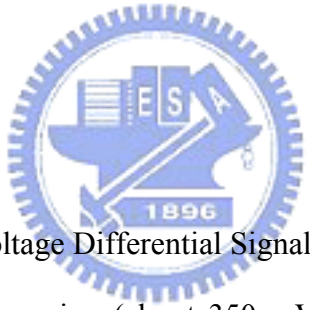
2.2.2 IEEE 1596.3 SCI-LVDS

SCI originally referenced a differential ECL (Emitter Coupled Logic) interface within the SCI 1596-1992 IEEE standard [5]. However, this only addressed the high data rates required and did not address the low power concerns. Thus, SCI-LVDS was defined as a subset of SCI, and is specified in IEEE 1596.3 standard. SCI-LVDS specifies signaling levels (electrical specifications) for the high-speed/low-power physical layer interface. It also defines the encoding for packet switching used in SCI data transfers. Packets are constructed from 2-byte (doublet) symbols. This is the fundamental 16-bit symbol size. No media are specified and the data rate can be in the order of 500 MT/s based on serial or parallel transmission of 1, 4, 8, 16, 32, and 64 ... bits. The IEEE 1596.3 standard was approved in March 1994. National

Semiconductor Corporation held the chairperson position for this standard. SCI-LVDS is similar to the TIA version but differs in some electrical requirements and load conditions. Both standards feature similar driver output levels, receiver thresholds and data rates. The TIA version is the more generic of the two standards and is intended for multiple applications. The electrical-only ANSI/TIA/EIA-644 standard is shown in Table 2.1, and it is intended to be referenced by other standards that specify the complete interface (connectors, protocol, etc.).

2.3 INTRODUCTION TO LVDS

Following is the detail discussion of low-voltage differential signaling (LVDS) applications and basic circuits.



2.3.1 Basic Concepts

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350 mV) differentially over two PCB traces or balanced cables. The simplified diagram of LVDS driver and receiver connected via 100 Ω differential impedance media is shown in Fig. 2.1. The driver consists of a current source which drives the differential pair lines. The basic receiver has high DC input impedance, so the majority of driver current flow across the 100 Ω termination resistor generating about 350 mV across the receiver inputs. When four MOS switches (the M1 - M4 in Fig. 2.1) of the driver switch, the direction of current across the resistor is changed, thereby creating a valid “one” or “zero” logic state. The signaling levels of LVDS are shown in Fig. 2.2.

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two

wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receiver which detects only the voltage difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. The current-mode driver is not prone to ringing and switching spikes, further reducing noise. Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low almost flat power consumption across frequency is obtained. Switching spikes in the driver are very small, so that total current consumption does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5 mA × 350 mV = 1.225 mW) is very small in magnitude.

2.3.2 Easy Termination

Whether the LVDS transmission medium consists of cables or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed signals. If the medium is not properly terminated, signals reflect from the end of the cables or traces and may interfere with succeeding signals. Proper termination also reduces unwanted electro-magnetic emissions and provides the optimum signal quality. To prevent reflections, LVDS requires a terminating resistor that is matched to the actual cables or PCB traces differential impedance.

Commonly a 100 Ω termination is employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input. The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL (Positive Emitter Coupled Logic) require more complex termination than the one-resistor solution for LVDS [6]. PECL drivers commonly require 220 Ω pull down resistors from each driver output, along with 100 Ω resistor across the receiver input.

2.3.3 LVDS Configurations

LVDS drivers and receivers are commonly used in a point-to-point configuration as shown in Fig. 2.3. However, other topologies/configurations are also possible. The configuration, as shown in Fig. 2.4, allows bi-directional communication over a single twisted pair cable. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (< 10 m). In Fig. 2.5, a multi-drop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than 12 mm application dependent). Dedicated point-to-point links provide the best signal quality due to the clear path they provide. LVDS has many advantages that make it likely to become the next famous data transmission standard rates from hundreds to thousands of megabits per second and short haul distances in the tens of meters. In this role, LVDS far exceeds the 20 Kb/s to 30 Mb/s rates of the common RS-232, RS-422, and RS-485 standards.

2.3.4 Cables and Connectors

LVDS was intended to be used on a wide variety of media [7]. The exact medium is not specified in the LVDS standard, as it is intended to be specified in the referencing standard that specifies the complete interface [8]. This includes the media, data rate, length, connectors, function, and pin assignments. In some applications that are very short (< 0.3 m), ribbon cables or flex circuits may be acceptable. In the box-to-box application, twisted pair or twin-ax cables would be a better option due to robustness, shielding and balance. When choosing cables and connectors for LVDS, following tips are important:

- Use controlled impedance media. The cables and connectors should have a differential impedance of about 100 Ω. They should not introduce major impedance discontinuities that cause signal reflections.
- Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electro-magnetic radiation as common-mode (not differential-mode) noise, which is rejected by the receiver.
- For cable distances less than 0.5 m, most cables can be made to work effectively. For cable distances less than 10 m, CAT 3 (Category 3) twisted pair cable works well and is readily available and relatively inexpensive. Other types of cables may also be used as required by a specific application. This includes twin-ax cables built from separate pairs and ribbon style constructions, which are then coiled.

As the tips that are mentioned above, try to use differential cables such as twisted pair cables, twin-ax cables, or flex circuits with closely coupled differential traces when designing a LVDS compatible I/O interface. Twisted pair cables, which provide

a good, low cost solution with good balance as shown in Fig. 2.6, are flexible, and capable of medium to long runs depending upon the application skew budget. It is offered with an overall shield or with shields around each pair as well as an overall shield. Twisted pair cables such as Category 3 (CAT3) cable is good for runs up to about 10 m, while CAT5 has been used for longer runs. Twin-ax cables, as shown in Fig. 2.7, are flexible, have low skew and shields around each pair for isolation. Since they are not twisted, they tend to have very low skew within a pair and between pairs. These cables are for long runs and have been commonly deployed in Channel Link and FPD-Link applications. Flex circuits, as shown in Fig. 2.8, is a good choice for very short runs, but it is difficult to be shielded. It can be used as interconnects between boards within systems. The members of differential pairs should be closely coupled (S < W) and use ground shield traces between the different differential pairs.

Connectors are also application dependent and depend upon the cable system being used, the number of pins, the need for shielding and other mechanical footprint concerns. Standard connectors have been used at low to medium data rates, and optimized low skew connectors have been developed for medium to high-speed applications.

2.3.5 Signal Quality

Signal quality may be measured by a variety of means [9]. Eye Patterns is commonly used to determine signal quality. The eye pattern is used to measure the effects of inter-symbol interference (ISI) on random data being transmitted through a particular medium. The prior data bits effect the transition time of the signal. This is especially true for none return to zero (NRZ) data that does not guarantee transitions on the line. For example, in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (101010) waveform. This is due

to the low pass filter effects of the cable. Fig. 2.9 illustrates the superposition of six different data patterns. Overlaid, they form the eye pattern that is the input to the cable. The right hand side of Fig. 2.9 illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider and the opening of the eye is also now smaller.

Fig. 2.10 describes the measurement locations for minimum jitter. Peak-to-peak jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0 V (differential). However, the receiver is specified to switch between + 100 mV and – 100 mV. Therefore for a worse case jitter measurement, a box should be drawn between ± 100 mV and the jitter is measured between the first and last crossing at ± 100 mV. If the vertical axis units in Fig. 2.10 were 100mV/division, the worse case jitter is at ± 100 mV levels.

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5 %, 10 %, or 20 % is acceptable with 20 % jitter usually being an upper practical limit. More than 20 % jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult.

2.3.6 Input Common Mode Range of LVDS Receiver

An LVDS receiver can tolerate a maximum of ± 1 V ground shift between the driver's ground and the receiver's ground. Note that LVDS has a typical output offset voltage of + 1.2 V, and the summation of ground shifting, output offset voltage and any longitudinally coupled noise is the common mode voltage seen on the receiver input pins with respect to the receiver ground. The common mode range of the

receiver is + 0.2 V to + 2.2 V, and the recommended receiver input voltage range is from ground to + 2.4 V. For example, if a driver has a V_{OH} of 1.4 V and a V_{OL} of 1.0 V (with respect to the driver ground), and a + 1 V ground shift is present (driver ground + 1 V higher than receiver ground), this will become + 2.4 V (1.4 + 1.0) as V_{IH} and + 2.0 V (1.0 + 1.0) as V_{IL} on the receiver inputs referenced to the receiver ground. On the contrary, with a − 1 V ground shift and the same driver levels results as 0.4 V (1.4 − 1.0) V_{IH} and 0.0 V (1.0 − 1.0) V_{IL} on the receiver inputs. This is shown in Fig. 2.11.

2.3.7 Advantages and Applications

LVDS has many advantages as following:

- The LVDS solutions are inexpensive CMOS implementations as compared to custom solutions on elaborate processes.
- High performance can be achieved by using low cost, off-the-shelf CAT3 cables and connectors, or FR4 materials.
- LVDS consumes very little power, so power supplies, fans, etc., can be reduced or eliminated.
- LVDS is a low noise producing, noise tolerant technology – power supply and EMI noise are greatly minimized.
- LVDS transceivers are relatively inexpensive and can also be integrated around digital cores providing a higher level of integration.
- LVDS can move data so much faster than TTL (Transistor-Transistor Logic), so multiple TTL signals can be serialized into a single LVDS channel, reducing board, connector, and cable costs. Fig. 2.12 shows the LVDS channel link serializers and deserializers.

The high-speed and low-power/noise/cost benefits of LVDS broaden the scope

of LVDS applications far beyond those for traditional technologies. The applications of LVDS in several aspects are summarized in Table 2.2.

2.3.8 Conclusion

LVDS technology solves the ever increasing data rate problem while decreasing power dissipation and can be widely used in telecom, routers, intelligent hubs, LCD displays, copiers and numerous other exciting applications. LVDS technology eliminates the trade-offs in speed, power, noise, and cost for high performance data transmission applications. This high speed interface allows designers to implement a simple point-to-point link without complex termination issues. Low power dissipation and the use of a core process allows for the integration of PLLs and digital blocks to provide optimized interface single chip solutions. LVDS technology provides solutions when gigabits at milliwatts are required. Merits and drawbacks of different I/O interface technologies are summarized in Table 2.3.

2.4 INTRODUCTION TO RSDS

Following is the detail discussion of reduced-swing differential signaling (RSDS) applications and basic circuits [10].

2.4.1 Scope

Reduced Swing Differential Signaling (RSDS) is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between flat panel timing controllers and flat panel column drivers. RSDS technology is originated from the LVDS technology. The RSDS interfaces tend to be used in flat panel display applications with

resolutions between VGA (600 × 480 pixels) and UXGA (1600 × 1200 pixels). The RSDS technology provides many benefits to flat panel display applications which include following items:

- Reduced bus width – enables smaller and thinner flat panel column driver boards.
- Low power dissipation – extends system run time.
- Low EMI generation – eliminates EMI suppression components and shielding.
- High noise rejection – maintains signal image.
- High throughput – enables high resolution flat panel displays.

RSDS is a differential interface with a nominal signal swing of 200 mV. It retains the many benefits of the LVDS interface which is commonly used between the host and the panel for a high bandwidth, robust digital interface. The RSDS applications are within a sub-system, the signal swing is reduced further from LVDS to lower power even further.

2.4.2 Electrical Specifications and Bus Configurations

An RSDS interface circuit is shown in Fig. 2.13. The interface contains three parts: a transmitter, receivers and a balanced interconnecting medium with a termination. The transmitter and receiver are defined in terms of direct electrical measurements in Table 2.4.

The RSDS is a versatile interface that may be configured differently depending upon the end application requirements. Considerations include the location of the timing controller (TCON), the resolution and the color depth of the flat panel displays. The common implementations include the following bus types:

- Type 1 – Multi-drop bus with double terminations.

- Type 2 – Multi-drop bus with single end termination.
- Type 3 – Double multi-drop bus with single termination.

In a type 1 configuration, the source (TCON) is located in the middle of the bus via a short stub as shown in Fig. 2.14. The bus is terminated at both ends with a nominal termination of 100 Ω. The interconnecting medium is a balanced coupled pair with nominal differential impedance of 100 Ω. The number of RSDS data pairs is 9 or 12 depending upon the color depth supported. In this configuration, the RSDS driver which is at the output part of the TCON will see a DC load of 50 Ω instead of 100 Ω. For this case, output drives of the RSDS driver must be adjusted to comply to the V_{OD} specification with the 50 Ω load presented by the type 1 configuration.

In a type 2 configuration, as shown in Fig. 2.15, the source (TCON) is located at one end of the bus. The bus is terminated at the far end with a nominal termination of 100 Ω. The interconnecting medium is a balanced coupled pair with nominal differential impedance of 100 Ω. The bus may be a single or dual bus depending upon the resolution of flat panel displays. The number of RSDS data pairs is 9 or 12 depending upon the color depth supported for a single bus. Or the number of RSDS data pairs is 18 or 24 depending upon the color depth supported for a dual bus.

In a Type 3 configuration, the source (TCON) is located in the center of the application. There are two buses out of the TCON that run to the right and left respectively. Each bus is terminated at the far end with a nominal termination of 100 Ω. The interconnecting medium is a balanced coupled pair with nominal differential impedance of 100 Ω. The number of RSDS data pairs is 9 or 12 depending upon the color depth supported for a single bus for each bus. The connection of the TCON to the main line is not a stub in this configuration, but rather is part of the main line. This helps to improve signal quality as shown in Fig. 2.16.

From Fig. 2.14 to Fig. 2.16, the complete bus is not illustrated, only a single

RSDS pair is shown. The number of column drivers on the bus is also application specific and depends upon the resolution of flat panel displays

2.4.3 Applications

RSDS like its predecessor LVDS, originated from the unique need of the LCD manufacturers for on glass interface with higher speeds, reduced interconnects, lower power, and lower EMI. As shown in Fig. 2.17, the RSDS drivers are embedded at the output of the flat panel timing controller and the RSDS input buffers are at the input of the flat panel column drivers. Since this new technology also uses a low voltage differential swing (+/- 200 mV), lower EMI and lower power consumption can also be realized. Also due to its low voltage swing (versus TTL), faster clock rates can be achieved and thereby enabling higher resolution of FPDs in the future. At present clock rates of 65 MHz have been EMI qualified in pre-production TFT LCD modules with relative ease when compared to their TTL counter parts. In the near future, higher clock rates in excess of 85 MHz or even 100 MHz plus can be expected. Since this interface is a serial interface, overall bus width is also reduced by half of the conventional TTL bus architecture. In a TTL 6 bit/color dual bus architecture, a total of 36 data lines plus 2 clock signals are required, for a total of 38 conductors. In an equivalent RSDS architecture, only one bus consisting of a total of 9 differential pairs of data lines plus a differential clock pair are required, for a total of 20 conductors. When implementing the same system with RSDS, an overall reduction of 47 % in bus conductors are achieved thereby enabling a small outline PCBs.

2.5 COMPARISON BETWEEN LVDS AND RSDS

The low-voltage differential signaling (LVDS) technology and the

reduced-swing differential signaling (RSDS) technology have been developed to provide the high-speed and low-power interface applications, which are used to replace other I/O interfaces, such as the PECL [11]. The LVDS technology is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between graphics cards and LCD timing controllers. However, the RSDS technology is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between LCD timing controllers and flat panel column drivers. The applications of LVDS and RSDS in the FPD systems are shown in Fig. 2.18. Both LVDS and RSDS use differential transmission and low-voltage signal swing to achieve the advantages of reduced power consumption and radiated less EMI. The difference between LVDS and RSDS is their intended applications and transmission data rates. The LVDS technology utilizes a 7:1 serialization scheme in a FPD system which is to transmit video signals at higher data rates. The RSDS technology instead uses a 2:1 serialization scheme which results in a less complex and low-power receiver architecture. The data rate in RSDS interface is lower because the RSDS receiver is utilized to drive flat panel column drivers which contribute huge capacitive loading. There are 8 or 10 column drivers in a liquid crystal panel and the input capacitive loading of each column driver is typically 2 to 5 pF.

Table 2.1

The electrical-only ANSI/TIA/EIA-644 (LVDS) standard of LVDS.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Output Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change to V_{OD}|		50	|mV|
ΔV_{OS}	|Change to V_{OS}|		50	|mV|
$I_{SA,} I_{SB}$	Short Circuit Current		24	|mA|
t_r / t_f	Output Rise/Fall Times (≥ 200 Mb/s)	0.26	1.5	ns
	Output Rise/Fall Times (≤ 199 Mb/s)	0.26	30 % of t_{ui}	ns
I_{IN}	Input Current		20	|μA|
V_{TH}	|Threshold Voltage|		± 100	mV
V_{IN}	Input Voltage Range	0	2.4	V

t_{ui} is unit interval (i.e. bit width).

Table 2.2

The scope of LVDS applications.

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	Box-to-box/rack-to-rack	
Multimedia peripheral links		

Table 2.3

Merits and drawbacks of different I/O interface technologies.

Advantages	LVDS	PECL	Optics	RS-422	GTL	TTL
Data rate up to 1 Gb/s	+	+	+	–	–	–
Very low skew	+	+	+	–	+	–
Low dynamic power	+	–	+	–	–	–
Cost effective	+	–	–	+	+	+
Low noise/EMI	+	+	+	–	–	–
Single power supply/reference	+	–	+	+	–	+
Migration path to low voltage	+	–	+	–	+	+
Simple termination	+	–	–	+	–	+
Wide common-mode range	–	+	+	+	–	–
Process independent	+	–	+	+	+	+
Allows integration with digital circuits	+	–	–	–	+	+
Cable breakage/splicing issues	+	+	–	+	+	+
Long distance transmission	–	+	+	+	–	–
Industrial temp/voltage range	+	+	+	+	+	+

Table 2.4

Electrical specifications of RSDS transmitter and receiver.

TX/RX	Parameter	Definition	Conditions	MIN	TYP	MAX	Units
TX	V_{OD}	Differential Output Voltage	R_L = 100 Ω	100	200	400	|mV|
TX	V_{OS}	Offset Voltage	V_{OD} = 0.2 V	1.1	1.3	1.5	V
TX	t_r / t_f	Transition Time			2		ns
RX	V_{TH}	Differential Threshold				± 100	mV
RX	V_{IN}	Input Range	V_{ID} = 0.2 V	0.1		1.4	V
–	R_T	Termination		95	100	105	Ω
–	Z_O	Differential impedance of interconnect		90	100	110	Ω

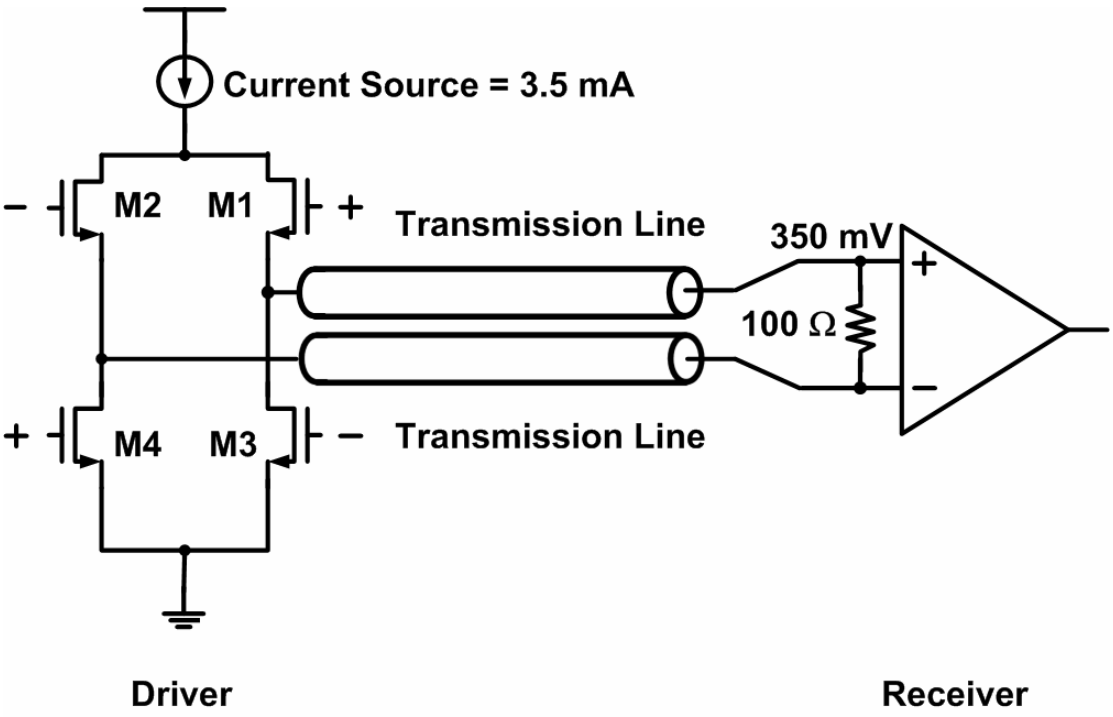


Fig. 2.1 The simplified diagram of LVDS driver and receiver connected via 100 Ω differential impedance media.

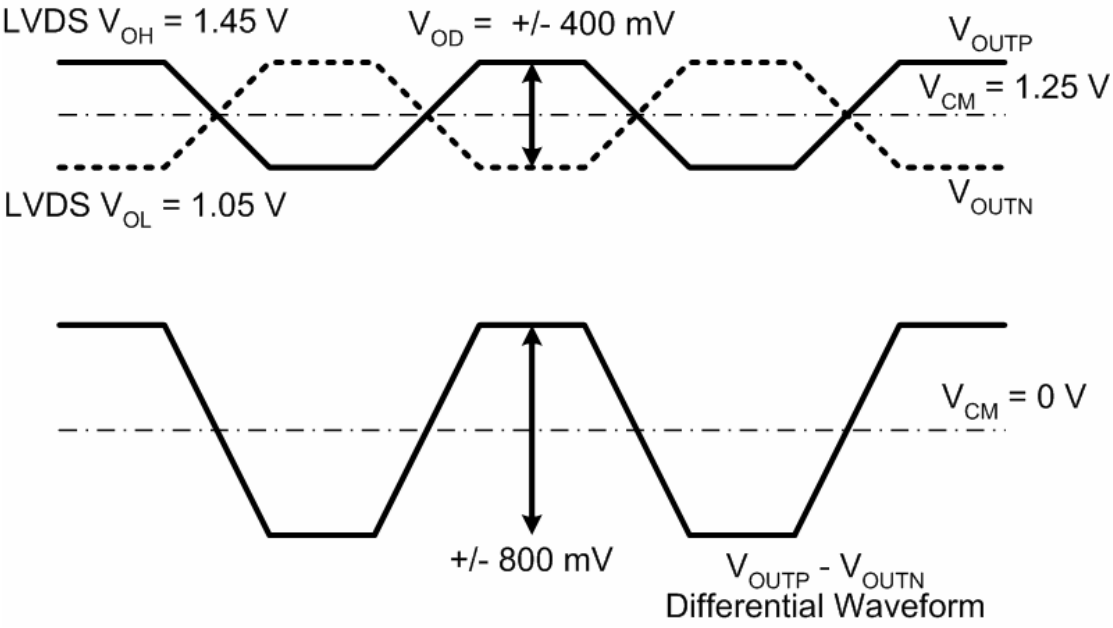


Fig. 2.2 The signaling levels of LVDS.

Fig. 2.3 Point-to-point configuration of LVDS.

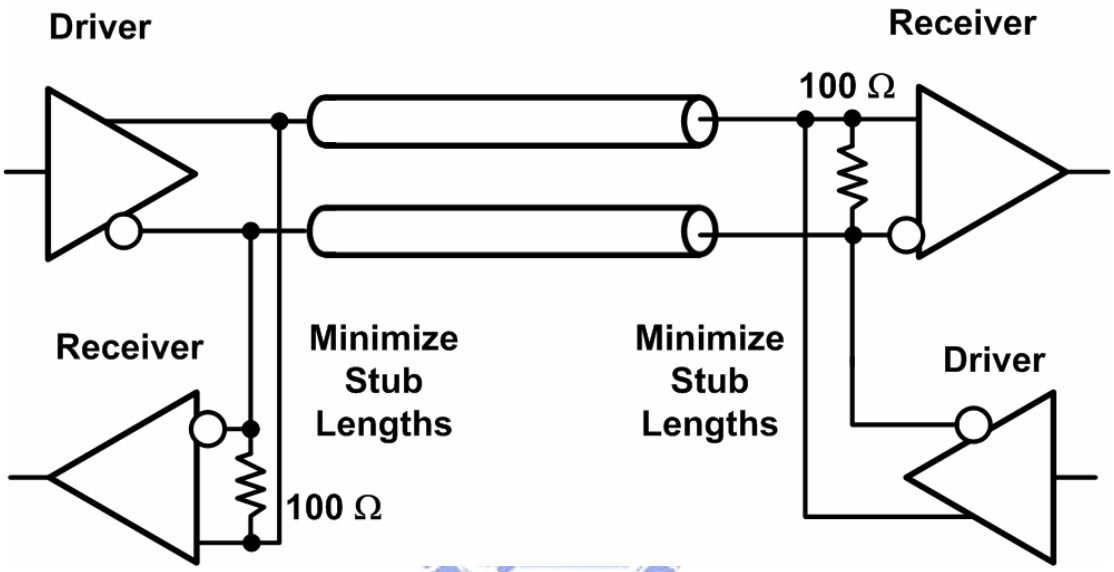


Fig. 2.4 Bi-directional configuration of LVDS.

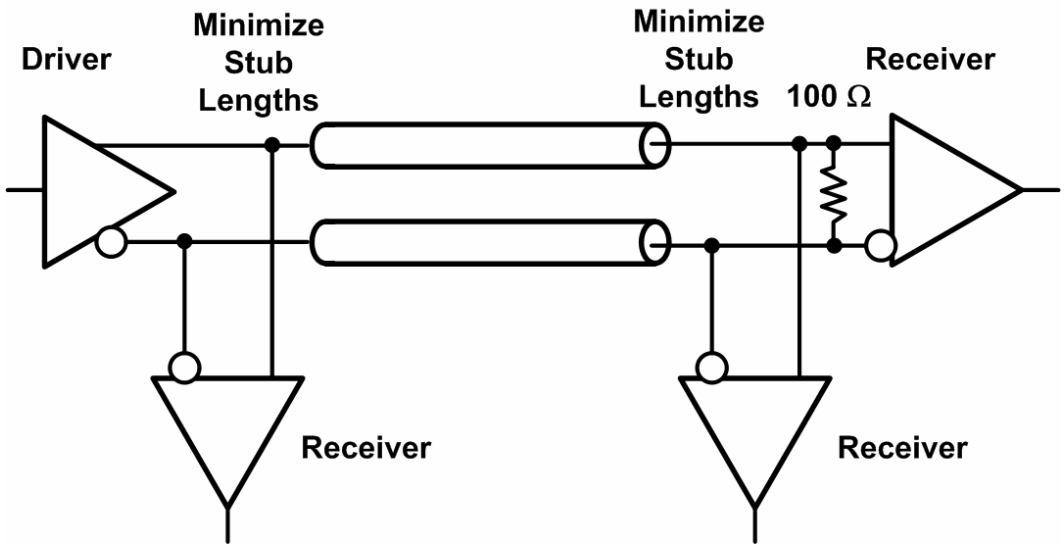


Fig. 2.5 Multi-drop configuration of LVDS.

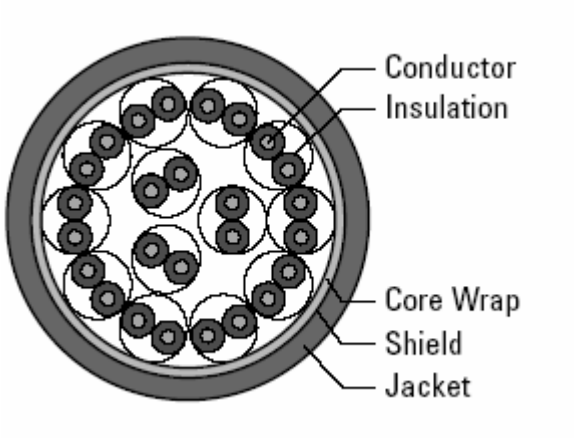


Fig. 2.6 Cross section drawing of a twisted pair cable.

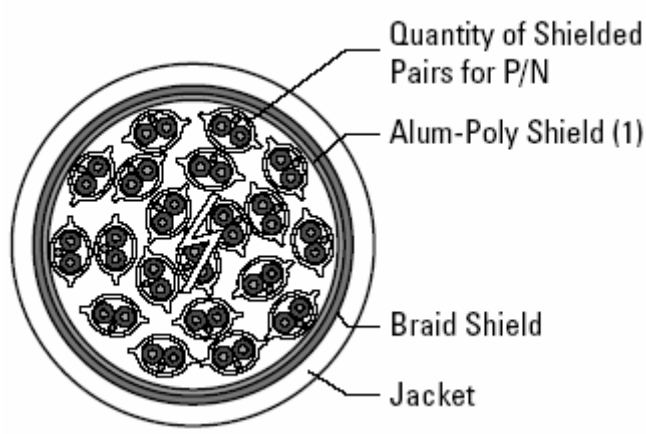


Fig. 2.7 Cross section drawing of a twin-ax cable.

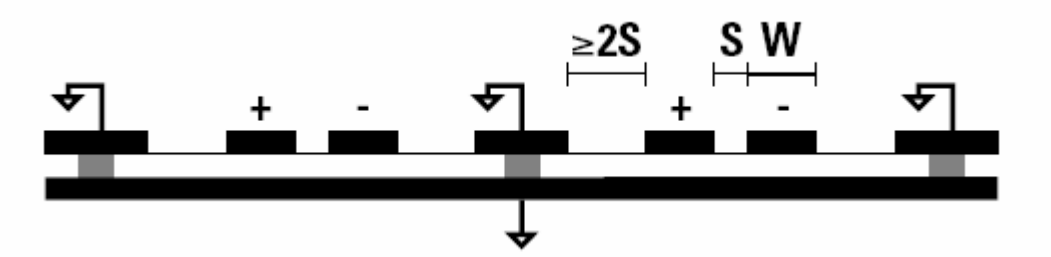


Fig. 2.8 Cross section drawing of a flex circuit.

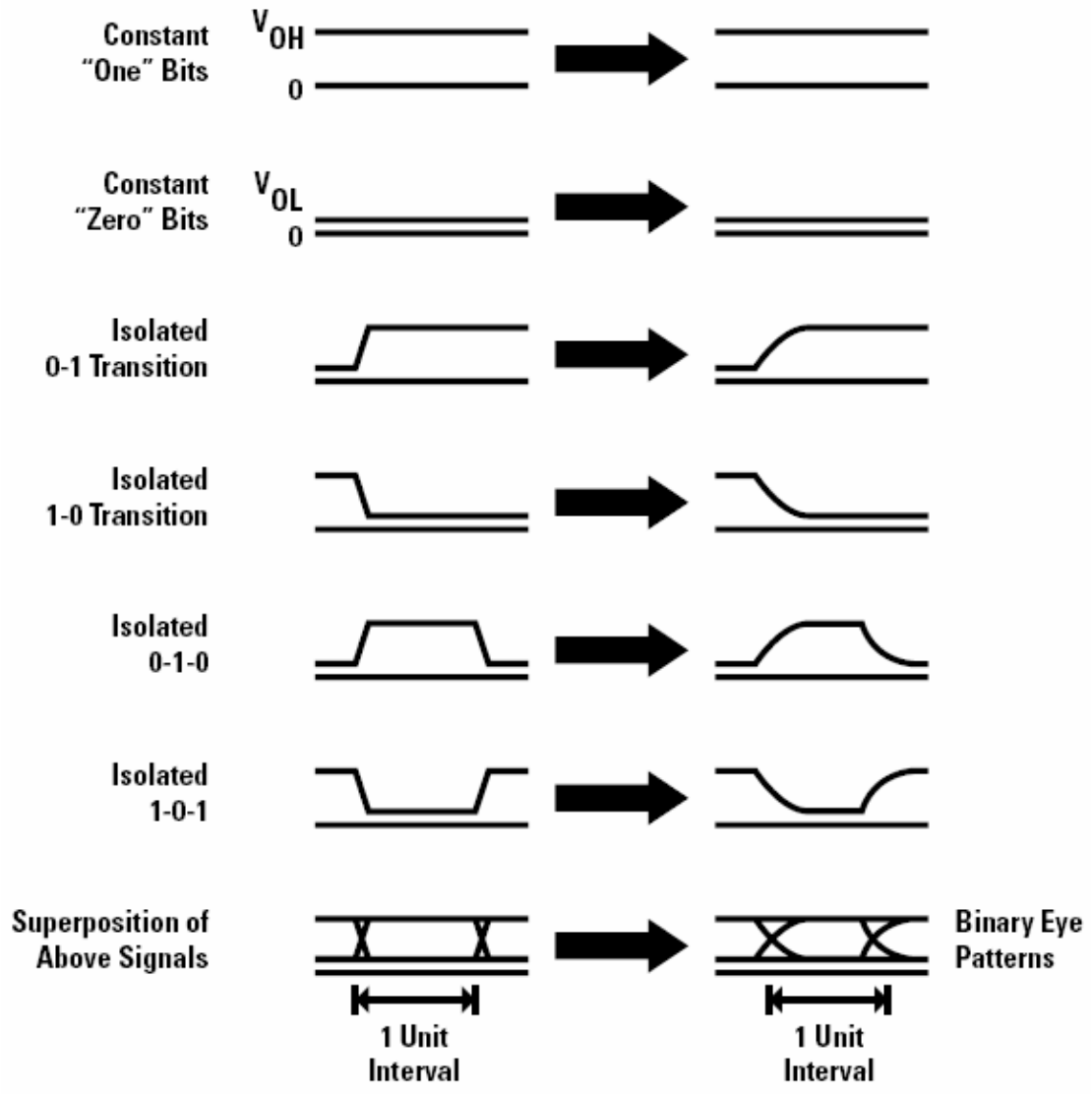


Fig. 2.9 Formation of an eye pattern by superposition. The left hand side is the eye pattern at the input of the cable and the right hand side is the eye pattern at the end of the cable.

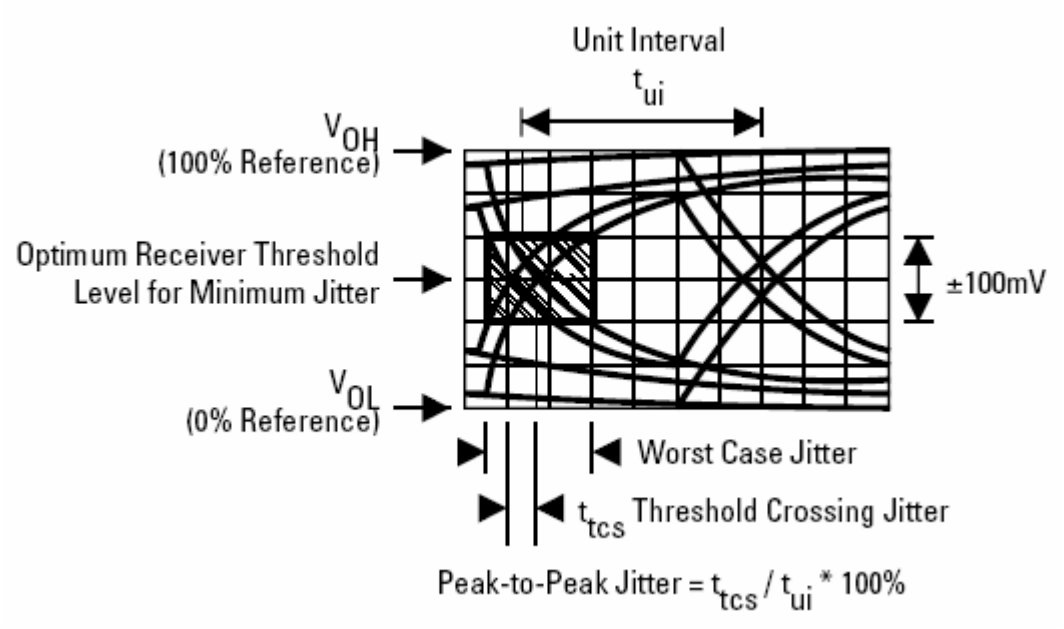


Fig. 2.10 Jitter measurements in an eye pattern of NRZ data.

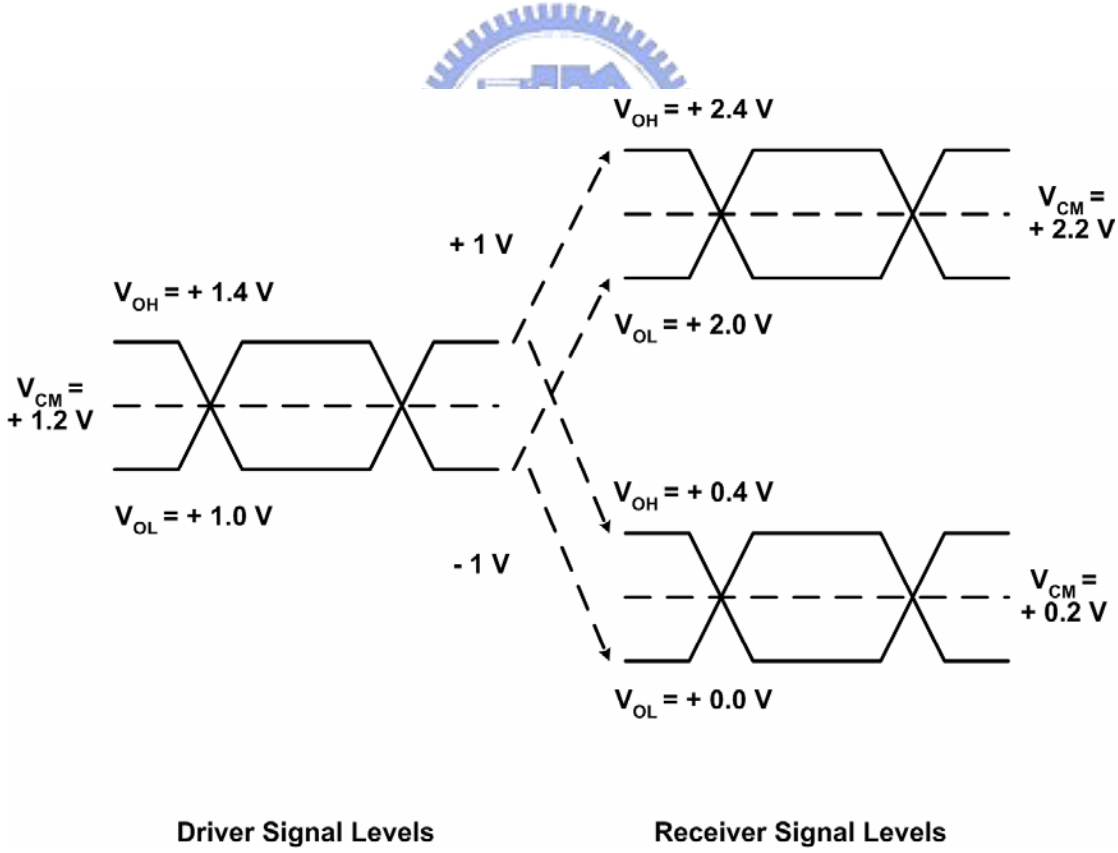


Fig. 2.11 The common mode voltage range of the LVDS receiver.

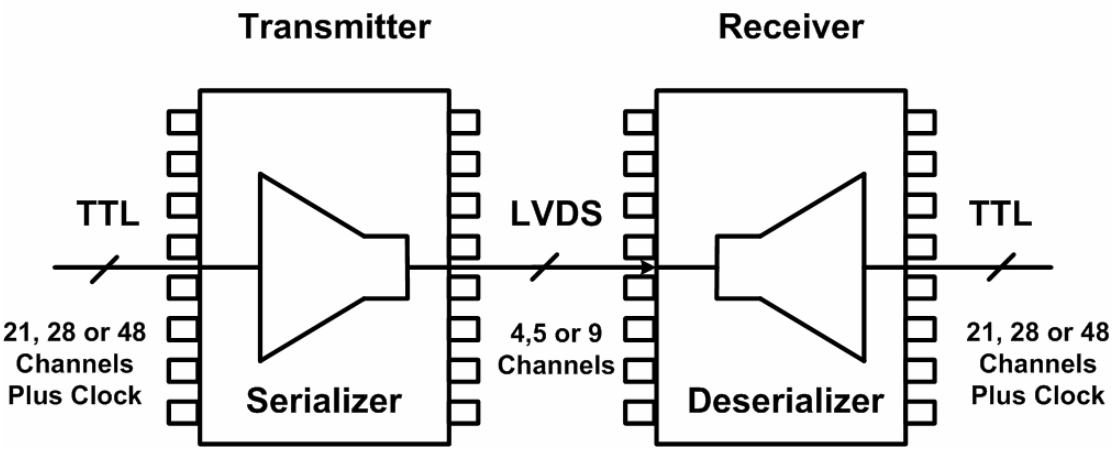


Fig. 2.12 The LVDS channel links which convert a TTL bus into a compact LVDS data stream and back to a TTL bus.

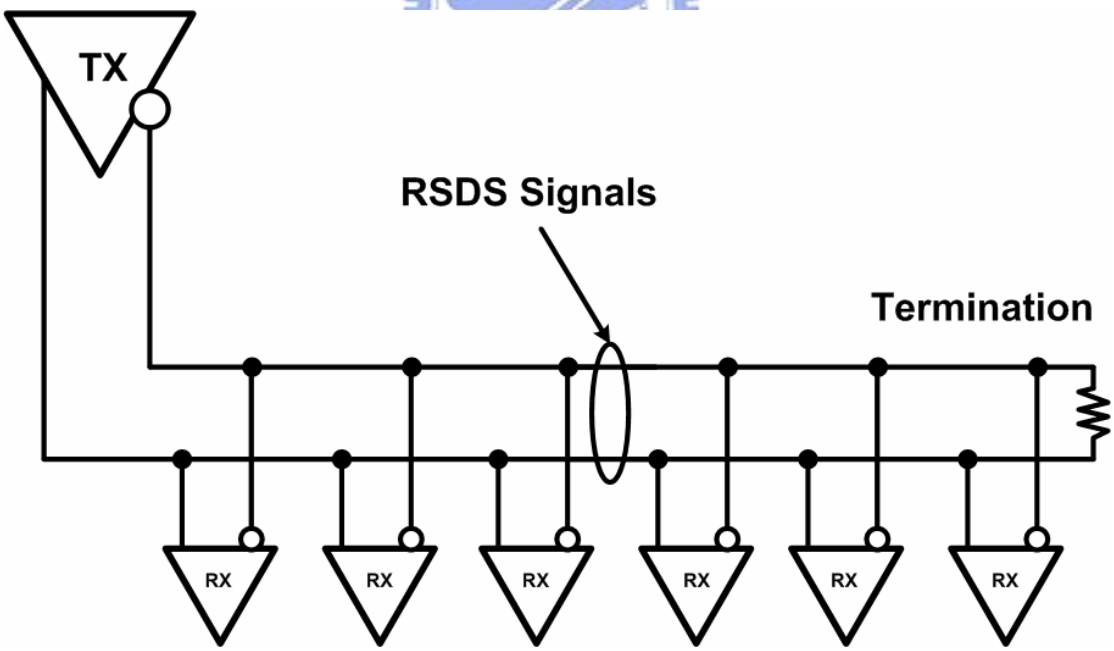


Fig. 2.13 The RSDS interface configuration. The interface contains three parts: a transmitter, receivers and a balanced interconnecting medium with a termination.

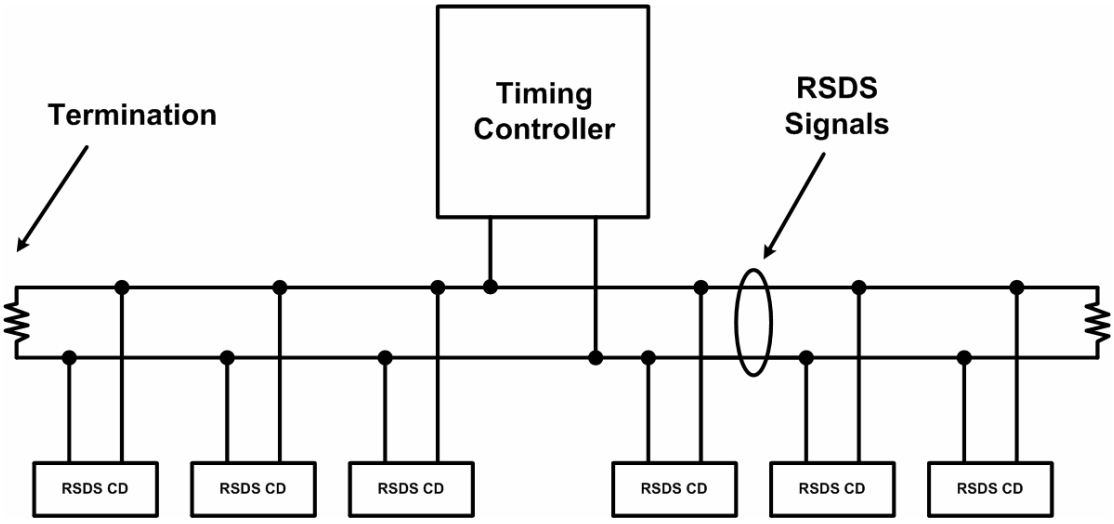


Fig. 2.14 Type 1 bus configuration of RSDS.

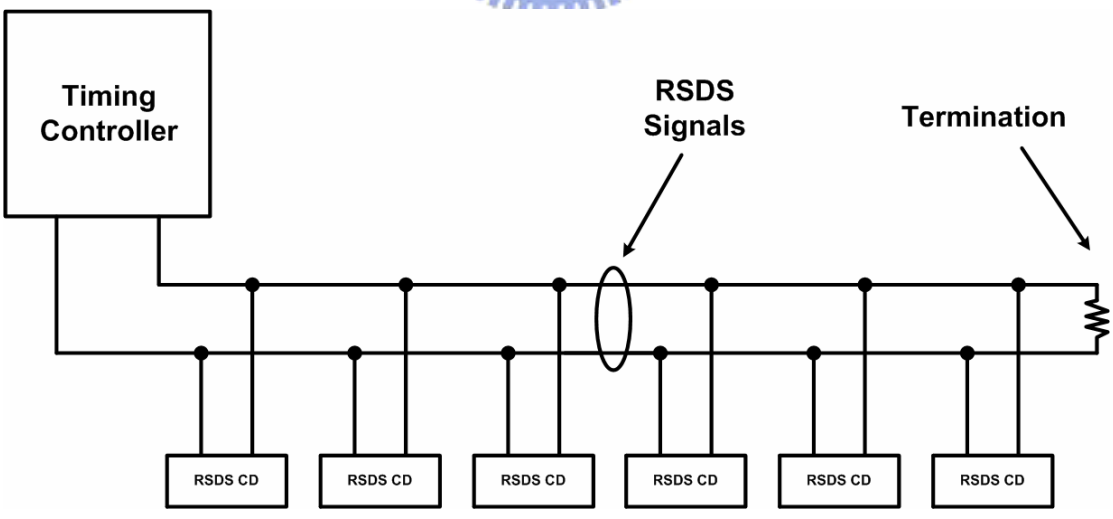


Fig. 2.15 Type 2 bus configuration of RSDS.

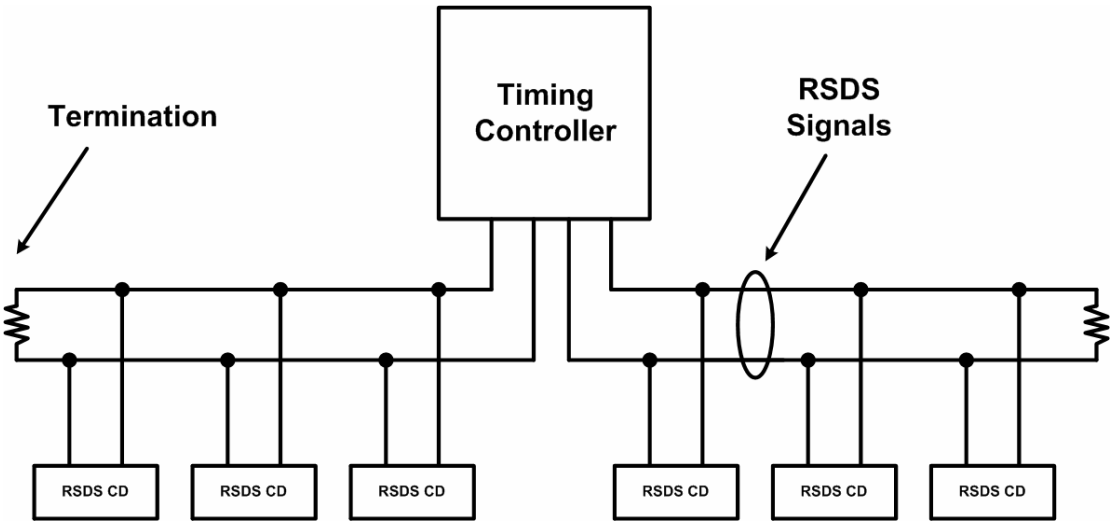


Fig. 2.16 Type 3 bus configuration of RSDS.

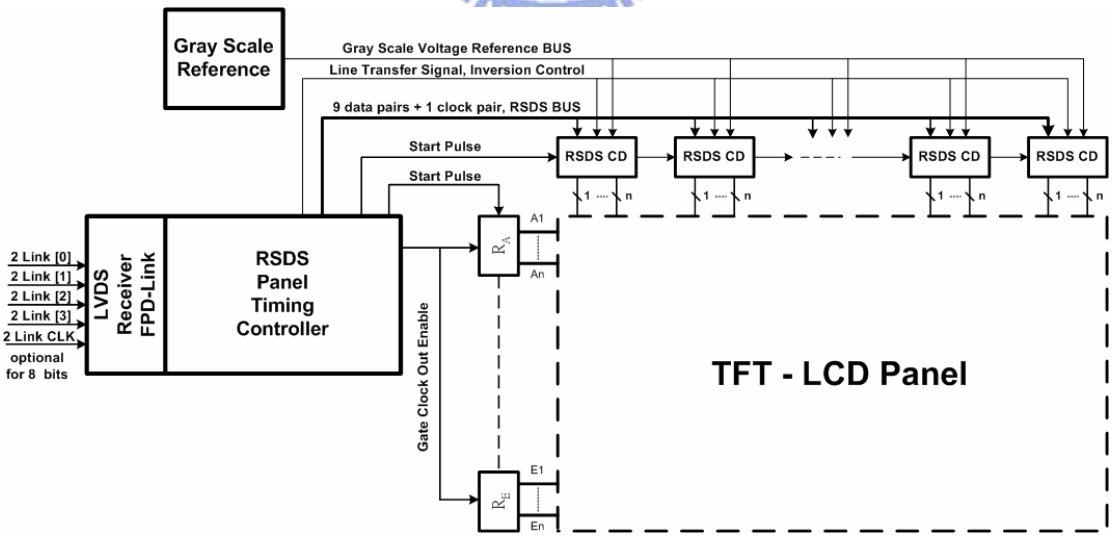


Fig. 2.17 The RSDS interface utilized in the flat panel display systems.

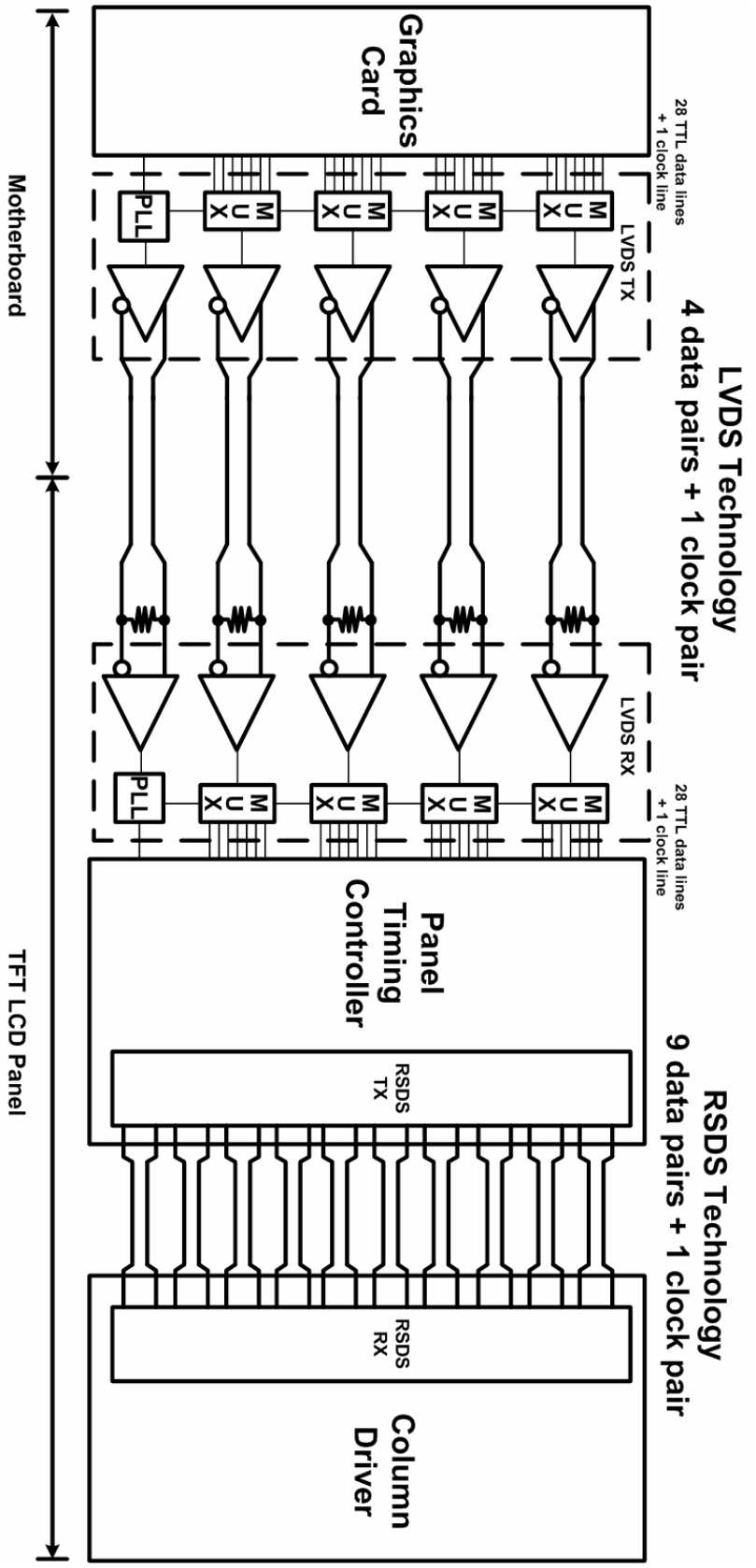


Fig. 2.18 Comparison between LVDS and RSDS technologies which are utilized in the interfaces of flat panel display systems.

Chapter 3

Phase-Locked Loop

3.1 INTRODUCTION

The phase-locked loop (PLL) concept was first developed in the 1930s. It has been used in communication systems of many types, particularly in satellite communication systems. Until recently, however, phase-locked systems have been too complex and costly for use in most consumer and industrial systems, where performance requirements are more modest and other approaches are more economical. The PLL is particularly amenable to monolithic construction, however, and integrated-circuit phase-locked loops can now be fabricated at very low cost. Their use has become attractive for many applications such as FM demodulators, stereo demodulators, tone detectors, frequency synthesizers and others.

PLLs are now often used in the I/O interfaces of digital integrated circuits in order to hide clock distribution delays and to improve overall system timing. In these applications, PLLs must closely track the input clock. However, the rising demand for high-speed I/O interfaces has created an increasingly noisy environment in which PLLs must function. This noise, typically in the form of supply and substrate noise, tends to cause the output clock of PLLs to jitter from their ideal timing. With a shrinking tolerance for jitter in the decreasing period of the output clock, the design of low jitter PLLs has become very challenging.

This chapter will introduce a PLL with 25 MHz reference clock frequency which can form ten uniform distributed phases of 200 MHz as clock signals for circuits, such

as multiplexers, to use. The measured output clock signals and jitter will be presented in the last section of this chapter.

3.2 BASIC PLL ARCHITECTURE

A PLL is basically an oscillator whose phase and frequency is locked to those of the input signal [12]. This is done by using a negative feedback control loop, as shown in Fig. 3.1. A PLL consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a frequency divider (divided by N). The negative feedback system synchronizes the internal signal (Fback) which is from the frequency divider to the external reference signal (Fref) by comparing their phases. The PFD develops two output control signals, Up and Downb, which are proportional to the phase errors. The purpose of the charge pump is to convert the logic states of PFD into analog signals suitable for controlling VCO which varies the frequency of the output signals (clock [0:6]) by charging or discharging the loop filter. In the loop filter, extra poles and zeros should be introduced to filter out high frequency signals from the PFD and the charge pump. In such system, the PLL is "locked" when the phase difference between Fref and Fback is constant. Therefore, the phase of Fref and Fback are aligned and the frequency of the output signals (clock [0:6]) is N-times of the input reference signal (Fref).

3.3 PLL CIRCUIT IMPLEMENTATION

Fig. 3.2 shows the architecture of the designed PLL [13]. The PLL has five delay stages and a second-order loop filter. The designed output clock frequency is 200 MHz with ten different phases. The divider divides the frequency of the output clock

by eight and then the phase detector compares the divided output clock (Fback) with the 25 MHz input reference clock (Frefin). The charge pump circuit charges or discharges the capacitance of the loop filter depended on the output logic of the phase detector. The bias generator circuit generates two property bias voltages, Vbp and Vbn, which are depended on the output voltage (Vctrl) of the loop filter for the voltage-controlled oscillator to correct the oscillating frequency. The differential-to-single-ended conversion circuit guarantees a 50 % duty-cycle for the output clock signals, Clock [0:9], which are more suitable for digital circuits to utilize. Following is the detail descriptions of each circuit block in the designed PLL.

3.3.1 Phase Frequency Detector

Fig. 3.3 shows the circuit implementation of the PFD which uses the standard NAND gate architecture. The PFD generates two output signals, UP and DOWN, for the charge pump which is the following circuit. Equal and short duration pulses at the UP and DOWN outputs of the PFD are needed for in-phase inputs in order to eliminate a dead zone region in the PFD as seen by the charge pump. Ideally, the PFD should have the ability to distinguish any phase error between reference and feedback signals. In practical, when the phase error is too small, the reset signal is so fast that the following charge pump circuit will not be activated. This will result in dead zone region (undetectable phase difference range). The dead zone is highly undesirable because it allows the VCO to accumulate as much random phase error as the phase difference with respect to the input while receiving no corrective feedback. The dead zone region could be eliminated by adding extra delay buffers in the reset path to ensure that when both reference and feedback signals are at the same phase, there would be equal and activated pulses at the output. The elimination of the dead zone region results in overall linear operating characteristics for the PFD, especially for

input signals with small but finite phase difference. However, inserting the delay buffers will limit the maximum operation frequency that is in inverse proportion to the total reset path delay.

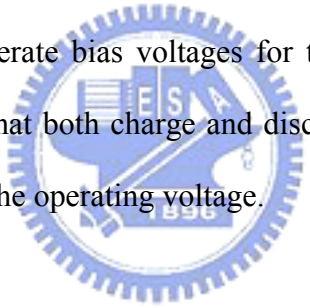
As the reason mentioned above, a delay path which contains six inverters is added into the reset path in the designed PLL as shown in Fig. 3.3. Because of this added delay, a signal transition at the Frefin or Fback input will cause the corresponding UP or DOWN output to be set to ground for some short delay before both outputs are reset for the case when the other output was already set to ground. Due to the designed PLL architecture, the PFD compares the phase difference of both Frefin and Fback inputs at the negative edge. The transmission gate (M1 and M2) and the inverter (INV1) are utilized to invert the DOWN signal in order to control the charge pump. The two extra inverters (INV2 and INV3) at the UP signal are employed to make the balance delay time between UPP and DOWNB outputs. Fig. 3.4 shows the simulation of the PFD that the reference signal is earlier than the feedback signal and Fig. 3.5 shows the simulation of the PFD that the reference signal and the feedback signal are in-phase.

3.3.2 Charge Pump

The schematic of the charge pump circuit is shown in Fig. 3.6. It can charge or discharge the loop filter to vary VCO center frequency according to UPP and DOWNB from the PFD. A conventional charge pump circuit has problems such as the charge sharing in high impedance state, the charge injection, and the clock feed through. The charge injection phenomenon is produced by the overlap capacitance of the switch devices and the capacitance at the intermediate node between the current source and switch devices. This charge injection phenomenon will result in a phase offset at the input of the PFD when the PLL is locked. To eliminate the charge

injection problem, the two switch devices (M1 and M2) are separated from the output voltage (Vctrl). Therefore, the output voltage is now isolated from the switching noise resulting from the overlap capacitance of the two switch devices. In addition, the intermediate node between the current source and switch devices will charge to the output voltage only by the gate overdrive of the current source devices (M3 and M4), |Vgs – Vt|, an amount which is independent of the output voltage. Moreover, since both the NMOS and PMOS current source devices always turn on in each cycle, any charge injection will cancel out to first order with equal current source device size.

The architecture of the charge pump circuit ensures high speed since all internal nodes are low impedance. Some MOS capacitances are employed to suppress noise on the DC bias voltages. The other characteristic of the charge pump is using replica current mirror circuits to generate bias voltages for the two current source devices (M3 and M4). It can ensure that both charge and discharge currents are the same as the reference current (Iref) at the operating voltage.



3.3.3 Loop Filter

A second-order on chip loop filter is designed to suppress the reference spurs [14]. The loop filter is a low pass filter that is utilized to extract the average value from the PFD outputs. As shown in Fig. 3.7, it is composed of a resistor R_1 in series with a capacitor C_1 and a capacitor C_2 in parallel. The loop filter provides a pole in the original to provide an infinite DC gain to get the zero static phase error, and a zero in the open loop response in order to improve the phase margin to ensure overall stability of the loop. Capacitance C_2 is used to provide higher-order roll off for reducing the ripple noise to mitigate frequency jump. However the adding of the capacitance C_2 will make the overall PLL system become third-order one and affect the stability of the loop. In general, by setting $C_1 > 20 \times C_2$, the third-order loop can

be approximated to second-order loop. The total transfer function of the loop filter can be expressed as

$$F(s)=\frac{1}{C_1+C_2}\frac{sR_1C_1+1}{s\left[(sR_1C_1C_2/C_1+C_2)+1\right]} \tag{3-1}$$

and hence

$$F(s)=\frac{K\times(s+\omega_z)}{s\times(1+s/\omega_p)} \tag{3-2}$$

where

$$\omega_z=1/R_1C_1,\ \ \omega_P=\omega_z\times(1+C_1/C_2),\ \ K=\frac{R_1\times C_1}{C_1+C_2}$$

The resistor in the loop filter is the N-well resistor, and the capacitors are made up of accumulation-mode MOS capacitors. Compared to their inversion or depletion mode counterparts, accumulation-mode capacitors manifest better frequency response and quality factors at high frequency operation. Due to achieve adequate phase margin of the PLL, the values of the resistor and both capacitors are usually very large. Using MOS capacitors and N-well resistors will save costs and areas compared to other materials in a general CMOS process as shown in Fig. 3.8. Figs. 3.9 and 3.10 show the simulation capacitor values of the two MOS capacitors which are in the accumulation region.

3.3.4 Bias Generator

The self-biased replica-feedback bias generator for the VCO delay cell is shown in Fig. 3.11. It provides two output bias voltages, Vbp and Vbn, from the input signal Vctrl. The primary function is to continuously adjust the bias current of the VCO delay cell to provide the correct lower swing limit Vctrl for the VCO delay cell stages.

As a result, it builds up a current that is held constant and independent of the supply voltage. The self-biased replica-feedback bias generator consists of a PMOS differential source coupled pair, a half-buffer replica and a control voltage buffer. The differential amplifier is actually a unity-gain buffer which forces the voltage of node Vx in Fig. 3.11 equal to Vctrl, a condition required for correct symmetric load swing limits and provides the bias voltage Vbn for the NMOS current source in the VCO delay cell. Besides, the bias voltage Vbn is dynamically adjusted by the differential amplifier to increase the supply noise immunity. With the half-buffer replica, the net result is that the output current of the NMOS current source which is in the VCO delay cell is established by the load element and is independent of the supply voltage. If the supply voltage changes, the amplifier will adjust two bias voltages in the VCO delay cell to keep the swing and the bias current constant. Because the differential amplifier utilizes the self-biased architecture, there are two stable states, one of which is unbiased. As a result, a start-up circuit is needed to bias the amplifier when power-up. Because the differential amplifier and the half-buffer replica form a two-stage negative feedback loop, frequency response issue must be taken into consideration.

Basically, there are two poles in the loop. One is at the differential amplifier output and the other is at the half-buffer replica output. Since the pole at the amplifier output is the dominant one, it can be moved toward origin to increase the phase margin of the loop by adding capacitive loads. Moreover, in order to track any supply and substrate noise that affect the VCO jitter performance, the bandwidth of the self-biased circuit is usually set equal to the operation frequency of the VCO. The bias circuit also provides a buffered version of the control voltage Vctrl using an extra control voltage buffer. This can isolate the control voltage Vctrl from capacitive coupling in the VCO delay cell stages.

3.3.5 Voltage-Controlled Oscillator

The building blocks of the VCO include a five stages ring oscillator. Figs. 3.12 and 3.13 show the schematic of the five stages VCO and the individual delay cell. In order to have the low jitter characteristic of the VCO output clock signals, the delay cell used in VCO should have low sensitivity and high noise rejection capability of the supply and substrate voltage. The supply noise can be categorized into static and dynamic noise. The architecture of the VCO used in this chapter can greatly improved the static and dynamic supply noise.

The delay cell of the VCO contains a source-coupled pair with diode-connected PMOS devices as resistive loads in shunt with an equally sized PMOS device. They are called symmetric loads because their I-V curve is symmetric about the center of the voltage swing, as shown in Fig. 3.14. Basically, to achieve the high noise rejection capability over the supply and substrate noise, the load of the differential pair should have a linear I-V characteristic. In practice, this is difficult to use MOS device to achieve it. However, the symmetric load can cancel the first order of the common mode voltage noise. Therefore, the symmetric load here, though nonlinear, could be used to have high dynamic supply noise immunity. The control voltage, Vbp, is the bias voltage for the PMOS device. In order to provide a bias current that is independent of the static supply noise, the bias voltage of the NMOS current source, Vbn, will be continuously adjusted. As the supply voltage changes, the drain voltage of the NMOS current source also changes. However, the gate bias is adjusted by the self-bias replica-feedback bias generator to keep the output current constant. It seems that it makes the output resistance of the NMOS current source higher. Hence the static supply noise is greatly improved.

Based on the analysis of the I-V curve, it can be shown that the effective resistance of a symmetric load (R_{eff}) is directly proportional to the small signal

resistance at the ends of the swing range which is just one over the transconductance (g_m) for one of the two equally sized PMOS biased at Vctrl. Therefore, the buffer delay is

$$t_d = R_{eff} C_{eff} = \frac{1}{g_m} C_{eff} \tag{3-3}$$

where C_{eff} is the effective buffer output capacitance. The drain current for one of the two equally sized devices biased at Vctrl is

$$Id = \frac{kp}{2}[(VDD - Vctrl) - |Vtp|]^2 \tag{3-4}$$

Taking derivative with respect to Vctrl, the transconductance g_m is given by

$$g_m = kp[(VDD - Vctrl) - |Vtp|] \tag{3-5}$$

The buffer delay is then given by

$$t_d = \frac{C_{eff}}{kp\,[(VDD - Vctrl) - |Vtp|]} \tag{3-6}$$

Thus, for N stages of the VCO, the oscillator frequency is given by

$$f_{osc} = \frac{1}{2Nt_d} = \frac{kp\,[(VDD - Vctrl) - |Vtp|]}{2NC_{eff}} \tag{3-7}$$

The gain of the VCO is given by

$$Kvco = \frac{df_{osc}}{dV_{ctrl}} = \frac{-kp}{2NC_{eff}} \tag{3-8}$$

As a result, Kvco is independent of the delay cell bias current and the VCO has first order tuning linearity. The PLL which is designed in this chapter has ten phases. Therefore, the VCO uses five delay cells with the output clock frequency at 200MHz. The transfer curve simulation result of the VCO is shown in Fig. 3.15. The supply

voltage is 2.5V. For Vctrl between 0.7 V to 1.7 V, the gain of the VCO is 280 MHz per volt and the transfer curve is monotonic.

3.3.6 Differential-to-Single-Ended Converter

Because of the output signal of the VCO delay cell is not full swing, a differential-to-single-ended converter circuit is employed to amplify the output signal. The differential-to-single-ended converter circuit shown in Fig. 3.16 can produce such a 50 % duty cycle full swing output signal. It is composed of two opposite phase NMOS differential amplifiers driving two PMOS common-source amplifiers connected by an NMOS current mirror. The two NMOS differential amplifiers are constructed from the symmetric load delay cell using the same NMOS current source bias voltage so that they receive the correct common-mode input voltage level. They provide signal amplification and a DC bias point for the PMOS common-source amplifiers. The PMOS common-source amplifiers provide additional signal amplification and conversion to a single-ended output through the NMOS current mirror. Because the two levels of amplification are differentially balanced with a wide bandwidth, the opposing differential input transitions have equal delay to the output. The limitations of this circuit in converting the differential signal transitions into rising and falling single-ended output transitions at medium and high bias levels are identical to those of a divider in converting single direction transitions into rising and falling single-ended output transitions. However, using this circuit instead of a divider to generate a 50 % duty cycle output can substantially relax the design constraints on the VCO for high frequency designs.

3.3.7 Divider

Because the output signal frequency of the VCO is 200 MHz and the input

reference signal frequency is 25 MHz, a divided-by-eight divider is needed. As shown in Fig. 3.17, a divided-by-eight divider is constructed from three divided-by-two dividers. A divided-by-two divider is made up of a TSPC D-type flip flop and an inverter. In order to make this circuit have correct operation, the input clock driving capability must be checked.

3.4 PLL PARAMETER DESIGN

Due to the charge pump switching characteristic, the PLL is generally a discrete-time domain operation that is difficult to use continuous-time domain analysis. However, if under some condition, the s-domain model could also be used to get a thorough understanding of the negative feedback loop. Fig. 3.18 shows the linear model of the PLL.

Assume the PLL is in lock state. The PFD and CP have a current change of $I_p/2\pi$ (A/rad), the loop filter has a transfer function F(s) (V/A), the VCO has a gain of K_{vco} (Hz/V), and the feedback factor is 1/N. The conversion gain of the VCO should be changed to $2\pi K_{vco}/s$ (rad/sec-V), because the phase is the integral of the frequency. Based on the above definitions and the PLL linear model, the open loop gain of the PLL can be represented as

$$G(s)\times\beta(s)=\frac{\theta_{back}(s)}{\theta_{in}(s)}=\frac{I_P\times K_{vco}\times F(s)}{s\times N} \tag{3-9}$$

The closed loop transfer function of the PLL is given by

$$H(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{G(s)}{1+G(s)\times\beta(s)}=\frac{N\times G(s)}{N+G(s)}=\frac{N\times K}{s+K} \tag{3-10}$$

Therefore, the 3-dB bandwidth is

$$\omega_{3dB} = K = \frac{I_P \times K_{vco} \times F(s)}{N} \tag{3-11}$$

From the analysis of the loop filter in section 3.3.3, it is obvious that the shunt capacitance C_2 is typically much smaller than C_1. Therefore, the capacitor C_2 is neglected and the classical two-pole system and second-order linear model of the PLL are used to analyze the characteristic of the PLL transient response. With $F(s) = R_1 + (1/sC_1)$, the closed loop transfer function can be derived as

$$H(s) = \frac{I_P \times K_{vco}}{C_1} \cdot \frac{(1 + SR_1C_1)}{S^2 + \frac{I_P K_{vco} R_1}{N} S + \frac{I_P K_{vco}}{NC_1}} \tag{3-12}$$

Equation (3-12) can be compared to the classical two-pole system transfer function

$$H(s) = \frac{2\zeta \times \omega_n + {\omega_n}^2}{S^2 + 2\zeta \times \omega_n \times S + {\omega_n}^2} \tag{3-13}$$

Therefore, the natural frequency ω_n, and the damping factor ζ can be derived as

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{NC_1}} \tag{3-14}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{vco} C_1}{N}} \tag{3-15}$$

In the case of the PLL design, the frequency noise of the VCO could be the dominant noise source to influence the phase noise performance. As will be seen in the later section, the noise of the VCO has the high pass characteristic. Therefore, a large loop bandwidth for the PLL feedback system is better because it can enhance the tracking ability. The choice of the damping factor ζ is a trade off between acquisition time and step response stability. If larger ζ is chosen, the system could have longer acquisition time. On the other hand, if smaller ζ is chosen, the system may be ringing for step response or become unstable.

Then, we use the loop bandwidth and the phase margin to determine the component values of the loop filter. By substituting equation (3-2) into equation (3-11), we can get

$$Loop\ BW = \frac{I_P \times K_{vco}}{N} \cdot \frac{R_1 C_1}{C_1 + C_2} \tag{3-16}$$

From equation (3-17), the phase term will be determined based on the pole and zero of the loop filter such that the phase margin is calculated as

$$PM = \tan^{-1}\frac{BW}{\omega_z} - \tan^{-1}\frac{BW}{\omega_p} \tag{3-17}$$

By setting the derivative of the phase margin equal to zero, the maximum phase margin is obtained when the loop bandwidth is set to the average of pole and zero.

$$BW = \sqrt{\omega_z \omega_p} \tag{3-18}$$

We can define a new parameter, γ, as

$$\gamma = \frac{BW}{\omega_z} = \frac{\omega_p}{BW} \tag{3-19}$$

From equation (3-20), the capacitance ratio of C_1 and C_2 can be represented by

$$\frac{C_1}{C_2} = \gamma^2 - 1 \tag{3-20}$$

The loop bandwidth (BW) now can be written as

$$BW = \frac{I_p \times K_{VCO}}{N} \cdot R_1 \left(1 - \frac{1}{\gamma^2}\right) \tag{3-21}$$

The design flow of a third-order PLL can be derived from equations (3-19), (3-20) and (3-21). The design flow can be summarized as follows:

(1) Determine K_{vco} by measuring VCO test keys or simulating a VCO using in the

design or referring to the data sheets of the employed commercial VCO.

(2) Depending on the desired noise and transient performance, determine the loop bandwidth BW. Usually, the BW is less than 1/10 of the reference clock.

(3) If the filter is off-chip, set I_p to be around 100μA to 1mA. If an on-chip filter is employed, decrease the value of I_p so that the reasonable trade off between chip area and charge pump current could be reached.

(4) Determine the nominal value of N according to the system to be applied to.

(5) Selecting the required PM specification. The zero and pole positions are then determined by equation (3-19).

(6) With BW, I_p, PM, N, and K_{vco} determined, R_1 can be calculated with equation (3-21).

(7) Calculate the value of C_1 with $C_1=1/R_1\omega_z$.

(8) Calculate the value of C_2 by equation (3-20).

The parameters used in the designed PLL are listed in Table. 3.1. The PLL open loop simulation result is shown in Fig. 3.19. Fig. 3.20 shows the SPICE simulation of the PLL closed-loop control voltage Vctrl. Fig. 3.21 shows the ten even-spaced phases of frequency 200 MHz which can be utilized to perform parallel-to-serial conversion of parallel data.

3.5 PLL NOISE ANALYSIS AND STABILITY

The PLL timing jitter could affect the maximum timing margin of the transceiver and therefore the performance of the serial link. The output clock jitter performance of the PLL depends on the jitter of the VCO, input source, and the design of the loop parameters. There are some sources of noise that contribute the output jitter in the

PLL as shown in Fig. 3.22, where θ_{in} is the reference noise, θ_{pfd} is the PFD and CP noise, θ_{lf} is the loop filter noise and θ_{vco} is the VCO noise.

These noise sources introduce the phase fluctuations or timing jitter in time domain. Using closed loop analysis, the transfer functions with different noise sources can be derived as

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{N \times K}{s + K} \tag{3-22}$$

$$H_{pfd}(s) = \frac{\theta_{out}(s)}{\theta_{pfd}(s)} = 2\pi \cdot \frac{N}{I_P} \cdot \frac{K}{s + K} \tag{3-23}$$

$$H_{lf}(s) = \frac{\theta_{out}(s)}{\theta_{lf}(s)} = 2\pi \cdot \frac{K_{vco}}{s + K} \tag{3-24}$$

$$H_{vco}(s) = \frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{s}{s+K} = 1 - \frac{H(s)}{N} \tag{3-25}$$

where H(s) and K are given in (3-10) and (3-11). Each noise transfer function has its own characteristics. H(s) and $H_{pfd}(s)$ are low-pass functions, $H_{lf}(s)$ is a band-pass function, and $H_{vco}(s)$ is a high-pass function. Therefore, based on the different frequency responses of the transfer functions, there exists a trade off in choosing the wide or narrow bandwidth. Narrow bandwidth of PLL will suppress noise from the input reference source and PFD part, while wide one will suppress noise from the VCO. Most of the time, the input source of the PLL is from the crystal oscillator, which has much smaller phase noise than the one of the VCO. Therefore, the input source could be viewed as jitter-free. Based on the analysis, the loop bandwidth of the PLL should be maximized to meet the high-pass function of the VCO to reduce the timing jitter. The maximum nature frequency ω_n of the PLL is restricted of the reference clock frequency ω_{in}. Using the analysis from the PLL, the criteria of the

stability limit can be derived as

$$\omega_n{}^2 < \frac{\omega_{in}{}^2}{\pi(R_1 C_1 \omega_{in} + \pi)} \tag{3-26}$$

As a rule of thumb, stability can be assumed by keeping $\omega_n < 1/10\ \omega_{in}$. Choosing larger loop bandwidth indicates that more phase noise from the input clock will transfer to the output with larger loop bandwidth. However, it does not cause a problem when the input is a clean clock source.

3.6 PLL MEASUREMENT RESULT

Fig. 3.23 shows the die photo of the PLL. The total chip area of the PLL is 420 μm × 280 μm. Fig. 3.24 shows the measurement setup of the PLL. The pulse generator (HEWLETT PACKARD 8131A) is utilized to generate the reference signal of the PLL and the oscilloscope (Tektronix TDS 3054B) is used to obverse the PLL output signals. One external resistor is employed between the power supply and the chip in order to provide an adequate current for the charge pump. Figs. 3.25 and 3.26 show the top and bottom view of the testing PCB photo. The different frequency of the VCO and divider output signals are shown in Fig. 3.27, Fig. 3.28, Fig. 3.29, Fig. 3.30 and Fig. 3.31. Due to the divided by eight divider, each time period of the divider output signal contains eight VCO output signals. The long-term peak-to-peak jitter of the divider output signal at 25 MHz is 64 ps which is 0.16 % of the divider output signal time period as shown in Fig. 3.32. The long-term peak-to-peak jitter of the VCO output signal at 200 MHz is 68 ps which is 1.36 % of the VCO output signal time period as shown in Fig. 3.33. Some simulated and measured parameters of the PLL are summarized in Table 3.1.

3.7 CONCLUSION

PLLs are analog building blocks used extensively in many analog and digital systems. Although PLLs are highly nonlinear systems, it has been found that when they are in lock, their transient behavior can be reasonably well approximated by linear differential equations. The designed PLL in this chapter has ten different phases of output signals which are 200 MHz. The tuning frequency of the PLL is from 80 MHz to 360 MHz. The main application of the designed PLL is to perform the parallel-to-serial conversion with a multiplexer which is used in a transmitter. The transmitter is utilized to transmit parallel video signals to the flat panel timing controller with high speed in flat panel display systems. In order to obtain a better performance transmitter, the embedded PLL should have good jitter performance and can resist supply and substrate noise.

Table 3.1

The simulated and measured parameters of the designed PLL.

Function	PLL
Simulation Results	
Operate Voltage	2.5 V
Input Frequency	25 MHz
Output Frequency	200 MHz
Charge Pump Current	50 μA
Divided by N	N = 8
VCO Gain	280 MHz/V
C_1	77.78 pF
C_2	3.68 pF
R_1	6 kΩ
Phase Margin	66 °
Loop Bandwidth	1.6 MHz
Extra Zero	0.34 MHz
Extra Pole	7.48 MHz
Natural Frequency	0.754 MHz
Damping Factor	1.1
Power	100 mW@200 MHz
Measurement Results	
Technology	VIS 0.25-μm 1P5M CMOS
Power	135 mW@200 MHz
Output Clock Jitter (1)	68 ps (long-term peak-to-peak jitter)@200 MHz, < 1.36 %
Output Clock Jitter (2)	64 ps (long-term peak-to-peak jitter)@25 MHz, < 0.16 %

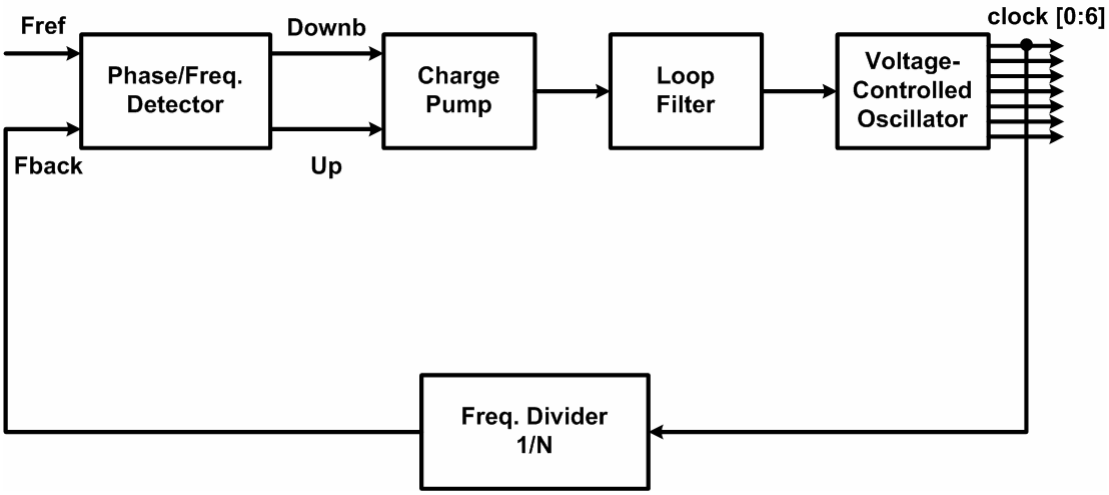


Fig. 3.1 The basic architecture of PLL.

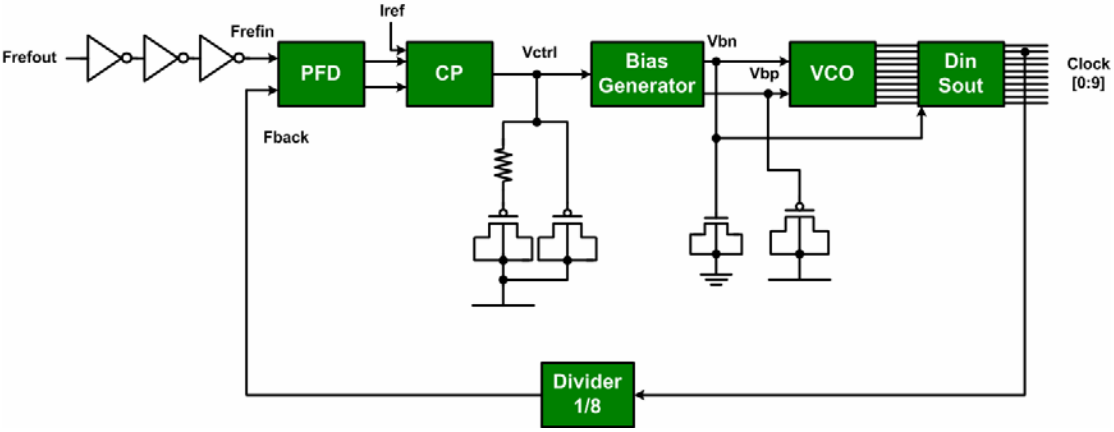


Fig. 3.2 The architecture of the designed PLL. The input reference clock frequency is 25 MHz and the output clock frequency is 200 MHz due to the frequency divider which is divided by eight.

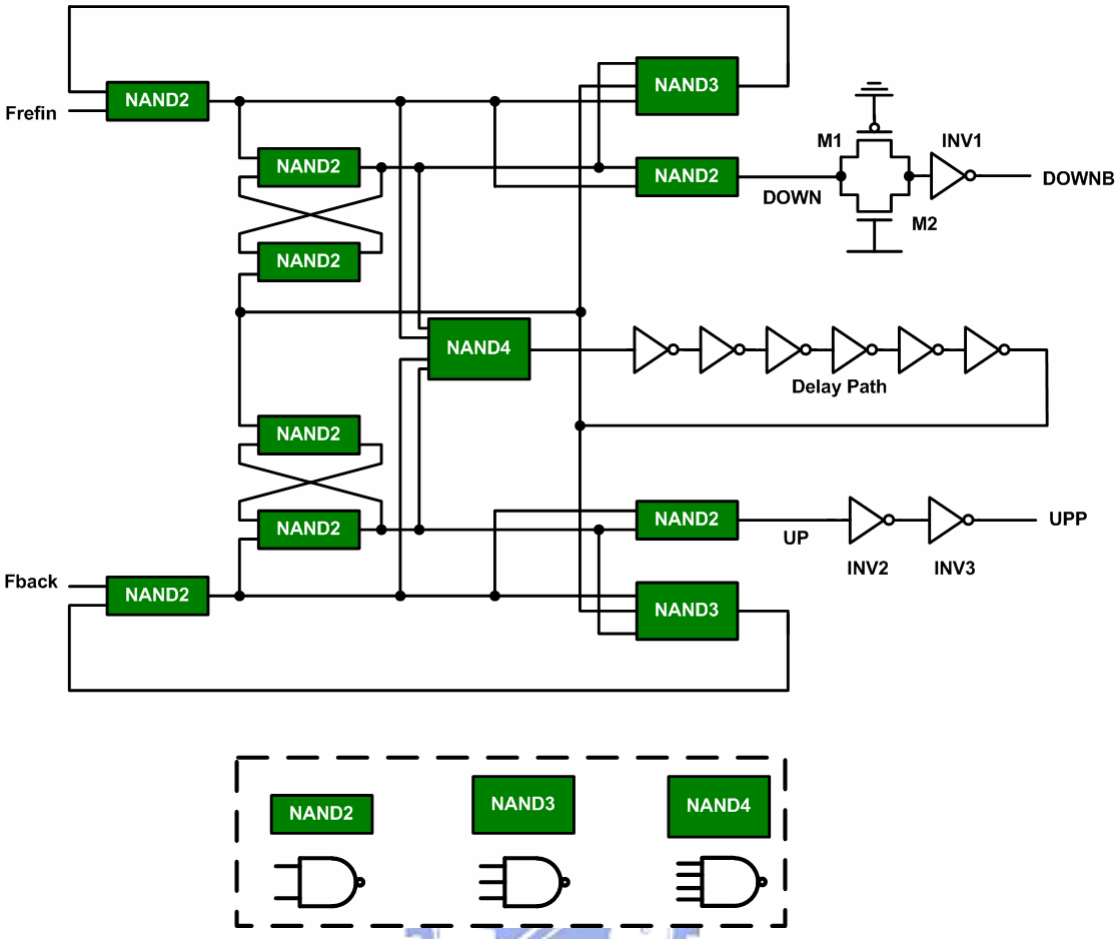


Fig. 3.3 The circuit implementation of the PFD.

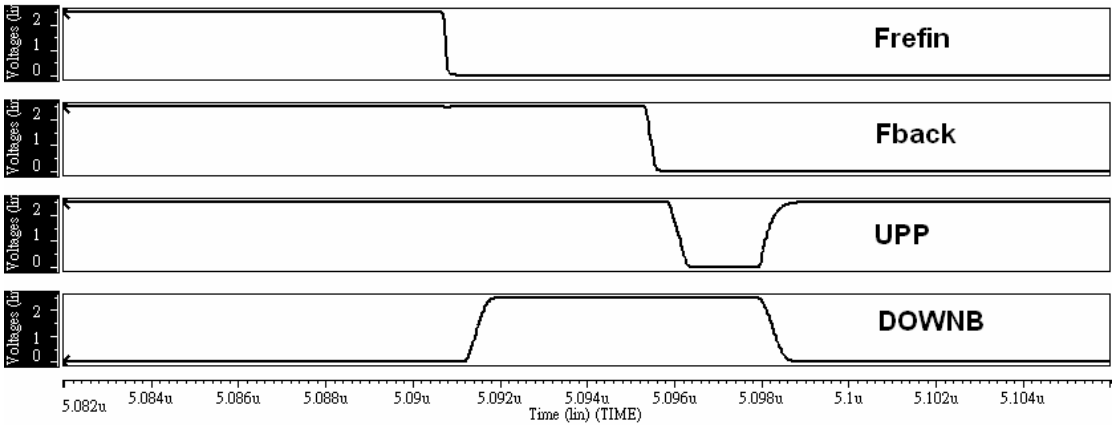


Fig. 3.4 The reference signal (Frefin) is earlier than the feedback signal (Fback). The output signal (UPP) is set to ground for a short duration after another output signal (DOWNB) was asserted for a while, and then both output signals are reset to their initial states.

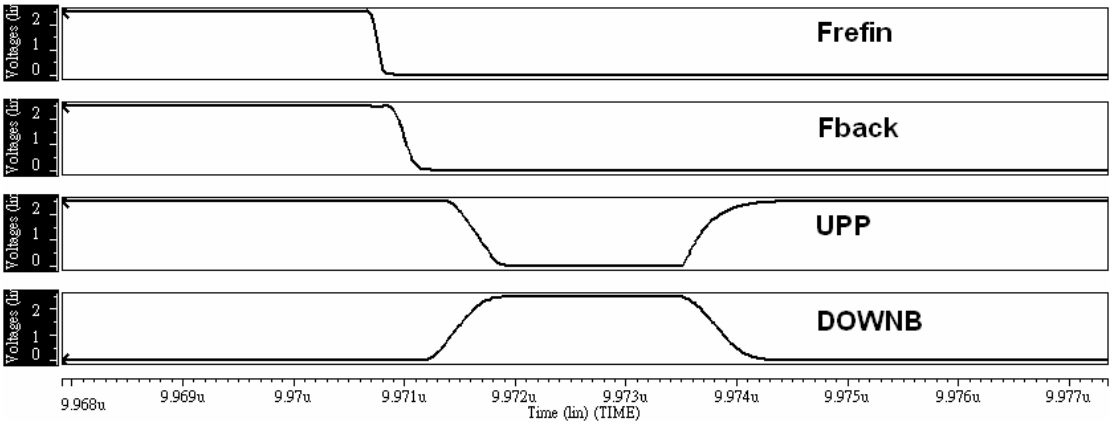


Fig. 3.5 The reference signal (Frefin) and the feedback signal (Fback) are in-phase. Both output signals (UPP and DOWNB) are altered from their initial states on every cycle in order to eliminate the dead zone region.

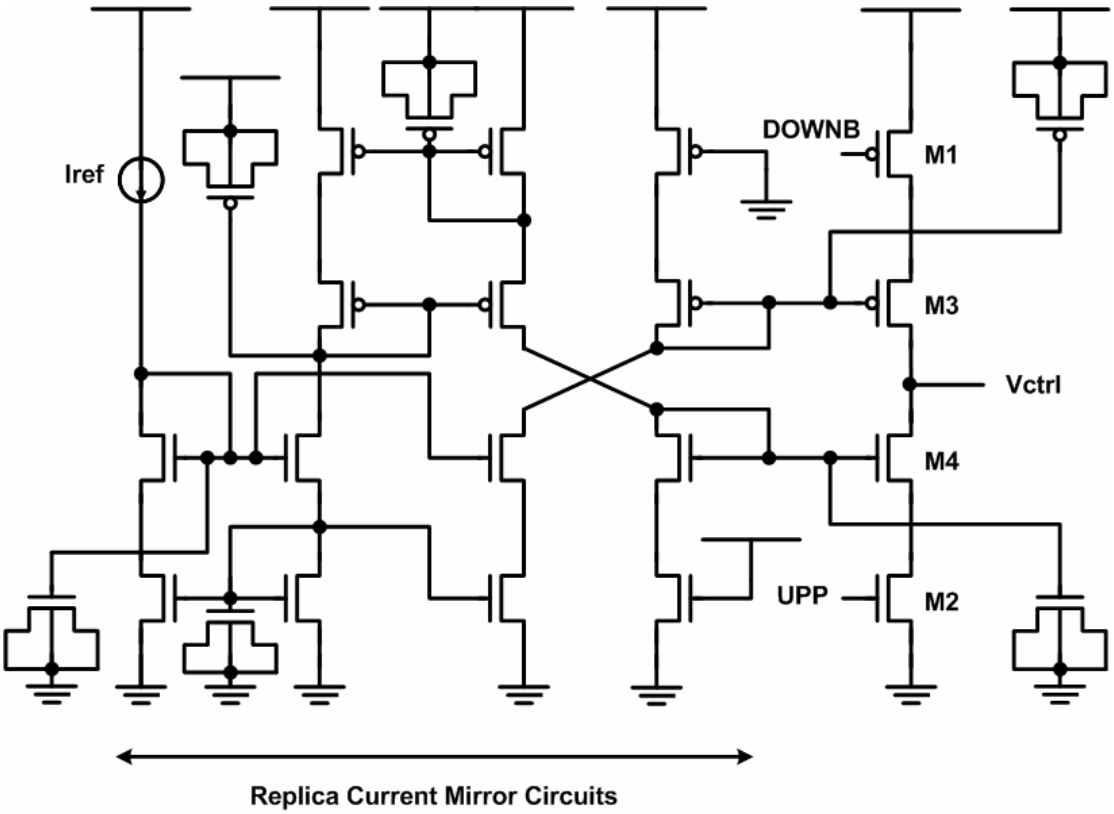


Fig. 3.6 The circuit implementation of the charge pump.

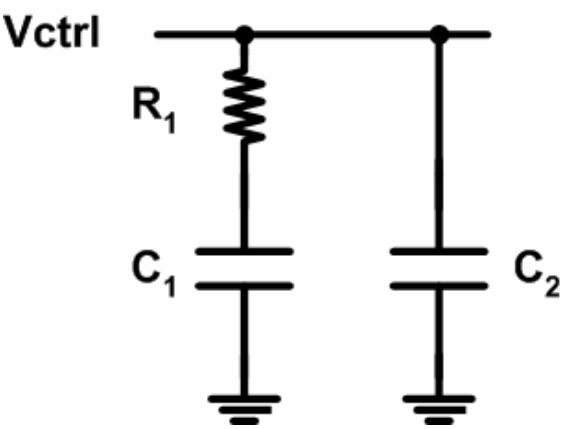


Fig. 3.7 Schematic of the loop filter.

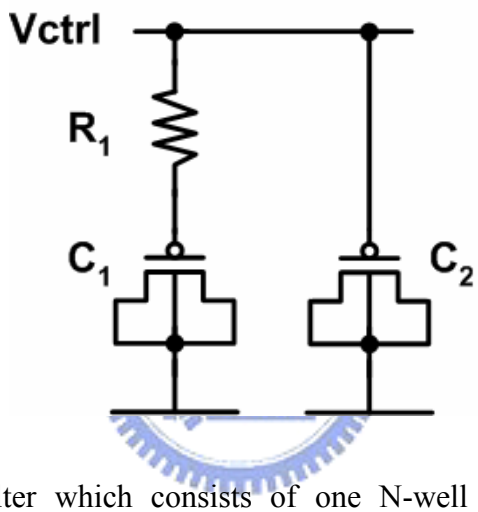


Fig. 3.8 The loop filter which consists of one N-well resistor and two MOS capacitors.

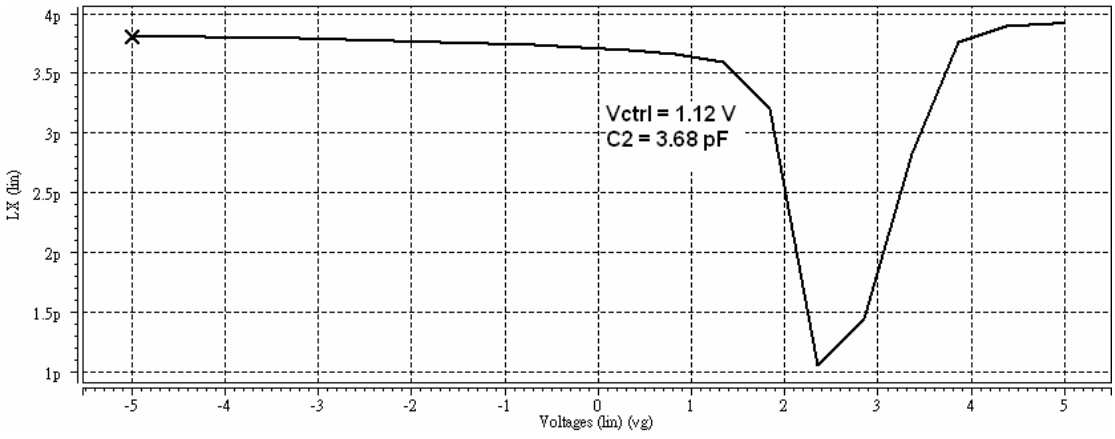


Fig. 3.9 Simulation of the MOS capacitor. The Vctrl is 1.12 V when the PLL is locked and the MOS capacitor C_2 is in the accumulation region with the capacitor value 3.68 pF.

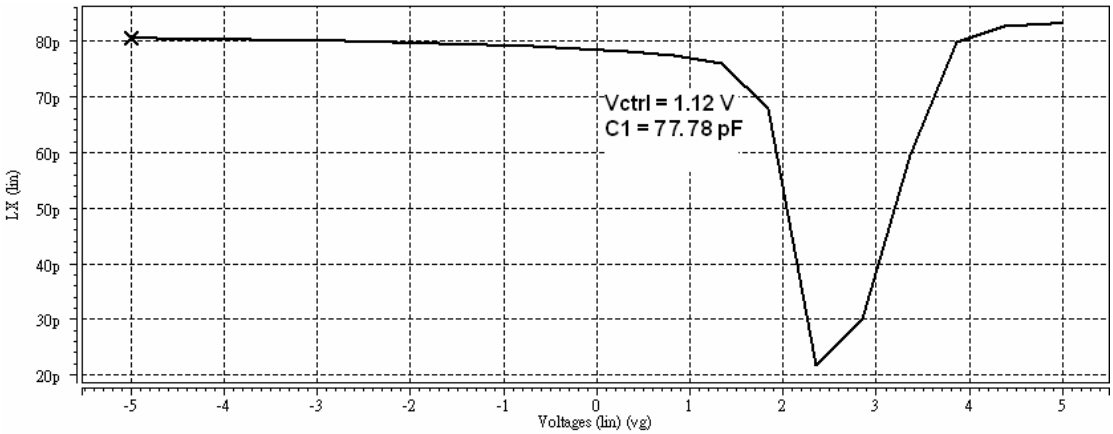


Fig. 3.10 Simulation of the MOS capacitor. The Vctrl is 1.12 V when the PLL is locked and the MOS capacitor C_1 is in the accumulation region with the capacitor value 77.78 pF.

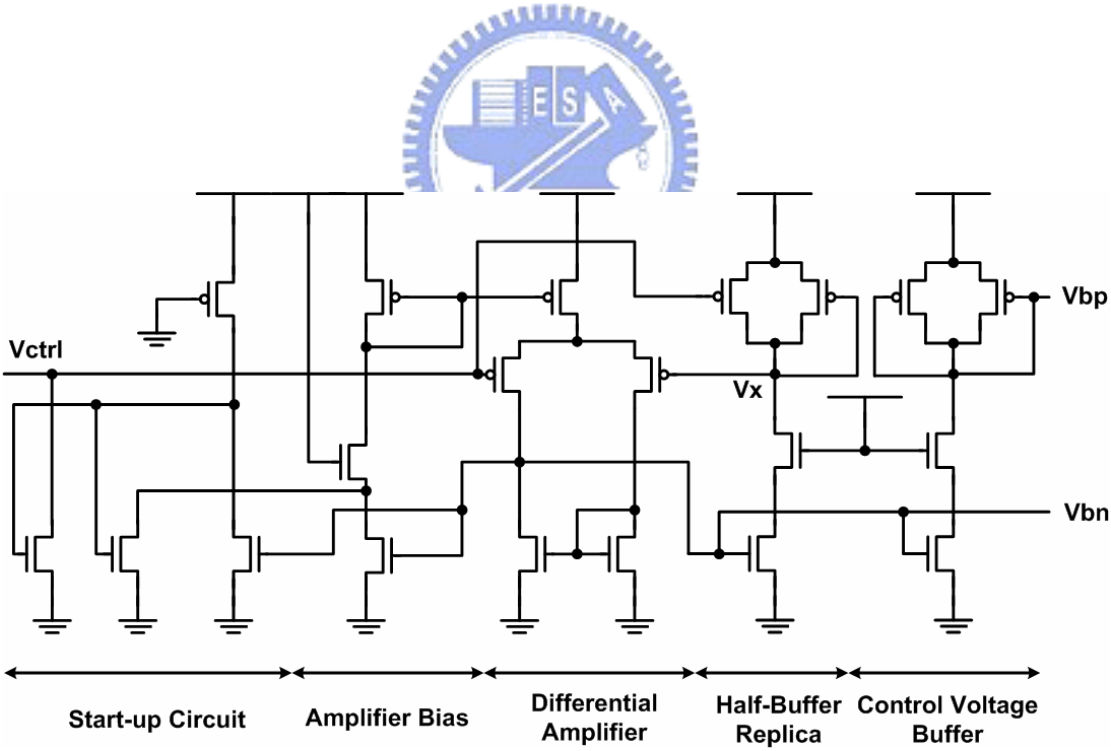


Fig. 3.11 The circuit implementation of the self-biased replica-feedback bias generator.

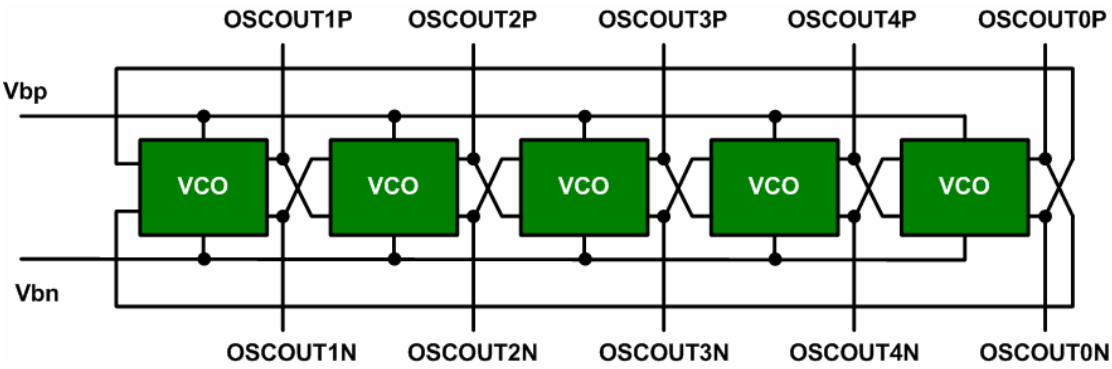


Fig. 3.12 Schematic of the five stages VCO.

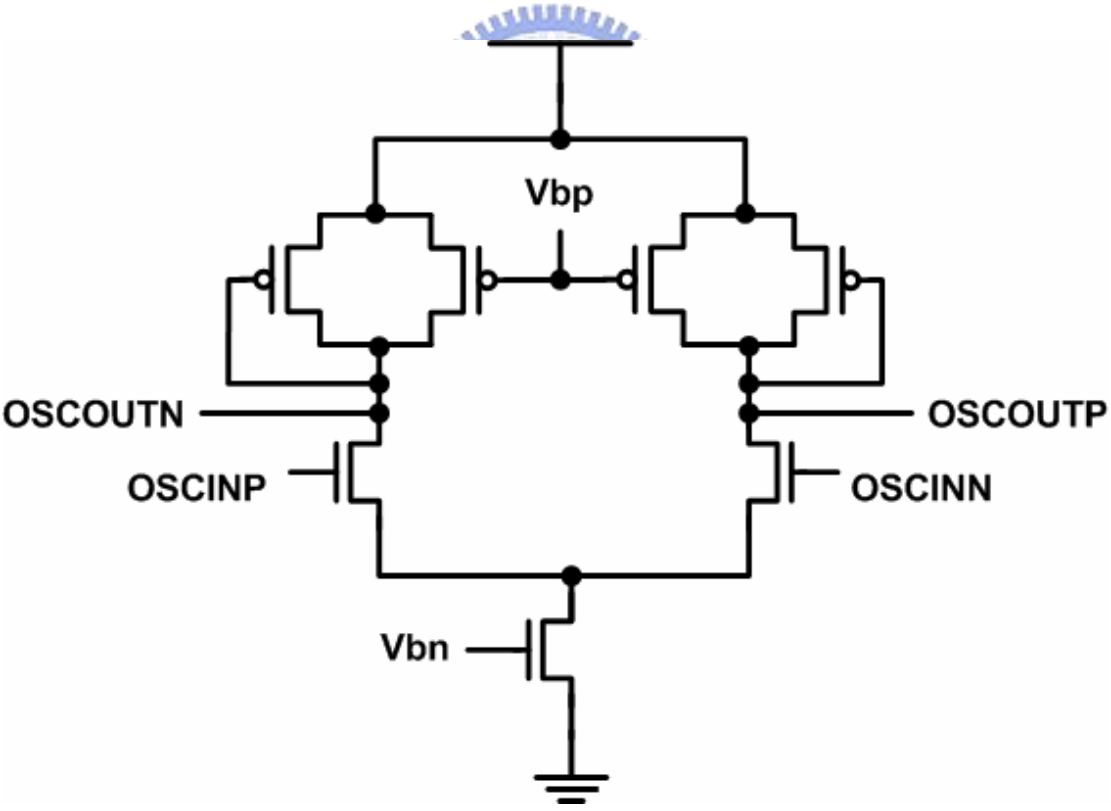


Fig. 3.13 The circuit implementation of the individual delay cell.

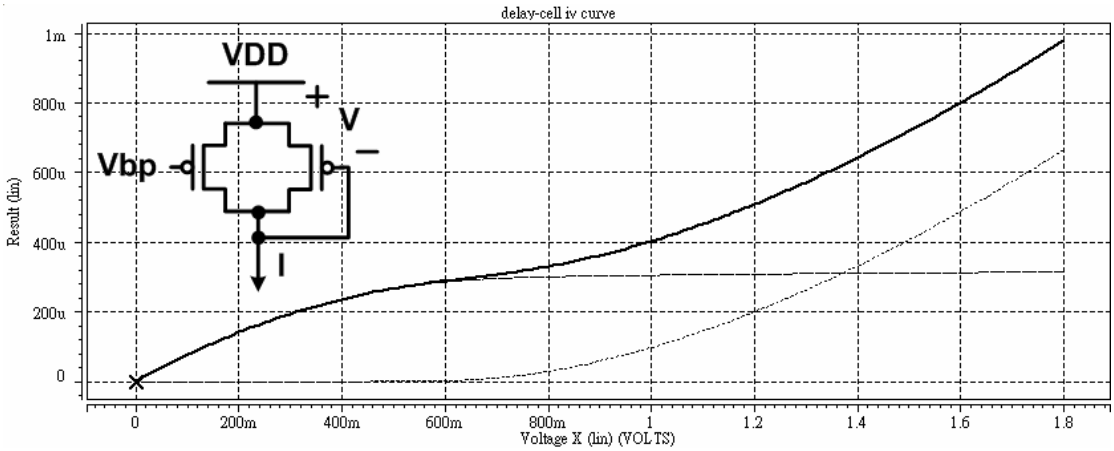


Fig. 3.14 I-V curve of the symmetric load.

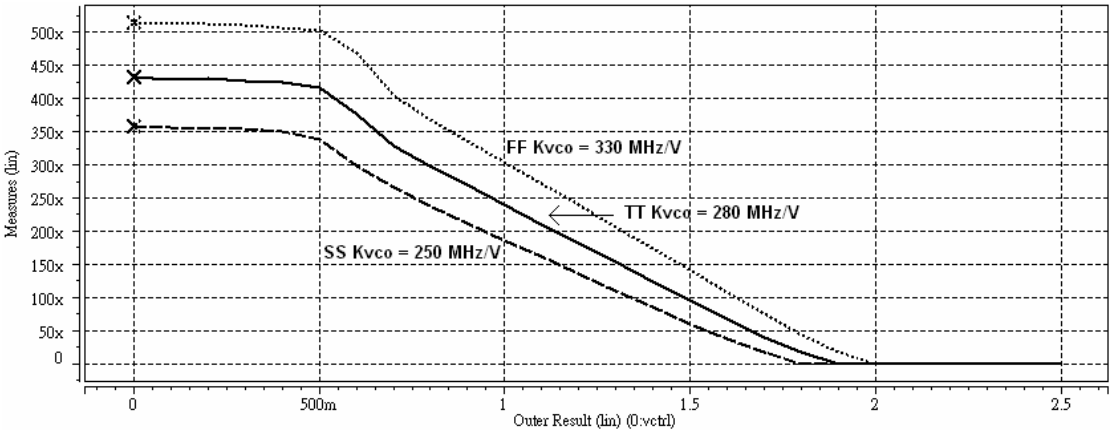


Fig. 3.15 Transfer curve of the VCO.

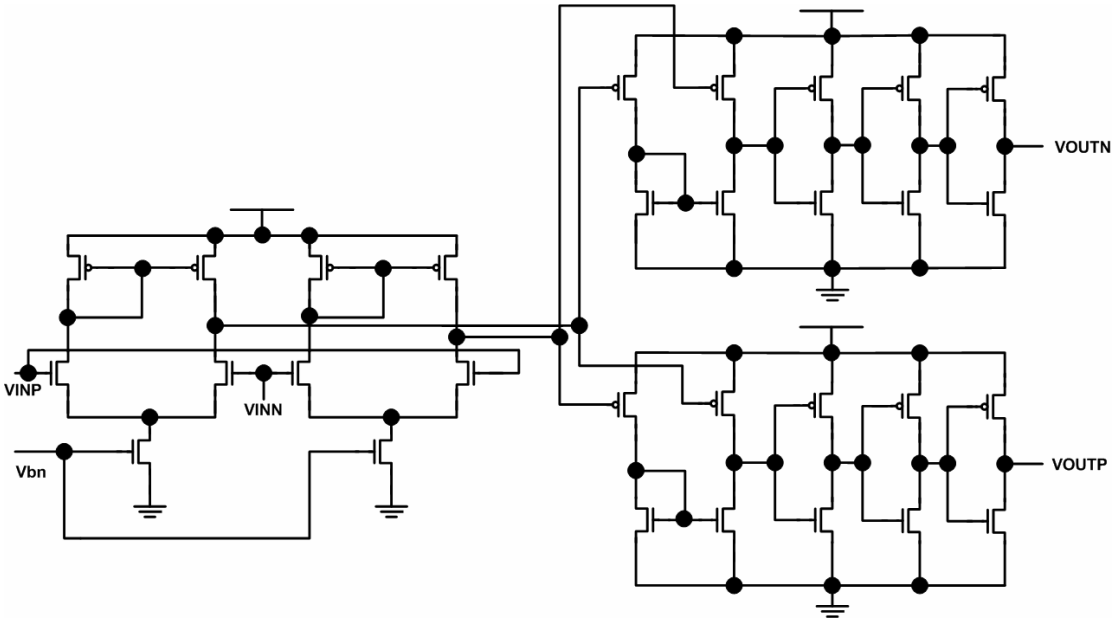


Fig. 3.16 The circuit implementation of the differential-to-single-ended converter.

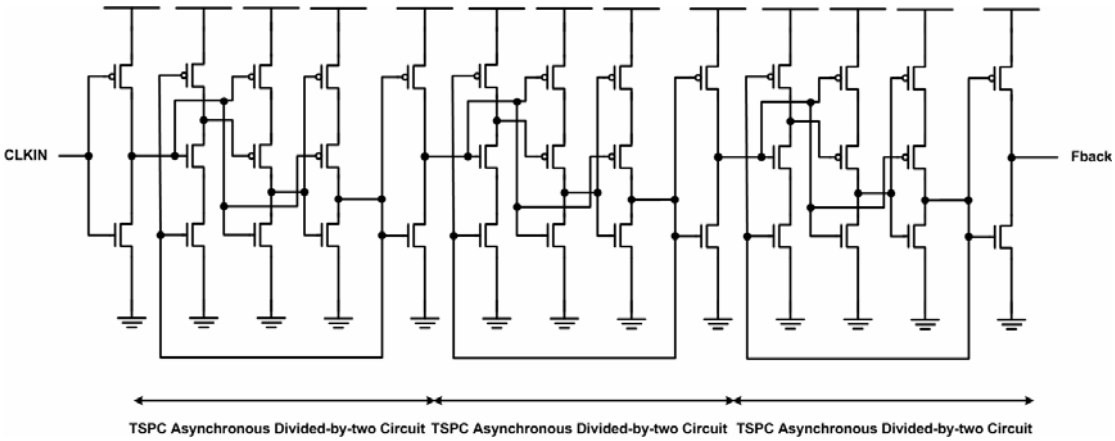


Fig. 3.17 The circuit implementation of the divided-by-eight divider which consists of three divided-by-two dividers.

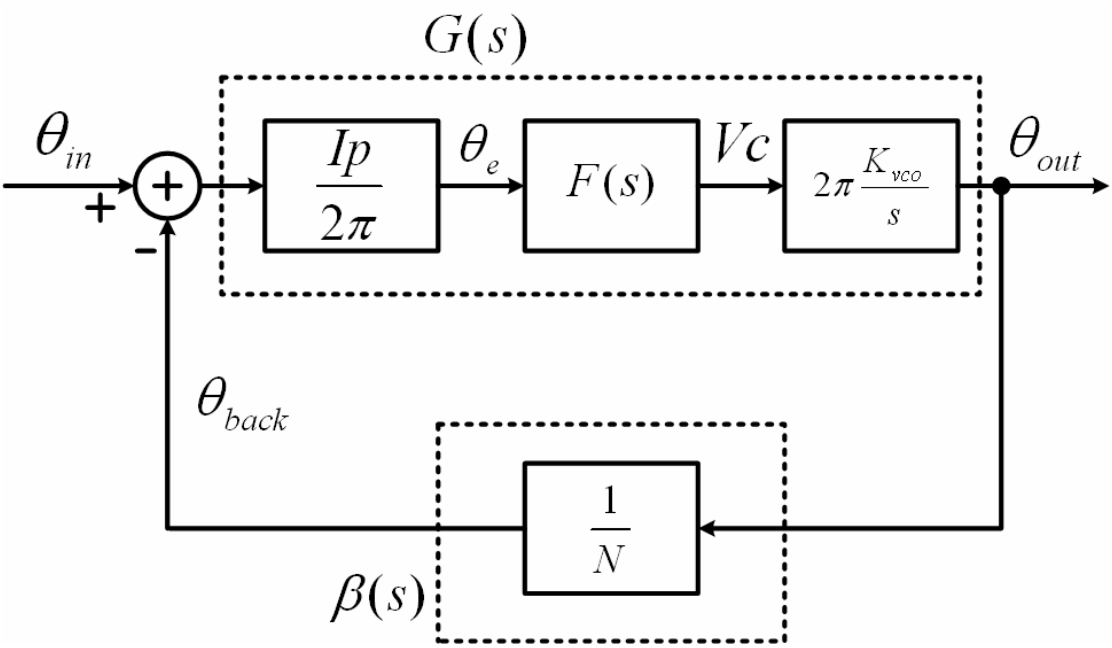


Fig. 3.18 Linear model of the PLL.

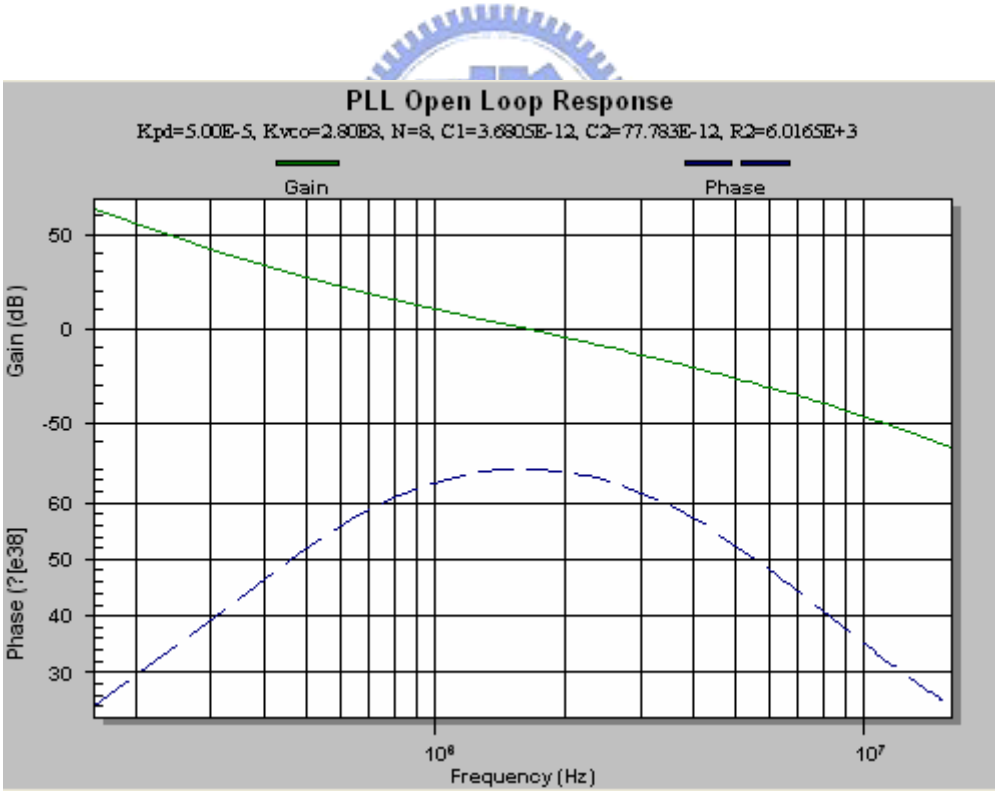


Fig. 3.19 The simulation of the PLL open loop using the parameters in Table 3.1.

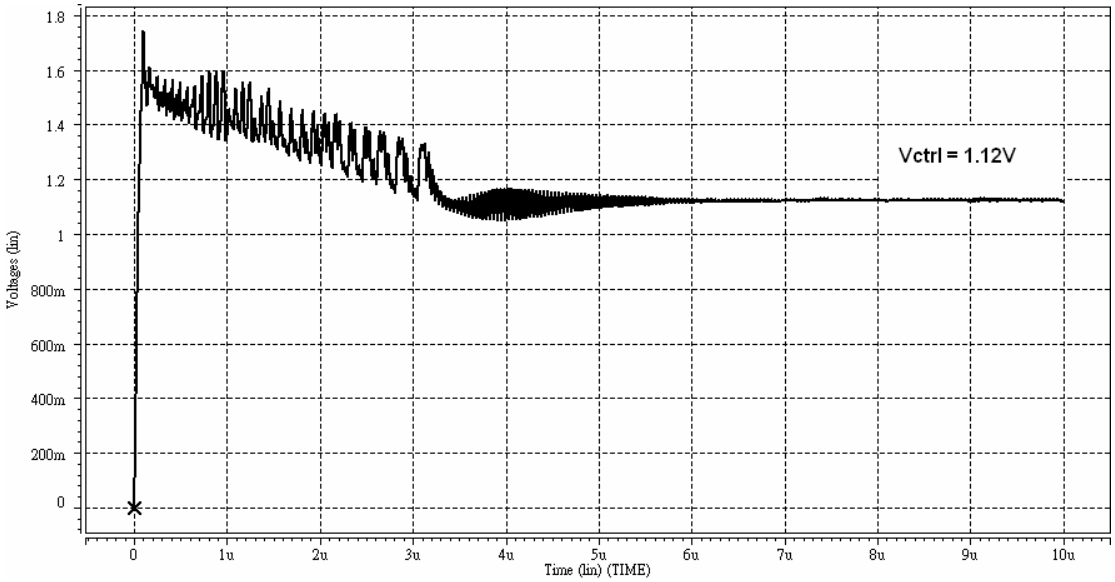


Fig. 3.20 The SPICE simulation of the PLL closed-loop control voltage Vctrl.

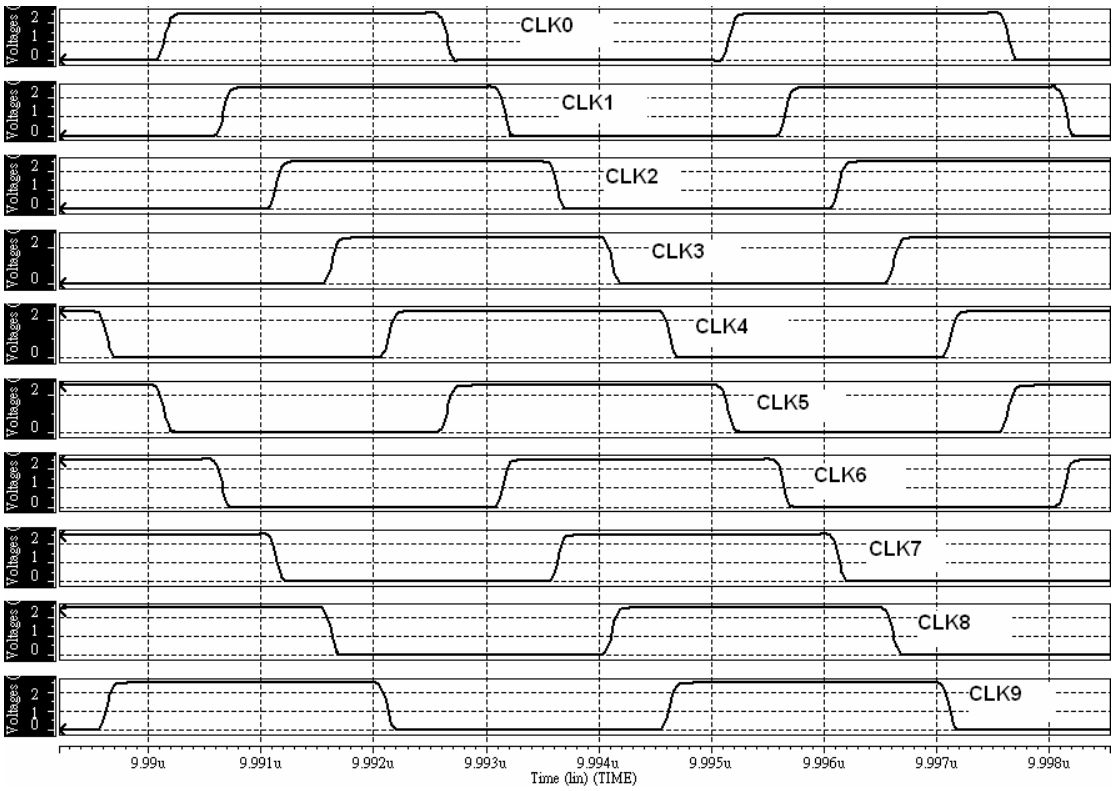


Fig. 3.21 The SPICE simulation of the ten even-spaced output phases of the PLL.

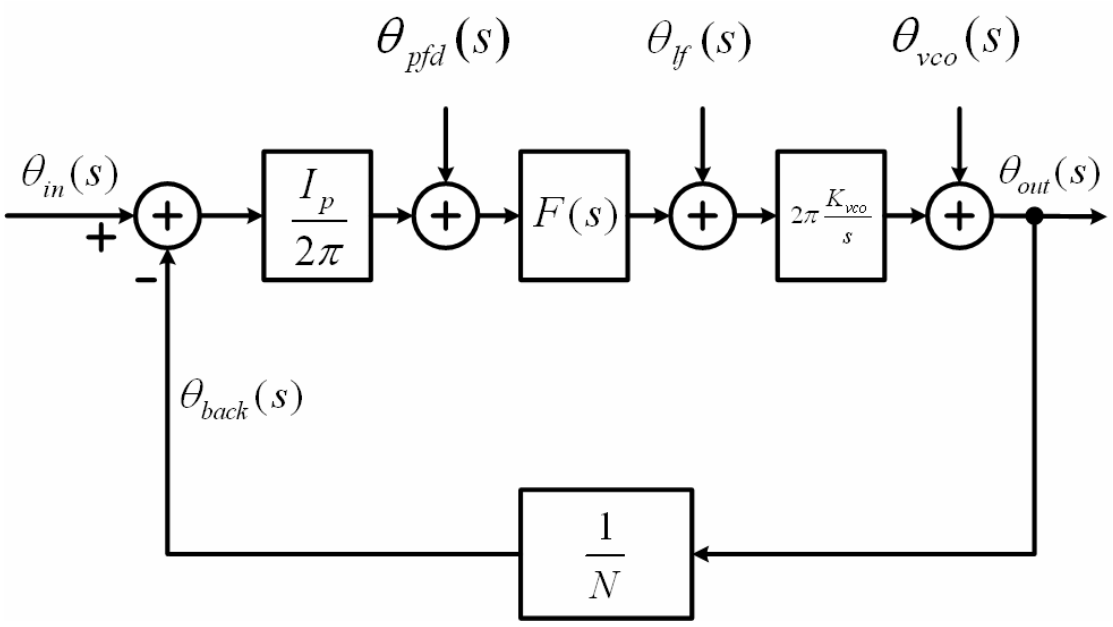


Fig. 3.22 The linear model of the PLL with different noise sources.

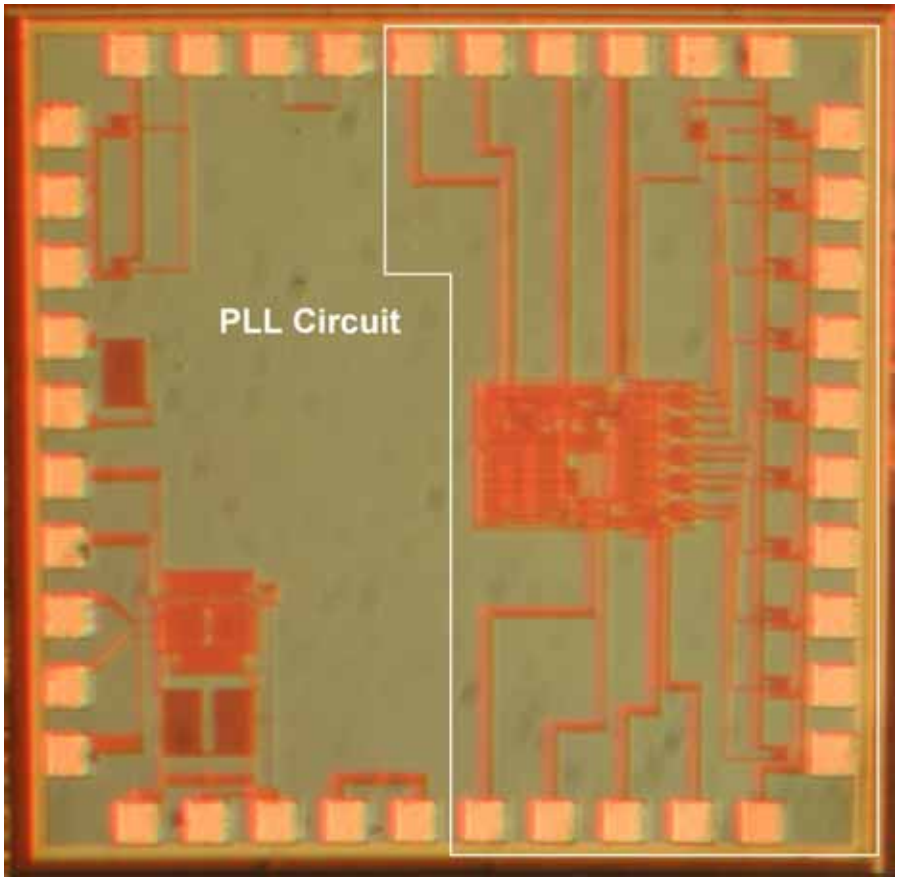


Fig. 3.23 The die photo of the PLL.

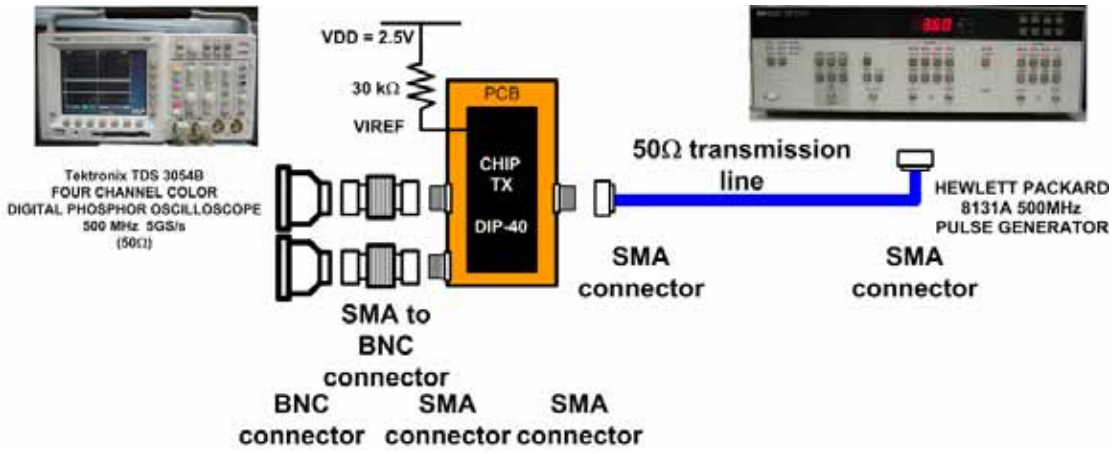


Fig. 3.24 The measurement setup of the PLL.

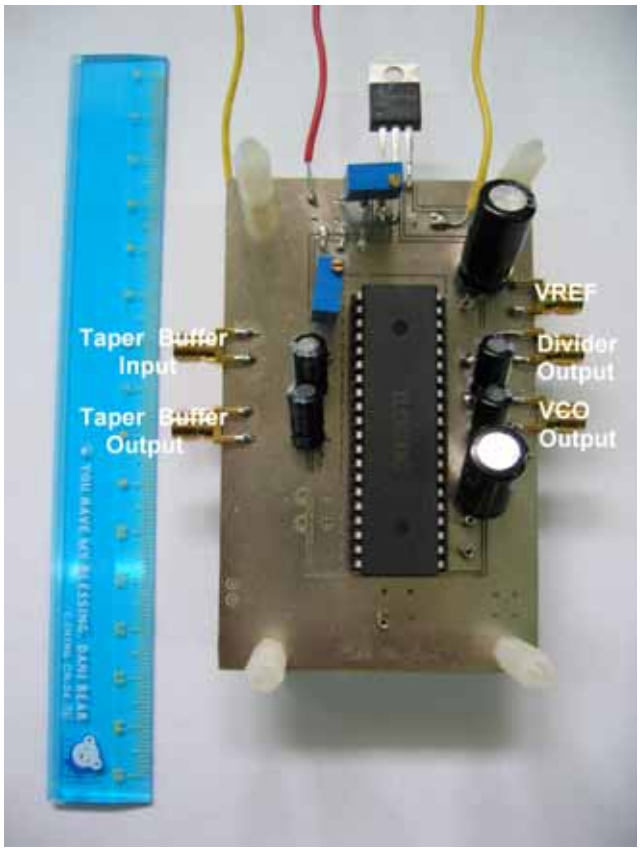


Fig. 3.25 The top view of the testing PCB photo.

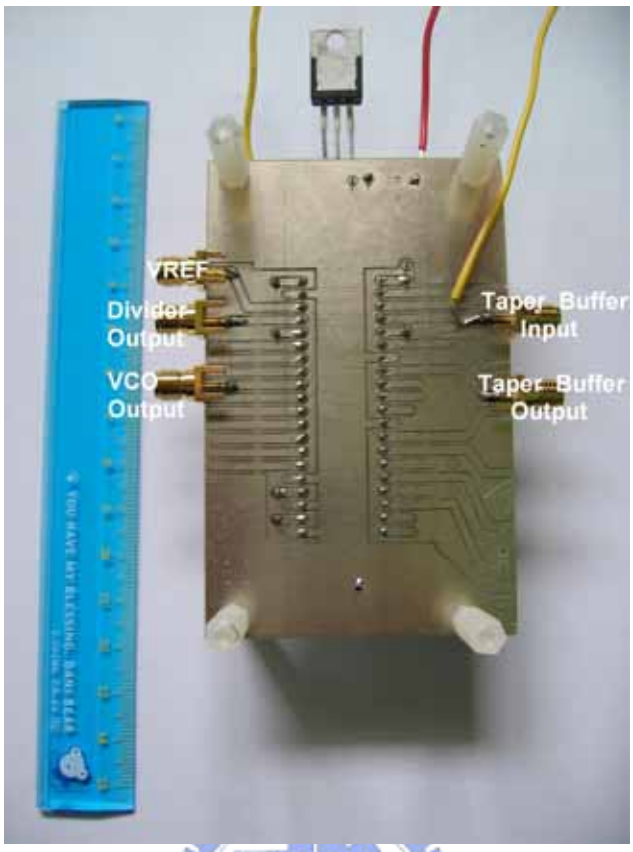


Fig. 3.26 The bottom view of the testing PCB photo.

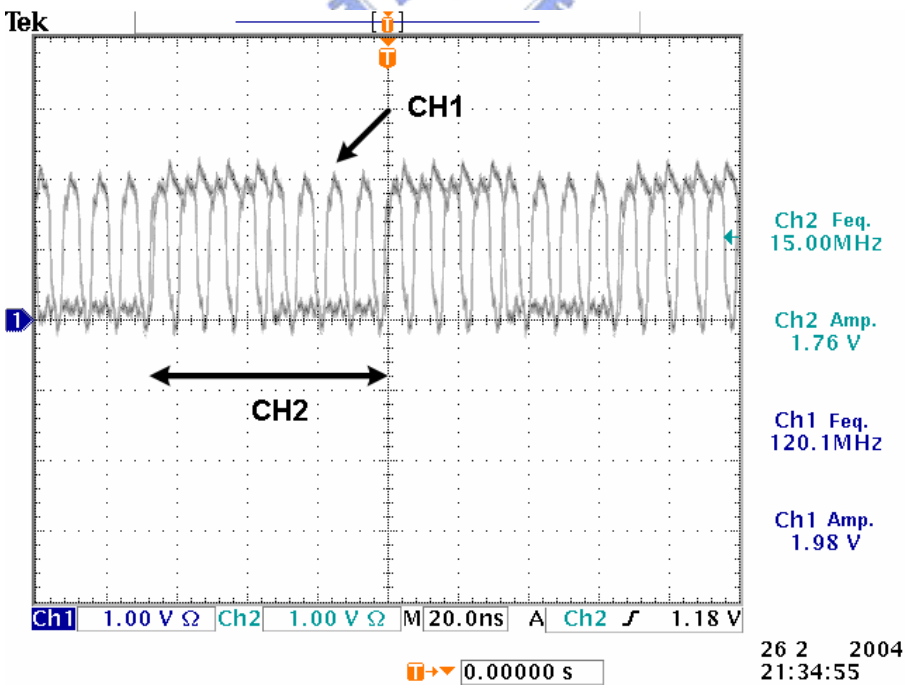


Fig. 3.27 Ch1 is the measured signal of the VCO output (120 MHz) and Ch2 is the measured signal of the divider output (15 MHz).

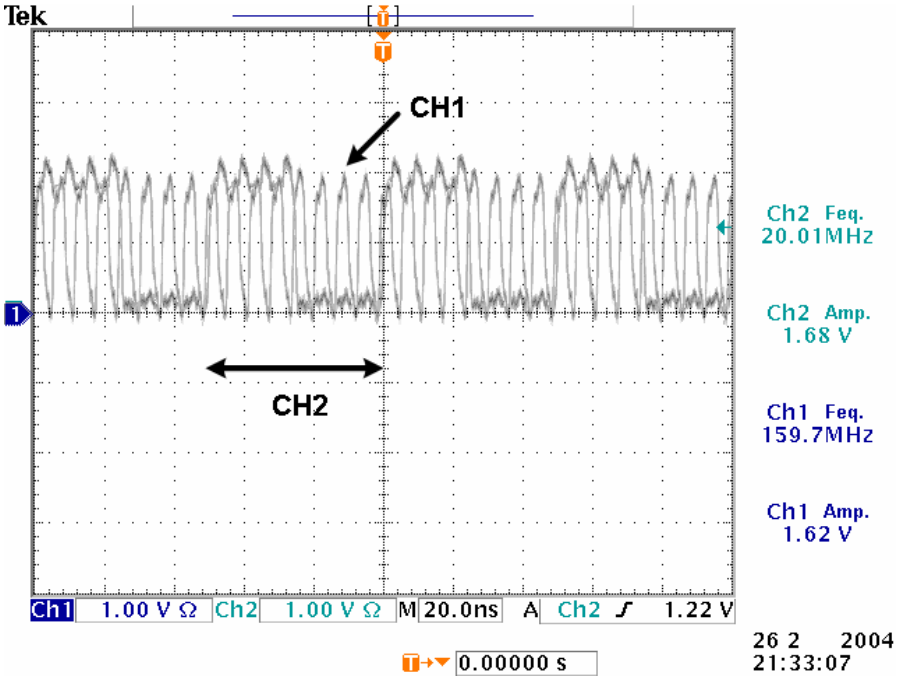


Fig. 3.28 Ch1 is the measured signal of the VCO output (160 MHz) and Ch2 is the measured signal of the divider output (20 MHz).

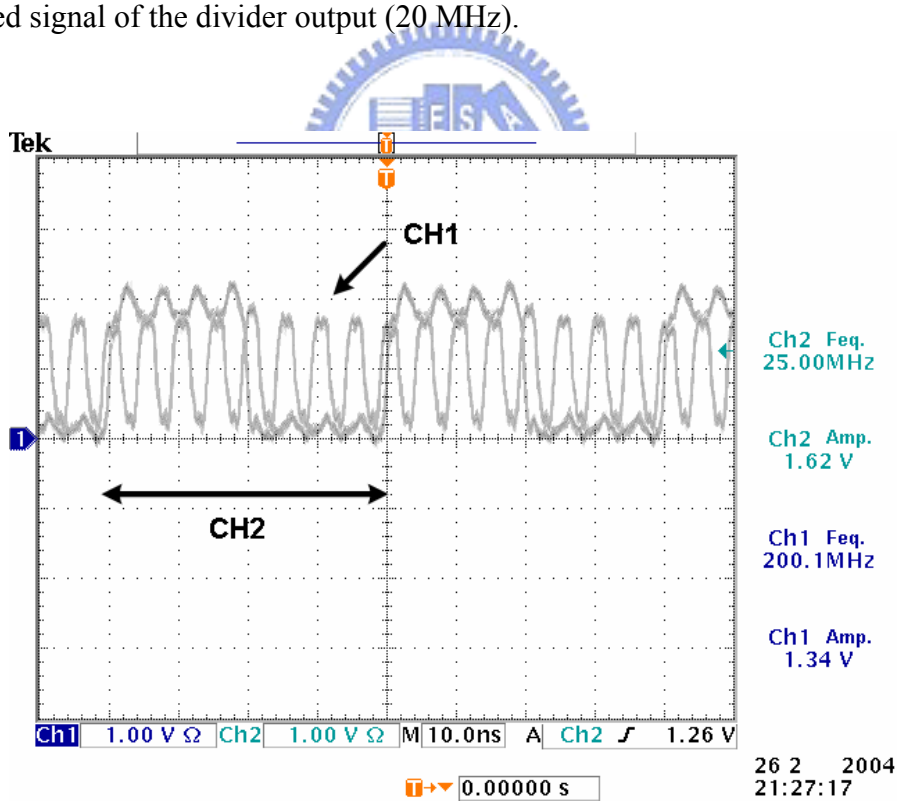


Fig. 3.29 Ch1 is the measured signal of the VCO output (200 MHz) and Ch2 is the measured signal of the divider output (25 MHz).

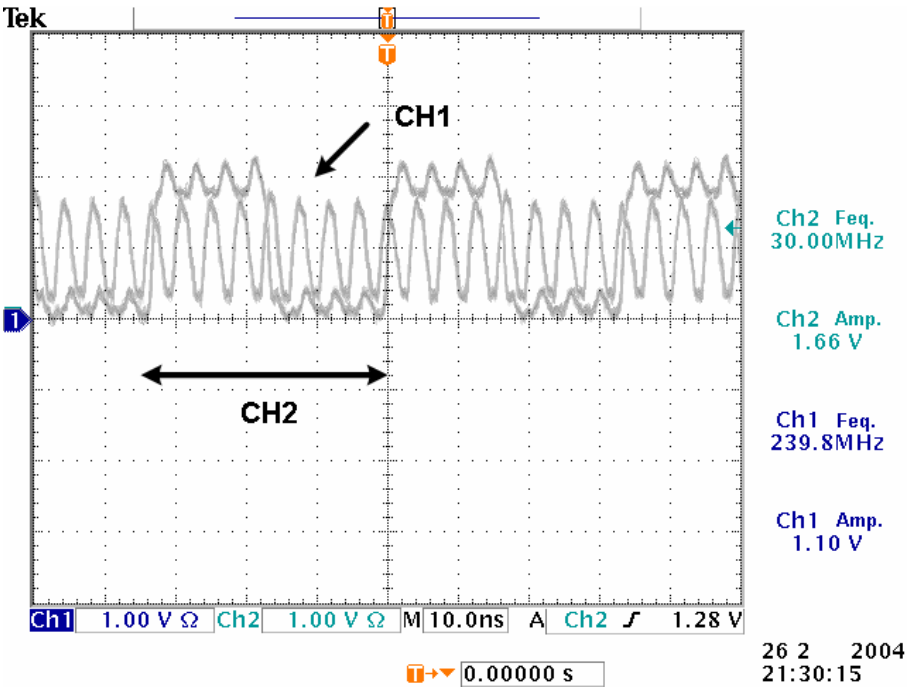


Fig. 3.30 Ch1 is the measured signal of the VCO output (240 MHz) and Ch2 is the measured signal of the divider output (30 MHz).

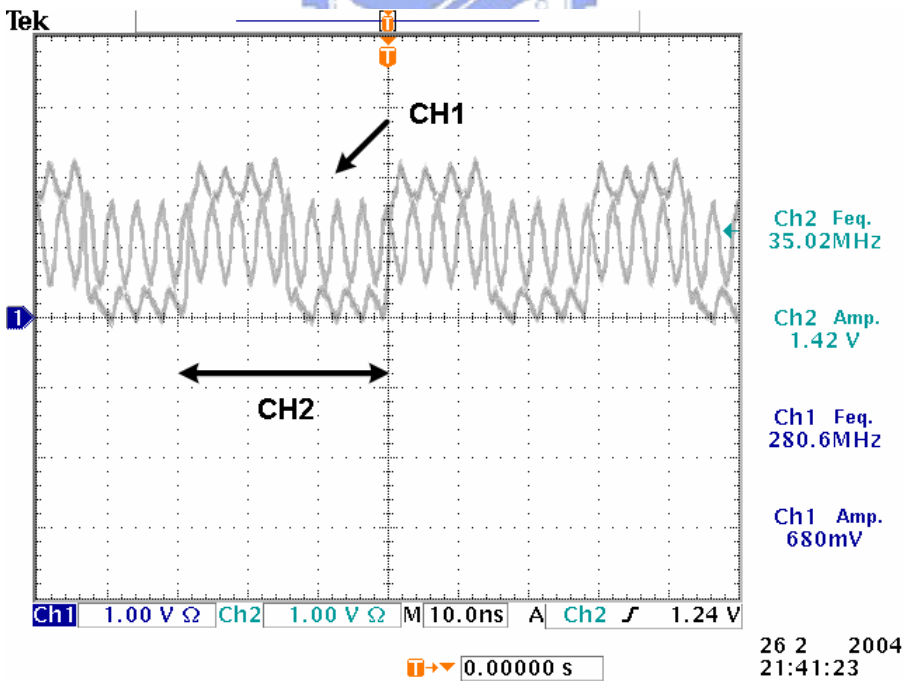


Fig. 3.31 Ch1 is the measured signal of the VCO output (280 MHz) and Ch2 is the measured signal of the divider output (35 MHz).

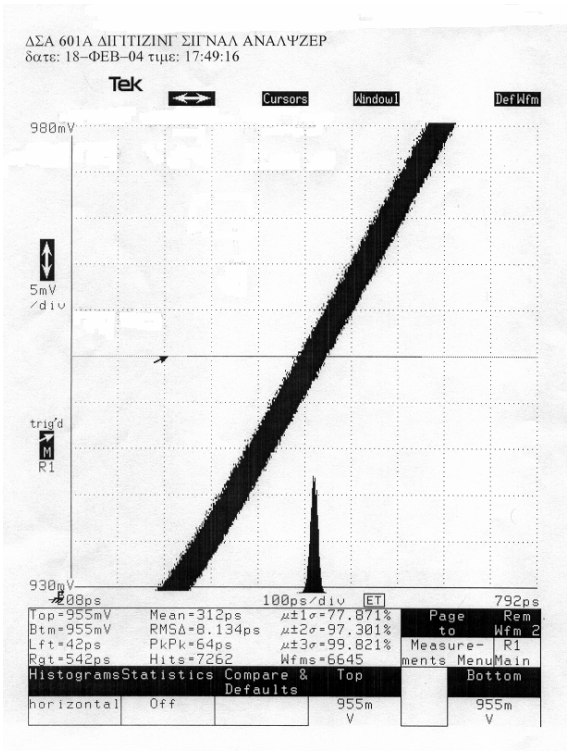


Fig. 3.32 The jitter histogram of the divider output signal at 25 MHz.

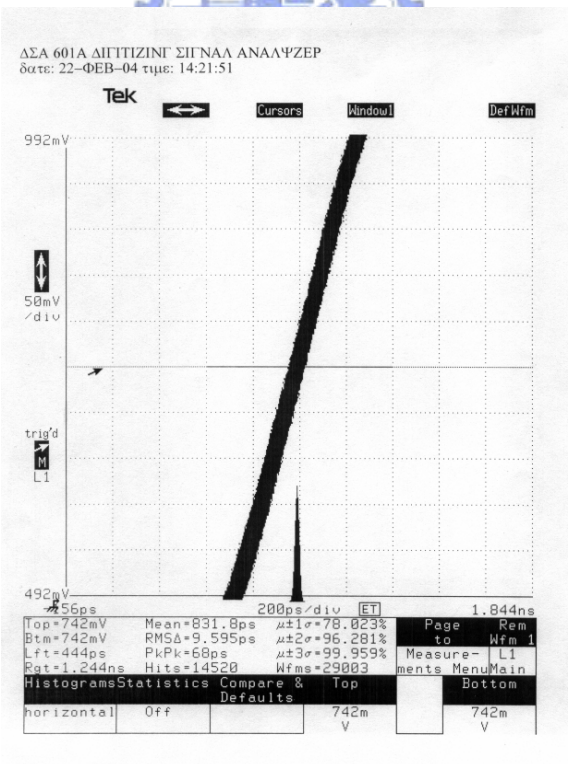


Fig. 3.33 The jitter histogram of the VCO output signal at 200 MHz.

Chapter 4
High-Speed I/O Interface Circuits

4.1 INTRODUCTION

In today's information-hungry society, how to speed up transmitting data over several inches even meters between computers or information electrical machines is more and more important. The data rate of transceiver is highly dependent on the I/O interface circuit of transceiver and the cable length. For many digital systems, the major performance limiting factor is the interconnection bandwidth between chips to chips or chips to boards. As process technologies continue to scale down, the on-chip data rate moves faster than the off-chip data rate and the interface between systems will become an even more significant bottleneck. Therefore, how to design high-speed I/O interface circuits is an important issue [15]. Besides, as the data rate of system is up to several gigabits-per-second range nowadays, the power consumption is another important issue. The design of high speed I/O interface circuits has led to concern on how to increase performance, decrease power consumption, reduce cost and mitigate noise or EMI. However, the above four factors are trade off to each other. Four I/O interface circuits are going to be discussed in the following sections.

4.2 TAPER BUFFER

4.2.1 Basic Concept

The simplest circuit design of the I/O interface circuit is the taper buffer. The

taper buffer has several inverters which are connected one after another. It can receive data came from an internal system and transmit it over a connecting medium toward a receiver. The optimal scaling factor between those connected inverters is u_{opt} (u_{opt} = e = 2.7182) which can achieve the minimum delay when driving different off-chip capacitance. Fig. 4.1 shows the schematic of the taper buffer, u is the scaling factor, C_{IN}, C_1 and C_2 are the internal parasitic capacitances and C_L is the off-chip capacitance.

4.2.2 Measurement Result

Fig. 4.2 shows the circuit design of the taper buffer. There are four inverters connected together. Fig. 4.3 shows the die photo of the taper buffer which is fabricated in a 0.25-μm 1P5M CMOS process with the 2.5 V power supply. The measurement setup of the taper buffer is shown in Fig. 4.4. The pulse generator (HEWLETT PACKARD 8133A) is utilized to generate the input signal of the taper buffer and the oscilloscope (Tektronix TDS 3054B) is used to obverse the taper buffer output signal. Figs. 4.5, 4.6 and 4.7 show the output signal of the taper buffer at 120 MHz, 200MHz and 280 MHz with the 13 pF capacitive loading at the oscilloscope. According to the measured output signals, the signal amplitude degrades as the operation frequency increases. Besides, the square waveform of the output signal becomes sinusoidal as the operation frequency increases which means that the taper buffer can not be operated at high data rate.

4.2.3 Conclusion

The taper buffer is the simplest design of the I/O interface circuit. However, it has many disadvantages. Due to the single-ended and full swing characteristics, the taper buffer is vulnerable to noise and has lower data rate (about less than 200 Mb/s)

with huge power consumption. Other I/O interface circuits should be utilized instead of taper buffers in order to have better qualities of data transmission in the high speed data link era.

4.3 LVDS OUTPUT BUFFER

4.3.1 Basic Concept

Low voltage differential signaling (LVDS) is one kind of high-speed I/O interface technologies which is already discussed in the chapter 2 of this thesis. It can transmit data with high speed and low power consumption. The circuit implementation of the designed LVDS output buffer is shown in Fig. 4.8 [16], [17]. It behaves as a current source with switched polarity. The output current flows through the load resistance, establishing the correct differential output voltage swing (350 mV typically). It uses the typical configurations with four MOS switches in bridge configuration (M1 - M4), with M1 and M3 switched on, the polarity of the output current is positive together with the differential output voltage. On the contrary, if M2 and M4 are switched on, the polarity of the output current and voltage is reversed. Since the proposed output buffer is intended for operation in the gigabits-per-second range, the double termination scheme is used and the termination resistors are integrated in the output buffer (R_{T-T}) and in the receiver input buffer (R_{T-R}) [18], [19]. With a nominal 100 Ω load at the front end of the receiver input buffer, both the common-mode voltage and the differential voltage swing at the output should fall within the LVDS standard specifications over the full range of process, supply voltage and temperature variations. Since this design aims at minimizing the PCB complexity and the production costs, external components and voltage references should be avoided together with wafer-level trimming. In order to define the correct output

levels, a simple low-power common-mode feedback control circuit is implemented in the output buffer as shown in Fig. 4.8. The common-mode output voltage is sensed by means of a high resistive divider (R_A and R_B) and compared with a 1.25 V reference voltage by the differential amplifier M5 - M8. The fraction of the tail current I_T flowing across M7 and M8 is mirrored to M_U and M_L, respectively, thus forcing V_{CM} = 1.25 V. In order to develop the correct voltage swing on the 50 Ω load resistance ($R_{T\text{-}T}$ // $R_{T\text{-}R}$), the bridge must be biased at $I_{OUT} = V_{OD\ nom}$ / 50 Ω. To this aim, I_T is set equal to I_{OUT} / K, where K is the gain of current mirrors M8 - M_L and M7 - M_U, a large gain was used in order to make negligible the power consumption of the common-mode feedback circuit. A large stability margin over PVT variations is achieved for the common-mode feedback circuit by means of a pole-zero compensation network, R_C - C_C.

4.3.2 Measurement Result

Fig. 4.3 shows the die photo of the LVDS output buffer which is fabricated in a 0.25-μm 1P5M CMOS process with the 2.5 V power supply. The chip area of the LVDS output buffer is 230 μm × 400 μm. The measurement setup of the LVDS output buffer is shown in Fig. 4.9. The pulse generator (HEWLETT PACKARD 8133A) is utilized to generate the input differential signal of the LVDS output buffer and the oscilloscope (Tektronix TDS 754D) is used to obverse the differential output signals. The external trigger source is employed to make the eye diagram of the differential output signal and the external resistor ($R_{T\text{-}R}$) is utilized to be the resistor which is integrated in the front end of the receiver input buffer. The other measurement setup which uses two coaxial cables as connecting media is shown in Fig. 4.10. Fig. 4.11 shows the characteristics of the 1-meter coaxial cable. It has little gain loss and 50-Ω intrinsic impedance as the transmission frequency is operated from 10 KHz up to 2

GHz. Since the coaxial cable has good transmission qualities, it will have little influence on the jitter performance of the LVDS output signals. Figs 4.12 and 4.13 show the measured eye diagrams at 840 Mb/s without and with coaxial cables. Figs 4.14 and 4.15 show the measured eye diagrams at 1.2 Gb/s without and with coaxial cables. The peak-to-peak jitter and worst case jitter of the eye diagram are measured in order to determine the quality of the transmitted output signal. As mentioned in the chapter 2, commonly 5 %, 10 %, or 20 % is acceptable with 20 % jitter usually being an upper practical limit. More than 20 % jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. The measured parameters of the output buffer at 840 Mb/s are summarized in Table 4.1.

4.3.3 Conclusion

As mentioned in the chapter 2, LVDS is one kind of I/O technologies, which is utilized to transmit data at very high data rate. It can eliminate trade off between speed, power consumption cost and noise with its low output voltage swing and differential transmission characteristics. It has variety applications, one of which is in the plat panel display system. In the following section, two new I/O buffers with both LVDS and RSDS technologies which are already discussed in the chapter 2 are proposed.

4.4 CO-DESIGNED I/O BUFFERS WITH BOTH LVDS AND RSDS STANDARDS

4.4.1 Basic Concept

Fig. 4.16 shows the proposed co-designed output buffer with both LVDS and RSDS standards. The output buffer is utilized to transmit preceding serialization

full-swing (3.3 V) data along transmission materials to the receiver with low output voltage swing, such as LVDS standard (+/- 350 mV) or RSDS standard (+/- 200 mV). The circuit block at the input (V_{IN}) of the co-designed output buffer is to convert single data to differential data. The detailed circuit implementation of the single-ended-to-differential conversion circuit is shown in Fig. 4.17, which is used to switch four MOS switches (the M1 - M4 in Fig. 4.16) in the bridge configuration. When a logical "1" (3.3 V) signal is arrived at the input of the output buffer, the node 1 and node 2 in Fig. 4.17 are charged to 3.3 V, and then node 3 is discharged to 0 V. This leads to the V_{OUTN} at logical "0" (0 V) and the V_{OUTP} at logical "1" (3.3 V). On the contrary, when input signal is logical "0" (0V), the circuit causes the V_{OUTP} at logical "0" (0 V) and V_{OUTN} at logical "1" (3.3 V). The core circuit of the output buffer, as shown in Fig. 4.16, is the four MOS switches, which are realized by the typical configuration of two current sources at the top and one current source at the bottom. The output buffer acts as a current source with switched polarity. The appropriate output current flows through the termination resistance in order to correctly establish the differential output voltage swings to meet the LVDS standard or RSDS standard. The polarity of the output current is positive together with the differential output voltage with M2 and M3 switched on, and the output current is negative together with the differential output voltage with M1 and M4 switched on. Since the data rate of this buffer is up to gigabits-per-second range, the mismatch of impedance between I/O interfaces may cause reflection of signal energy during data transmission which destroys signal quality. Therefore, double termination scheme is used in this co-designed output buffer to minimize signal reflection. However, double termination has the drawback of larger power consumption. The termination resistors of 100 Ω are integrated in the output of the transmitter (R_{TT}) and the input of the receiver (R_{TR}).

In order to strictly keep the output offset voltage within the voltage range that defined in LVDS and RSDS standards, a common-mode feedback circuit is used in the output buffer. The common-mode voltage is sensed by two high resistors R_{A1} - R_{B1} (R_{A1} = R_{B1} = 100 kΩ) and compared with a 1.25 V reference by the differential amplifier M8 - M13. Furthermore, the resistor R_{A2} of 20 kΩ is designed to reduce noise on the common- mode voltage (V_{CM}) that sensed by R_{A1} - R_{B1}. R_{B2} (20 kΩ) is added to balance the differential input pair, M8 - M9. A compensation network C_C - R_C (C_C = 6pF and R_C = 4 kΩ) is added in the loop of the common-mode feedback circuit to achieve good stability over PVT variations.

Two control pins, LR and EN, are used to determine the co-designed output buffer for applications in the LVDS standard, RSDS standard, or in the sleep mode. As shown in Fig. 4.16, when the LR is logical “1” (3.3 V) and the EN is logical “1” (3.3 V), two current mirror circuits provide appropriate current to M5 - M6 in order to establish the differential output voltage swing of LVDS standard. On the contrary, when the LR is logical “0” (0 V) and the EN is logical “1” (3.3 V), the right side current mirror circuit is turned off by M28 and the left side current mirror circuit provide current to M6, which establishes the voltage swing of RSDS standard at the output of the co-designed output buffer. The co-designed output buffer is in sleep mode when the EN is logical “0” (0 V) and the input of the co-designed output buffer is clamped to logical “1” (3.3 V), the two current mirrors are turned off by M28 - M29 with M22 - M27 to further avoid any possible current path except leakage current (measured under μA order). Fig. 4.18 shows the simulated both LVDS standard (top) and RSDS standard (bottom) output differential signals, which are transmitted at 1.2 Gb/s over two 1.44-mm-width, 3-cm-long 50-Ω micro-stripe lines. The thickness of printed circuit board (PCB) is 0.6-mm and the dielectric constant of the PCB is 4.5 to realize such 50 Ω micro-stripe lines. The simulation includes the package model (DIP

28-pin) with parasitic RLC and a 10-pF capacitive loading at differential outputs.

Fig. 4.19 shows the co-designed receiver input buffer with both LVDS and RSDS standards. The input buffer is designed to correctly sense an incoming low-voltage differential signal and convert it to a single-ended full-swing (3.3 V) signal, which can be processed by following circuits. The NMOS differential pair (M1 - M2) is used to sense an incoming low-voltage differential signal of both LVDS and RSDS standards. However, M3 - M4 is a positive feedback circuit which can quickly obtain a larger differential voltage swing at node 1 and node 2. The circuit at the top in Fig. 4.19 is a differential-to-single-ended converter, which can further amplify the differential signal between node 1 and node 2 in Fig. 4.19 and convert it to a single-ended full-swing signal with 50 % duty cycle. The input buffer is in sleep mode when the control pin EN is logical "0" (0 V), and the output of the input buffer is clamped to logical "0" (0 V) by M5. The simulated waveforms are shown in Fig. 4.20, where the dotted line is a differential input pattern provided to the input buffer under the worst case condition (V_{OD} = ± 100 mV). However, the solid line is an output pattern, which can be recovered to a single-ended full-swing (3.3 V) pattern in order to be processed by the following circuits. Both input and output patterns in Fig. 4.20 are simulated with the operating speed of 1.2 Gb/s. Fig. 4.21 is the AC response of the input buffer. It shows that the DC gain of the input buffer is still enough (more than 24.3 dB) at the desired operation data rate (1.2 Gb/s).

4.4.2 Measurement Result

Fig. 4.22 shows the die photo of the I/O buffers which are fabricated in a 0.25-μm 1P5M CMOS process with the 3.3 V power supply. The chip area of the co-designed output buffer is 220 μm × 350 μm and the chip area of the co-designed input buffer is 100 μm × 240 μm. The measurement setup of the co-designed output

buffer is shown in Fig. 4.9 except that the differential input is changed to the single input. The measurement setup of the co-designed input buffer is also shown in Fig. 4.9 except that the differential output is changed to the single output. The measurement setup that connects the co-designed output buffer and input buffer is shown in Fig. 4.23. Fig. 4.24 shows the measured LVDS eye diagram of the co-designed output buffer at 840 Mb/s when the control pin LR is switched to logical "1" (3.3 V). Fig. 4.25 shows the measured RSDS eye diagram of the co-designed output buffer at 840 Mb/s when the control pin LR is switched to logical "0" (0 V). Figs. 4.26 and 4.27 show the measured LVDS and RSDS eye diagram of the co-designed output buffer at 1.2 Gb/s when the control pin LR is switched to logical "1" (3.3 V) and logical "0" (0 V). The co-designed output buffer is in sleep mode when the control pin EN is logical "0" (0 V) and the measured current consumption is under μA range with the input of the co-designed output buffer is clamped to logical "1" (3.3 V). Fig. 4.28 shows the measured output signal of the receiver input buffer at 400 MHz. The input differential signal is at the worst case (V_{OD} = ± 100 mV) defined in LVDS and RSDS standards and the output signal is a single-ended full-swing signal with 50 % duty cycle. Fig. 4.29 shows the measured eye diagram of the receiver input buffer at 400 Mb/s. Fig. 4.30 shows the measured output signal of the receiver input buffer at 600 MHz. Fig. 4.31 shows the measured eye diagram of the receiver input buffer at 600 Mb/s. Fig. 4.32 shows the measured output signal of the receiver input buffer at 840 MHz. Fig. 4.33 shows the measured eye diagram of the receiver input buffer at 840 Mb/s. Fig. 4.34 shows the measured output signal of the receiver input buffer at 1.2 GHz. Due to the capacitive loading of the oscilloscope the output signal voltage swing shrinks as the operation frequency rises. The output signal is clamped to logical "0" (0 V) when the control pin EN is switched to logical "0" (0 V) and the current consumption is measured under μA range. Figs. 4.35, 4.36 and 4.37 show the

measured eye diagram of the I/O buffers which are connected together via two coaxial cables at 300 Mb/s, 400 Mb/s and 600 Mb/s. The measured parameters of the I/O buffers are summarized in Table 4.2.

4.4.3 Conclusion

The co-designed I/O buffers with both LVDS and RSDS standards can be operated at very high speed. They also have variety applications one of which is in the flat panel display systems. The eye diagram which is at 840 Mb/s can support the SXGA (1280 × 1024 pixels) resolution of the flat panel displays and the eye diagram which is at 1.2 Gb/s can support the UXGA (1600 × 1200 pixels) resolution of the flat panel displays. These co-designed I/O buffers can be used in the transmitter which is utilized in the flat panel display systems will be discussed in the later chapter.

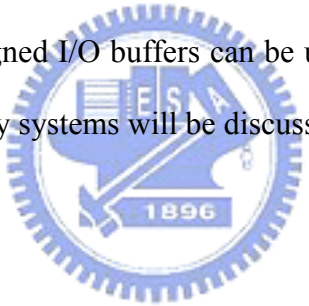


Table 4.1

The measured parameters of the LVDS output buffer.

Function	LVDS Output Buffer
Operate Voltage	2.5 V
Current Consumption	17.2 mA@840 Mb/s
Power Consumption	43 mW@840 Mb/s
Data Rate	Target at 840 Mb/s (Measured up to 1.2 Gb/s)
Technology	VIS 0.25-μm 1P5M CMOS

Table 4.2

The measured parameters of the co-designed I/O buffers.

Function	Co-Designed Output Buffer
Operate Voltage	3.3 V
Data Rate	Measured up to 1.2 Gb/s
Power Consumption LR = 3.3 V, EN = 3.3 V → LVDS LR = 0 V, EN = 3.3 V → RSDS	42 mW@840 Mb/s LVDS 28 mW@840 Mb/s RSDS 44 mW@1.2 Gb/s LVDS 30 mW@1.2 Gb/s RSDS
Sleep Mode EN = 0 V, LR = 0 V or 3.3 V	Measured current consumption is under μA range
Technology	VIS 0.25-μm 1P5M CMOS
Function	Co-Designed Input Buffer
Operate Voltage	3.3 V
Data Rate	Measured up to 1.2 GHz
Power Consumption	120.6 mW@840 Mb/s
Technology	VIS 0.25-μm 1P5M CMOS
Sleep Mode EN = 0 V, RL = 0 V or 3.3 V	Measured current consumption is under μA range

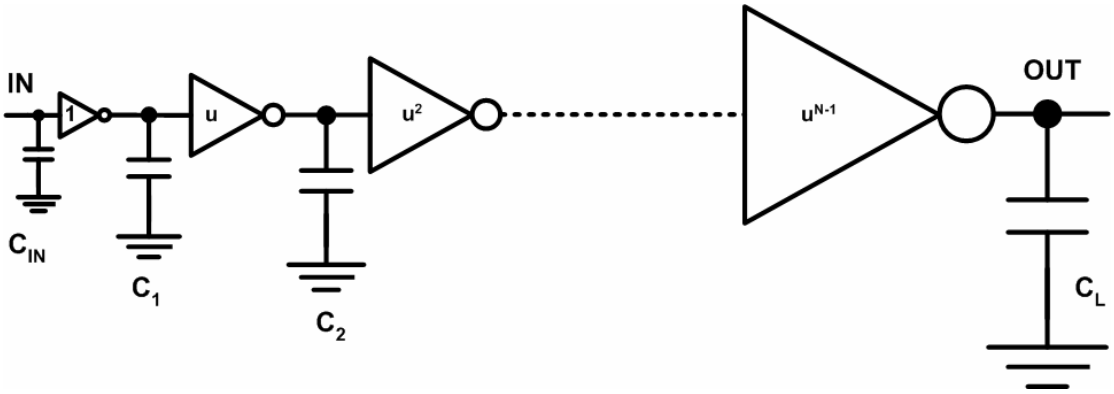


Fig. 4.1 Schematic of the taper buffer.

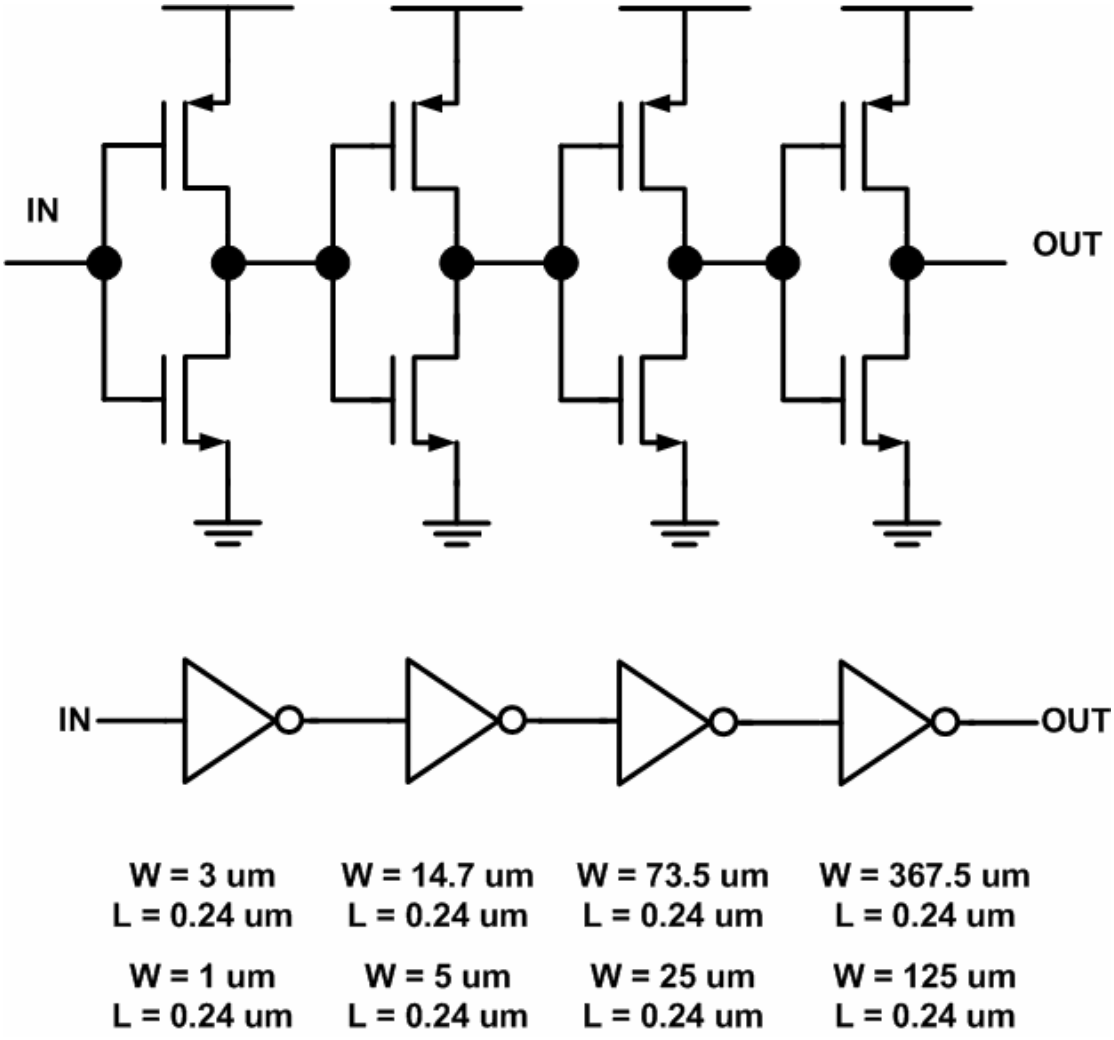


Fig. 4.2 The circuit design of the taper buffer.

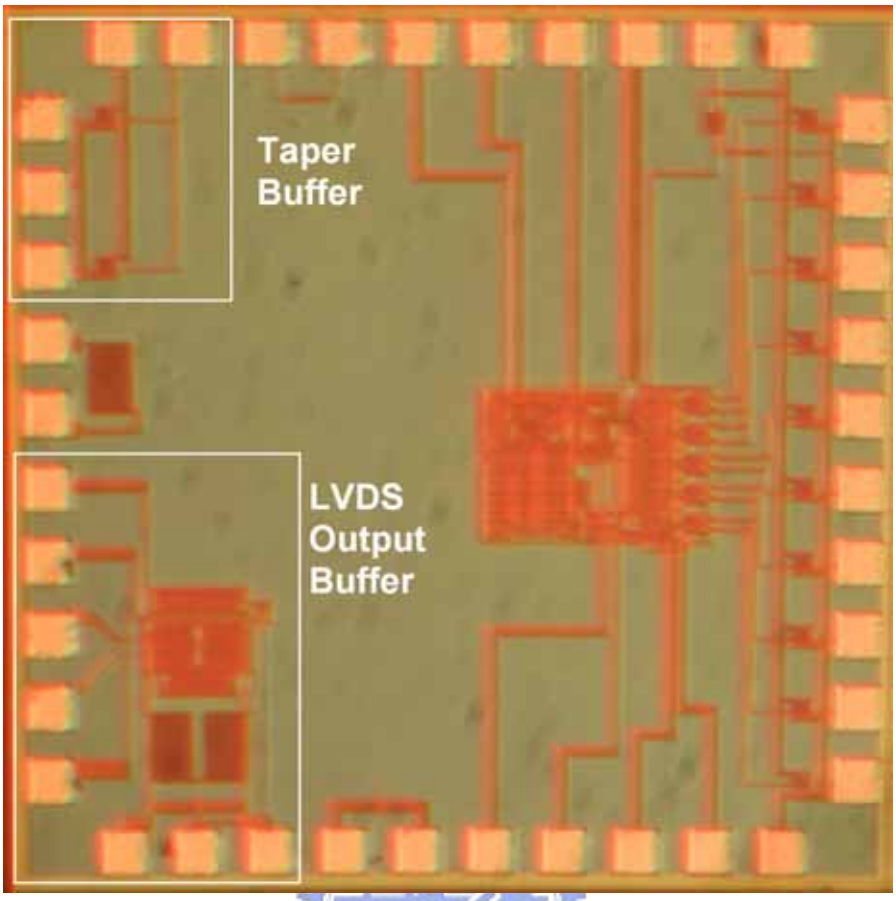


Fig. 4.3 The die photo of the taper buffer and the LVDS output buffer.

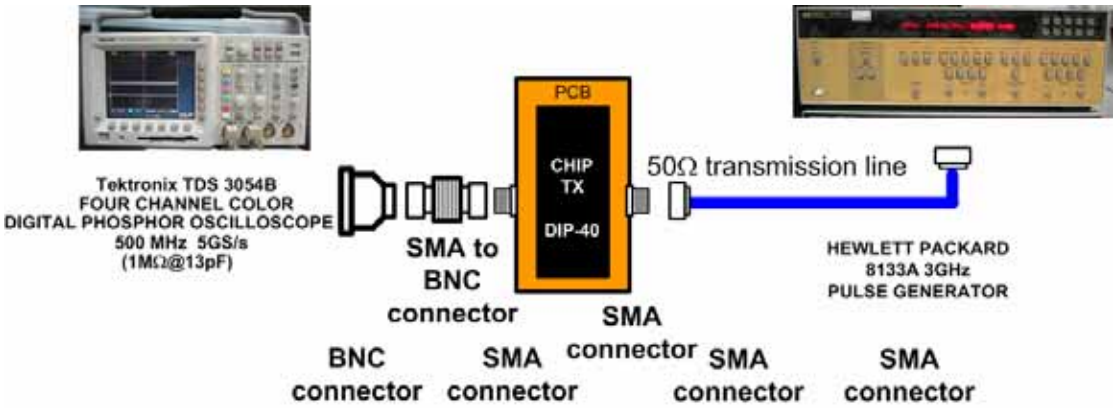


Fig. 4.4 The measurement setup of the taper buffer.

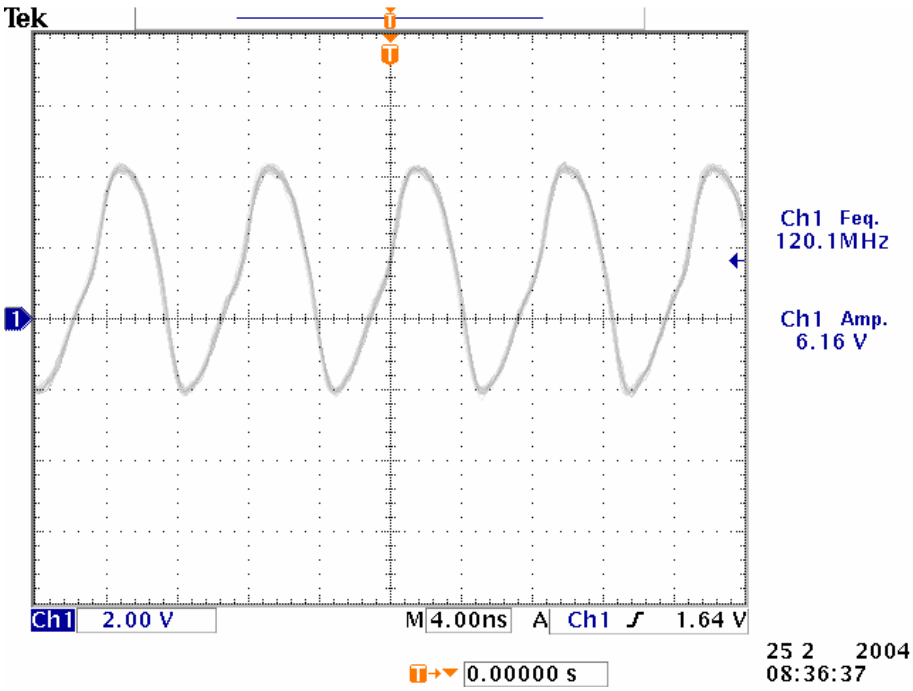


Fig. 4.5 The output signal of the taper buffer at 120 MHz. The capacitive loading of the oscilloscope is 13 pF (@1 MΩ).

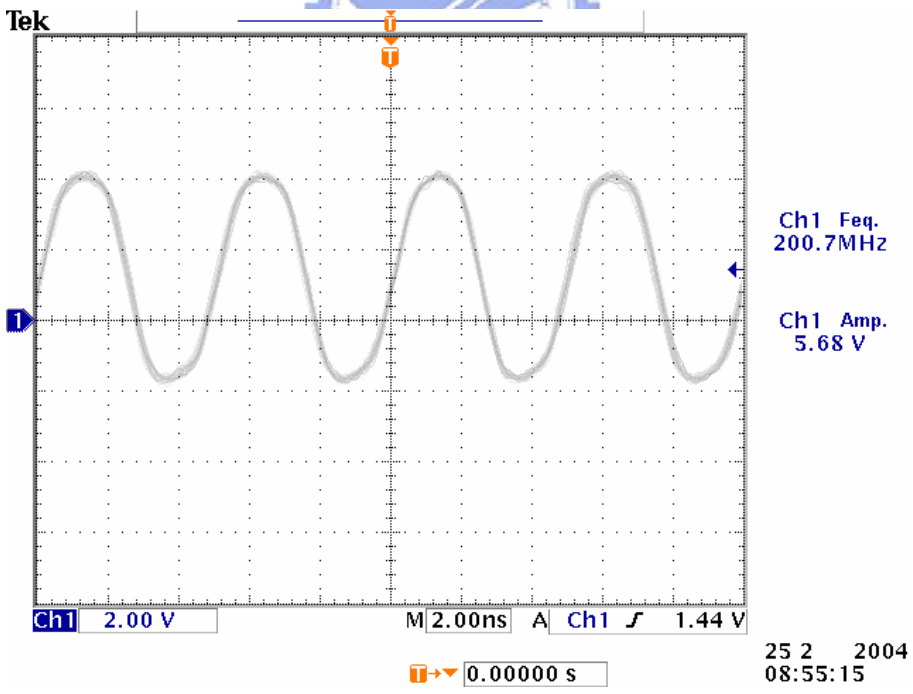


Fig. 4.6 The output signal of the taper buffer at 200 MHz. The capacitive loading of the oscilloscope is 13 pF (@1 MΩ).

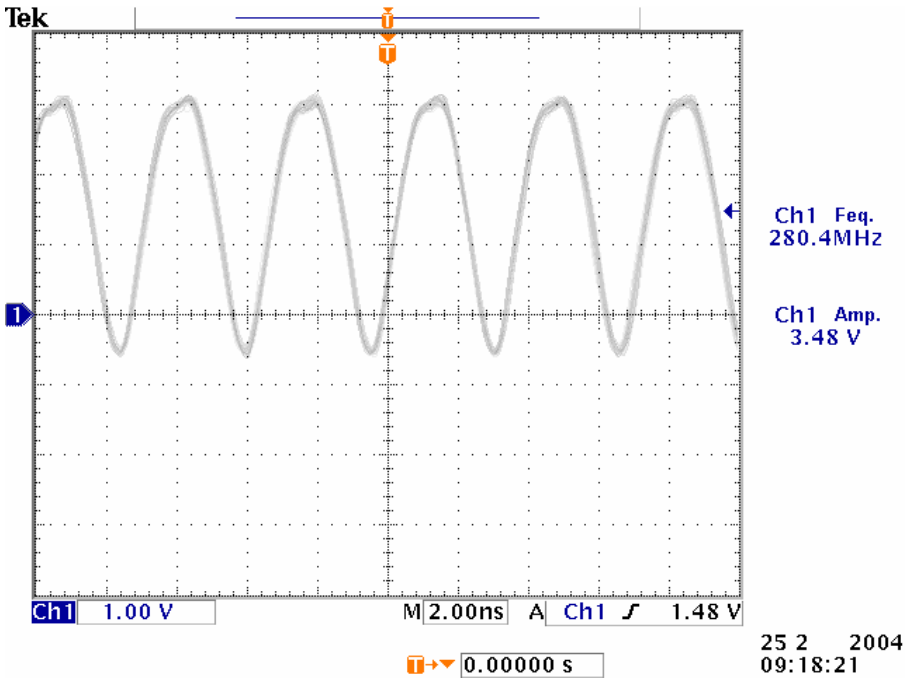


Fig. 4.7 The output signal of the taper buffer at 280 MHz. The capacitive loading of the oscilloscope is 13 pF (@1 MΩ).

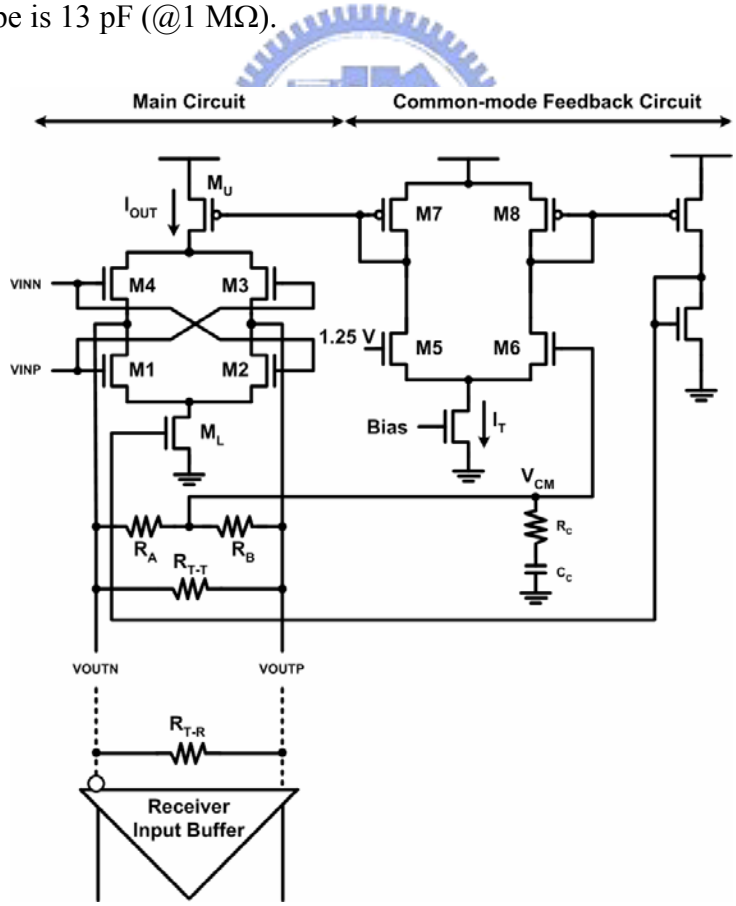


Fig. 4.8 Schematic diagram of the LVDS output buffer.

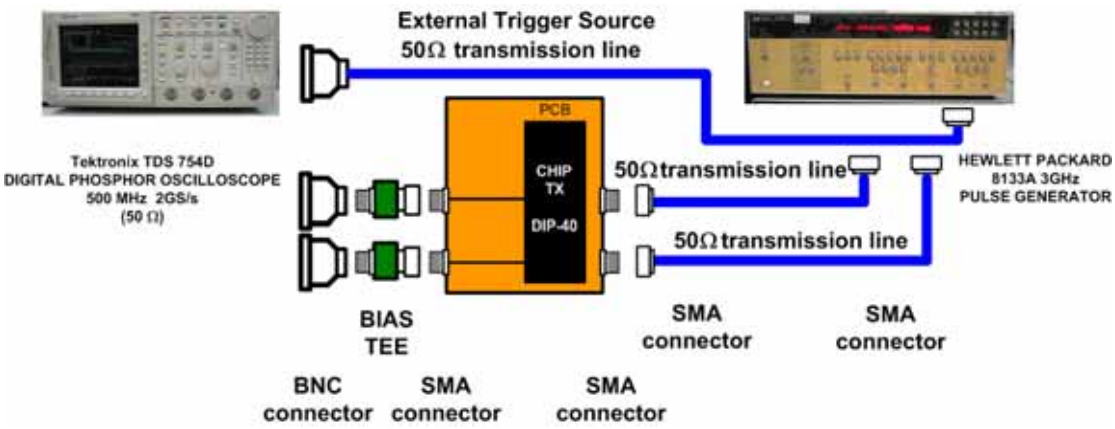


Fig. 4.9 The measurement setup of the LVDS output buffer.

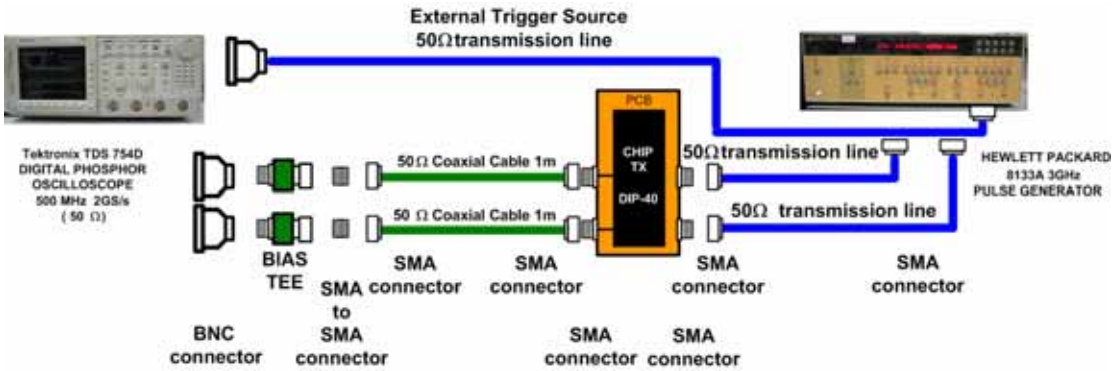


Fig. 4.10 The measurement setup of the LVDS output buffer which uses two coaxial cables.

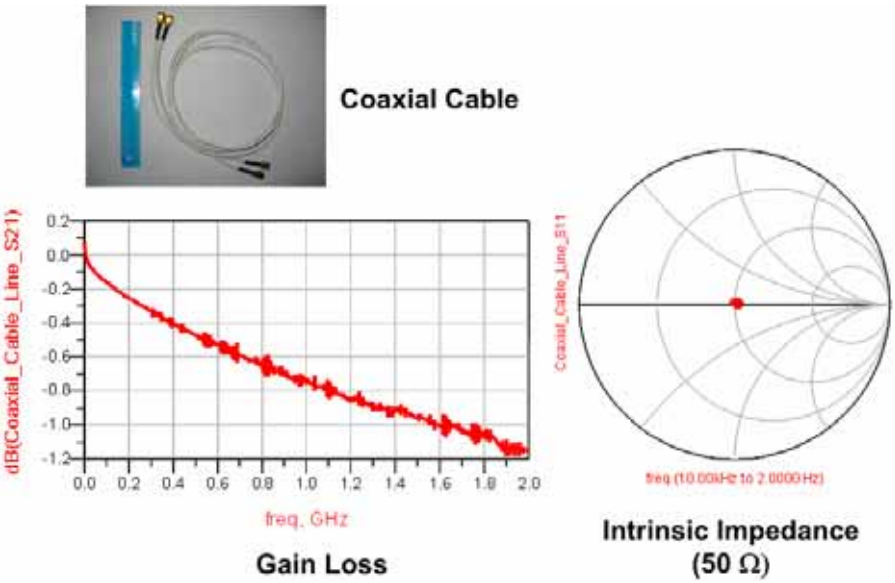


Fig. 4.11 Measurement of the coaxial cable.

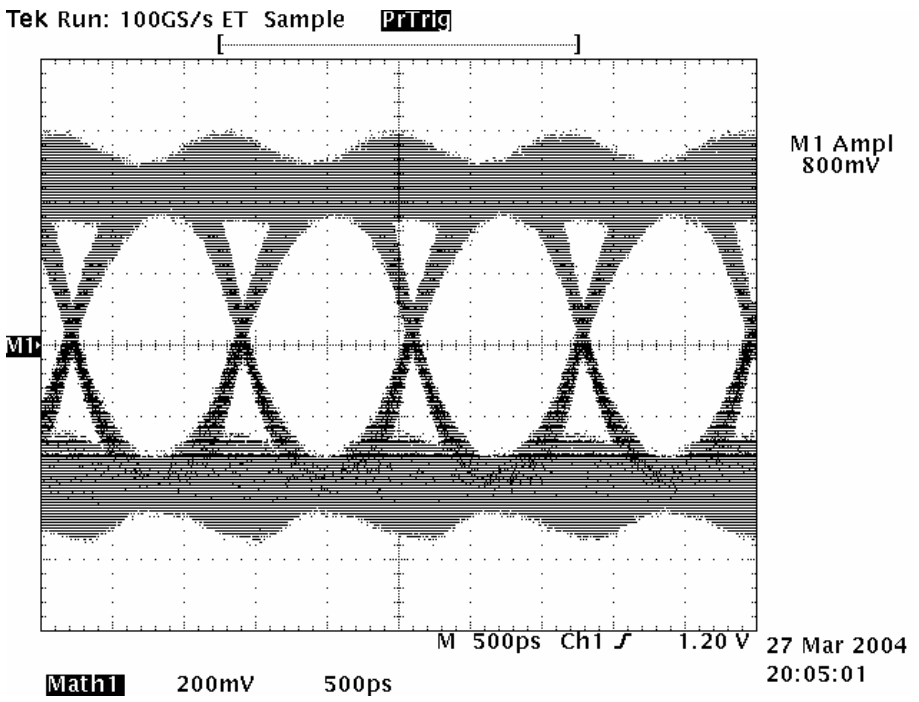


Fig. 4.12 The measured eye diagram of the output buffer at 840 Mb/s without coaxial cables. The peak-to-peak jitter is 9.19 % and the worst case jitter is 17 %.

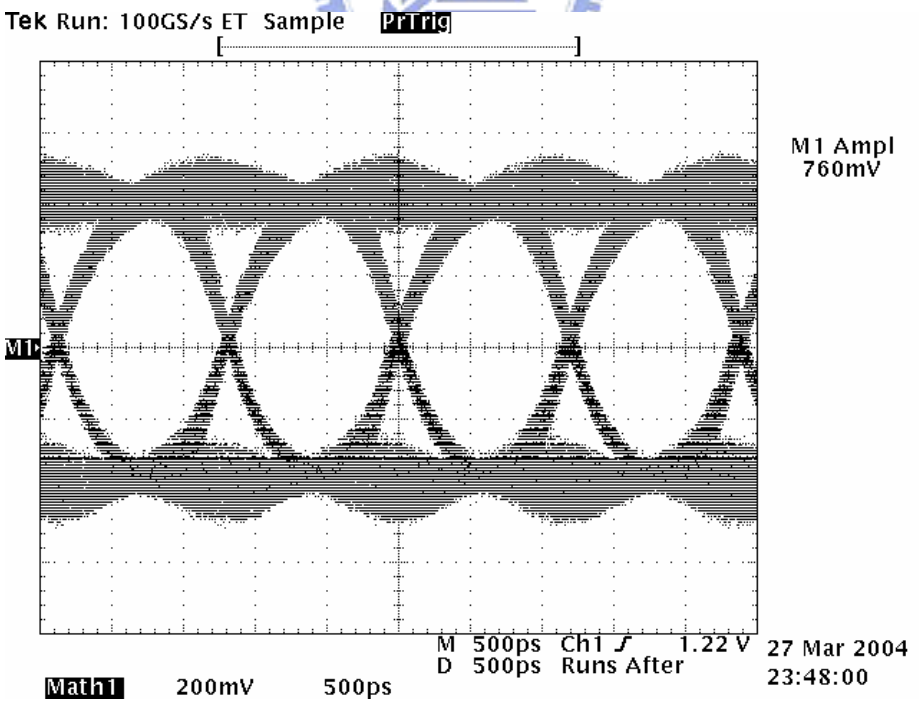


Fig. 4.13 The measured eye diagram of the output buffer at 840 Mb/s with coaxial cables. The peak-to-peak jitter is 10.5 % and the worst case jitter is 21.5 %.

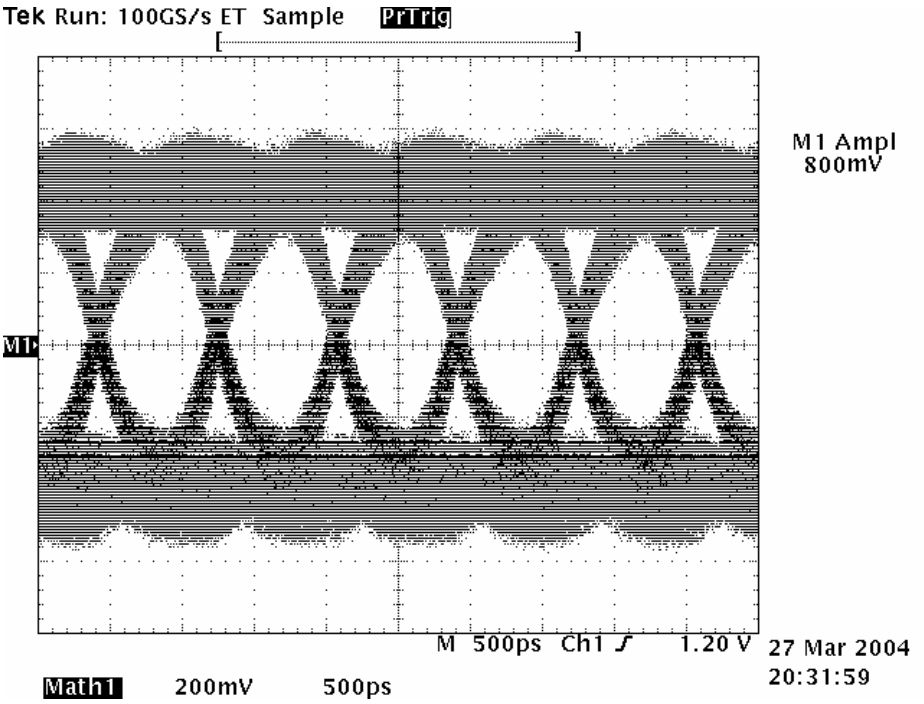


Fig. 4.14 The measured eye diagram of the output buffer at 1.2 Gb/s without coaxial cables. The peak-to-peak jitter is 18.75 % and the worst case jitter is 30 %.

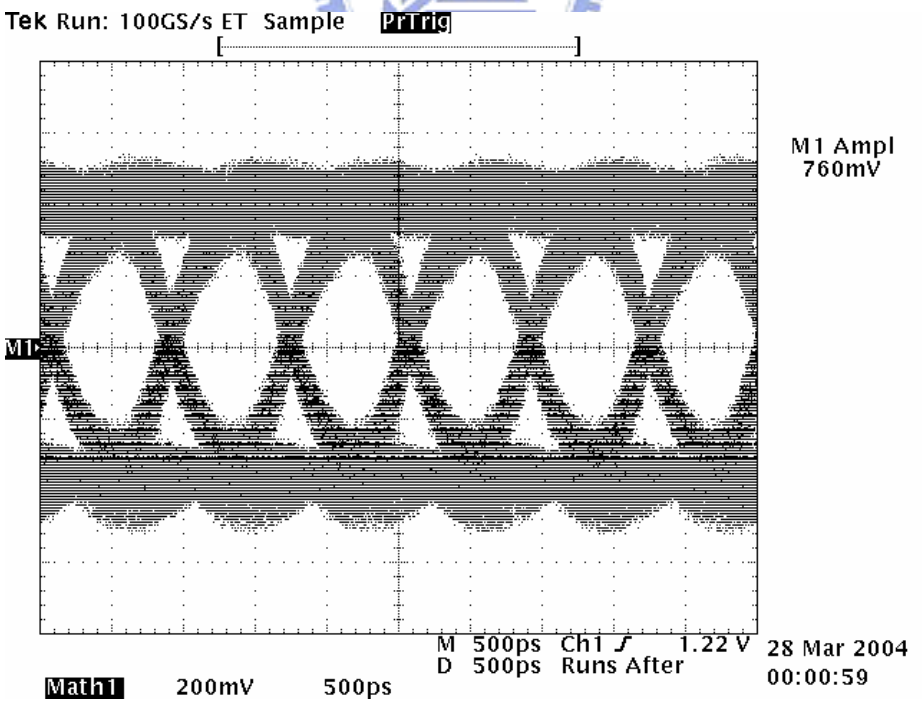


Fig. 4.15 The measured eye diagram of the output buffer at 1.2 Gb/s with coaxial cables. The peak-to-peak jitter is 23.25 % and the worst case jitter is 35.6 %.

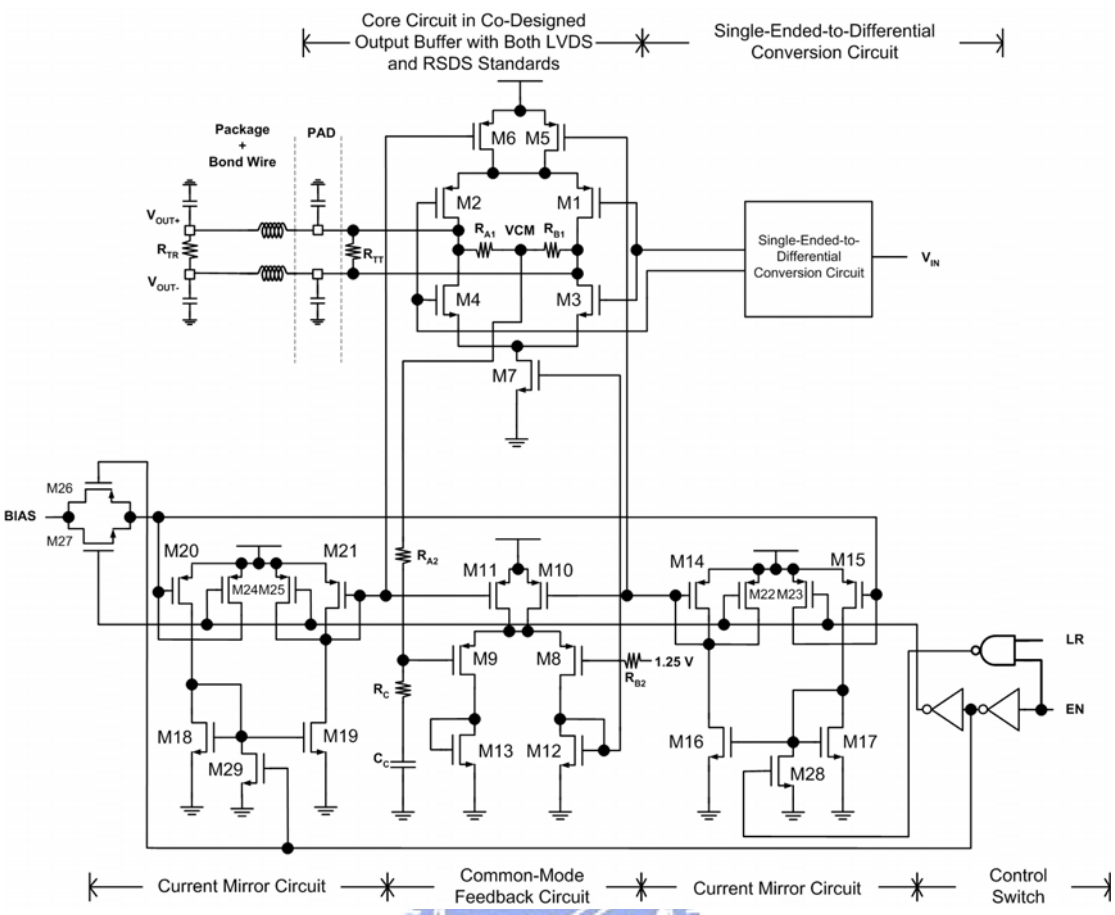


Fig. 4.16 Schematic diagram of the co-designed output buffer with both LVDS and RSDS standards.

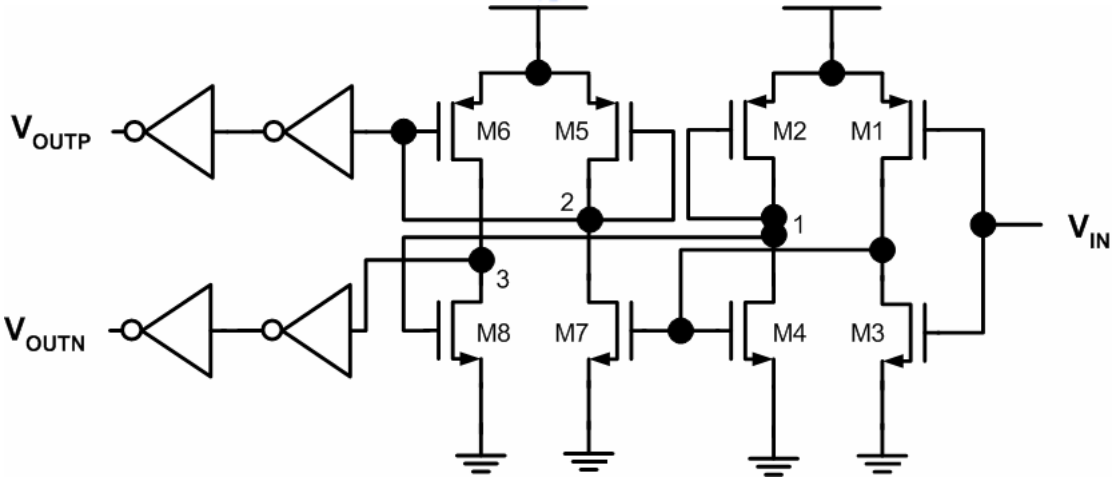


Fig. 4.17 The circuit implementation for the single-ended-to-differential conversion circuit.

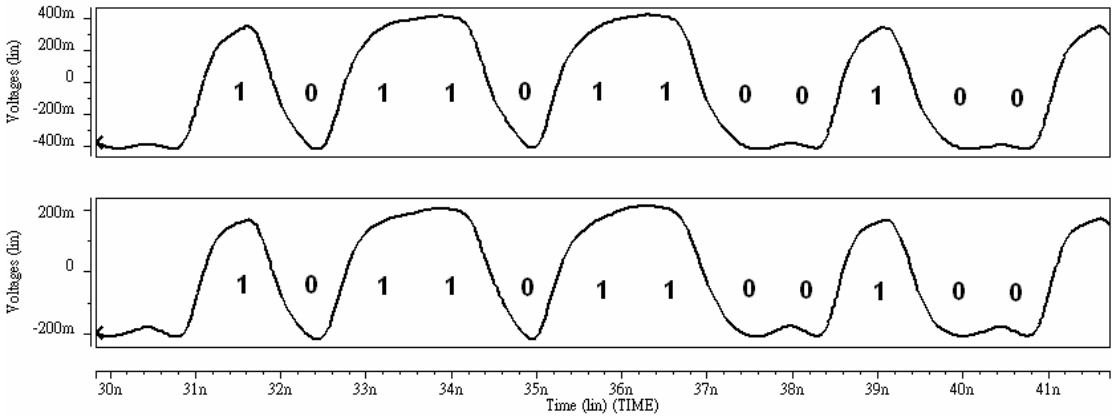


Fig. 4.18 Simulation of both LVDS standard (top) and RSDS standard (bottom) output voltage swings with a 101101100100 input pattern transmitted at 1.2 Gb/s.

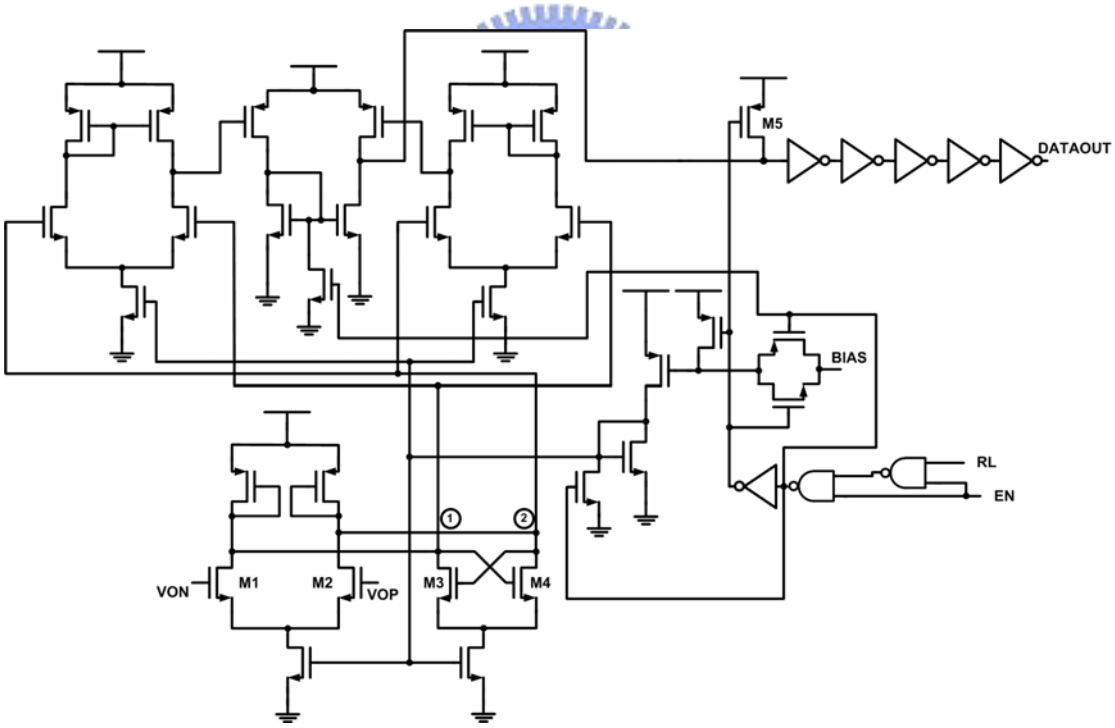


Fig. 4.19 Schematic diagram of the co-designed receiver input buffer with both LVDS and RSDS standards.

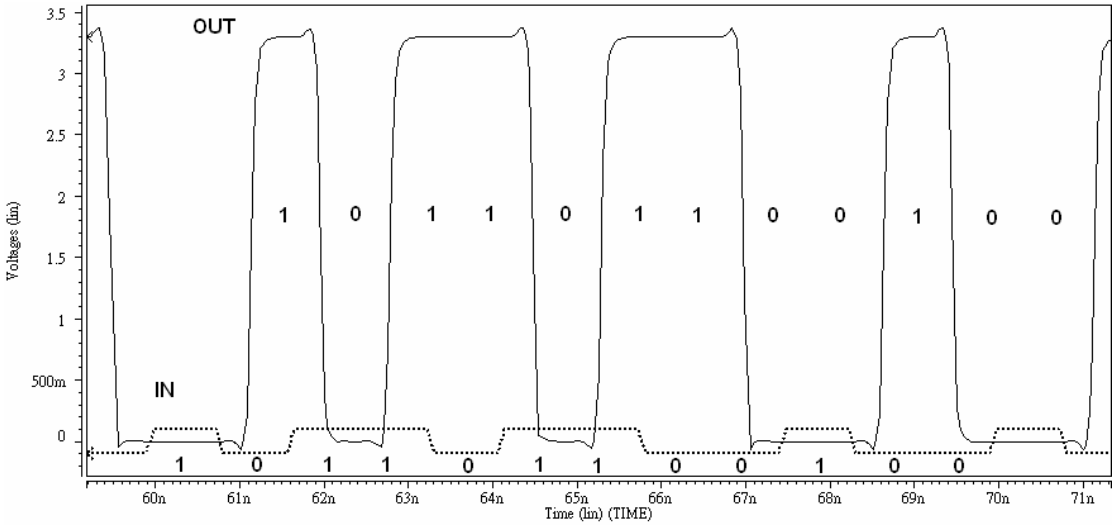


Fig. 4.20 Simulation of the co-designed receiver input buffer at 1.2 Gb/s. The dotted line is a 101101100100 differential input pattern provided to the input buffer. The solid line is a recovered single full-swing output pattern.

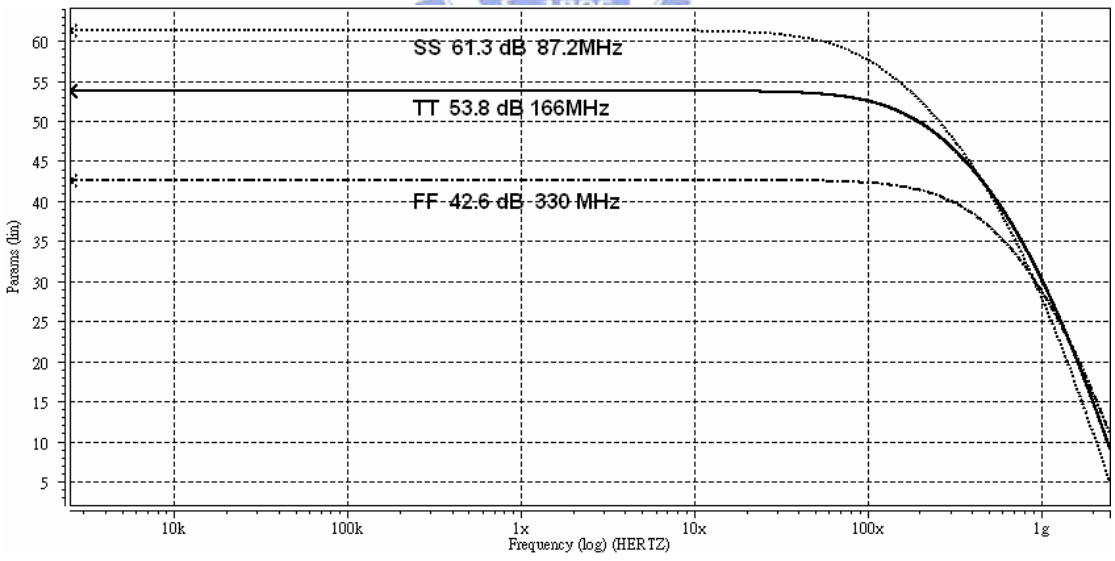


Fig. 4.21 AC response of the receiver input buffer.

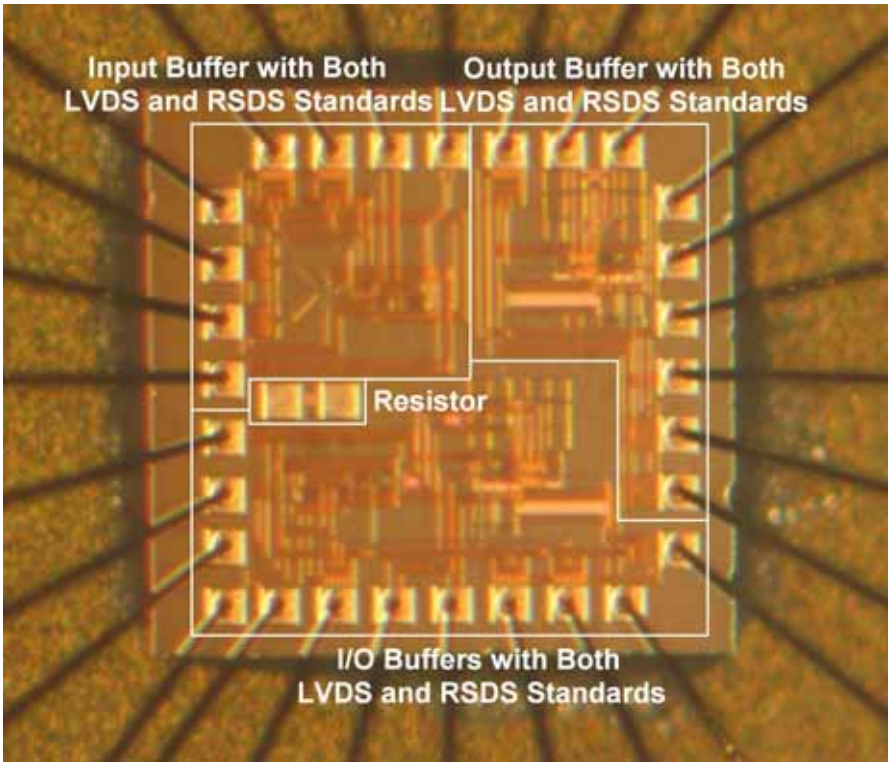


Fig. 4.22 The die photo of the co-designed I/O buffers.

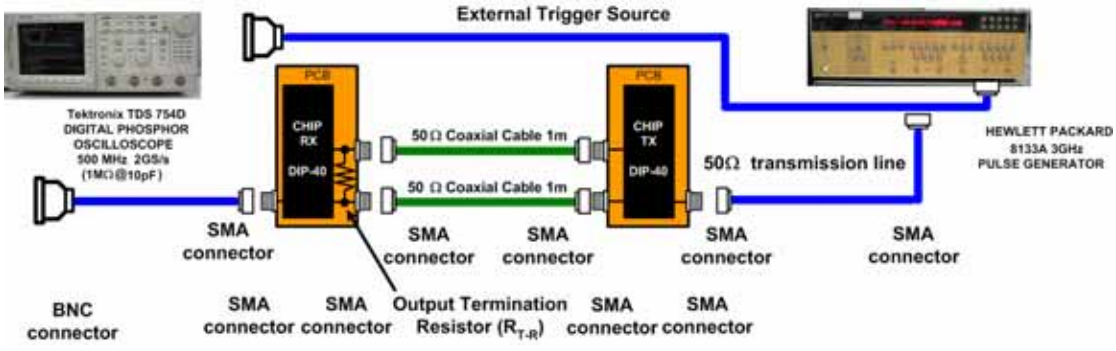


Fig. 4.23 The measurement setup of the co-designed I/O buffers.

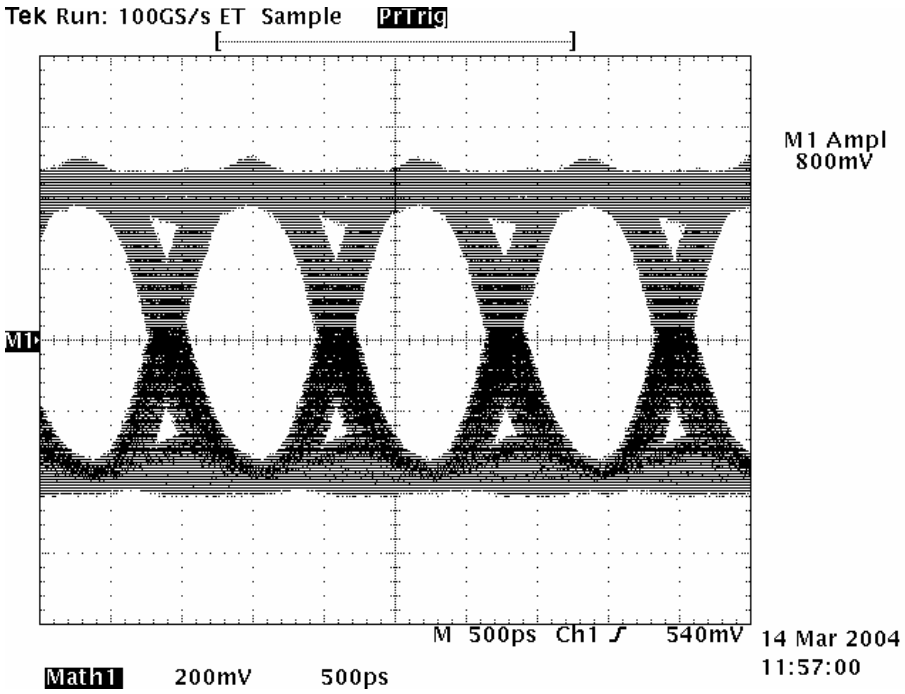


Fig. 4.24 The measured eye diagram of the output buffer operating in the LVDS standard at 840 Mbps with 2^{23}-1 PRBS. The measured power consumption is 42 mW. The peak-to-peak jitter is 23.6 %.

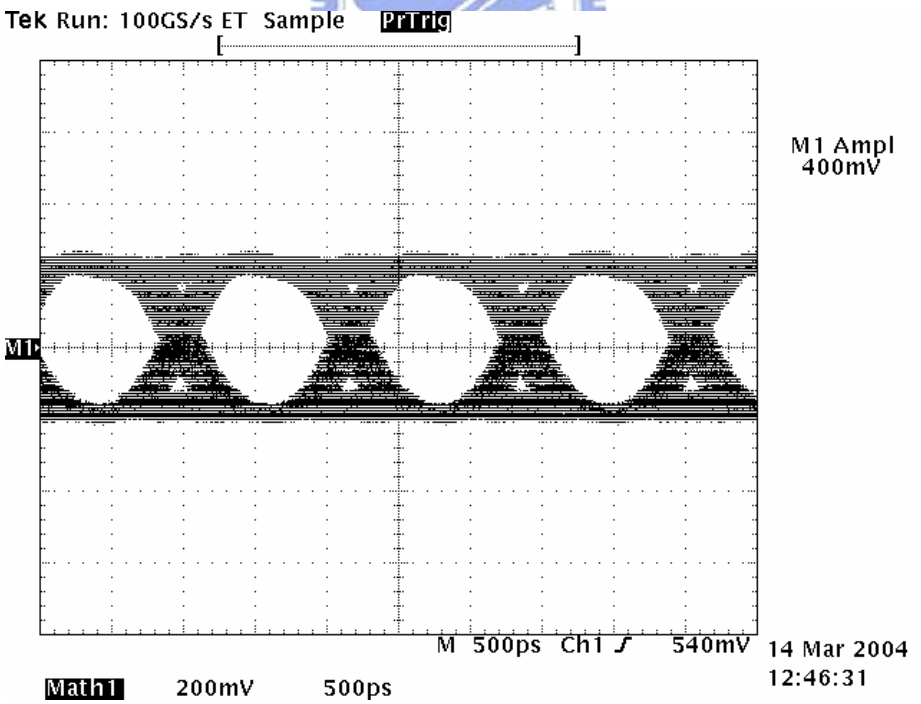


Fig. 4.25 The measured eye diagram of the output buffer operating in the RSDS standard at 840 Mbps with 2^{23}-1 PRBS. The measured power consumption is 28 mW. The peak-to-peak jitter is 26.26 %.

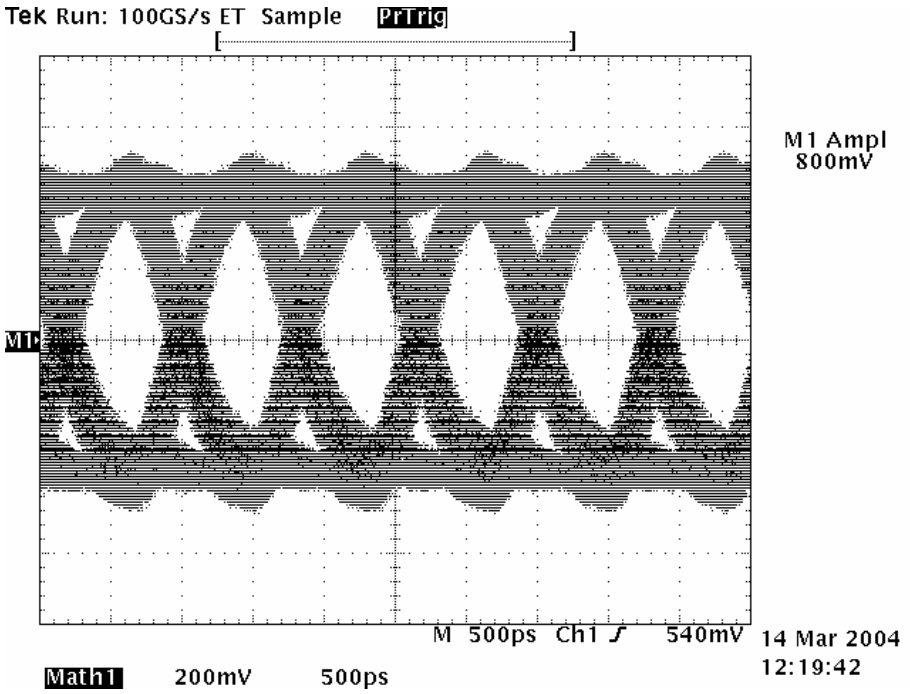


Fig. 4.26 The measured eye diagram of the output buffer operating in the LVDS standard at 1.2 Gbps with 2^{23}-1 PRBS. The measured power consumption is 44 mW. The peak-to-peak jitter is 33.75 %.

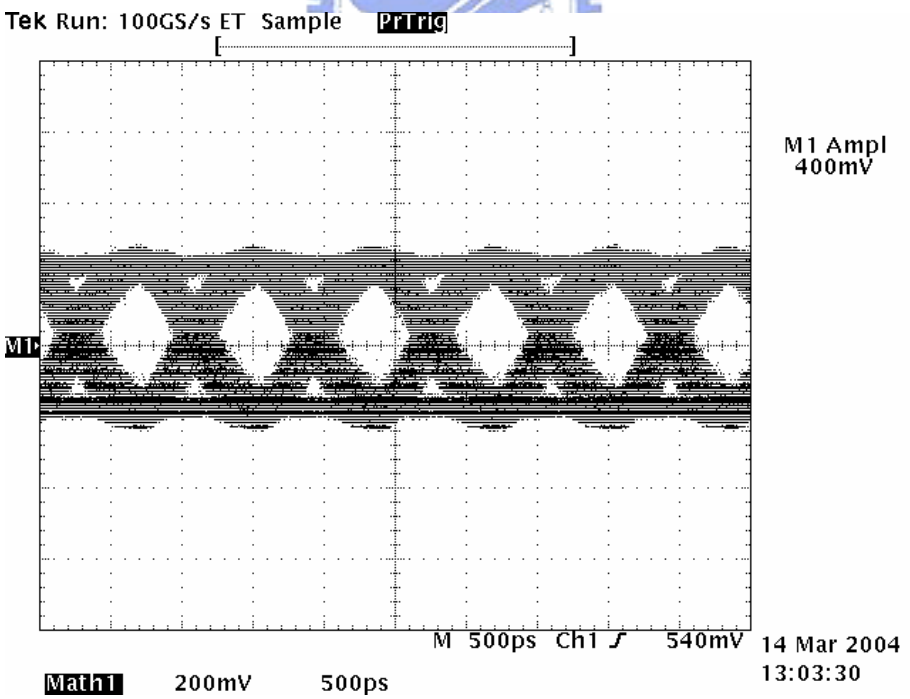


Fig. 4.27 The measured eye diagram of the output buffer operating in the RSDS standard at 1.2 Gbps with 2^{23}-1 PRBS. The measured power consumption is 30 mW. The peak-to-peak jitter is 37.5 %.

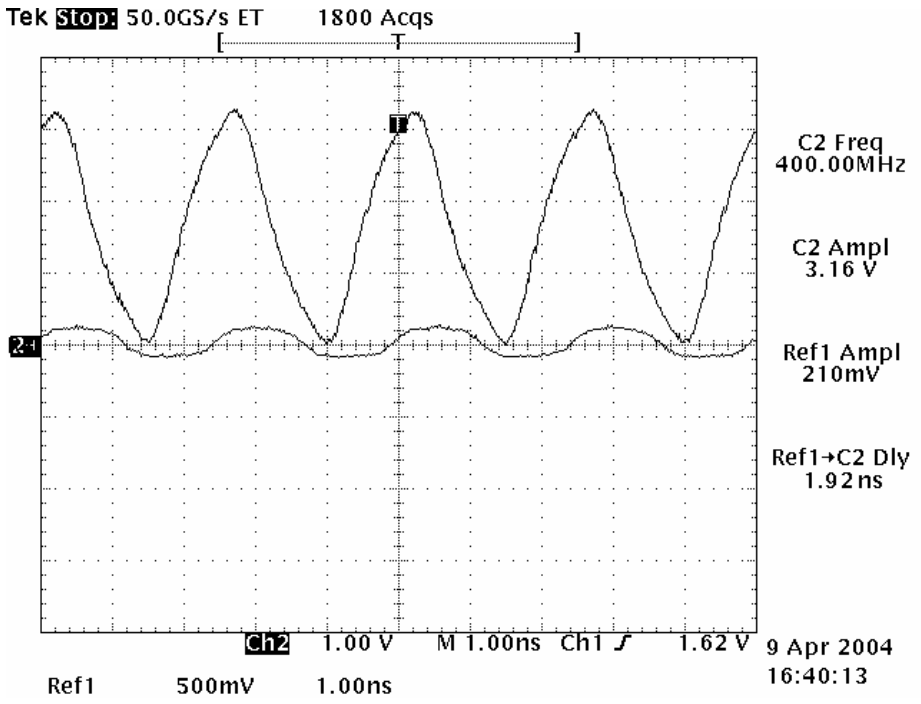


Fig. 4.28 The measured output signal of the receiver input buffer at 400 MHz. The output signal is a single-ended full-swing signal with 50 % duty cycle and the input differential signal is at the worst case (V_{OD} = ± 100 mV) defined in LVDS and RSDS standards.

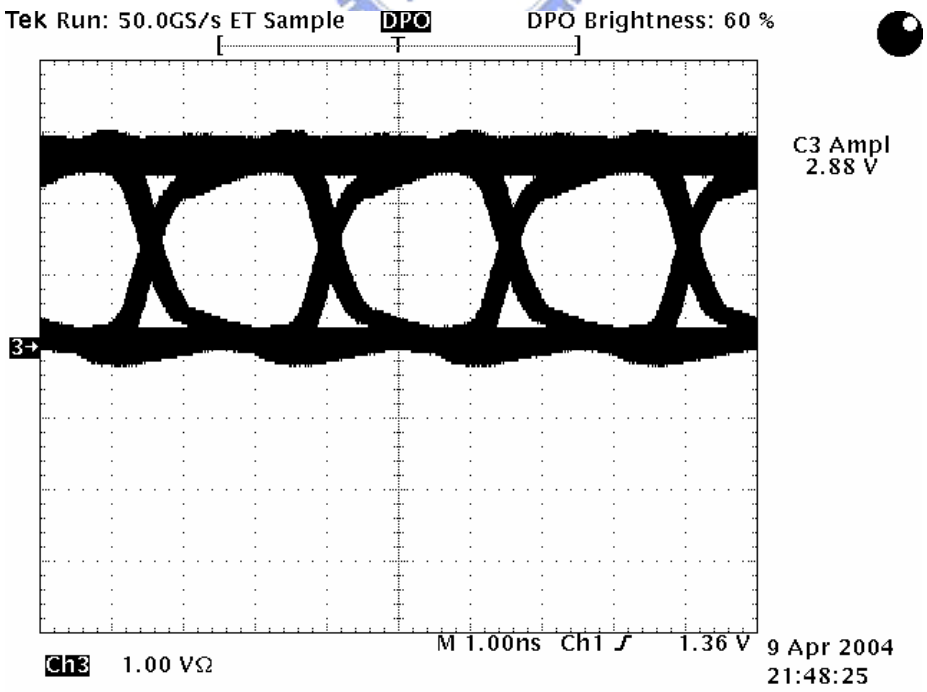


Fig. 4.29 The measured eye diagram of the receiver input buffer at 400 Mb/s. The peak-to-peak jitter is 12.94 %.

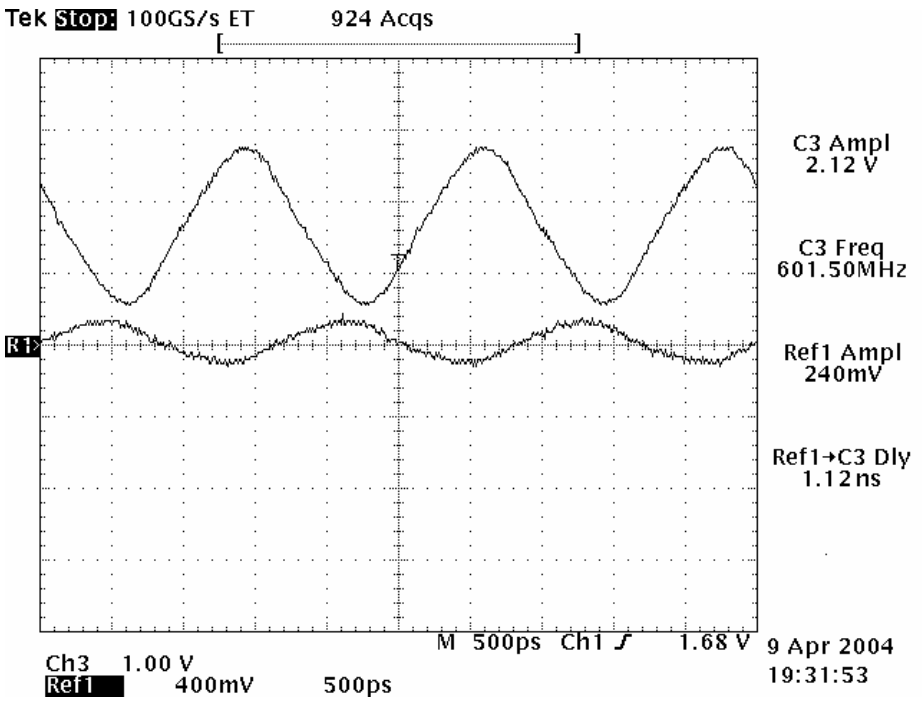


Fig. 4.30 The measured output signal of the receiver input buffer at 600 MHz. The output signal is a single-ended full-swing signal with 50 % duty cycle and the input differential signal is at the worst case (V_{OD} = ± 100 mV) defined in LVDS and RSDS standards.

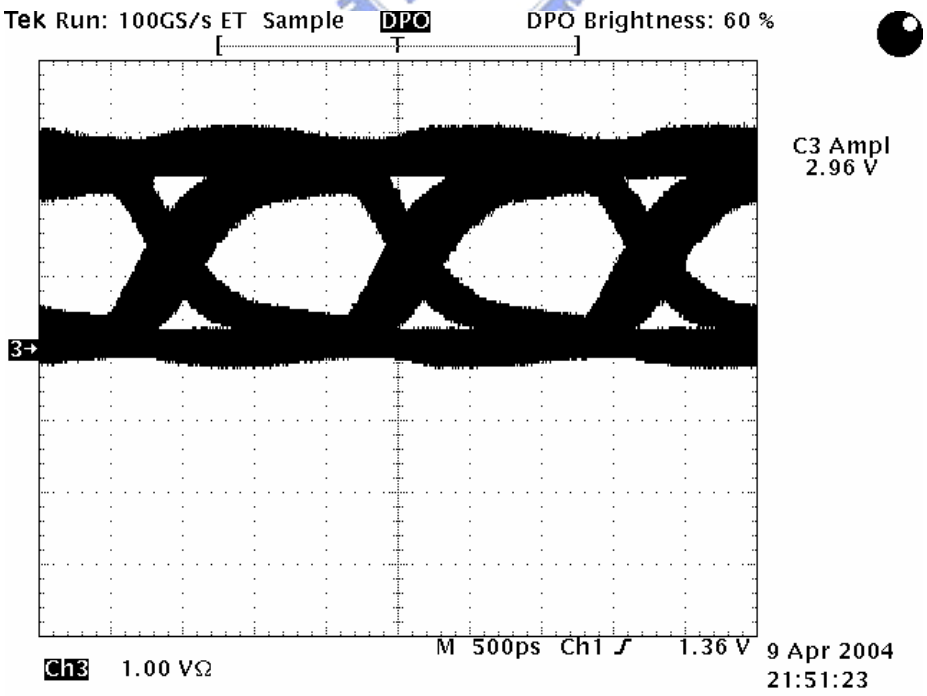


Fig. 4.31 The measured eye diagram of the receiver input buffer at 600 Mb/s. The peak-to-peak jitter is 26.47 %.

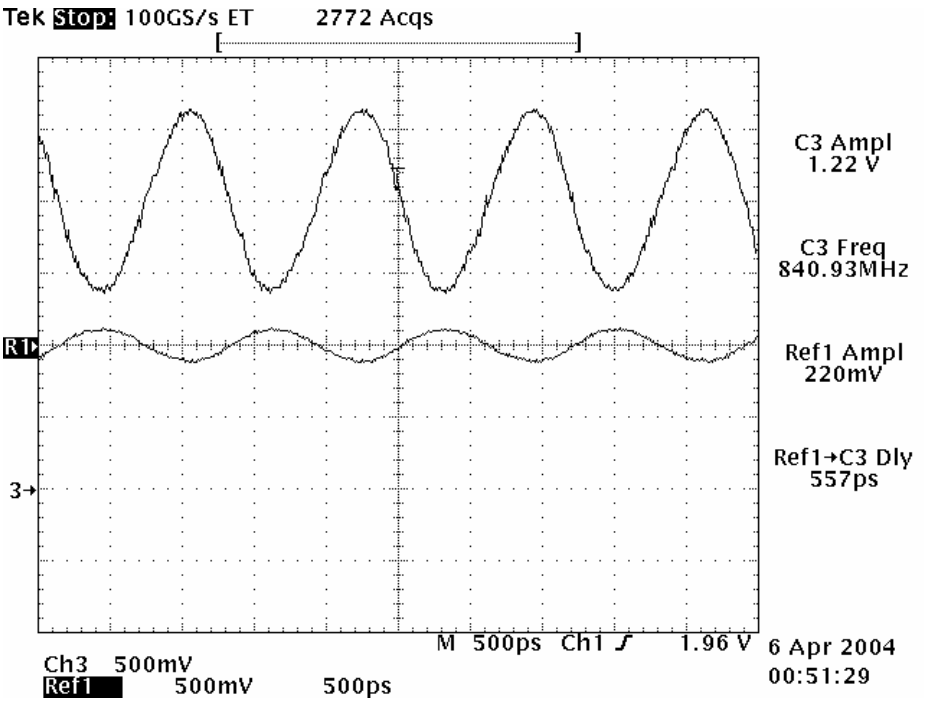


Fig. 4.32 The measured output signal of the receiver input buffer at 840 MHz. The output signal is a single-ended full-swing signal with 50 % duty cycle and the input differential signal is at the worst case (V_{OD} = ± 100 mV) defined in LVDS and RSDS standards.

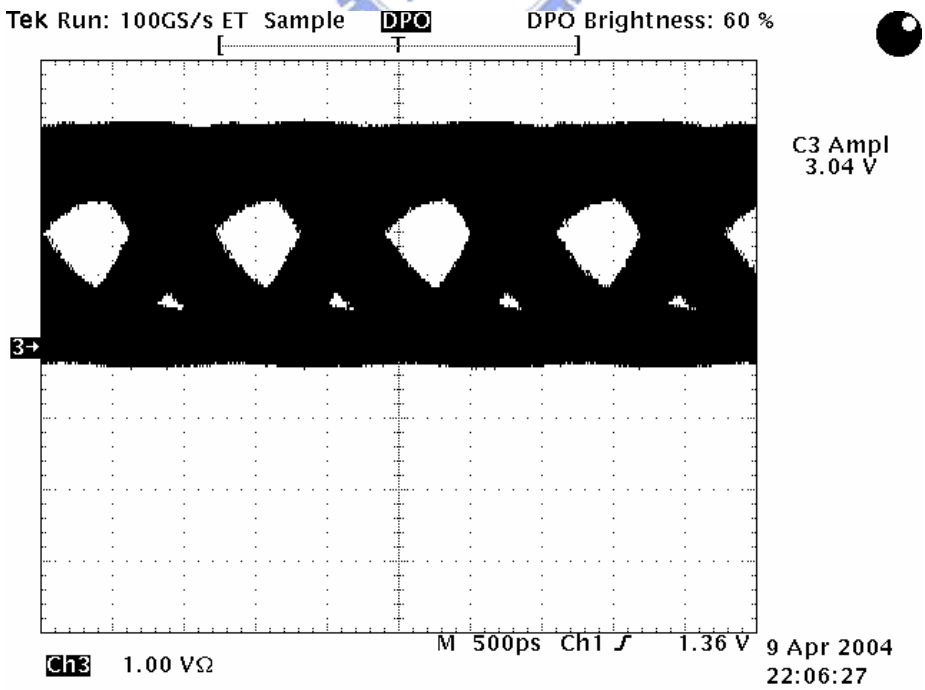


Fig. 4.33 The measured eye diagram of the receiver input buffer at 840 Mb/s. The peak-to-peak jitter is 48.2 %.

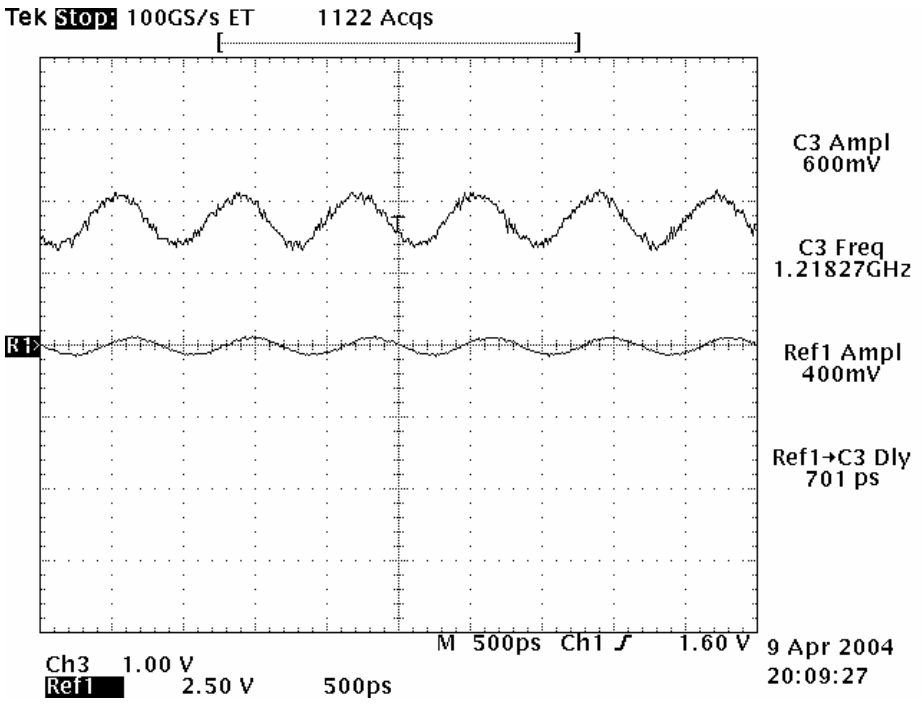


Fig. 4.34 The measured output signal of the receiver input buffer at 1.2 GHz. The output signal is a single-ended full-swing signal with 50 % duty cycle and the input differential signal is at the worst case (V_{OD} = ± 100 mV) defined in LVDS and RSDS standards.

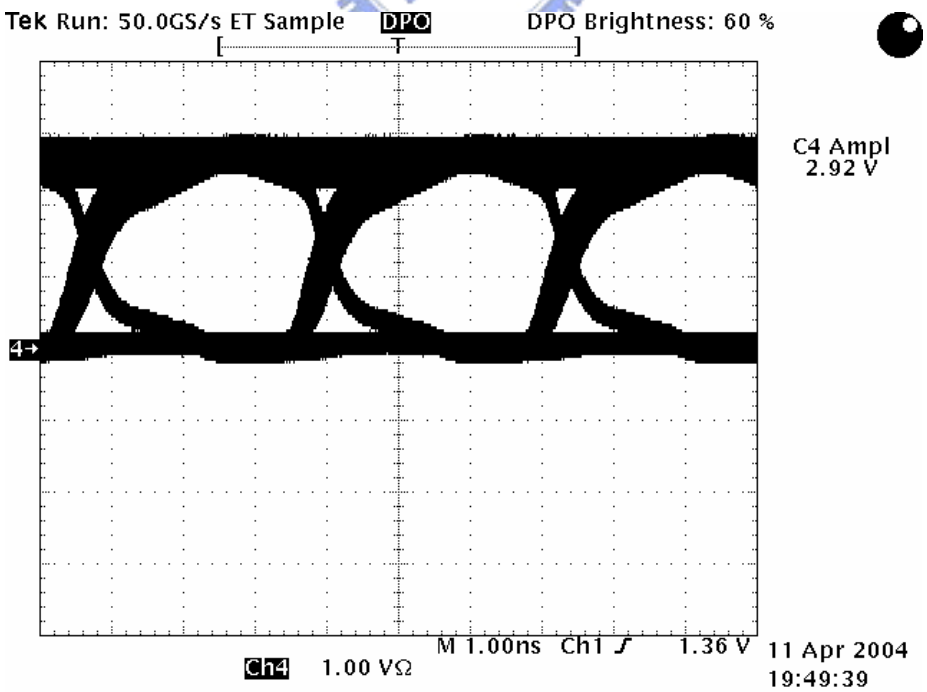


Fig. 4.35 The measured eye diagram of the I/O buffers which are connected together via two coaxial cables at 300 Mb/s. The peak-to-peak jitter is 12.8 %.

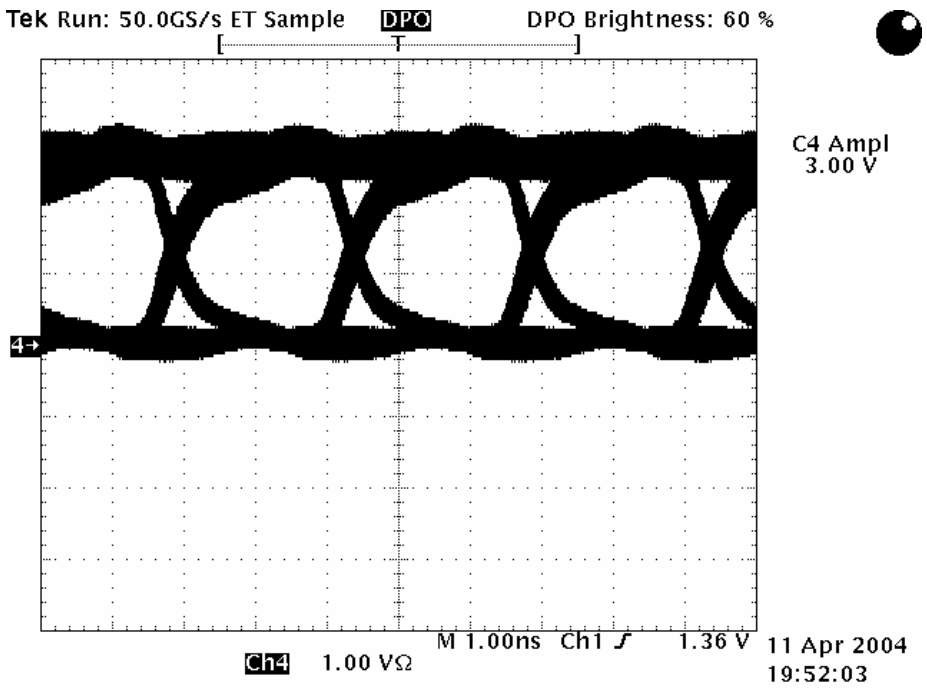


Fig. 4.36 The measured eye diagram of the I/O buffers which are connected together via two coaxial cables at 400 Mb/s. The peak-to-peak jitter is 13.7 %.

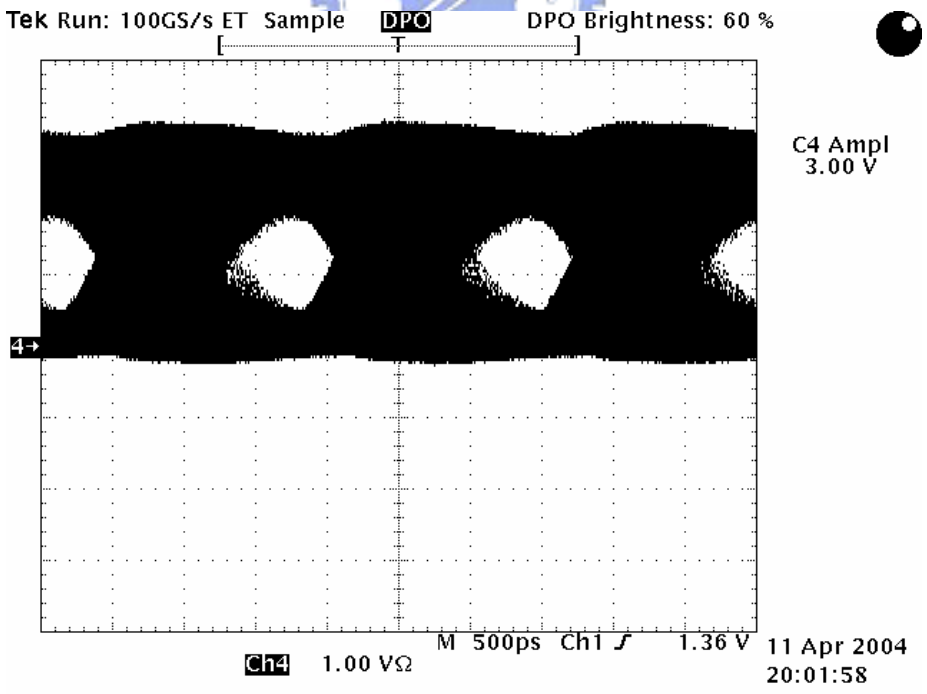


Fig. 4.37 The measured eye diagram of the I/O buffers which are connected together via two coaxial cables at 600 Mb/s. The peak-to-peak jitter is 58.2 %.

Chapter 5

Transmitter

5.1 INTRODUCTION

As the high-speed output buffers which are mentioned in the chapter 4 can successfully support the data rate up to 1.2 Gb/s, they can be embedded in the transmitter to have variety applications [20], [21]. In this chapter, a transmitter utilized in the interface that directly connect a graphics card to a liquid crystal display (LCD) timing controller of the flat panel display systems is proposed [22]. Fig. 5.1 shows the block diagram of the transmitter. The transmitter converts 28 bits of TTL data into four LVDS data streams. It means that each LVDS data stream contains seven serial data. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmitted clock, 28 bits of input TTL data are sampled and transmitted. Fig. 5.2 shows the more detail circuit blocks of the transmitter.

5.2 BUILDING BLOCKS OF THE TRANSMITTER

In this section, each component of the transmitter which is shown in Fig. 5.3 will be discussed [23].

5.2.1 Pseudo Random Binary Sequence

A pseudo random binary sequence (PRBS) is a test pattern that appears to be

random, but is actually a predictable and repeatable sequence with a very long interval, depending upon the pattern. A PRBS is an algorithmically determined bit sequence that has the same statistical characteristics as a truly random sequence and simulates live traffic. The transmitter has a PRBS generator as shown in Fig. 5.4, it uses D-type flip flops and one OR logic gate to realize algorithmically determined bit sequence. The circuit implementation of the D-type flip-flop which is utilized in the PRBS is true single-phase clock logic (TSPC) as shown in Fig. 5.5. The RESET pin in the PRBS is employed to trigger the PRBS in case of the all zero state and the CLK pin is connected to the external pulse generator in order to generate the same frequency pseudo random patterns as the external clock source. When the RESET pin is logic low, the PRBS is forced to enable. After a while, the RESET pin should be changed to logic high in order to keep the patterns correct. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors. The bit length of the PRBS is 2^9-1. Fig. 5.6 shows the simulated output signals of the seven PRBS outputs.

5.2.2 Phase-Locked Loop

The architecture of the PLL which is used in the transmitter is almost the same as the one mentioned in the chapter 3. Fig. 5.7 shows the architecture of the PLL. The seven NAND logic gates in the PLL is employed to make a four to three duty cycle of the seven output clocks in order to perform the parallel to serial conversion better. Fig. 5.8 shows the circuit implementation of the phase frequency detector. Fig. 5.9 shows the circuit implementation of the charge pump. Fig. 5.10 shows the circuit implementation of the self-biased replica-feedback bias generator. Fig. 5.11 shows the circuit implementation of the voltage-controlled oscillator. Fig. 5.12 shows the circuit implementation of the differential-to-single-ended converter. The simulated seven

output clocks with four to three duty cycle of the PLL are shown in Fig. 5.13. The simulated and measured parameters of the designed PLL are shown in Table 5.1.

5.2.3 Multiplexer and Co-Designed Output Buffer

Fig. 5.14 shows the circuit implementation of the multiplexer. It receives seven parallel output signals from the PRBS and uses seven phases came from the PLL to perform the parallel to serial conversion. Fig. 5.15 is the timing diagram of the multiplexer. The co-designed output buffer which follows the multiplexer is the same as the one mentioned in the chapter 4. The only difference is that four NMOS switches are used in order to have balance rise time and fall time of the output signals. Fig. 5.16 shows the circuit implementation of the co-designed output buffer. Fig. 5.17 shows the main function of the transmitter. It can be realized that the data rate of the output signal is seven times higher than the input reference clock.

5.3 MEASUREMENT RESULT

Fig. 5.18 shows the chip photo of the transmitter which is fabricated in a 0.25-μm 1P5M CMOS process with the 3.3-V power supply. The chip area of the transmitter is 1500 μm × 1500 μm. The measurement setup of the transmitter is shown in Fig. 5.19. Fig. 5.20 shows the top view of the testing PCB photo for the transmitter. One of the four data channels and the PLL channel are tested. Fig. 5.21 shows the bottom view of the testing PCB photo for the transmitter. The measured output signals of the transmitter which is in the LVDS or RSDS mode are shown in Figs. 5.22 and 5.23 respectively. The output signal voltage swings of the LVDS and RSDS mode are all in the defined voltage range of the specifications. Fig. 5.24 shows the measured LVDS eye diagram of the transmitter at 700 Mb/s. The peak-to-peak jitter is 24 %.

Fig. 5.25 shows the measured RSDS eye diagram of the transmitter at 700 Mb/s. The peak-to-peak jitter is 25.15 %. Fig. 5.26 shows the measured LVDS eye diagram of the transmitter at 840 Mb/s. The peak-to-peak jitter is 31.5 %. Fig. 5.27 shows the measured RSDS eye diagram of the transmitter at 840 Mb/s. The peak-to-peak jitter is 32.8 %. Fig. 5.28 shows the measured LVDS eye diagram of the transmitter at 1.05 Gb/s. The peak-to-peak jitter is 26.25 %. Fig. 5.29 shows the measured RSDS eye diagram of the transmitter at 1.05 Gb/s. The peak-to-peak jitter is 27.89 %. All above eye diagrams are measured with package. In order to have better jitter performance, bare die with bond wires is tested on the PCB. Fig. 5.30 shows the measured LVDS eye diagram of the transmitter at 700 Mb/s by using bare die. The peak-to-peak jitter is 21.87 %. Fig. 5.31 shows the measured LVDS eye diagram of the transmitter at 840 Mb/s by using bare die. The peak-to-peak jitter is 18.4 %. Fig. 5.32 shows the measured LVDS eye diagram of the transmitter at 1.05 Gb/s by using bare die. The peak-to-peak jitter is 19.7 %. It is obvious that the jitter performance of the transmitter is better by using bare die rather than package. Figs. 5.33 and 5.34 show the measured output clock of the PLL at 120 MHz and 150 MHz. The duty cycle of the output clocks at 120 MHz and 150 MHz are almost four to three. The long-term peak-to-peak jitter of the PLL output signal at 120 MHz is 88 ps which is 1.056 % of the PLL output signal time period as shown in Fig. 5.35.

Fig. 5.36 shows the measurement setup of the transmitter with a 3-meter long UTP Cat.6 line. The measurement of the 3-meter long UTP Cat.6 line with two termination boards is shown in Fig. 5.37. Figs. 5.38, 5.39 and 5.40 show the measured 840-Mb/s eye diagram of the transmitter with UTP Cat.6 lines at 1 meter, 2 meter and 3 meter. Figs. 5.41, 5.42 and 5.43 show the measured 1-Gb/s eye diagram of the transmitter with UTP Cat.6 lines at 1 meter, 2 meter and 3 meter. Fig. 5.44 shows the layout and schematic of the ESD protection circuit which is employed to protect the

core circuit. Fig. 5.45 shows the measurement setup of the ESD testing. The testing model is the human body model (HBM). Fig. 5.46 shows the measurement results of the ESD protection circuit. The measured parameter of the transmitter is summarized in Table 5.1.

5.4 CONCLUSION

A transmitter that can converts 28 bits of TTL data to four LVDS or RSDS data streams plus one clock data is implemented in this thesis. The 28 bits of TTL data include eight Red data, eight Green data, eight Blue data and four control lines which is one of the specifications in the flat panel display links. The measured data rate of the transmitter is up to 1.05 Gb/s which can support the SXGA (1280 × 1024 pixels) resolution of flat panel displays.

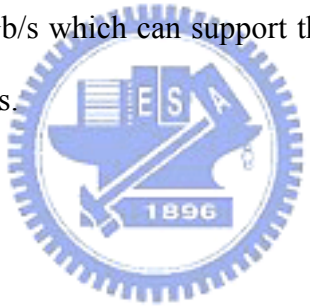


Table 5.1

The simulated and measured parameters of the designed PLL.

Function	PLL
Simulation Results	
Operate Voltage	3.3 V
Input Frequency	120 MHz
Output Frequency	120 MHz
Charge Pump Current	100 μA
Divided by N	N = 1
VCO Gain	167 MHz/V
C_1	78.75 pF
C_2	4.07 pF
R_1	1.89 kΩ
Phase Margin	65 °
Loop Bandwidth	4.8 MHz
Extra Zero	1.07 MHz
Extra Pole	21.77 MHz
Natural Frequency	2.32 MHz
Damping Factor	0.766
Power	34.48 mW@120 MHz
Measurement Results	
Technology	VIS 0.25-μm 1P5M CMOS
Output Clock Jitter	88 ps (long-term peak-to-peak jitter)@120 MHz, < 1.056 %
Function	Transmitter
Measurement Results	
Operate Voltage	3.3 V
Power Consumption (1)	283 mW@840 Mb/s
Power Consumption (2)	300.3 mW@1.05 Gb/s
Data Rate	Target at 840 Mb/s (Measured up to 1.05 Gb/s)
Technology	VIS 0.25-μm 1P5M CMOS

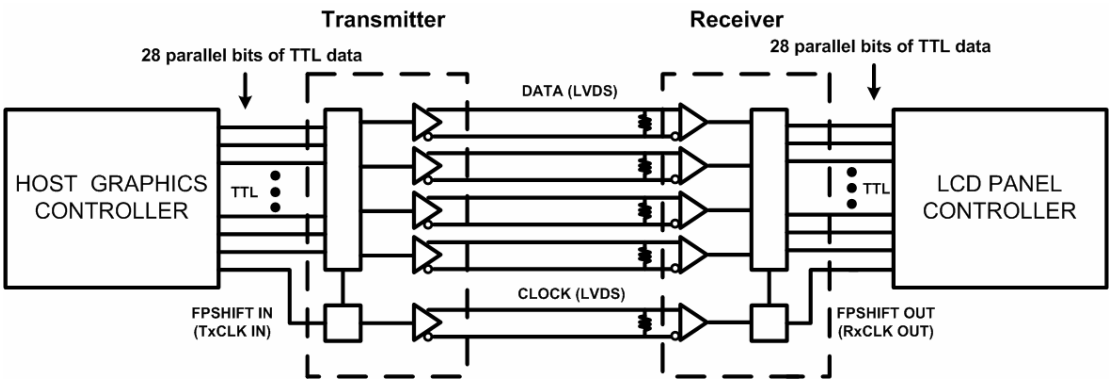


Fig. 5.1 The block diagram of the transmitter.

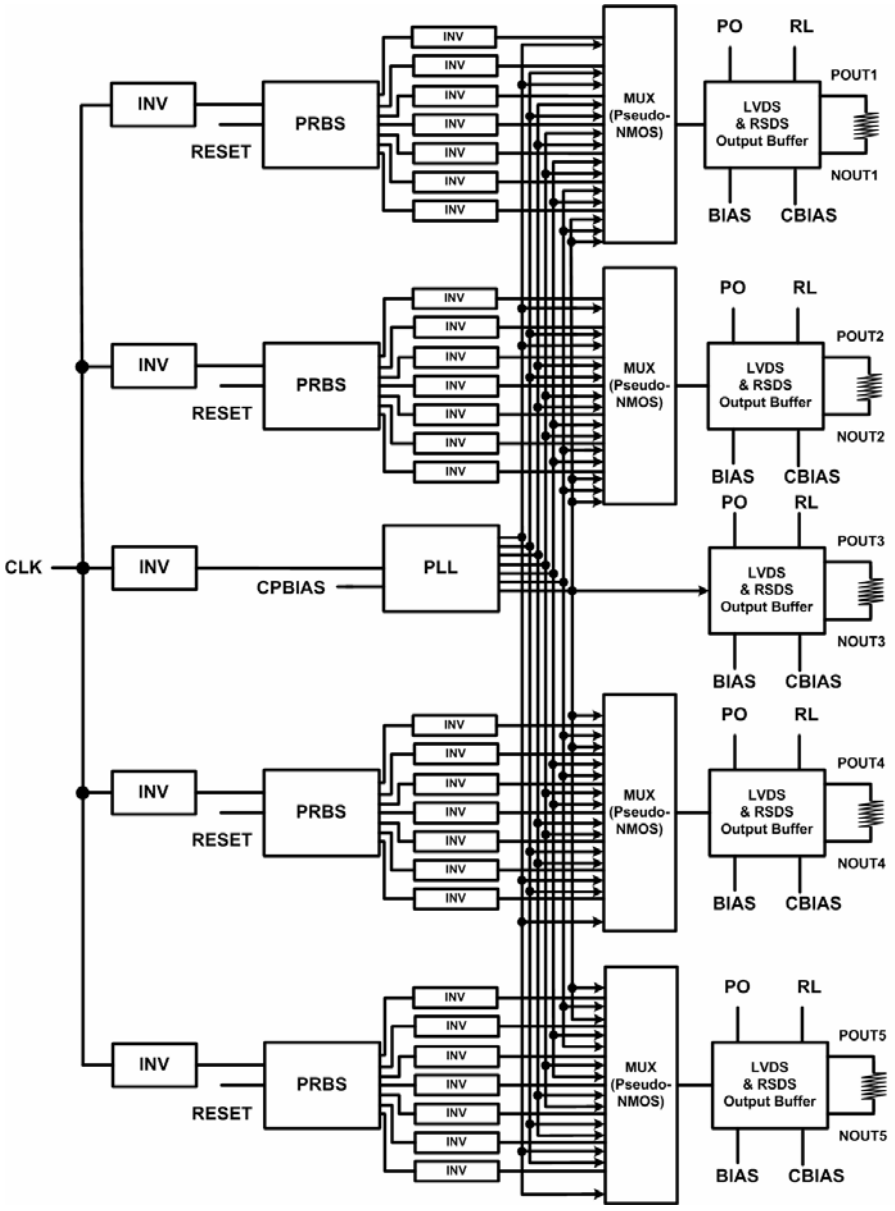


Fig. 5.2 The more detail circuit blocks of the transmitter.

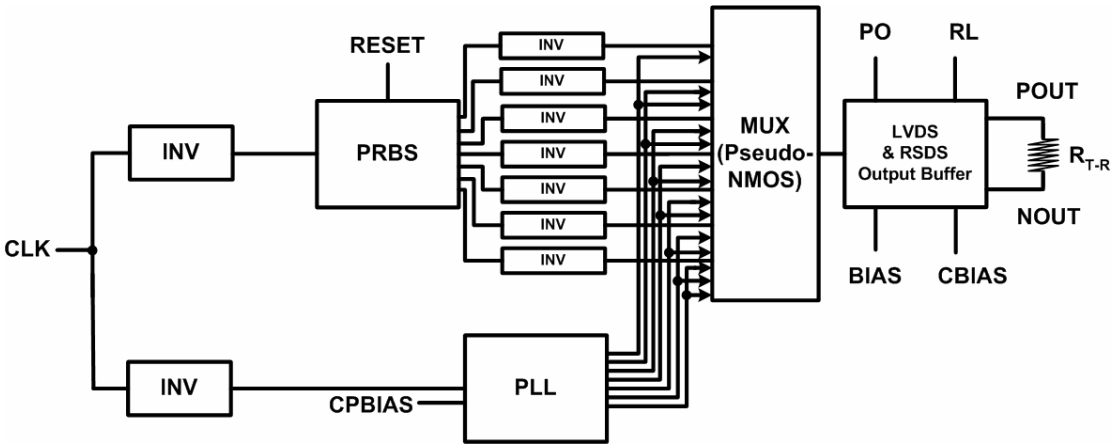


Fig. 5.3 The circuit block of the transmitter which converts seven parallel TTL data to one serial LVDS or RSDS data stream.

Fig. 5.4 The circuit implementation of the pseudo random binary sequence (PRBS).

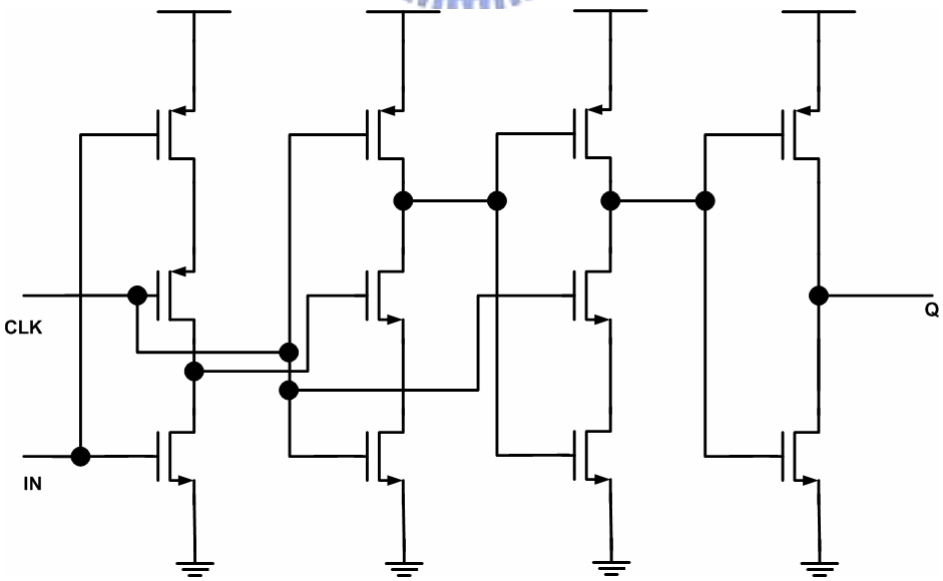


Fig. 5.5 The circuit implementation of the positive edge-triggered D-type flip-flop using true single-phase clock logic (TSPC).

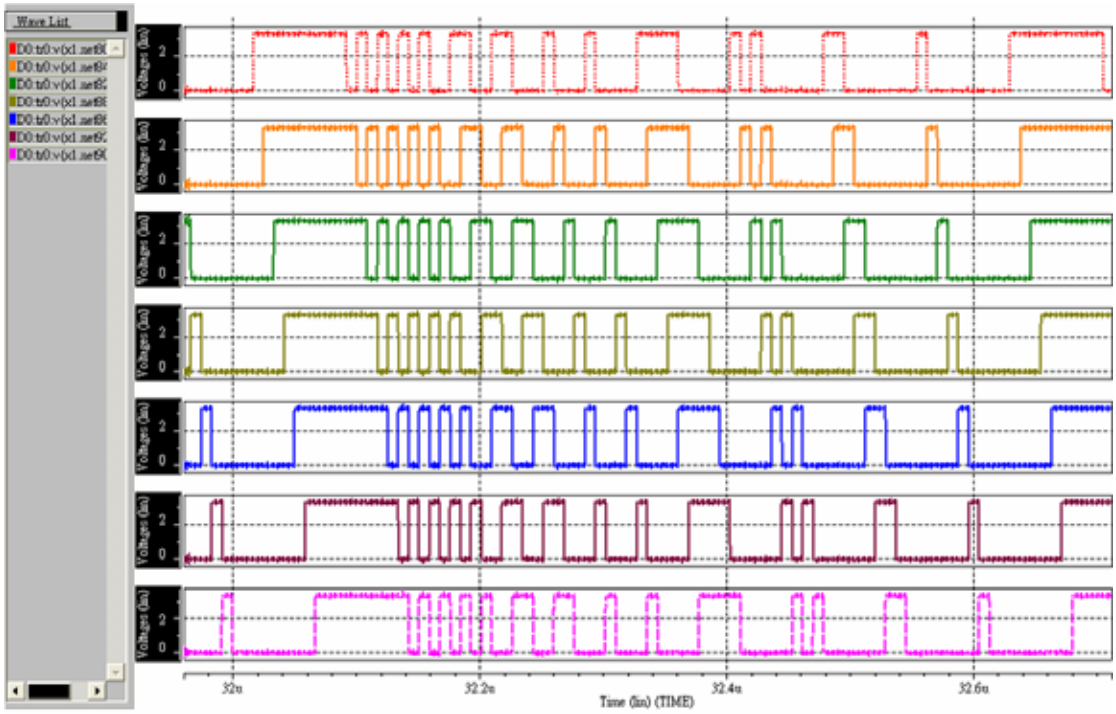


Fig. 5.6 The simulated patterns of the pseudo random binary sequence (PRBS).

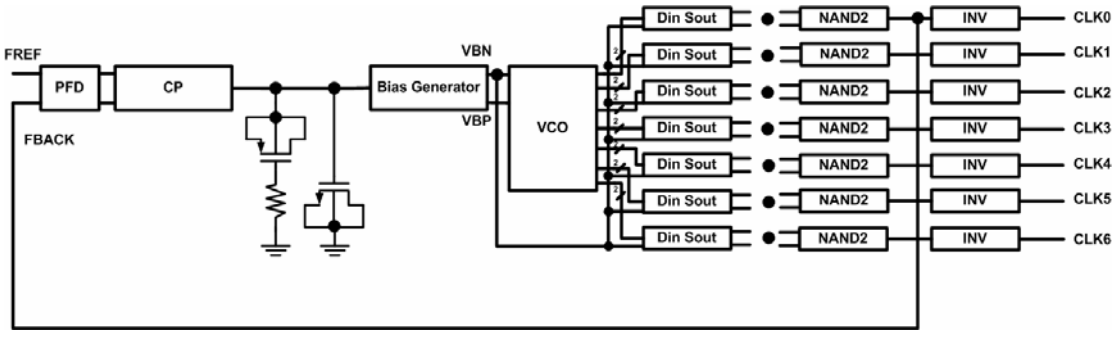


Fig. 5.7 The architecture of the PLL which is used in the transmitter.

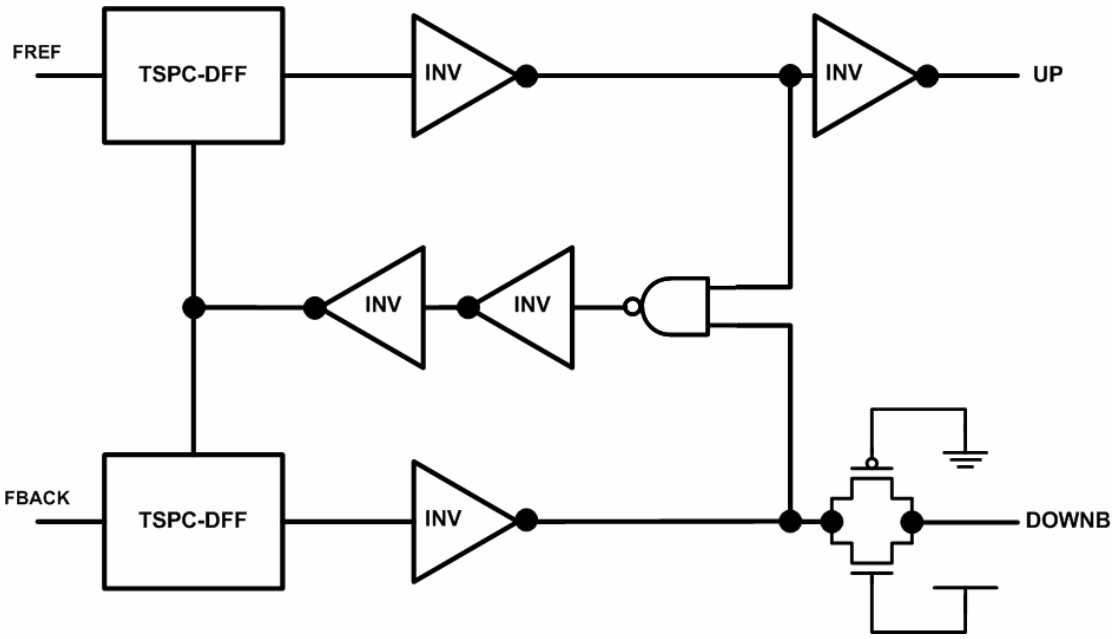


Fig. 5.8 The circuit implementation of the phase frequency detector.

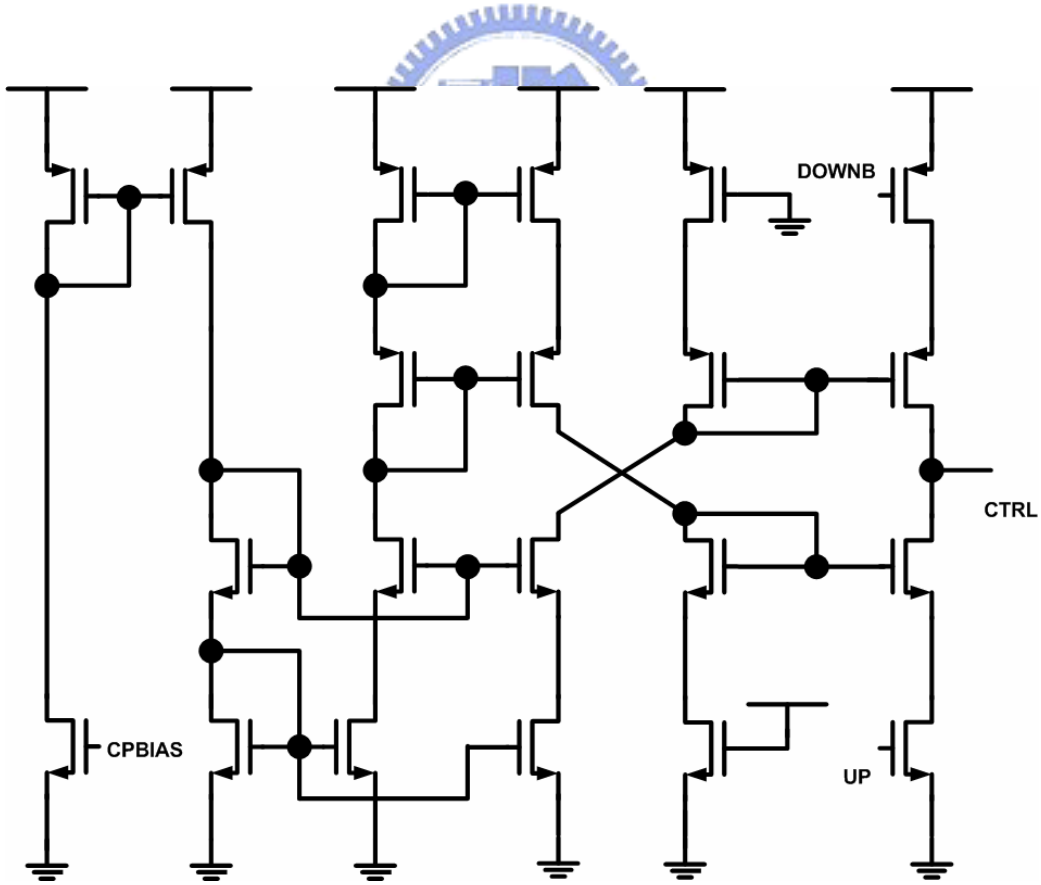


Fig. 5.9 The circuit implementation of the charge pump.

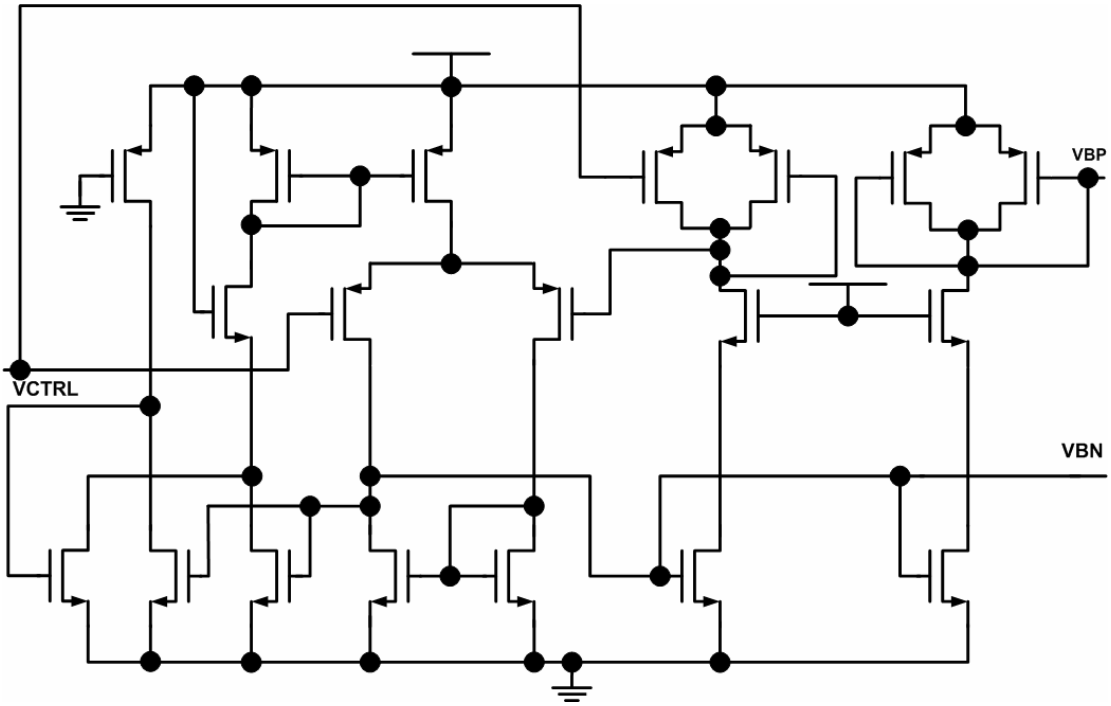


Fig. 5.10 The circuit implementation of the self-biased replica-feedback bias generator.

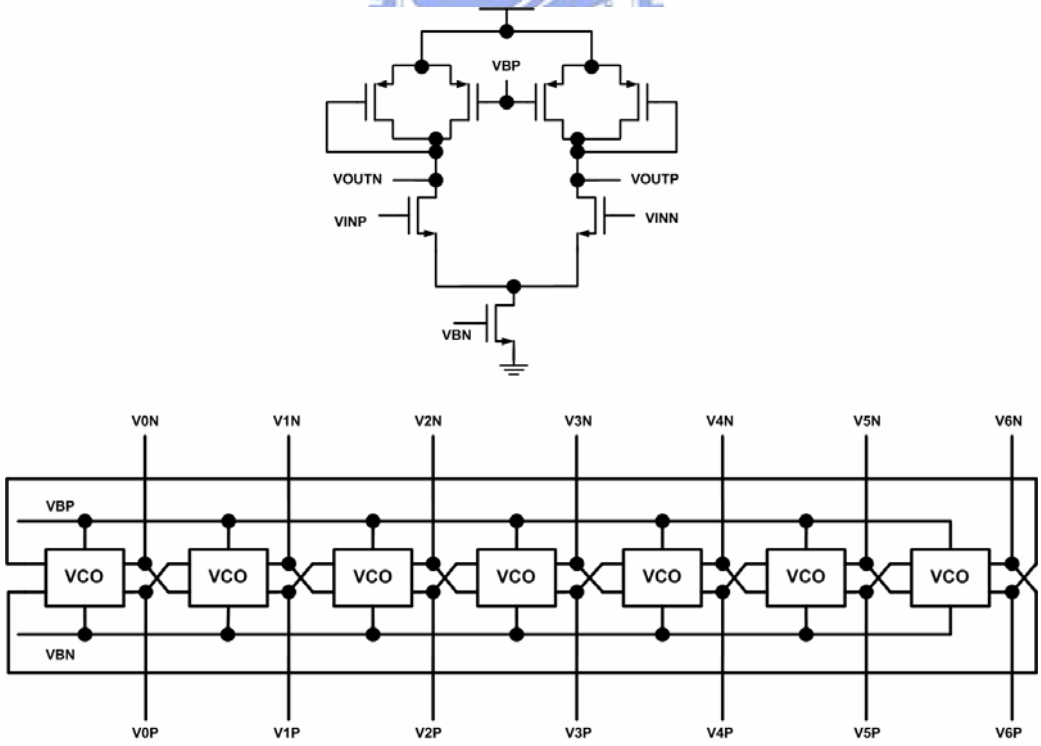


Fig. 5.11 The circuit implementation of the voltage-controlled oscillator.

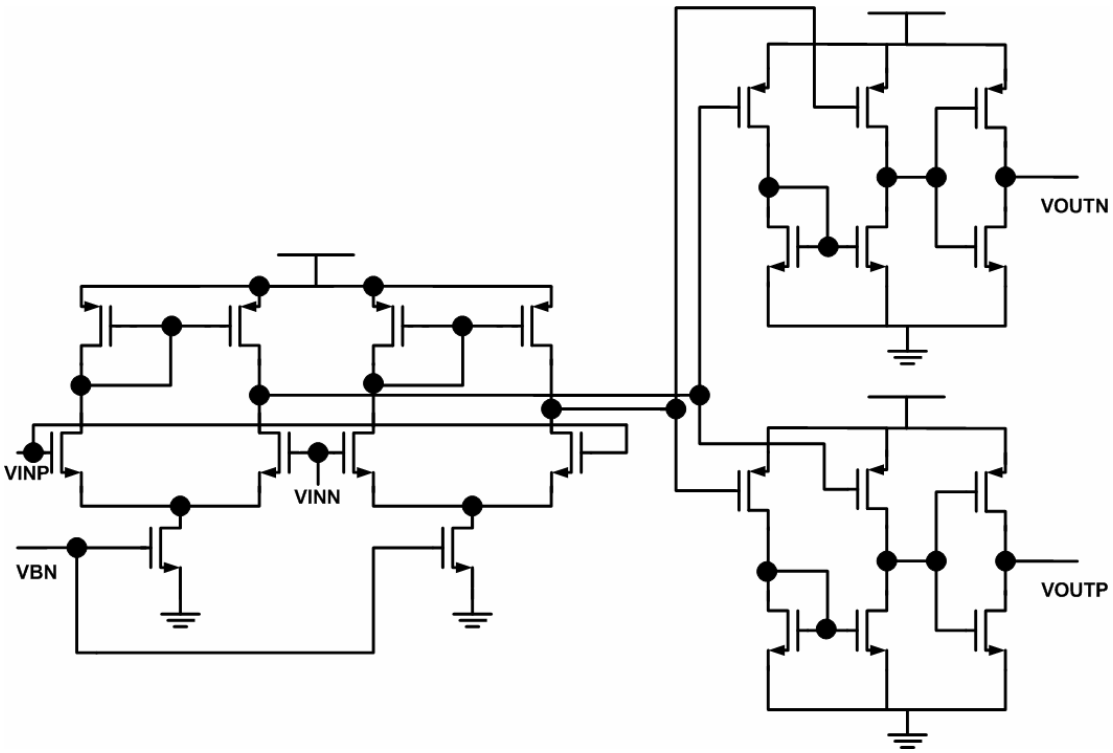


Fig. 5.12 The circuit implementation of the differential-to-single-ended converter.

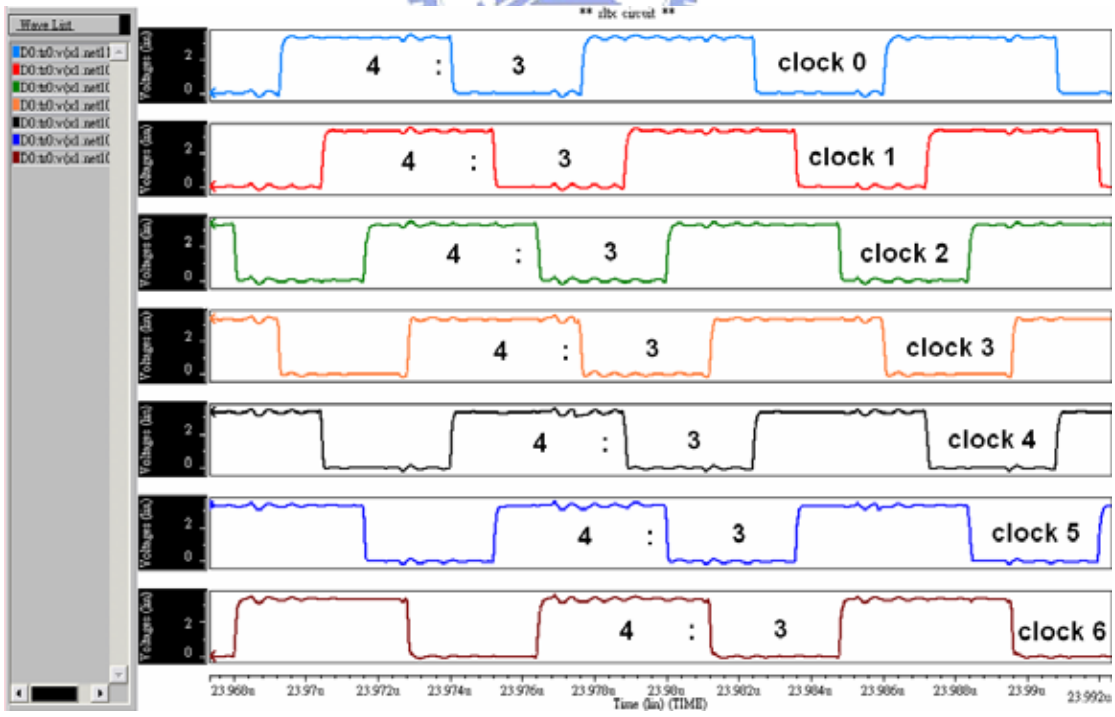


Fig. 5.13 The simulated seven output clocks with four to three duty cycle of the PLL.

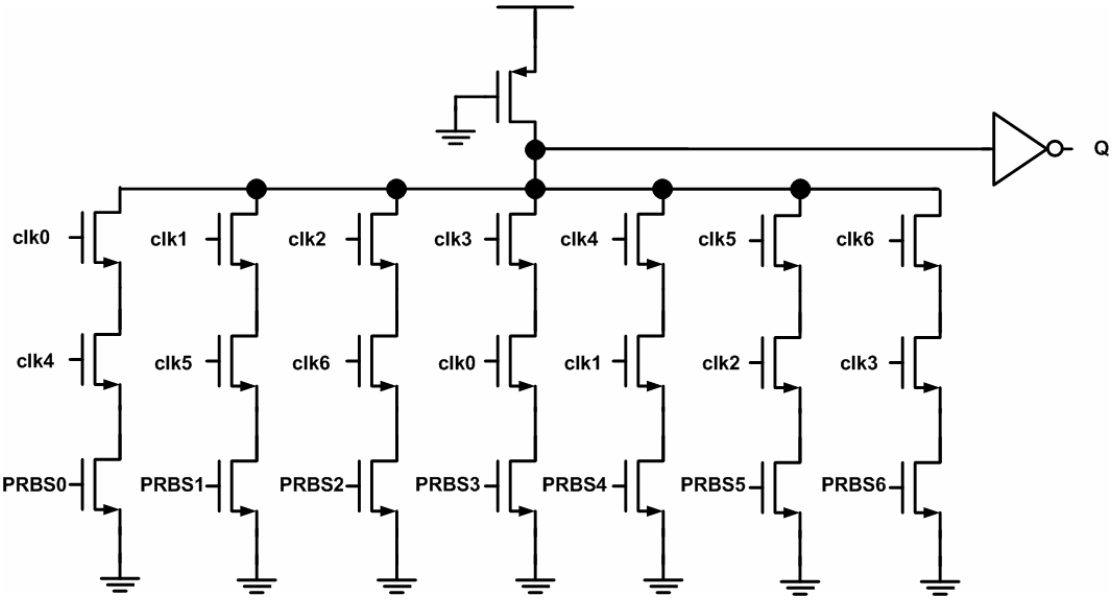


Fig. 5.14 The circuit implementation of the multiplexer.

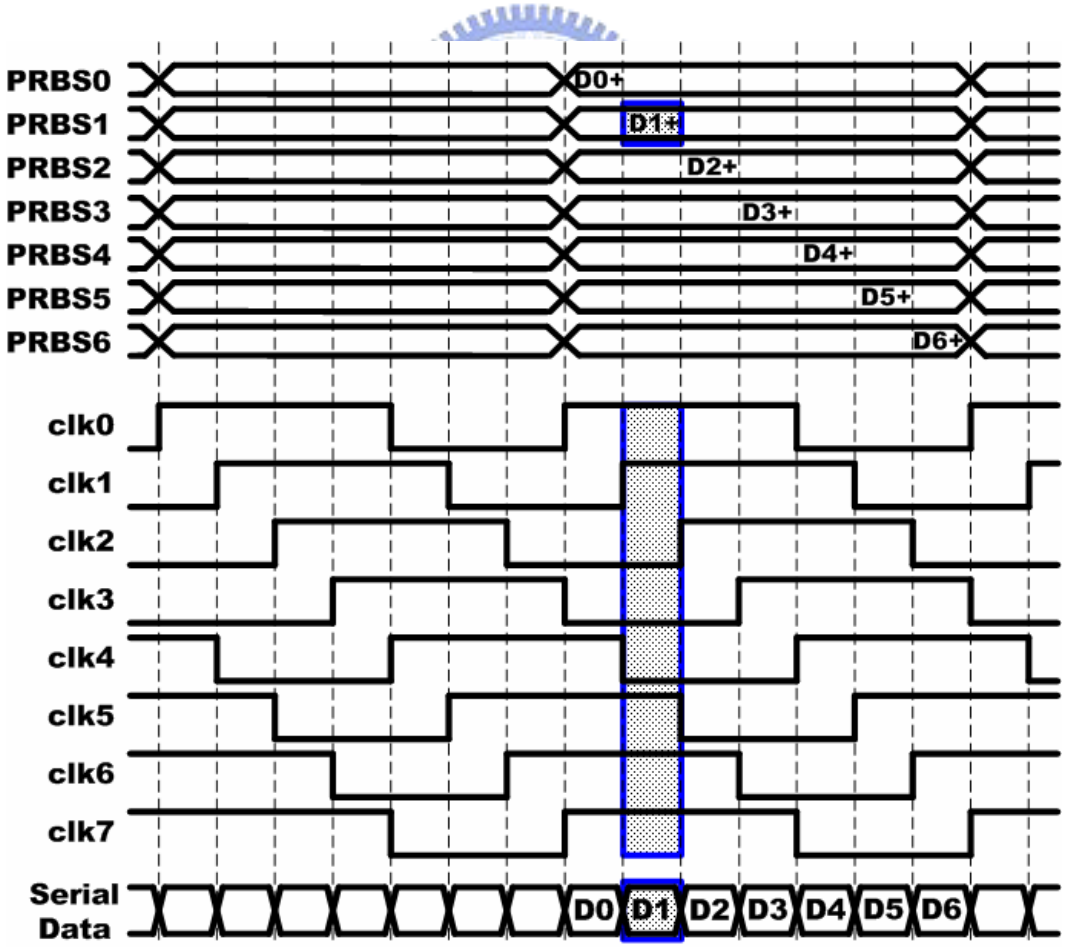


Fig. 5.15 The timing diagram of the multiplexer.

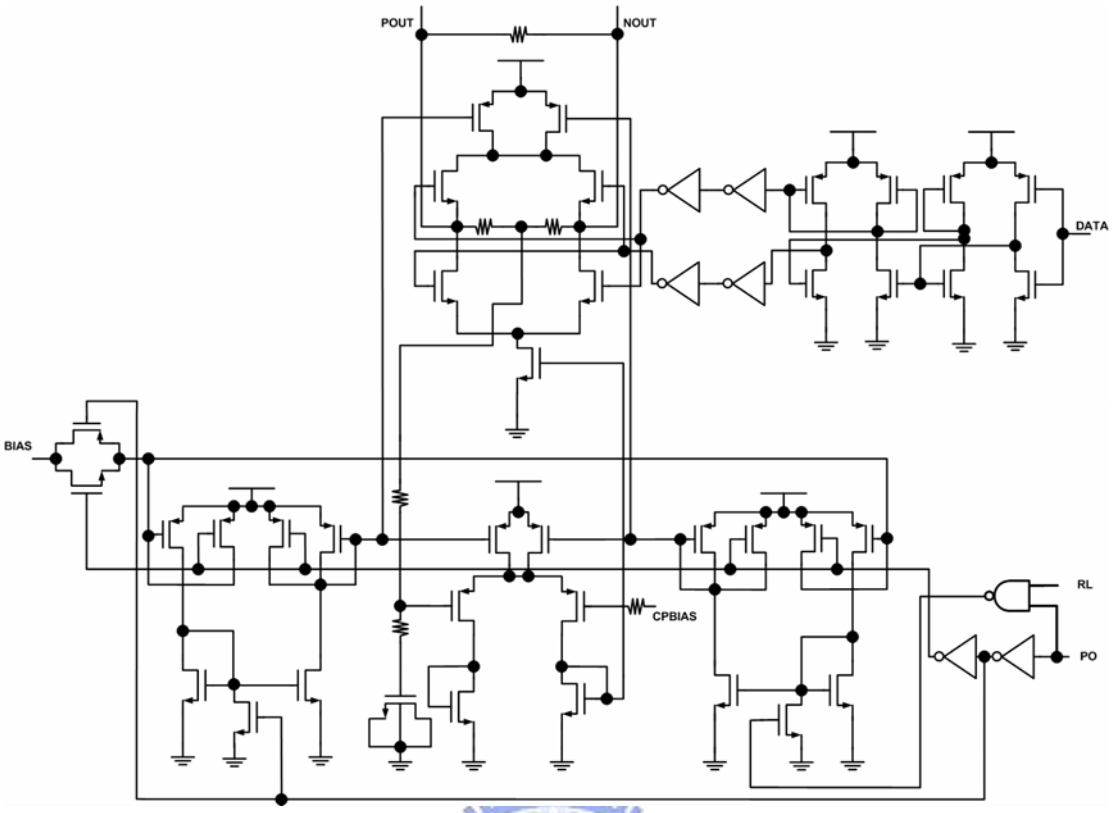


Fig. 5.16 The circuit implementation of the co-designed output buffer.

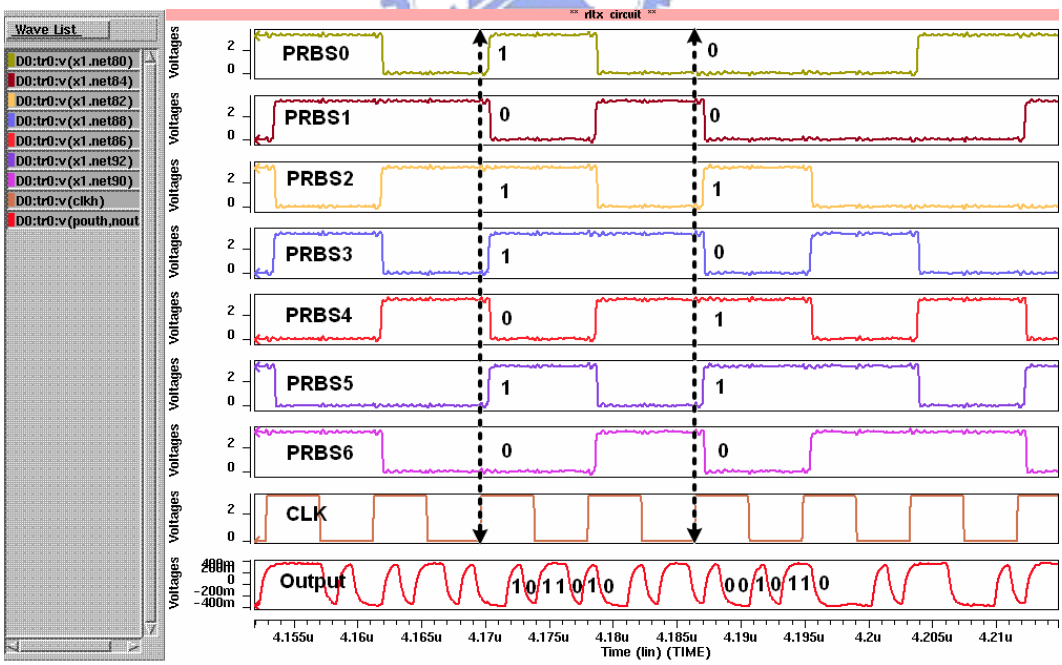


Fig. 5.17 The parallel to serial conversion of the seven parallel PRBS data to one serial LVDS data stream.

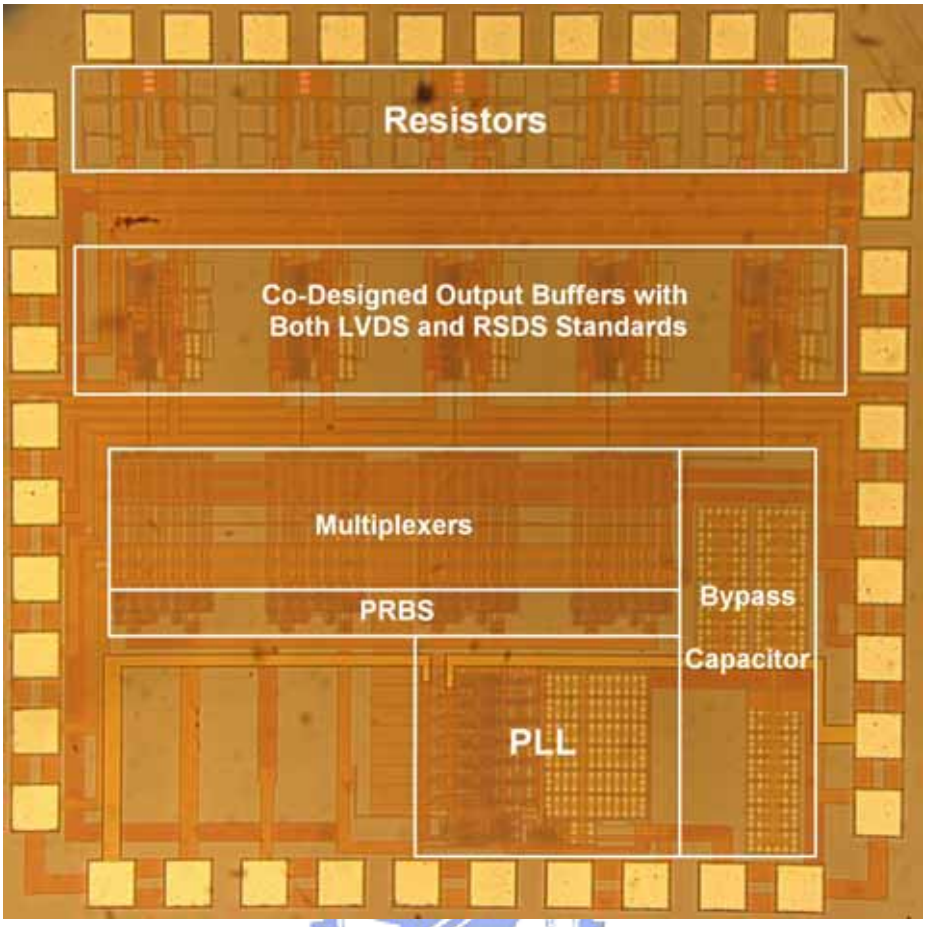


Fig. 5.18 Photograph of the transmitter in a 0.25-μm 1P5M 3.3-V CMOS process.

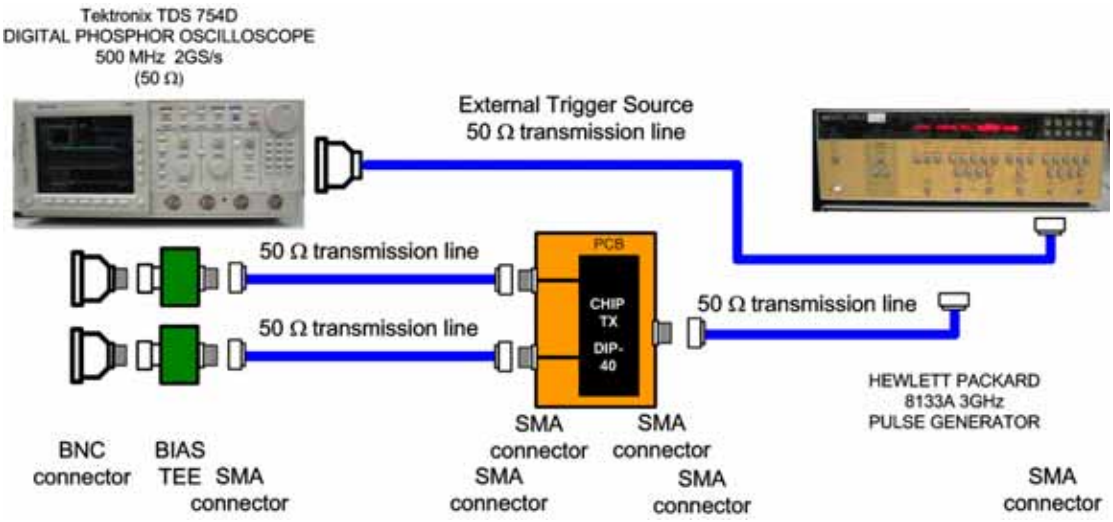


Fig. 5.19 Measurement setup of the transmitter.

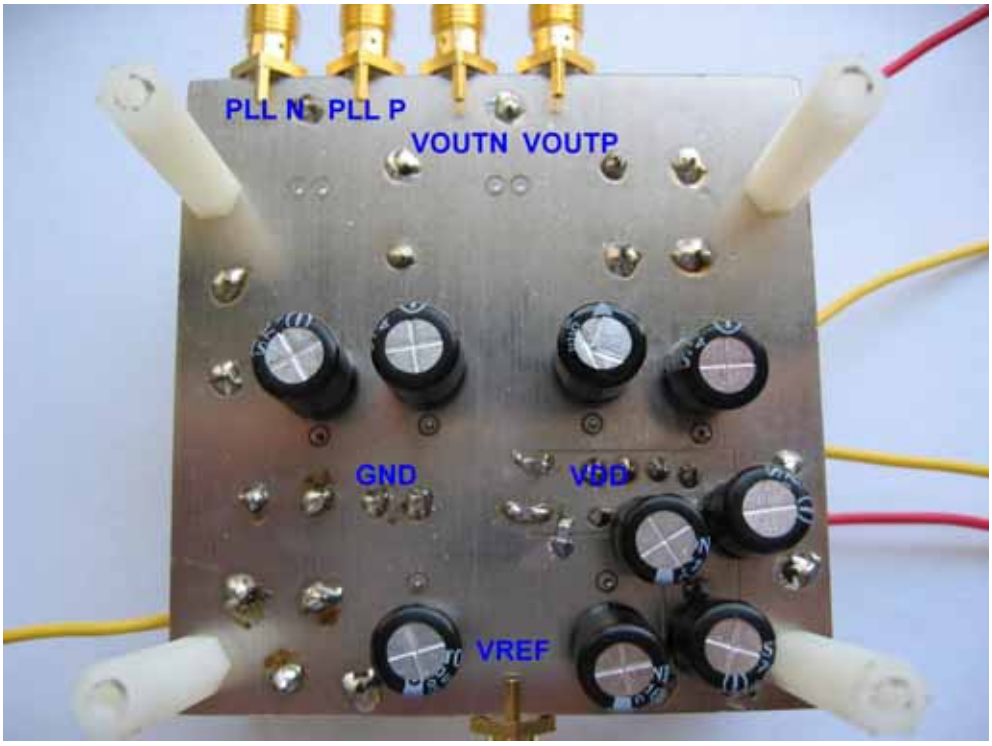


Fig. 5.20 The top view of the testing PCB photo for the transmitter.

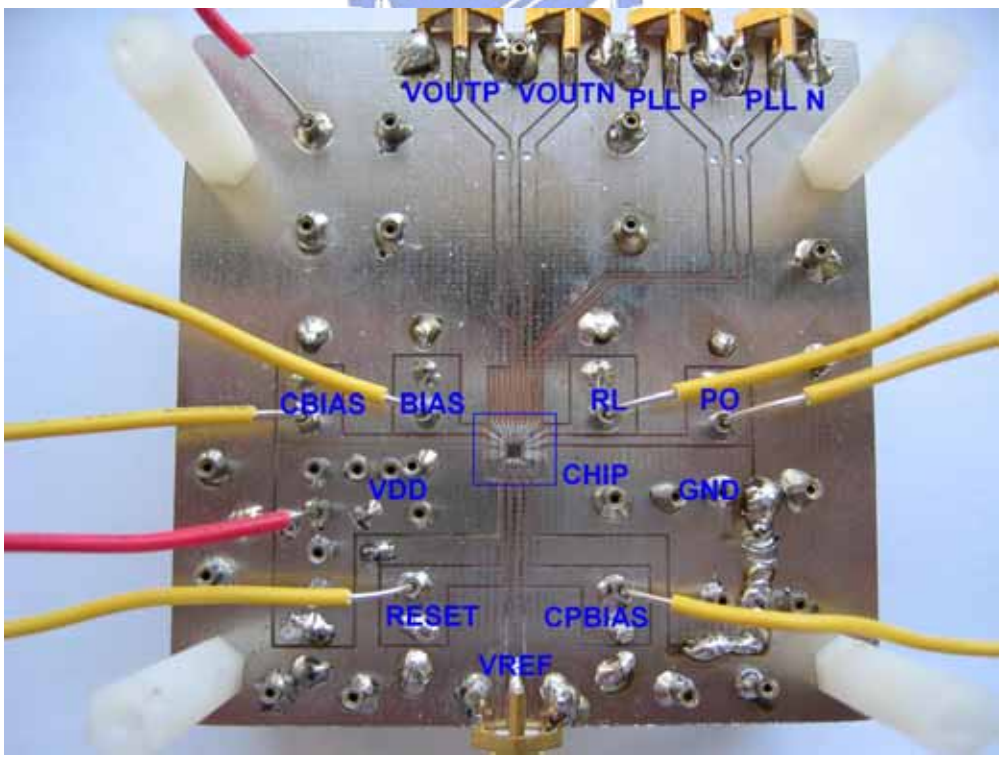


Fig. 5.21 The bottom view of the testing PCB photo for the transmitter.

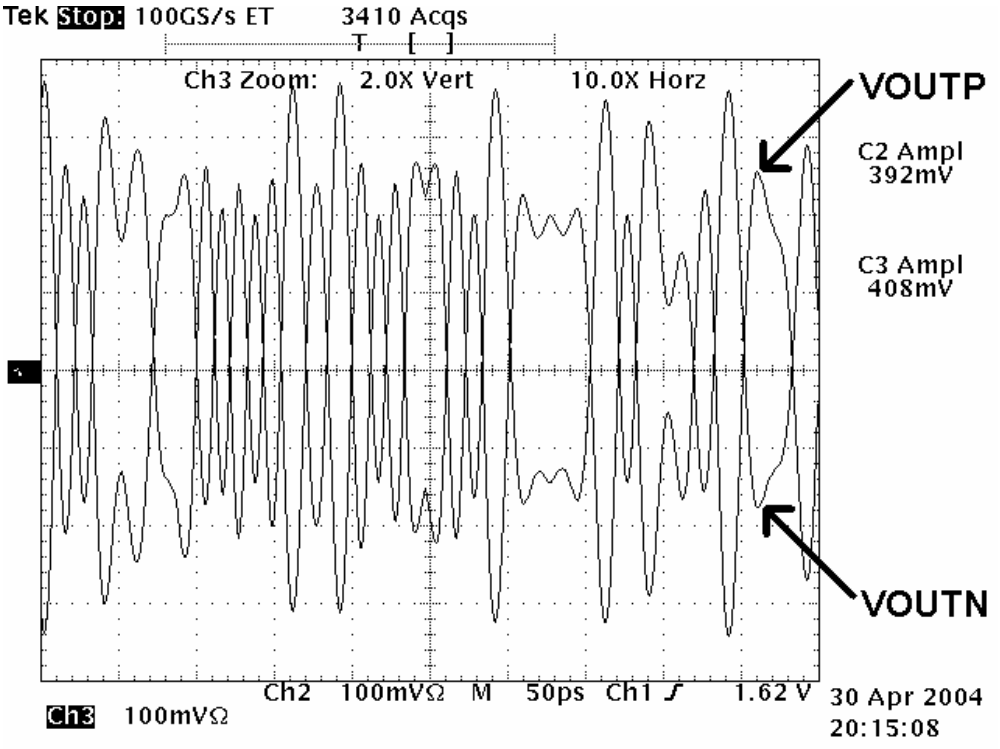


Fig. 5.22 The differential output signals of the transmitter in the LVDS mode.

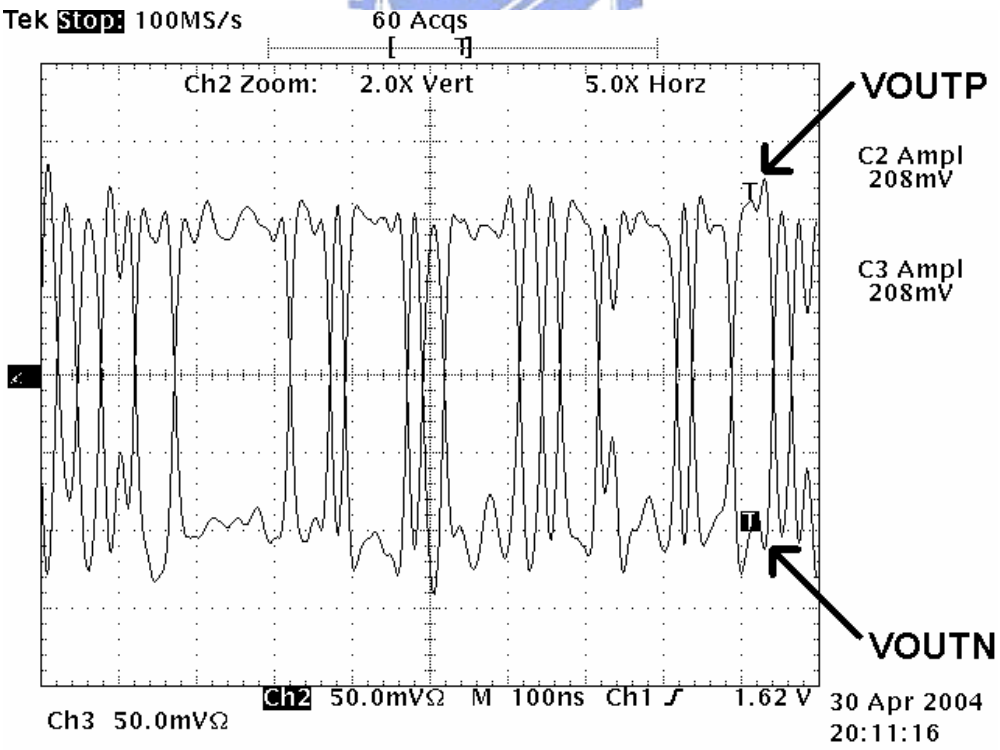


Fig. 5.23 The differential output signals of the transmitter in the RSDS mode.

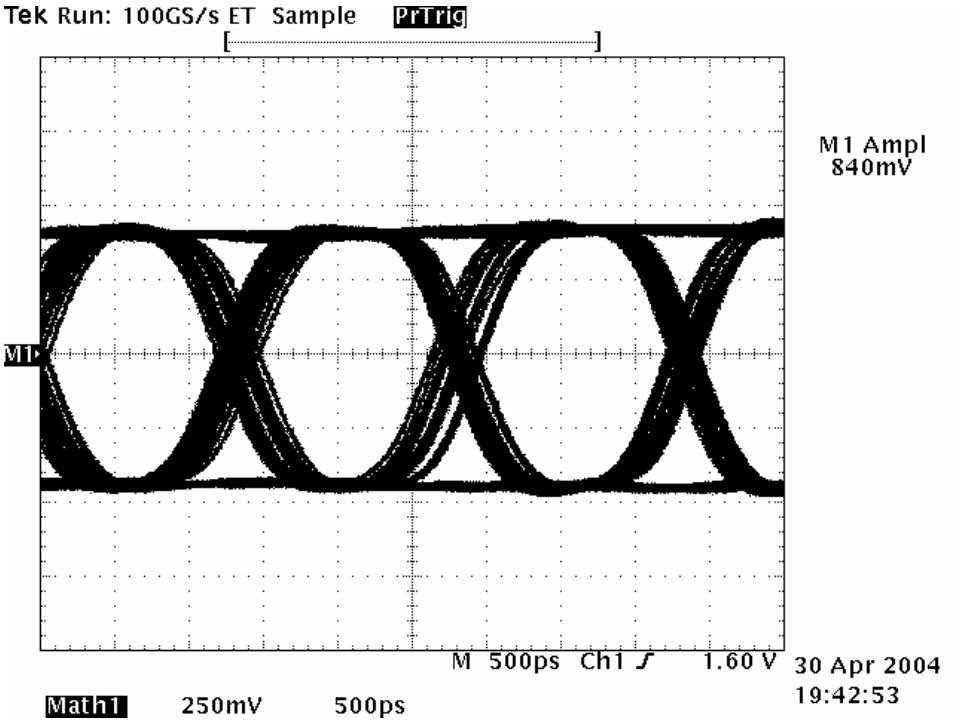


Fig. 5.24 The measured eye diagram of the transmitter at 700 Mb/s with package. The peak-to-peak jitter is 24 %. The transmitter is in the LVDS mode.

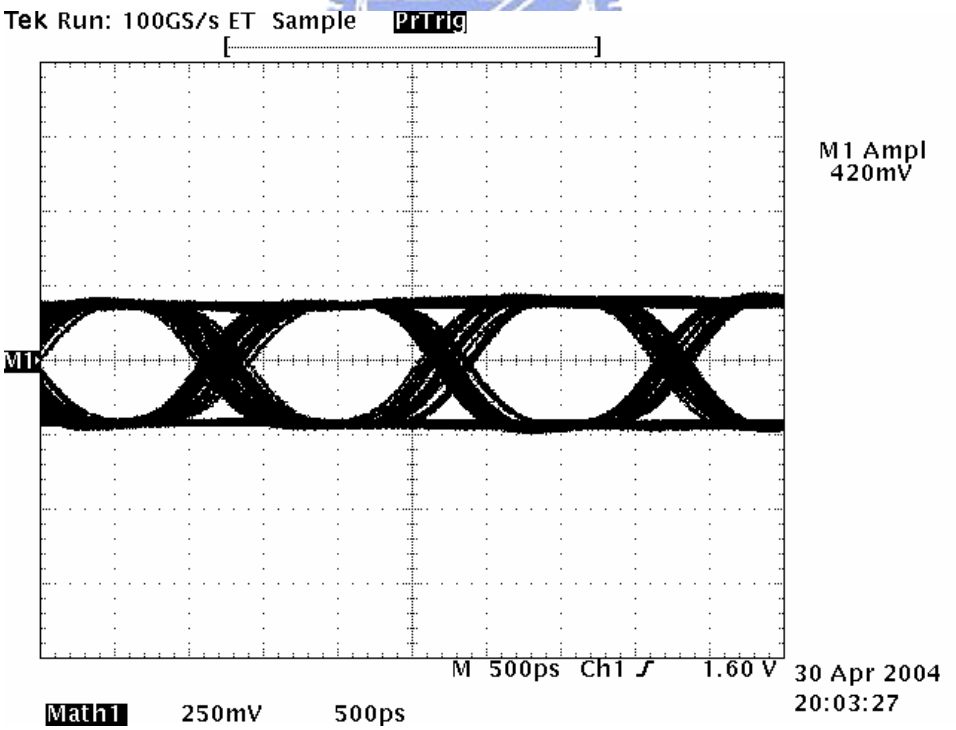


Fig. 5.25 The measured eye diagram of the transmitter at 700 Mb/s with package. The peak-to-peak jitter is 25.15 %. The transmitter is in the LVDS mode.

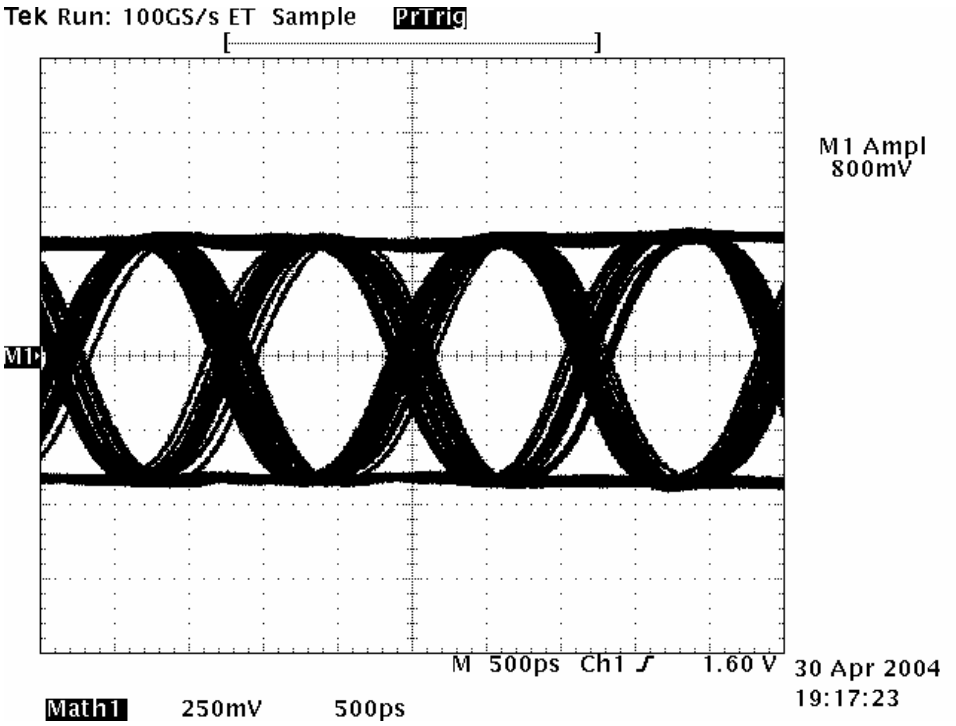


Fig. 5.26 The measured eye diagram of the transmitter at 840 Mb/s with package. The peak-to-peak jitter is 31.5 %. The transmitter is in the LVDS mode.

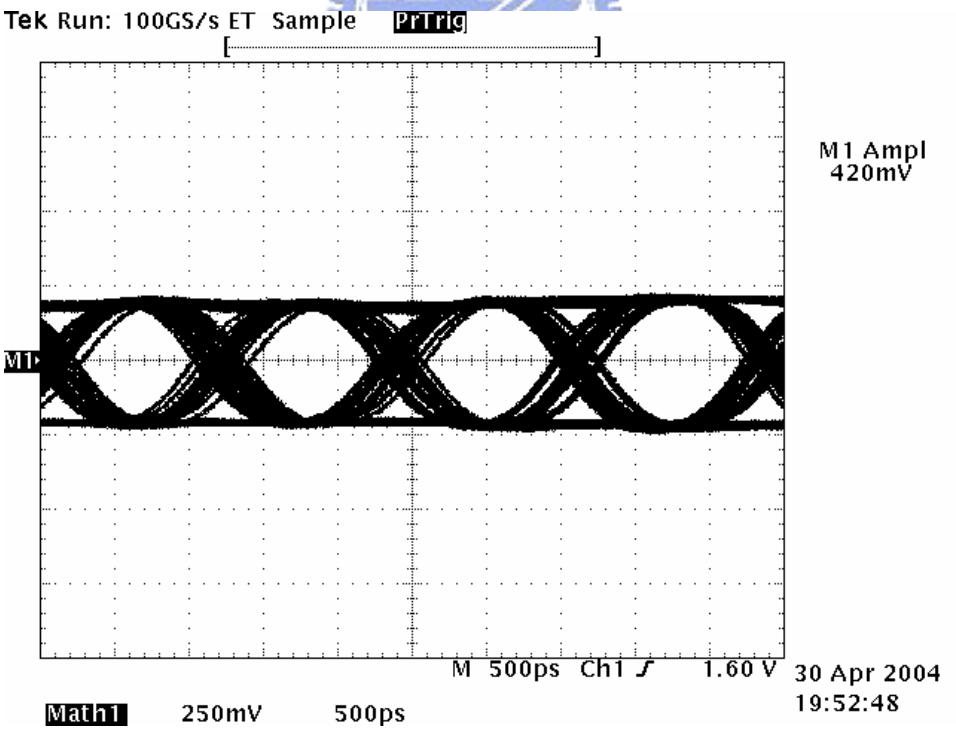


Fig. 5.27 The measured eye diagram of the transmitter at 840 Mb/s with package. The peak-to-peak jitter is 32.8 %. The transmitter is in the RSDS mode.

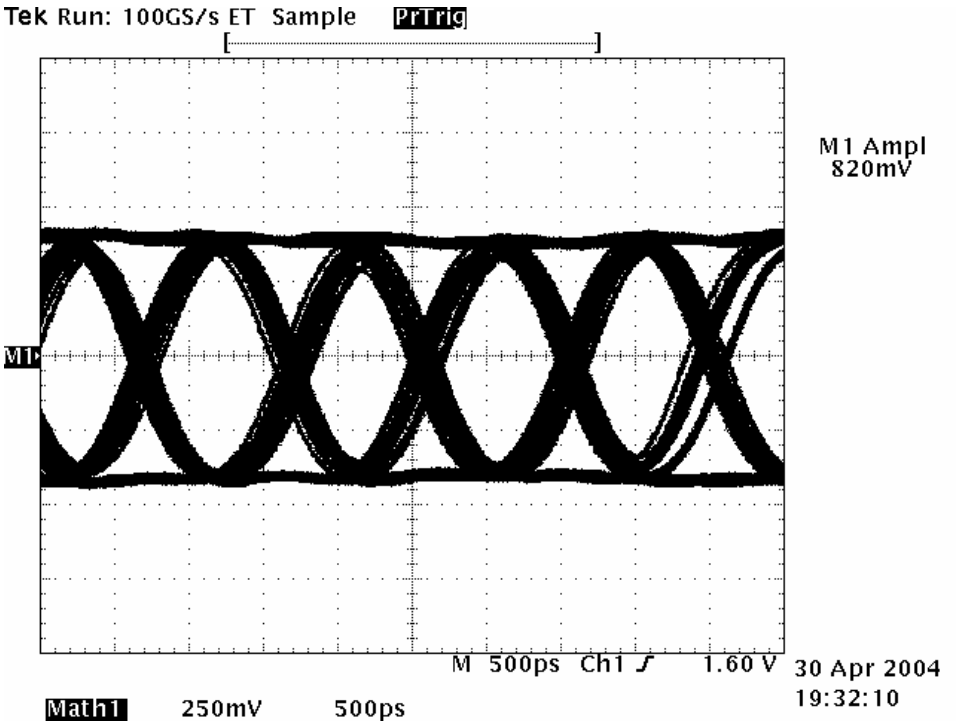


Fig. 5.28 The measured eye diagram of the transmitter at 1.05 Gb/s with package. The peak-to-peak jitter is 26.25 %. The transmitter is in the LVDS mode.

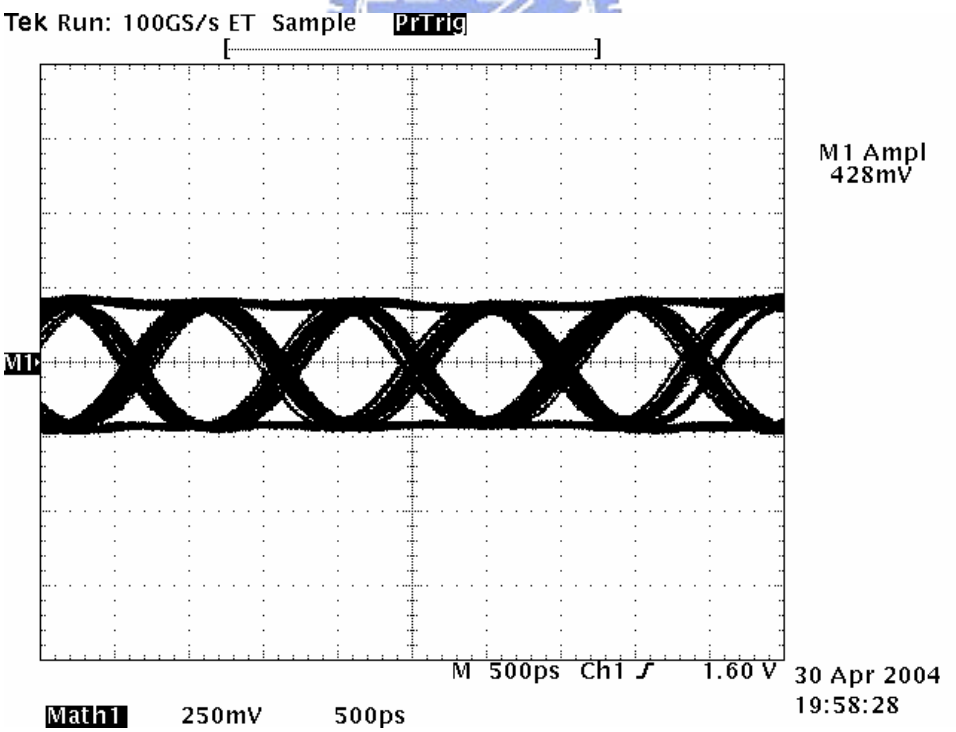


Fig. 5.29 The measured eye diagram of the transmitter at 1.05 Gb/s with package. The peak-to-peak jitter is 27.89 %. The transmitter is in the LVDS mode.

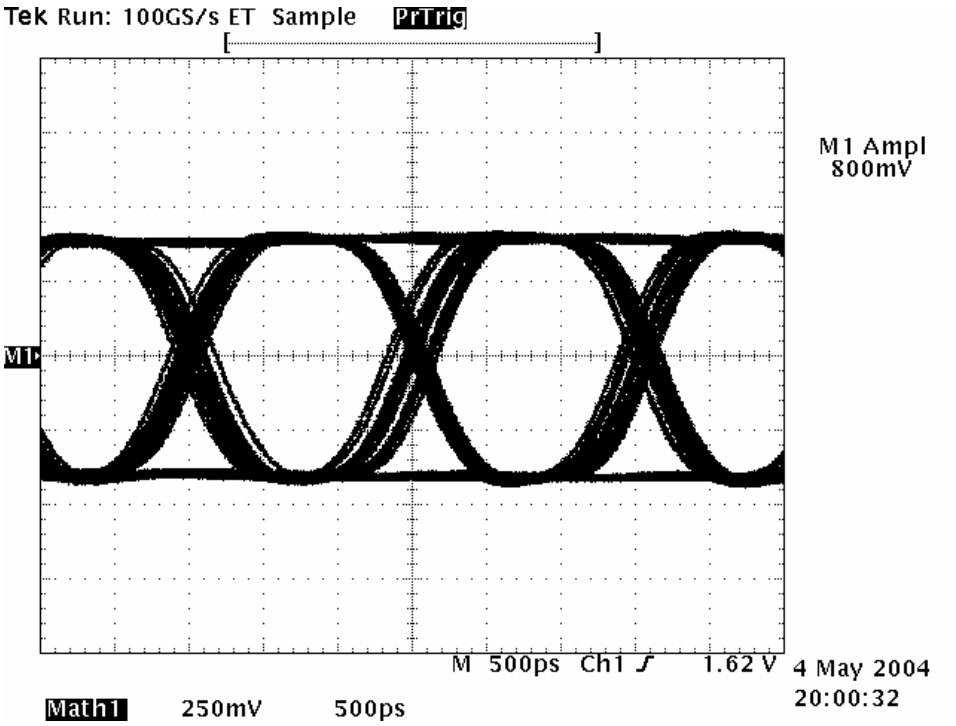


Fig. 5.30 The measured eye diagram of the transmitter at 700 Mb/s without package. The peak-to-peak jitter is 21.87 %. The transmitter is in the LVDS mode.

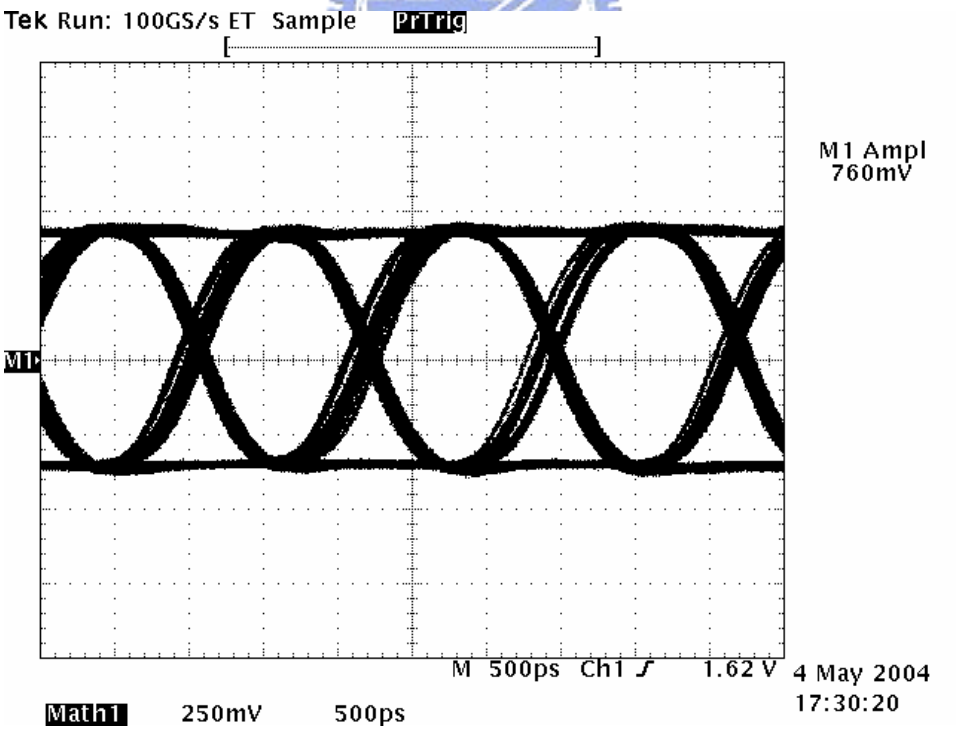


Fig. 5.31 The measured eye diagram of the transmitter at 840 Mb/s without package. The peak-to-peak jitter is 18.4 %. The transmitter is in the LVDS mode.

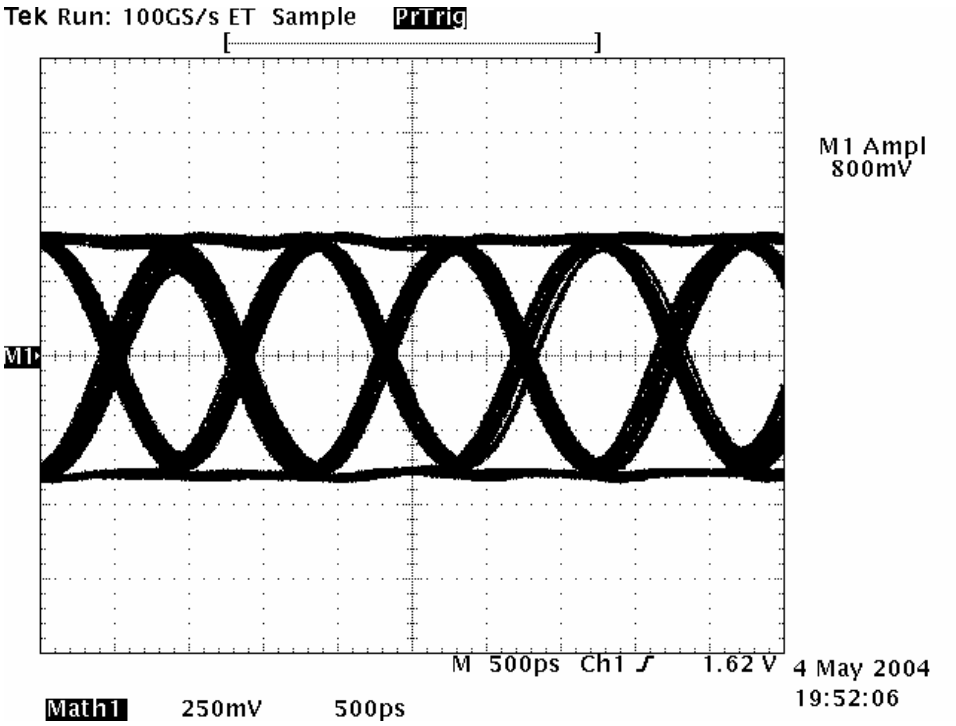


Fig. 5.32 The measured eye diagram of the transmitter at 1.05 Gb/s without package. The peak-to-peak jitter is 19.7 %. The transmitter is in the LVDS mode.

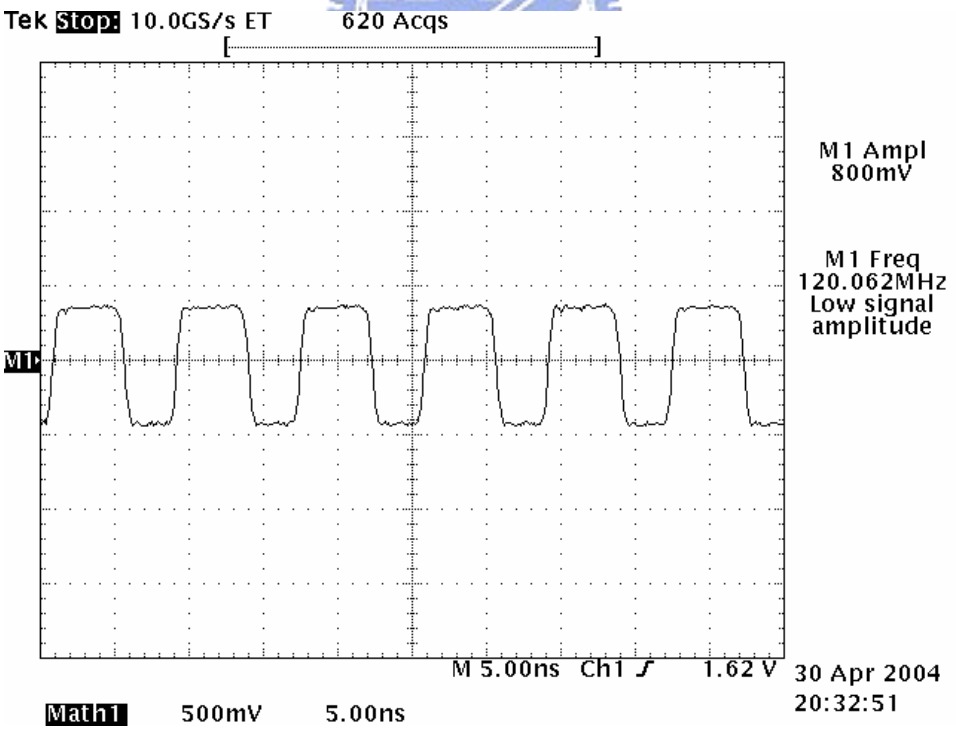


Fig. 5.33 The measured output clock of the PLL at 120 MHz with package. The duty cycle of the output clock is almost four to three.

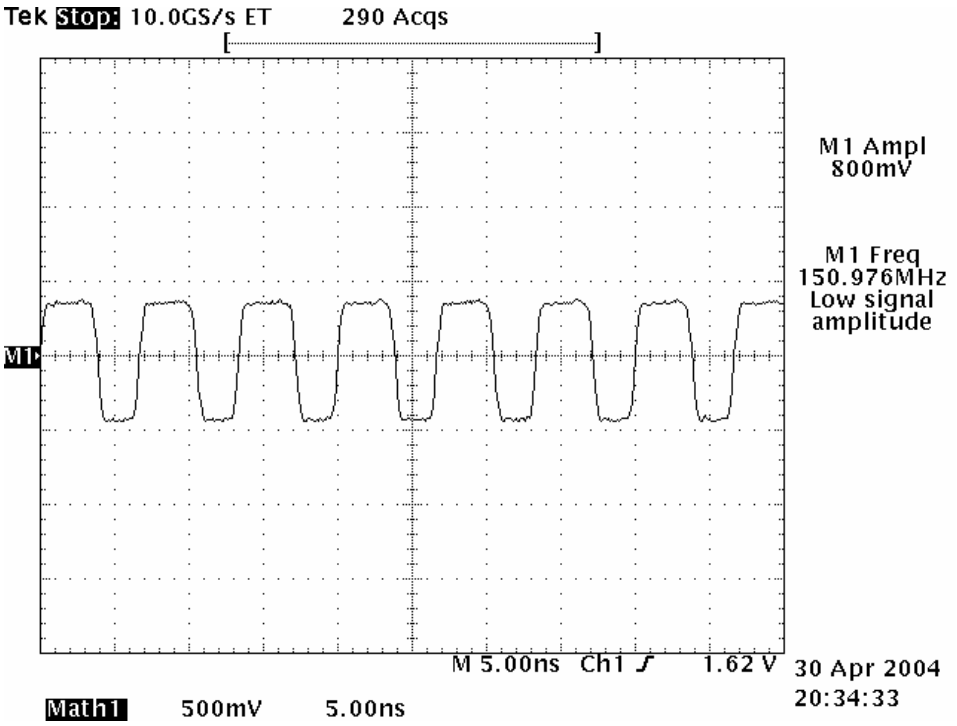


Fig. 5.34 The measured output clock of the PLL at 150 MHz with package. The duty cycle of the output clock is almost four to three.

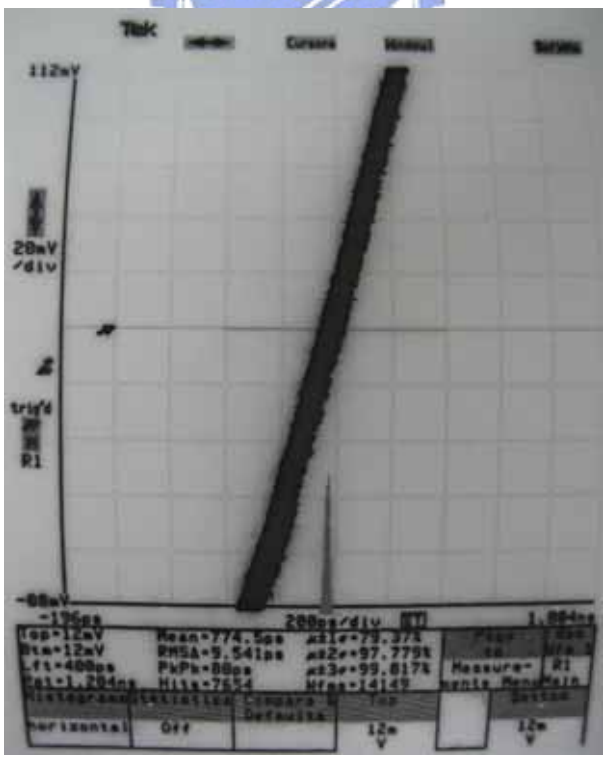


Fig. 5.35 The jitter histogram of the PLL output clock at 120 MHz. The long term peak-to-peak jitter is 88 ps.

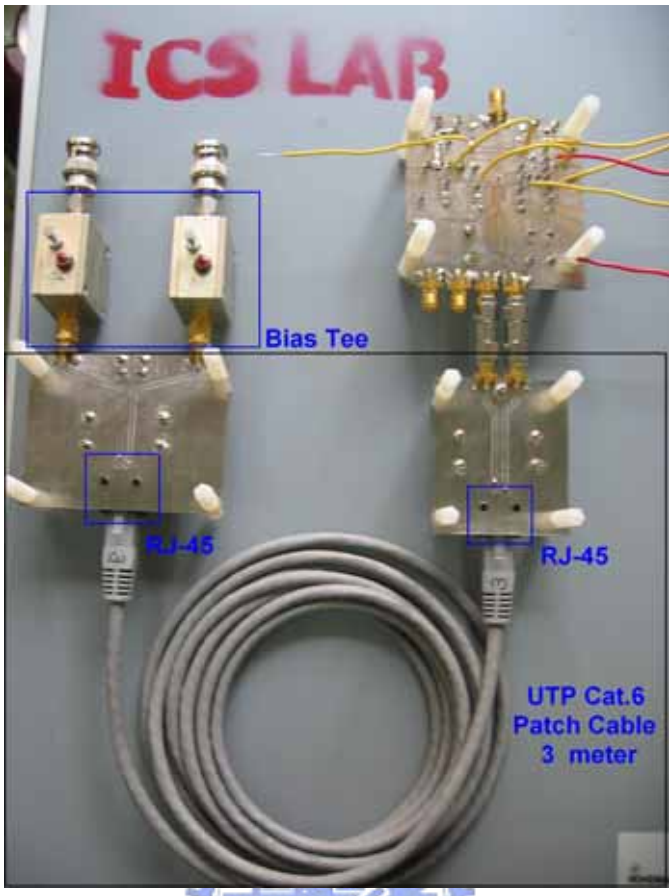


Fig. 5.36 The measurement setup of the transmitter with a 3-meter long UTP Cat.6 line.

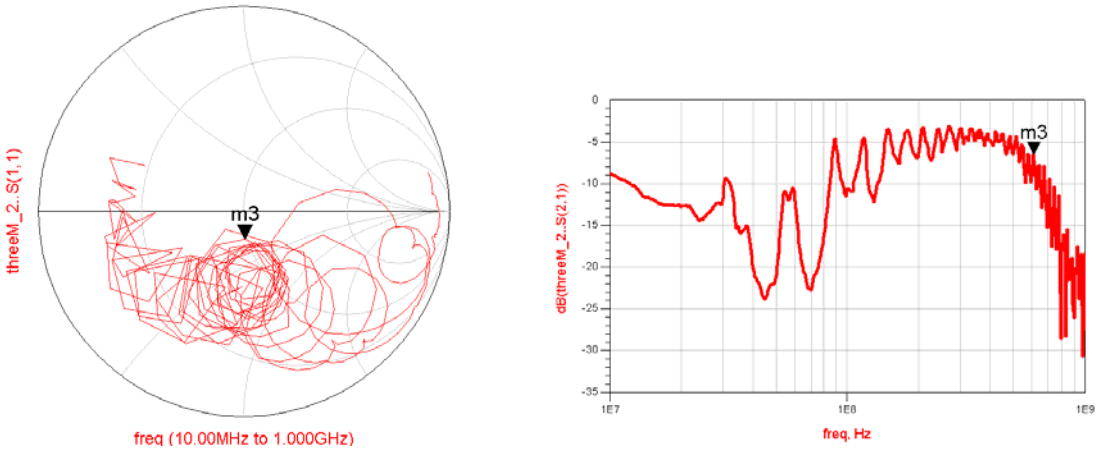


Fig. 5.37 Measurement of the 3-meter long UTP Cat.6 line with two termination boards.

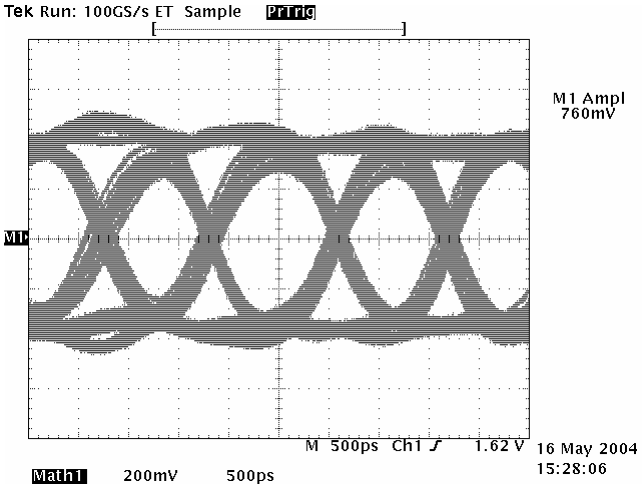


Fig. 5.38 The eye diagram of the transmitter at 840Mb/s with 1-m UTP Cat.6 line.

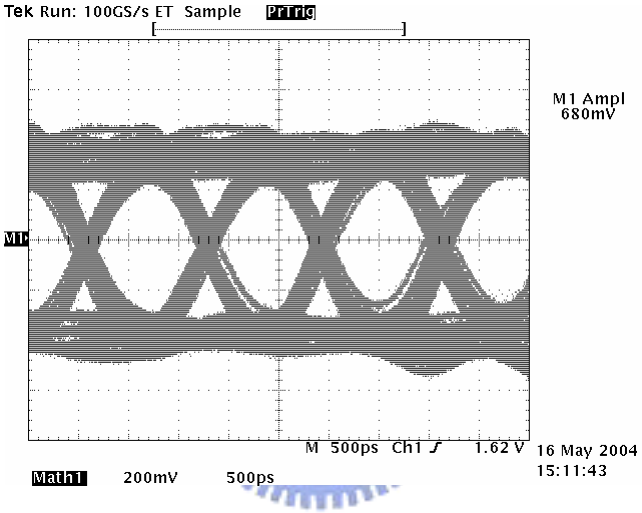


Fig. 5.39 The eye diagram of the transmitter at 840Mb/s with 2-m UTP Cat.6 line.

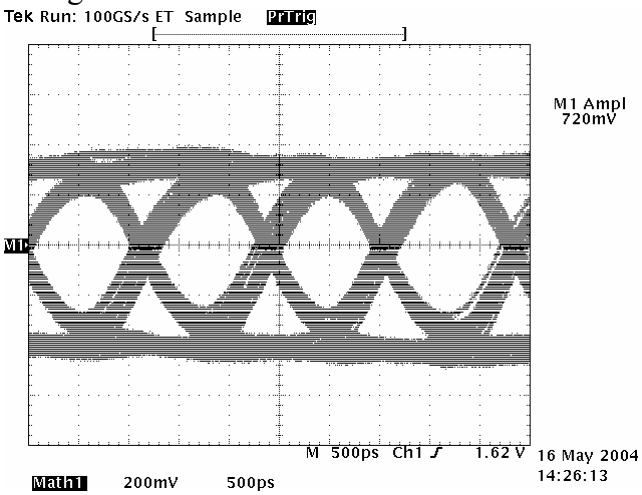


Fig. 5.40 The eye diagram of the transmitter at 840Mb/s with 3-m UTP Cat.6 line.

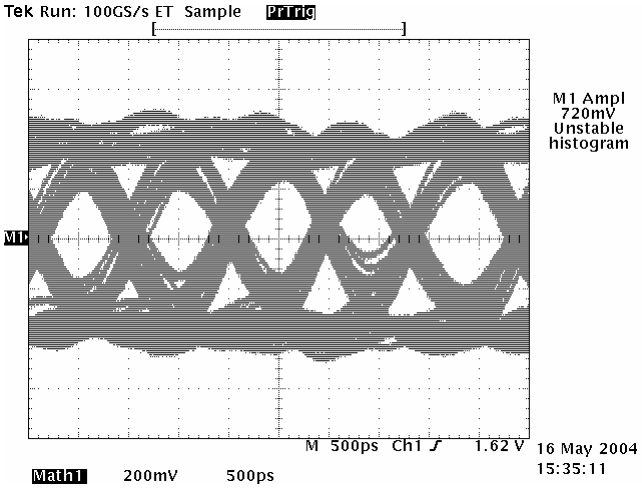


Fig. 5.41 The eye diagram of the transmitter at 1 Gb/s with 1-m UTP Cat.6 line.

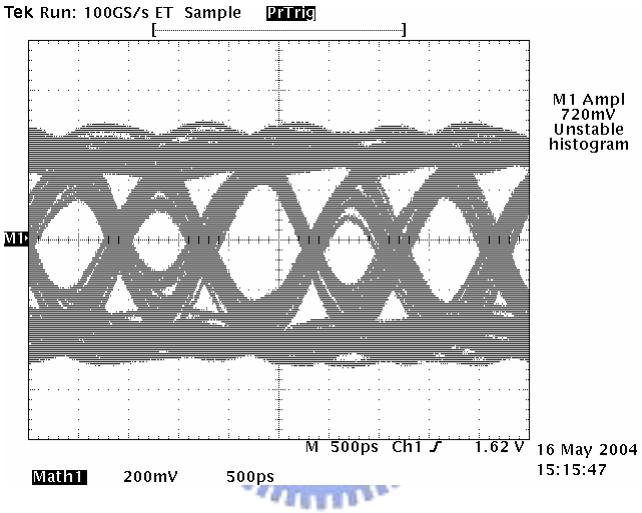


Fig. 5.42 The eye diagram of the transmitter at 1 Gb/s with 2-m UTP Cat.6 line.

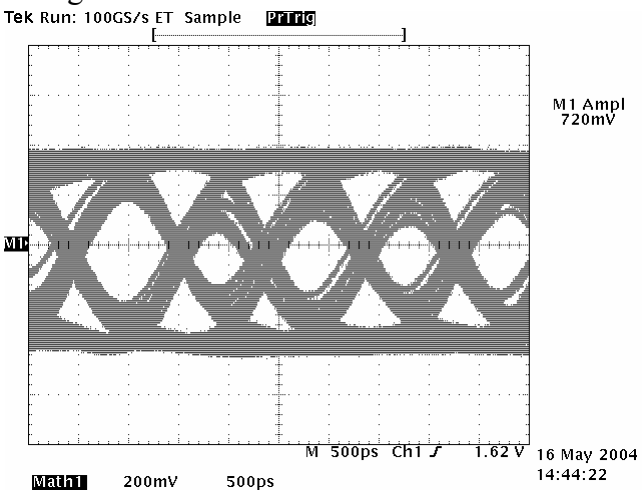


Fig. 5.43 The eye diagram of the transmitter at 1 Gb/s with 3-m UTP Cat.6 line.

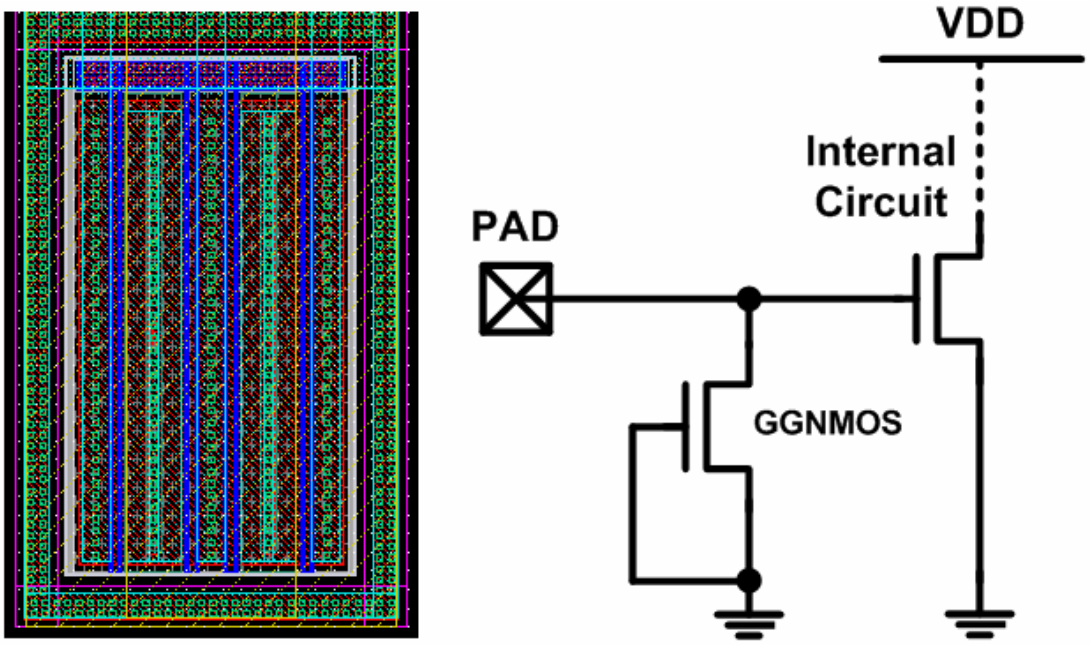


Fig. 5.44 The layout and schematic of the ESD protection circuit (GGNMOS).

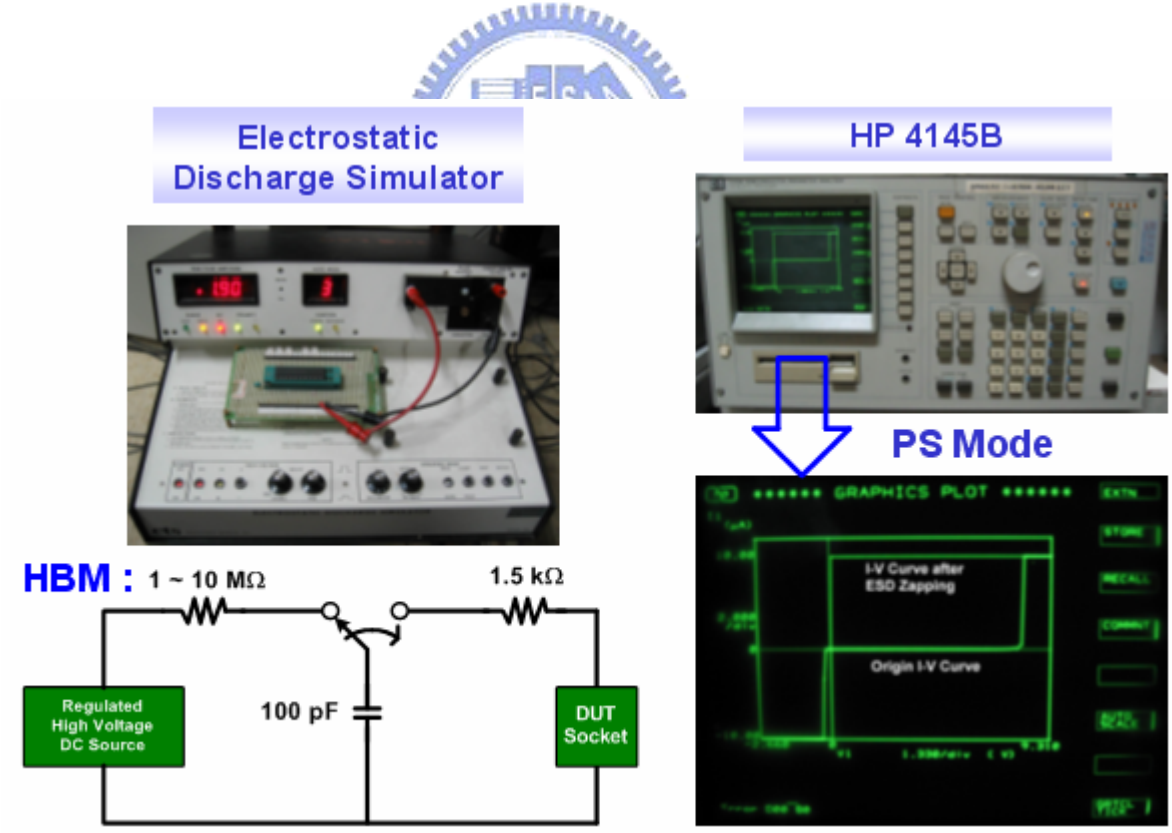


Fig. 5.45 The measurement setup of the ESD testing. The ESD testing model is the human body model (HBM).

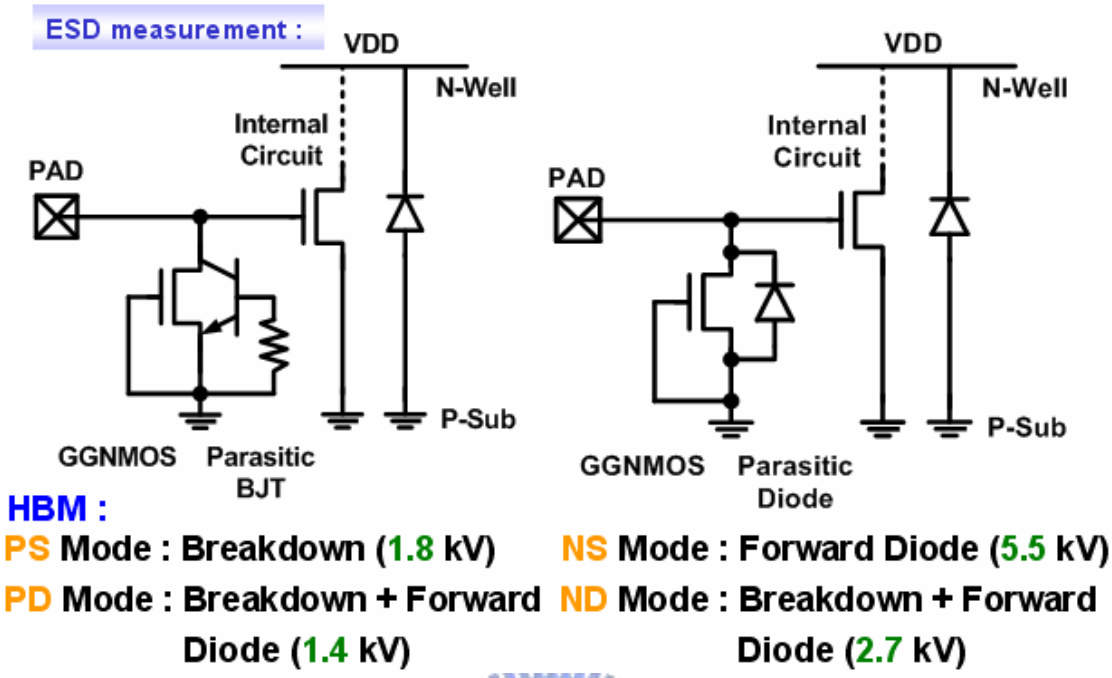


Fig. 5.46 The measurement results of the ESD testing.

Chapter 6

Summary and Future Works

6.1 SUMMARY

In the chapter 2, detail DC specifications of the LVDS and RSDS standards are discussed. LVDS stands for Low Voltage Differential Signaling and RSDS stands for Reduced Swing Differential Signaling. Both technologies have been developed to provide the high-speed and low-power interface applications which can be used in variety aspects. One of the applications is in the flat panel display systems which is the main issue in this thesis.

In the chapter 3, a phase-locked loop has been implemented in a 0.25-μm 1P5M CMOS process and the power supply is 2.5 V. The PLL has ten different output phases which are 200 MHz. The tuning frequency of the PLL is measured from 80 MHz to 360 MHz. The main application of the designed PLL is to perform the parallel-to-serial conversion with a multiplexer which is used in a transmitter. According to the measured jitter of the PLL, it is good enough to be employed in the transmitter to have better performance.

In the chapter 4, three I/O buffers have been fabricated in a 0.25-μm 1P5M CMOS process and the power supply is 3.3 V. These I/O buffers are fully compatible with both LVDS and RSDS standards. The data rate of the output buffers are tested up to 1.2 Gb/s which can support the UXGA (1600 × 1200 pixels) resolution of the flat panel displays. The data rate of the input buffer is tested up to 840 Mb/s. The output buffer can be embedded in the transmitter which is discussed in the chapter 5.

In the chapter 5, a transmitter which converts 28 bits of parallel TTL data into four LVDS or RSDS data streams plus one clock data stream has been implemented in a 0.25-μm 1P5M CMOS process and the power supply is 3.3 V. The PLL in the transmitter has seven different clock phases in order to perform parallel-to-serial conversion of incoming data. The data rate of the transmitter is tested up to 1.05 Gb/s which can support the SXGA (1280 × 1024 pixels) resolution of the flat panel displays.

6.2 FUTURE WORKS

Although the functions of the designed circuits in this thesis are all verified, there are still many drawbacks needed to be improved. First is that new proposed circuit technologies should be employed in the transmitter in order to reduce the jitter of the measured eye diagrams. Second is to design pre-emphasis circuit in the transmitter in order to have better transmission qualities through connecting materials. Models of transmission lines and packages should also be measured and modeled. Third is to keep on studying the architecture of receiver such as 3x-oversampling in order to complete the whole transceiver function [24].

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簡歷

姓　　名：莊凱嵐

學　　歷：

台灣省立台南第一高級中學　　(84年9月~87年6月)

國立中央大學電機工程學系　　(87年9月~91年6月)

國立交通大學電子研究所碩士班　　(91年9月~93年6月)

研究所修習課程：

類比積體電路 I	吳介琮教授
類比積體電路 II	吳介琮教授
數位積體電路	陳巍仁教授
積體電路設計實驗 I	李鎮宜教授
積體電路設計實驗 II	李鎮宜教授
積體電路之靜電放電防護設計特論	柯明道教授
數位通訊	桑梓賢教授

永久地址：台南市西區藥王里 11 鄰大福街 15 巷 8 號

Email： klchuang.ee91g@nctu.edu.tw

u3470627@cc.ncu.edu.tw

m9111588@alab.ee.nctu.edu.tw