國立交通大學

電子工程學系　　電子研究所碩士班

碩 士 論 文

低溫複晶矽玻璃基板上之
液晶顯示器驅動電路設計

On-Glass Driving Circuits Design for LCD in LTPS Technology

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摘要

本論文利用低溫複晶矽的製程，將液晶顯示器驅動電路設計並實現在玻璃基板上。液晶顯示器的驅動電路主要分為閘級驅動電路及源級驅動電路；其中閘級驅動電路包含移位暫存器、電位轉換器和輸出緩衝器；而源級驅動電路則是由移位暫存器、閂鎖器、電位轉換器、數位對類比轉換器及輸出電壓緩衝器組成。

本論著重於將源級驅動電路實現在玻璃基板上。由於液晶顯示器具有高負載的特性，所以在輸出電壓緩衝器的部分，本論文設計了兩種具有驅動高負載功能的電路，分別為具有高旋轉率和低功率消耗的 B 類電壓輸出緩衝器。此外，也針對了低溫複晶矽的臨界電壓漂移問題，設計了一個具有臨界電壓補償的輸出緩衝器；在數位對類比轉換器的方面，因為液晶之穿透率和偏壓電位成一非線性關係，所以本論文也設計了一個具有珈瑪修正功能的數位對類比轉換器來補償這效應；在電位轉換器的部分，本論文則是以基底加偏壓的方式，並利用台積電 0.35-μm CMOS 的高壓製程，模擬且分析在不同偏壓下其操作速度和功率消耗的關係。而以上的電路皆以統寶的 6-μm 或 3-μm 低溫複晶矽製程實現。

最後，為了滿足高解析度的液晶顯示器，源級驅動電路在資料的接收端上，常會使用 RSDS 的規格來做傳輸介面，以增加其資料的傳輸速度並克服電磁干擾的效應，所以本論文也嘗試利用統寶的 6-μm 低溫複晶矽製程，設計一 RSDS 接收端的基本驅動電路。

On-Glass Driving Circuits Design for LCD in LTPS Technology

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ABSTRACT

In this thesis, on-glass driving circuits for LCD are designed and implemented in low temperature poly silicon (LTPS) technology. The driving circuits for LCD are divided into two parts, gate driver and source driver. Gate driver includes shift registers, level shifters, and output buffers. Source driver is composed of shift registers, latches, level shifters, a digital to analog converter, and output buffers.

The implement of the on-glass source driver is the focus in this thesis. First, two circuits, which are slew rate enhancement output buffer and low power class-B output buffer, are designed to drive the heavy loading of LCD. Second, a threshold voltage compensation circuit is proposed to solve the drift of the threshold voltage in LTPS process. Third, due to the nonlinear relationship between transparency and voltage across liquid crystal, a digital to analog converter with gamma correction is adopted to compensate this effect. Finally, level shifters using body-bias technique are also proposed. According to TSMC 0.35-μm CMOS HV process, the operational speed and power consumption of level shifters in different body-bias voltages are simulated and analyzed. All of above circuits have been implemented in TOPPOLY 6-μm or 3-μm LTPS process.

Moreover, in order to satisfy the high resolution LCD, source driver usually employs the specification for reduced swing differential signaling (RSDS) as the transition interface in the data receiver. Besides, the application of the specification for RSDS will increase the data transition speed and reduce the electric magnetic interference (EMI) effect. So, a fundamental RSDS receiver in TOPPOLY 6-μm LTPS process is also included in this thesis.

誌謝

首先，感謝我的指導老師柯明道教授，在碩士這兩年的求學過程中，不厭其煩的指導我，讓我不僅學到如何有效率的做研究，更學會如何嚴謹的看待問題。

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黃如琳

國立交通大學

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CHAPTER 1

INTRODUCTION

1.1 Motivation

With information technology (IT) industry progressing, LCD (liquid crystal display) becomes the central feature of many consumer products. The main consideration of LCD performance is high resolution, wide view-angle, and high contrast ratio, etc. Besides, a current trend of LCD is lower power, light weight, and small volume. Based on the above descriptions, some fundamental requirements for LCD are listed below as a reference:

- Full color (8 bits/color).
- High resolution (200 dots per inch).
- Large panel size (960 × 1100 mm^2).
- Wide view angle (180° both axes).
- High contrast ratio (200:1).
- Light weight (2.5g/cm^2).
- Small volume (0.5 mm).
- Low power.

Furthermore, LTPS (low temperature poly silicon) technology is the novel technology specific for LCD application. The manufacture of LTPS is apparently more complicated than amorphous poly silicon technology, but LTPS TFT (thin film transistor) has 100 times high mobility than amorphous silicon (α-Si) TFT and can carry out CMOS process on the glass substrate. Some advantages for LTPS over

amorphous poly silicon are shown below:

- **Slimmer peripheral dimension**: Capability for integrating driving circuit on glass substrate is better, which means slimmer peripheral dimension and low cost.
- **High aperture**: The LTPS TFT device with high mobility can achieve a short charging time by small size and so that it contributes more pixel area to light transition.
- **Compatible for OLED** (organic light emitting diode): The LTPS TFT device with high mobility can provide high-current driving capability for OLED application.
- **Compact module**: Less PCB (printed circuit board) area is required due to driver integrated on glass.

According to above discussion, it can see that the fabrication cost will gradually be lowed and SOP (system on panel) will be implemented step by step in the future. Moreover, LTPS technology is compatible with OLED, which is another promising display device. Therefore, design of driving circuit for LCD in LTPS technology is worthy expecting in the future.

1.2 Thesis Organization

In this thesis, an on-glass data driver is designed and implemented to satisfy the specification for LCD in TOPPOLY 6-μm LTPS process. Furthermore, a fundamental RSDS receiver in TOPPOLY 6-μm LTPS process has also been included and discussed in this thesis. And the main point of each chapter is described in below.

In chapter 2, some background of liquid crystal display is discussed.

In chapter 3, a slew rate enhancement and a low power class-B output buffer are designed. Besides, in order to overcome the variation of V_{TH} (threshold voltage) in output buffer, an output buffer with V_{TH} compensation is also proposed.

In chapter 4, a 6-to-64 gray level DAC with gamma correction are proposed and implemented to solve the nonlinear-transparency characteristics in liquid crystals.

In chapter 5, the function of a TFT device with body bias is verified. Furthermore, some modified level shifters by body bias technique are also proposed and analyzed in this chapter.

In chapter 6, a fundamental RSDS receiver is also included to increase the data transition speed and to reduce the electric magnetic interference (EMI) effect in data transition.

In chapter 7, some conclusions and future works are summarized.

CHAPTER 2

BACKGROUND OF LIQUID CRYSTAL DISPLAY

2.1 Liquid Crystal Display Structure

2.1.1 Liquid Crystal

Liquid crystal is a phase of matter whose order is intermediate between that of a liquid and that of a crystal. The phase variation of liquid crystal in different temperature is shown in Fig. 2.1. And the molecules are typically rod-shaped organic moieties about 25 Angstroms in length and their ordering is a function of temperature [1]-[3]. In addition, the molecular orientation can be controlled with applying various electric fields.

According to the way that liquid crystals are formed, it can be distinguished into thermotropic and lyotropic liquid crystals. For lyotropic liquid crystals, the phases formed depend upon the nature of the molecules involved, the temperature, and the type of solvent. In themotropic liquid crystals, the phase formed is characteristic of the temperature. But, if base on the arrangement of liquid crystal molecules, liquid crystals can be divided into three types — smetcic, nematic and cholesteric.

Because the twist of liquid crystals can be controlled by the electric field that is applied across it, liquid crystals are used as a switch that passes or blocks the light. TN (twisted nematic) and STN (super twisted nematic) are the terms used to describe two types of liquid crystal displays. TN displays have a twist of 90 degrees or less. And almost all active matrixes have a 90 degree twist. As the name implies, STN displays have a twist that is greater than 90 but less than 360 degrees. Currently most

STN displays are made with a twist between 180 and 240 degrees. The higher twist angle causes steeper threshold curve which puts the on and off voltages closer together. As a result, it is usually applied in passive matrixes. And the transparency of TN and STN in different voltage is illustrated in Fig. 2.2.

2.1.2 Structure of LCD

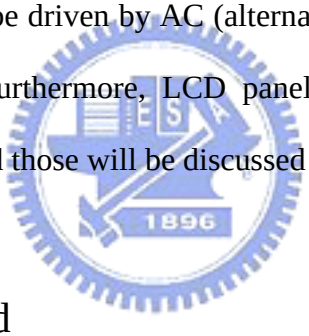
The cross section of LCD with polarizer, glass, LC (liquid crystal) material, and color filter is shown in Fig. 2.3. Polarizer can be divided into top polarizer and bottom polarizer. The top polarizer can polarize the incident light from random polarization into unique one. Before electric field is applied on the electrodes, the liquid crystals are aligned in a twist pattern. The path of light is then changed with the twist pattern of the liquid crystals. The bottom polarizer is aligned opposite of the top polarizer. Consequently, when the light reaches the bottom polarizer, they will align with each other and the light can pass through, which is illustrated in Fig. 2.4(a). On the contrary, if the electric is applied on the electrode, the liquid crystals will turn to the same direction. Then, the light can not pass the bottom polarizer, which is shown in Fig 2.4(b). In this case, it is usually called normally white.

The multiple step-and-repeat images of the LCD electrode on glass substrate are created by precise photolithography technique. TFT glass has so many TFT as the number of pixels while color filter glass has color filter that generates color. Three primary colors, red, green, and blue, can generate more than million kinds of color in different degrees of light.

2.2 Driving Method in LCD

2.2.1 Gamma Correction

Gamma correction of liquid crystal displays involves the pixel nonlinear voltage and the light modulation characteristics, so that equal changes in digital input must correspond to equal changes in light transmission. Base on this description, the relationship between digital input codes and input voltage across liquid crystals can be shown in Fig. 2.5(a). In this way, the smooth curve between digital input code and light transmission rate can be achieved in Fig 2.5(b). Moreover, there are something should be emphasized. In Fig 2.5(a), the curve is symmetrical to the input voltage axis. This is because that the permanent deflections of liquid crystal molecules will occur if the DC (direct current) stress given on the LCD panel sustains a long period. As a result, the LCD panel should be driven by AC (alternating current) mode to eliminate the defect on LCD panel. Furthermore, LCD panel driven by AC mode can be classified into many kinds, and those will be discussed in the following sections.



2.2.2 Driving Method

Liquid crystal molecules will be defected under a fixed voltage in a long period. Although the fixed voltage has vanished, the characteristic of the liquid crystals will be destroyed and the twist of liquid crystals can not change with electric field. Therefore, the electric field should be recovered every period to avoid the destruction of liquid crystals. When the frame picture is kept on the same gray level, the electric field across liquid crystals is divided into two electrodes — positive electrode and negative electrode. As electric field is higher than common mode voltage the electrode is called positive electrode, otherwise it is called negative electrode. By this way, the liquid crystal molecules will avoid defection in the fixed electric field. In term of above description, LCD panel can be principally composed of four types —

frame inversion, row inversion, column inversion, and dot inversion. They are listed in Fig. 2.6. Frame inversion is that all the adjacent pixels of the LCD panel have the same electrode. Row inversion and column inversion is that each adjacent column pixel and adjacent row pixel have the same electrode respectively. Finally, all the adjacent pixels of LCD panel have different electrode is called dot inversion. Dot inversion is the major driving method of LCD panel. By the opposite polarity of the voltage vertically and horizontally side by side to each pixel, dot inversion can reduce clustered DC voltage in the screen which may result image sticking and to reduce the screen flickering. No matter what methods the LCD panel will be driven, all the pixels will change polarity on the frequency of 60 Hz (16ms). In other word, the polarity of each pixel is alternating changed.

Based on the operational type of common mode voltage, the driving method can also be classified into direct driving and AC modulation driving. They are shown in Fig. 2.7 and Fig. 2.8 respectively. Direct driving method would keep its common voltage on a constant level. But, the common mode voltage of AC modulation driving method would change its polarity in turns. The characteristics of two driving methods are listed below:

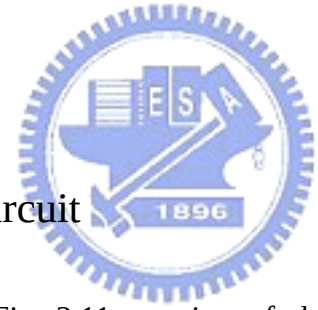
Direct driving method:

- Frame, row, column, and dot inversion are all available.
- Crosstalk and flicker can be eliminated.

- AC modulation driving method:
  - Frame and row inversion are available.
  - Low power dissipation in data driver.

2.3 Periphery Circuit Block

The periphery circuit blocks of LCD panel are composed of four parts — display panel, timing controller, scan driver and data driver. In Fig. 2.9 is the block diagram of the LCD panel driver circuits. Display panel is constructed of active matrixes and its structure layout is illustrated in the Fig. 2.10. The active matrixes are similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor on the pixels. Timing controller is responsible for transiting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. As soon as one voltage level of the scan lines rises, the RGB signals will be transited through the data driver. After a period, the voltage level of this scan line will be disabled and next scan line will act. All voltage levels of those scan lines will change in turn. As for scan driver and data driver, they will be further discussed in the following sections.

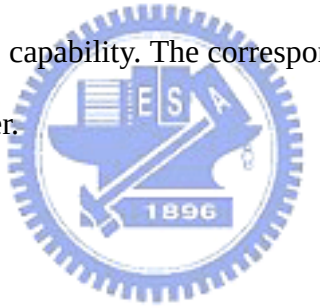


2.3.1 Scan Driver Circuit

Scan driver, shown in Fig. 2.11, consists of shifter register, level shifter, and output buffer. Shifter register is used to store digital input signals and transit them to the next stage according to timing clock. Because the turn-on voltage of active pixels is high, scan driver should drive the active pixels with a high voltage. The purpose of the level shifter is to convert the digital signals to a higher level voltage. Finally, since the scan lines can be modeled as RC (resister and capacitor) ladder shown in Fig 2.12, the output buffer should be used in the last stage. The output buffer is composed of inverter chain. The number of stages employed in the inverter chain depends on the RC ladder.

2.3.2 Data Driver Circuit

Data driver, shown in Fig. 2.13, mainly contains shifter register, data latch, level shifter, digital to analog converter and output buffer. Furthermore, the first three parts classify as digital architectures. The other two parts belong to analog architectures. Shifter register and data latch manage to transit and store the RGB signals. Also, the purpose of level shifter is the same as the one in scan driver. It is applied to translate the RGB signal to a higher level voltage. As implied by the name, digital to analog converter is used convert the digital RGB signal to analog gray level. Its structures can be divided into many types, and there will be much more detailed discussion in the following chapters. As for output buffer, its purpose is applied to drive active pixels into a desired gray level. The LCD panel usually has large loading, especially in larger panel display or higher resolution display. For this reason, the output buffer should enhance its own charge capability. The corresponding output buffer circuit will be described in the next chapter.



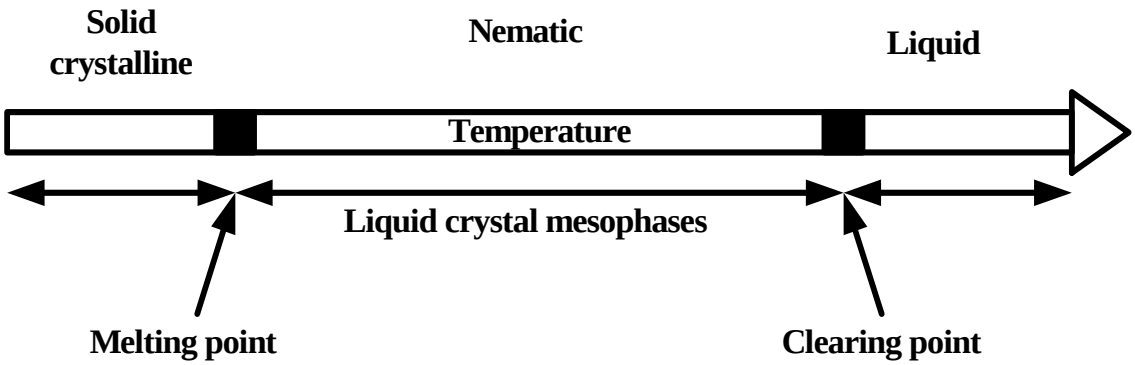


Fig. 2.1 Phase variation of liquid crystal in different temperature.

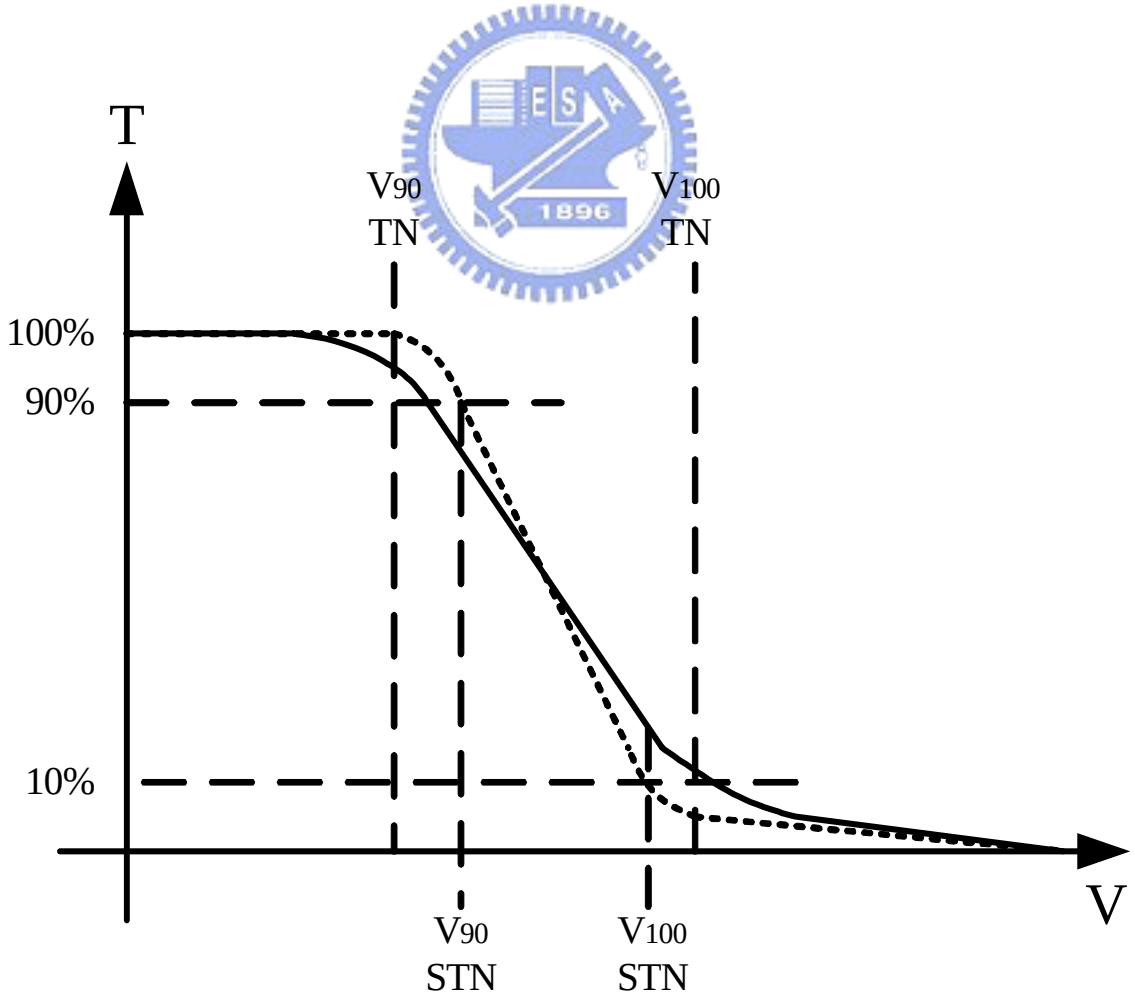


Fig. 2.2 Transparency of TN and STN in different voltage.

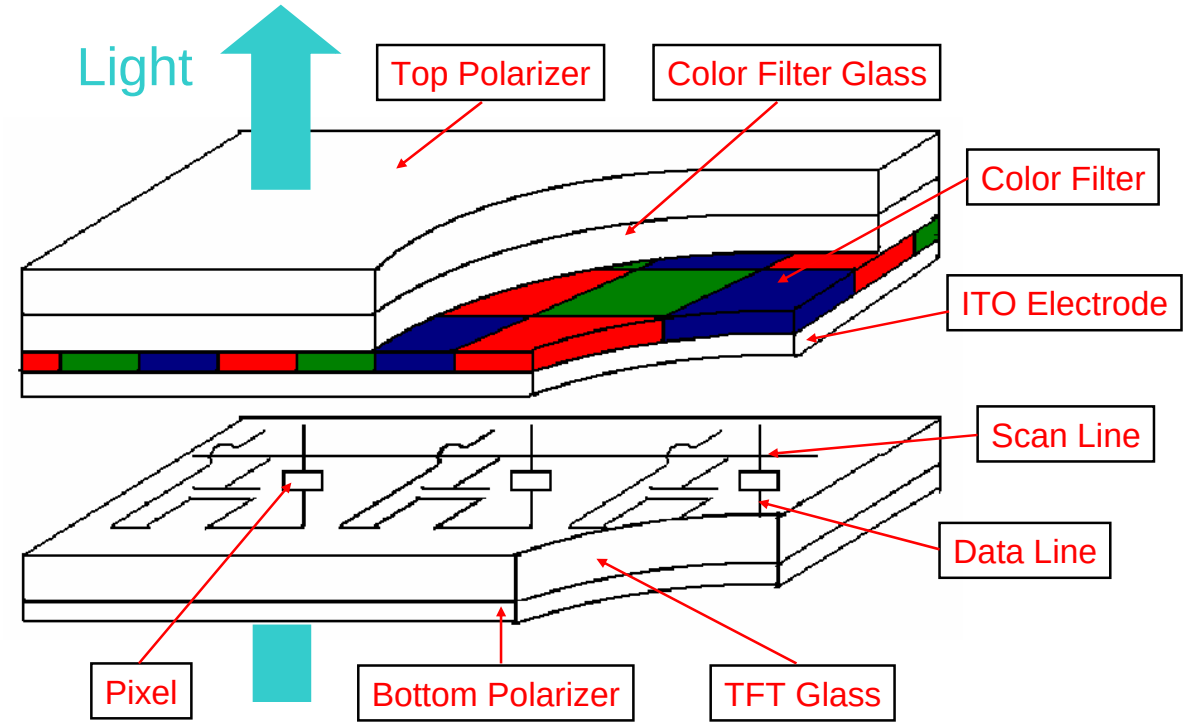


Fig. 2.3 Cross section of LCD module.

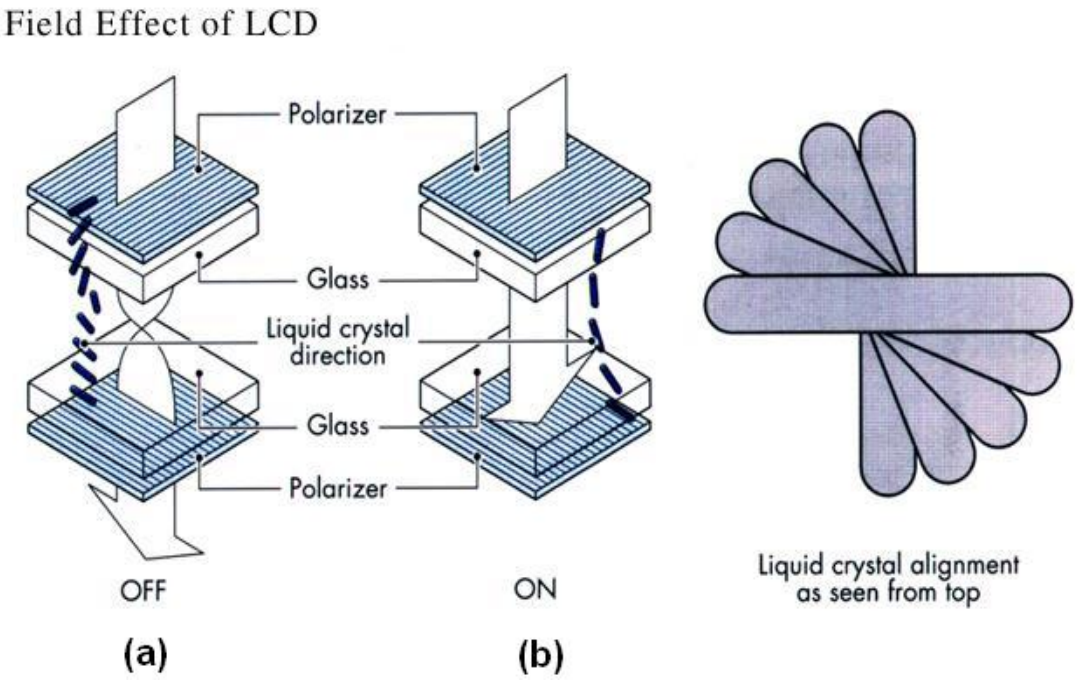


Fig. 2.4 The liquid crystal operates in normally white case: (a) light can pass and (b) light is blocked.

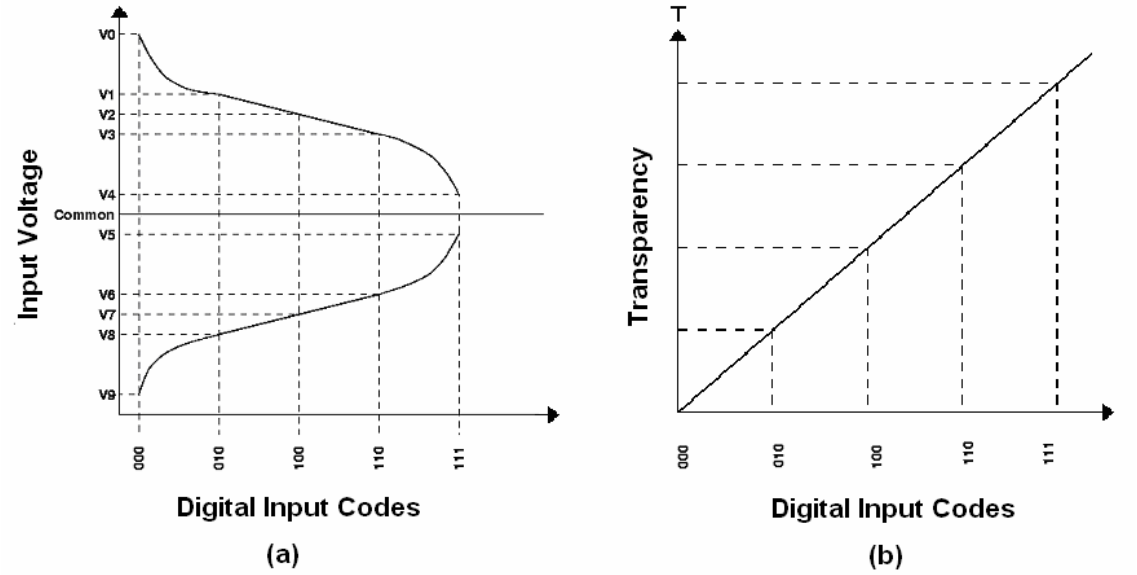
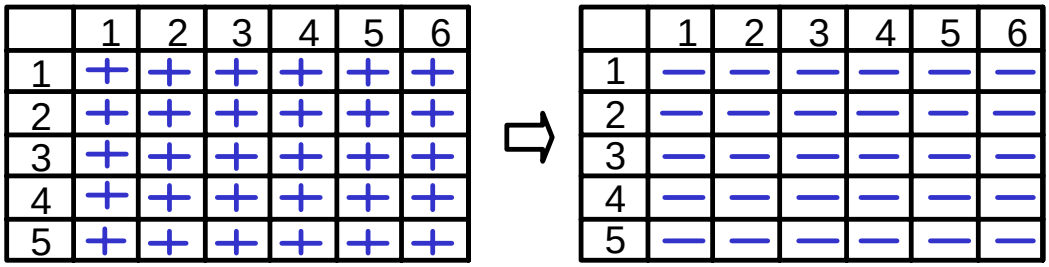
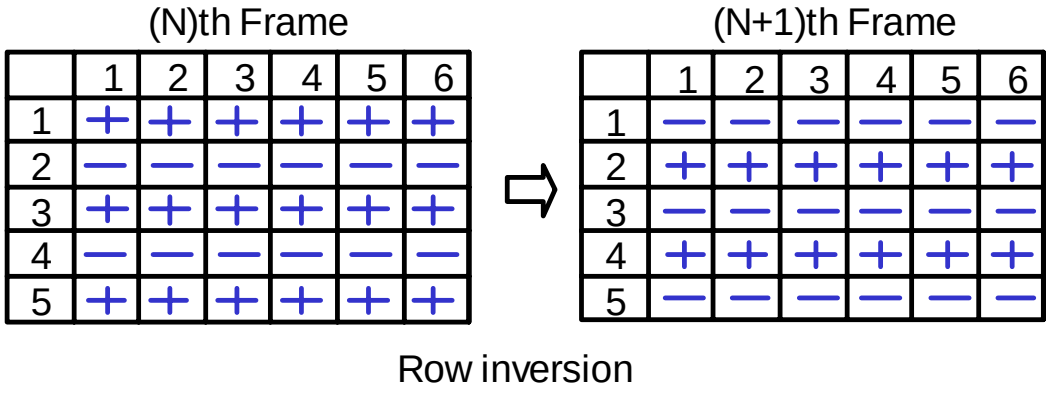


Fig. 2.5(a) The relationship between digital input codes and input voltage across liquid crystals and (b) the smooth curve between digital input codes and light transmission rate.





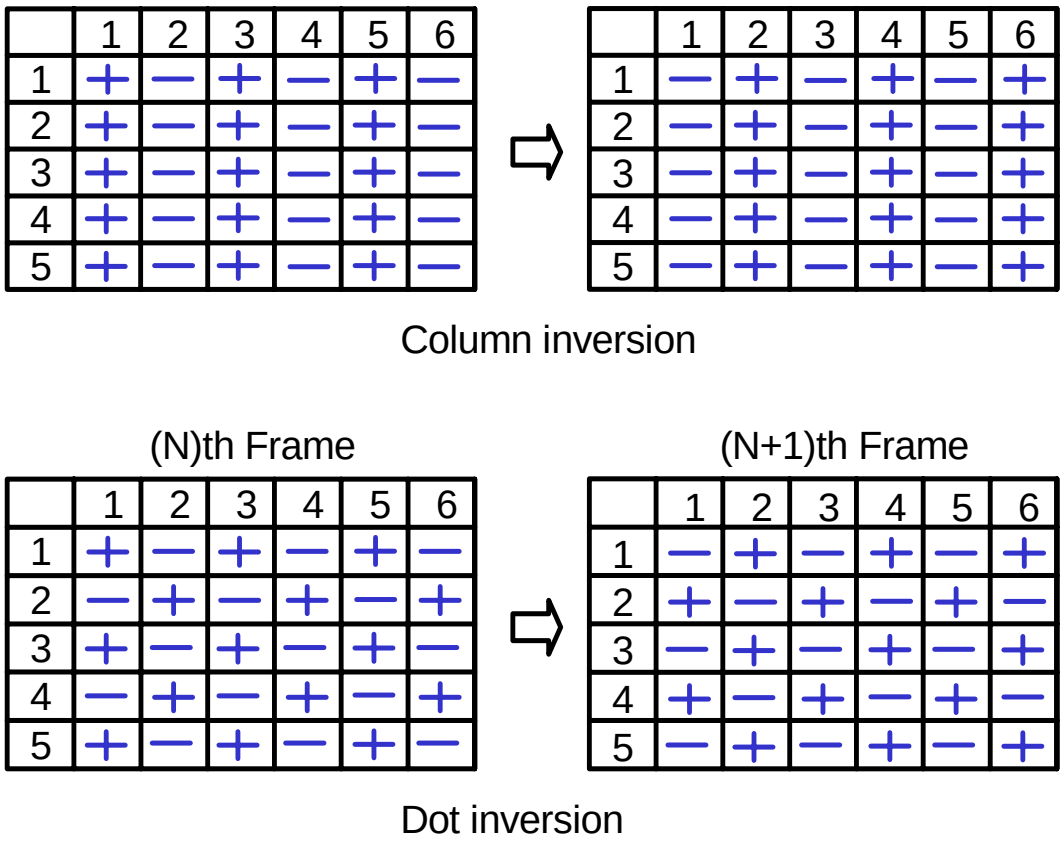


Fig. 2.6 Inversion of LCD panel.

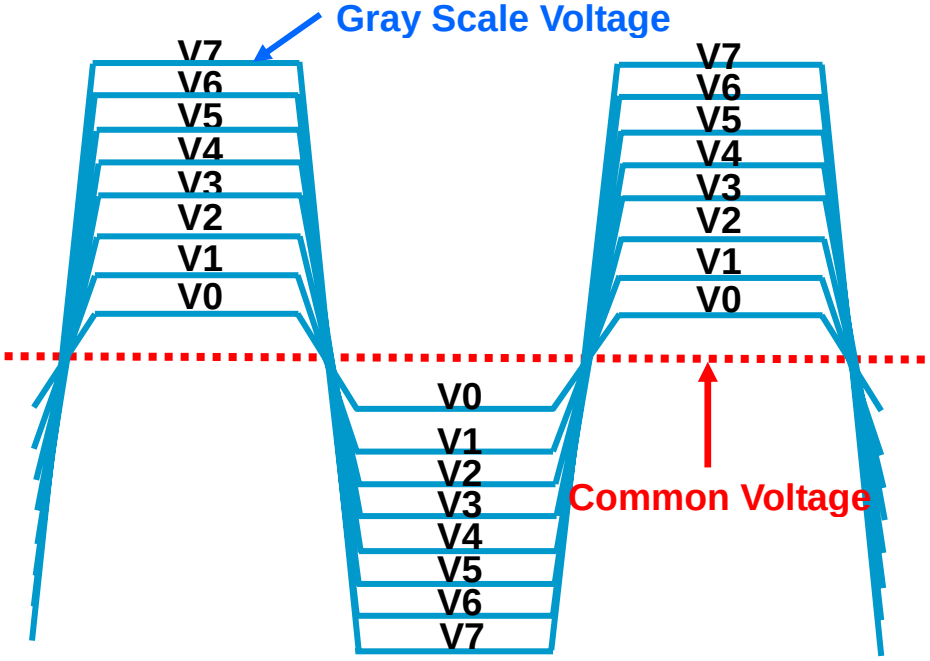


Fig. 2.7 The operational waveform of direct driving method.

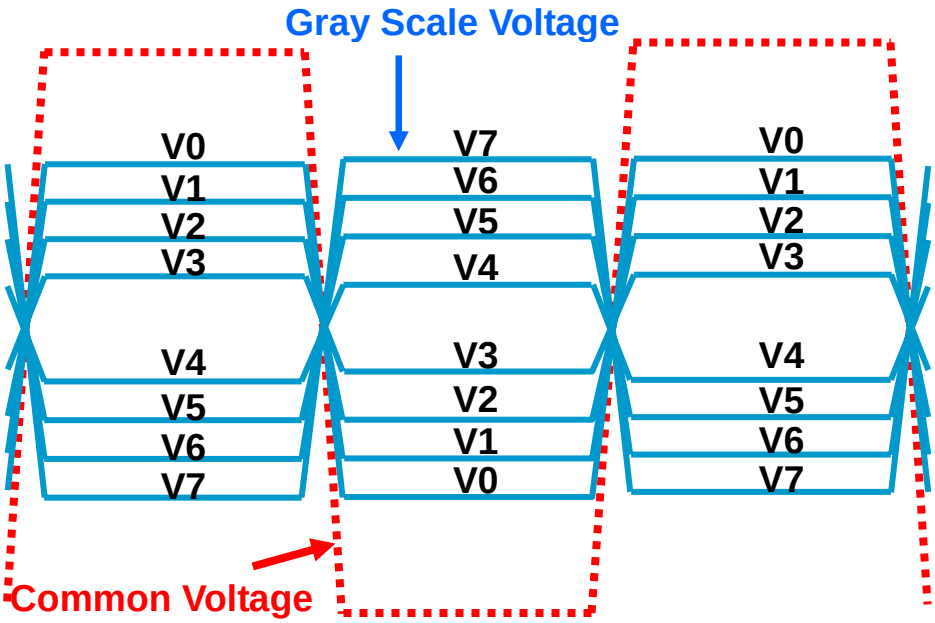


Fig. 2.8 The operational waveform of AC modulation driving method.

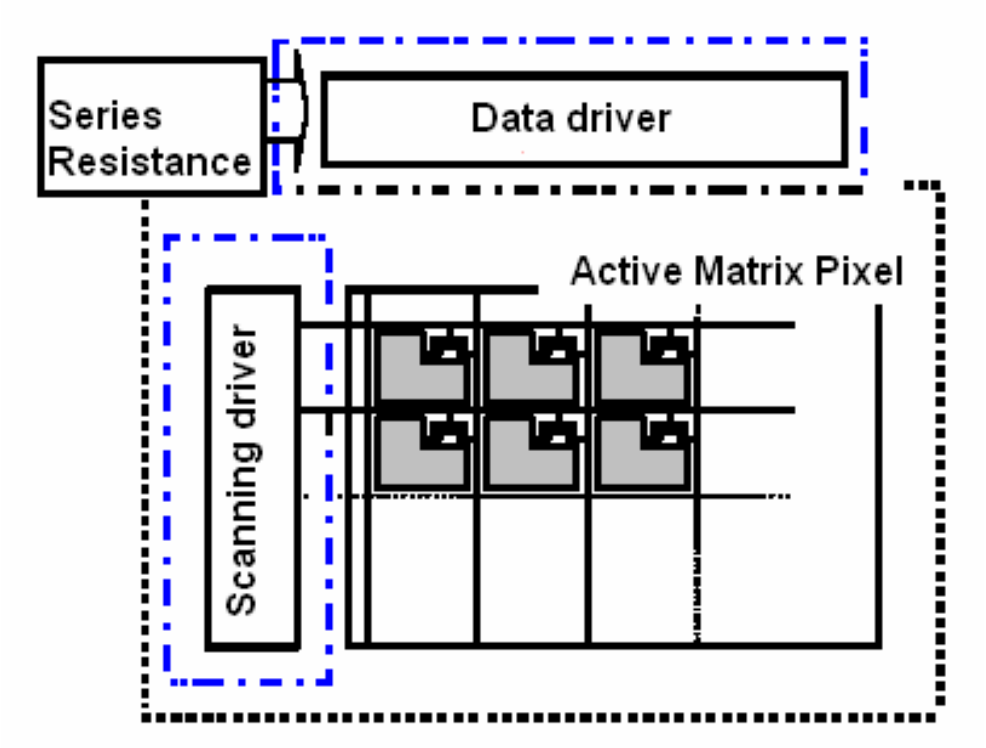


Fig. 2.9 Block diagram of the LCD panel driver circuits.

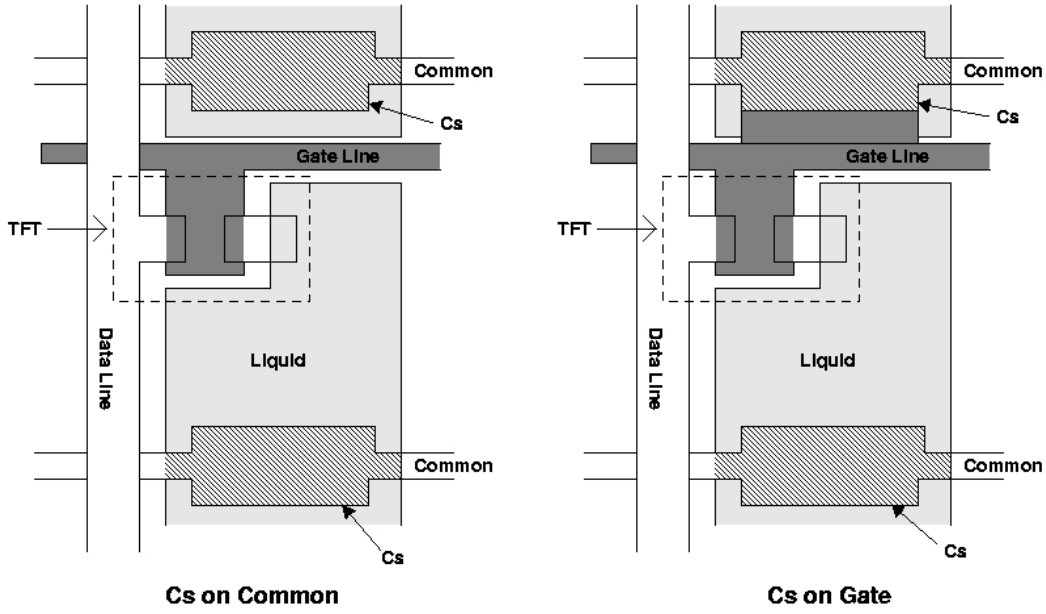


Fig. 2.10 The pixel layout structure of active matrix cell on LCD panel.

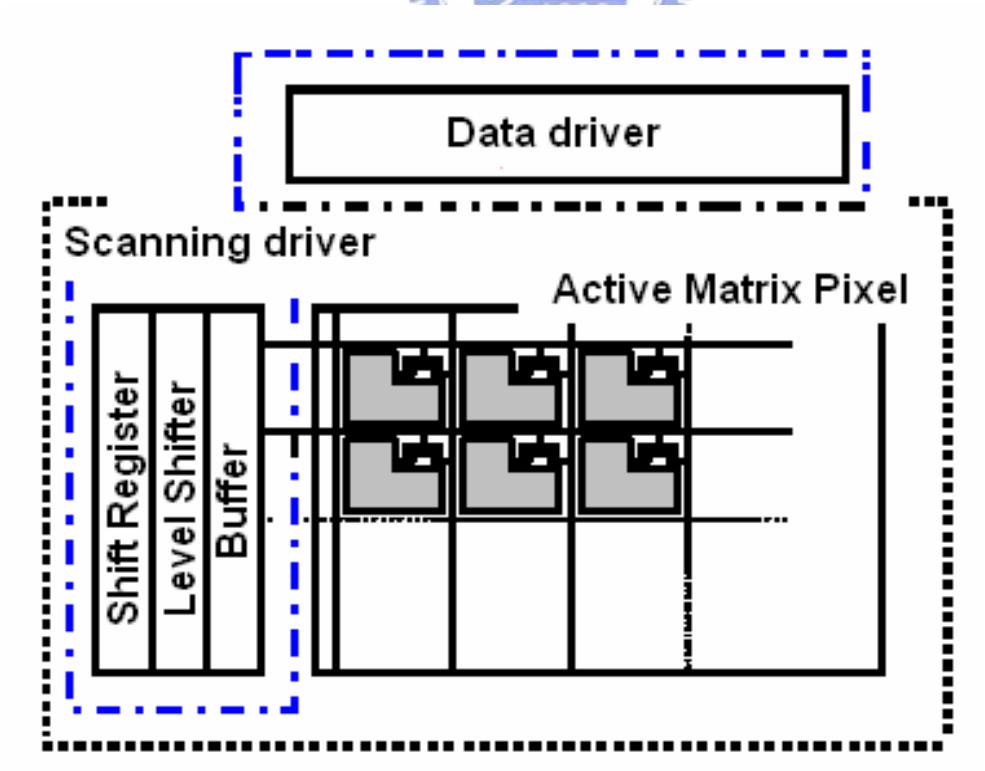


Fig. 2.11 The block diagram of scanning driver.

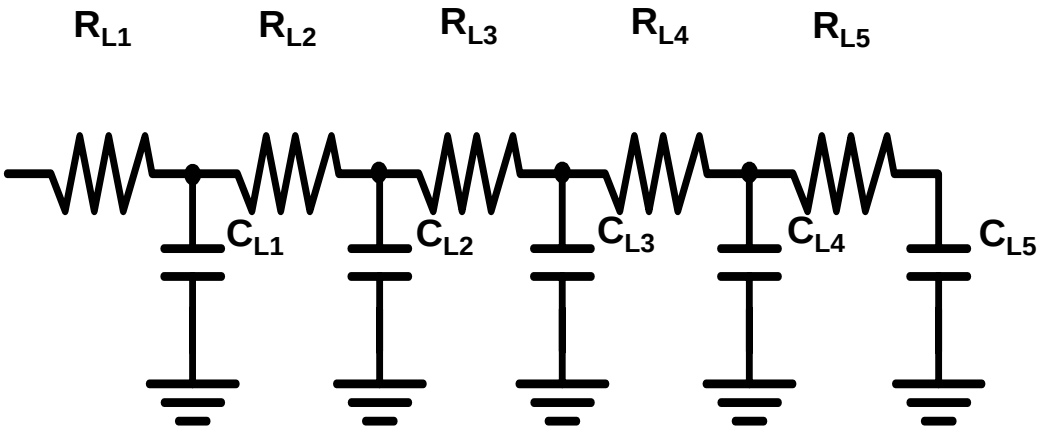


Fig. 2.12 RC (resister and capacitor) ladder of scanning line.

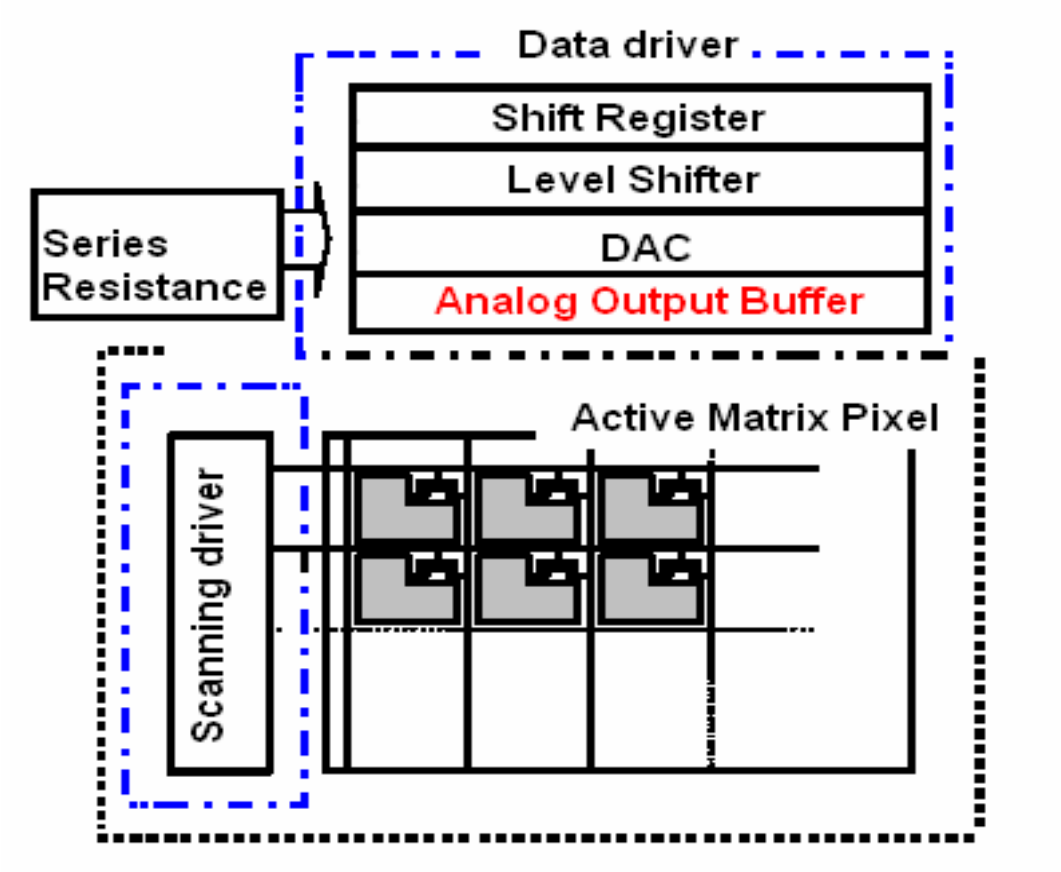


Fig. 2.13 The block diagram of data driver.

CHAPTER 3

OUTPUT BUFFER WITH THRESHOLD VOLTAGE COMPENSATION

3.1 Design Consideration of Output Buffer for LCD

As LCD panel has come into wide use in portable system, such as notebook computer, there is a big demand of developing low power dissipation, high resolution, high speed and large output swing LCD driver. The detailed architecture of LCD driver has been discussed in the last chapter. They include shifter registers, level shifters, DAC, output buffer, etc. Output buffer is much critical to achieve high speed driving, high resolution, low power dissipation and large output swing. In this thesis some output buffers will be proposed to fit the aforementioned concerns.

Furthermore, take the data sheet of KS0625 in Samsung Corp. as reference, some design specifications will be decided in this thesis. For example, the full swing of output voltage in data driver is ±4 V, and the resolution of DAC has 6-to-64 gray level. Besides, the operational frequency is 50 kHz which is applied for XGA (extended graphic array) resolution. And Table I, gives some examples about operational frequencies for typical (frame rate is 60 kHz) display resolution. The loading in this data sheet is a RC ladder whose value and structure are both illustrated in Fig. 3.1. Finally, due to the serious drift of V_{TH} (threshold voltage) in LTPS technology, some output buffers with V_{TH} compensation will also be designed and discussed to overcome the drift of V_{TH}.

3.1.1 Rail-to-Rail Operational Amplifier

In order to get the large output swing, a rail-to-rail operational amplifier is employed to achieve this purpose [5]-[6]. Make the use of dot inversion driving characteristic in LCD panel; an elegant and lower power rail-to-rail amplifier is proposed which is shown in Fig. 3.2. A PMOS input differential amplifier has a large discharge capability and a NMOS input differential amplifier has a large charge capability. In a dot inversion method; a negative-to-positive or positive-to-negative voltage with respect to the fixed voltage of the backside electrode is driven from the column driver with alternating polarities between column lines. When the column lines are under the negative polarity, electrodes are connected to the outputs of PMOS input differential amplifiers. As the column lines are alternated to the positive polarity, the NMOS differential input amplifiers drive the electrodes to higher level. In brief, the PMOS input differential amplifiers, which have a good discharge capability, drive the negative-going transitions and the NMOS input differential amplifiers, which have a good charge capability, drive the positive-going transitions. So, the common mode input voltage of the PMOS input differential amplifier can be very low and vice versa for the NMOS input differential amplifier. In summary, a large output swing and low power output buffer is achieved by this method.

3.1.2 High Slew Rate Operational Amplifier

Due to the large output loading and timing limit of LCD panel, the slew rate of output buffer in data driver must be enhanced. Fig. 3.3 is a fundamental circuit structure of slew rate enhancement. As shown in this circuit, Amplifier-C monitors the output voltage of first stage amplifier. Then, the voltage of this output is converted to current by the V-I (voltage to current) converter, and the converted current will be

added to the bias current of first stage. By this way, the slew rate of this operational amplifier will be enhanced significantly.

3.2 Slew Rate Enhancement Output Buffer

As previously discussed, a simple operational amplifier with slew rate enhancement in LTPS technology is proposed in Fig. 3.4. For an output buffer, the output is connected to the inverting input (in-) and the input signal is applied to the non-inverting terminal (in+). The differential pair M5-M6, which is biased by a constant current source M1-M4, is actively loaded by the current mirror formed by M7 and M8. Besides, M9 and M10 form a common source output stage and the loading in the output is 680pF. When the output stage of M9-M10 is used to drive a large capacitive load of a LCD panel under a step wise input, it will have a better fall time but a poor rising time since M9 is controlled by a constant current which provides limited charging capability to the load. To overcome this problem, M11–M12, which forms a current comparator and a charging transistor M13 are added. The width and length of M12 is chosen the same as those of M7 and M8 to draw the same amount of current, I/2, where I is the biasing current of the input differential stage. However, the width and length of M11 is chosen to be a little bit larger than half of M4.

$$(W/L)_{11} = 1/2(W/L)_4 + \Delta(W/L) \qquad (3\text{-}1)$$

In the stable state with no input signal, the output voltage will equal to the input voltage. The current flowing in M5, M6, M7, M8, and M12 are all I/2. At this

moment, the current flowing in M11 is also I/2. However, since the aspect ratio of M11 is designed to be greater than half of M4, this will force M11 go out of the saturation region and be in the triode region. As a result, the gate voltage of M13 will be forced to be close to the value of VDD. M13 will then stay at "off". That is, when no input signal is applied, M13 is cut off from the output.

When the input voltage of the non-inverting terminal is raised by a step voltage ΔV_1, the current in M5 will be increased to $I/2 + (1/2)gm\Delta V_1$ but the current in M6 will be decreased to $I/2 - (1/2)gm\Delta V_1$, where gm is the trans-conductance of M5 and M6.

$$\mathbf{I_{D5} = I/2 + (1/2)gm\Delta V_1} \quad (3\text{-}2)$$

$$\mathbf{I_{D6} = I/2 - (1/2)gm\Delta V_1} \quad (3\text{-}3)$$

$$\mathbf{gm = [I(W/L)_5\mu_P Cox]^{1/2}} \quad (3\text{-}4)$$

μ_P and Cox are the mobility in the p channel and the gate oxide capacitor per unit area, respectively. If I_{D5} is greater than $I/2 + \Delta I$, it will get the formula which is shown as follow:

$$\mathbf{\Delta V1 > 2\Delta I/gm} \quad (3\text{-}5)$$

$$\mathbf{\Delta I = 1/2\mu_P Cox\Delta(W/L)(V_{GS11} - V_{THP})^2} \quad (3\text{-}6)$$

That is, transistor M11 will go into the saturation region and the gate voltage of M13 will decrease to turn on M13. So, M13 begins to charge the output terminal. The larger varies in ΔV_1, the more M13 will be turned on. Since V_{GS13} can reach a value of VDD, the gate voltage of M13 can be decreased to a really low and M13 can be turned to fully "on" to charge the output terminal by a maximal speed. When the

output voltage reaches to the level that the voltage difference between the input and output is less than 2ΔI/gm, M13 will stop to charge the output terminal. By this way, the output buffer can be used to drive a larger capacitive load. Furthermore, the driving capability can be improved by increasing the size of M13, M9, and M10. But, there is one thing must be noticed. Increasing the aspect ratio of M13 does not increase the static current; however, increasing the sizes of M9 and M10 will increase the static current. In other ward, that will increase the total power consumption.

The simulation results of frequency response in TOPPOLY 6-μm LTPS model are shown in Fig. 3.5. It can find that open loop gain is 61.5 dB, unit gain frequency is 2.1 MHz, and the phase margin is 53.9°. Fig. 3.6 shows the output waveform when input signal is applied. The input signal swing is 2V-10V and operational frequency is 50 kHz. Besides, the rising and falling time of output waveform are 1.58 μs and 1.40 μs, respectively. In summary, the specification of this output buffer is listed in Table II. Fig. 3.7 is the whole layout of this circuit in TOPPOLY 6-μm LTPS process.

3.3 Low Power Class-B Output Buffer

3.3.1 Design Conception

According to the above circuit, it can drive heavy loading by slew rate enhancement structure, but there is still a lot to be improved in terms of power consumption. In this section a low power class-B output buffer is included and implemented in TOPPOLY 6-μm LTPS process [7]-[9]. Fig. 3.8 is the whole operational amplifier circuit diagram and its own loading is also shown in this figure. The loading also take the data sheet of KS0625 in Samsung Corp. as a reference. As an output buffer, the output is connected to the inverting input (in-) and the input signal is applied to the non-inverting terminal (in+). This output buffer is composed

of a differential stage (M4-M8), two comparators (M9-M12), and a push-pull output stage (M13-M14). The differential pair M5-M6, which is biased by the constant current source M1-M4, is loaded by the diode-connected transistors M7 and M8. The comparators are used to sense and amplify the voltage difference of two inputs. Then the output of the comparators turns on or off the push-pull transistors. The aspect ratios of M9 and M11 are chosen to be the same as those of M7 and M8. However, the W/L of M10 is chosen to be a little bit larger than half of M4 but M12 a little bit smaller than half of M4.

$$(W/L)_{10} = 1/2(W/L)_4 + \Delta(W/L) \quad (3\text{-}7)$$

$$(W/L)_{12} = 1/2(W/L)_4 - \Delta(W/L) \quad (3\text{-}8)$$

In the stable state with no input signal, the output voltage will equal to the input voltage. The current flowing in M5, M6, M7, M8, M9 and M11 are all I/2. Then, the current flowing in M10 and M12 are also I/2. However, since the aspect ratio of M10 is designed to be greater than half of M4, this will make M10 go out of the saturation region and be in the triode region. So, the gate voltage of M14 will be forced to be close to the value of GND. M14 will then stay at “off”. For the comparator M11-M12, similarly, M11 will be in the triode region. The gate voltage of M13 will be forced to be close to the value of VDD. M13 will also stay at “off”. That is, when no input is applied, M13 and M14 are almost cut off from the output. However, when the input voltage of the non-inverting terminal is raised by a step voltage ΔV_1, the current in M5 will be increased to $I/2 + (1/2)gm\Delta V_1$, but the current in M6 will be decreased to $I/2 - (1/2)gm\Delta V_1$, where gm is the trans-conductance of M5 and M6. And all of these are list in formula (3-9), (3-10), and (3-11).

$$\mathbf{I_{D5} = I/2 + (1/2)gm\Delta V_1} \quad (3\text{-}9)$$

$$\mathbf{I_{D6} = I/2 - (1/2)gm\Delta V_1} \quad (3\text{-}10)$$

$$\mathbf{gm = [I(W/L)_5\mu_nCox]^{1/2}} \quad (3\text{-}11)$$

μ_n and Cox are the mobility in the n channel and the gate oxide capacitor per unit area, respectively. The current in M6 is mirrored by M8, M9, and M11 to the two comparators M9-M12. Since I_{D6} is decreased, M10 will still stay in the triode region. M14 will than still stay at "off". However, if I_{D6} is smaller than I/2 + ΔI, it will get the formula which is shown as follow:

$$\mathbf{\Delta V1 > 2\Delta I/gm} \quad (3\text{-}12)$$

$$\mathbf{\Delta I = 1/2\mu_nCox\Delta(W/L)(V_{GS4} - V_{THP})^2} \quad (3\text{-}13)$$

That is, transistor M11 will go into the saturation region and its drain voltage will decrease to turn on M13. Then, M13 begins to charge the output node. The larger varies in ΔV_1, the more M13 is turned on. Since the gate voltage of M13 can be decreased to a really low and M13 can be turned to almost "on" to charge the output by a maximal speed. Hence, the output transistors M13-M14 can be designed to be of smaller sizes than the conventional output buffer. When the output voltage reaches the level that the voltage difference between the input and output is less than 2ΔI/gm, V_{GS13} will be reduced and M13 begins to stop charging the output node. The smaller voltage varies, the more M13 is turned off. Similarly, when the input voltage of the non-inverting input is reduced by a step voltage ΔV_1 from the stable state, M13 will still stay at "off". If ΔV_1 is greater than 2ΔI/gm, M10 will go into the saturation region and M14 starts to discharge the output node. Also, when the output voltage reaches the level that the voltage difference between the input and output is less than 2ΔI/gm,

M14 begins to stop discharging output node. Hence, with the consideration of the offset voltage, the operation of this buffer can be summarized as follow:

- When Vin – Vout – Vos > 2ΔI/gm, M13 will charge the output node.
- When Vin – Vout – Vos < –2Δ/Igm, M14 will charge the output node.
- When –2Δ/Igm < Vin – Vout – Vos < 2ΔIgm, both output transistors stay at off.

Where Vos is the input offset voltage of the output buffer. Since transistor M13 and M14 are almost "off" at the stable state, they consume almost no current. That is why this architecture of output buffer is low power while the operational speed can maintain relatively high.

3.3.2 Measurement Result

Based on lower power considerations, a low power class-B output buffer is proposed and implement in TOPPOLY 6-μm LTPS process. Furthermore, the simulation results of frequency response in TOPPOLY 6-μm LTPS model are shown in Fig. 3.9. It can find that open loop gain is 40 dB, unit gain frequency is 1.7 MHz, and the phase margin is 73.8°. Fig. 3.10 shows the output waveform when input signal is applied. The input signal swing is 2V-10V and operational frequency is 50 kHz. Besides, the rising and falling time of output waveform are 2.88 μs and 3.30 μs, respectively. In summary, the specification of this output buffer is listed in Table III.

Fig. 3.11 is the whole layout of this circuit in TOPPOLY 6-μm LTPS process. Also, the measurement environment and glass photo are shown in Fig. 3.12. The input pattern and DC bias are generated by pulse generation and power supply through probe station. Besides, the output waveform is also investigated by oscilloscope through probe station. The total instruments for measuring class-B output buffer are

illustrated in Fig. 3.13. According to above descriptions, the performance of this circuit are measured and list below. Fig. 3.14 is the waveform when input signal swing is 2V-10V and operational frequency is 50 kHz. In this figure, it can see that the rising time and falling time are 3.478 μs and 4.654 μs. These results are a little different from the simulation. About this different, it may be caused by the drift V_{TH}, and this problem will be solve in next section. But the function of this class-B output buffer is work in general. Besides, the output waveform is also shown in Fig. 3.15 when input signal swing is 5.75V-6.25V and operational frequency is 50 kHz. It can see that the output waveform has a little overshot in rising and falling step. These results are caused by the phase margin and it also shows the relationship between phase margin and overshot in Table IV. Furthermore, the output waveform when input signal swing is 2V-10V and operational frequency is 100 kHz, 200 kHz, 400 kHz and 800 kHz is also measured and shown in Fig. 3.16(a), Fig. 3.16(b), Fig. 3.16(c), and Fig. 3.16(d). As it can see, when input operational frequency is fewer than 400 kHz, the output waveform can reach the full swing in 20 μs. In addition, Fig. 3.17(a), Fig. 3.17(b), Fig. 3.17(c), and Fig. 3.17(d) are the output waveform when input signal swing is 5.75V-6.25V and operational frequency is 100 kHz, 200 kHz, 400 kHz and 800 kHz. It also shows that, the output waveform can function well when input signal operational frequency is fewer than 400 kHz. In summary, it can announce that this class-B output buffer in TOPPOLY 6-μm LTPS process can operate upper to 400 kHz. Furthermore, it will not consume extra power when input signal is stable.

3.4 Output Buffer with V_{TH} Compensation

3.4.1 The Causation of Offset Voltage

With the high demand for portable systems such as cell phones, PDAs (personal

digital assistant) as well as notebook computers, data driver which are integrated in TFT (thin film transistor) have recently been developed to reduce cost and complexity in manufacture. As what is showed in Fig. 3.18, analog output buffer is the major circuit block for the data driver in TFT-LCD. It can amplify the input analog signal because the signal may be too small to drive a load. And, the operational amplifier is considered as analog output buffer because the operational amplifier has rather low linearity error, wide output range and high driving capability. Therefore, it should be urgently realized on glass in LTPS technology. However, the device in LTPS technology has serious problems for analog output buffer such as kink effect and dramatic variation of threshold voltage.

It should be noted that the mismatch of device in LTPS technology results in the output variation. For example, a finite mismatch is due to the uncertainties in each step of the manufacturing process. As shown in Fig. 3.19, the gate dimensions of the TFT device suffer from random and microscopic variations; hence mismatches exists between the equivalent lengths and widths of two transistors that are identically laid out. Besides, the TFT device has the large varied characteristics such as mobility and threshold voltage. These variations vary randomly from one device to another. And the offset voltage in output is increased when the variation of threshold voltage is serious. Express the characteristics of a TFT device in saturation region as $I_D = (1/2)\mu C_{OX}(W/L)(V_{GS}-V_{TH})^2$, it can be observed that mismatches between μ, C_{OX}, W, L and V_{TH} result in mismatch between drain currents (for a given V_{GS}) or gate-source voltages (for a given drain current) of two nominally-identical transistors. Consider the conventional operational amplifier without offset cancellation shown in Fig. 3.20(a). With $V_{IN} = 0$ and perfect symmetry, $V_{OUT} = 0$, while in the presence of mismatches, $V_{OUT} \neq 0$. As shown in Fig. 3.20(b), the circuit suffers from an offset voltage equal to the observed value of V_{OUT} when V_{IN} is set to zero. In practice, it is

more meaningful to specify the offset voltage in input, defined as the input level that forces the output voltage to go to zero. According to the above description, the conventional operational amplifier without offset cancellation of Fig. 3.20(a) is to amplify a small input voltage. Then, as depicted in Fig. 3.21, the output contains amplified replicas of both the signal and offset voltage. And, if the offset voltage is serious, the offset voltage in output will force the conventional operational amplifier falls into nonlinear operation.

To calculate the offset voltage of the conventional operational amplifier without offset cancellation, Fig. 3.20(a) is be modified as Fig. 3.21. The offset voltage of N-type TFT device and P-type TFT device is inserted in Fig. 3.21. If $I_{D1} = I_{D2}$ and $I_{D3} = I_{D4}$, then a formula of input offset voltage is shown below.

$$\mathbf{V_{OS,N} = [(V_{GS}-V_{TH})_N/2][\Delta(W/L)/(W/L)]_N + \Delta V_{TH,N}} \quad (3\text{-}14)$$

$$\mathbf{V_{OS,P} = [(|V_{GS}-V_{TH}|)_P/2][\Delta(W/L)/(W/L)]_P + \Delta V_{TH,P}} \quad (3\text{-}15)$$

Besides, $V_{OS,P}$ is amplified by a gain of $g_{mP}(r_{ON} \parallel r_{OP})$ and divided by $g_{mN}(r_{ON} \parallel r_{OP})$ when referred to the main input. Then, according to formula (3-14) and (3-15), a total offset voltage referred to the main input can be calculated in following formula.

$$\mathbf{V_{OS,IN} = \{ [(|V_{GS}-V_{TH}|)_P/2][\Delta(W/L)/(W/L)]_P + \Delta V_{TH,P} \}(g_{mP}/ g_{mN})} + \mathbf{[(V_{GS}-V_{TH})_N/2][\Delta(W/L)/(W/L)]_N + \Delta V_{TH,N}} \quad (3\text{-}16)$$

As previously described, the offset voltage caused by P-type TFT device can be decreased by enlarging the size of N-type TFT device. In addition, the offset voltage caused by the mismatch and random variation of the N-type TFT device can be eliminated by adopting common centroid layout. Furthermore, the offset voltage

caused by the latter gain stage can also be improved, because it will be divided by the gain of first stage. Therefore, if the variation of threshold voltage caused by the N-type TFT device can be minimized, the operational amplifier can function well and has rather low linearity error.

According to the above discussion, if the analog output buffer can be designed more elegant to eliminate the offset voltage, the data driver can be integrated on glass in LTPS technology promisingly. Thus, this thesis aims to propose some new analog output buffers with threshold voltage compensation. An AZ (auto zeroing) method was employed to reduce the offset voltage and it can process the higher resolution and higher quality panel.

3.4.2 Design of Output Buffer with V_{TH} Compensation

The basic idea of auto zeroing method is sampling the unwanted input offset voltage and then subtracting it from the instantaneous value of contaminated signal at the input [10]. A three-phase auto zeroing method using to reduce the offset voltage is shown in Fig. 3.22. The operational amplifier is employed class-B structure which is discussed in last section. The offset voltage of the operational amplifier is reduced as follow. During the first phase (ϕ1), the offset-holding capacitor C is reset by the output of the amplifier. Then, during the second phase (ϕ2), the offset voltage is detected in the output voltage and hold by capacitor C. Finally, during third phase (ϕ3), the detected offset voltage is added to the amplifier input, completing the offset cancellation. The output waveform of the three phase threshold voltage compensation which is simulated with TOPPOLY 6-μm LTPS model shows in Fig. 3.23. Through this sequence, the offset-holding capacitor C is pre-charged by the operational amplifier and finally compensates the offset voltage caused by the variation of

threshold voltage in TFT device. In additional, Fig. 3.24 is the layout diagram in TOPPOLY 6-μm LTPS process.

According to the discussion above, the analog output buffer must has three phases to complete the threshold voltage compensation. It will limit the operational speed of output buffer. For this reason, if the phases for threshold voltage compensation can be reduced, the operational speed for analog output buffer can be enhanced further. Besides, it will be more promising to process the higher resolution and higher quality panel. So, a two-phase output buffer is proposed and shown in Fig. 3.25 to improve above drawbacks. As shown in this circuit architecture, Vcm is the common mode voltage of the data driver, and C is the offset-holding capacitor. During the first phase ($\phi1$), the offset voltage is detected in the output terminal and hold by capacitor C. Then, $V_O(\phi1) = Vcm + V_{OS}(\phi1)$ and $V_C(\phi1) = V_{OS}(\phi1)$. During the second phase ($\phi2$) the detected offset voltage is added to the amplifier input, and completes the offset cancellation. So, $V_O(\phi2) = Vi + [V_{OS}(\phi2) - V_{OS}(\phi1)]$ and $V_C(\phi2) = V_{OS}(\phi1)$. From the above description, the analog output buffer only needs two phases to complete the threshold voltage compensation. The output waveform of the two-phase threshold voltage compensation simulated with TOPPOLY 6-μm LTPS model is shown in Fig. 3.26. Fig. 3.27 is the full layout in TOPPOLY 6-μm LTPS process. As a result, the analog output buffer will have a better immunity to the variation of the threshold voltage. Furthermore, a more advance analysis is also done in this thesis. By modifying the V_{TH} in TFT model, it can observe the output variation in output buffer. As describe above chapter, if a 64 gray level data driver must be implemented, the output variation must less than 1/2 LSB (last significant bit). In other word, if the output swing in output buffer is ±4 V, the output variation must less than 32 mV to fit above demands. Fig. 3.28 (Vi = 10 V) and Fig. 3.29 (Vi = 2 V) show the relationship between V_{TH} and output variation in output buffer. It can see that, if

the drift V_{TH} in transistors M5-M8 and M13-M14 are less than 0.6 V (42.8%), the variation in output can be controlled under 32 mV.

Besides, a secondary analog output buffer with modified two-phase threshold voltage compensation is also designed and shown in Fig. 3.30. This structure only needs two phases to complete the threshold voltage compensation, too. What more important is that it does not need the extra common mode voltage (Vcm). Similarly, during the first phase (ϕ1), the offset voltage is detected in the output terminal and hold by capacitor C. Then, $V_O(\phi1) = Vi + V_{OS}(\phi1)$ and $V_C(\phi1) = V_{OS}(\phi1)$. During the second phase (ϕ2) the detected offset voltage is added to the amplifier input, and completes the offset cancellation. So, $V_O(\phi2) = Vi + [V_{OS}(\phi2) - V_{OS}(\phi1)]$ and $V_C(\phi2) = V_{OS}(\phi1)$. However, this structure is simulated in TOPPOLY 3-μm LTPS model. The simulated waveform is shown in Fig. 3.31. Fig. 3.32 is the full layout diagram of this circuit in TOPPOLY 3-μm LTPS process. Also, a more advanced analysis is done in this circuit. By modifying the V_{TH} in TFT model, it can observe the output variation in output buffer. Because the output swing in this output buffer is ±3V, the output variation must less than 23 mV to fit above regulation. Fig. 3.33 (Vi = 8 V) and Fig. 3.34 (Vi = 2 V) show the relationship between V_{TH} and output variation in output buffer. It can see that, if the drift V_{TH} in transistors M5-M8 and M13-M14 are less than 0.6V (48.3%), the variation in output can be controlled under 23 mV.

In summary, this invention of analog output buffer with threshold voltage compensation can be applied in the data drivers for LCD panel system. By employing the threshold voltage compensation method, the analog output buffer can overcome the variation of threshold voltage. Besides, output buffer will be more promising to be integrated in the higher resolution and higher quality LCD panel.

Table I

Operation frequencies specification of LCD panel.

Resolution	VGA	SVGA	XGA	SXGA	UXGA
Total	800×525	1056×628	1344×806	1688×1066	2160×1250
Active	640×480	800×600	1024×768	1280×1024	1600×1200
Frame Rate	60 Hz	60 Hz	60 Hz	60 Hz	60 Hz
Fr (row rate)	31.46 KHz	37.87 KHz	48.36 KHz	63.98 KHz	75.00 KHz
Fp (pixel rate)	25 MHz	40 MHz	65 MHz	108 MHz	162 MHz
Row Period	31.78 μs	26.40 μs	20.68 μs	16.63 μs	13.33 μs

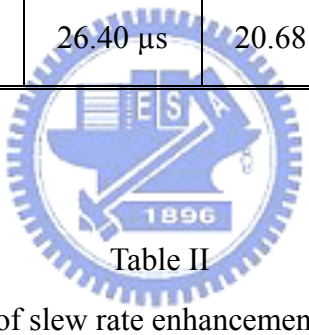


Table II

Specification of slew rate enhancement output buffer.

Output Buffer	Specification
Operational Frequency	50 kHz
Gain	61.5 dB
Phase Margin	53.9°
Unit Gain Frequency	2.1 MHz
Dynamic Range	2 V – 10 V
Rising Time	1.58 μs
Falling Time	1.40 μs
Power Consumption	3 mW

Table III

Specification of Class-B output buffer.

Output Buffer	Specification
Operational Frequency	50 kHz
Gain	40 dB
Phase Margin	73.8°
Unit Gain Frequency	1.7 MHz
Dynamic Range	2 V – 10 V
Rising Time	2.88 μs
Falling Time	3.30 μs
Power Consumption	1.6 mW

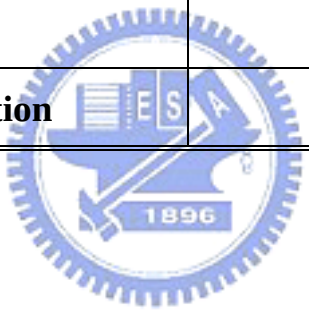


Table IV

The relationship between phase margin and overshot.

Phase Margin	Wu/W2	Overshoot
45°	1.000	36.8%
55°	0.700	13.3%
60°	0.577	8.7%
65°	0.466	4.7%
70°	0.364	1.4%
75°	0.268	0.008%

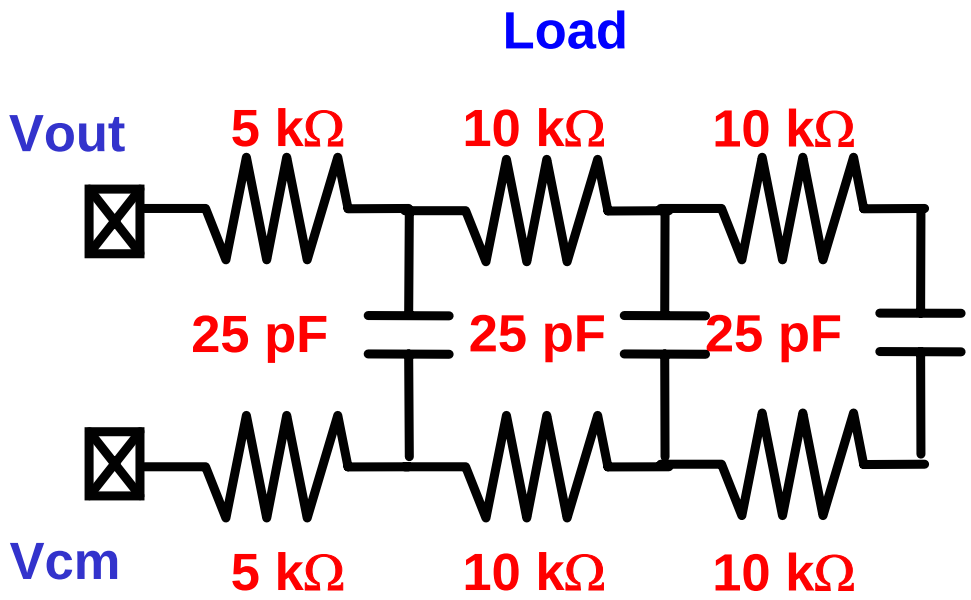


Fig. 3.1 The values of RC ladder in Samsung data sheet.

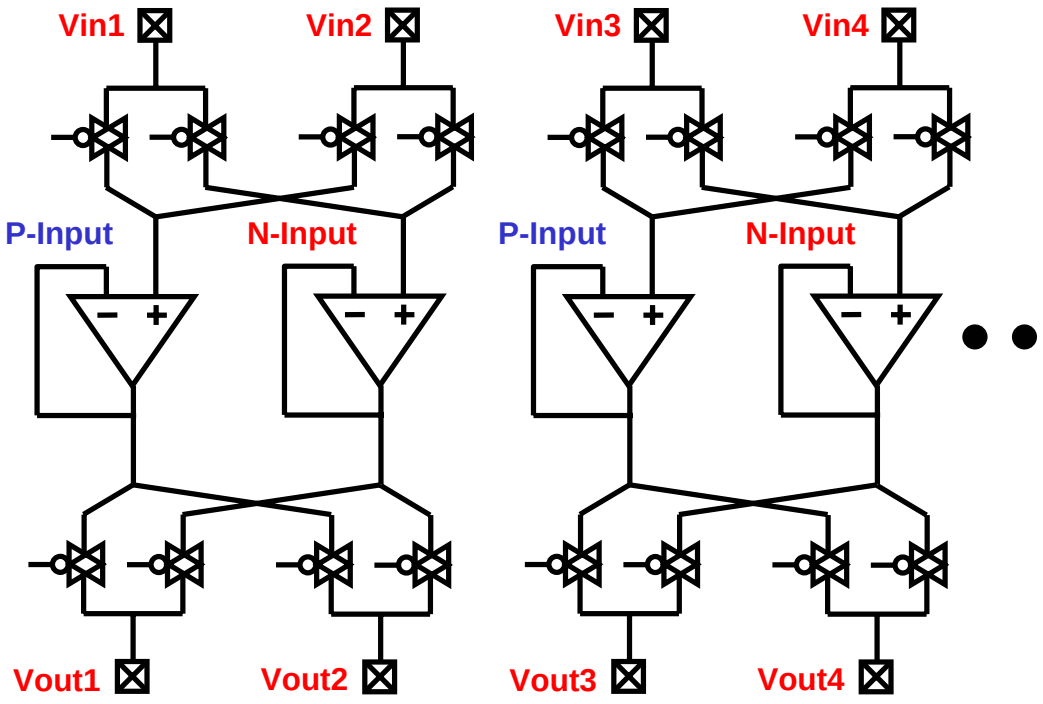


Fig. 3.2 An elegant and lower power rail-to-rail amplifier.

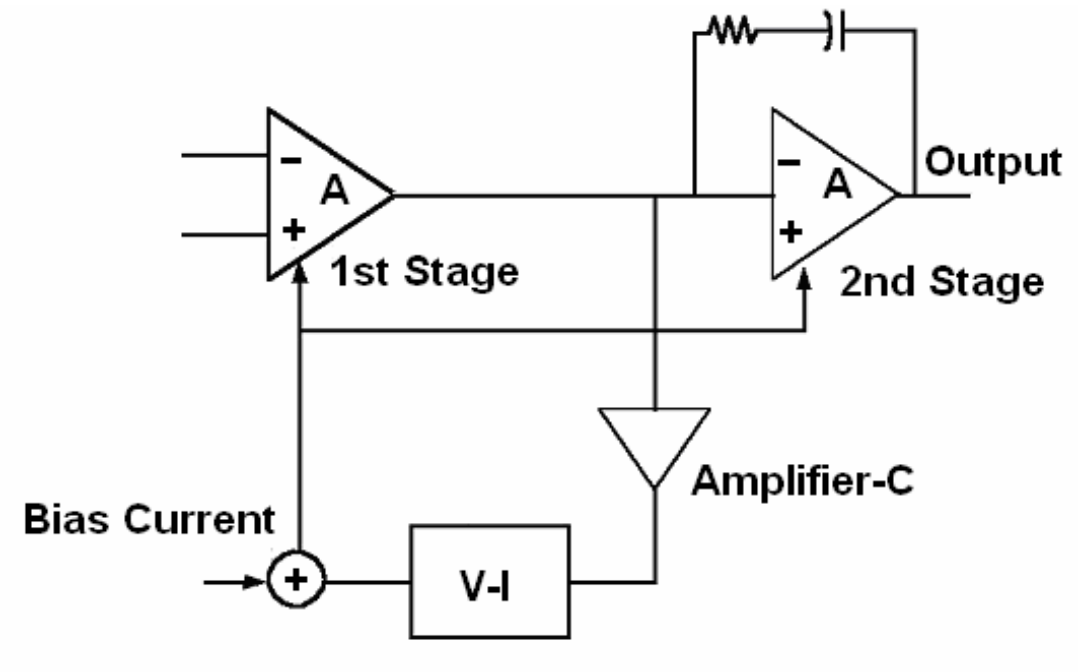


Fig. 3.3 A fundamental circuit structure of slew rate enhancement.

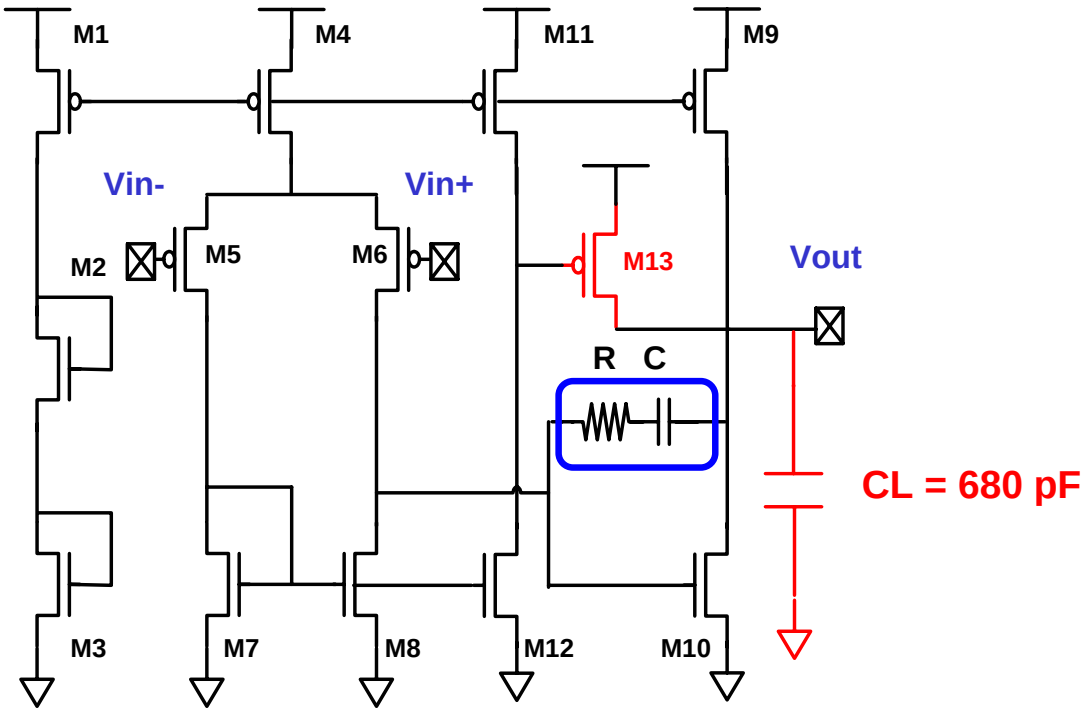


Fig. 3.4 A simple operational amplifier with slew rate enhancement.

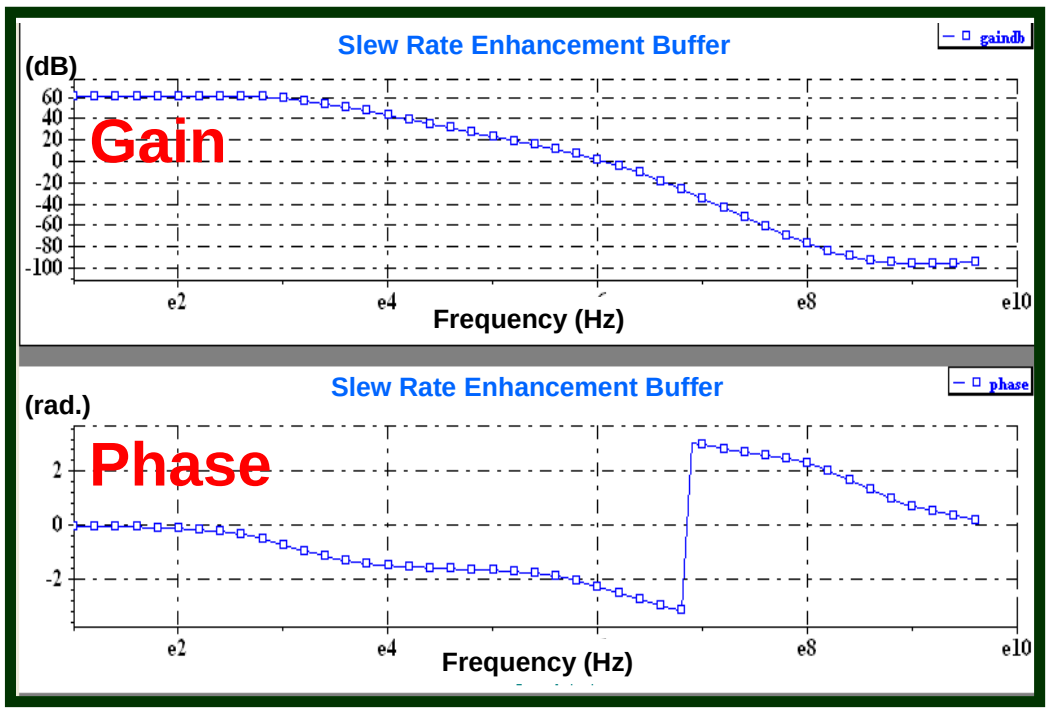


Fig. 3.5 AC simulation of slew rate enhancement output buffer.

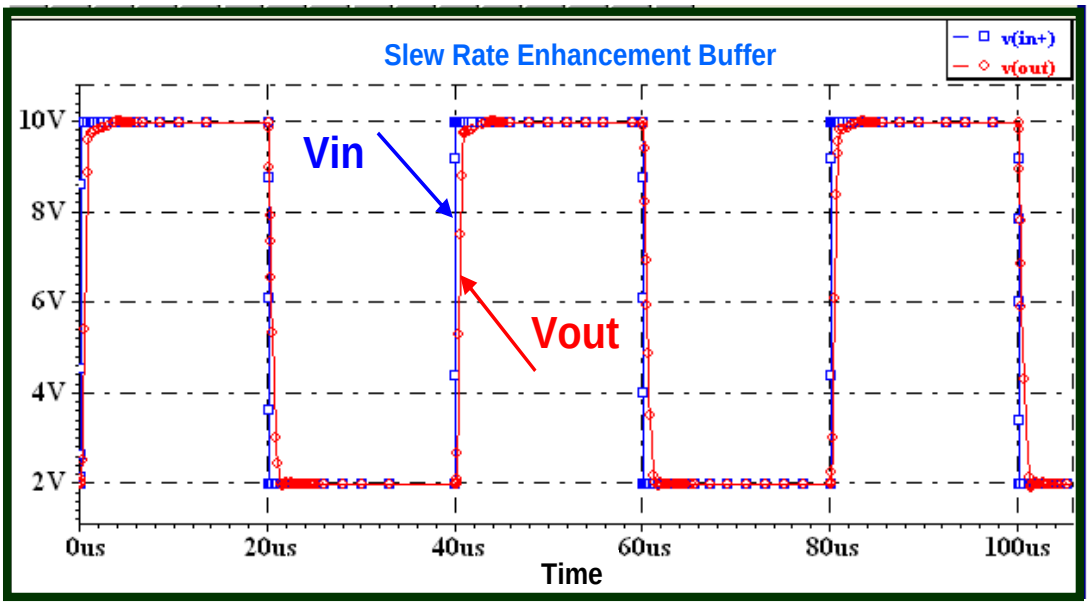


Fig. 3.6 Output waveform of slew rate enhancement output buffer.

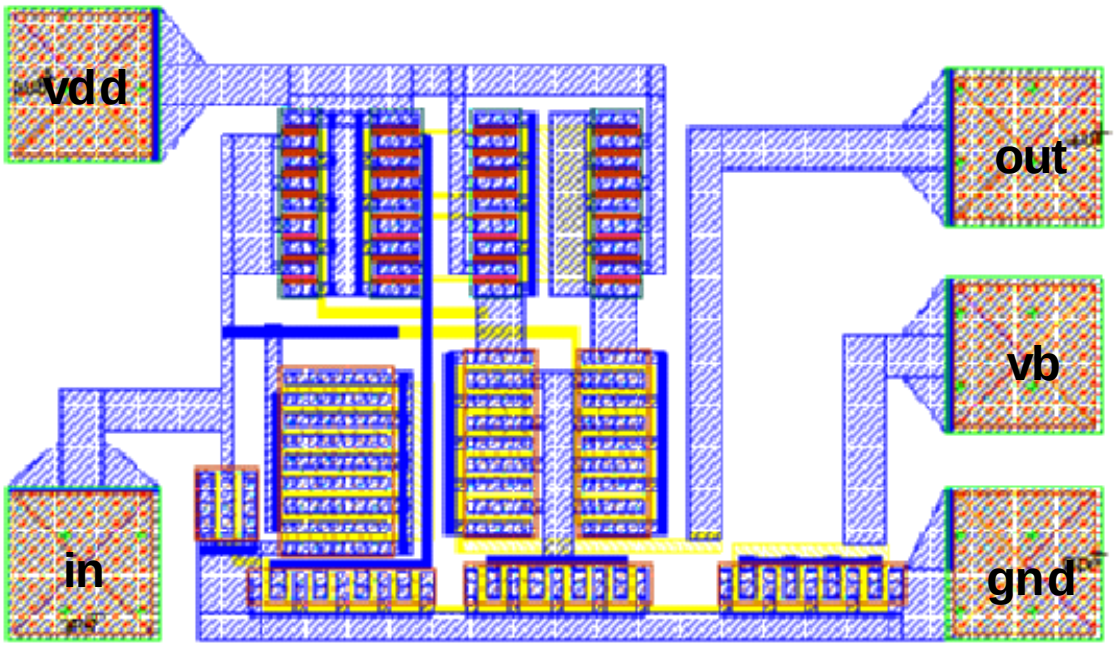


Fig. 3.7 Layout of slew rate enhancement output buffer.

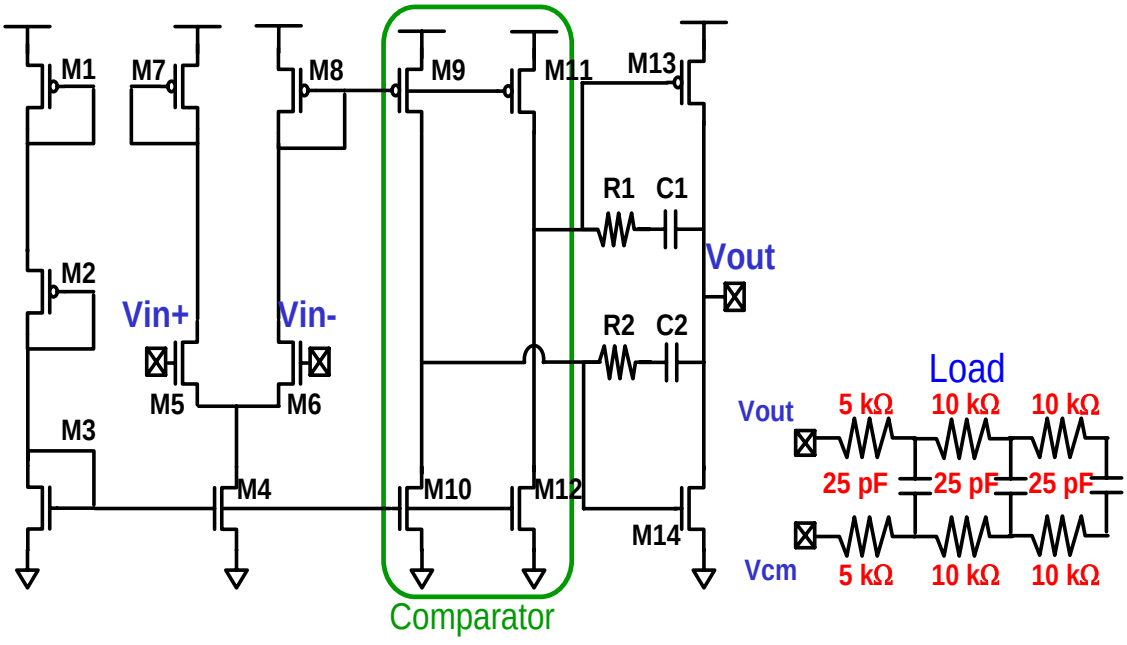


Fig. 3.8 A low power class-B output buffer.

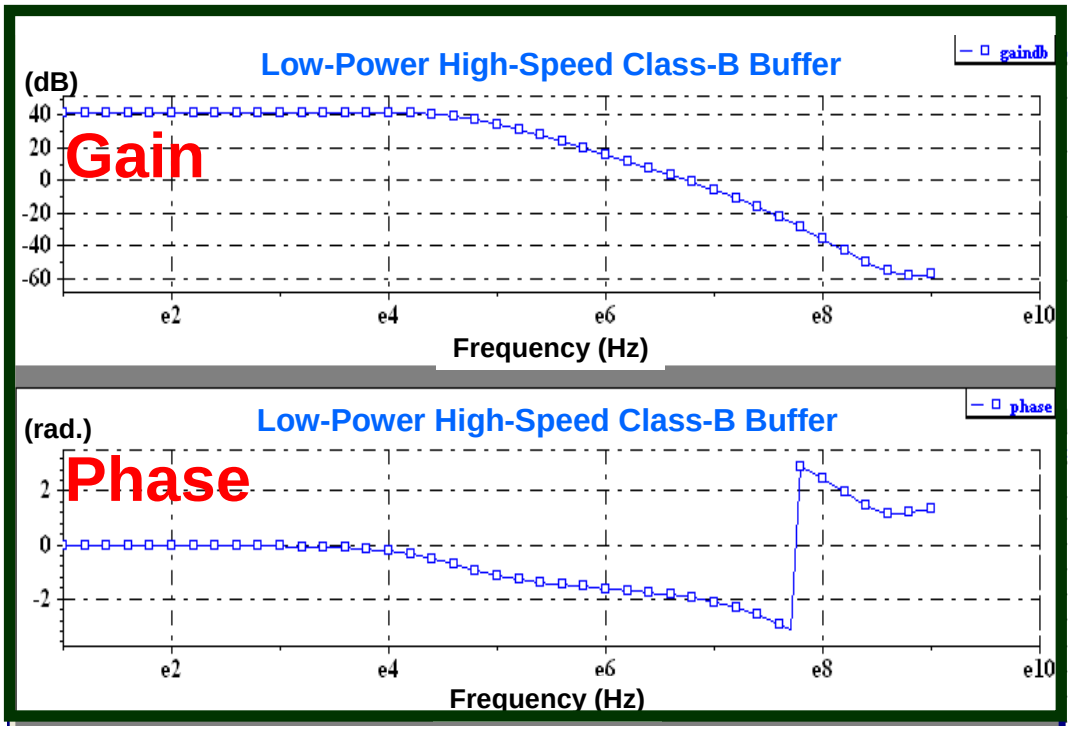


Fig. 3.9 AC simulation of class-B output buffer.

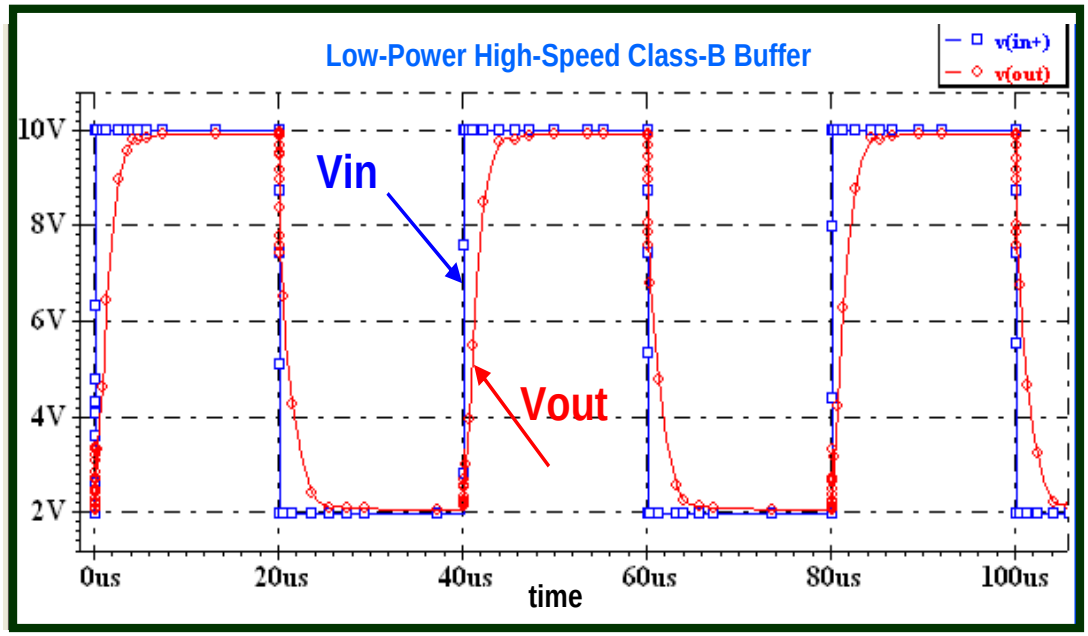


Fig. 3.10 Output waveform of class-B output buffer.

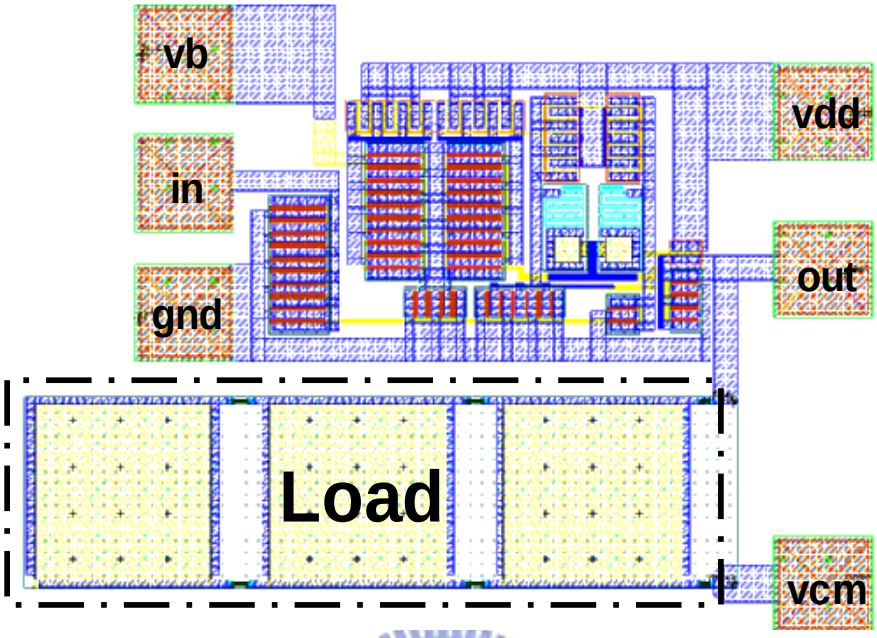


Fig. 3.11 Layout of class-B output buffer.

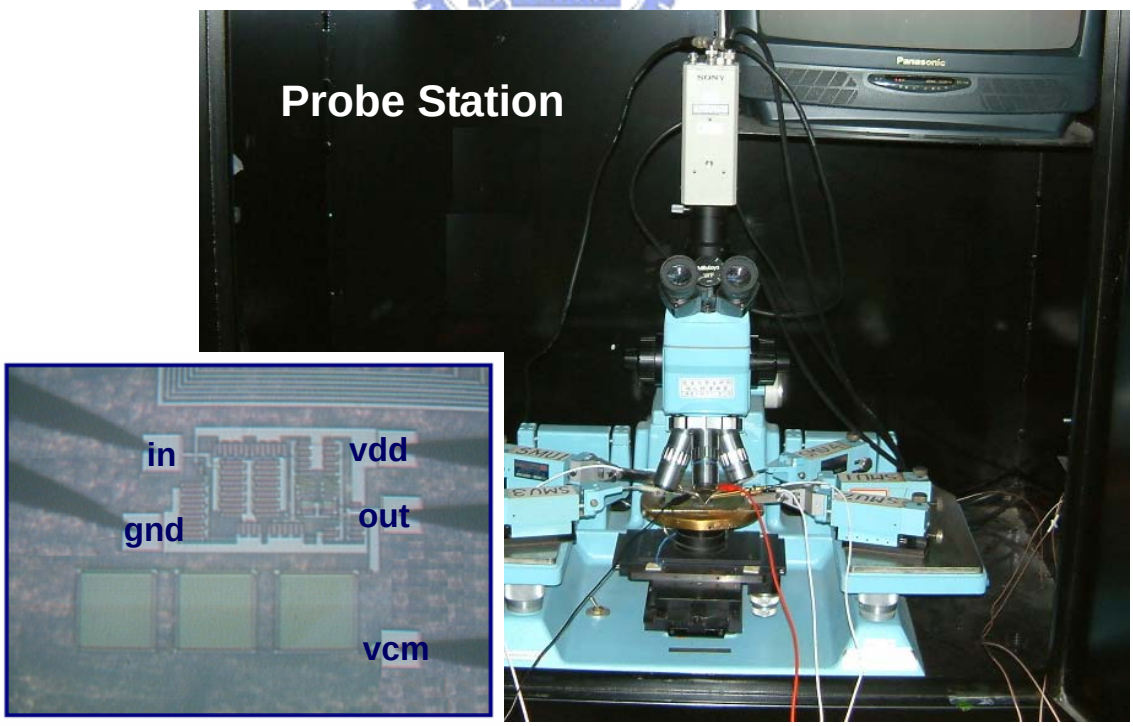


Fig. 3.12 The input pattern and DC bias are generated by pulse generation and power supply through probe station.

Fig. 3.13 Instruments for measuring class-B output buffer.

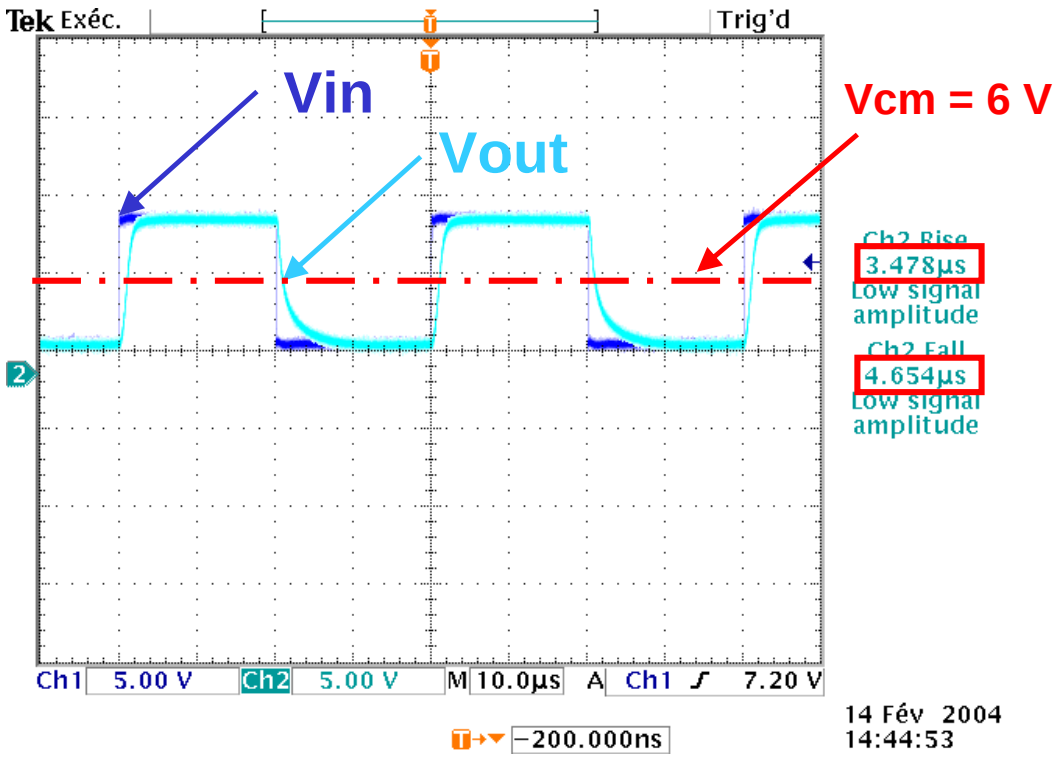


Fig. 3.14 The output waveform when input signal swing is 2V-10V and operational frequency is 50 kHz.

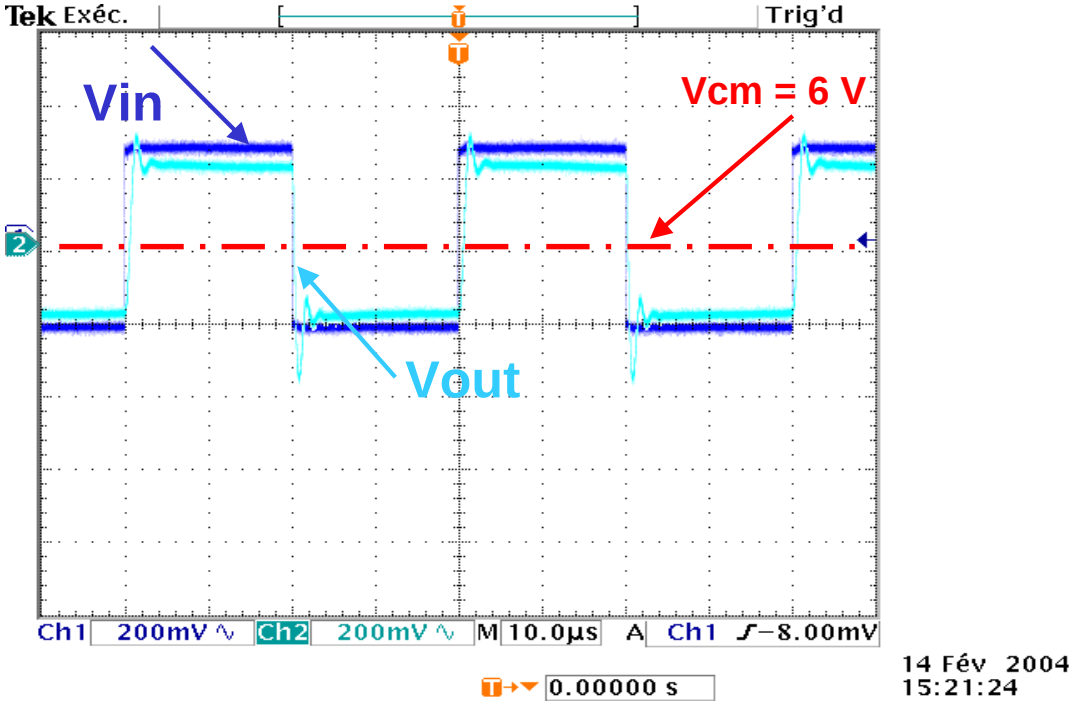
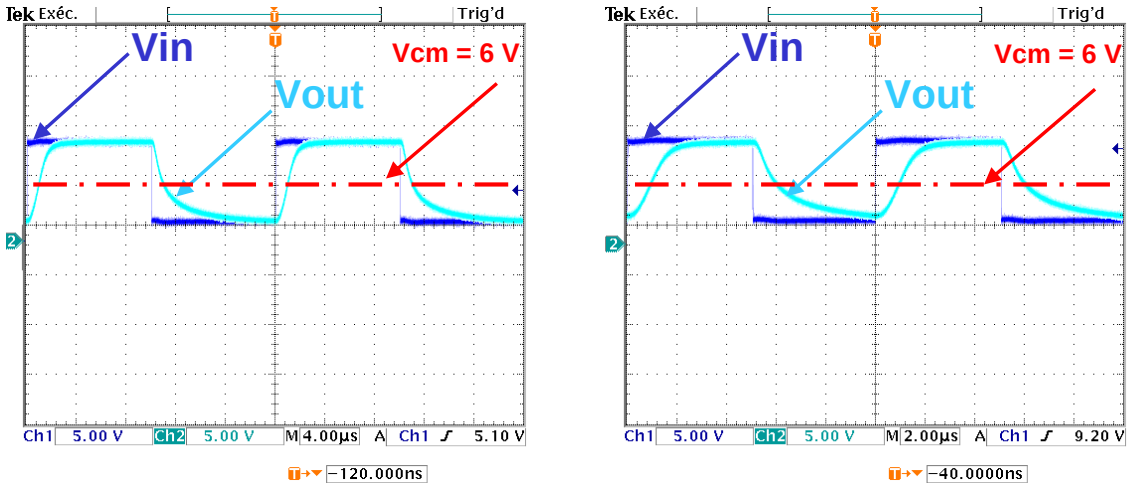
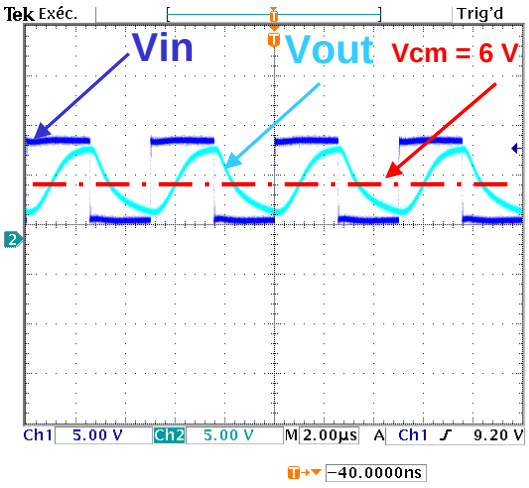


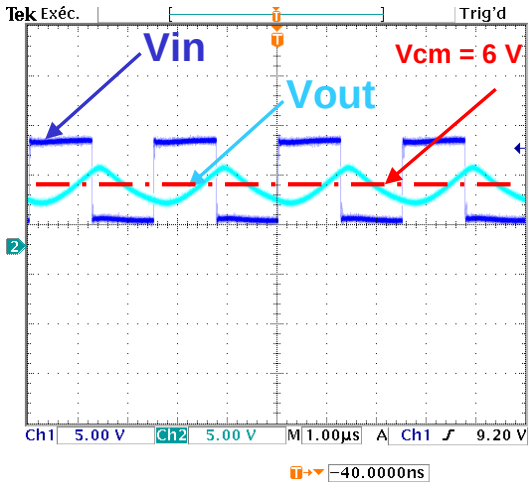
Fig. 3.15 The output waveform when input signal swing is 5.75V-6.25V and operational frequency is 50 kHz.



(a) **(b)**

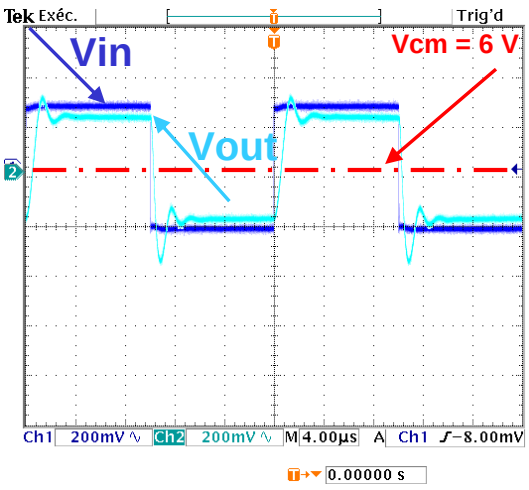


(c)

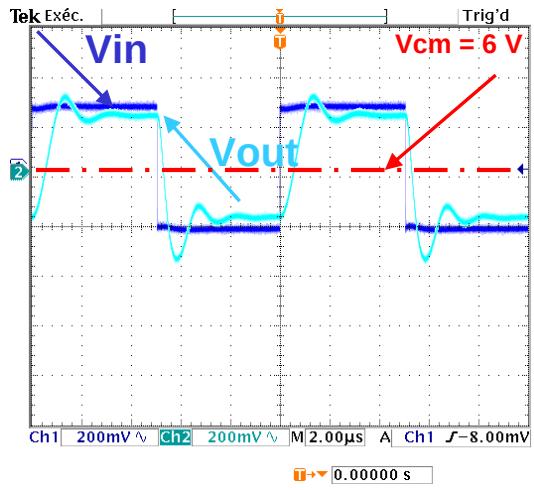


(d)

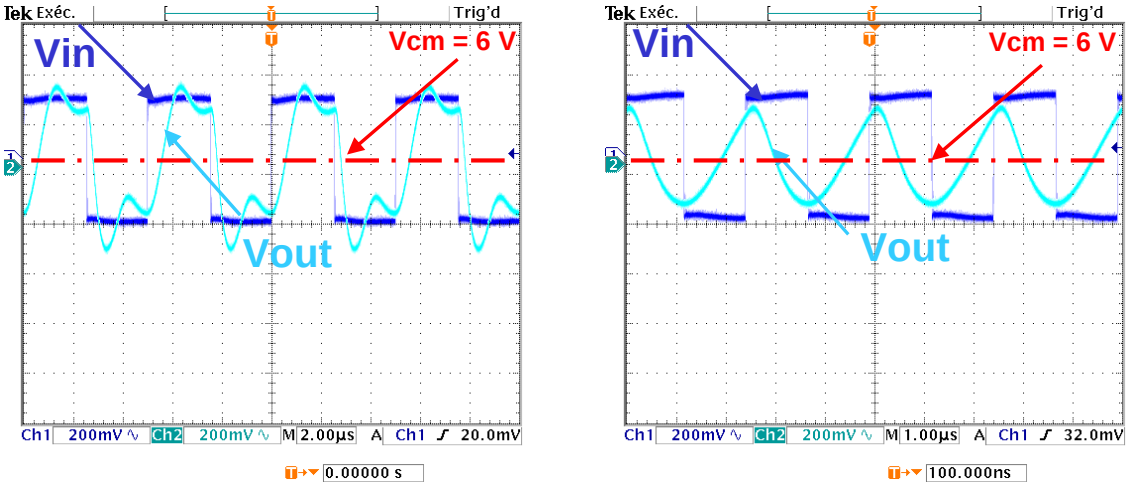
Fig. 3.16 The output waveform when input signal swing is 2V-10V and operational frequency is (a) 100 kHz, (b) 200 kHz, (c) 400 kHz and (d) 800 kHz.



(a)



(b)



(c) **(d)**

Fig. 3.17 The output waveform when input signal swing is 5.75V-6.25V and operational frequency is (a) 100 kHz, (b) 200 kHz, (c) 400 kHz and (d) 800 kHz.

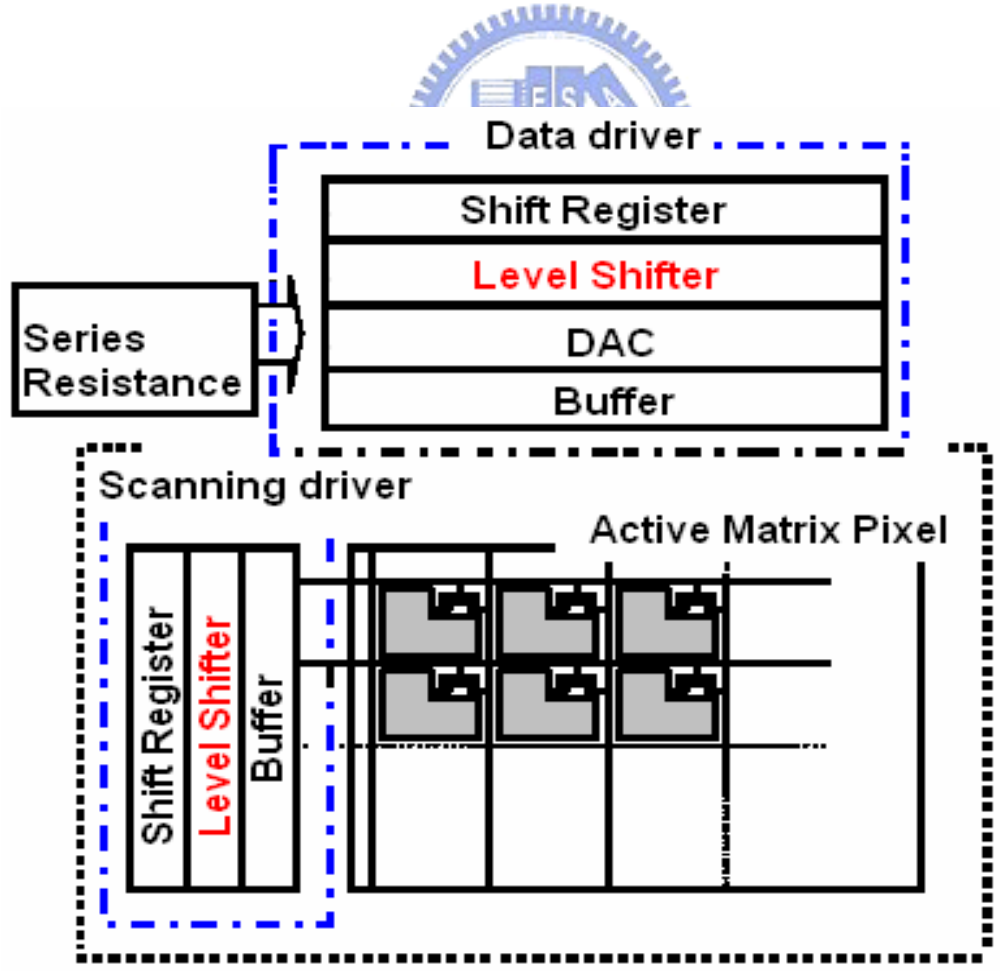


Fig. 3.18 The structure of data driver in TFT-LCD.

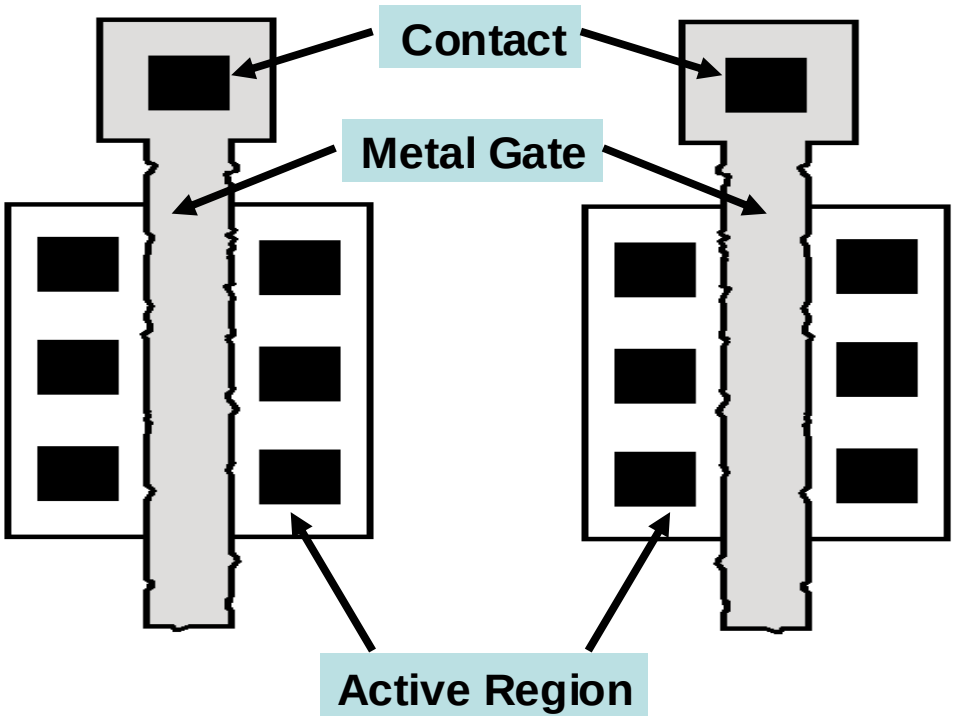


Fig. 3.19 The gate dimensions of the TFT device suffer from random and microscopic variations.

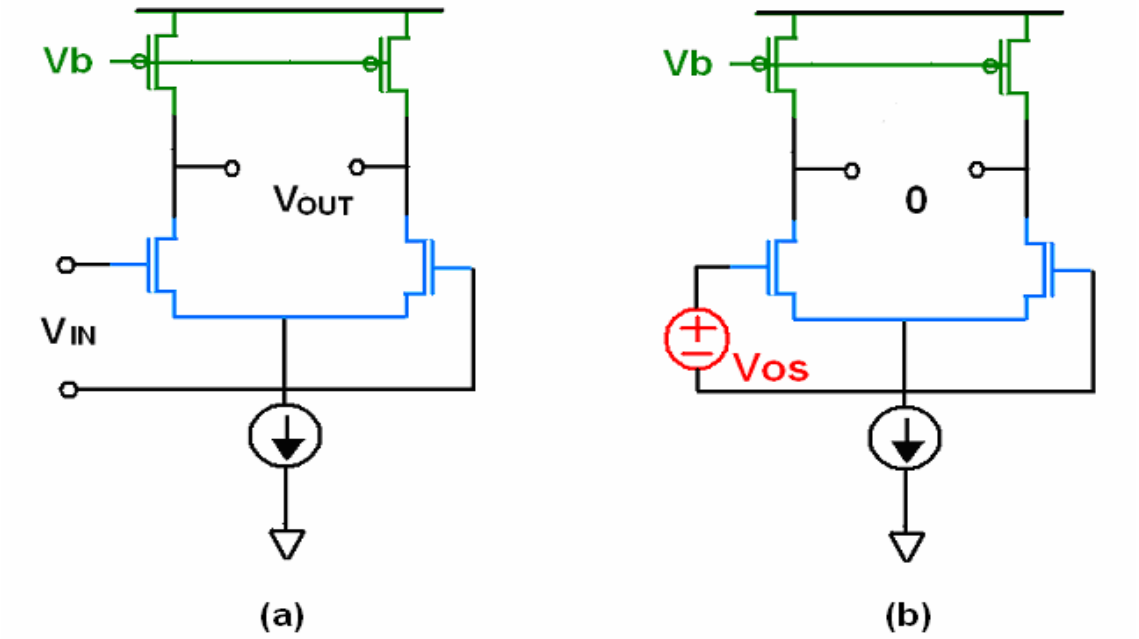


Fig. 3.20(a) The conventional operational amplifier with offset voltage measured at the output, (b) circuit of (a) with its offset voltage referred to the input.

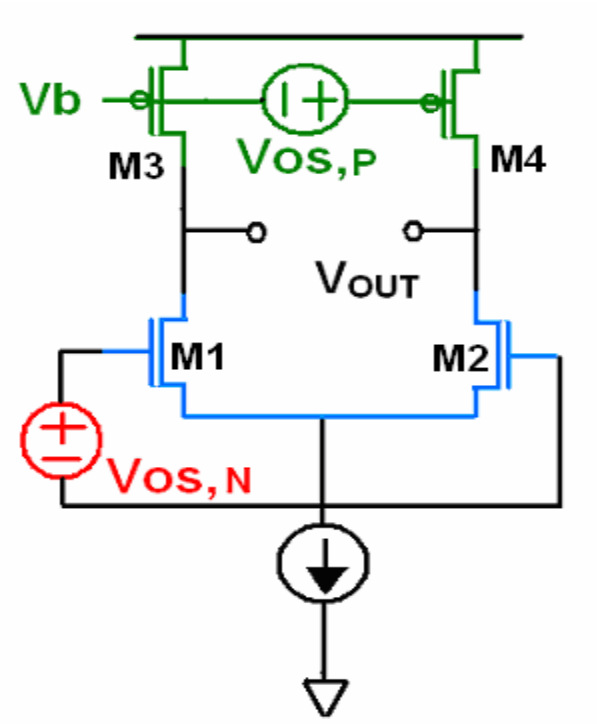


Fig. 3.21 The input referred offset voltage of the N-type TFT and P-type TFT.

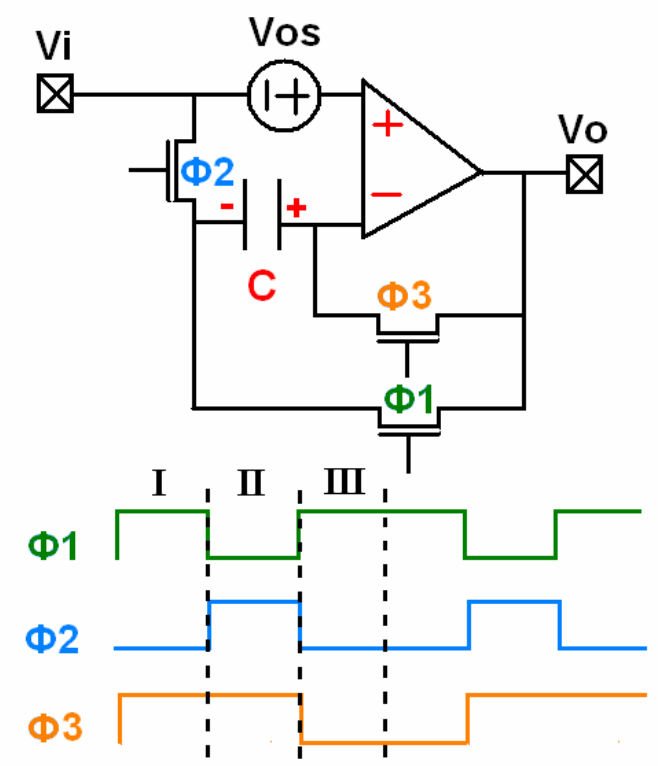


Fig. 3.22 Circuit diagram of analog output buffer with three-phase threshold voltage compensation.

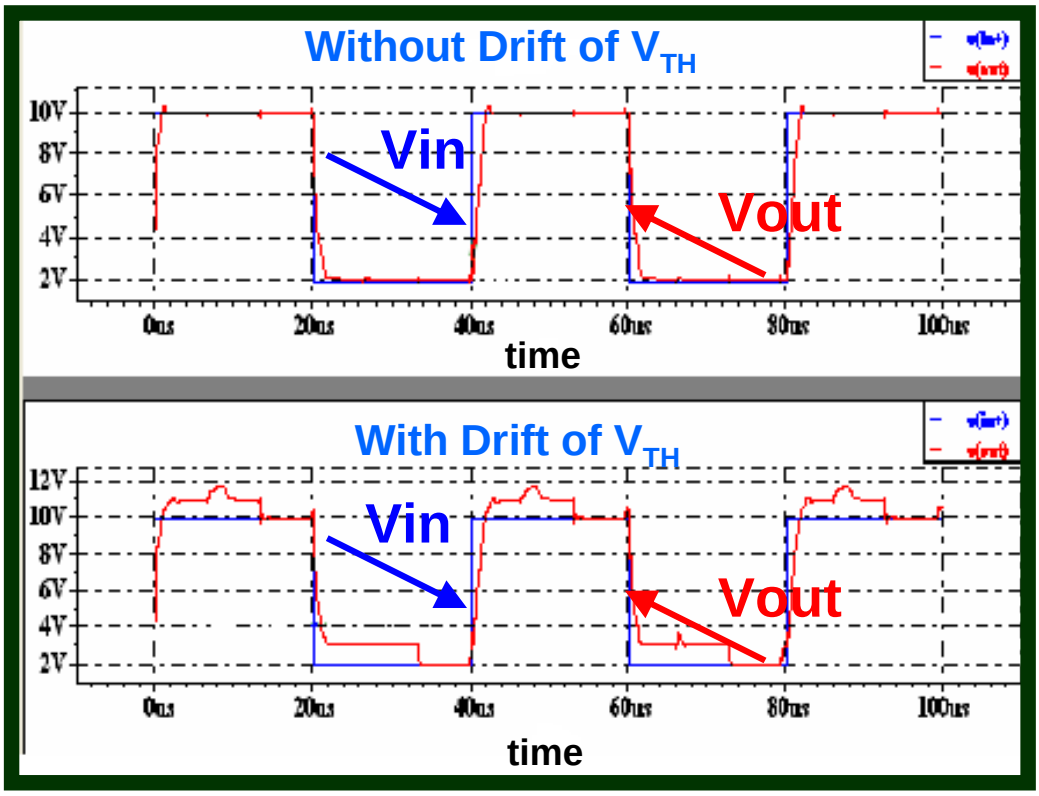


Fig. 3.23 Waveform diagram of analog output buffer with three-phase threshold voltage compensation.

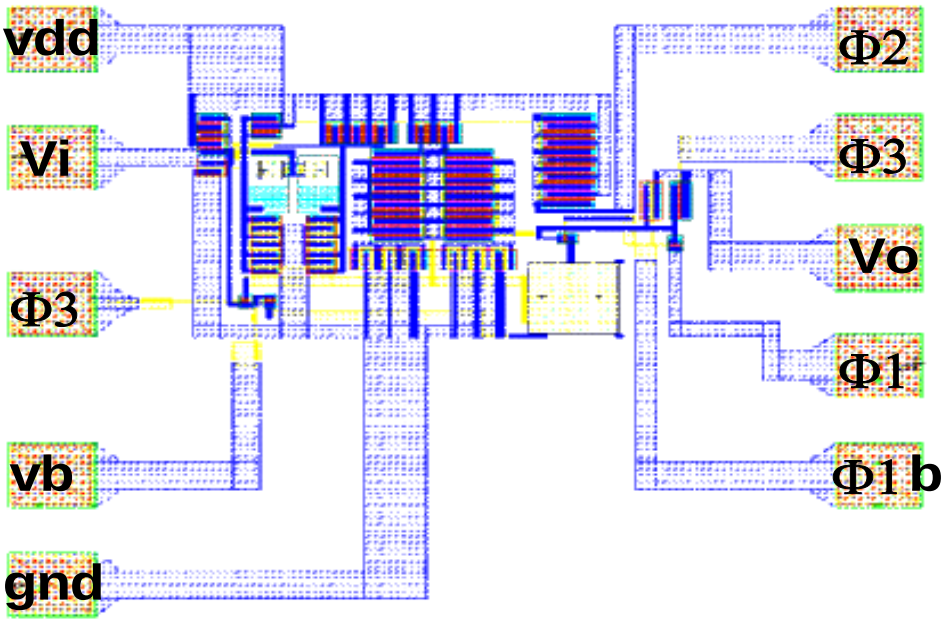


Fig. 3.24 Layout of output buffer with three-phase threshold voltage compensation.

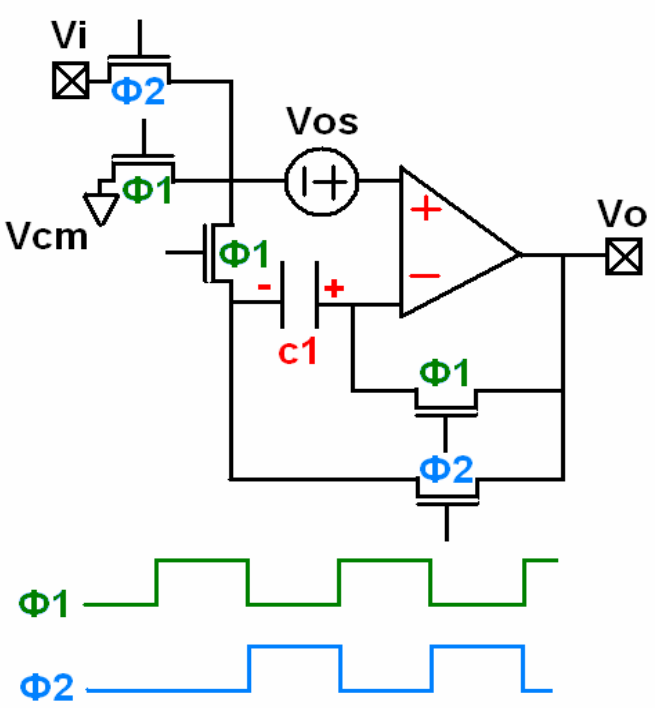


Fig. 3.25 Circuit diagram of analog output buffer with two-phase threshold voltage compensation.

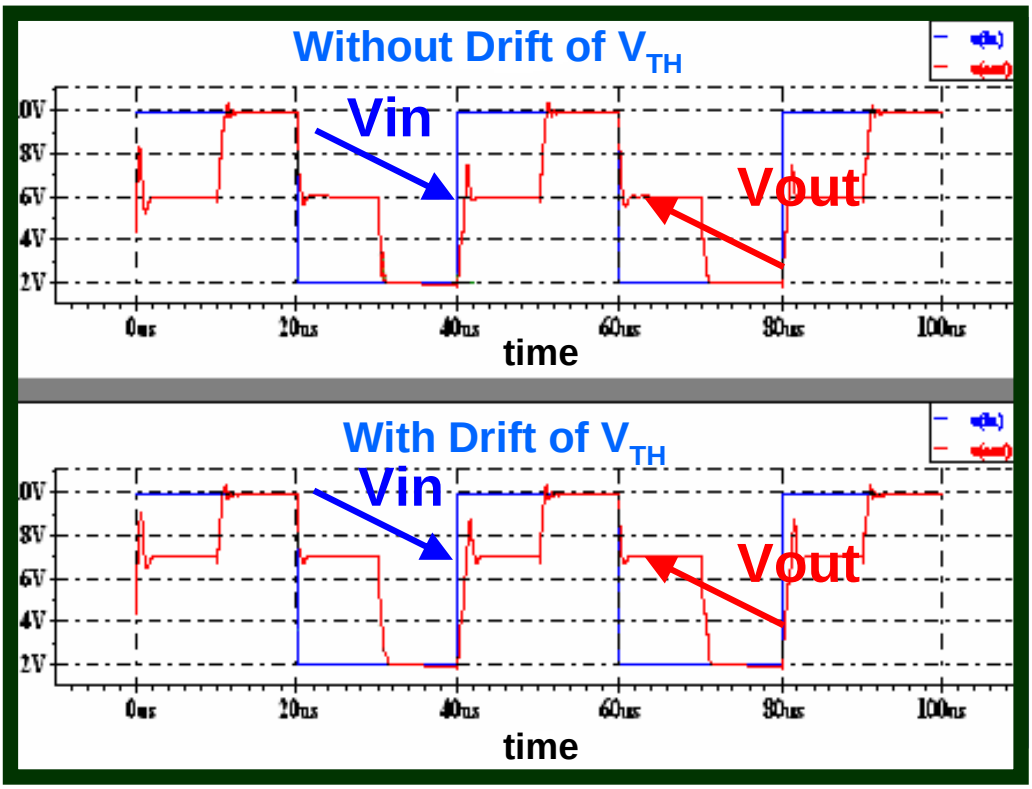


Fig. 3.26 Waveform diagram of analog output buffer with two-phase threshold voltage compensation.

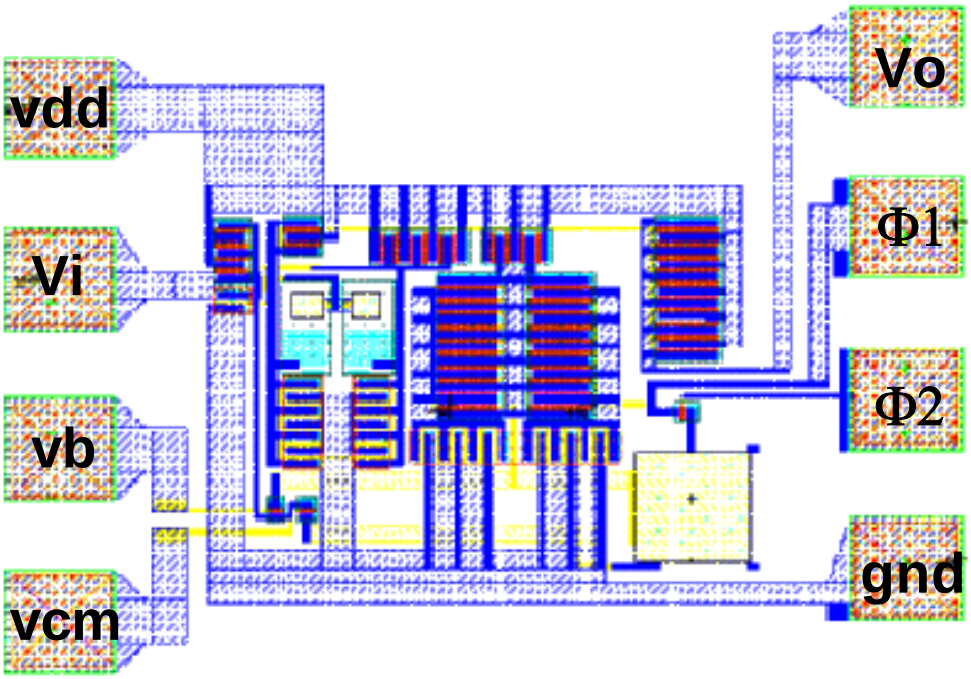


Fig. 3.27 Layout of output buffer with two-phase threshold voltage compensation.

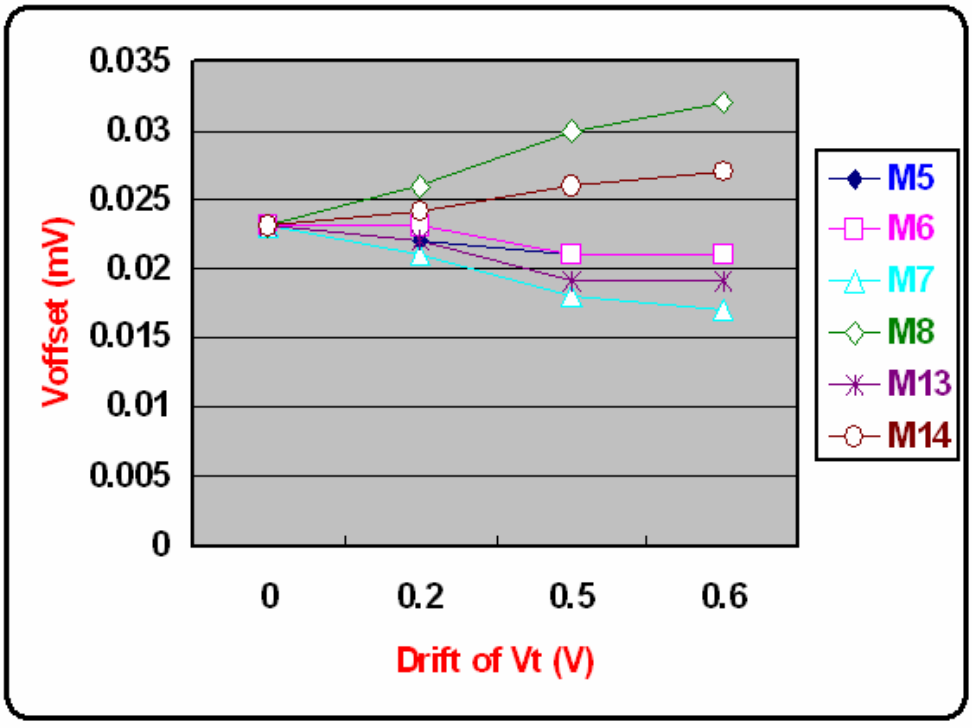


Fig. 3.28 The relationship between V_{TH} and output variation when Vin = 10 V.

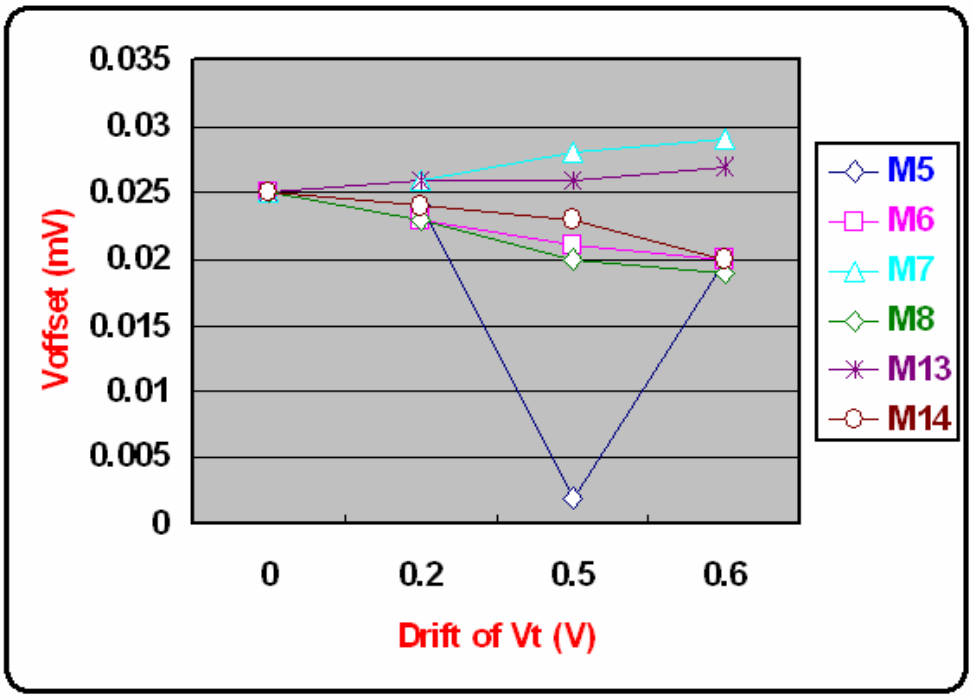


Fig. 3.29 The relationship between V_{TH} and output variation when Vin = 2 V.

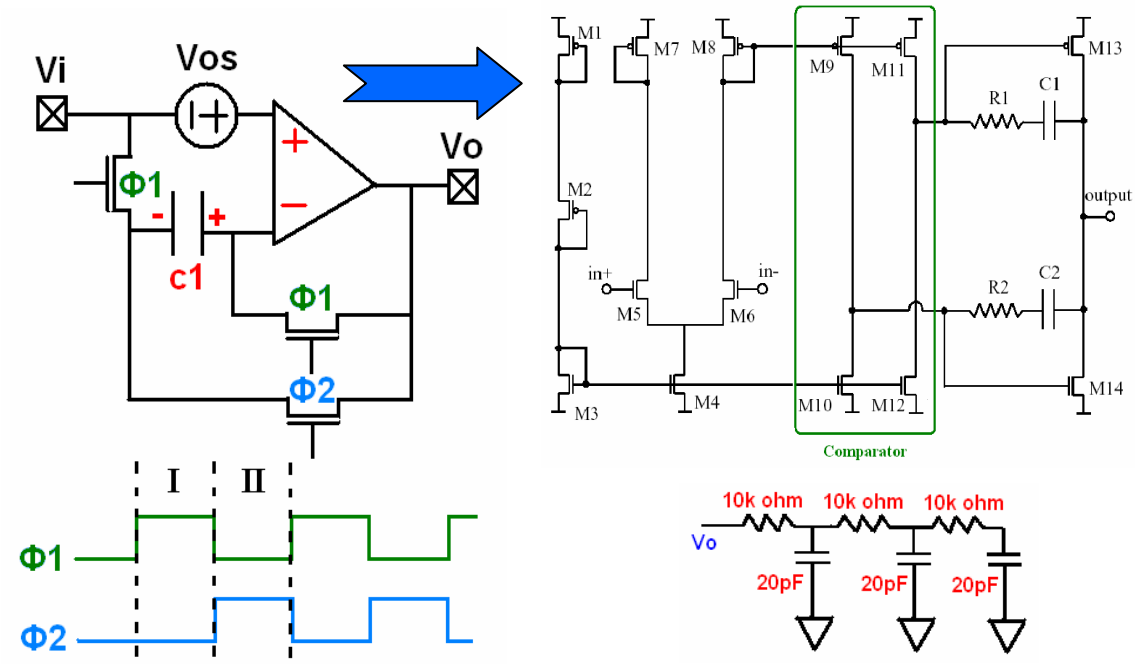


Fig. 3.30 A secondary analog output buffer with modified two-phase threshold voltage compensation.

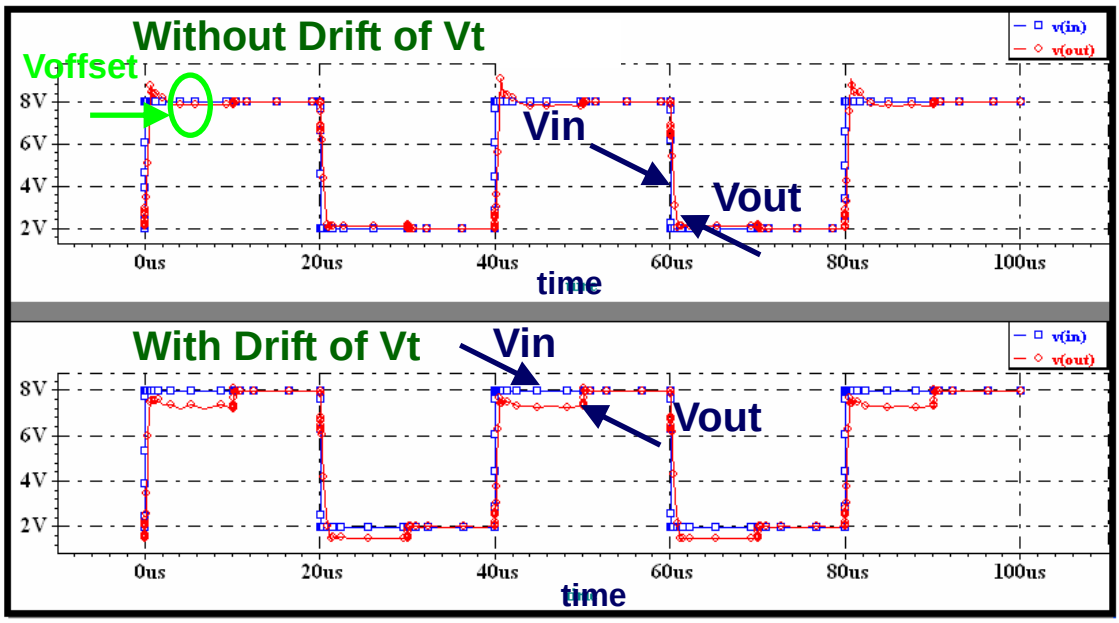


Fig. 3.31 Waveform diagram of secondary analog output buffer with modified two-phase threshold voltage compensation.

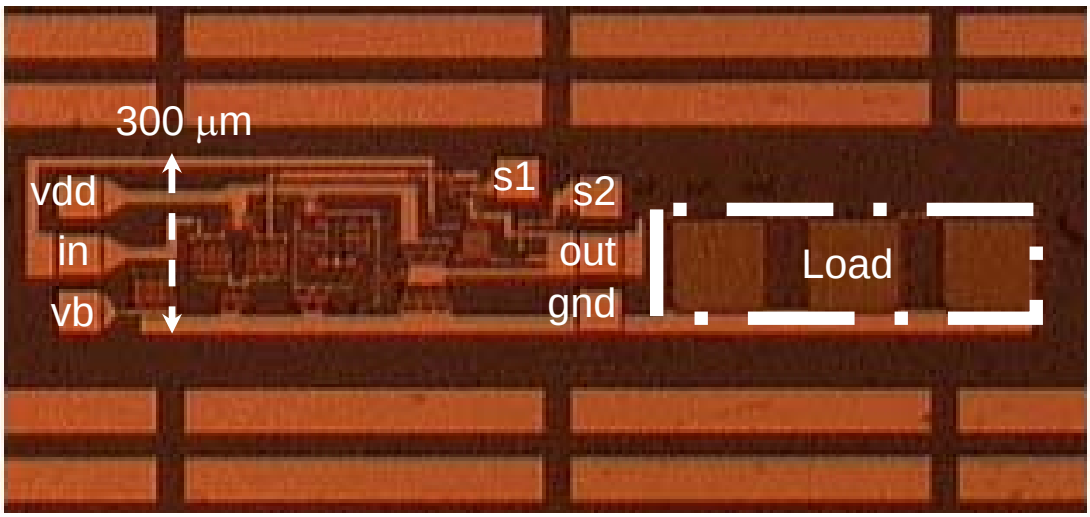


Fig. 3.32 Layout of secondary analog output buffer with modified two-phase threshold voltage compensation.

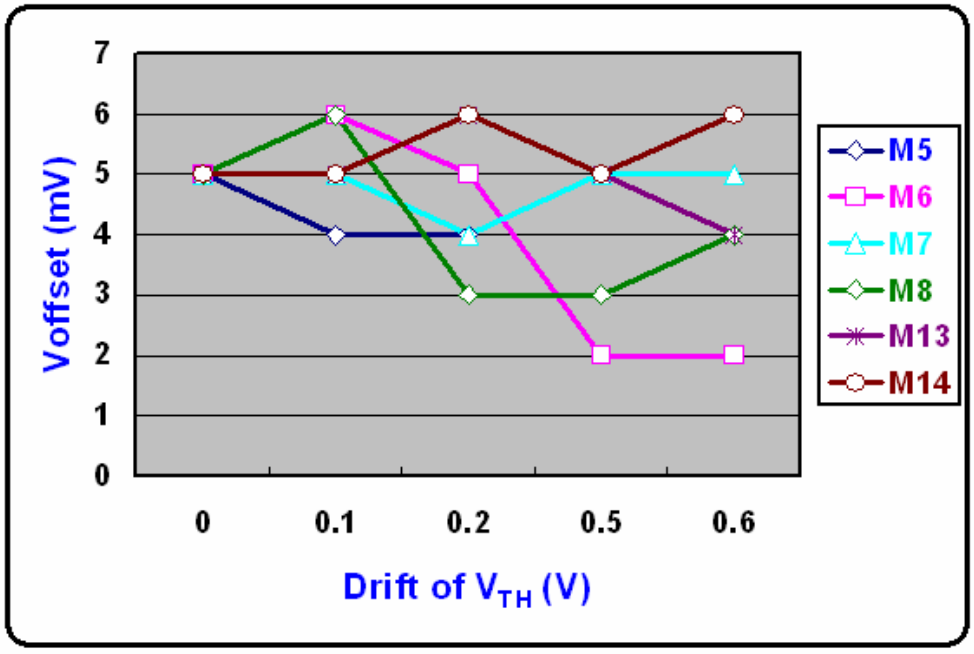


Fig. 3.33 The relationship between V_{TH} and output variation when Vin = 8 V.

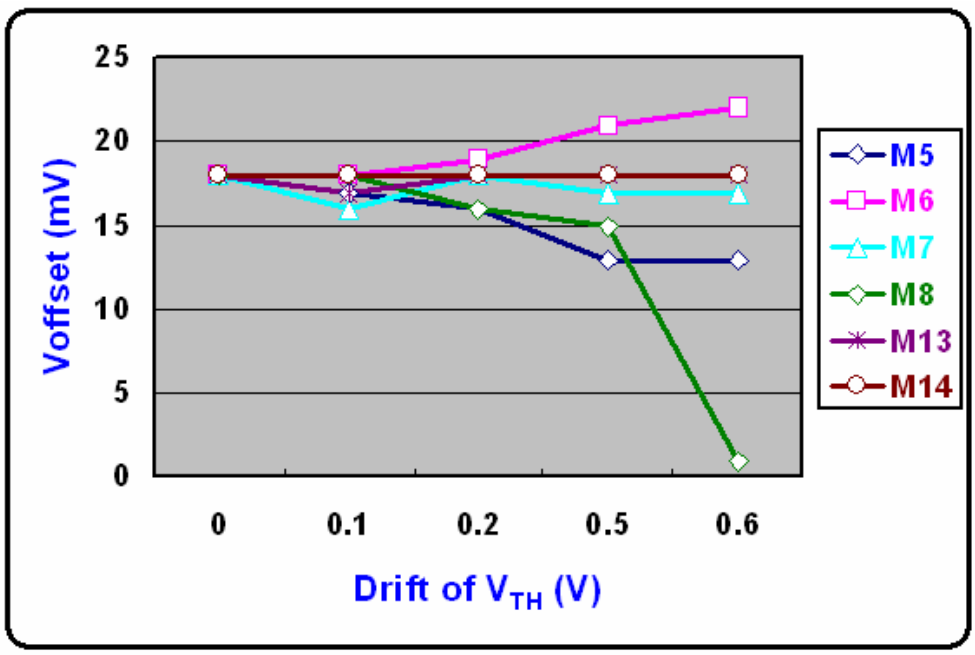


Fig. 3.34 The relationship between V_{TH} and output variation when Vin = 2 V.

CHAPTER 4

GAMMA CORRECTION DAC FOR LCD

4.1 Digital to Analog Converter

4.1.1 Resistor-String DAC

With a resistor-string approach, if the buffer's offset voltage does not depend on its input voltage, the DAC (digital to analog converter) has guaranteed monotonicity since any section on the resistor string must has a low voltage than its upper, neighbor section. In addition, the accuracy of this DAC depends on the matching precision of resistors on the resistor string. However, the matching precision of resistor depends on the process of resistors used. Fig. 4.1 and Fig. 4.2 show two types of resistor-string DAC. The major differences between them are the architecture of decoder. First type employs the tree-like decoder as its decoder, and the decoder of second type used digital method. The properties of them are compared and listed bellow:

- DAC using tree-like decoder:
  - Speed is limited by the delay through switch network.
  - Using binary coder.
- DAC using digital decoder:
  - Simple and monotonic.
  - Good DNL (differential nonlinearity) error.
  - Higher speed than tree-like decoder.
  - Large chip size at higher bits.

In summary, it can say that, both of them are suitable for gamma correction DAC,

because they are easy to produce different sections in resistor string. Furthermore, the operational speed of DAC using digital decoder is faster than DAC using tree-like decoder. But, DAC using digital decoder will consume more die area.

4.1.2 Charge-Redistribution DAC

As shown in Fig. 4.3, it is the conventional charge-redistribution DAC. In this circuit, it has two phases. In first phase ($\phi 1$), all capacitor bottom plates are connected to a reference voltage and top plates are connected to ground. During second phase ($\phi 2$), capacitor bottom plates are connected to a reference voltage or ground according to logic high or logic low in codes. And capacitor top plates are floating during this phase. By this operation, the voltage level in output terminal can be determined by a formula which is shown in follow:

$$V_O = Vref \times \left(\frac{C}{2^N C + Cp} \right) \times \sum_{i=0}^{N-1} b_i 2^i \qquad (4\text{-}1)$$

Where bi is the bit number in input code and N is the total bit number. This circuit structure has some advantages better than the resistor-string DAC. First, the process matching for capacitor is better than resistor string. Second, charge-redistribution DAC can save more power. However, it has a big problem in LCD panel application. That is, this method is very difficult to achieve gamma correction. In other word it can not compensate the inherent characteristic of liquid crystal.

4.1.3 Hybrid DAC Architecture

The benefits and drawbacks of resistor-string DAC and charge-redistribution DAC have been discussed previously. In order to get their benefits and exclude the drawbacks in gamma correction DAC, a hybrid structure has been proposed in Fig. 4.4. In this circuit, the upper bits are adopted in resistor-string architecture and the lower bits are employed the charge-redistribution structure. There are two phases in this circuit operation. In first phase (ϕ1), all capacitor bottom plates are connected to ground. During second phase (ϕ2), capacitor bottom plates are connected to a reference voltage V1 and capacitor top plates are connected to the other one V2 which is according to logic high or logic low in input codes. Furthermore, a formula about this circuit is shown in below.

$$V_O = \frac{Vref}{2^M} \times \sum_{i=0}^{M-1} b_{i+L} 2^i + \frac{Vref}{2^{M+L}} \times \sum_{j=0}^{L-1} b_j 2^j = \frac{Vref}{2^N} \times \sum_{i=0}^{N-1} b_i 2^i \quad (4\text{-}2)$$

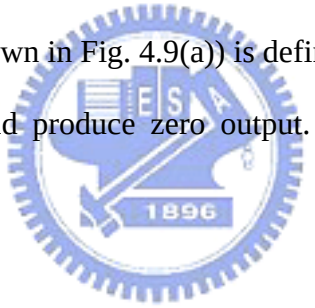
Where M is the total bit number in resistor-string DAC and L is the total bit number in charge-redistribution DAC. This hybrid structure can achieve high performance in operational speed, die area, and power consumption. Besides, it is also suitable in gamma correction DAC.

4.2 Gamma Correction DAC

4.2.1 Design of Gamma Correction DAC

Gamma correction of LCD panel involves compensating for the pixel nonlinear voltage and light modulation characteristics, so that equal changes in digital input correspond to equal changes in light transmission. Fig. 4.5(a) shows the transparency

versus operation voltage of liquid crystal and Fig 4.5 (b) shows the input codes versus transparency that gamma correction DAC must achieve. According this an input codes versus operational voltage are shown in Fig. 4.6. So, in this thesis a 6-to-64 gray level gamma correction DAC with resistor-string architecture in TOPPOLY 6-μm LTPS process is designed [11]-[12]. The full circuit diagram is shown in Fig. 4.7. The resistor values of resistor string and output loading is taken the data sheet of KS0625 in Samsung Corp. as reference. And the values are all list in Table V. In addition, the output analog buffer is employed the class-AB which is discussed in last chapter. Fig. 4.8 is the simulation waveform in TOPPOLY 6-μm LTPS model. The dynamic range is ±4 V, power consumption is 4 mW and delta is fewer than 0.5 LSB (last significant bit). Delta indicates the difference between the output value and the desired value. In a DAC, the offset error (as shown in Fig. 4.9(a)) is defined to be the output that occurs for the input code that should produce zero output. The mathematical formula is shown in below.



$$\textbf{Offset Error} = \textbf{Aos}/\Delta \qquad \textbf{Aos} = \textbf{Ao}|_{\textbf{Din=0}} \tag{4-3}$$

Besides, the gain error (as shown in Fig. 4.9(b)) is defined to be the difference at the full-scale value between the ideal and actual curves when the offset error has been reduce to zero. The formula about gain error is listed in below.

$$\textbf{Gain Error} = (\textbf{Ao.max} - \textbf{Aos})/[(2N-1)\Delta] \tag{4-4}$$

After both the gain error and offset error have been removed, INL error (as shown in Fig. 4.10) is defined to be the deviation from a desired line. Fig. 4.11 and Fig. 4.12 show the delta and INL error of the proposed gamma correction DAC, respectively.

As it can see, the delta and INL are both less than 0.5 LSB when the input codes are employed and this are suitable for LCD panel.

4.2.2 Measurement Result

Fig. 4.13 is the full layout in TOPPOLY 6-μm LTPS process. Region A is the sample of resistor-string and region C is the TFT devices. The glass sample of this layout is shown in Fig. 4.14. At first, the TFT devices are measured and shown in Fig. 4.15(a) and Fig. 4.15(b). According to constant current method, it can get the threshold voltage of N-TFT (8 μm/6 μm) device is 0.66 V and P-TFT (8 μm/6 μm) device is -1.05 V. This value of threshold voltage is almost the same as simulation which are shown in Fig. 4.16(a) and Fig. 4.16(b). Then, the boding diagram of 6-to-64 gray level gamma correction DAC is shown in Fig. 4.17. The measurement results of the output data are listed in Table VI. Besides, Fig. 4.18 and Fig. 4.19 are the plots of the delta and INL error, respectively. Where the resistors ratio (R0:R1:R3) of resistor string are 6:3:2. It shows that the delta is less than 4LSB and the INL error is less than 2.5LSB. These results seem not to fit the simulation result, and it will not be suitable for LCD panel. According to the detailed discussions and inspections, these deviations can impute the un-matching resistors in resistor string. And the advanced analysis of the resistor deviations will be discussed in next section.

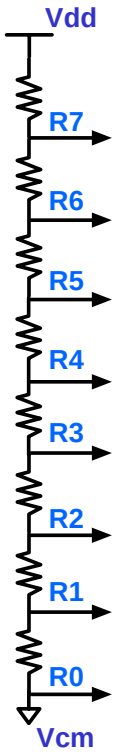
4.2.3 Analysis in Resistor and Capacitor Sample

Due to the process variation in resistors, an advance analysis in resistor is discussed now. As show in Fig. 4.20, the R0, R1 and R2 are resistor samples which are made in metal1. The ratio of these resistor samples are 6:3:2 in layout. In addition,

R_{Poly} is resistor made in poly with N doping and C is capacitor sample made in metal1 and poly. About above samples are all measured and list in Table VII. The total panel numbers are 6, and the average of this measurement results are also show in this table. According this table, the deviations of these resistors in different glass panels are compared in Fig. 4.21. As it can observe, the variation to the average value are up to 20% in worst case. And this is why the performance of the 6-to-64 gray level gamma correction DAC is not the same as the anticipation. In order to overcome these unexpected results, the layout ratio of width and length in resistor of gamma correction DAC can be drawn to larger. Moreover, DAC using capacitors can also be employed to reduce the process variation. And, Fig. 4.22 is the measurement results of capacitor samples in TOPPOLY 6-μm LTPS process. As it can see, the variations in different panels are less than the variations of resistor samples which are already discussed previously.

Table V

The resistor values of resistor string.



R0	4.08 kΩ	R1	2.04 kΩ	R2	1.36 kΩ	R3	1.36 kΩ
R00	510 Ω	R10	255 Ω	R20	170 Ω	R30	170 Ω
R01	510 Ω	R11	255 Ω	R21	170 Ω	R31	170 Ω
R02	510 Ω	R12	255 Ω	R22	170 Ω	R32	170 Ω
R03	510 Ω	R13	255 Ω	R23	170 Ω	R33	170 Ω
R04	510 Ω	R14	255 Ω	R24	170 Ω	R34	170 Ω
R05	510 Ω	R15	255 Ω	R25	170 Ω	R35	170 Ω
R06	510 Ω	R16	255 Ω	R26	170 Ω	R36	170 Ω
R07	510 Ω	R17	255 Ω	R27	170 Ω	R37	170 Ω
R4	1.36 kΩ	R5	1.36 kΩ	R6	2.04 kΩ	R7	4.08 kΩ
R40	170 Ω	R50	170 Ω	R60	255 Ω	R70	510 Ω
R41	170 Ω	R51	170 Ω	R61	255 Ω	R71	510 Ω
R42	170 Ω	R52	170 Ω	R62	255 Ω	R72	510 Ω
R43	170 Ω	R53	170 Ω	R63	255 Ω	R73	510 Ω
R44	170 Ω	R54	170 Ω	R64	255 Ω	R74	510 Ω
R45	170 Ω	R55	170 Ω	R65	255 Ω	R75	510 Ω
R46	170 Ω	R56	170 Ω	R66	255 Ω	R76	510 Ω
R47	170 Ω	R57	170 Ω	R67	255 Ω	R77	510 Ω

Table VI

The measurement results of gamma correction DAC.

Code	0	1	2	3	4	5	6	7	LSB(V)	Offset(V)	Gain Error	(LSB)
Idea(V)	9.893701	9.787402	9.681102	9.5748031	9.4685039	9.362205	9.255906	9.149606	0.106299			
Sim.(V)	9.8383	9.7279	9.6116	9.5009	9.3846	9.2739	9.1576	9.0469	0.106299	0.03	0.62941	(LSB)
Meas.(V)	9.872	9.747	9.622	9.492	9.3631	9.241	9.114	9.091	0.106299			
INL(LSB)	-1.11578	-1.20179	-1.2878	-1.42085	-1.54355	-1.60228	-1.7071	-0.8336				
ΔM(LSB)	-0.20415	-0.38007	-0.556	-0.77896	-0.99158	-1.14022	-1.335	-0.5513				
Code	8	9	10	11	12	13	14	15	LSB	Offset	Gain Error	(LSB)
Idea(V)	9.09252	9.035433	8.978346	8.9212598	8.8641732	8.807087	8.75	8.692913	0.057087			
Sim.(V)	8.997	8.9361	8.8808	8.8254	8.7701	8.7147	8.6593	8.5984	0.057087	0.03	0.74087	(LSB)
Meas.(V)	9.0392	8.9372	8.9073	8.8211	8.7722	8.7014	8.63446	8.6273	0.057087			
INL(LSB)	-2.2004	-2.88132	-2.29925	-2.7034	-2.45415	-2.58853	-2.6553	-1.6749				
ΔM(LSB)	-0.93401	-1.72077	-1.24454	-1.75452	-1.61112	-1.85134	-2.0239	-1.1494				
Code	16	17	18	19	20	21	22	23	LSB	Offset	Gain Error	(LSB)
Idea(V)	8.649606	8.606299	8.562992	8.519685	8.476378	8.433071	8.389764	8.346457	0.043307			
Sim.(V)	8.5896	8.5468	8.5198	8.4627	8.4357	8.3886	8.3515	8.3145	0.043307	0.03	-3.1715	(LSB)
Meas.(V)	8.4272	8.4195	8.3915	8.3637	8.3367	8.3191	8.3001	8.2914	0.043307			
INL(LSB)	-2.65676	-2.28764	-2.38726	-2.48226	-2.55879	-2.41827	-2.3101	-1.964				
ΔM(LSB)	-5.13556	-4.31336	-3.95991	-3.60184	-3.22529	-2.63169	-2.0704	-1.2713				
Code	24	25	26	27	28	29	30	31	LSB	Offset	Gain Error	(LSB)
Idea(V)	8.30315	8.259843	8.216535	8.1732283	8.1299213	8.086614	8.043307	8	0.043307			
Sim.(V)	8.2774	8.2404	8.1913	8.1662	8.1192	8.0952	8.0471	8.0151	0.043307	0.03	-1.9223	(LSB)
Meas.(V)	8.2304	8.2022	8.1741	8.1485	8.1207	8.0961	8.0683	8.0405	0.043307			
INL(LSB)	-0.45027	-0.37605	-0.29952	-0.16526	-0.08181	0.07554	0.159	0.24245				
ΔM(LSB)	-1.67985	-1.33102	-0.97987	-0.571	-0.21293	0.21904	0.57711	0.93518				

Table VI
The measurement results of gamma correction DAC (contd.).

Code	32	33	34	35	36	37	38	39	LSB	Offset	Gain Error	(LSB)
Idea(V)	7.956693	7.913386	7.870079	7.8267717	7.7834646	7.740157	7.69685	7.653543	0.043307			
Sim.(V)	7.9631	7.9324	7.8655	7.8481	7.8112	7.7743	7.7452	7.6983	0.043307	0.03	0.79318	(LSB)
Meas.(V)	8.0118	7.9871	7.9596	7.9319	7.9071	7.8793	7.8525	7.7043	0.043307			
INL(LSB)	-0.21344	0.32953	0.80784	1.28154	1.82219	2.29358	2.78805	0.47929				
ΔM(LSB)	1.27247	1.70213	2.06713	2.42751	2.85485	3.21293	3.59409	1.17202				
Code	40	41	42	43	44	45	46	47	LSB	Offset	Gain Error	(LSB)
Idea(V)	7.610236	7.566929	7.523622	7.480315	7.4370079	7.393701	7.350394	7.307087	0.043307			
Sim.(V)	7.6414	7.6071	7.5748	7.5466	7.5114	7.4618	7.4279	7.3827	0.043307	0.03	-1.9431	(LSB)
Meas.(V)	7.5432	7.5175	7.4898	7.4619	7.4343	7.4084	7.3821	7.3542	0.043307			
INL(LSB)	-0.29756	-0.16858	-0.08579	-0.00761	0.0775	0.20186	0.31698	0.39516				
ΔM(LSB)	-1.54793	-1.14136	-0.78098	-0.42522	-0.06253	0.33942	0.73213	1.08789				
Code	48	49	50	51	52	53	54	55	LSB	Offset	Gain Error	(LSB)
Idea(V)	7.25	7.192913	7.135827	7.0787402	7.0216535	6.964567	6.90748	6.850394	0.057087			
Sim.(V)	7.3391	7.2869	7.2262	7.1725	7.1147	7.0582	7.0031	6.9452	0.057087	0.03	1.52564	(LSB)
Meas.(V)	7.2864	7.2217	7.1712	7.1119	7.0461	6.9787	6.9108	6.8297	0.057087			
INL(LSB)	-1.41353	-1.32895	-0.99562	-0.81644	-0.75113	-0.71384	-0.6853	-0.888				
ΔM(LSB)	0.63763	0.50426	0.61964	0.58087	0.42823	0.24757	0.05815	-0.3625				
Code	56	57	58	59	60	61	62	63	LSB	Offset	Gain Error	(LSB)
Idea(V)	6.744094	6.637795	6.531496	6.4251969	6.3188976	6.212598	6.106299	6	0.106299			
Sim.(V)	6.8403	6.7234	6.6095	6.4956	6.3821	6.2698	6.1557	6.001	0.106299	0.03	0.19384	(LSB)
Meas.(V)	6.7647	6.6603	6.5412	6.4281	6.3034	6.2212	6.1292	6.03	0.106299			
INL(LSB)	-0.28222	-0.23666	-0.32939	-0.36568	-0.51109	-0.25669	-0.0945	2.3E-15				
ΔM(LSB)	0.19384	0.21171	0.09129	0.02731	-0.14579	0.08092	0.21544	0.28222				

Table VII
The resistor values of resistor string.

	R0	**R1**	**R2**	**Rpoly**	**C**
Panel 1	18.419 Ω	10.810 Ω	6.507 Ω	126.760 Ω	1.600 pF
Panel 2	17.298 Ω	12.065 Ω	8.877 Ω	133.825 Ω	1.595 pF
Panel 3	17.948 Ω	10.130 Ω	7.417 Ω	129.995 Ω	1.620 pF
Panel 4	19.285 Ω	10.970 Ω	7.567 Ω	109.810 Ω	1.615 pF
Panel 5	19.333 Ω	11.132 Ω	7.522 Ω	109.360 Ω	1.590 pF
Panel 6	19.031 Ω	10.886 Ω	7.364 Ω	103.595 Ω	1.605 pF

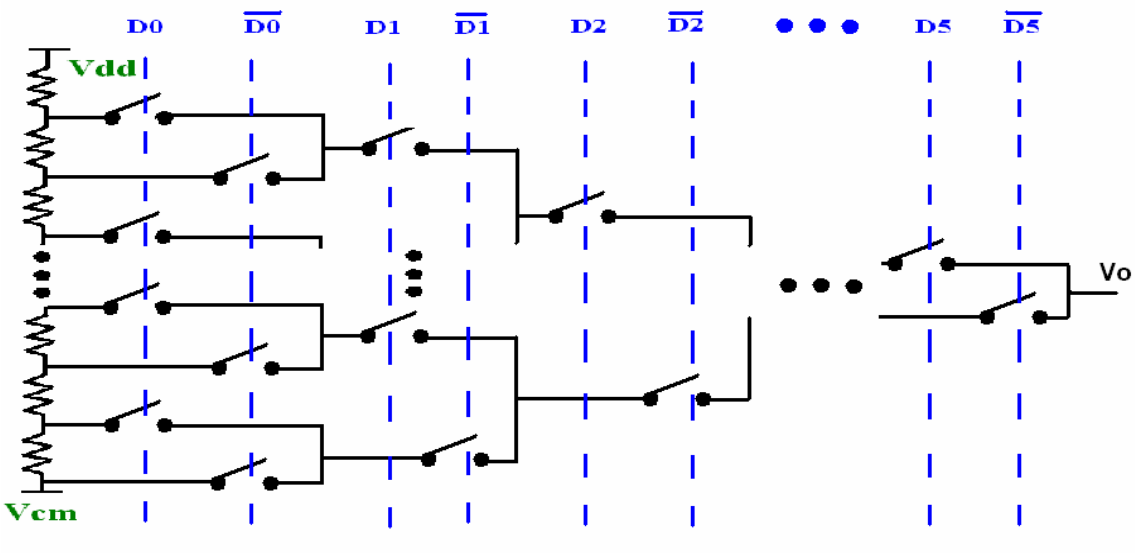


Fig. 4.1 DAC using tree-like decoder.

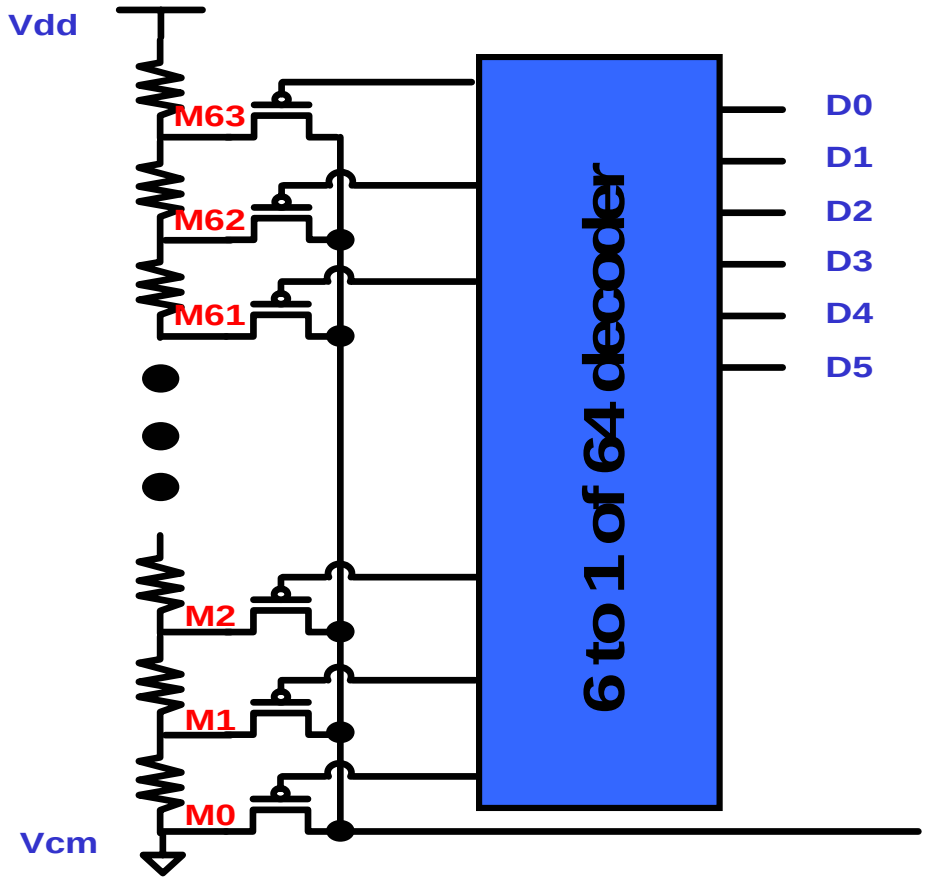


Fig. 4.2 DAC using digital decoder.

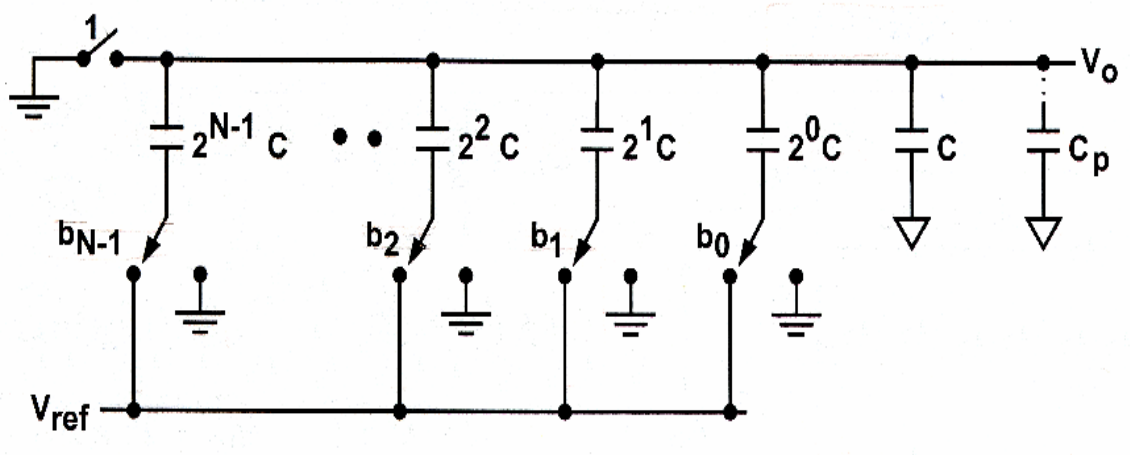


Fig. 4.3 Charge-redistribution DAC.

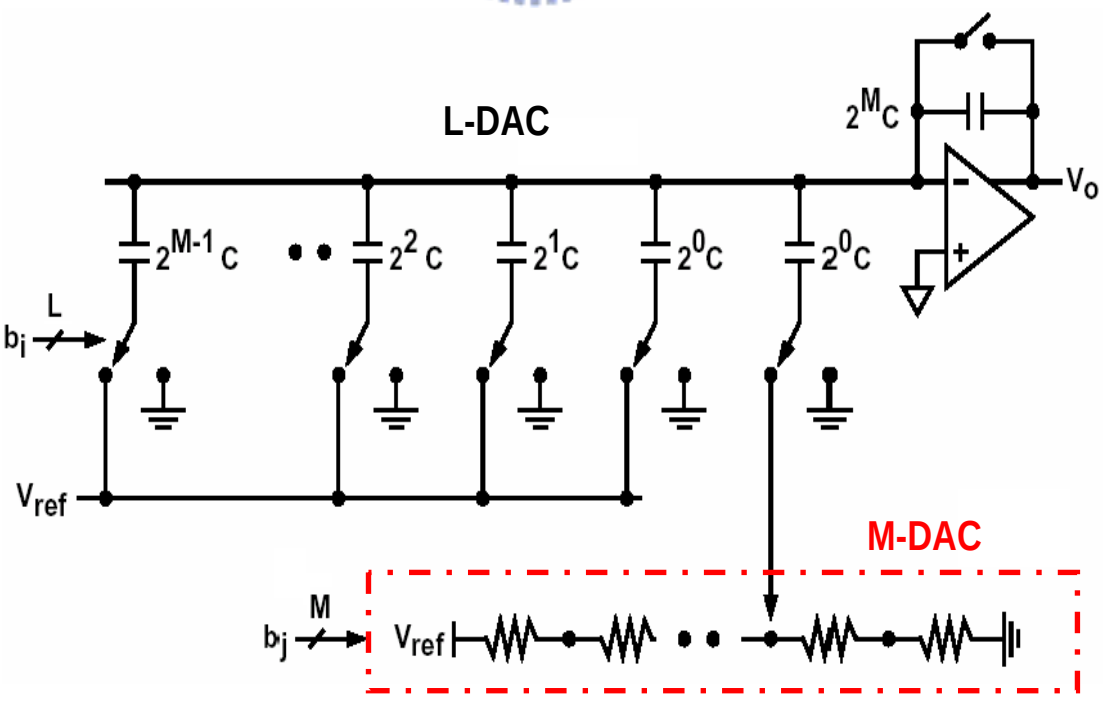


Fig. 4.4 A hybrid structure of gamma correction DAC.

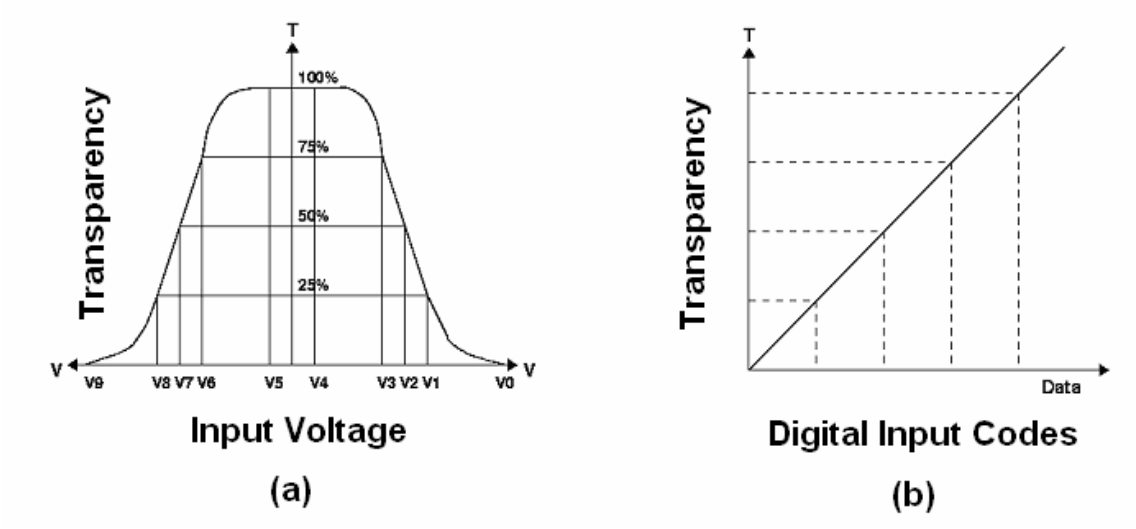


Fig. 4.5(a) shows the transparency versus operation voltage of liquid crystal and (b) shows the input codes versus transparency.

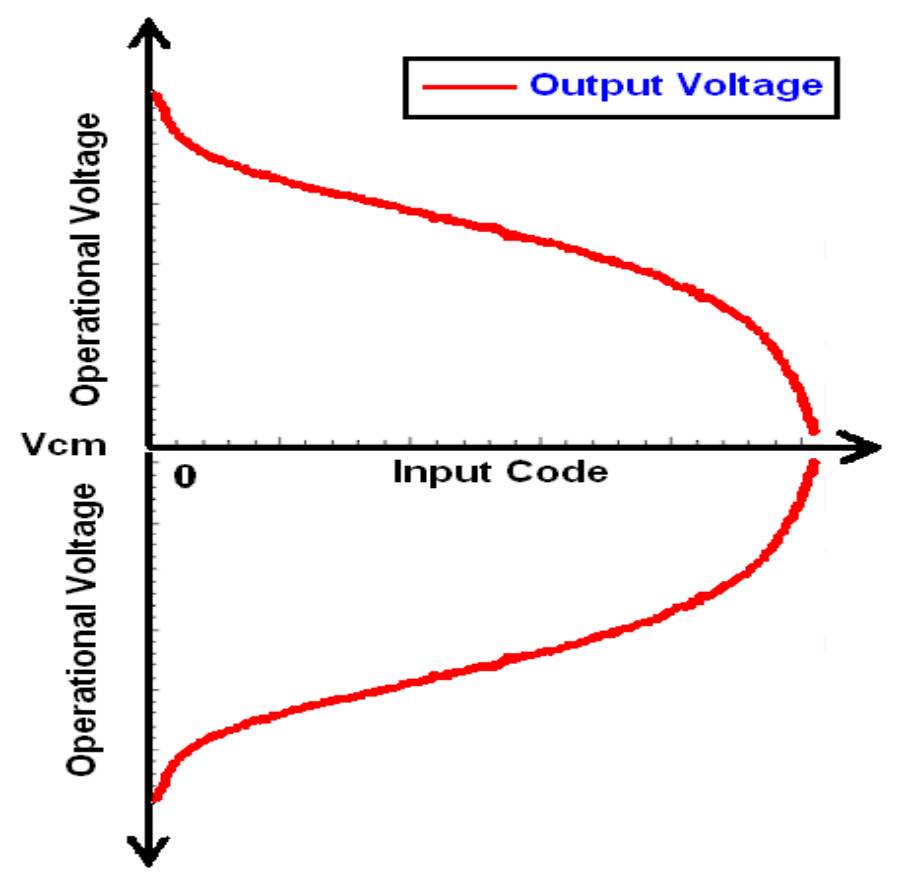


Fig. 4.6 Input codes versus operational voltage.

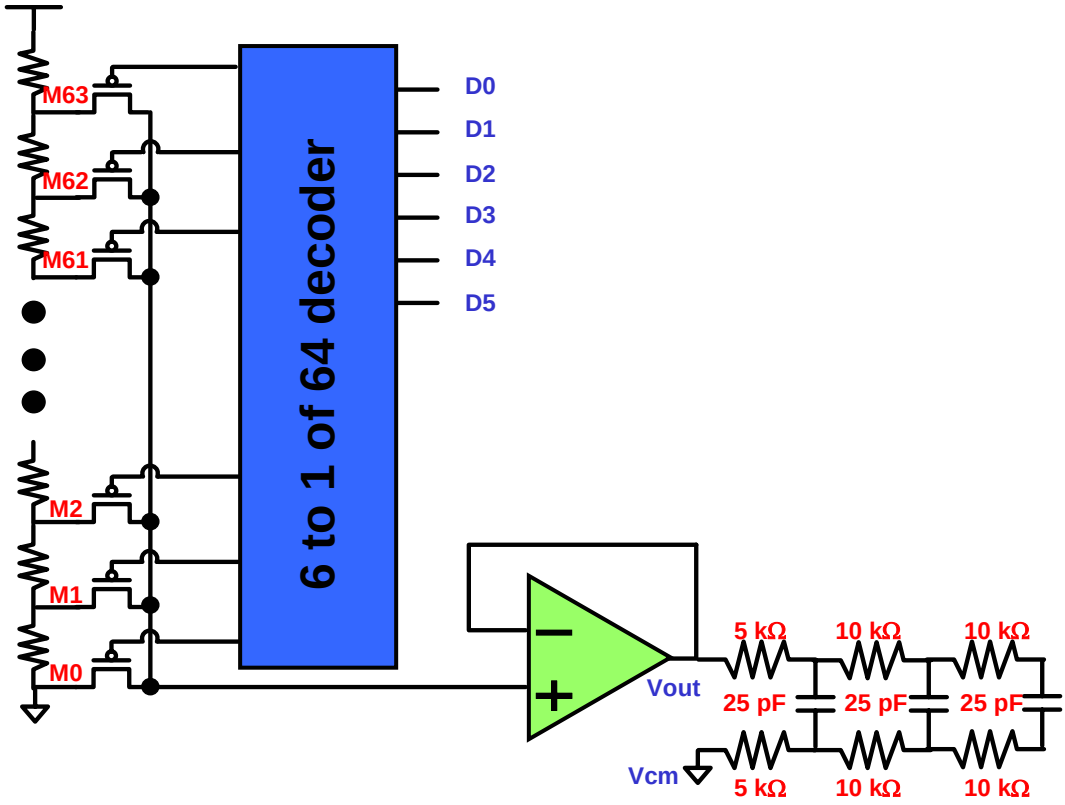


Fig. 4.7 A 6-to-64 gray level gamma correction DAC with resistor-string architecture.

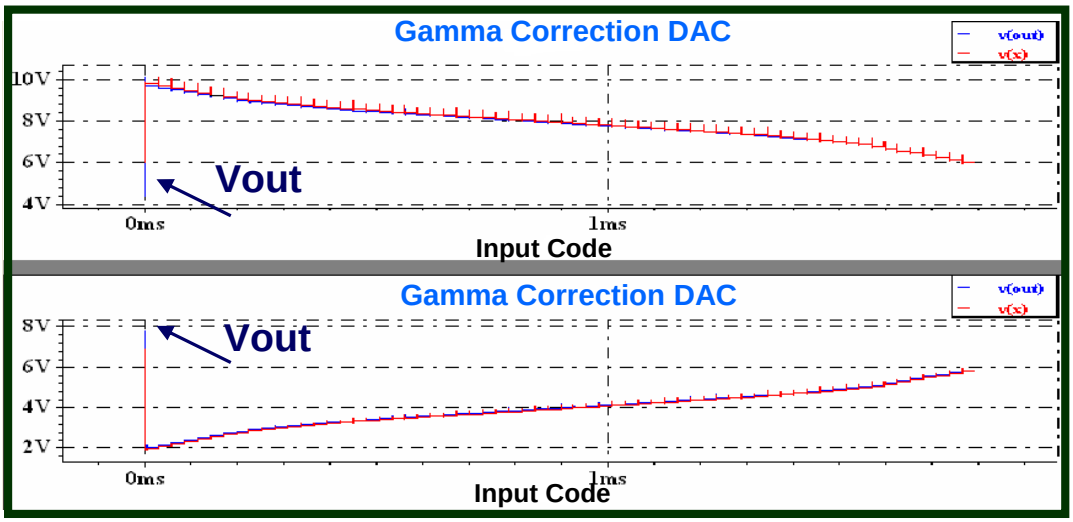


Fig. 4.8 The simulation waveform of gamma correction DAC with resistor-string architecture.

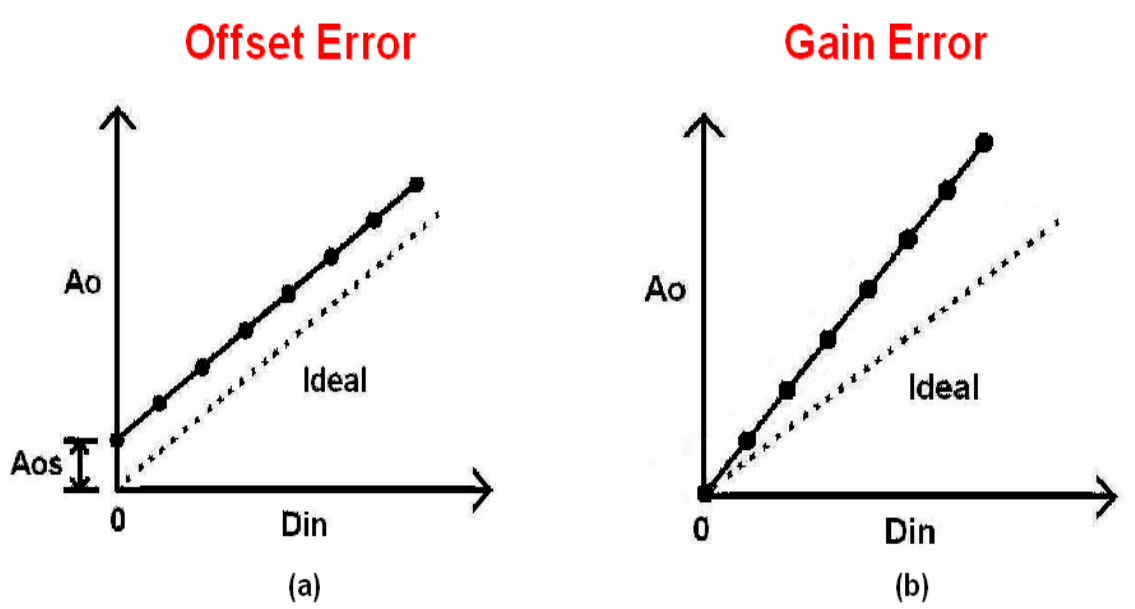


Fig. 4.9 The definitions of (a) offset error and (b) gain error.

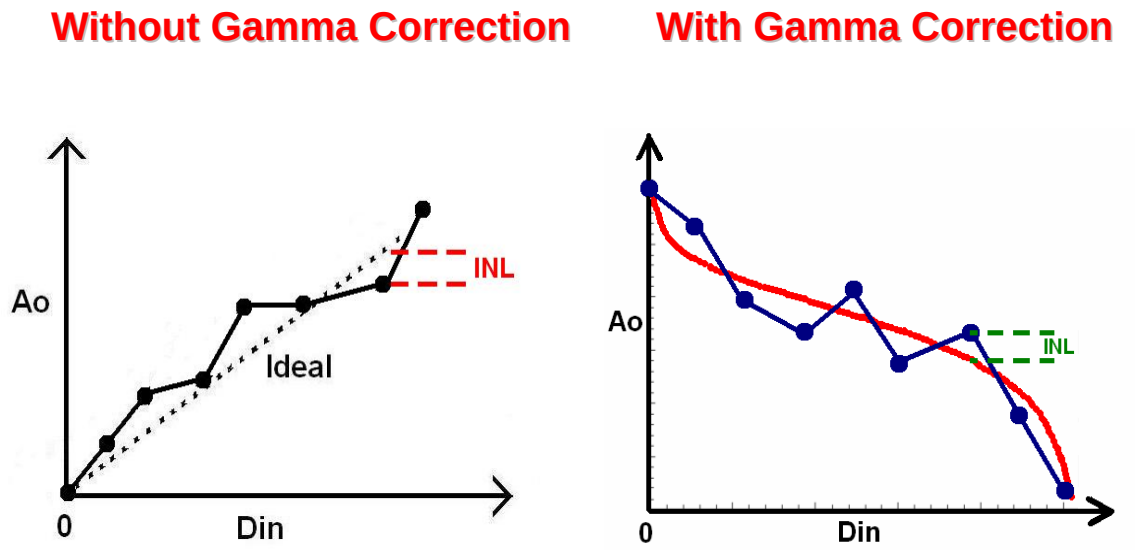
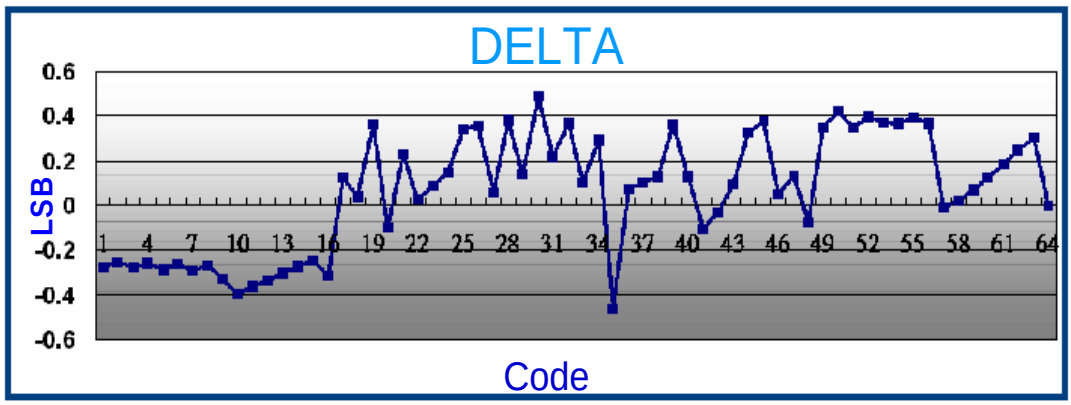


Fig. 4.10 The definition of INL error.

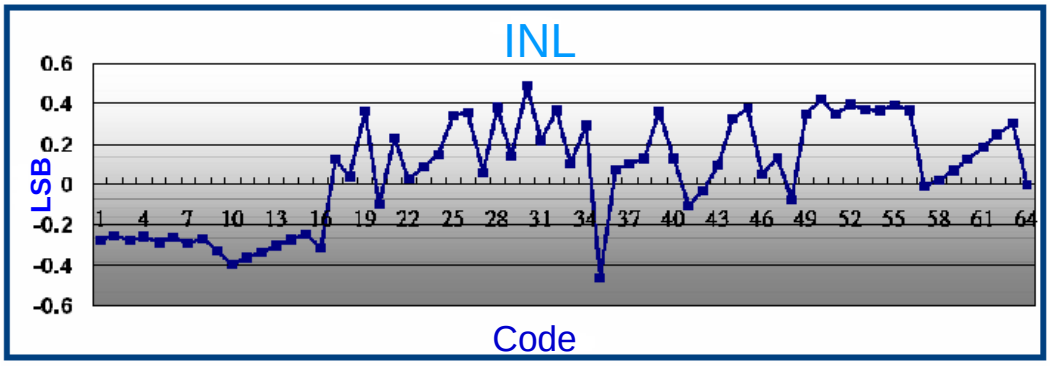
R0:R1:R2 = 6:3:2



➢Delta < 0.5 LSB

Fig. 4.11 Delta of the proposed gamma correction DAC.

R0:R1:R2 = 6:3:2



➢INL < 0.5 LSB

Fig. 4.12 INL error of the proposed gamma correction DAC.

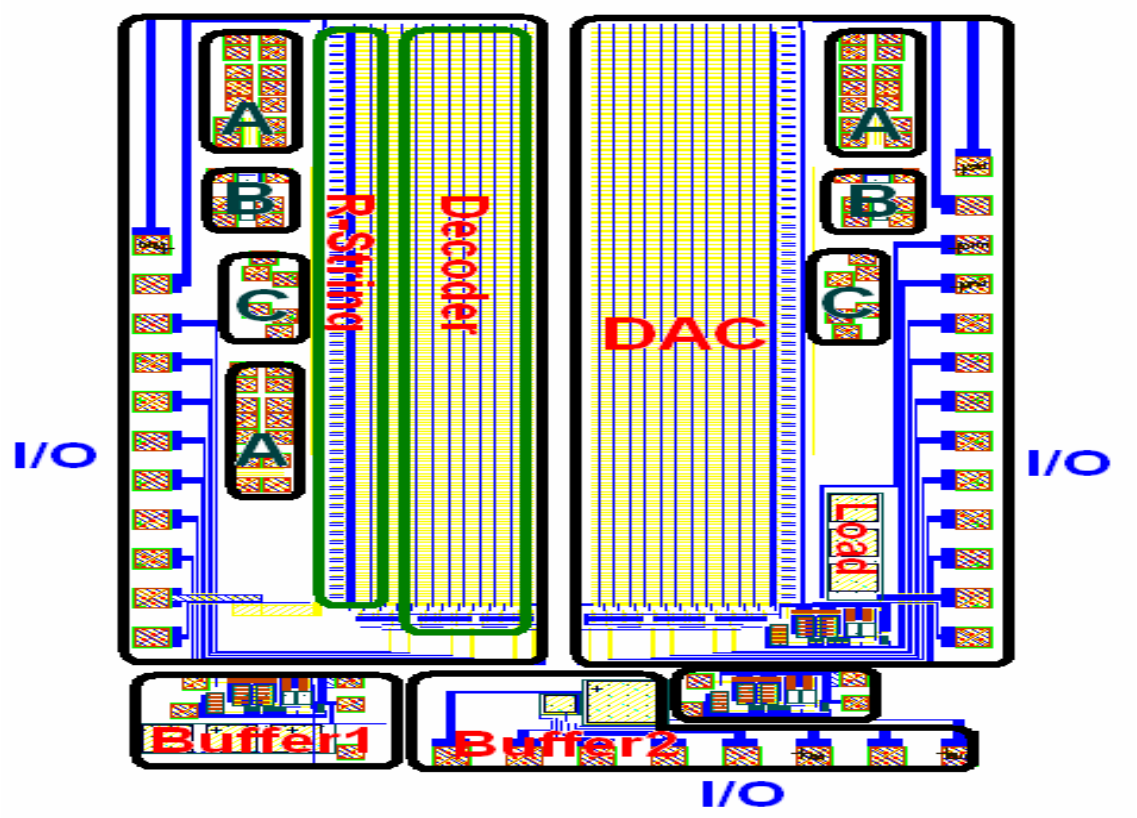


Fig. 4.13 The full layout in TOPPOLY 6-μm LTPS process.

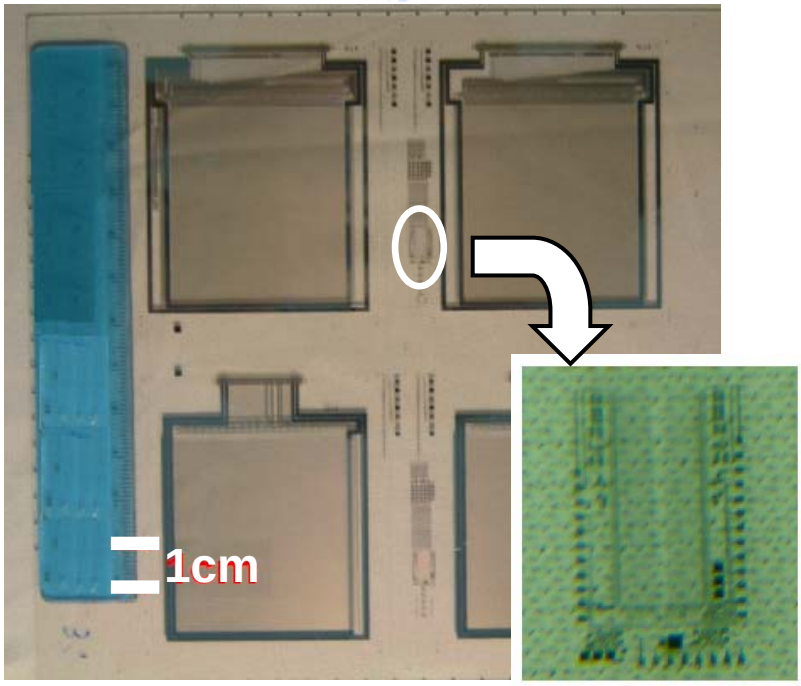


Fig. 4.14 The glass sample of gamma correction DAC.

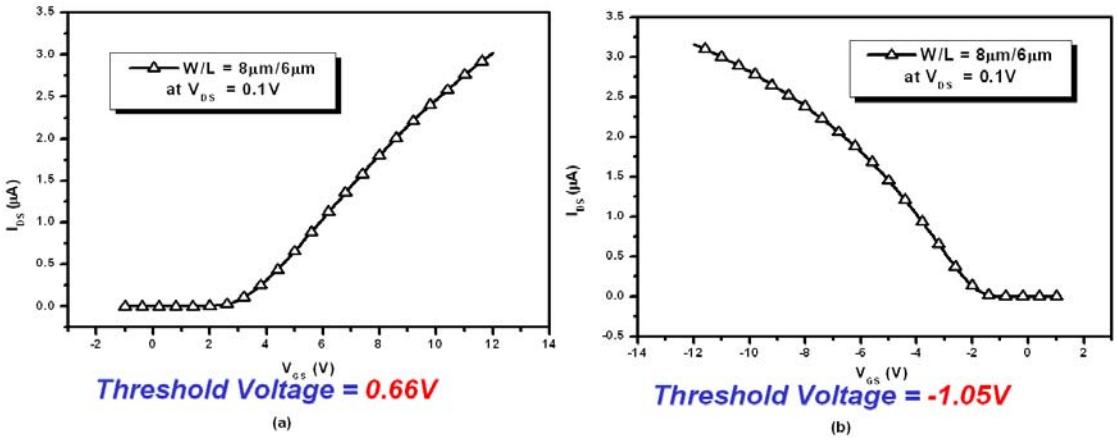


Fig. 4.15 The measurement result of (a) N-TFT device and (b) P-TFT device.

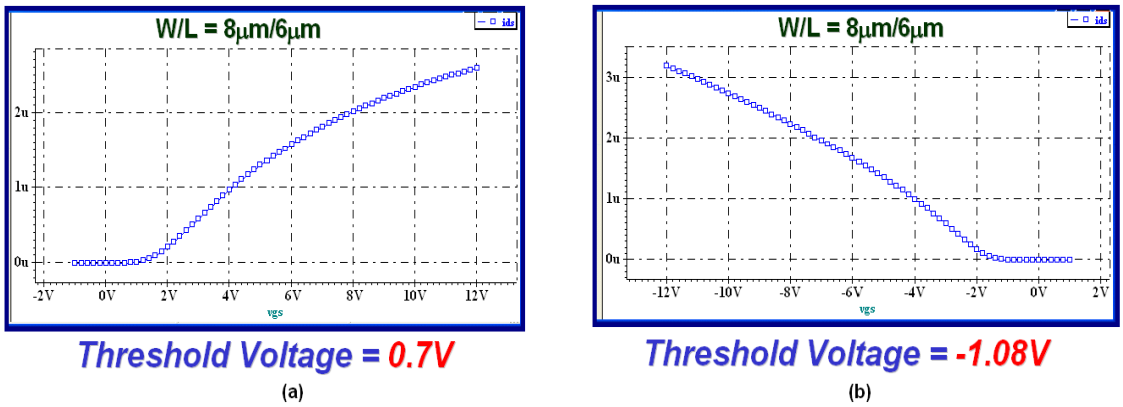


Fig. 4.16 The simulation result of (a) N-TFT device and (b) P-TFT device.

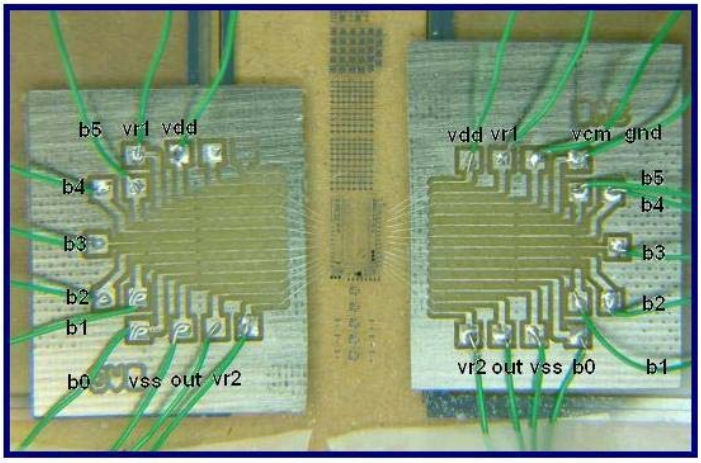
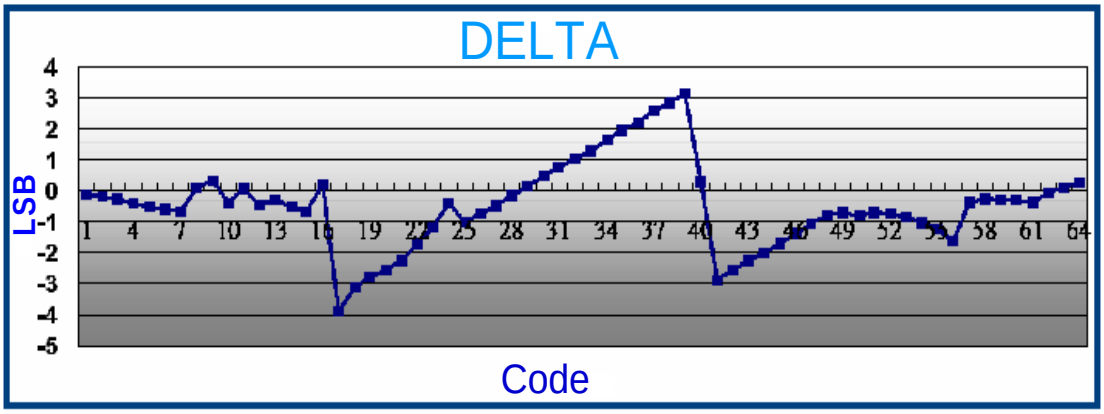


Fig. 4.17 The boding diagram of 6-to-64 gray level gamma correction DAC

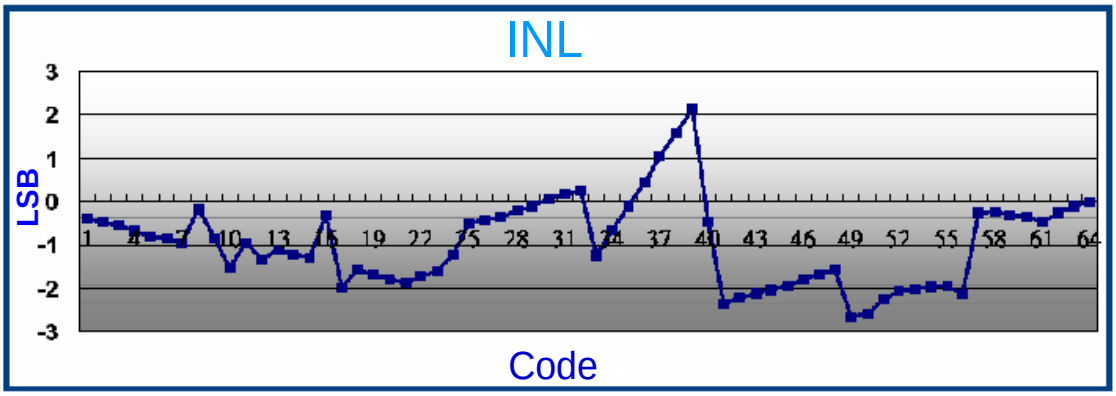
R0:R1:R2 = 6:3:2



➢Delta < 4 LSB

Fig. 4.18 The measurement result of delta.

R0:R1:R2 = 6:3:2



➢INL < 2.5 LSB

Fig. 4.19 The measurement result of INL error.

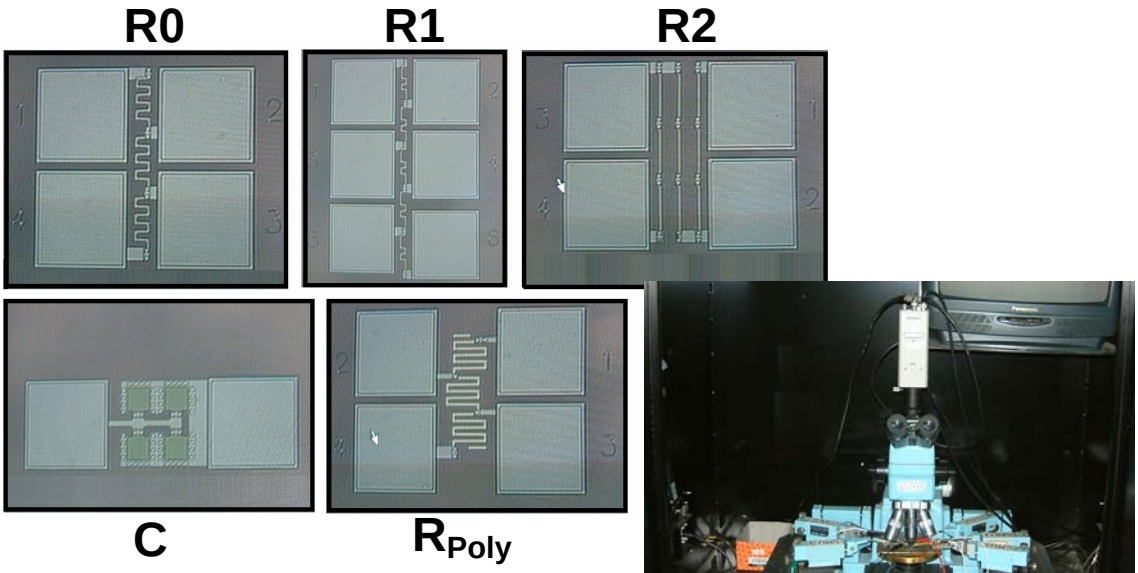


Fig. 4.20 The resistor samples made in metal1 which ratio are 6:3:2 in layout.

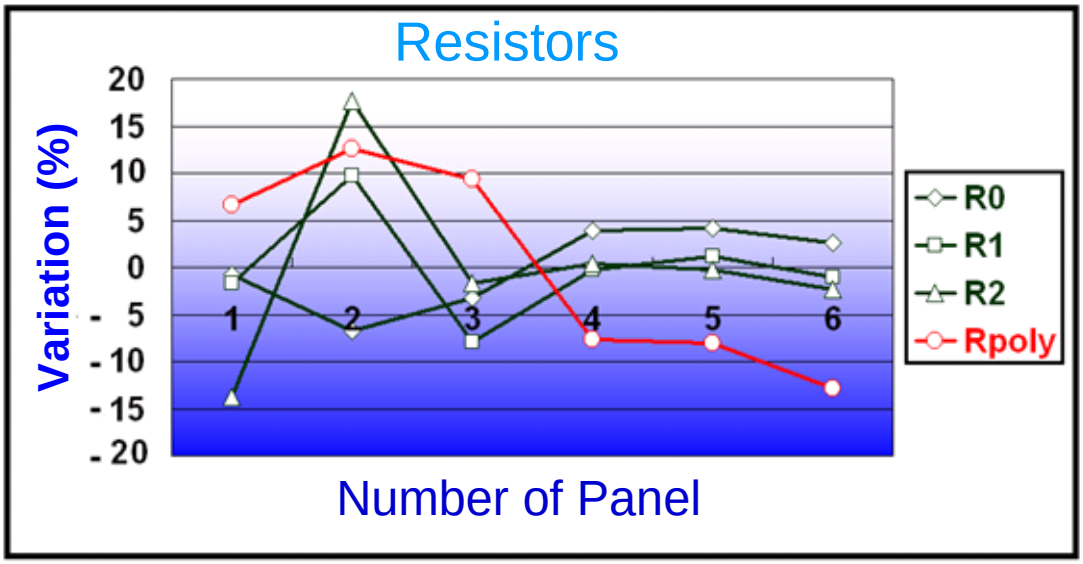


Fig. 4.21 The deviations of resistors in different glass panels.

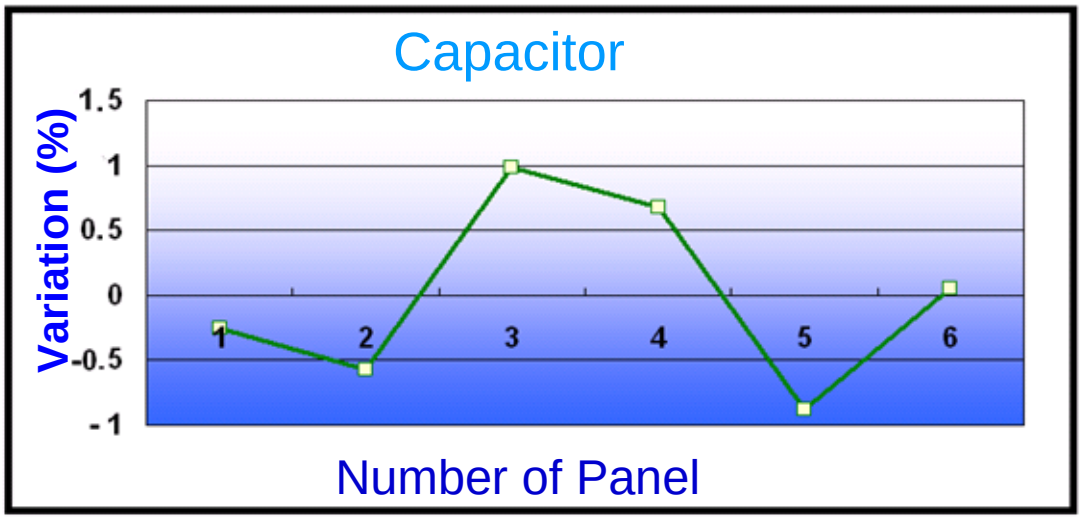


Fig. 4.22 The deviations of capacitors in different glass panels

CHAPTER 5

LEVEL SHIFTER USING BODY BIAS

5.1 SOI CMOS with Body Bias

Comparing with bulk CMOS (complementary-metal-oxide-silicon) technology, SOI (silicon-on-insulator) technology is more attractive for low-power and high-performance applications. Using SOI technology, the latch-up can be eliminated and the integration density can be improved. According above reasons, SOI device is widely used in some application. Fig. 5.1(a) is the cross section of SOI NMOS device [16]-[20]. As usual, SOI can be roughly classified into PDSOI (partial depleted SOI) and FDSOI (fully depleted SOI) according to the thickness of thin film on the buried oxide. The thin of PDSOI is thicker and only the top portion of it is depleted when the bottom portion is neutral. On the contrary, the thin film of FDSOI is fully depleted. The detailed comparisons of PDSOI device and FDSOI device are listed below:

PDSOI device:

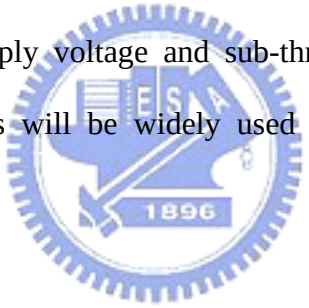
- Kink effect in I-V curve due to floating body.
- Parasitic lateral BJT (bipolar junction transistor) operation.
- Body contact is needed.

- FDSOI device:
  - V_{TH} (threshold voltage) variation with thickness of silicon thin film.
  - No kink effect in I-V curve.
  - High transconductance.

General speaking, PDSOI technology with body contact is widely employed to

overcome the V_{TH} variation which is usually caused by FDSOI technology. T-gate DTMOS (dynamic threshold MOS), shown in Fig. 5.1(b), is one kinds of applications in PDSOI technology. By varying the voltage which is employed on the extra body contact, the V_{TH} can be controlled effectively. But there are some problems in direct connection. First, the supply voltage across the extra body contact can not be more than 0.8V. The reason is that the parasitic diode between body and source will be turned on if above situation is happen. Second, it may be unstable under high frequency operation. This is because that the charges in body can not be released quickly enough from the reverse-biased diode.

In addition, one idea that the auxiliary SOI device is connected to the extra body contact is proposed in some applications. The further comparisons of delay time, rising time, falling time, supply voltage and sub-threshold current are concerned. Finally, all above discussions will be widely used and carefully analyzed in the following sections.



5.2 Level Shifter with Body Bias

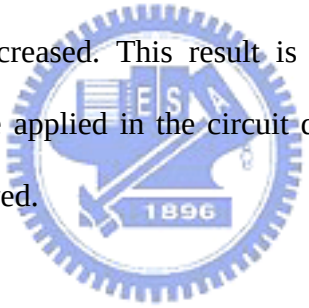
5.2.1 TFT Device with Body Bias

According to the understanding of SOI technology with body contact, LTPS TFT device are similar to SOI devices, no matter their structures, characteristics, or operations. Based on this reason, the formula about threshold voltage of N-TFT can be approximated in below:

$$\mathbf{V_{TH} = V_{TH0} + \gamma[(2\phi_F + V_{SB})^{1/2} - (2\phi_F)]} \quad (5\text{-}1)$$

Where V_{SB} is body to source voltage, V_{TH} is threshold voltage, V_{TH0} is the threshold

voltage for V_{SB}=0V, γ and ϕ_F are fabrication-process parameters. Based on this formula, it can see that if the body voltage is enhanced, the voltage of V_{SB} will be lowered, and then the voltage of V_{TH} will be lowered too. In order to prove this result, the N-TFT device in TOPPOLY 6-μm LTPS process with body contact was proposed. Fig. 5.2 shows the layout of body contact and Fig. 5.3 shows the photo die of N-TFT device with body bias. The width and length of this N-TFT device is 18-μm and 6-μm respectively. The IV curve measurement with different body bias was shown in Fig. 5.4. The voltage of V_{DS} is fixed in 10 V, the V_{GS} is varied from -2 V to 4 V, and the body bias is applied from 0 V to 1 V with the step of 0.1 V. Based on this IV curve, the current of I_D in triode region will be enhanced significantly when the body bias is enlarged. According to constant current method, it can find that as body bias is decrease the V_{TH} will be decreased. This result is clearly shown in Fig. 5.5. In summary, if this result can be applied in the circuit design, then there will be large power consumption can be saved.



5.2.2 Level Shifter Using Body Bias Technique

As what is showed in Fig. 5.6, level shifters are the major circuit blocks for the scanning driver and the data driver in LCD panel [21]. Therefore, level shifter should be urgently realized in LTPS. However, there are two problems to realize it. First, the voltage level of the logic input is getting lower and lower with the decrease of the scale in CMOS technology; then it may not apply level shifters in LTPS technology. Second, owing to the poor driving ability of LTPS, the level shifters may not transit quickly when the pixels of a panel are increasing. Therefore, if the threshold voltage can be lowered during the transition period of level shifters, above problems can certainly be solved. According above descriptions, a level shifter with body-bias

technique is proposed. The circuit can achieve high-efficiency by employing a simple but elegant N-TFT device to change the voltage level of body bias on level shifter. Furthermore, it will not consume extra power after signal transition and is very suitable to the application of LCD panel with integrated driver circuit in LTPS technology.

The mechanism of active body bias can lower the threshold voltage in the active mode, when input signals are transiting. In addition, the threshold voltage can be recovered in the static mode, when the input signals remain unchanged. The conventional level shifter (LS_C) and the other two modified level shifter (LS_G and LS_G) with body bias are shown in Fig. 5.7(a), Fig. 5.7 (b), and Fig. 5.7(c). Where, LS_G means that the gate of auxiliary TFT device is connected to the signal input terminal. As the same, the LS_D means that the drain of auxiliary TFT device is connected to the signal input terminal.

In LS_G, the bodies of the main N-TFT (Mn1 and Mn2) are connected to the sources of the auxiliary N-TFT (Mn1* and Mn2*). The size of auxiliary N-TFT is designed to be as small as possible in order to reduce the input capacitance of the level shifter. Initially, when Vin1 is staying at “High” and Vin2 is staying at “Low”, Mn1* is weakly on and Mn2* is off. Therefore, the body potential of Mn1 is “Low” and Mn2 is floating. On the other hand, when Vin1 falls from “High” to “Low” and Vin2 rises from “Low” to “High”, both Mn1* and Mn2* are turned on in the meanwhile. Then, the body potential of Mn1 and Mn2 will be charged up. Owing to the body bias, the threshold voltage of Mn1 and Mn2 will be lowered. Then the drain current of that will be enhanced. Also, the time for pull down transition can be decreased because of charge injection from Mn1* (Mn2*) and drain to body coupling effect of Mn1 (Mn2). After the signal transition, the Mn1* and Mn2* will be turned

off and the threshold voltage of Mn1 and Mn2 will be recovered. In this way, no static power will consume as the transition is finished. Similarly, the Mn2* is weakly on and Mn1* is off, when Vin1 is staying at “Low” and Vin2 is staying at “High”. Thus, the body potential of Mn1 becomes floating and Mn2 is “Low”. If the Vin1 rises from “Low” to “High” and Vin2 falls from “High” to “Low”, the body potential of Mn1 and Mn2 will be increased. That is due to the charge injection from Mn1* (Mn2*) and the drain to body capacitive coupling of Mn1 (Mn2). Therefore, the rising time of level shifter can be significantly reduced. Of course, the threshold voltage of Mn1 and Mn2 will be recovered after signal transition. Besides, LS_D can also reduce both rising and falling time without consuming extra static power in the same method.

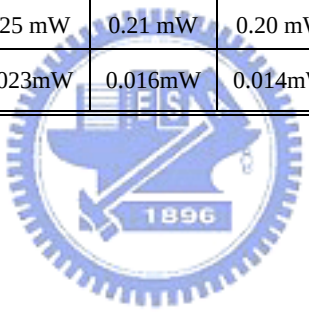
Because the TFT device in LTPS technology does not have SPICE model for body contact, this thesis employs TSMC 0.35-μm CMOS HV model to simulate and prove the function. The simulation results of LS_C, LS_G and LS_D are shown in Table VIII. The frequency of input signal is operated in 50 kHz for XGA resolution. According this table, it can see that if level shifter with body bias, the allowed input signal swing can be decreased. In addition, LS_D can accept lower input signal swing than LS_G. In summary, it can say that level shifter with body bias will more suitable for advanced applications. Besides, the rising time, falling time and delay time are all compared in this simulation. As shown in Fig. 5.8 and Fig. 5.9, it can find that LS_D and LS_G are better than LS_C; especially when input signal swing is lower. Also, LS_D is better than LS_G. When discussed delay time between LS_C, LS_G, and LS_D, it also has the same results. LS_D is best of the all, and LS_G is better than LS_C. All these comparisons are shown in Fig. 5.10. Finally, the comparison of power consumption is shown in Fig. 5.11. From the comparison, it can find that level shifter with body bias will not consume extra power than conventional level shifter. This is because that, power is only consumed when signal is during transition. As a

result, if delay time can be reduced, the power consumption can be down. This is why LS_D and LS_G are better than LS_C, and LS_D is better than LS_G. Fig. 5.12 is the layout of LS_C, LS_G, and LS_D in TOPPOLY 6-μm LTPS process. They will all implement in the same panel to compare and verify above simulations and comparisons.

Table VIII

The simulation results of LS_C, LS_G and LS_D.

	ΔV	**1.1V**	**1.2V**	**1.3V**	**1.4V**	**1.5V**	**1.6V**	**1.7V**
LS_C	**Tr**				1550 ns	190 ns	62 ns	31 ns
	Tf				440 ns	150 ns	67 ns	42 ns
	Td				2750 ns	350 ns	130 ns	77 ns
	P				0.42 mW	0.24 mW	0.20 mW	0.19 mW
LS_G	**Tr**		2060 ns	140 ns	45 ns	25 ns	22 ns	22 ns
	Tf		500 ns	100 ns	54 ns	39 ns	33 ns	30 ns
	Td		2840 ns	240 ns	100 ns	68 ns	58 ns	52 ns
	P		0.40 mW	0.23 mW	0.20 mW	0.19 mW	0.19 mW	0.19 mW
LS_D	**Tr**	930 ns	170 ns	59 ns	34 ns	26 ns	24 ns	23 ns
	Tf	650 ns	160 ns	76 ns	49 ns	39 ns	35 ns	33 ns
	Td	1560 ns	300 ns	120 ns	81 ns	65 ns	56 ns	51 ns
	P	0.37 mW	0.25 mW	0.21 mW	0.20 mW	0.19 mW	0.19 mW	0.19 mW
	P_{Extra}	0.043mW	0.023mW	0.016mW	0.014mW	0.014mW	0.014mW	0.014mW



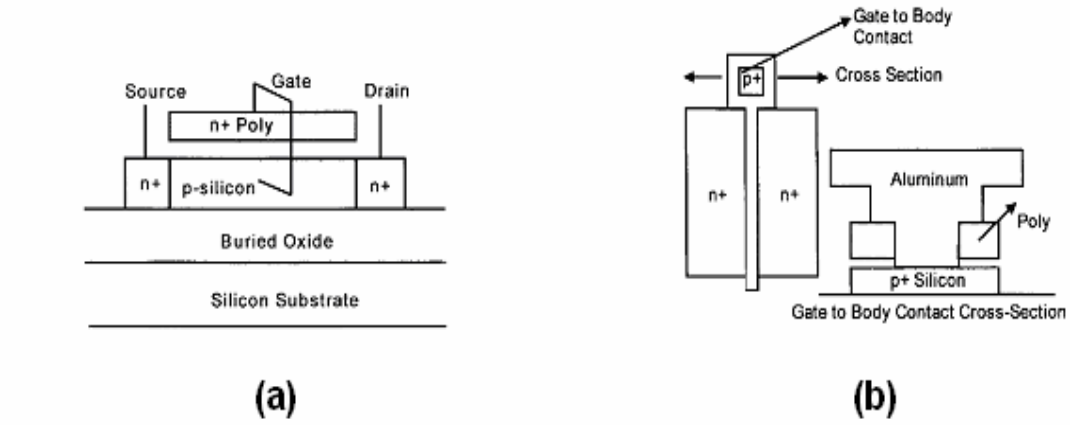


Fig. 5.1(a) is the cross section of SOI NMOS device and (b) is the T-gate DTMOS (dynamic threshold MOS).

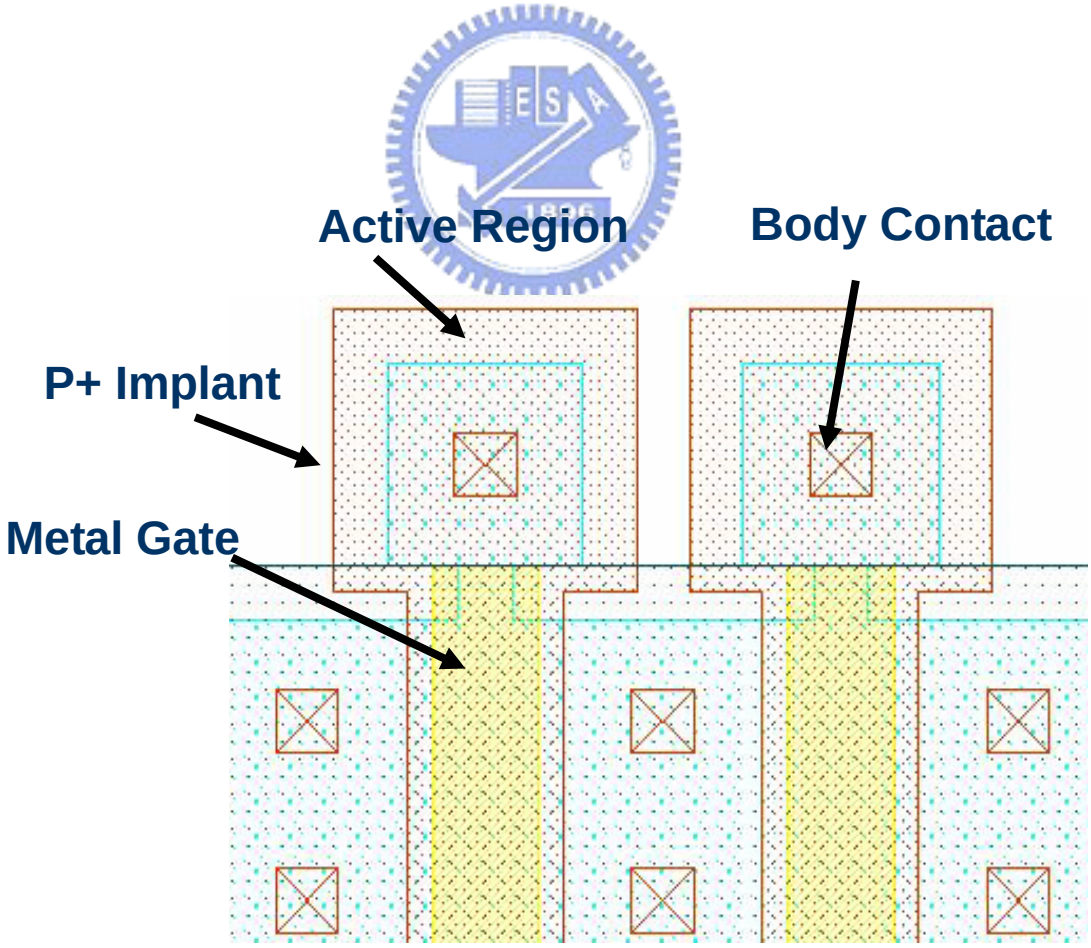


Fig. 5.2 Layout technique of body contact.

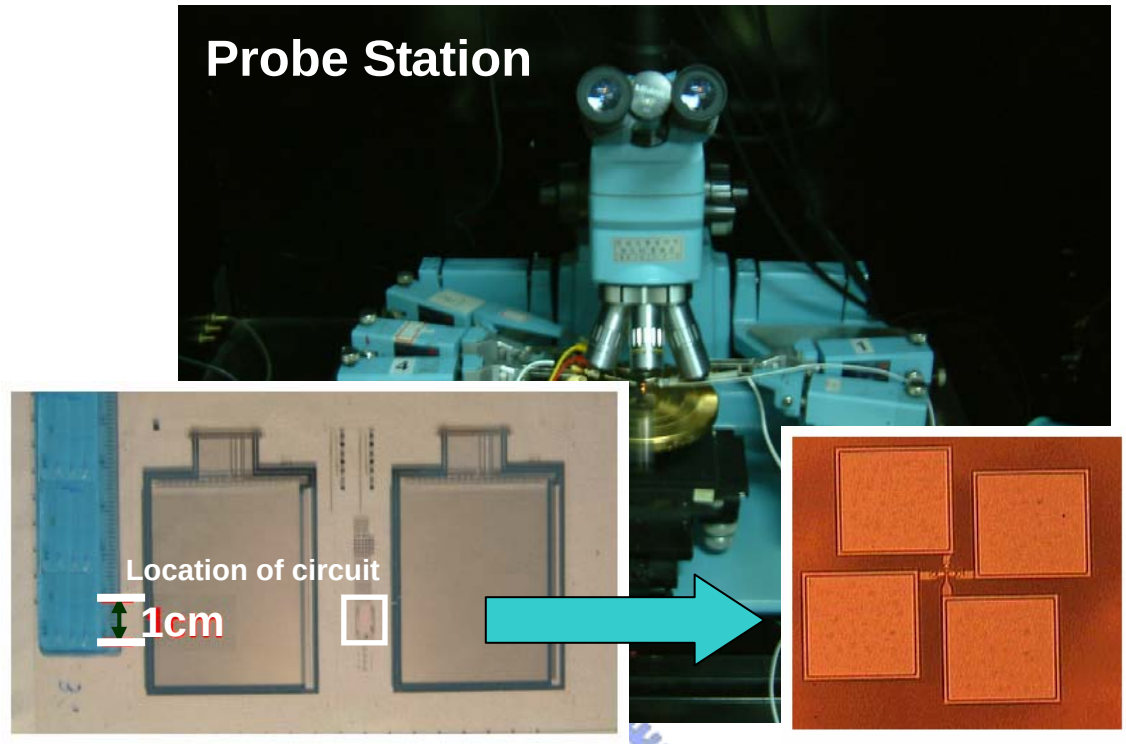


Fig. 5.3 The whole layout of N-TFT device with body bias.

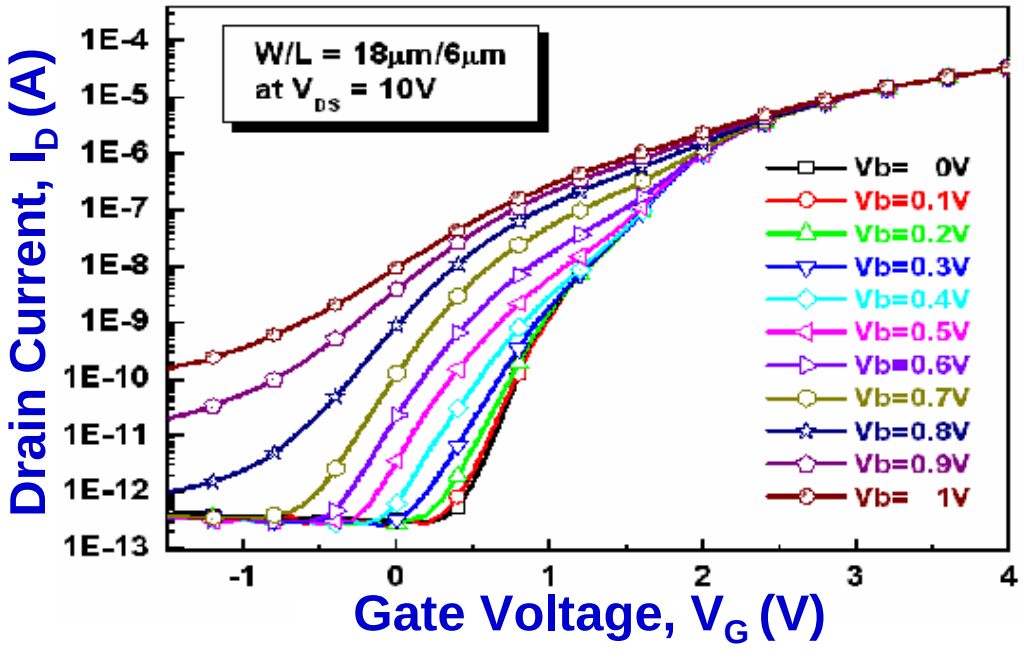


Fig. 5.4 The IV curve with different body bias.

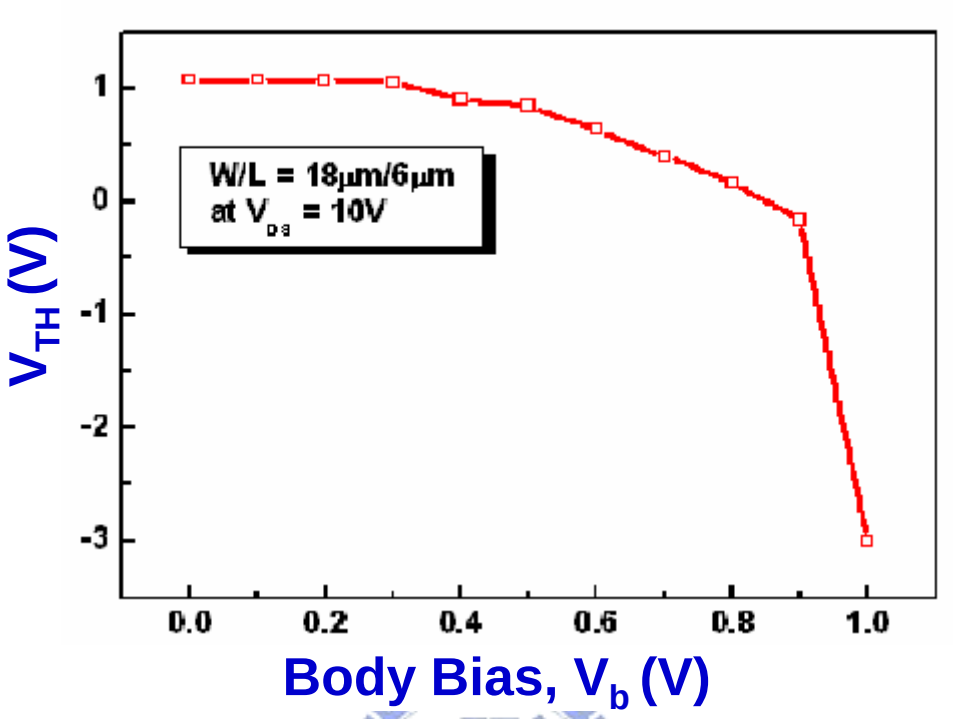


Fig. 5.5 The relationship between threshold voltage and body bias.

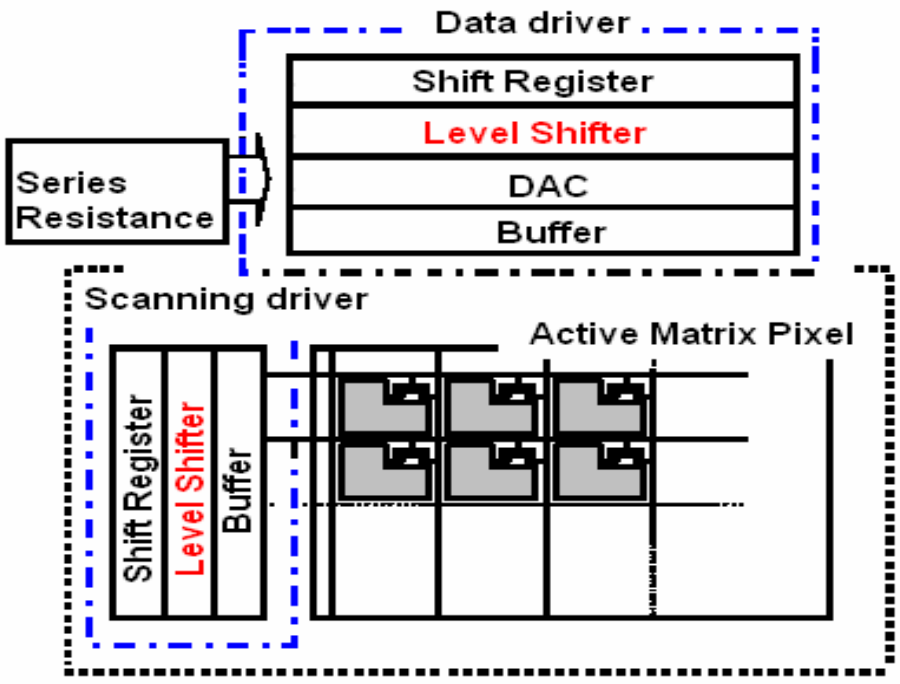
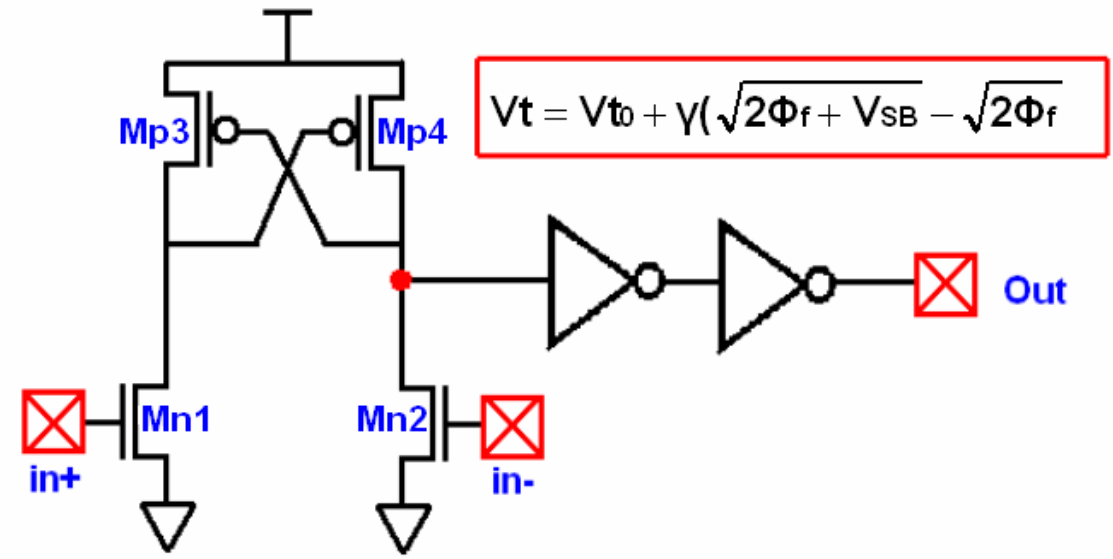
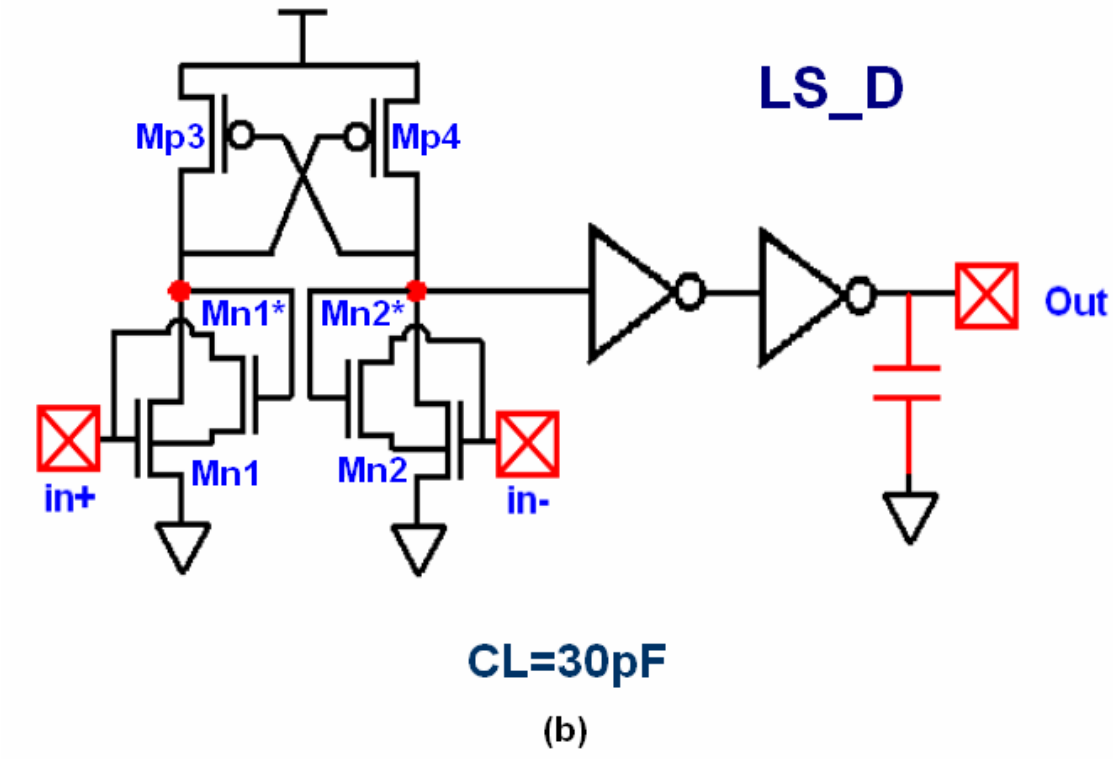


Fig. 5.6 The structure of driver circuit for LCD panel.


Vt = Vt0 + γ(√2Φf + VSB − √2Φf
Mp3
Mp4
Out
Mn1
Mn2
in+
in-

(a)


LS_D
Mp3
Mp4
Mn1*
Mn2*
Out
Mn1
Mn2
in+
in-
CL=30pF

(b)

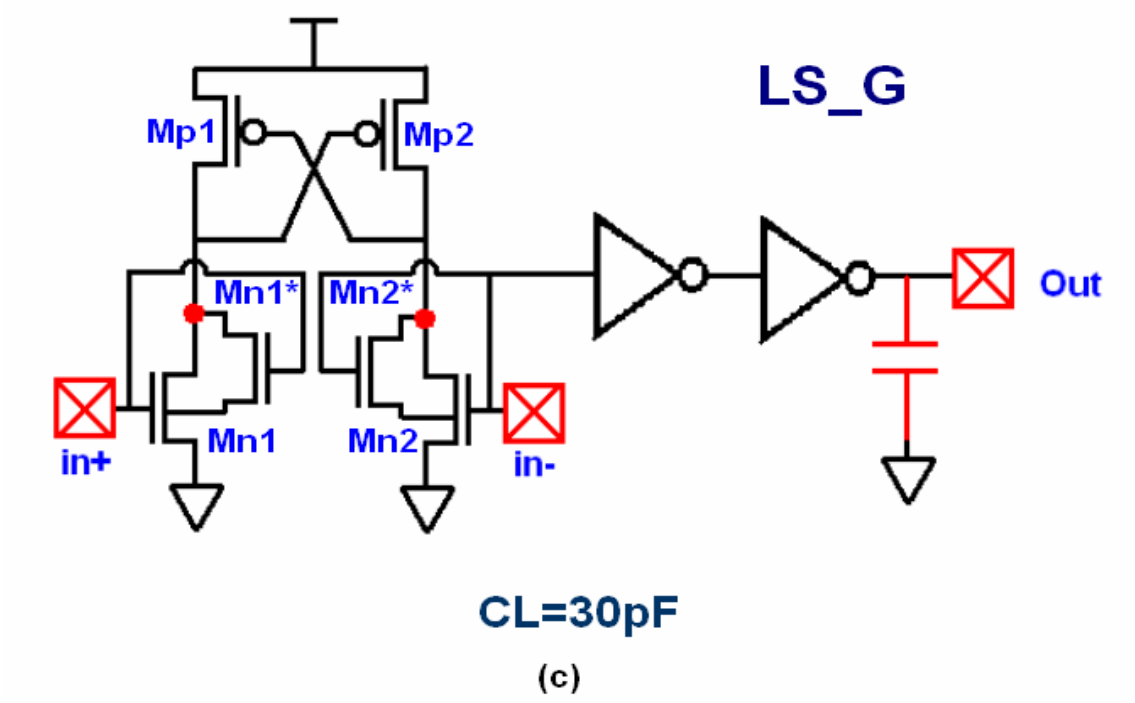


Fig. 5.7(a) is conventional level shifter (LS_C); (b) and (c) are two modified level shifter LC_D and LS_G, respectively.

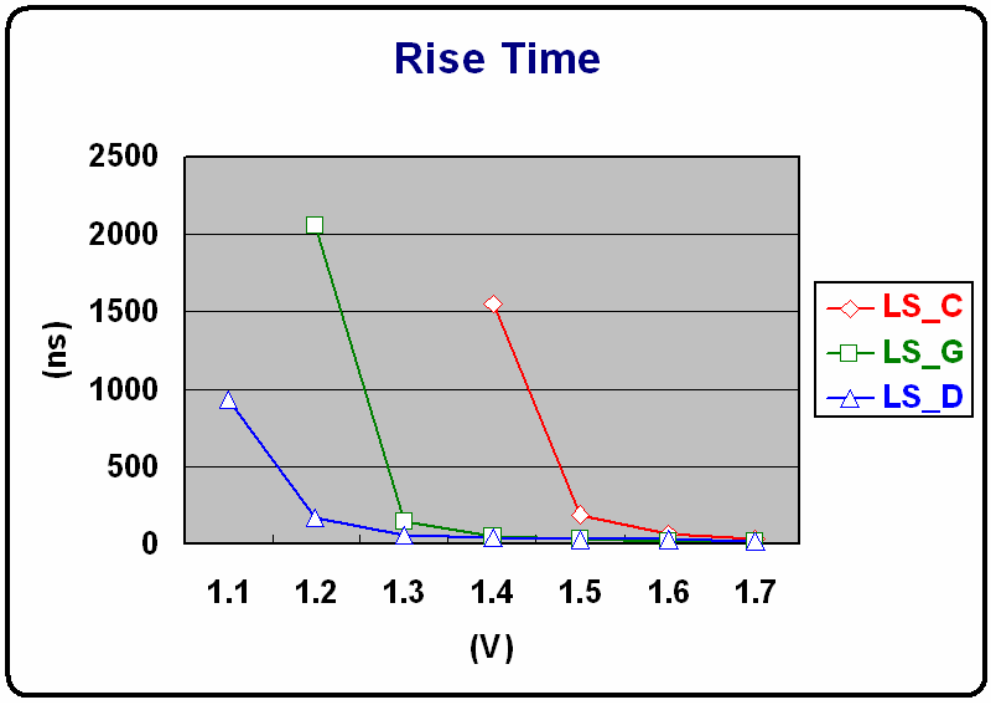


Fig. 5.8 The comparisons of rise time.

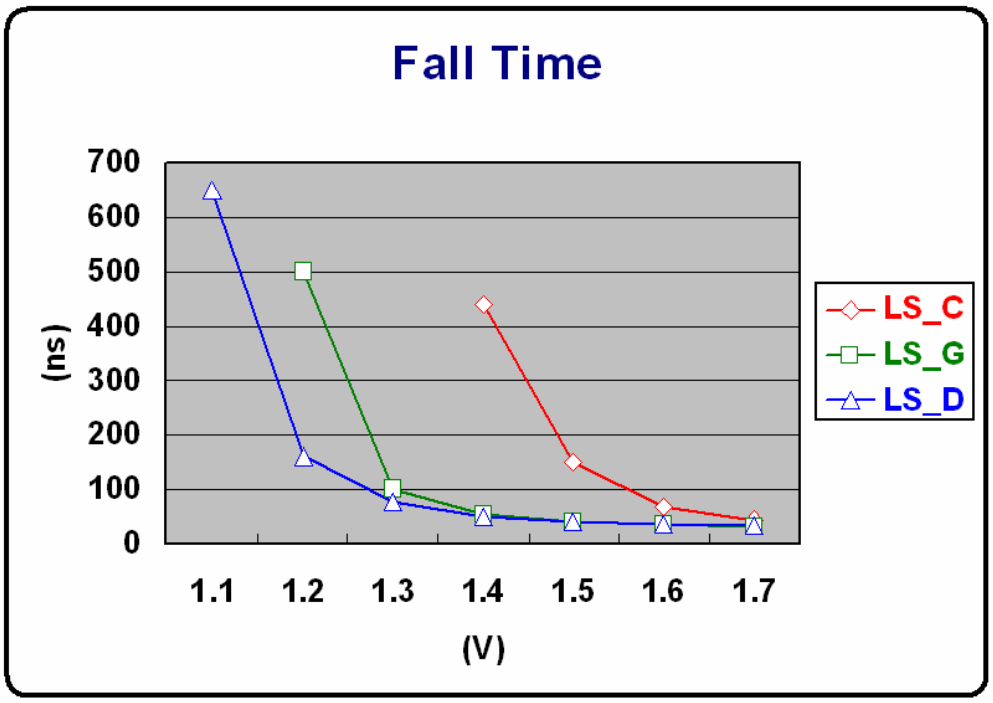


Fig. 5.9 The comparisons of fall time.

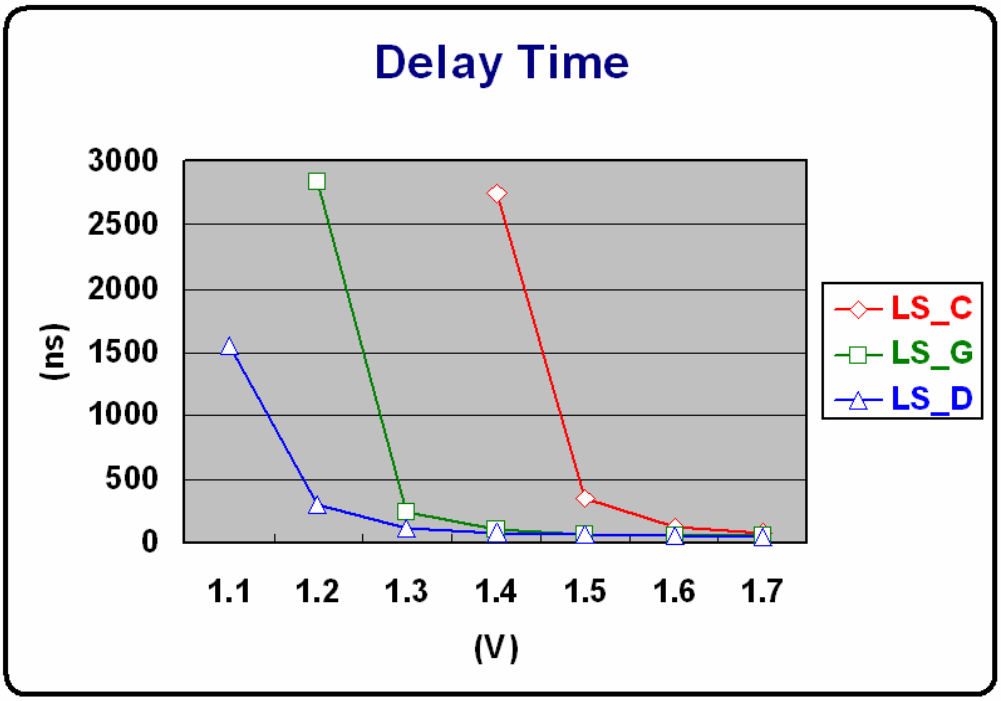


Fig. 5.10 The comparisons of delay time.

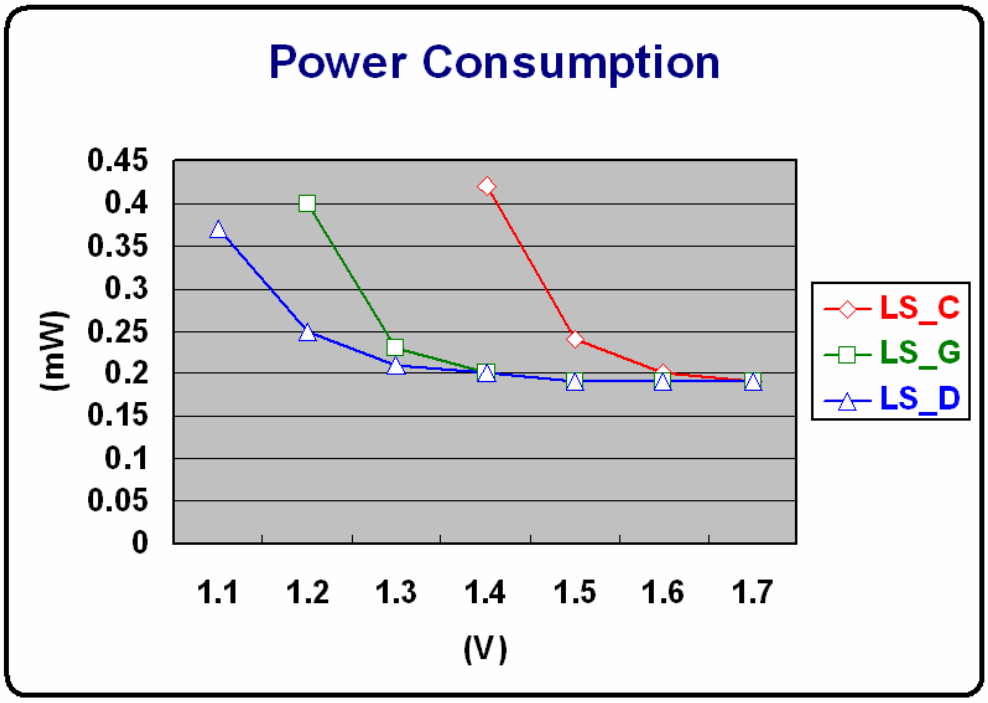


Fig. 5.11 The comparisons of power consumption.

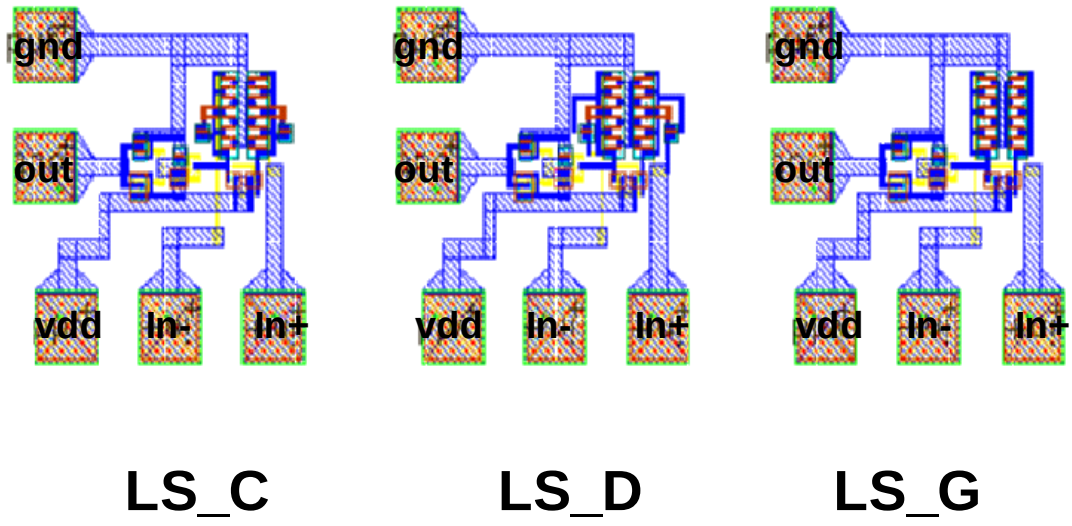


Fig. 5.12 Layout of LS_C, LS_G, and LS_D.

CHAPTER 6

DESIGN DRIVER CIRCUIT FOR RSDS RECEIVER

6.1 The Specification of RSDS Receiver

Generally speaking, TCON (timing controller) is a key element in LCD panel [22]. It is essentially the brain, the control center, and the heart of a LCD panel. In the current generation and past years, TCON has been implemented through the use of fully custom ASIC (application-specific integrated circuit) devices. The custom ASIC can rarely be reused in other LCD panel design. Along with TCON, discrete LVDS (low voltage differential signaling) devices are also required for interface and control of the LCD module. A new family of highly programmable and highly integrated TCON has now been developed which can be used on multiple LCD panel designs. They can support non-standard resolutions and different LCD panel configurations from various LCD manufacturers. This TCON offers higher level of integration resulting in smaller PCB (printed circuit board) outlines and lower power consumption. This higher level of integration has been achieved by integrating an on-chip LVDS receiver. In addition to the higher levels of integration, a new high speed low voltage differential interface between the TCON and data driver has also been developed. This new development, RSDS (reduced swing differential signaling) offers higher data transfer rates, enabling higher display resolutions at lower EMI (electric magnetic interference). Besides, Table IX is the specification of RSDS which

is proposed by National Semiconductor Corp. Fig. 6.1 is the system diagram of the LCD panel.

6.2 Driver Circuit for RSDS Receiver

6.2.1 Design Concept of RSDS Receiver

RSDS is a signaling standard, which defines the output characteristics of transmitter and input characteristics of receiver, for protocol of TCON and data driver on the panel. Besides, RSDS bus has many advantages in data transition. These advantages are described in below:

- Reduced bus width – suits in thinner data driver board.
- Low power dissipation – extends system run time.
- Low EMI generation – eliminates EMI disturbance.
- High noise rejection – maintains signal image.
- High throughput – enables high resolution LCD panel.

RSDS interface with a nominal signal swing of 200mV is usually used in VGA (video graphic array) and UXGA (ultra extended graphic array). Using RSDS architecture to realize a high bandwidth and robust digital interface between the host and the panel is better than using LVDS architecture. Table X shows the LVDS specification. The differences between RSDS receiver and LVDS receiver include the output voltage swing, output drive current, and data duplexer. The RSDS receiver for VGA and UXGA applications will be realized with the LTPS process progress, although its data-transition speed is not fast today (shown in Table XI). However, the designed tricks and experiences can be learned through the design flow of input buffer for RSDS receiver. In this thesis, an input buffer for RSDS receiver is designed in TOPPOLY 6-μm LTPS process.

6.2.2 Architecture of RSDS Receiver

As shown in Fig. 6.2 and Fig. 6.3, they are two popular structures in RSDS receiver. First type is taken the paper structure as reference [23]. Second type is the take the product of Samsung Corp as reference. They both sense the low swing signal in input terminal and pull the signal to full swing in the output terminal. Owing to the parasitical capacitor in the pad of output terminal, an inverter chain is always needed to drive the heavy loading. The parasitical capacitor is estimated to be 20 pF whose value includes output pad and oscilloscope. The simulation waveform of first type in TOPPOLY 6-μm LTPS process is shown in Fig. 6.4. As it can see, the output waveform can pull full high and full low when the swing of input signal is in 200 mV. Due to the poor mobility in TFT device, the maximum operational speed in this driver circuit can only reach to 40 MHz. Fig. 6.5 is the whole layout diagram of this driver circuit and inverter chain in TOPPOLY 6-μm LTPS technology. Besides, Fig. 6.6 is the simulation waveform of the second type driver which is also simulated in TOPPOLY 6-μm LTPS process. The output signal also has full swing when the dynamic range of input signal is in 200 mV. In addition, the maximum operational speed is also 40 MHz. Fig. 6.7 is the layout diagram of this driver circuit and inverter chain in TOPPOLY 6-μm LTPS technology.

Table IX

The specification of RSDS which is proposed by NS Corp.

	RSDS
Output voltage Swing	±200 mV
Termination	100 Ω
Output Drive Current	2 mA
Data Mux	2:1
Content	RGB data
Application	Intra-system interface

Table X

The specification of LVDS which is proposed by NS Corp.

	RSDS
Output voltage Swing	±350 mV
Termination	100 Ω
Output Drive Current	3.5 mA
Data Mux	7:1
Content	RGB data and control signal
Application	System-system interface

Table XI

Operational frequency of receiver in different resolutions.

Resolution	**CLK Freq.**
VGA(640×480)	25 MHz
SVGA(800×600)	40 MHz
XGA(1024×768)	65 MHz
SXGA(1280×1024)	112 MHz
UXGA(1600×1200)	165 MHz

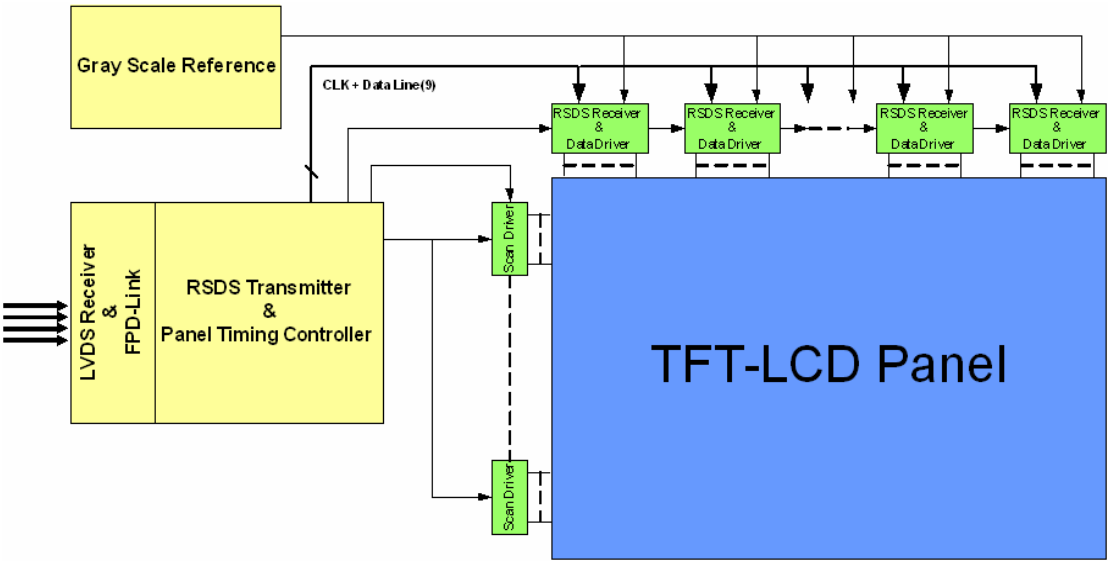


Fig. 6.1 System diagram of the LCD panel.

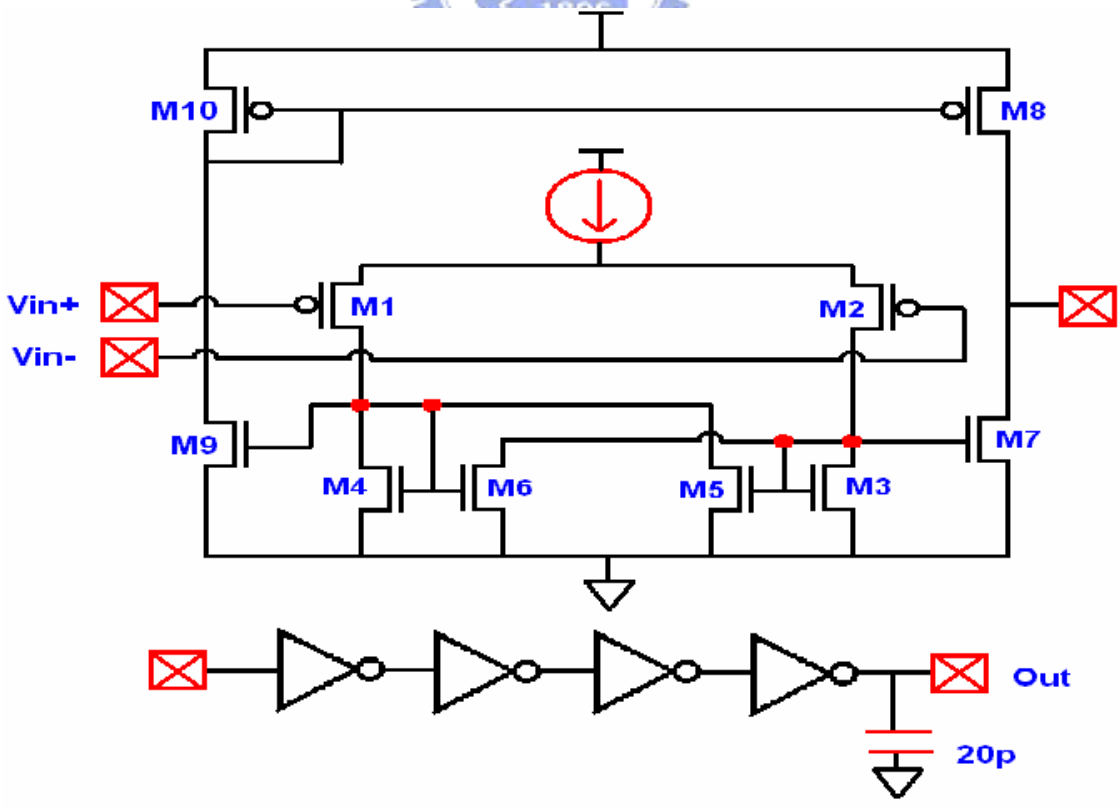


Fig. 6.2 The first type driver circuit for RSDS receiver.

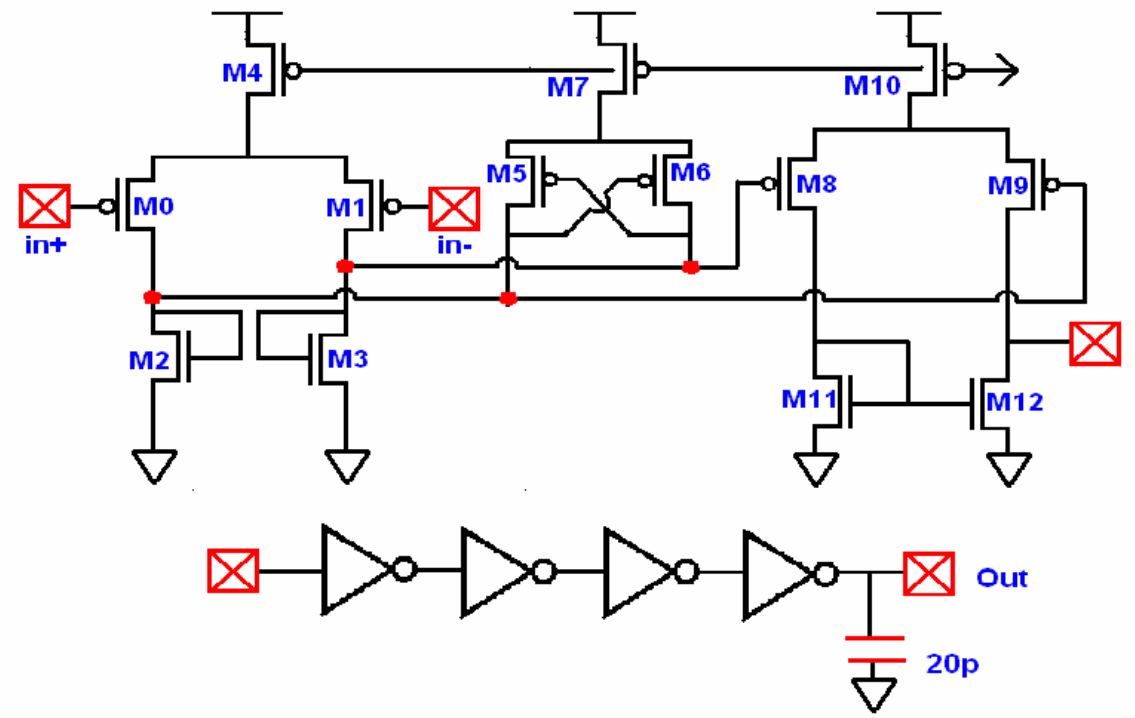


Fig. 6.3 The second type driver circuit for RSDS receiver.

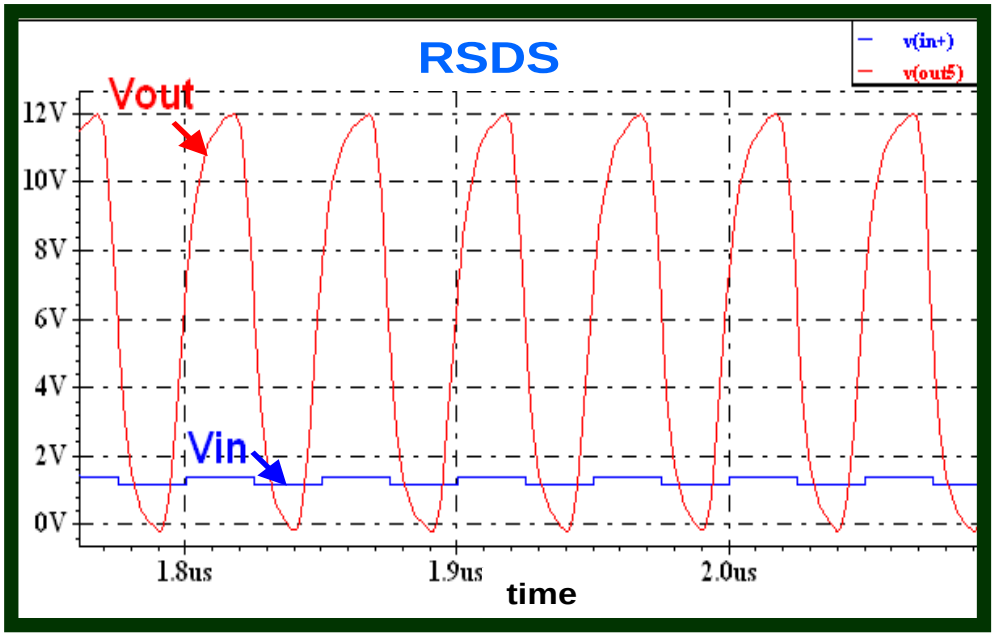


Fig. 6.4 Simulation result of the first type driver circuit for RSDS receiver.

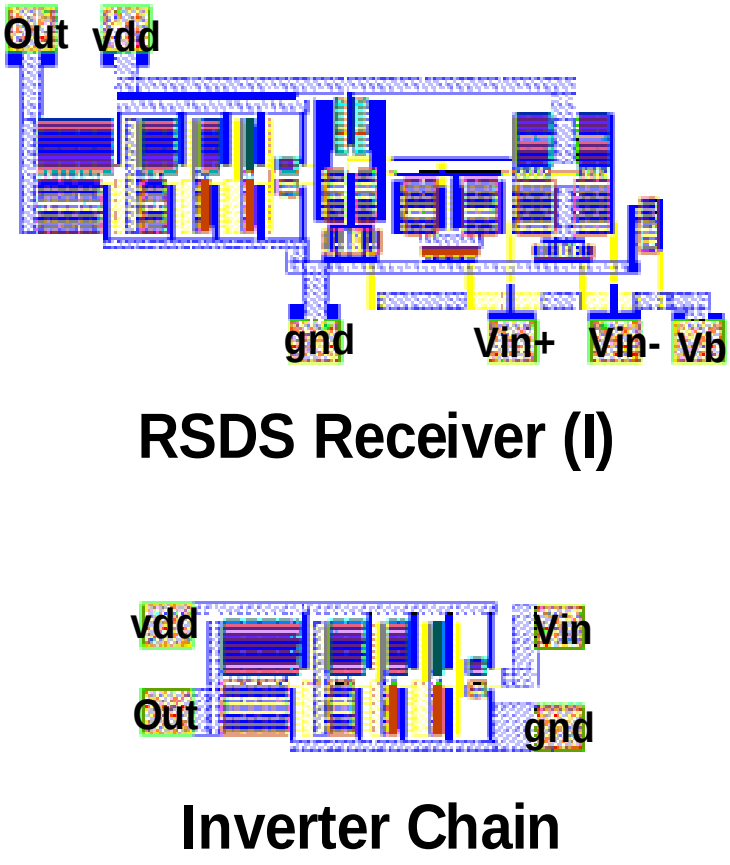


Fig. 6.5 Layout diagram of the first type driver circuit for RSDS receiver.

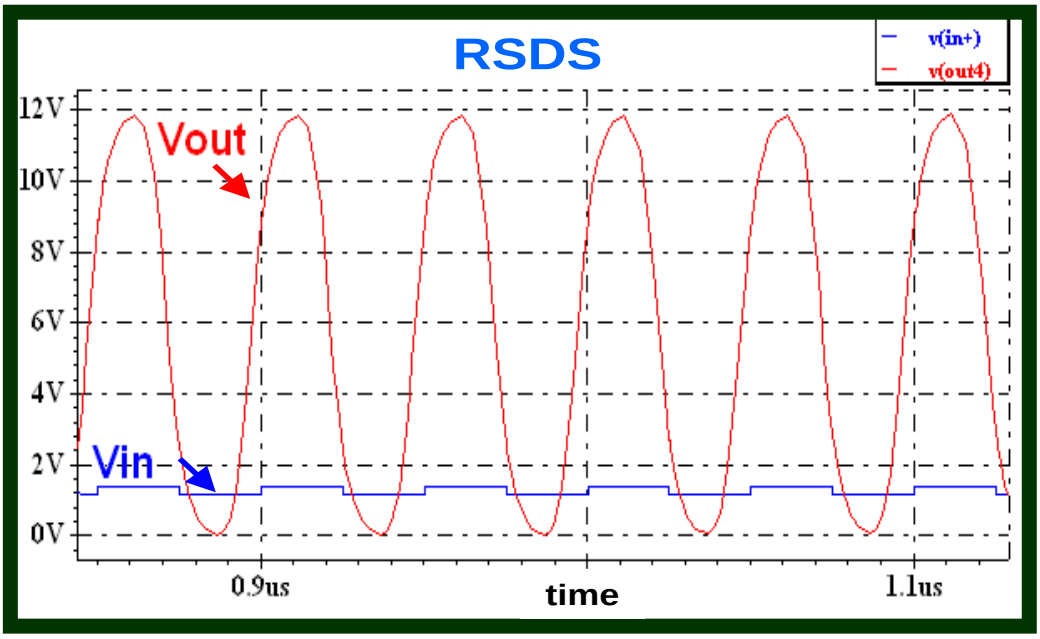


Fig. 6.6 Simulation result of the second type driver circuit for RSDS receiver.

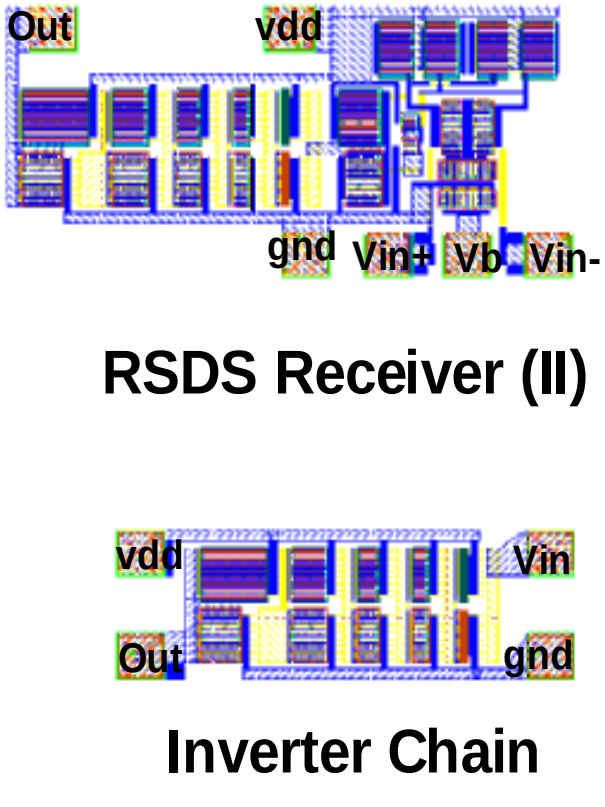


Fig. 6.7 Layout diagram of the second type driver circuit for RSDS receiver.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

7.1 Conclusions

In this thesis, two analog output buffers which can drive heavy loading are implemented in TOPPOLY 6-μm LTPS process. They are slew rate enhancement output buffer and low power class-B output buffer. The operational frequency of two output buffers can achieve 50 kHz to meet the specification for 1024 × 768 LCD panel. Moreover, a threshold voltage compensation circuit is realized to eliminate the variation of V_{TH} caused by characteristic variations of LTPS process. With the employment of this technique, the errors of gray level in output buffer can be all controlled below 1/2 LSB. Also, a more advanced analog output buffer with two-phase threshold voltage compensation is also proposed to increase its operational speed.

In the aspect of digital to analog converter, a digital to analog converter with gamma correction is designed to compensate the nonlinear effect in liquid crystal. Furthermore, the unexpected results caused by resistor string of DAC are discussed and analyzed here. In addition, level shifters using body-bias technique are also verified. In this method, the performance of operational speed and power consumption in level shifters are better than those of conventional one. All of above circuits are also implemented in TOPPOLY 6-μm LTPS process.

Finally, in order to meet the high resolution LCD, source driver usually employs the specification for RSDS as the transition interface in the data receiver. Besides, the application of the specification for RSDS will increase the data transition speed and

reduce the electric magnetic interference (EMI) effect. So, two input buffers for RSDS receiver application are proposed in this thesis. The transition speed of the proposed input buffers can reach to 40 MHz in TOPPOLY 6-μm LTPS process.

7.2 Future Works

In order to integrated driver circuit in LCD panel, the area of analog buffer and the drift of threshold voltage should be minimized as small as possible. Some elegant analog output buffers whose driver capabilities are poorer than operational amplifiers can also be adopted and designed in small-sized panel [24]-[25]. In addition, the auto-zeroing method which has been discussed can also be employed here to reduce the drift of threshold voltage.

DAC with gamma correction can reach to a more accurate level with the employment of the hybrid structure which is mentioned in the above chapter. Moreover, for designed more accurate DAC with gamma correction, the capacitors can do more advanced analysis and discussion after obtaining a lot of statistics in vary sizes of capacitor samples [26].

Finally, even though the mobility of LTPS is not fast enough to integrate the receiver in LCD panel, the tendency toward SOP (system on panel) is inevitable. Therefore, the designed tricks and experiences can be learned through the design flow of input buffer for RSDS receiver. Also, the more complex structure of RSDS receiver will be tried in advanced research.

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