Chapter 1

Introduction

1.1 Overview of xDSL Systems

Technology of digital subscriber line (DSL) systems have been greatly pursued and designed to carry the high data rate over telephone lines. Instead of using fiber all the way to customers' residence, DSL technology provides high-speed data transmission for Video-On-Demand (VOD), net-meeting, Ethernet in the first mile (EFM) or else. Many DSL systems such as high-bit-rate digital subscriber line (HDSL), Asymmetric digital subscriber line (ADSL) and Very-high-bit-rate digital subscriber line (VDSL), have been specified for the required transmission rate. The most up-to-date DSL technology, VDSL, is an extension of ADSL to higher rates, up to 52 Mb/s. Under such high bit rate, the loops must be short that optical fiber will be used for all but the last few thousand feet.

1.2 Motivation

There are two possible transmission modulation schemes, namely, single-carrier modulation (SCM) and multi-carrier modulation (MCM), adopted by xDSL systems. Recently, MCM has received a great deal of attention. Discrete multi-tone (DMT) and orthogonal frequency division multiplexing (OFDM) are two popular MCM schemes for wired and wireless communications, respectively. Synchronization is a crucial task in any digital receivers, especially for a DMT or OFDM system which has much shorter frequency spacing between sub-carriers than that of an SCM system. Phase rotations and inter-carrier interference due to synchronization errors are especially harmful in a VDSL system, because significant sub-carrier ICI is introduced for the

relatively short DMT sub-carrier spacing. If a synchronized clock frequency is desired at receiver side, a straightforward solution is to adjust the sampling clock with a VCXO (Voltage-controlled crystal oscillator) in the continuous time domain. However, a VCXO usually has higher cost and higher noise jitter than a XO (Crystal oscillator). With a fixed XO, all-digital timing correction can be performed in time domain, frequency domain or both. Note that the cost of frequency-domain approach is very high for a VDSL system due to the large number of sub-carriers. In this work, we try to find an efficient clock synchronization scheme based on digital time-domain signal interpolation for a VDSL system.

1.3 Organization of This Thesis

This thesis is organized as follows. In chapter 2, we explain the basic concept of DMT and discuss the characteristics of wire-line transmission environment. In chapter 3, we introduce the physical layer and considerations of ANSI T1E1.4 VDSL standard. In chapter 4, we describe the effects of clock offset and various clock synchronization techniques. Among the clock synchronization schemes, we suggest a better one for VDSL system by judging their computation complexities and performances. In addition, many interpolator designs for timing correction are evaluated. In chapter 5, guidelines for interpolator design are described. Whole system simulations and comparisons are also given in this chapter. Finally is our conclusion.