Chapter 5

Simulations and Performance Comparisons

Each function block of the adopted synchronization structure has been simulated and verified with MATLAB. After that, the whole system performance is evaluated to see if the specification requirements are met. Section 5.1 shows the simulation environment for a VDSL system. Section 5.2 shows how to choose a suitable interpolator for timing correction, where magnitude distortion ratios (MDR) and phase mean square error (Phase MSE) are introduced. Section 5.3 shows the complexity comparisons among different interpolators. At last, achievable bit-rate for each interpolator design are listed in section 5.4.

5.1 Simulation Environment

The proposed transceiver architecture is shown in Figure 5.1. With 50ppm clock offset, a number of test loops and interpolators are simulated to see how the system performance varies under different circumstances. Details of simulation settings are listed in Table 5.1.

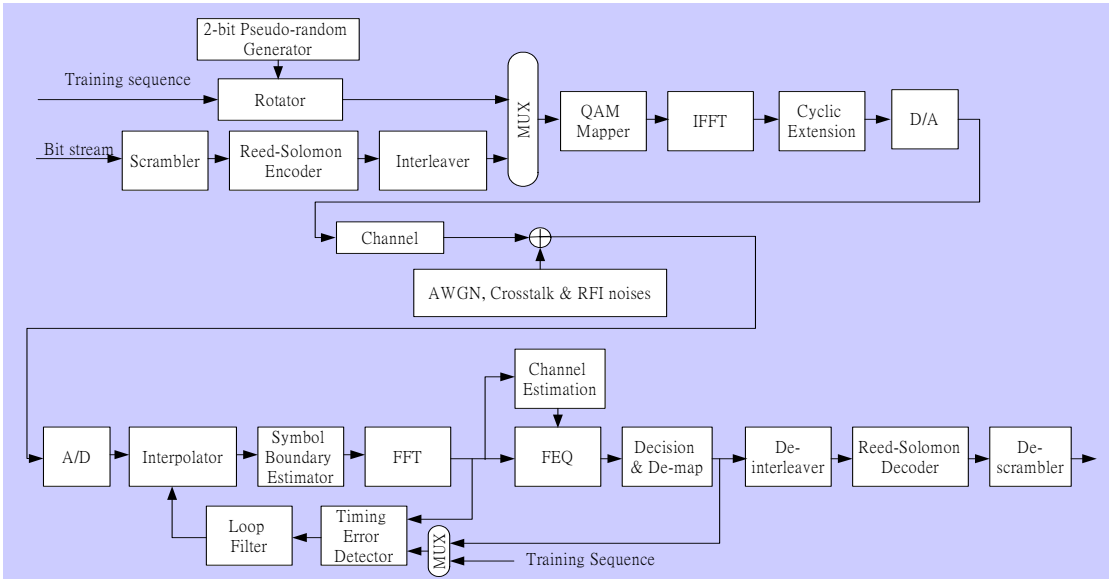


Figure 5.1 The VDSL transceiver architecture

Table 5.1 Parameters of the simulation environment

AWGN	80dB
Channel Model	VDSL#1 (1000ft/1500ft/4500ft) VDSL#5 (Short), VDSL#6 (Medium), VDSL#7 (Long)
Clock Offset	50ppm
Interpolator Type	Sinc with Rectangular window Sinc with Hamming window Sinc with Kaiser window Sinc with Chebyshev window General Least-squares Equiripple Cubic Lagrange Cubic B-spline
Interpolator length	4 taps
Coefficient-approximating polynomial order	3^{rd} -order

5.2 Mean Phase Square Errors and Magnitude Distortion Ratios

Since the non-ideal frequency response of the interpolator can be greatly compensate by a single-tap per-tone frequency-domain equalizer, the actual shape of an interpolator's frequency response is not so important. As described in section 4.2.5, the dispersion of magnitude responses and phase delay errors are due to the time-varying coefficients of an interpolator. The magnitude dispersion and phase delay error introduce additional noise to the system and hard to be compensated by the FEQ. Phase errors due to interpolator have dramatic impact on clock synchronization because they result in incorrect timing error estimation after FFT. Therefore, one should try to find an interpolator with the least phase errors, especially on pilot tones, and most coherent magnitude responses. Assuming a uniform distribution of the timing error over the interval [0,1], the mean-square-error of phase

delay per tone can be expressed as

$$\begin{aligned} \textit{Phase delay}\ \ MSE_k &= \frac{1}{4\pi^2}\int_0^1 (2\pi \mathrm{d} - 2\pi \tilde{\mathrm{d}}_k)^2\, p(d)d\mathrm{d} \\ &= \int_0^1 (\mathrm{d} - \tilde{\mathrm{d}}_k)^2\, d\mathrm{d} \end{aligned} \tag{5.1}$$

where k is the tone index, d is the desired fractional delay in sample, $\tilde{\mathrm{d}}_k$ is the resulting fractional delay of the k^{th} tone produced by the interpolator and $p(\mathrm{d})$ is the probability density function of d.

The dispersion of magnitude response can be measured by magnitude distortion ratios (MDR), which is represented by Eq. (5.2).

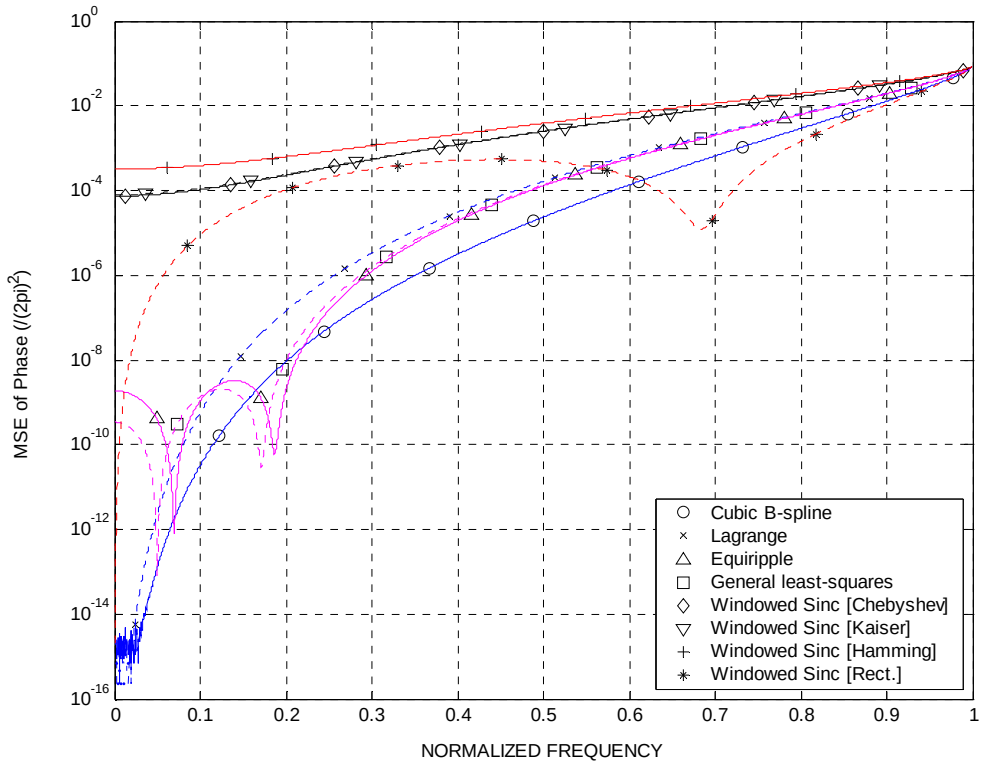
$$MDR_k = \frac{\overline{|H_k|^2}}{\overline{|H_k|^2} - \overline{|H_k|}^2} \tag{5.2}$$

where H_k is the frequency response of the interpolator at the k^{th} tone, $|H_k|$ is the magnitude response of the interpolator at the k^{th} tone, $\overline{|H_k|}$ is the mean value of magnitude response at the k^{th} tone and $\overline{|H_k|^2}$ is the square mean value of magnitude response at the k^{th} tone. $\overline{|H_k|}$ and $\overline{|H_k|^2}$ are defined as

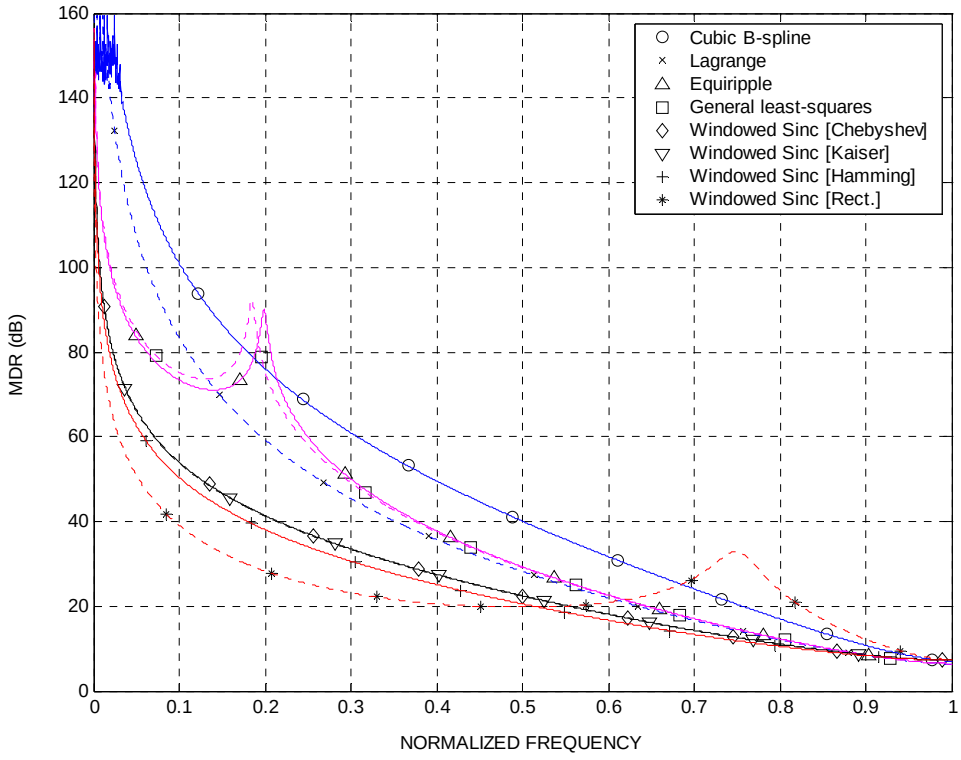
$$\overline{|H_k|} = E[|H_k|] = \int_0^1 |H_k|\, p(\mathrm{d})d\mathrm{d} \tag{5.3}$$

$$\overline{|H_k|^2} = E[|H_k|^2] = \int_0^1 |H_k|^2\, p(\mathrm{d})d\mathrm{d} \tag{5.4}$$

Figure 5.2 (a) (b) shows the MSE of phase delay per tone and the MDRs of the mentioned interpolators. Clearly, the cubic B-spline interpolator has the smallest phase error and most coherent magnitude response. Besides, windowed sinc interpolators are not suitable for VDSL system due to their poor phase responses.



(a)



(b)

Figure 5.2 (a) The MSE of phase delay and (b) the MDR of each 4-tap interpolator.

5.3 Computational Complexity

5.3.1 Polyphase Structure [29]

As described in Section 4.2.5, a polyphase interpolator is only suited for applications with fixed fractional delay steps. Since a VDSL system is very sensitive to small timing errors, the desired fractional delay for timing correction will be very small, which results in a large look-up table for a polyphase structure. Thus the polyphase structure is not feasible for a VDSL system.

5.3.2 Farrow Structure

An efficient implementation for continuously variable delay element was proposed by Farrow [28]. Recall from Eq. (4.26), the basic idea is to design a set of filters approximating a fractional delay in the desired range, $0 \le d \le 1$, and then to approximate each coefficient as a p^{th}-order polynomial of fractional delay.

$$h(n) = \sum_{m=0}^{p} c_{m,n} d^m, \quad n \in \{0, 1, 2, ..., (\mathrm{L}-1)\} \tag{4.26}$$

where $\boldsymbol{c_{m,n}}$ are real-valued coefficients of approximating polynomials. The transfer function of the filter becomes

$$\begin{aligned} H(z) &= \sum_{n=0}^{L-1} h(n) z^{-n} \\ &= \sum_{n=0}^{L-1} \left[\sum_{m=0}^{p} c_{m,n} d^m \right] z^{-n} = \sum_{m=0}^{p} \left[\sum_{n=0}^{L-1} c_{m,n} z^{-n} \right] d^m \\ &= \sum_{m=0}^{p} C_m(z) d^m \end{aligned} \tag{5.5}$$

This is the well-known Farrow structure, which is illustrated in Figure 5.3.

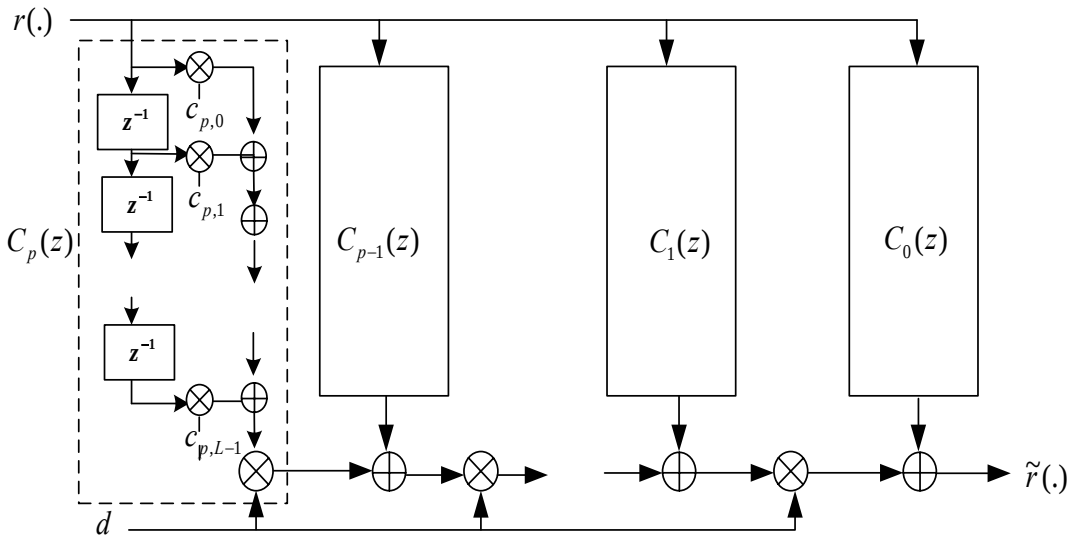


Figure 5.3 The Farrow structure of an interpolator

An interpolator with Farrow polynomial approximation coefficients is able to produce continuous delays. The delay accuracy is affected by the filter length L and the Farrow polynomial order p. After some trials, we found that it is sufficient for an interpolator with $L = 4$ and $p = 3$. Note that polynomial-based interpolator, such as Lagrange interpolation and B-spline interpolation, can be directly realized by the Farrow structure without further approximation.

Increasing filter length of an interpolator results in better phase and magnitude responses. However, the filter length of an interpolator cannot be arbitrarily long. Here are two reasons: First, the length of composite channel, including the transmission channel and the interpolator of the receiver, must be shorter than the guard interval to avoid ISI. Second, longer interpolator length means higher computational and hardware complexities. After some trials, we found that a 4-tap interpolator is sufficient. To further reduce the complexity, Farrow structure is applied to implement the interpolator. Table 5.2 shows the Farrow coefficients $c_{m,n}$ of approximating polynomials for each interpolator.

Table 5.2 Farrow coefficients Cm,n of 3rd-order approximating polynomials for several interpolators with L=4: (a) Cubic Lagrange; (b) Cubic B-spline; (c) General least-squares; (d) Equirriple approximation

(a)

$c_{m,n}$	$m=0$	$m=1$	$m=2$	$m=3$
$n=0$	0	-1/6	0	1/6
$n=1$	0	1	1/2	-1/2
$n=2$	1	-1/2	-1	1/2
$n=3$	0	-1/3	1/2	-1/6

(b)

$c_{m,n}$	$m=0$	$m=1$	$m=2$	$m=3$
$n=0$	0	0	0	1/6
$n=1$	1/6	1/2	1/2	-1/2
$n=2$	2/3	0	-1	1/2
$n=3$	1/6	-1/2	1/2	-1/6

(c)

$c_{m,n}$	$m=0$	$m=1$	$m=2$	$m=3$
$n=0$	0.00011558716467	-0.18244862414608	0.00836421136531	0.174113241888099
$n=1$	-0.00008438989326	1.00762432260056	0.51592150964278	-0.523637055893489
$n=2$	0.99982438645660	-0.46855617420566	-1.05498965803770	0.523637055893501
$n=3$	0.0001444162719	-0.3566195242487	0.5307039370295	-0.17411324188805

(d)

$c_{m,n}$	$m=0$	$m=1$	$m=2$	$m=3$
$n=0$	0.00009484461886	-0.17917953935513	0.00416257481495	0.17504875737509
$n=1$	-0.00006203384095	1.00378828812900	0.52181431419784	-0.525700016716772
$n=2$	0.99984055176787	-0.47031686637354	-1.05528573595328	0.52570001671675
$n=3$	0.00012663745422	-0.3542918824003	0.52930884694047	-0.17504875737506

Farrow coefficients of both cubic Lagrange interpolator and cubic B-spline interpolator are simple enough to be implemented with few multiplications and additions. Note that the scale-by-2 or scale-by-1/2 operation can be realized by binary shifts with wiring, while the scale-by-1/3 operation can be realized by simple shift-and-add operations. The corresponding architectures of cubic Lagrange and cubic B-spline interpolator are shown in Figure 5.4 and Figure 5.5. The computational complexities of these two interpolators are listed in Table 5.3

Table 5.3 Computational complexities per sample of cubic Lagrange and cubic B-spline interpolator

Interpolator type	+ /–	× constant	<< *or* >>	× *d*
Cubic Lagrange	11	2	4	3
Cubic B-spline	11	4	3	3
Equirriple / General LS.	15	16	0	3

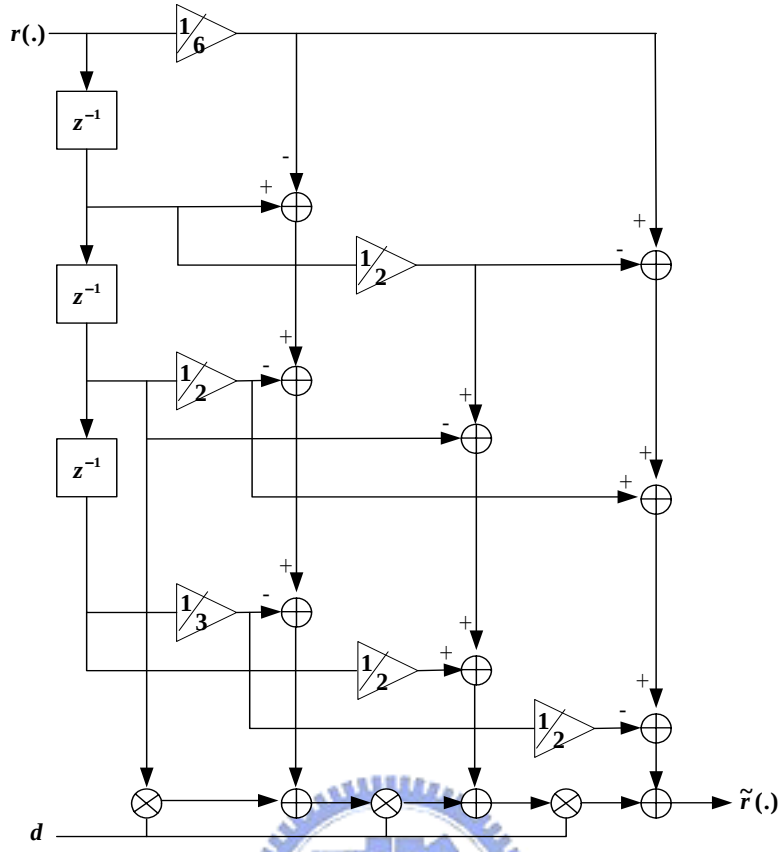


Figure 5.4 Farrow structure for cubic Lagrange interpolator

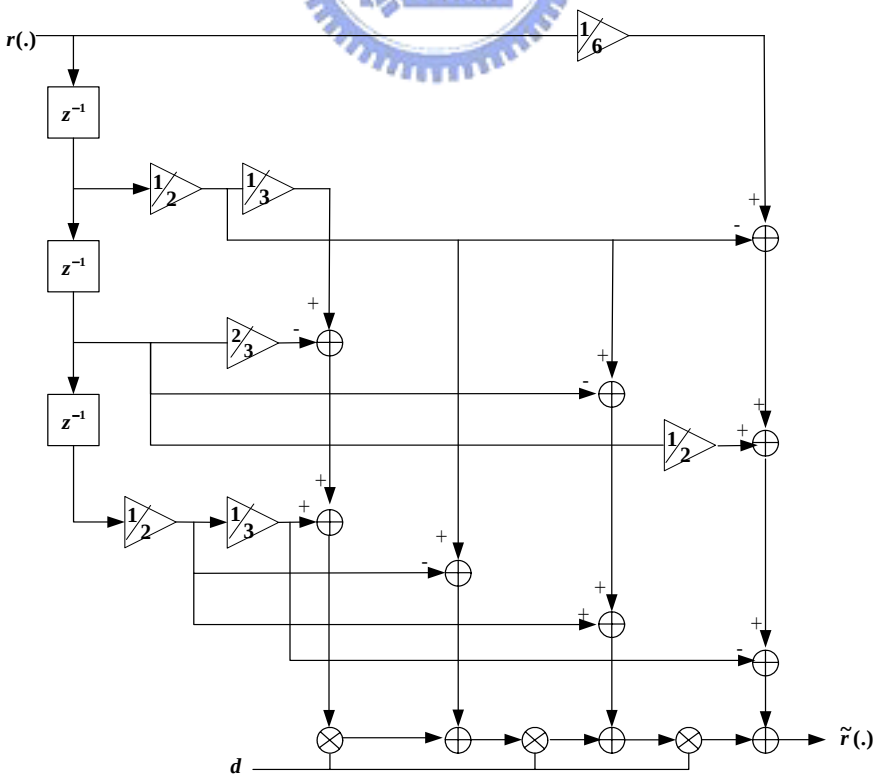


Figure 5.5 Farrow structure for cubic B-spline interpolator

5.4 Performance Evaluation of the Whole System

We evaluate the system performance by achievable bit-rates due to the discussed interpolators while the BER requirement is met. Under different channel conditions, the simulation results are listed in Table 5.4.

Table 5.4 Achievable bit-rates of various interpolators and channel conditions

Test Loop	Interpolator type	Bit-rate (Mbps)	BER
VDSL#1 (1000ft)	Cubic B-spline	56.3	$<10^{-7}$
	Cubic Lagrange	55.1	$<10^{-7}$
	Equirripple	52.2	$<10^{-7}$
	General least-squares	52.0	$<10^{-7}$
VDSL#1 (1500ft)	Cubic B-spline	42.9	$<10^{-7}$
	Cubic Lagrange	40.1	$<10^{-7}$
	Equirripple	41.4	$<10^{-7}$
	General least-squares	41.1	$<10^{-7}$
VDSL#1 (4500ft)	Cubic B-spline	15.2	$<10^{-7}$
	Cubic Lagrange	15.4	$<10^{-7}$
	Equirripple	15.4	$<10^{-7}$
	General least-squares	15.5	$<10^{-7}$
VDSL#5 (Short)	Cubic B-spline	49.9	$<10^{-7}$
	Cubic Lagrange	49.9	$<10^{-7}$
	Equirripple	49.3	$<10^{-7}$
	General least-squares	48.9	$<10^{-7}$
	Cubic B-spline	23.7	$<10^{-7}$

VDSL#6 (Medium)	Cubic Lagrange	23.8	$<10^{-7}$
	Equirripple	23.1	$<10^{-7}$
	General least-squares	23.9	$<10^{-7}$
VDSL#7 (Long)	Cubic B-spline	10.7	$<10^{-7}$
	Cubic Lagrange	10.6	$<10^{-7}$
	Equirripple	10.8	$<10^{-7}$
	General least-squares	10.7	$<10^{-7}$

As shown in Table 5.4, 4-tap interpolators, which are designed by cubic B-spline interpolation, Lagrange interpolation, equirripple approximation and general least-squares approximation, all provide reasonable bit-rates for a VDSL system in all the channel conditions we simulated. Considering the computational complexities of these Farrow-structured interpolators, polynomial-based interpolators are superior to others. For short and high-SNR-channel loops, the cubic B-spline interpolator achieves a higher bit-rate than the Lagrange interpolator with a slight higher computational complexity.

5.5 Fixed-point Simulations

To reduce the hardware complexity, the goal of fixed-point simulations is to decide the word length of each node in the receiver with as least performance degradation as possible. Finite-precision computation in the receiver causes a decrease in data rate. In this work, we assume that a decline of less than 1 Mbps in data rate is tolerable for fixed-point simulations. The precisions are decided by the following procedures: First, decide the precision of ADC output while the following stages still perform floating-point operations. Second, decide the precision of Loop filter output.

Its precision directly affects the accuracies of re-sampling process and output of the timing error detector. Then, the word length of interpolator output should be decided next. Following the received signal flow, the other nodes' precisions are decided in a similar way. If the simulation result is poor, i.e. the resulting data rate is too low, then set a higher word length for the node and repeat the simulation once again. The resulting word length of each node is shown in Table 5.5 and Figure 5.6.

Table 5.5 Word length of each node in the receiver

Node Name	Word Length (bit)
ADC Output	12
Loop Filter Output	12
Timing Error Detector Output	14
Interpolator Output	16
FFT Output	20
FEQ Output	20

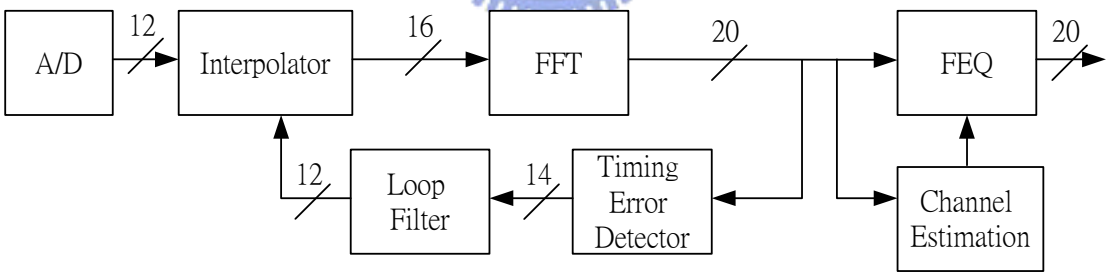


Figure 5.6 Simulated fixed-point receiver architecture

Alternatively, Table 5.6 shows the achievable bit rates of the mentioned interpolators, while the BER requirement is met. Since running fixed-point simulations for each channel condition is very time-consuming and the results among different test loops should have similar trend, we simply shows the system performance with fixed-point simulations under the test loop, VDSL#1 (1500ft).

Table 5.6 Achievable bit-rates of various interpolators

Test Loop	Interpolator type	Bit-rate (Mbps)	BER
VDSL#1 (1500ft)	Cubic B-spline	43.1	$<10^{-7}$
	Cubic Lagrange	40.1	$<10^{-7}$
	Equirripple	40.6	$<10^{-7}$
	General least-squares	41.2	$<10^{-7}$