# Chapter 6

# Conclusion

This work proposes a synchronization procedure for ANSI T1E1.4 VDSL system, and also addresses the design of an interpolator for timing error correction. Quantitative measures of the filter performance are given by MDRs and MSE of phase responses. Comparisons among different interpolators based on fixed filter length, MDRs, phase MSEs and computational complexity are done. Cubic B-spline interpolator is found to be superior over other interpolators. By combining Farrow structure techniques, the computational complexity of cubic B-spline interpolator includes 11 additions, 4 scale-by-constant operations, 3 binary shift operations and 3 real multiplications per sample. It has slightly higher computational complexity but achieves higher bit-rate than cubic Lagrange interpolator. With the cubic B-spline interpolator for timing correction, 56.3Mbps bit-rate is achieved while the BER is less than $10^{-7}$ under VDSL test loop #1. The future work will be deriving a cost function for least phase delay error and most coherent magnitude response, a more efficient implementation for cubic B-spline interpolator and hardware implementation for the VDSL system.