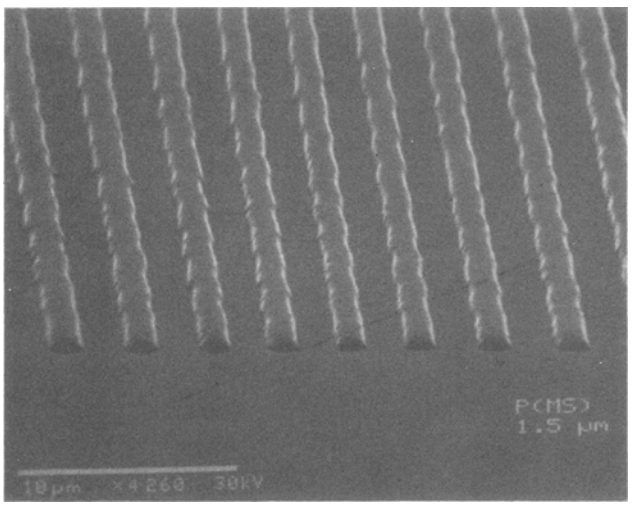

Fig. 1. A scanning electron micrograph of 1.5 μm line and space pattern.

cially photosensitive toward photoinduced cross-linking by onium salts is poly(N-vinylcarbazole). Similarly, poly(vinylanthracene), poly(vinylperylene), poly(vinylphenanthrene), and poly(vinylpyrene) would likewise be expected to undergo facile electron transfer reactions in the presence of onium salt photoinitiators leading to cross-linking.

Poly(4-chlorostyrene) and poly(4-bromostyrene) are examples of halogen containing polymers which are cross-linked on irradiation in the presence of photosensitive onium salts.

In contrast to those polymers described above which undergo electron transfer induced cross-linking, polymers such as polystyrene, poly(α-methylstyrene), and poly(4-nitrostyrene) which either are not activated toward electron transfer or possess deactivating electron substituents such as the nitro group are not useful as negative photoresists. Similarly, poly(1- and 2-vinylnaphthalene) are not cross-linked under the same conditions presumably because their reduction potentials are not sufficiently low enough to permit them to easily undergo the required electron abstraction from the naphthalene rings.

A more detailed photoimaging study was carried out with poly(4-methoxystyrene) and the specifics of the procedure are described in the experimental portion of this paper. To briefly summarize, the above mentioned polymer together with the onium salt, di(4-t-butylphenyl)-iodonium hexafluoroantimonate, were spin coated onto silicone wafers. After bake drying the wafers, they were subjected to imagewise exposure at 254 nm using a quartz mask and then baked for 30s at 130°C. Finally, the unexposed portions of the resist were removed preferentially by immersion in an equal volume mixture of n-hexane and dichloromethane. In Fig. 1 is shown a scanning electron micrograph of 1.5 μm line and space patterns produced using the above described process. A slight bridging can be observed in the otherwise well-resolved patterns. The patterns show some loss of line profile; however, this is to be expected since the postbake temperature was considerably above the reported T_g at 89°C (7). Perhaps most striking is the apparent lack of solvent induced wavyness in the pattern, usually termed "snaking," although this can be observed under conditions of low dose and in the 1-1.5 μm features. The photoresist has an unexpectedly high photosensitivity since the pattern shown in Fig. 1 was made at an irradiation dose of only 30 mJ/cm^2.

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A Novel Process for High-Performance Schottky Barrier PMOS

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ABSTRACT

A novel process for high-performance rinsed asymmetric Schottky barrier PMOS transistors with a Schottky barrier junction source and a P-N junction drain is proposed. PtSi is used to form the source Schottky junction. No spacer oxide is necessary for this process to isolate the poly-Si gate and the source PtSi; thus the source PtSi may directly contact the inverted channel. Measured results show that the new Schottky barrier PMOS can circumvent the drawback of the conventional Schottky barrier PMOS, such as low drain driving current, poor transconductance, and high drain to substrate leakage current.

Using Schottky barrier contacts for the source and drain of a MOSFET may result in performance and fabrication advantages. With the reduction of device dimensions, it is necessary to achieve very shallow source and drain structure with junction depth less than 0.15 μm. Such a shallow structure can be easily obtained from n^+ layers where the relatively heavy mass of implanted dopants results in shallow projected ion ranges. For PMOS devices, unfortunately, this is not the case. However, an effective shallow junction can be achieved by using a Schottky contact, and no dopant lateral diffusion will occur. The high conductivity of the Schottky contact can also minimize the source series resistance which is an inherent problem of shallow junction (1). In addition, eliminating high-temperature annealing steps promotes the oxide quality and also leads to better control of geometry. Recently, it has also been shown that the employment of Schottky source/drain PMOS devices is an efficient method to reduce latch-up susceptibility in CMOS owing to the absence of minority carrier injection (2-4).

However, the Schottky barrier PMOS also suffers from some problems, such as poor transconductance and large subthreshold leakage current. Typically, the gate sidewall spacer oxide is used to prevent the source/drain-to-gate

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bridging effect. The potential barrier between the Schottky source and the inverted P-channel, due to spacer oxide, significantly degrades the transconductance (2, 5). The ultrashallow drain Schottky junction enhances the electric field at the junction edge which, combining with the characteristics of voltage-dependent reverse current of Schottky junction, makes the subthreshold leakage current of the Schottky barrier PMOS several orders of magnitude larger than that of the conventional PMOS.

To solve these problems, a p^- region is usually inserted between the channel and the Schottky S/D (3, 6, 7). The device performance is improved, but these methods employ rather unconventional processing which requires more critical process control. Furthermore, a tradeoff between the doping level of the p^- region (and thus the device performance) and the latch-up resistance is another factor to be considered (3).

In this work, we are interested in the performance of the Schottky barrier PMOS device while a novel process and thus a modified structure was employed to prevent the device's characteristics from degradation. The process and the final device structure are presented in the next section. Following this, key process is further examined and discussed. Finally, measured electrical characteristics are presented and followed by a conclusion.

Rinsed Asymmetric Schottky Barrier PMOS

Besides the incorporation of the implanted p^- region, it is possible to extend the S/D silicide to the gate edge to improve the device performance (2). The sheet resistance of the extended silicide is much lower than that of the implanted p^- region, and no tradeoff exists between the device performance and the latch-up resistance. Since the emitter of the PNP parasitic transistor is the source of the PMOS device in the CMOS latch-up path, only the Schottky junction source is needed for the purpose of latch-up prevention. In addition, since the subthreshold leakage current is due to the reverse-bias drain-to-substrate junction, preserving the drain as a conventional p^+ structure would make the leakage as low as that of the conventional PMOS (4). Therefore, an asymmetric Schottky barrier PMOS with a Schottky barrier junction source and a P-N junction drain was fabricated.

The starting material was (100)-oriented, 4-7 Ω-cm, phosphorus-doped silicon wafer. Following the RCA cleaning process, LOCOS technology was used to define the active region. This was followed by 500Å gate oxide growth and 5000Å LPCVD polysilicon deposition. The poly-Si was then doped by $POCl_3$ at 900°C for 25 min. The sheet resistance was about 14 Ω/□. After the poly-Si pattern delineation and S/D oxide etch, 500Å oxide was thermally grown on the source and drain regions (Fig. 1a). At this stage, the oxide on the poly-Si was about 2500Å. An additional photolithography process was employed to mask the source region, the alignment tolerance of which is half of the gate length (Fig. 1b). Alignment of this mask is not critical except for devices with submicron channel length. Drain oxide was etched and BF_2^+ was implanted into the drain region with a dose of 5×10^{15} ions/cm^2 at 30 keV, and activated and diffused at 1000°C for 30 min (Fig. 1c). The junction depth was 0.47 μm as measured by spreading resistance, and the sheet resistance was 94 Ω/□. The S/D and poly-Si oxide were etched and then a novel process was employed.

The wafer was then rinsed in DI water at 20°-23°C for 10 min. For the heavily doped poly-Si gate and drain, a thin native oxide layer grows on the surface with this rinse condition (Fig. 1d). The thickness of the thin oxide was about 25Å as estimated by ellipsometer measurement assuming refraction index 1.465. A Pt film of 300Å thickness was deposited in an E-beam evaporation system with a base pressure below 5×10^{-6} torr. A 550°C 30 min sinter in N_2 ambient followed. Pt on the source region interacted with Si to form PtSi Schottky junction while Pt on the poly-Si and drain region were actually isolated by the thin oxide grown during the DI water rinse; thus, no Pt silicide was formed. All the unreacted Pt was etched by diluted aqua regia (Fig. 1e). The sheet resistance of the source PtSi was about 11 Ω/□. Finally, Al metallization and patterning were performed and followed by a 400°C 20 min sintering. The cross-sectional view of the finished structure is shown in Fig. 1f. All devices reported in this work have a 25 μm channel width and a channel length of 9 μm as determined by SEM measurement on the poly-Si gate strip.

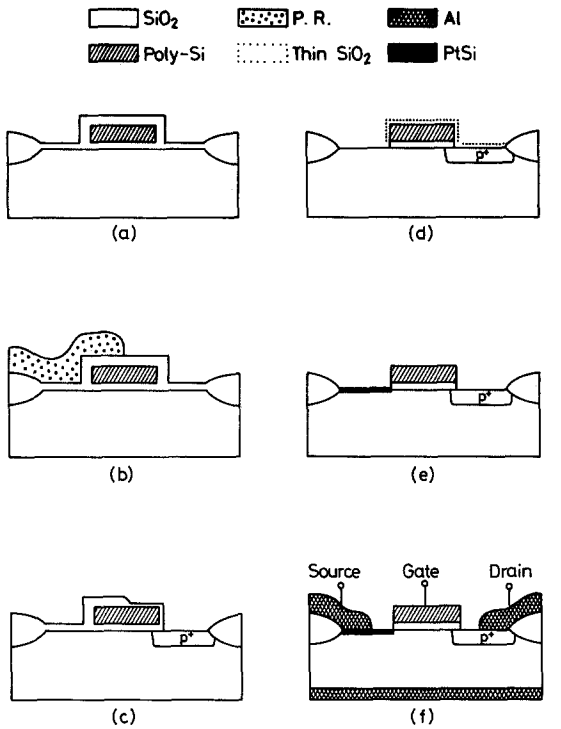

Fig. 1. (a-f) Cross-sectional view of the rinsed asymmetric Schottky barrier PMOS process sequence and the finished structure.

For comparison purposes, a conventional PMOS was also fabricated. The process was identical with that of the rinsed asymmetric Schottky barrier PMOS except that both source and drain were implanted and no Pt film was deposited.

Reliability of Key Process

The most critical step of the asymmetric Schottky barrier PMOS fabrication process presented above is the DI water rinsing step. The rinse time and water temperature of this step must be controlled so that the thin oxide grown on the surface of the heavily doped poly-Si is thick enough to prevent Pt from interacting with Si; otherwise, the source and/or drain region will bridge to the gate. On the other hand, however, the rinse time should not be too long and the water temperature too high; otherwise, the native oxide grown on the source region will degrade the characteristics of the Schottky junction. Thus, the rinse process must be examined in detail.

First, the effect of rinse time on the characteristics of the Pt Schottky junction formed after the rinse was considered. The starting material for this purpose was the same as that used in the previous section; the impurity concentration was about 1×10^{15} atoms/cm^3. Following the

Table I. Characteristics of PtSi Schottky junction prepared at various rinse times

Parameters \ Samples	DA 0 min rinse	DB 10 min rinse	DC 20 min rinse
Ideality factor	1.009	1.007	1.005
Barrier height (eV)	0.873	0.872	0.874
I_R (nA)[a] at −10V	2.40	1.69	1.82

[a]Junction area: 0.01 cm^2.

definition of active region by LOCOS, wafers were split into three groups — DA, DB, and DC — and were rinsed in DI water for 0, 10, and 20 min at 20°-23°C, respectively. A Pt film of 300Å thickness was deposited and then annealed in N_2 ambient at 550°C for 30 min to form PtSi Schottky junction. Table I shows the measured ideality factor, barrier height, and reverse-biased leakage current of the PtSi Schottky junction. It is found that the silicon surface can be exposed to DI water rinse at 20°-23°C for as long as 20 min without degrading the characteristics of the PtSi Schottky junction.

Second, the growth ability of the thin oxide on the heavily doped poly-Si surface during the DI water rinse was considered. A poly-Si gate MOS capacitor structure was fabricated with a process similar to that of the poly-Si gate process presented in the previous section. The wafer was then rinsed in DI water until the poly-Si surface was hydrophilic, while the substrate surface was still hydrophobic (about 10 min at 20°-23°C). A Pt film of 300Å thickness was deposited and annealed in N_2 at 550°C for 30 min. The sample was then analyzed by x-ray diffraction spectrum. The Pt on Si substrate had reacted with Si to form PtSi; however, only Pt signal was observed on the poly-Si region. The poly-Si region was bridged to the Si substrate region due to the sidewall Pt. After unreacted Pt was etched in dilute aqua regia, there was an open circuit between the poly-Si and the substrate. Thus, no bridge effect will occur using the rinsed process.

Based on these experiments, we may conclude that the rinsed process is reliable and works with less constraint; thus, no spacer oxide is necessary to prevent the device from the bridge effect.

Measured Electrical Characteristics

Measurement and comparison were made on the electrical characteristics of the conventional PMOS and the rinsed asymmetric PMOS devices. The consideration includes the current driving capability, transconductance, subthreshold leakage current, and the breakdown voltage.

The first drawback of the existing Schottky barrier PMOSs is their low drain current driving capability due to large series resistance at source and drain. Figure 2 shows the I_{ds}-V_{ds} curves of the conventional PMOS and the rinsed asymmetric Schottky barrier PMOS devices. The gate voltage was stepped from −2 to −7V with a −1V step. Comparing the characteristics, we observed that the current driving capability of the rinsed asymmetric Schottky barrier PMOS is slightly superior to that of the conventional PMOS. This is mainly because among other factors, such as deviation of the threshold voltage and the effective channel length between the two devices, the source sheet resistance of the rinsed asymmetric Schottky barrier PMOS (11 Ω/□) is smaller than that of the conventional PMOS (94 Ω/□).

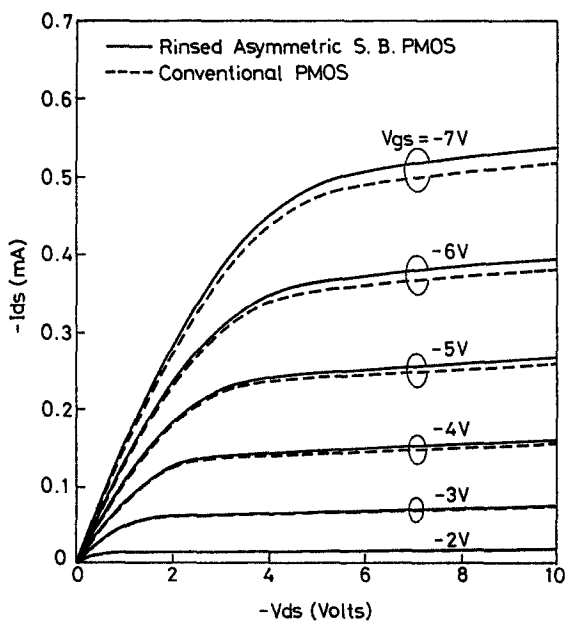

Fig. 2. Comparison of drain characteristics of the rinsed asymmetric Schottky barrier PMOS (solid line) and the conventional PMOS (dashed line) with W/L = 25 μm/9 μm. The gate voltage is stepped from −2 to −7V.

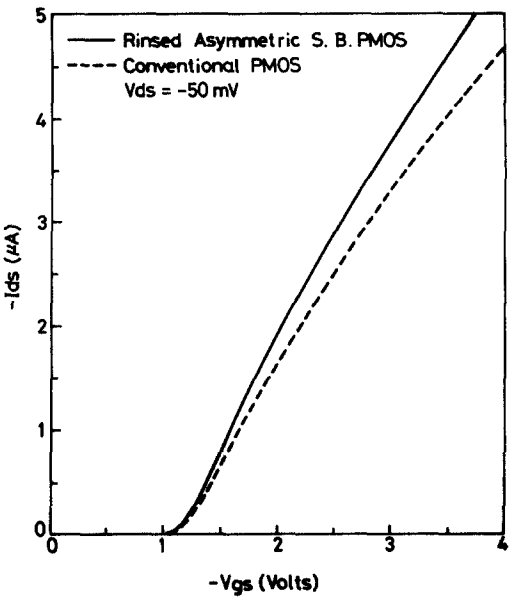

Fig. 3. Comparison of the drain current *vs.* gate voltage characteristics of the rinsed asymmetric Schottky barrier PMOS (solid line) and the conventional PMOS (dashed line) with W/L = 25 μm/9μm. The drain voltage is V_{ds} = −0.05V.

Figure 3 shows the I_{ds}-V_{gs} characteristics of the conventional PMOS and the rinsed asymmetric Schottky barrier PMOS measured at V_{ds} = −0.05V. The gate voltage was swept from 0 to −5V. It is seen that the rinsed asymmetric Schottky barrier PMOS fully recovers the transconductance. The slight difference in slope is mainly due to the difference in source sheet resistance once again.

Figure 4 shows the subthreshold behavior of the conventional PMOS and the rinsed asymmetric Schottky barrier PMOS. Measurements were performed with the drain biased at −0.05 and −5V, respectively, on devices which have a 50 × 25 μm size of source and drain regions. It is seen that the subthreshold behavior can be fully recovered by the rinsed asymmetric Schottky barrier PMOS because of the employment of the conventional drain structure.

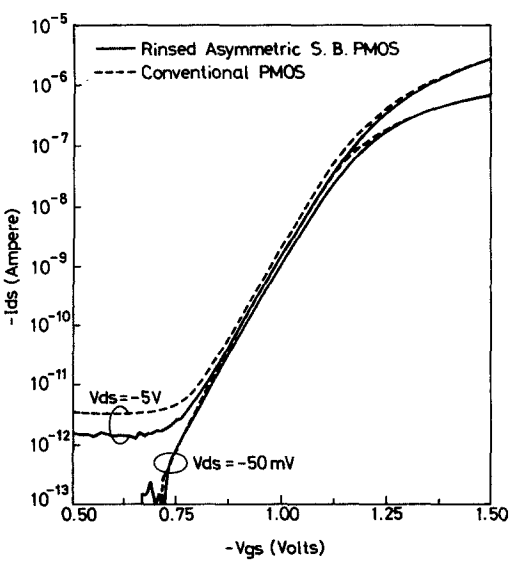

Fig. 4. Comparison of subthreshold characteristics of the rinsed asymmetric PMOS (solid line) and the conventional PMOS (dashed line) with W/L = 25 μm/9 μm. The drain is biased at −50 mv and −5V, respectively.

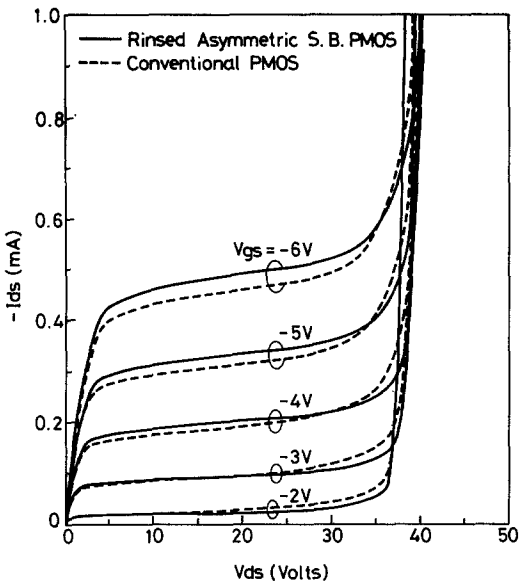

Fig. 5. Comparison of breakdown characteristics of the rinsed asymmetric PMOS (solid line) and the conventional PMOS (dashed line) with W/L = 25 μm/9 μm.

Comparison of the breakdown behavior is shown in Fig. 5. The breakdown voltage of the asymmetric Schottky barrier PMOS is comparable to that of the conventional PMOS. It is reasonable to expect that for the short channel devices, the breakdown voltage of the rinsed asymmetric Schottky barrier PMOS would be higher than that of the conventional PMOS due to longer effective channel length at the same mask channel length.

Conclusion

In this work, a novel process for a high-performance modified Schottky barrier PMOS device was developed. The process is very simple compared to that of the existing Schottky barrier PMOS and results in a Schottky source device without oxide sidewall spacer. The key step, DI water rinse step, was examined in detail and was shown to be reliable and works with less constraint. The asymmetric device structure with a P-N junction drain completely resolves the large subthreshold leakage problem associated with the symmetric Schottky barrier devices. Thus, the novel process makes the application of the Schottky barrier PMOS possible.

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LPCVD of Tin Oxide from Tetramethyltin and Oxygen

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ABSTRACT

A low-pressure chemical vapor deposition (LPCVD) process using tetramethyltin (TMT) and oxygen has been developed for preparing tin oxide films. Effects of temperature, pressure, and gas flow rates are systematically examined so that the wafer-to-wafer and within-wafer thickness uniformities of less than 5% are obtained in the hotwall LPCVD reactor. Twenty-three 75 mm or 100 mm wafers could be deposited during each run. Nominal deposition rate was 55 Å/min. Deposition rates as high as 120 Å/min was obtained at higher pressure and oxygen flow rates. Characterization results showed that the films were polycrystalline SnO_2 with a refractive index of between 2.00 to 2.10, a visible-light transmission of 84%, and resistivity of 0.6 Ω-cm.

Transparent electrode materials find applications in optoelectronics devices such as solar cells, electroluminescent displays, liquid crystal displays, and solid-state imagers. With increased process complexity for advanced optoelectronic devices, good chemical and thermal stability and mechanical hardness are critical parameters. For example, to directly replace polysilicon gates in a charge-coupled device (CCD), the transparent electrode must undergo ion implantation, high-temperature anneal, wafer clean-ups, photoresist strip, HF acid deglaze, SiO_2 dry etch, and metallization processes. Both polysilicon and tin oxide films meet these requirements, but quantum efficiency of the polysilicon-gated CCD is only 35% in the blue region, in contrast to 60% for tin oxide-gated CCDs (1). Various techniques have been employed to prepare SnO_2 films, such as spray hydrolysis, vacuum evaporation, reactive RF sputtering, chemical vapor deposition (CVD), and dc glow discharge (2-15). Among these various techniques, LPCVD is commonly used for thin film deposition in the fabrication of silicon devices due to its advantages of lower manufacturing cost (15). Thus it is highly desirable to develop a LPCVD process for SnO_2 that is compatible with present silicon manufacturing technology.

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Experimental Technique

Apparatus.—The deposition is done by direct oxidation of tetramethyltin (TMT) with oxygen in a commercial horizontal hotwall LPCVD system. A schematic of the system is shown in Fig. 1. TMT has a relatively low vapor pressure of 60 mtorr at 21°C. The mass flow controllers (MFC) and gas line were modified so that adequate flow of TMT vapor could be maintained without having to heat the TMT liquid source and gas lines. Instead, the TMT was chilled in