CHAPTER 2

THE OPERATIONAL PRINCIPLES OF NANODEVICE AND CMOS SENSING CHIP

2.1 THE OPTICAL AND ELECTRICAL PROPERTIES OF CdSe AND Au NANOPARTICLES

Recently, research interests in exploring various nanostructures with functional electrical and optical properties have been increasing significantly. Among many nanostructures, semiconductor nanoparticles (NPs), or nanocrystals, have shown their unique attraction due to the spectacular size-dependent properties when the size regime is below 10 nm [4] [6]. There are two major effects to explain these size variation properties in nanocrystals. First, the number of surface atoms is a large fraction of the total atoms of a single nanocrystal. The high surface-to-volume ration will make a contribution to variations in thermodynamic properties of nanocrystals, such as melting point, and solid-solid phase transition. Second, nanocrystals with the same interior bonding geometry as the corresponding bulk material but with only a few hundred to thousand atoms exhibit dramatic size-dependent optical and electrical properties [4]. These variations are because the density of states of electronic energy levels transforms as a function of the size of interior nanocrystal, known as **quantization effects** [4]. The diagrams of density of states in metal and semiconductor nanocrystals are shown in Fig. 2.1. This can be understood by considering that the bands of a solid are centered about atomic levels, with the width of the band related to the strength of nearest-neighbor interactions. As the size of solid increases, the center of a band develops first and the edges develop last. Therefore, in metal, the Fermi level lies in

the center of a band, so that the relevant energy level spacing is very small. At temperature above a few Kelvin, the electrical and optical properties of a metal solid react more closely like those of no energy level spacing, even as small as tens or hundreds of atoms. However, in semiconductor, the Fermi level lies between two bands, so that the edges of bands dominate the low-energy optical and electrical behavior. Besides, the HOMO-LUMO gap increases as the semiconductor nanocrystals become smaller (bellow 10 nm) [4].

In addition to the surface atoms and interior nanocrystal structure, the interfaces between nanocrystals and environment play an important role in virtually every property, from structural transformation to photoluminescence efficiency to solubility. Two entirely different types of interfaces are here presented: the inorganic/organic interface, typically appearing in nanocrystal colloid, and the inorganic/inorganic interface of solid nanocrystal that are embedded completely inside a host material. Colloidal nanocrystals have a solid/liquid interface, so that the colloid becomes soluble and not aggregate. In the case of CdSe NPs, the colloids are synthesized directly in a hot surfactant, n-trioctylphosphine oxide, TOPO. At the end of this preparation, the nanocrystals are capped by a monolayer of TOPO, which coordinates to Cd sites. The TOPO molecules are packed as densely on the nanocrystal surface as the curvature of the surface allow. However, the phosphine oxide-Cd interaction is relatively weak, and the TOPO can be displaced by dissolution in a coordinating solvent, such as pyridine. The pyridine interacts more weakly with the Cd site but can displace TOPO by mass action. Besides, the TOPO-coated CdSe NPs are unstable with respect to photooxidation. Upon exposure to visible light, the Se at the surface is oxidized to selenate. In turn, this oxide will evaporate from the surface, leaving reduced Cd and a freshly exposed layer of Se behind. The inorganic/inorganic interface appears by capping nanocrystals inside an inorganic shell, with organic molecules modifying only the outer shell. In the case of CdSe/ZnS (core/shell) NPs, the core (CdSe) is passivated in a shell (ZnS) of a wider energy bandgap, resulting in highly luminescent property. In this work, we used

4-(2-Aminoethyl)phenol (Tyramine)-modified (for aqueous operation) CdSe NPs of approximately 5 nm in diameter as photoreceptors to detect lamination with above band gap photoexcitation [4].

The **Bohr exciton radius** r_b is the spatial extent of the electron hole pair in material and is defined as $r_b = 4\pi\hbar^2\varepsilon / (m * e^2)$, where $\hbar$ is the Plank's constant, ε is the permittivity in bulk material, and m* is the effective mass. For CdSe semiconductor, the electron's effective mass is 0.13 m_e and the hole effective mass is 0.45 m_e. So the Bohr exciton radius of CdSe is calculated to be 4.9 nm [5] [6]. If the dimension of CdSe NPs is smaller than 4.9 nm, the **quantum confinement** of electron hole pairs effects significantly. As size is reduced, the electronic excitation shift higher energy, and there is concentration of oscillator strength into a few transitions [6].

For metal NPs, as described above, the Fermi level lies in the center of a band, so that the energy level spacing is very small. At temperature above a few Kelvin, the electrical and optical properties of a metal solid react more closely like those of no energy level spacing, even small as tens or hundreds of atoms [4]. Therefore, across almost entire size regime, their optical and electronic behaviors are described with classical equations rather than quantum mechanical concepts. The classical free electron theory combined with optical constants for bulk gold is employed to successfully model the intense visible extinction of Au NPs [7]. Moreover, the optical and electrical properties of metal NPs can also be tuned considerably by changing the size, shape or the extent of aggregation [7]. For example, a typical solution of 13 nm diameter Au NPs is red in color and exhibits a surface plasmon band centered at 518-520 nm. After aggregation, the extended polymeric Au NPs/polynucleotide aggregate shows a red to purplish blue color change in solution, due to a red shift in surface plasmon resonance of Au NPs [8]. (Surface plasmon resonance (SPR) is a surface-sensitive analytical technique based on the ability to detect dielectric constant changes induced by molecular adsorption at a noble metal thin film. In a typical experiment, the reflectivity of a

~50 nm thick Au film is measured as a function of incident angle. Metallic nanoparticles have been employed to enhance SPR response. These particles offer ease of preparation, high density, large dielectric constant, and biocompatibility [13]. The optical property of Au NPs is dominated by collective oscillation of conduction electrons resulting from the interaction with electromagnetic radiation. The electric field of incoming radiation induces the formation of a dipole in the NP. A restoring force in the NP tries to compensate for this, resulting in a unique resonance wavelength. The oscillation wavelength depends on particle size, particle shape and surrounding medium. [14]) In this work, the Au NPs serve as bridges that connect between CdSe NPs or between CdSe NPs and the electrodes, to deliver electrons from one to the other and enhance the overall conductivity of photo-sensing nanodevice composed of Au and CdSe NPs [5].

The electrical transport properties of nanocrystals also depend strongly on size. On extended crystal, the energy required to add successive charges does not vary. In a nanocrystal, the presence of one charge prevents the addition of another charge. Thus, in metal or semiconductor, the current-voltage curves of individual nanocrystal resemble a staircase, known as **Coulomb blockade effect** [4]. Steps in the staircase are spaced proportional to 1/radious of nanocrystal. A typical Coulomb blockade staircase is shown in Fig. 2.2.

The dynamics of the charge carriers in CdSe NPs have been studied in several reports. These studies revealed that photoexcitation leads to a bleach of the lowest exciton transition within the first few hundred femtoseconds [9]. The bleach recovery has a lifetime between several picoseconds to microseconds, which is similar to the lifetime of the photoluminescence. In literature, it is well-known that electron acceptors adsorbed on the surface of CdSe NPs quench the exciton emission by fast electron transition [9]. Investigation of CdS with methyl viologen cations as adsorbates (CdS-MV^+) showed that MV^+ is able to accept the photoexcited electrons from CdS NPs. Burda et al. monitored the

electrons shuttling across the interface of CdSe NPs by femtosecond laser spectroscopy and showed that in CdSe NPs with no electron acceptors adsorbed on the particle surface, the excited electrons get trapped at the surface within 30 ps. Subsequently, electron-hole recombination takes place on a much longer time period of > 10^{-7} s [9]. This is quite a useful knowledge for understanding the dynamics of electrons in CdSe NPs.

2.2 THE OPERATIONAL PRINCIPLES OF NANODEVICE

The optical and electrical properties of CdSe and Au NPs described above provide a potential application as photo-sensor. In this work, we used approximately 5 nm diameter CdSe NPs and approximately 15 nm diameter Au NPs to fabricate photo-sensing nanodevice on silicon oxide substrate of CMOS sensing chip, where the Au NPs serve as bridges to connect between CdSe NPs. The cross sectional figure of photo-sensing nanodevice on silicon chip is shown in Fig. 2.3.

Theoretically, the CdSe NPs with photoconductivity property are the main parts for photo-detection in the nanodevice structure. By illuminating the CdSe NPs with light source of wavelength for above bandgap excitation, the electrons in the nanocrystal will be excited to the particles surface, and be trapped on the surface for 30 ps. If the electric field between electrodes is large enough to take these electrons into current flow, the increased conductivity of nanodevice will be observed. However, if the electric field is not large enough or the nanostructure of CdSe NPs is partially damaged by photooxidation, the phenomenon of increased conductivity after illumination will not be observed. For Au NPs, they have no response to illumination, even with quantum size. As we described above, across all size regime, the Au NPs are always behave like pure metal.

In addition to the photoconductivity property of CdSe NPs, the junctions between CdSe and Au NPs are also very important in photo-sensing behavior. Any interface between CdSe

and Au NPs will result in a “nano Schottky diode” structure. For a nano diode structure, it is reasonable to detect photo illumination, like the photodiode structure based on p-n junction.

2.3 THE OPERATIONAL PRINCIPLES OF CMOS SENSING CIRCUIT

As we discussed in section 1.3, one of the main goals of this work is to fabricate the photo-sensing nanodevice directly on the surface of CMOS sensing chip, where a CMOS sensing circuit embedded in silicon substrate is designed to linearly amplify the signal generated by nanodevice. Therefore, after finishing the development of technologies to control NPs in photo-sensing nanodevice formation, we start to construct the nanodevice directly on the silicon oxide region of CMOS sensing chip. Then, we will measure the electrical property of the nanodevice by using the electrodes structure on CMOS sensing chip. Finally, the electrodes will be connected to CMOS sensing circuit, and the measurement of nanodevice combined with circuit will be accomplished. In this section, we will first introduce CMOS sensing circuit.

Theoretically, the CdSe NPs have well-known size-dependent photoconductivity property, which means that the conductivity of CdSe NPs will increase when illuminated with light source of proper wavelength. When the size of particles becomes smaller, the energy bandgap will become larger, resulting in blue-shift of absorbance spectrum. In contrast, the Au NPs have no photoconductivity behavior like CdSe NPs and behave like metal material regardless of the size variation. However, when the two NPs are assembled together to form nanodevice on silicon oxide substrate, the overall conductivity of the nanodevice is expected to have photo-sensing property. But, the mechanism and measurement of this photo-sensing property is still unclear in literature. Therefore, in this work, CMOS sensing circuit is designed to detect the transient dc conductivity of photo-sensing nanodevice when illuminated

with light of different wavelength. In conductivity measurement, to make electrodes attach firmly to the nanodevice is conventionally the most difficult part. In this work, to form electrodes structure, we take advantage of the passivation window opened up over the two Al metal lines of little spacing (less than 1 μm), as shown in Fig. 3.1(a) or Fig. 3.19(a). The silicon oxide region is the place to form nanodevice and eventually the nanodevice will touch the two Al electrodes.

To detect the transient dc conductivity, there are two commonly used methods---to apply a constant voltage across the nanodevice and measure the resulting current or to apply a constant current through the nanodevice and measure the resulting voltage across. The second one is difficult to implement because it is hard to generate a constant current source of very small quantity (≤10 nA) if the dc resistance of nanodevice is very large (it is possible to be ≥300 MΩ). Therefore, in this work, we adapt the first method---that is to apply a constant voltage bias across the nanodevice and measure the resulting small current (designed to be 200 nA) flowing through device. The most convenient method to linearly amplify the small dc current is to integrate the current with time by charging a capacitance. The schematic of CMOS sensing circuit is shown Fig. 2.4. The characteristics of this circuit are: First, low current (200 nA) flowing through the photo-sensing nanodevice, preventing from unanticipated oxidation or other forms of damage of the device. Second, high linearity and sensitivity.

The **Mc1 Md1~4** and **Mf** form an operation amplifier with negative feedback loop to stabilize and lock the voltage at **Vip** with **Vin**. **R**t is representative of the photo-sensing nanodevice and the voltage difference between **Vbias** and **Vip** is the voltage bias across the nanodevice (Vcross). The current flowing through nanodevice is linearly amplified by current mirror **Mcm1-Mcm2** and **Mcm6-Mcm8**, each current mirror providing dc current gain 5 and 6 respectively. The current signal generated by nanodevice has two parts, the background current when dark and the added light current due to illumination. Only the

light current is the signal we desire. As a result, the constant background current is subtracted by **Ioffset**, to make only the added light current able to charge capacitance **Ca** and make integration with time. In this circuit, **Mcm5**, **Mcm7**, **Mcm4** and **Mcm9** are used to form cascode structure to make current mirrors have larger output resistance. **Reset**, **Ms1** and **Ms3** are used to control the length of charging and discharging time period. Finally, **Mcm12** and **Mcm15** form the output stage. The DC analysis of CMOS sensing circuit is shown below:

Output (dark) = [(Vcross / Rto) * Ai – Ioffset] * Tcharge * (1 / Ca)

Output (illumination) = [Vcross / (Rto – dRto) * Ai – Ioffset] * Tcharge * (1 / Ca)

Output (illumination) – Output (dark)

= (Vcross * Ai * Tcharge / Ca)[(1 / Rto – dRto) – (1 / Rto)]

≈ (Vcross * Ai * Tcharge / Ca)(**dRto** / Rto^2) if dRto << Rto

(Ai = *DC current gain = 5 * 6 = 30*, Vcross = *voltage bias across the device*

Rto = *the resistance of nano-photo-sensing device under dark situation*

dRto = *the reduction of resistance while illuminating*

Ca = *the charging capacitance = 5.5 pF*)

The Hspice simulation result (tt) of CMOS sensing circuit is shown in Fig. 2.5. The voltage bias of the simulation is shown in Table 2.1. The simulation result of output versus the resistance value of photo-sensing nanodevice is also shown in Fig. 2.6. In addition to the output waveforms, it is also very important to make sure the voltage value of Vip is locked to that of Vin due to the existence of operational amplifier and negative feedback loop. A part of list file of the simulation result is shown below. As we can see, the vds of Md4 + the vgs of Mf = 1.1883 + 0.514 = 1.7 = Vin. Besides, the current flowing through Rt is 203.5377

nA, the value we desire. Finally, the simulation results of the other four corners (ss, sf, fs, ff) are also accomplished and checked for all mosfets in saturation region and the whole circuit in normal function.

**** mosfets

subckt						
element	0:mc1	0:md1	0:md2	0:md3	**0:md4**	**0:mf**
model	0:pch.11	0:pch.11	0:pch.11	0:nch.11	0:nch.11	0:pch.4
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-181.3538u	-91.2416u	-90.1122u	91.2416u	90.1124u	**-203.5377n**
ibs	35.5626a	13.0636f	13.0636f	-130.5222a	-128.9090a	115.9100a
ibd	8.1777f	48.8975p	145.3387p	-49.2477f	-49.2476f	116.0089a
vgs	-1.0000	-926.4175m	-923.7511m	703.2203m	703.2203m	**-1.1883**
vds	-373.5825m	-1.9232	-2.1121	703.2203m	**514.3597m**	-1.0373
vbs	0.	373.5825m	373.5825m	0.	0.	1.2973
vth	-751.9120m	-811.8320m	-810.4549m	565.7736m	566.2257m	-1.0087
vdsat	-281.3432m	-167.4955m	-166.4362m	150.3598m	150.0299m	-211.8233m

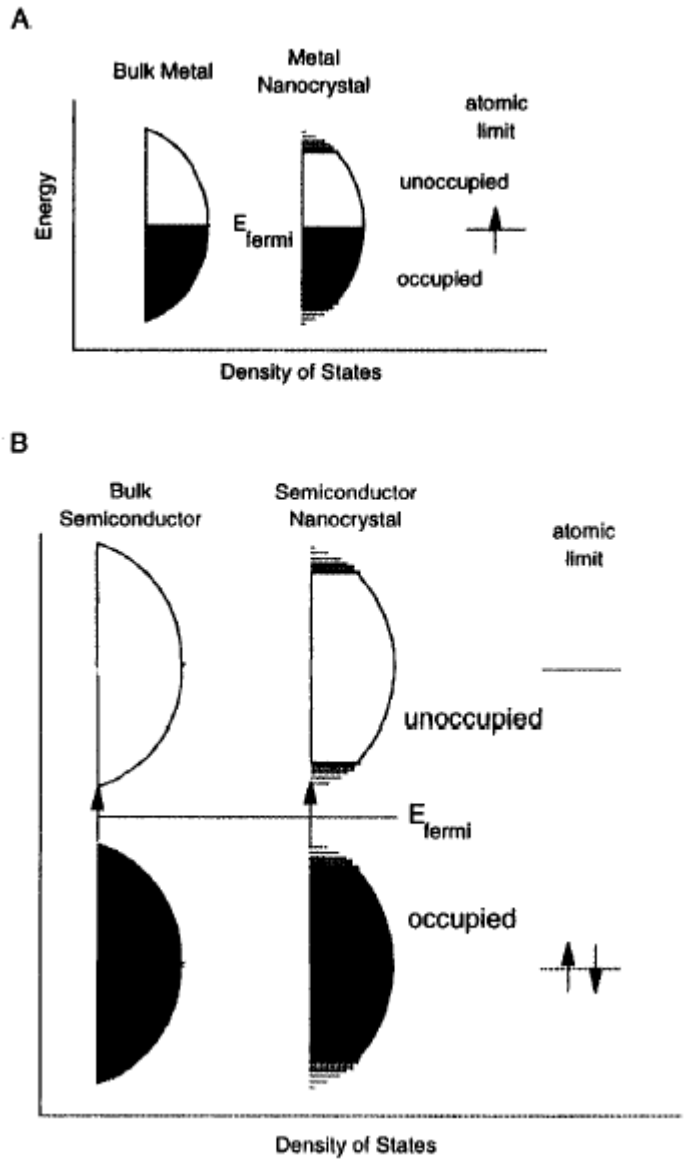
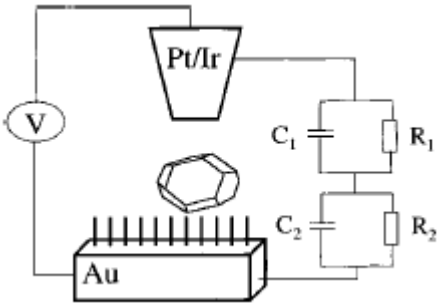
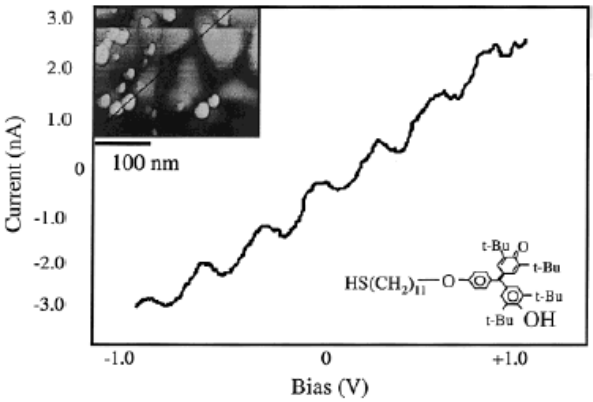


Fig. 2.1 Density of states in metal (A) and semiconductor nanocrystals (B). In each case, the density of states is discrete at the band edges. In metal, the Fermi level is in the center of a band. As a result, kT will exceed the level spacing even at low temperature and small size. In semiconductor, the Fermi level lies between two bands, so that there is large level spacing even at large size. The HOMO-LUMO gap increases as the semiconductor nanocrystals become smaller (bellow 10 nm) [4].



(a)



(b)

Fig. 2.2 (a) Illustration of a STM tip-single metal NP-insulator coated gold substrate double tunnel junction and corresponding equivalent circuit. (b) Current versus voltage for a single galvinol-coated Au NP acquired in aqueous solution at pH 5. Insect shows an STM image of the sample. Tip was coated with Apiezon wax and gold substrate was coated with hexanethiol [7].

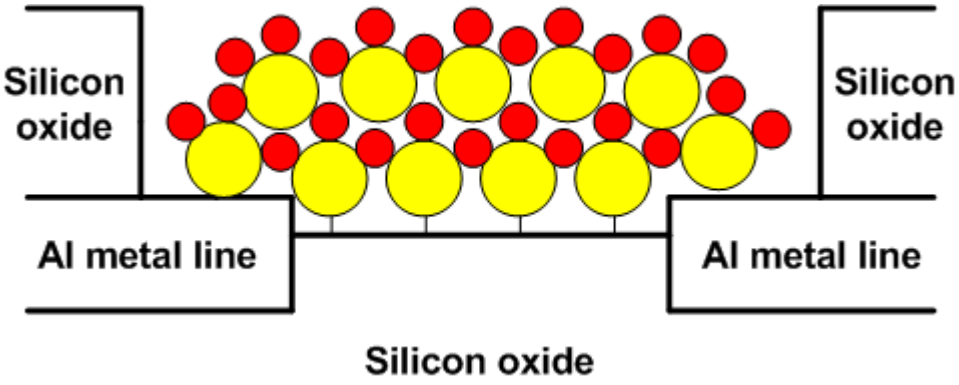


Fig. 2.3 The cross sectional figure of photo-sensing nanodevice on CMOS sensing chip

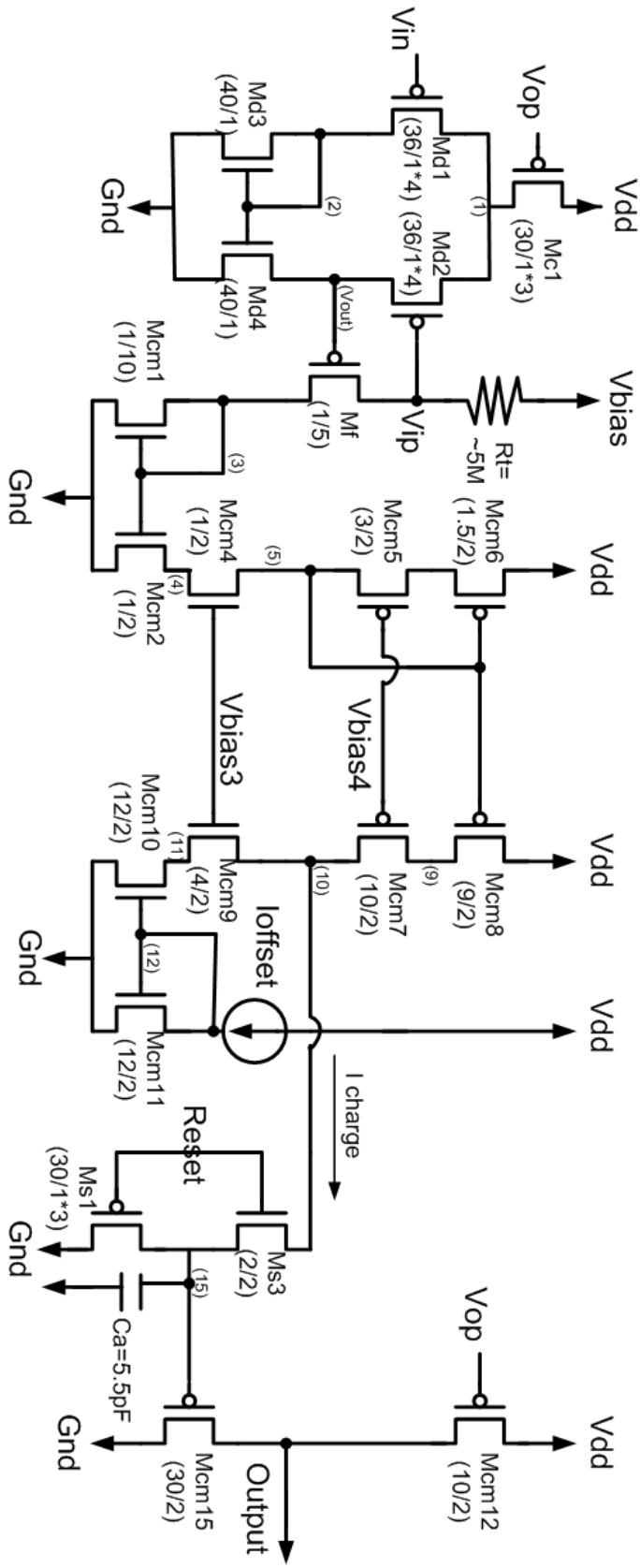
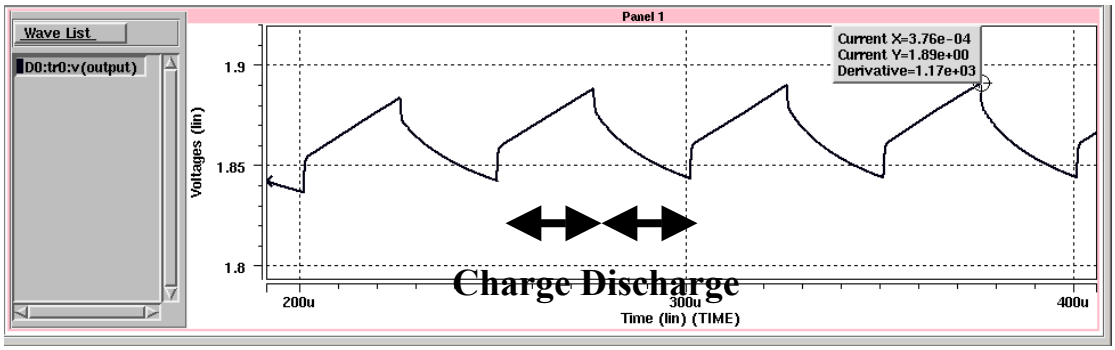


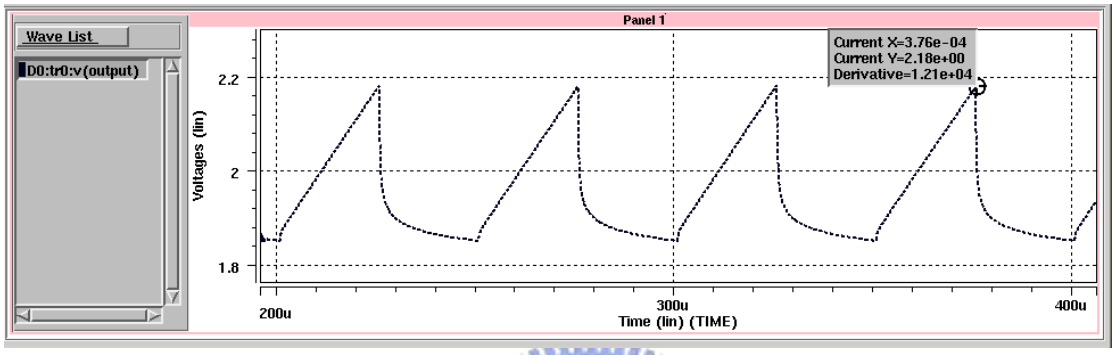
Fig. 2.4 The schematic of CMOS sensing circuit.

Vdd	3 V
Vop	2 V
Vin	1.7 V
Vbias	2.7 V
Vbias3	1.3 V
Vbias4	1.5 V
Ioffset	7.82 μA
Reset	Square wave, 3~0 V, 20 kHz
Rt	5.00 MΩ~4.75 MΩ

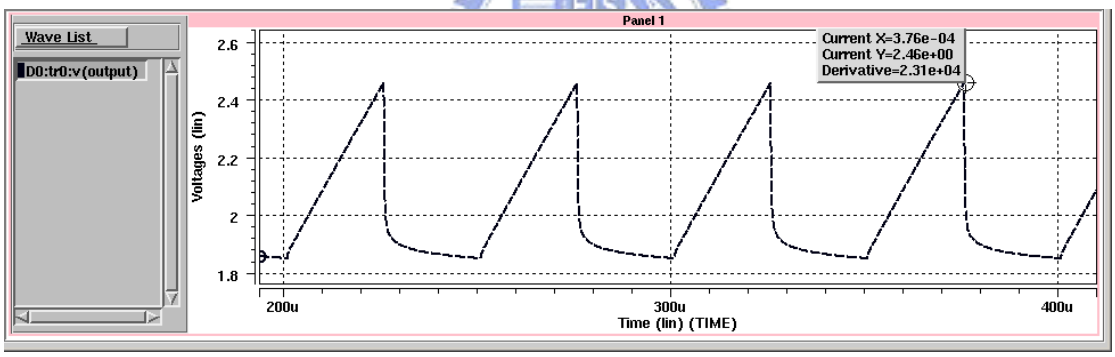
Table. 2.1 The voltage biases of CMOS sensing circuit for simulation results shown below.



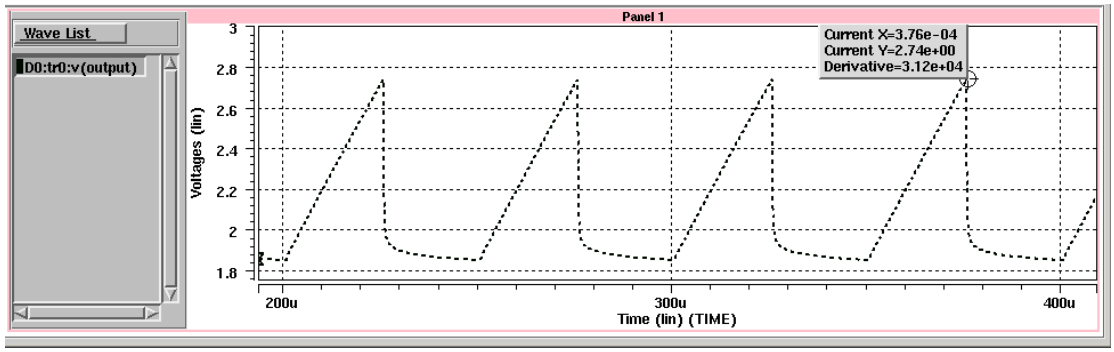
(a) Rt = 5.00 MΩ



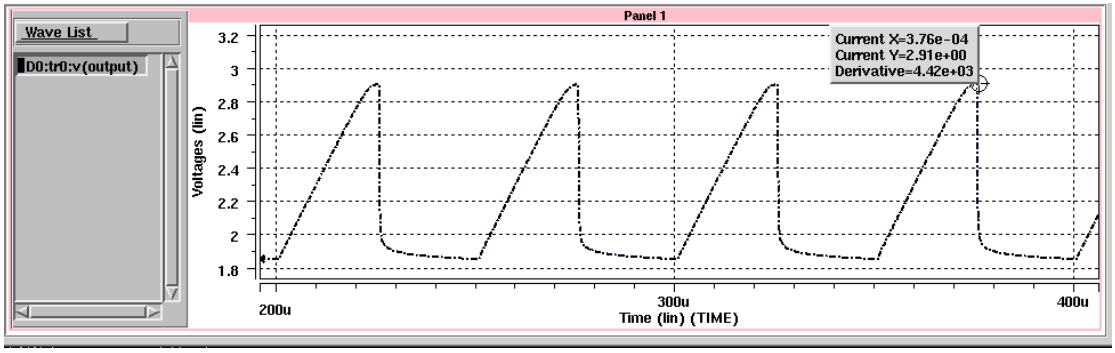
(b) Rt = 4.95 MΩ



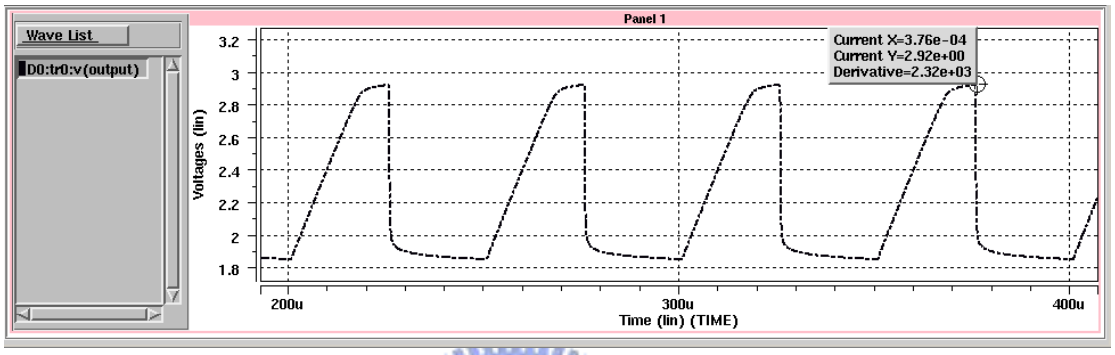
(c) Rt = 4.90 MΩ



(d) Rt = 4.85 MΩ



(e) Rt = 4.80 MΩ



(f) Rt = 4.75 MΩ

Fig. 2.5 The Hspice simulation of CMOS sensing circuit (a)~(f). The curve in the figure of different Rt value represents the output signal in Fig. 4.1.

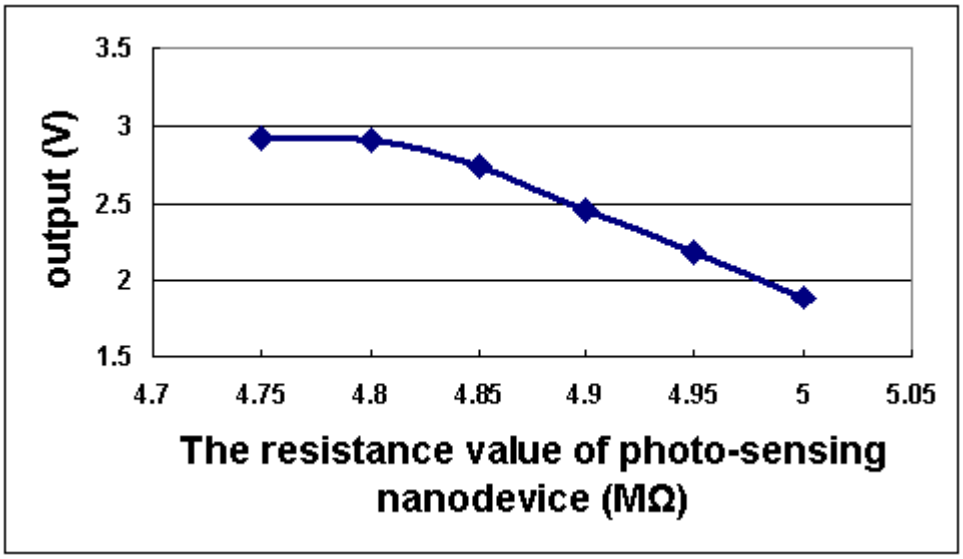


Fig. 2.6 The simulation result of output versus Rt, the resistance value of photo-sensing nanodevice, is shown above. When the resistance of Rt is below 4.85 MΩ, the output will saturate because Mcm12 will leave the saturation region, entering triode region.