CHAPTER 4

THE EXPERIMENTAL RESULTS AND DISCUSSIONS

4.1 THE EXPERIMENTAL RESULTS OF CMOS SENSING CIRCUIT AND DISCUSSIONS

The layout figure of entire CMOS sensing chip is shown in Fig. 4.1. The most significant characteristic of the layout design of CMOS sensing chip is the electrodes structure and the combination with CMOS sensing circuits on the same silicon substrate. The electrodes structure are fabricated by using passivation window over two closely separated (0.8 μm~15 μm) metal lines, as shown in Fig. 3.1(a), Fig. 3.19(a) and Fig. 4.2. The electrodes are placed at the center of silicon chip surface for convenient nanodevice construction. The SEM image of the 13 electrodes and their sizes (width * length of oxide region between electrodes) are shown in Fig. 4.3. The central 6 electrodes, (1)~(6), are connected to the six identical CMOS sensing circuits. The rest seven electrodes are connected directly to pads for direct measurement. The silicon oxide region, the place for nanodevice construction, is a little over etched in real fabrication process, which will be discussed in detail in section 4.2.

The measurement results of CMOS sensing circuit are shown in Fig. 4.5. The measurement result of output voltage versus the value of Vbias is shown in Fig. 4.8. The voltage biases of CMOS sensing circuit under measurement are shown in Table 4.2. In this measurement, instead of changing Rt, we changed the Vbias to simulate the changing Rt for convenience in measuring. In other words, Rt is fixed at 3.22 MΩ and Vbias is ranging from 2.00 V to 2.35 V to simulate the conductivity variation of photo-sensing nanodevice under dark or illumination. Another important part of the measurement is to check if Vip is locked

with Vin. As we can see, the value of Vip is very close to Vin = 1.355 V, which means the gain of negative feedback loop is large enough to lock Vip with Vin. As for the value of current flowing through Rt---It, it was first set to 200 nA in both Hspice simulation and this measurement.

The main drawback of the circuit is that the current flowing through Rt, 200 nA, is too small to make Mcm1 enter saturation region in real measurement. In other words, Mcm1 and Mcm2 enter sub-threshold region because the voltage value of (3), the gate voltage of Mcm1 and Mcm2, is too small (less than 0.6 V). This phenomenon has not been observed in Hspice simulation result. Therefore, we have to decrease Vbias3 in order to make the V_{DS} value of Mcm1 and Mcm2 approach to the same, so as to have a better linearity. If we lower Vbias3, it is necessary to increase Vbias4 to make Mcm6 work in saturation region. Mcm8 and Mcm9 must work in saturation region because the voltage value of (10) is ranging from [Vthp of Ms1] (≈0.75 V) to [Vdd - (V_{OV} of Mcm12) – (V_{SG} of Mcm15)] (≈2 V), which provides a wide range for Mcm8, 9 to operate in saturation region. However, the lowered Vbias3 will force Mcm9 to consume most of the voltage range from (10) to ground, which will make Mcm10 operate in triode region when (10) is not large enough. This is the reason why we see there are transitions in curves of the measurement results from the start of charging.

4.2 THE EXPERIMENTAL RESULTS FOR FABRICATION OF NANODEVICE ON CMOS SENSING CHIP

The construction process of photo-sensing nanodevice on CMOS sensing chip is similar to that on SiO_2/Si wafer fragments, as described in section 3.2.3. First, the silicon oxide surface is modified by N-[3-(trimethoxysilyl)propyl]-ethylene diamine (TMSPED), which provides positive-charged amino ($-NH_3^+$) groups to attract negative ($-COO^-$) charged Au NPs.

Then, the Tyramine-modified CdSe NPs that have positive-charged amino groups on particle surfaces are assembled on Au NPs. Theoretically, the assembly process can be repeated for several times to form multi-layers structure of Au and CdSe NPs. The fabrication process of photo-sensing nanodevice on silicon oxide substrate of TSMC 0.35 μm silicon chip was observed by SEM, as shown in Fig. 4.6, Fig 4.7 and Fig 4.8. The overall experimental procedure of fabrication and measurement of photo-sensing nanodevice on TSMC 0.35 μm silicon chip is shown in Fig 4.9.

4.3 THE ENVIRONMENT SETUP FOR NANODEVICE MEASUREMENT

The measurement environment setup is shown in Fig. 4.10. The laser diode, laser diodes driver, optical measurement table and the clean room are all in Professor Eric Diau's Femtochemistry Laboratory. The laser diode driver is PicoQuant POL 800D and the 375 nm laser diode is PicoQuant LDH-P-C375. The current meter is Keithley 2410 1100V SourceMeter. The vacuum chamber is fabricated in Experimental Equipment Center, National Tsing Hua University. The PCB on which there is nanodevice-modified TSMC 0.35 μm silicon chip was located in vacuum chamber. During the measurement, the environment was kept in dark except the laser diode.

4.4 THE EXPERIMENTAL RESULTS OF NANODEVICE MEASUREMENT AND DISCUSSIONS

The measurement was performed by applying voltage biases to electrodes and measuring the current flowing through nanodevice while in dark or illumination of 375 nm laser diode. The electrodes under measuring and the measurement result are shown in Fig. 4.11 and Fig.

4.14, respectively. Electrodes 1 and 2 have silicon oxide region of 30 μm * 15 μm and 30 μm * 5 μm (width * length) respectively. Both electrodes are connected directly to pads without connection with CMOS sensing circuits, because here we focused on the electrical property of photo-sensing nanodevice composed on Au and CdSe NPs. The photo-sensing nanodevice structure is two layers of approximately 15 nm diameter Au NPs combined with two layers of approximately 5 nm CdSe NPs (CdSe NPs + Au NPs + CdSe NPs + Au NPs on silicon oxide substrate), as shown in Fig. 4.12(b). The multi-layers structure of Au and CdSe NPs resembles those shown in Fig. 3.24 and Fig. 3.25. In Fig. 4.13, we show the reflective UV-visible absorbance spectrum of this multi-layers structure, which proves that the 375 nm laser diode was an effective light source for this nanodevice. Because of the limitation of instrument, we showed only the range from 320 nm to 800 nm.

If there is only one layer of Au NPs labeling between electrodes, as shown in Fig. 4.12(a), the resistance across the electrodes is as large as those across blank electrodes. The current flowing through any blank electrodes is less than 10 fA under the same voltage biases in this measurement and has no response to illumination.

There are several notable characteristics of the measurement results, shown as following:

(1) **The Width/Length of the electrodes:** With the same width, the larger length of the electrodes is, the less conductivity of nanodevice we got, however the better variation margin after illumination. For electrodes 1 (30 μm * 15 μm), it had average R_{dark} = 33.1 kΩ, and average difference $I_{illumination} - I_{dark}$ = 1.8 nA. In contrast, for electrodes 2 (30 μm * 5 μm), it had average R_{dark} = 24.1 kΩ, and average difference $I_{illumination} - I_{dark}$ = 1.2 nA. Theoretically, with the same length, the larger width of the electrodes will result in the better conductivity and worse variation margin.

(2) **The density of Au NPs in the composition of nanodevice structure:** As we discussed previously, the Fermi level lies in the center of a band, so that the energy level spacing is very small in Au NPs. Therefore, in this work, the Au NPs serve as bridges that connect

between CdSe NPs, to enhance the conductivity of nanodevice. In this measurement, we had two layers of Au NPs and two layers of CdSe NPs on silicon chip surface, where the density of Au NPs is large enough that we can observe gold color on the surface by naked eyes.

(3) **The freshness of CdSe NPs and Au NPs:** The CdSe NPs are very unstable with respect to photooxidation and the attack from air or water. From the moment that the synthesis of HDA-coated CdSe NPs were finished, every operation would threaten the intrinsic optical and electrical property of CdSe NPs by the redox cycles within a few days, including the Tyramine modification, the assembly process, the bonding wires process, and the long storage period. For Au NPs, although there is no specific harmful oxidation reported in literature, the particle solution is still as fresh as possible. In this measurement, all the preparation of Au and CdSe NPs, assembly process, and measurement are finished within one week, to ensure the freshness of particles.

(4) **The "nano Schottky diode" behavior of I-V curves:** As we can see the I-V curves in Fig. 4.13, the difference between $I_{illumination}$ and I_{dark} is almost constant, 2 nA for Electrodes 1 and 1.2 nA for Electrodes 2. This phenomenon is a little similar to the I-V behaviors of conventional photodiode based on p-n junction. In this nanodevice structure we proposed here, any interface between a CdSe and Au NP will result in the "nano Schottky diode" structure, where some are forward bias and some are reverse. Besides, compared to conventional Schottky diode structure, the nano diode here is quite different, because both CdSe and Au NPs are not bulk material described in conventional Schottky diode and many organic modification molecules are included in the interface. In addition to Schottky diode effect, there may be some other mechanisms that affect the I-V behaviors of nanodevice, including the photoconductivity property of CdSe NPs. However, the thousands to millions nano Schottky diodes seem to dominate the overall behavior.

(4) **Structural property and intrinsic optical and electrical properties of nanodevice:** The

structural property of nanodevice means the density and uniformity of NPs packing, which can be observed by SEM on the corresponding structure on SiO_2/Si wafer fragments. The intrinsic optical and electrical property can be measured by UV-visible absorbance spectrum and PL of Au and CdSe NPs. Both properties are very important to the measurement results.

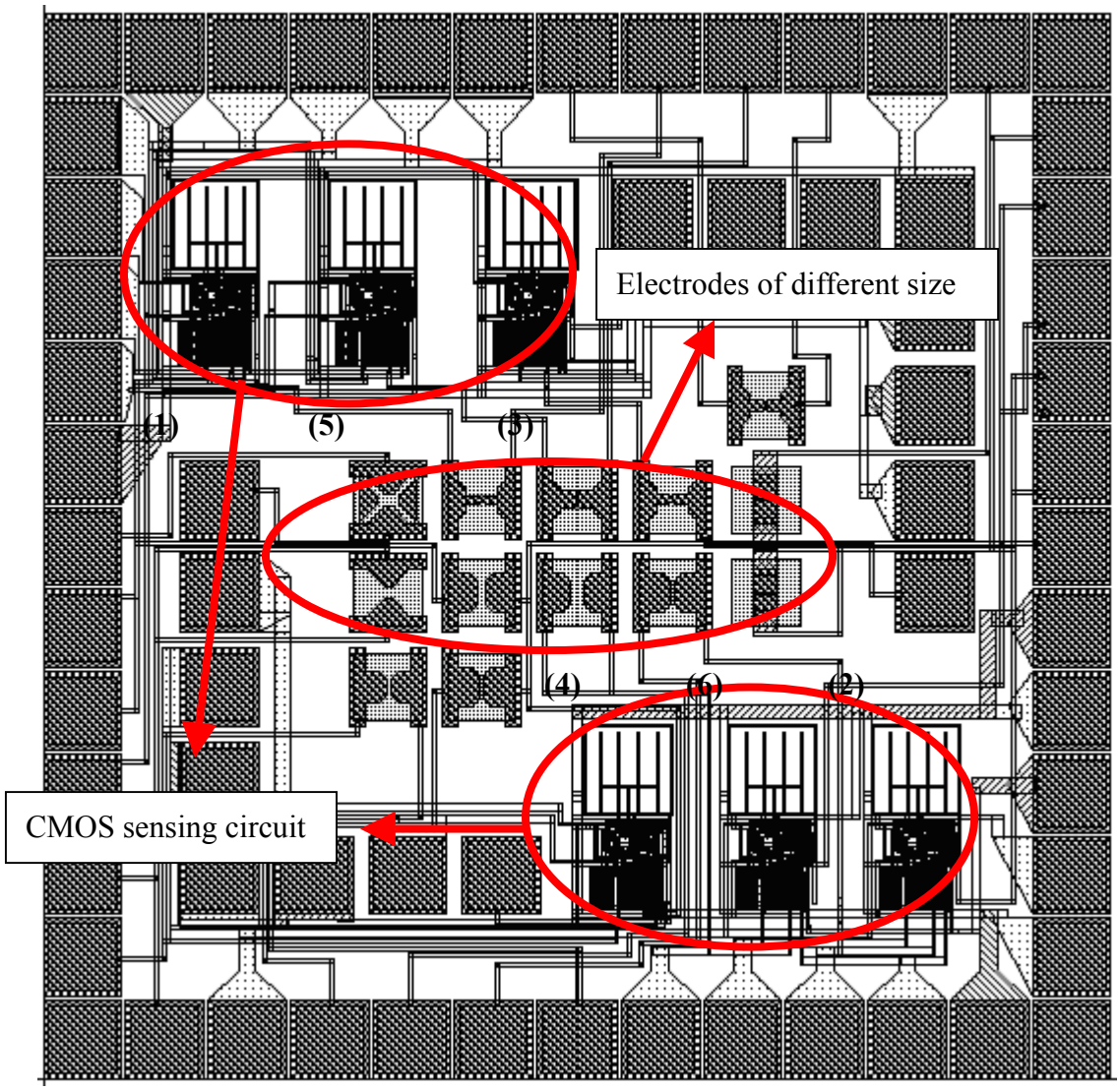


Fig. 4.1. The layout of the CMOS sensing chip is shown above. The chip is 1.35 mm * 1.35 mm and has 48 pins. There are six identical CMOS sensing circuits, (1)~(6)

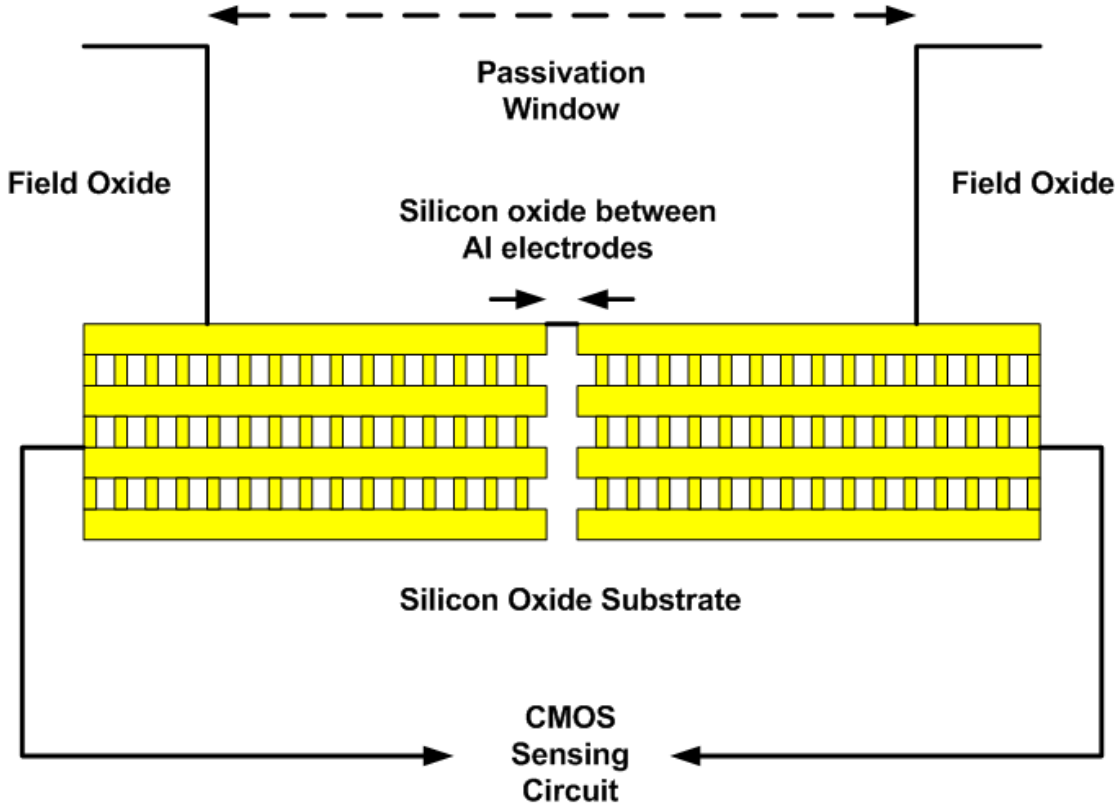
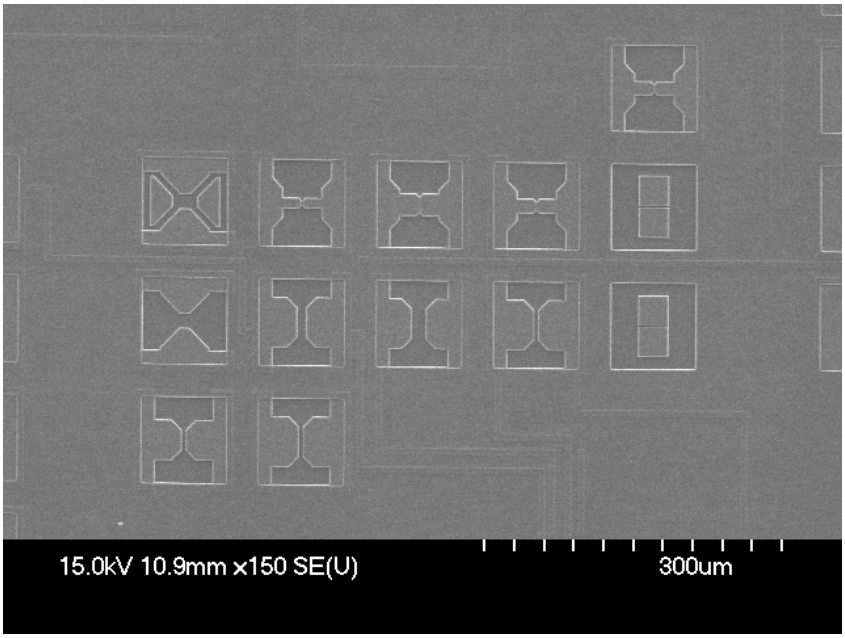


Fig. 4.2. The cross section figure of electrodes structure is shown above, where the four layers of metal lines are connected by vias. The passivation window in this work is 86 μm * 86 μm. The silicon oxide region between Al electrodes has different shapes. The length of the region is ranging from 0.8 μm to 15 μm.



(a)

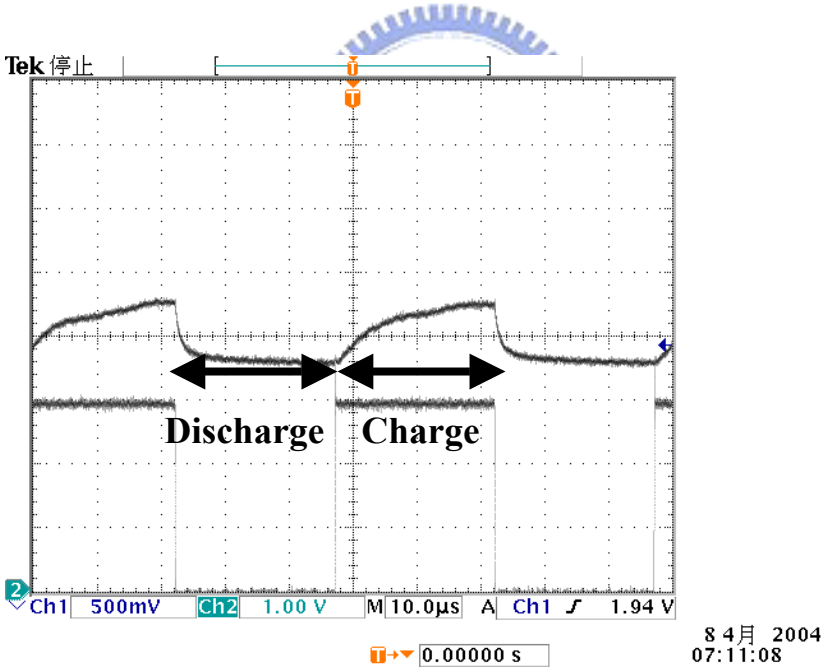
				E1=8*0.8
E7=15*10	(1)=4*0.8	(5)=16*0.8	(3)=8*0.8	E2=30*2
E6=15*10	(4)=30*10	(6)=30*15	(2)=30*5	E3=30*0.8
E5=20*5	E4=30*5			

(b)

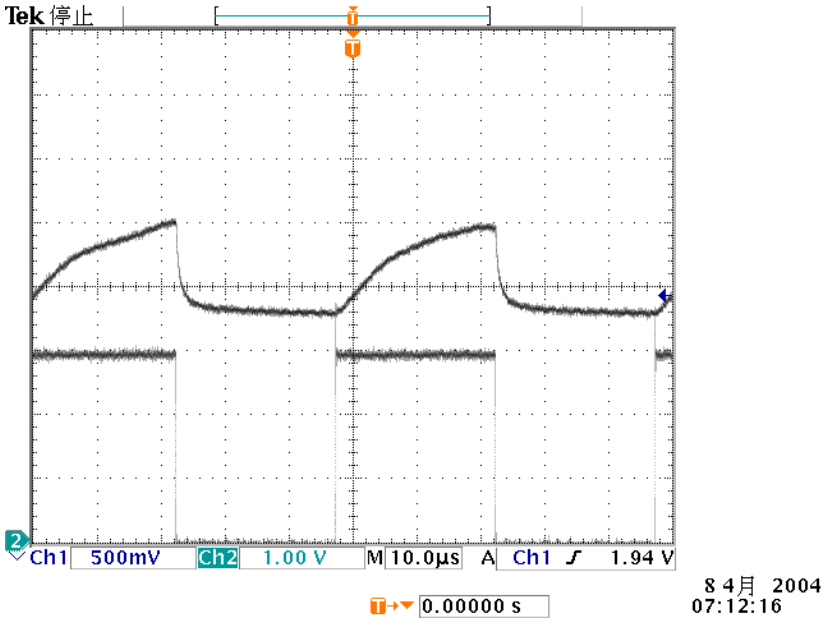
Fig. 4.3. (a) The SEM image of the 13 electrodes. (b) The size (width * length between electrodes) table of the corresponding 13 electrodes. The central 6 electrodes, (1)~(6), are connected to the six identical CMOS sensing circuits. The rest seven electrodes are connected directly to pads for direct measurement.

Vdd	3 V
Vop	2 V
Vin	1.3767 V
Vbias	2.10 V~2.35 V
Vbias3	0.75 V
Vbias4	2.00 V
Ioffset	7.25 μA
Reset	Square wave, 3~0 V, 20 kHz
Rt	3.22 MΩ

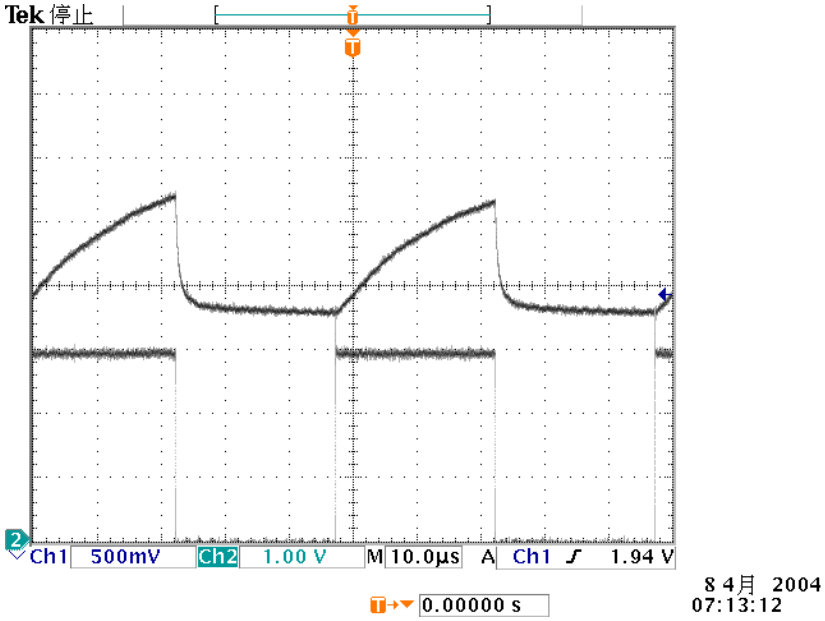
Table. 4.1 The voltage biases of CMOS sensing circuit for this measurement results shown below.



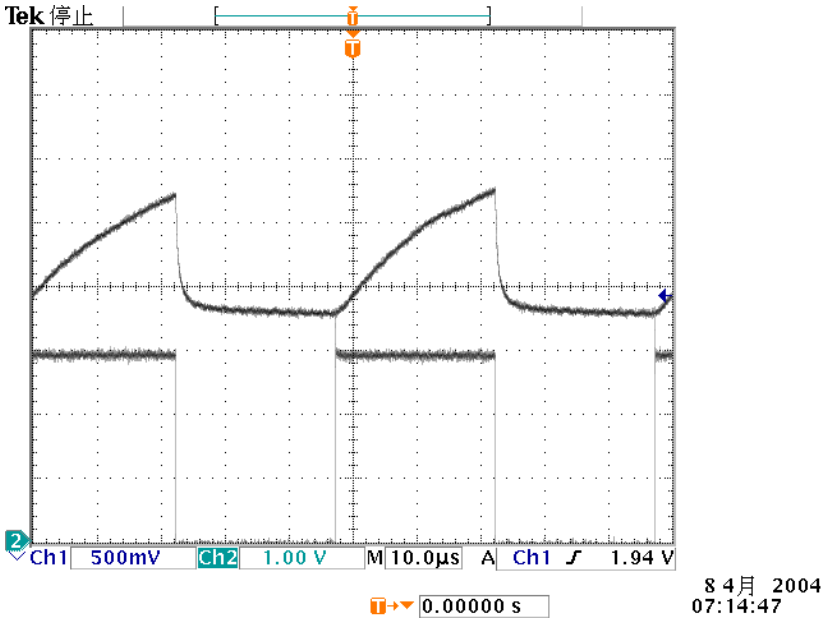
(a) Vbias = 2.10 V, Vip = 1.3785 V, It = 224 nA, output = 2.25 V



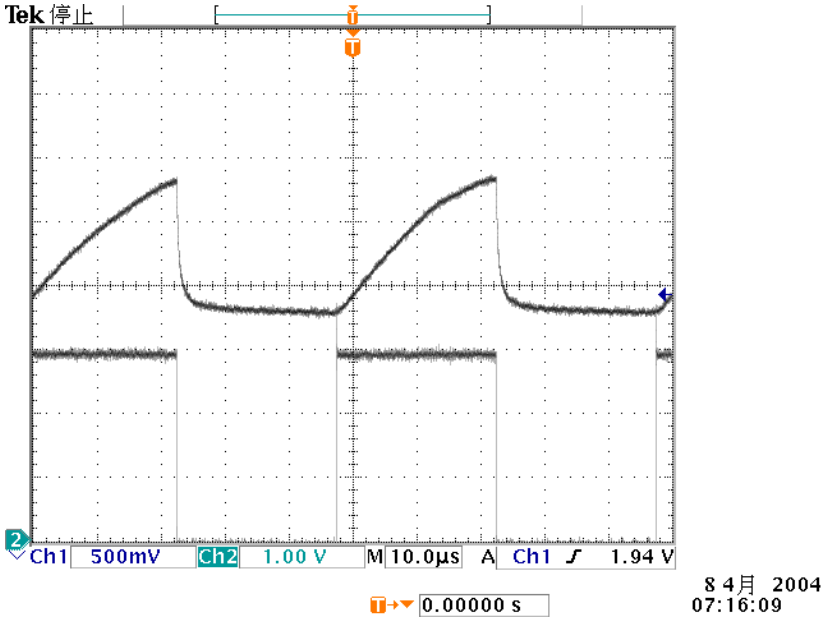
(b) Vbias = 2.15 V, Vip = 1.3798 V, It = 239 nA, output = 2.50 V



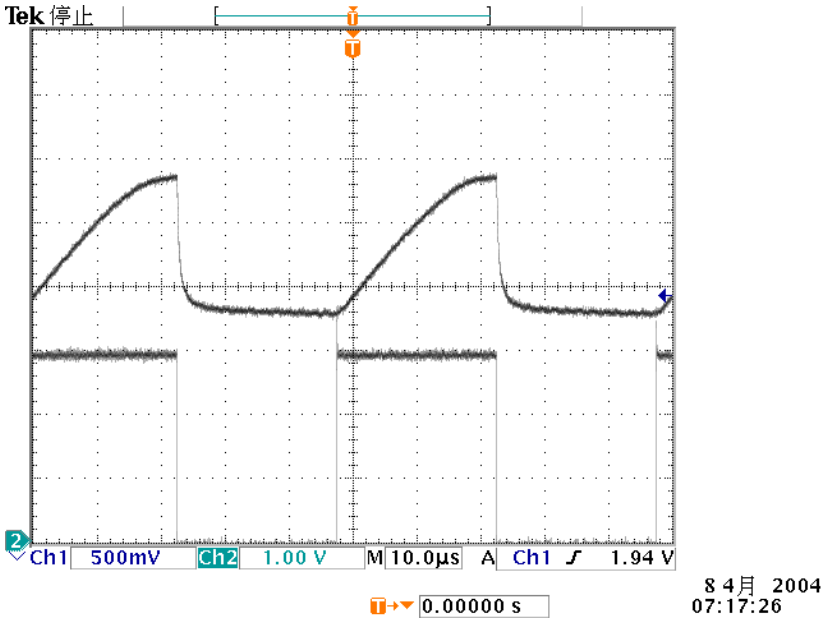
(c) Vbias = 2.20 V, Vip = 1.3812 V, It = 254 nA, output = 2.70 V



(d) Vbias = 2.25 V, Vip = 1.3820 V, It = 270 nA, output = 2.80 V



(e) Vbias = 2.30 V, Vip = 1.3829 V, It = 285 nA, output = 2.85 V



(f) Vbias = 2.35 V, Vip = 1.3841 V, It = 300 nA, output = 2.85 V

Fig. 4.4 The measurement results of CMOS sensing circuit are shown above (a)~(f), where It means the current following through the Rt. In this measurement, instead of changing Rt, we change the Vbias to simulate the changing Rt for convenience in measuring. The value of Vip is very close to Vin = 1.355 V, which means the gain of negative feedback loop is large enough to lock Vip with Vin.

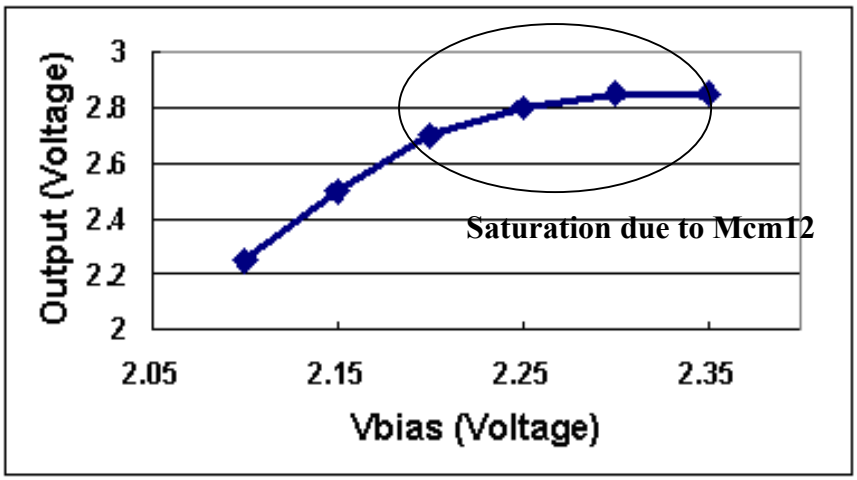
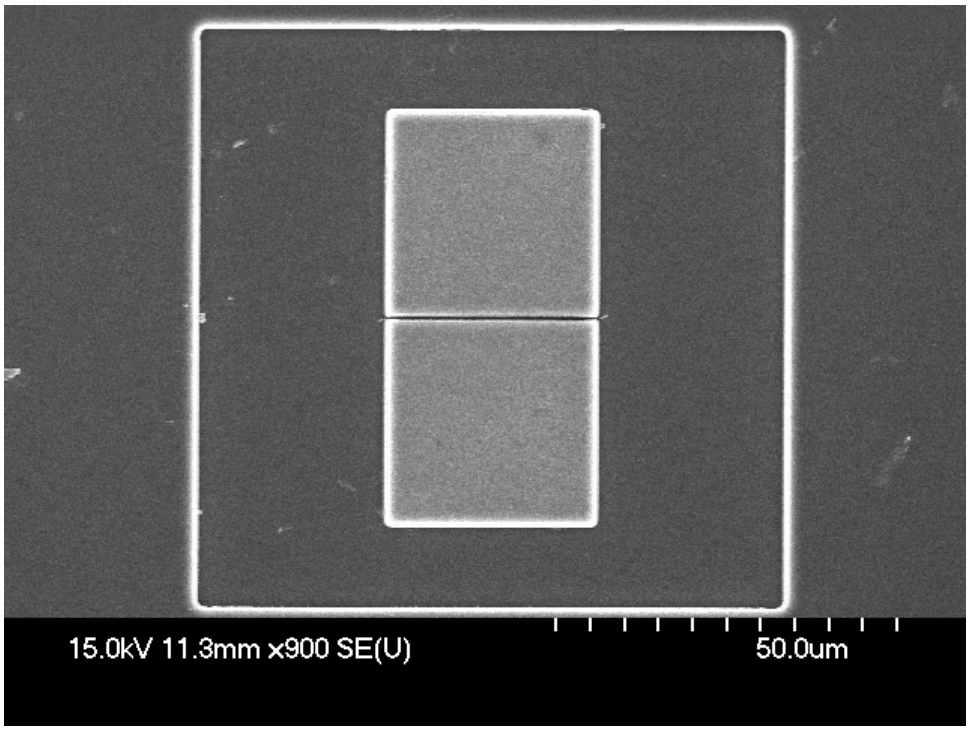
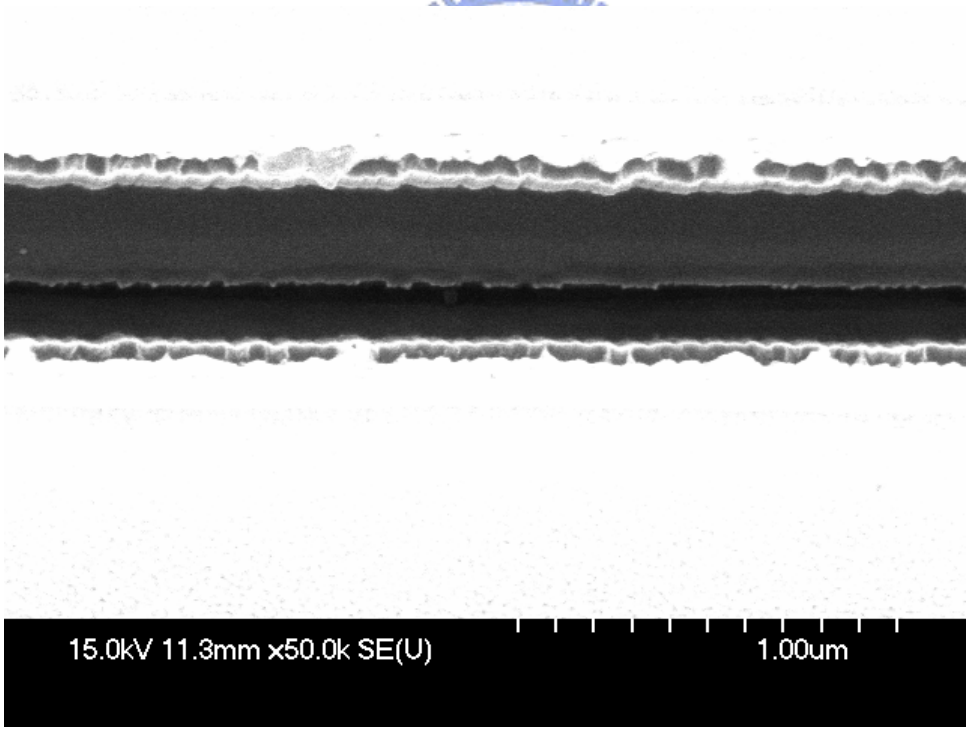


Fig. 4.5 The measurement result of output versus Vbias.

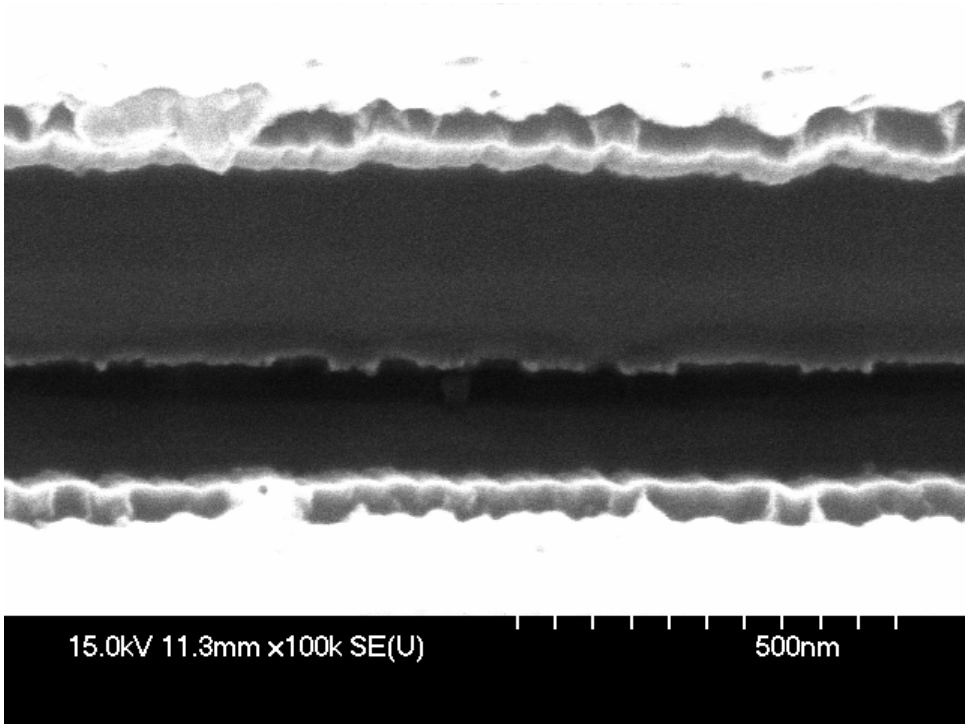


Silicon oxide region between Al electrodes is 30 μm * 0.6 μm

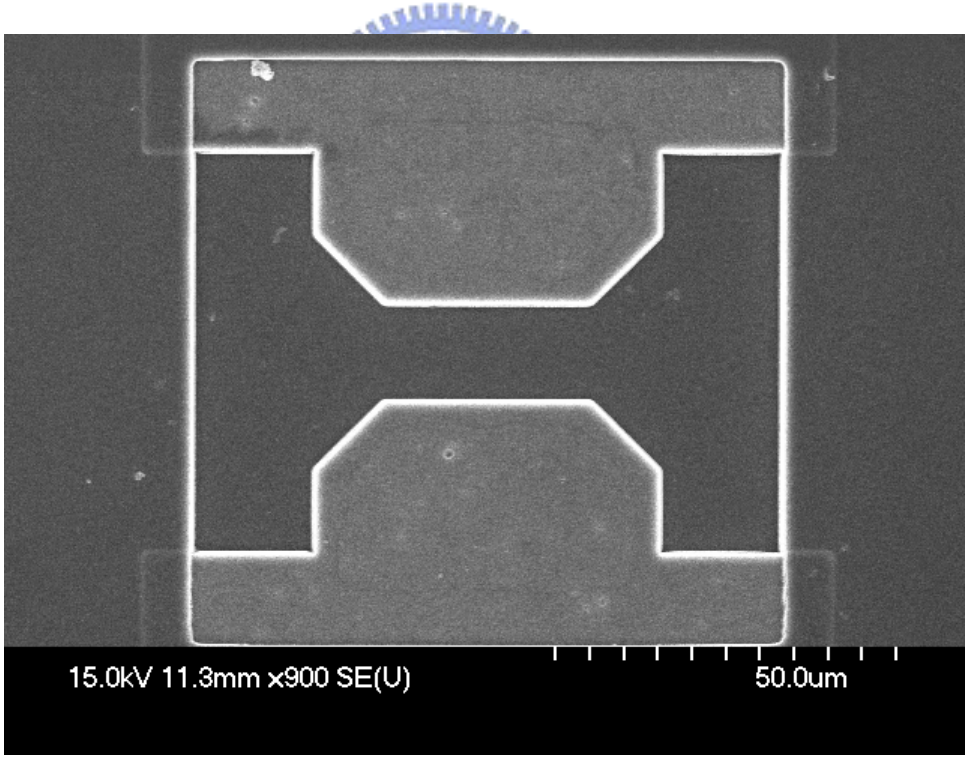
(a_*900)



(a_*50k)

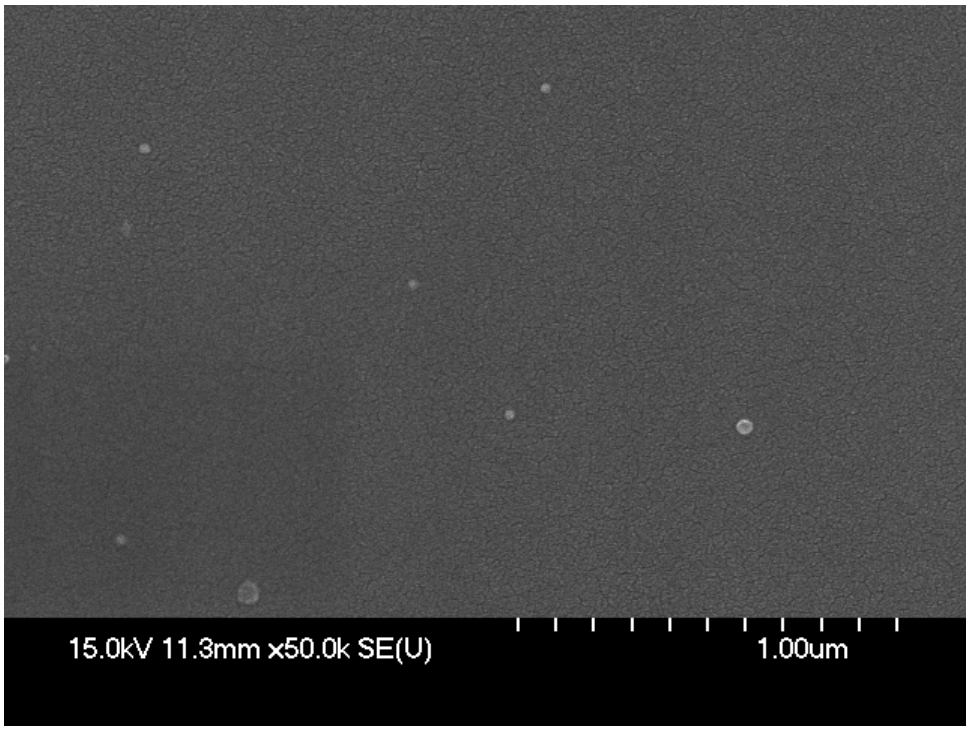


(a_*100k)

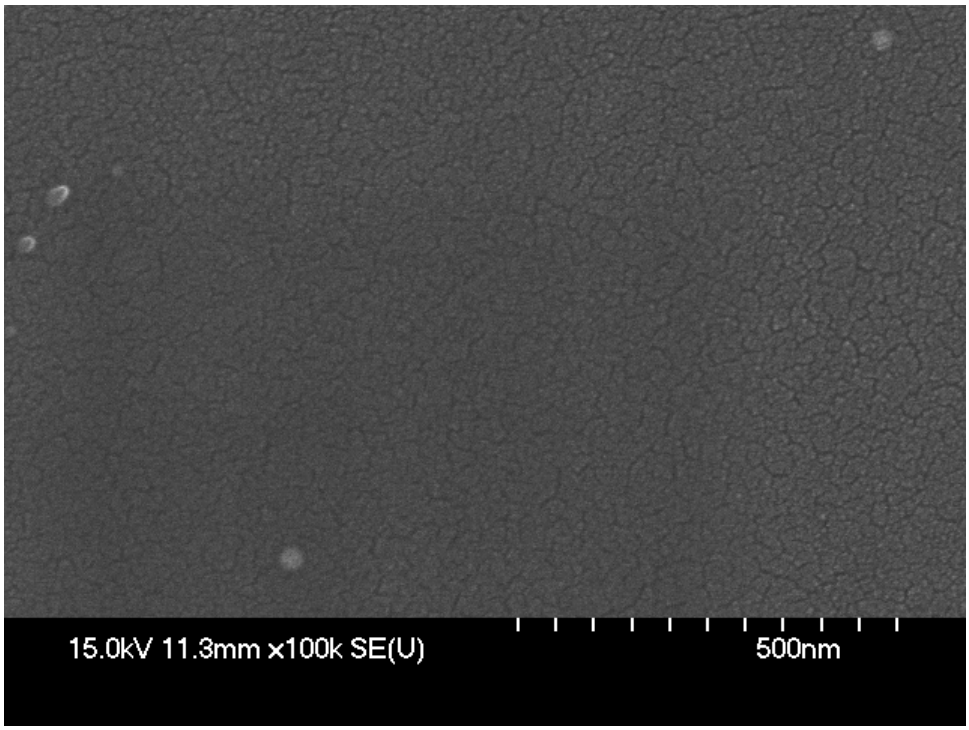


Silicon oxide region between Al electrodes is 30 μm * 15 μm

(b_*900)

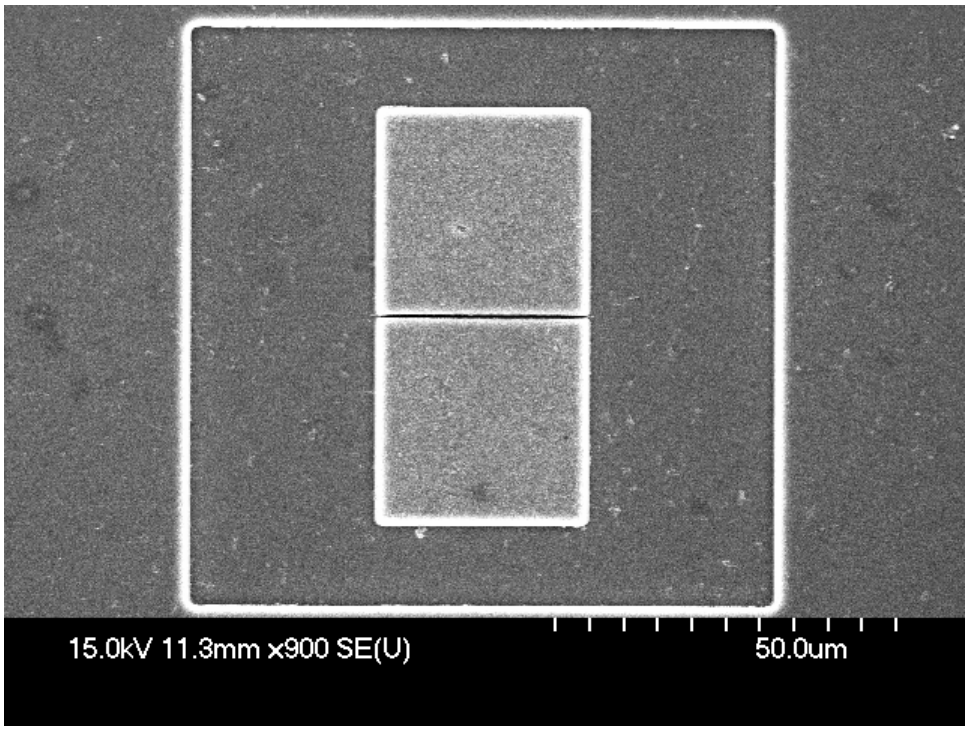


(b_*50k)



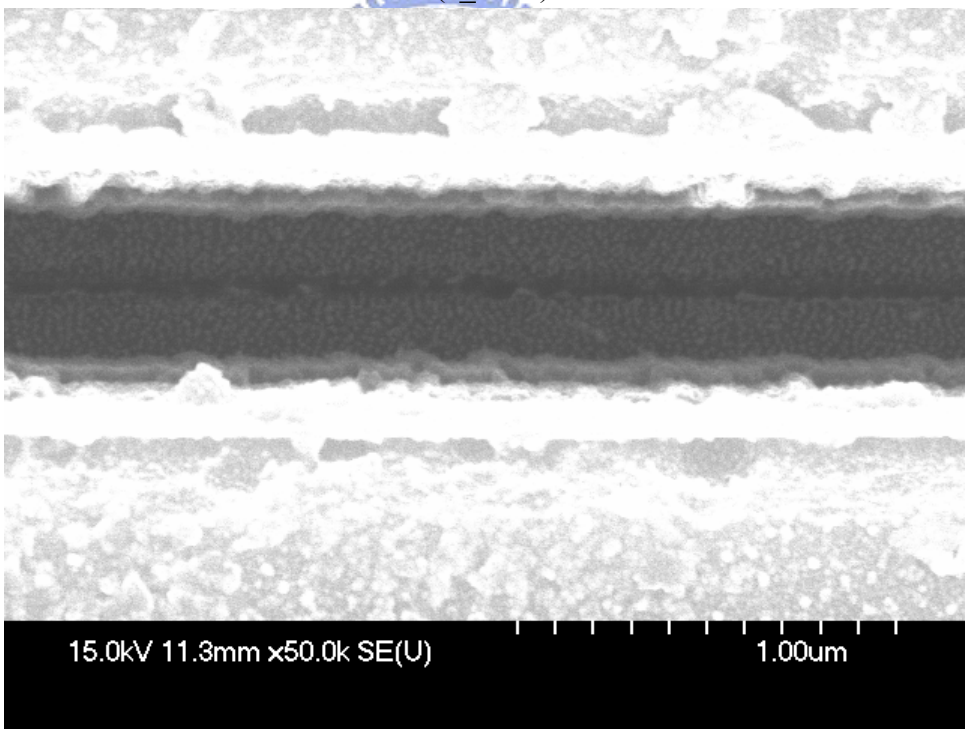
(b_*100k)

Fig. 4.6 The SEM images (with different magnification) of blank electrodes (a) short and (b) wide.

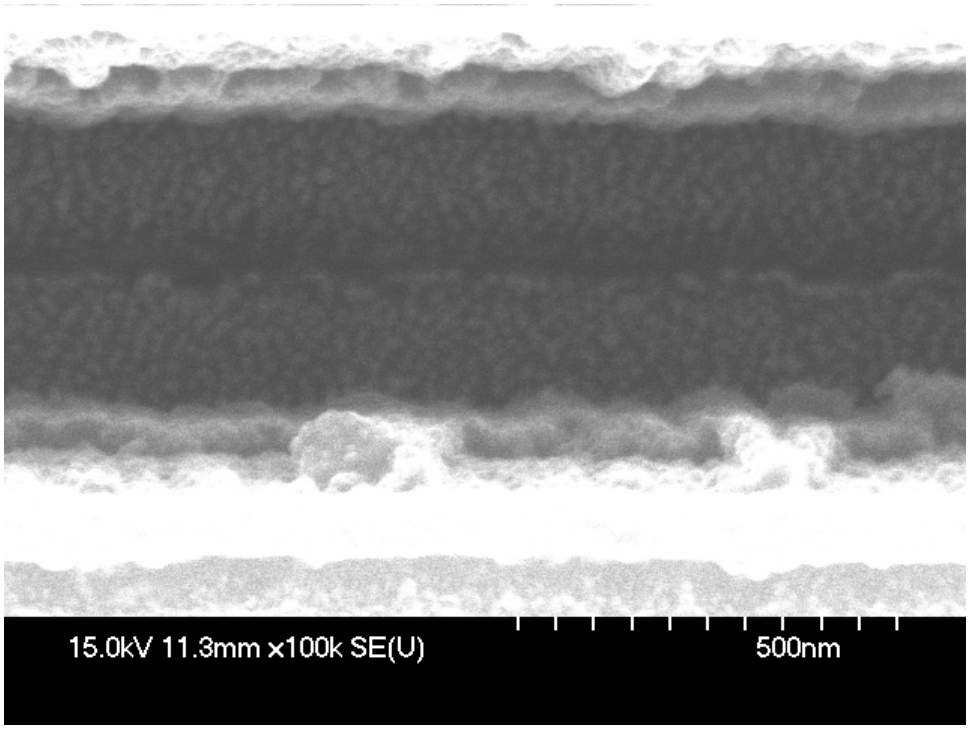


Silicon oxide region between Al electrodes is 30 μm * 0.6 μm

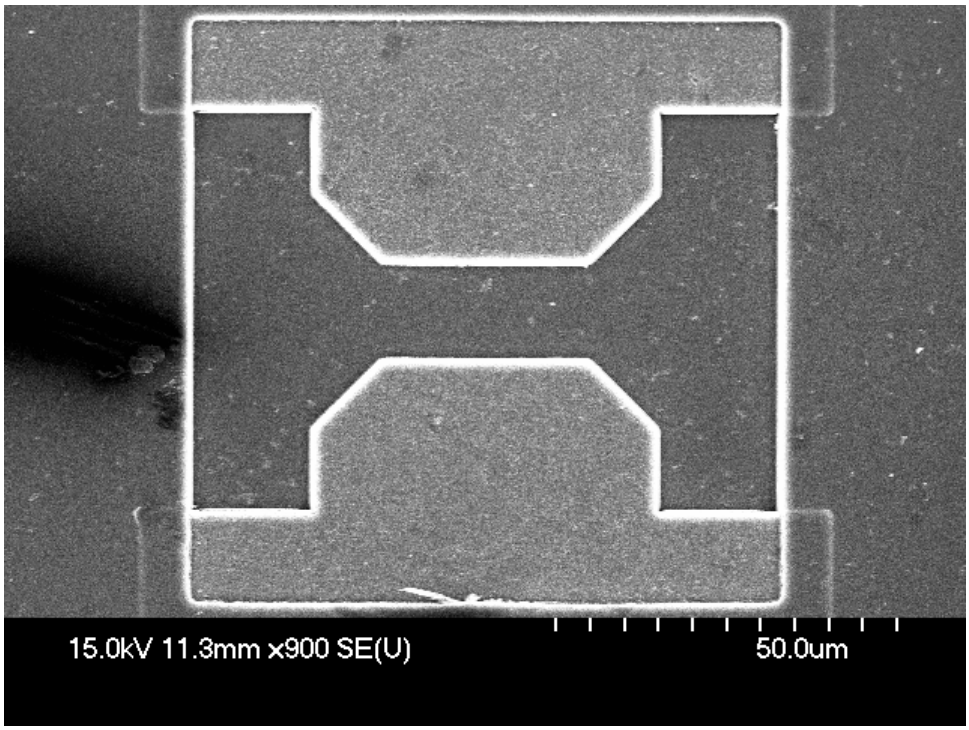
(a_*900)



(a_*50k)

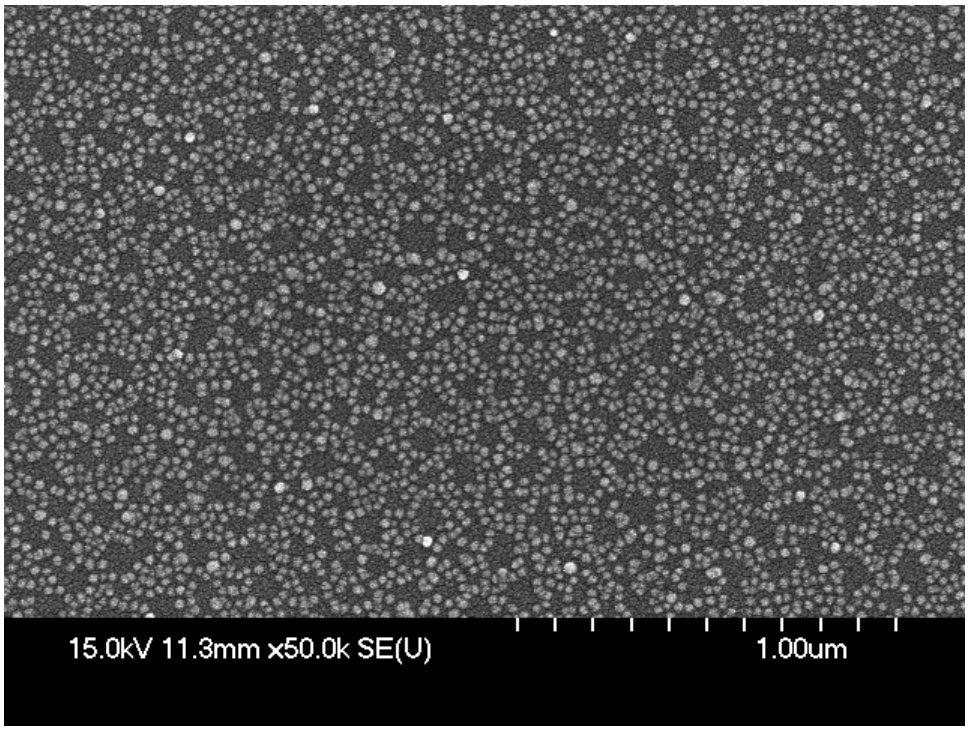


(a_*100k)

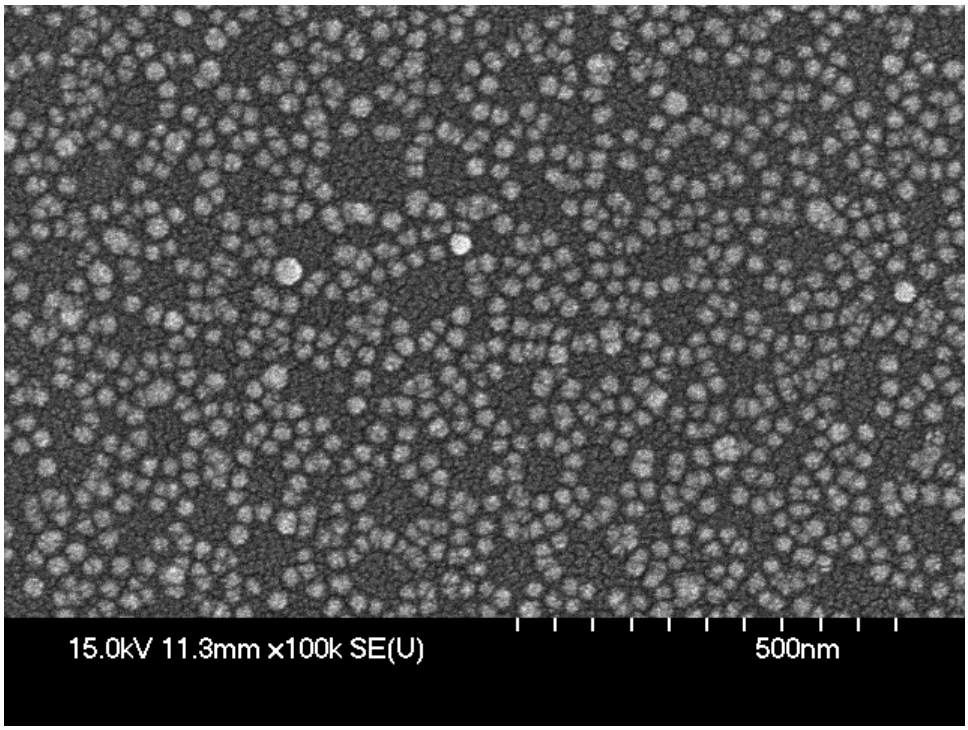


Silicon oxide region between Al electrodes is 30 μm * 15 μm

(b_*900)

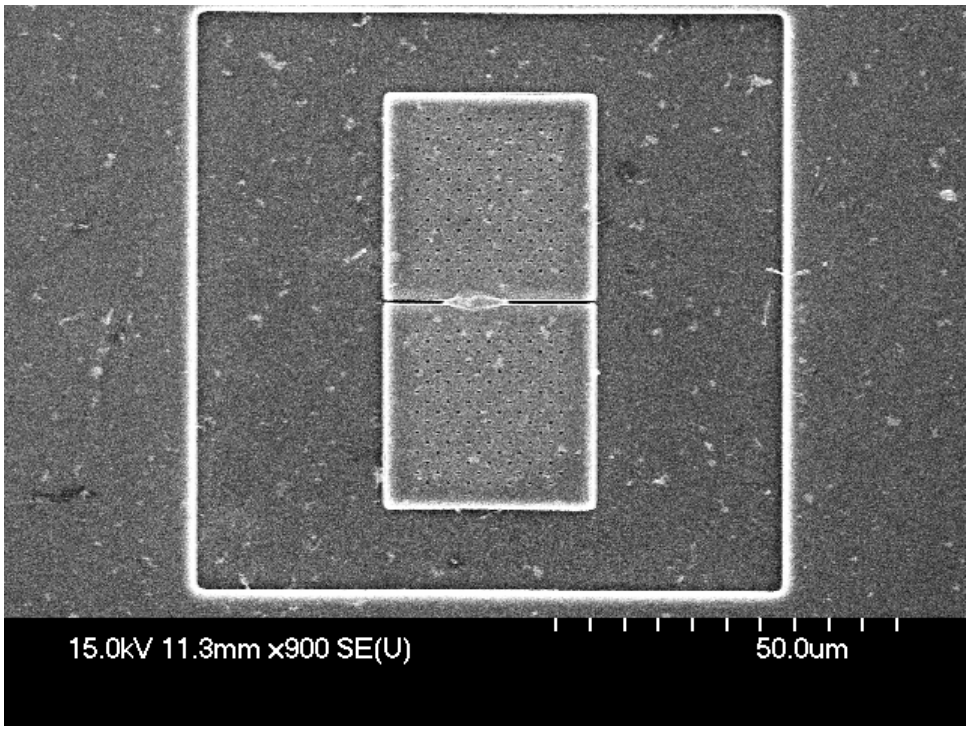


(b_*50k)



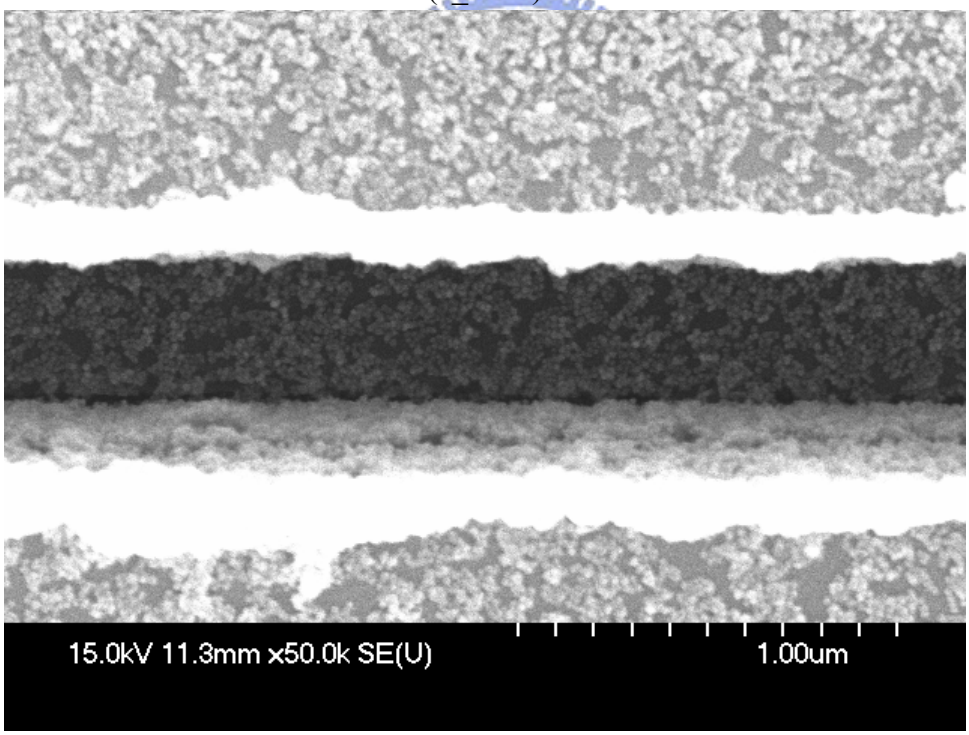
(b_*100k)

Fig. 4.7 The SEM images (with different magnification) of Au NPs modified electrodes (a) short and (b) wide.

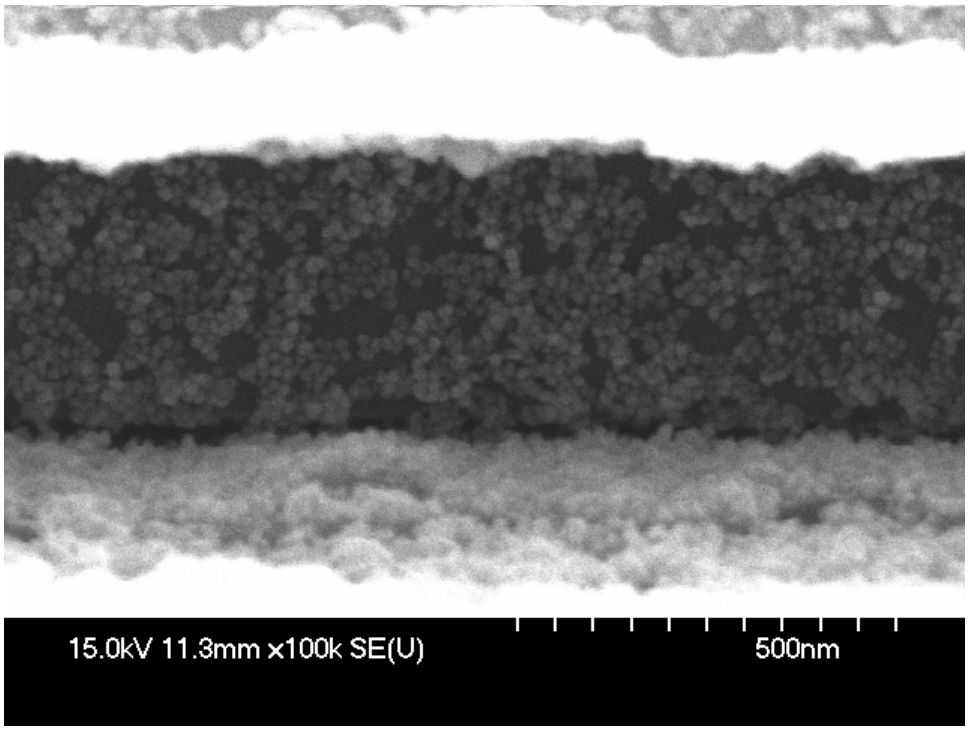


Silicon oxide region between Al electrodes is 30 μm * 0.6 μm

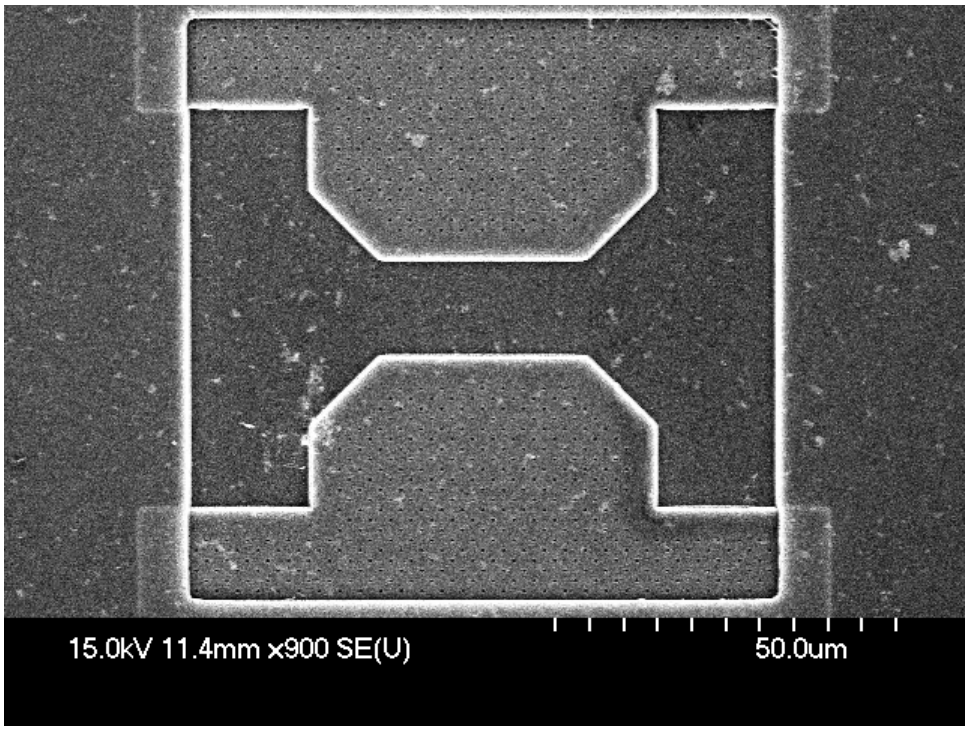
(a_*900)



(a_*50k)

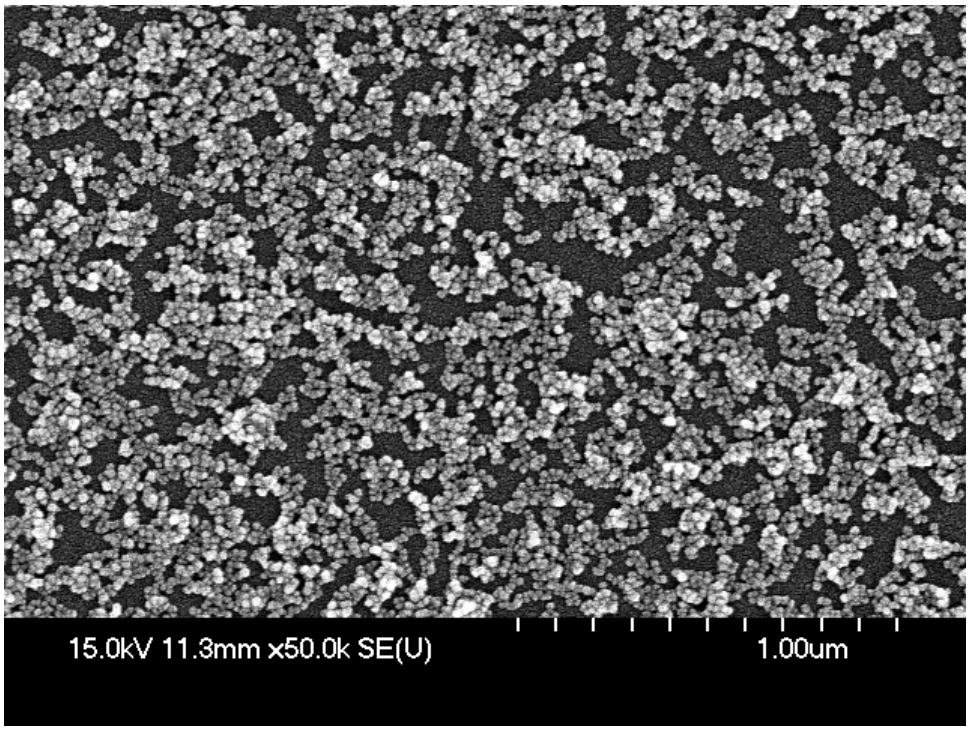


(a_*100k)

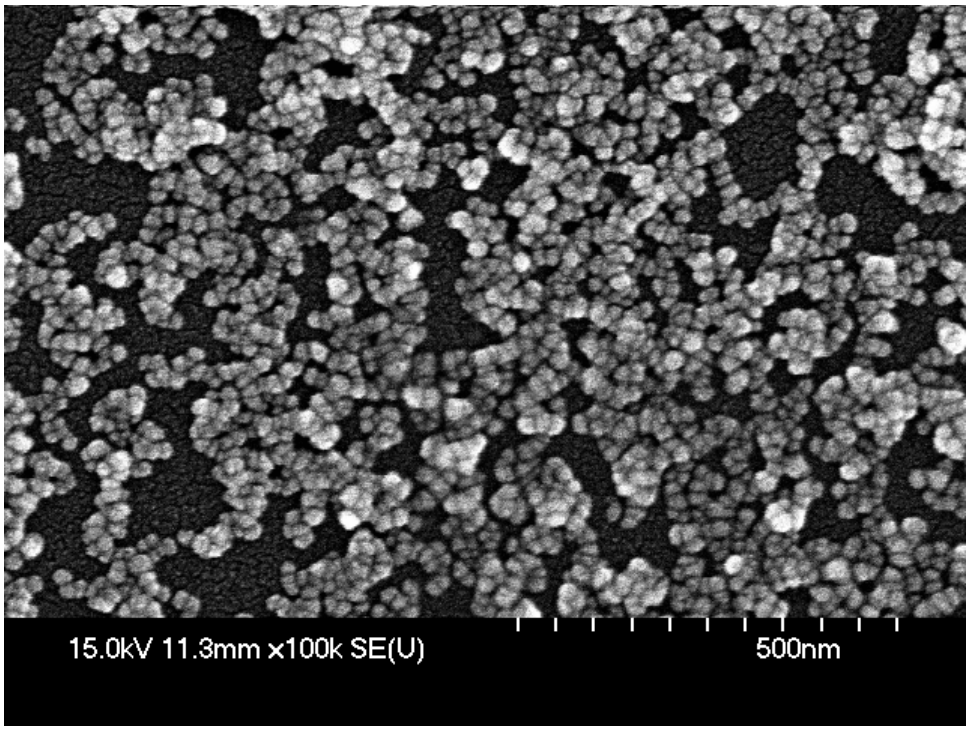


Silicon oxide region between Al electrodes is 30 μm * 15 μm

(b_*900)



(b_*50k)



(b_*100k)

Fig. 4.8 The SEM images (with different magnification) of Au NPs + CdSe NPs + Au NPs modified electrodes (a) short and (b) wide.

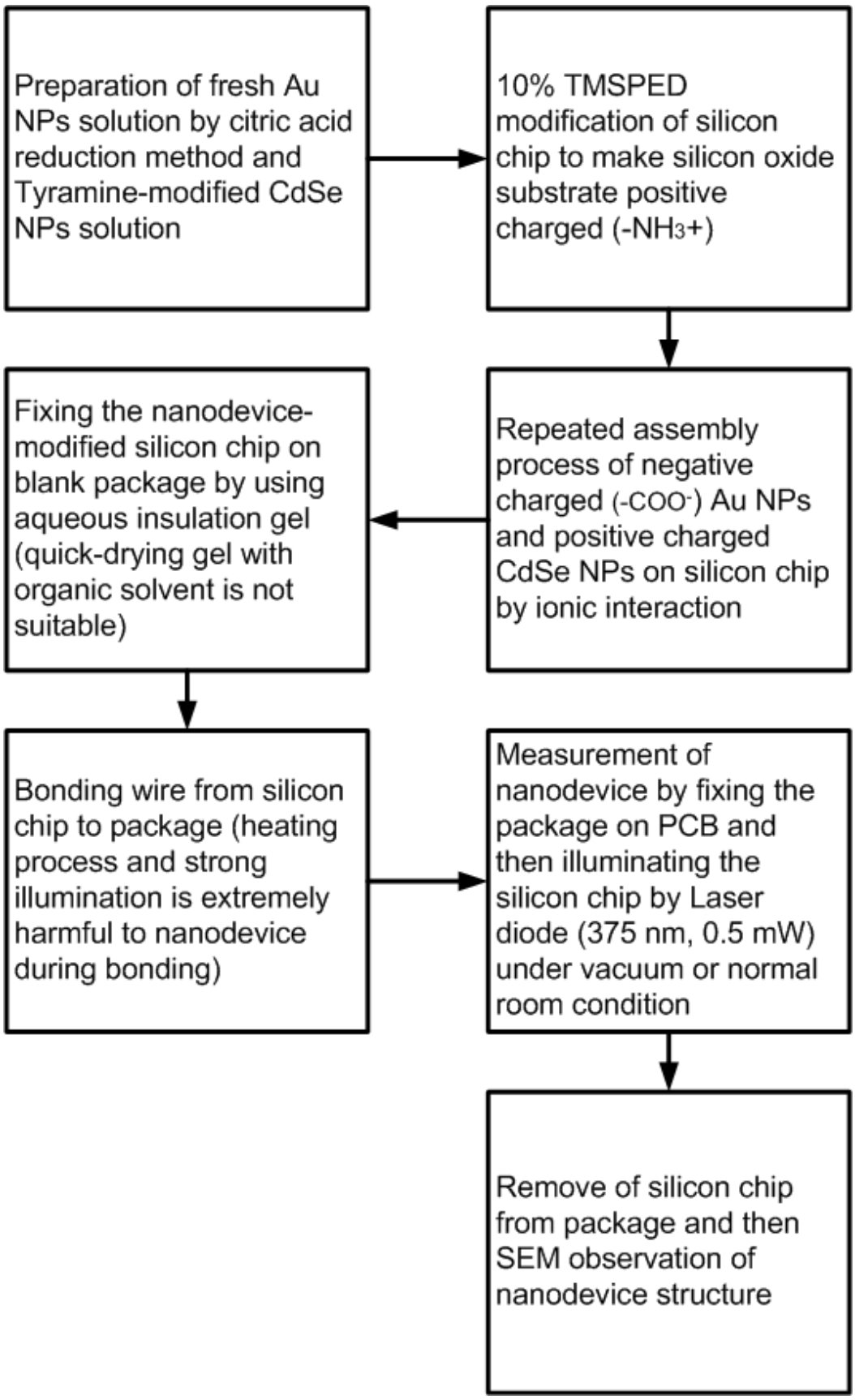


Fig. 4.9 The overall experimental procedure of fabrication and measurement of photo-sensing nanodevice on TSMC 0.35 μm silicon chip is shown above.

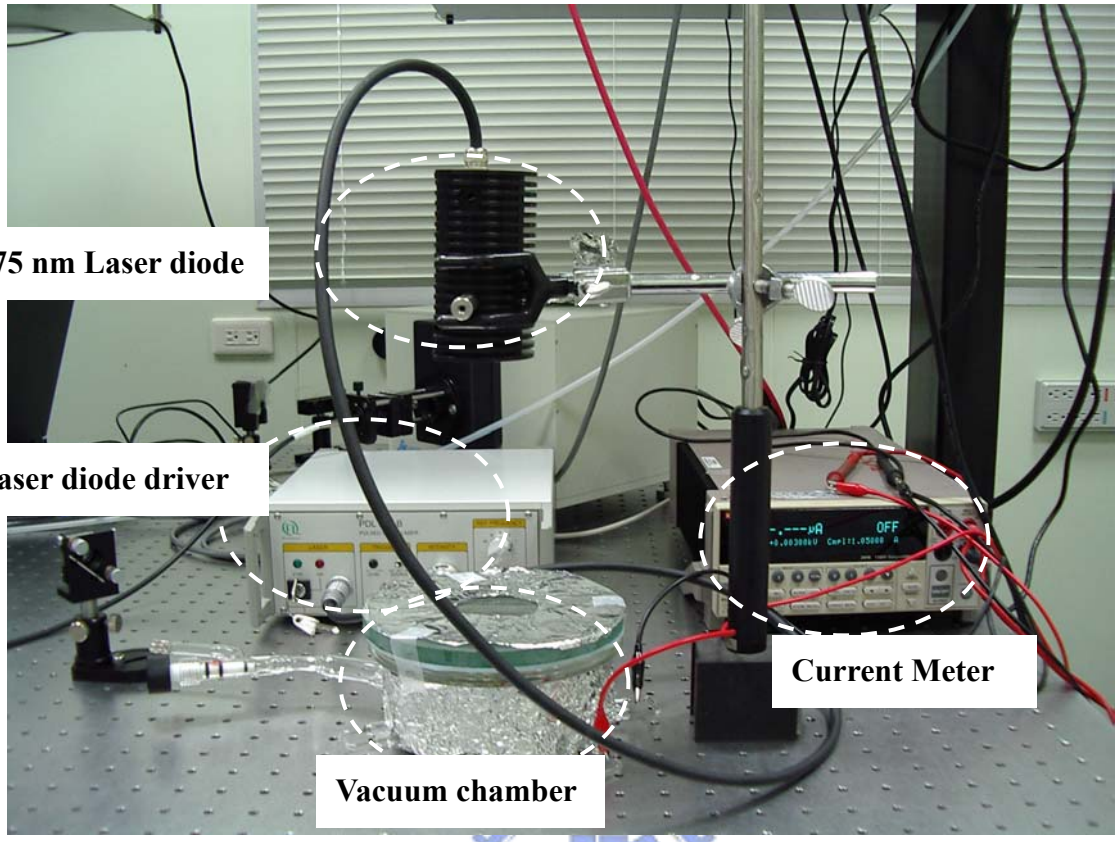


Fig. 4.10 The measurement environment setup.

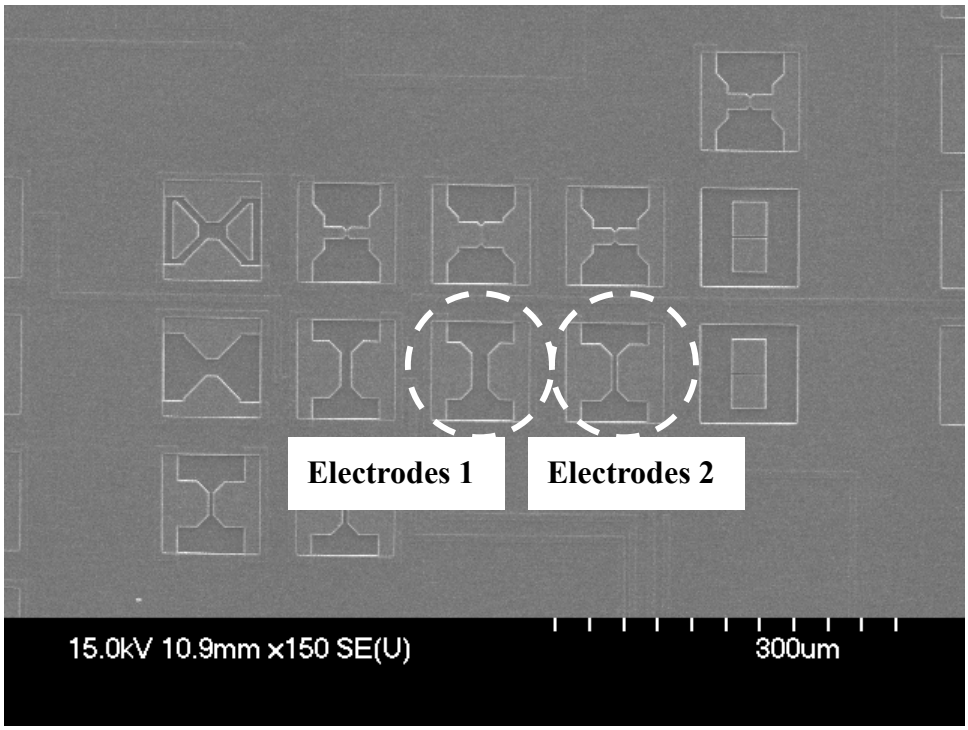
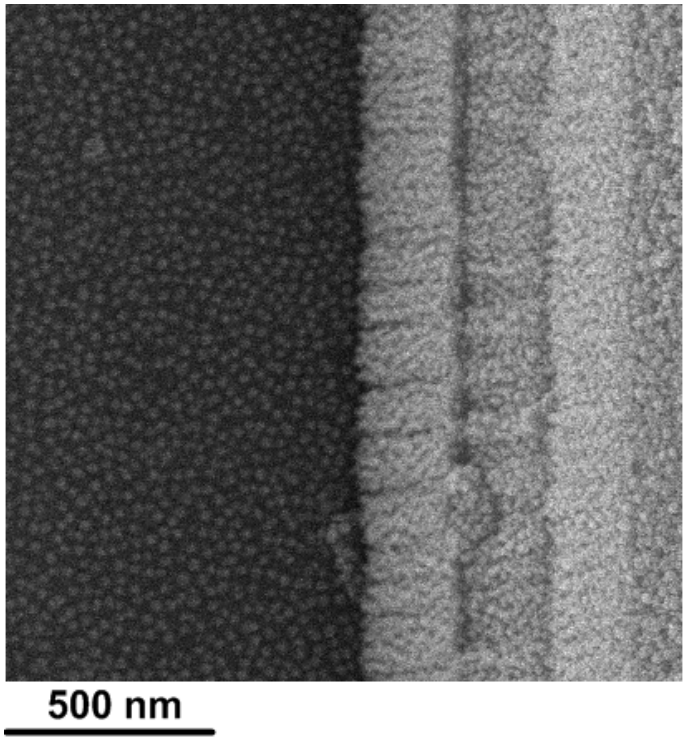
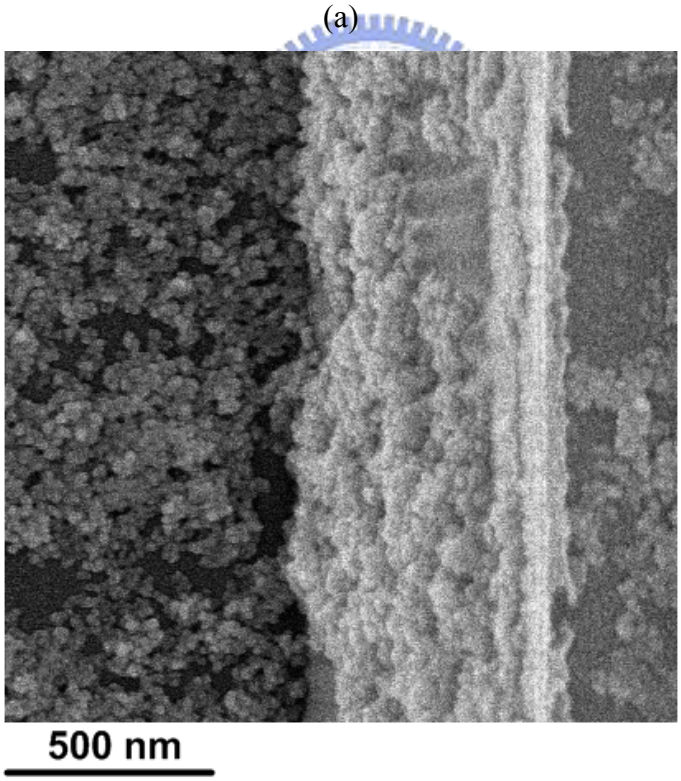


Fig. 4.11 The electrodes under measuring are shown above. Electrodes 1 and 2 have silicon oxide region of 30 μm * 15 μm and 30 μm * 5 μm (width * length) respectively. Both electrodes are connected directly to pads without connection with CMOS sensing circuits.



(a)



(b)

Fig. 4.12 The SEM images of electrodes after labeling Au NPs (a) and after labeling CdSe NPs + Au NPs + CdSe NPs + Au NPs (b) are shown above. The two electrodes in this measurement have the same nanostructure in SEM images due to the same fabrication process. Because the electrodes are too large to be included in the image, we show only the edges parts of electrodes.

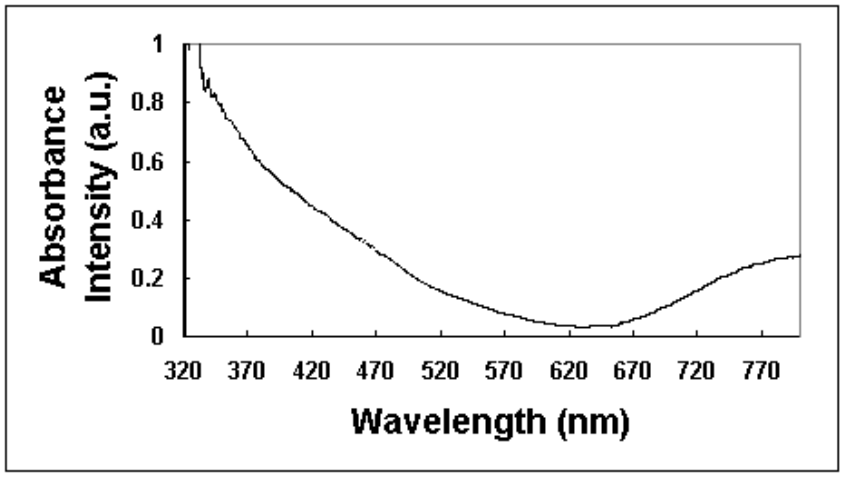
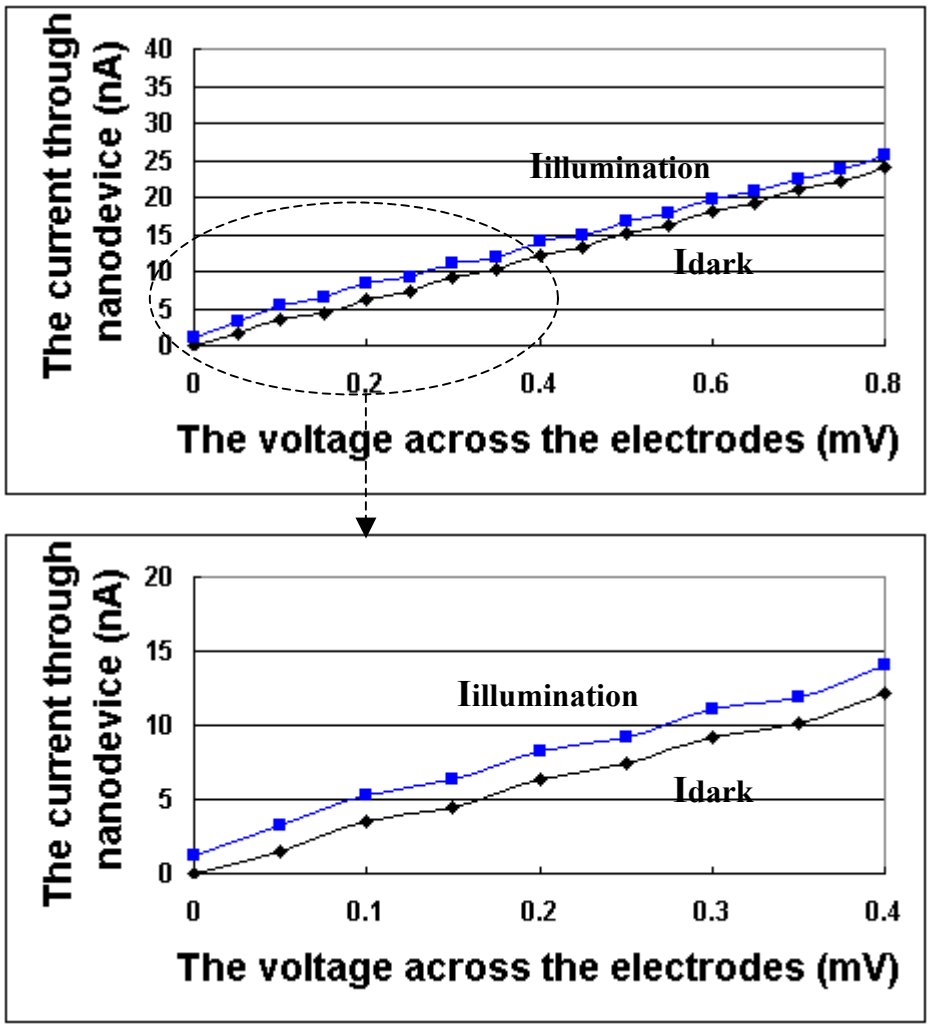
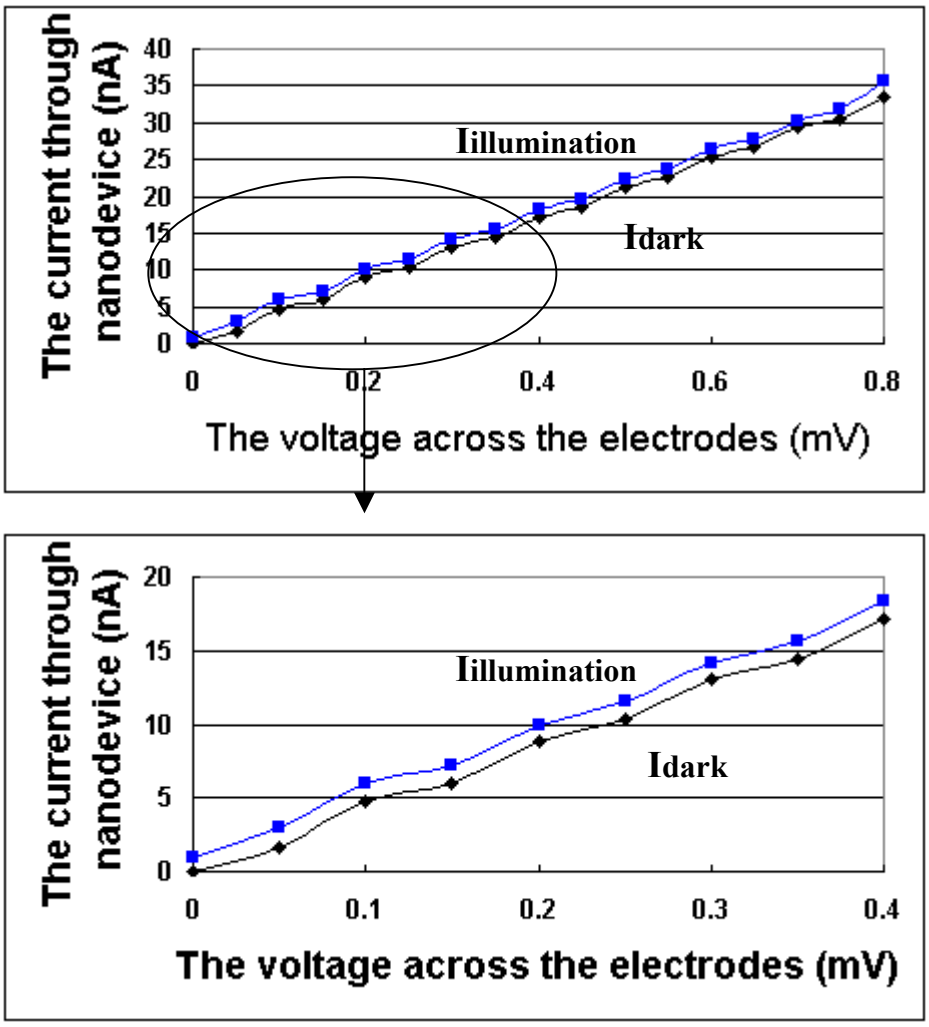


Fig. 4.13 The reflective UV-visible absorbance spectrum of nanodevice with structure CdSe + Au +CdSe + Au NPs on silicon oxide substrate is shown above, where the clean silicon oxide was used as blank.



(a) Electrodes 1



(b) Electrodes 2

Fig. 4.14 The I-V curves of the photo-sensing nanodevice on Electrodes 1 (a) and 2 (b) when in dark or illumination with 375 nm laser diode. The black line (I_{dark}) means the measuring under dark environment and the blue line ($I_{illumination}$) means measuring under illumination of 375 nm laser diode.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUTIONS

In this work, the process to construct photo-sensing nanodevice structure on silicon chip has been presented. We used approximately 5 nm diameter CdSe NPs and approximately 15 nm diameter Au NPs as essential building blocks to form the nanodevice on the silicon oxide substrate between Al electrodes structure on TSMC 0.35 μm silicon chip. To control and assemble CdSe and Au NPs into well-defined nanostructure, we utilized the ionic interaction between CdSe and Au NPs or between NPs and silicon oxide substrate. To achieve this goal, the silicon oxide substrate was first modified by N-[3-(trimethoxysilyl)propyl]-ethylene diamine (TMSPED), which provided concentrated positive charges on silicon oxide substrate after the amino ($-NH_2$) groups were protonated. Then, we synthesized approximately 15 nm diameter Au NPs by the well-known citric acid reduction method. After synthesis, the Au NPs are naturally negative-charged ($-COO^-$) due to citric acids adsorbed on the surface. For CdSe NPs, the original approximately 5 nm diameter HDA-coated CdSe NPs solution was converted to aqueous solution by Tyramine modification, which formed a relatively stable covalent bond between the -OH group of Tyramine and the Cd site of NPs. The Tyramine-modified CdSe NPs are positive ($-NH_3^+$) charged due to the amino group of Tyramine molecule. After preparation of NPs, we sequentially immersed the TMSPED-modified silicon chip into Au and CdSe NPs solution, followed by cleaning process at each step, resulting in closely packed multi-layers structure of CdSe and Au NPs. The process of construction after formation of each layer on silicon oxide substrate was observed by SEM. Finally, the electrical property of photo-sensing nanodevice was observed. We

used two closely separated Al metal lines connected directly to bonding pads as electrodes structure and 375 nm laser diode, that is close to the excitation wavelength of CdSe NPs, as light source to measure the I-V curves of nanodevice on electrodes of different length scale (30 μm * 15 μm and 30 μm * 5 μm). We have demonstrated that the multi-layers structure of CdSe and Au NPs has photo-sensing ability---that is, the enhanced conductivity of nanodevice after illumination. However, the definite mechanism of this phenomenon still needs further research and study.

5.2 FUTURE WORKS

The future works of this project can be divided into two parts---the further research on photo-sensing nanodevice and the development on sensitive and multicolored photo-sensing system based on nanodevice on silicon chip. We will have a brief discussion on these as following.

The further research on photo-sensing nanodevice:

(1) The finding of more efficient method of Tyramine modification and MUA modification on CdSe NPs. The current method of modification based on reflux is too complicated and full of unknown factors that will seriously damage the optical and electrical properties of CdSe NPs. Therefore, it is important to cooperate with Professor Teng-Ming Chen's inorganic synthesis laboratory to develop more efficient methods.

(2) The construction and measurement of different nanostructures based on positive or negative-charged CdSe NPs. In this work, we currently used only positive-charged CdSe NPs, combined with negative-charged Au NPs to form nanostructure. However, it is quite worthy of research on other structures based on negative-charged CdSe NPs.

(3) The understanding of definite mechanism of photoconductivity of nanodevice. So far, we only observed the phenomenon, without confident and clear explanation of the whole mechanism. This part is especially important for further application and can be achieved by only cooperating with others, such as the Femtosecond Laser Spectroscopy of Professor Eric Diau's Femtochemistry Laboratory.

The development of sensitive and multicolored photo-sensing system based on NPs on silicon chip:

In this work, we have developed the construction method on silicon chip and demonstrated the photoconductivity property of the photo-sensing nanodevice. The following works that we Electronics Engineering students can do are to incorporate these inorganic nanodevices into nano-electronics system, like forming arrays of photo-sensing pixels based on NPs, combined with digital controls and analog linear amplifier of extremely small photocurrent. I think this part should be conducted in parallel with *the further research on photo-sensing nanodevice*, because they are actually very closely connected.

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簡　歷

姓　　名：杜長慶

性　　別：男

出生日期：民國 68 年 11 月 26 日

住　　址：台北縣板橋市南雅南路二段 144 巷 7 號 7 樓之 4

學　　歷：

1995 - 1998　台北市立建國高級中學

1998 - 2002　國立交通大學電子工程系

2002 - 2004　國立交通大學電子研究所碩士班

論　　文：

矽晶片上之硒化鎘與金奈米粒子感光元件設計與製程

The Design and Fabrication of Photo-Sensing Nanodevice Composed of CdSe and Au Nanoparticles on Silicon Chip