國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

1Gbps 串列連結收發器

A 1Gbps Serial-Link Transceiver

研 究 生　：　周政賢

指導教授　：　吳錦川　教授

中華民國九十三年五月


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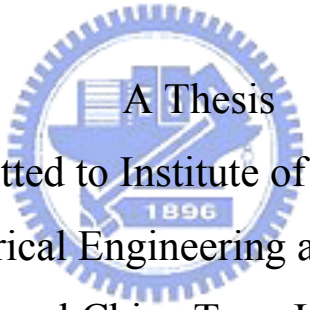

A Thesis

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In

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1Gbps 串列連結收發器

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摘要

隨著積體電路製程技術的進步，對於需要高頻寬和低延遲晶片之間資料傳輸也隨之增加。本論文描述一個高速串列式連結輸入輸出界面之設計。傳輸資料頻率定於 1Gbps。

傳送器使用一個鎖相迴路作為一個時脈電路來提供八個相位給八對一多工器。此鎖相迴路輸入頻率為 31.25MHz，而輸出頻率為 125MHz。平行資料的預先調整相位機制被使用來減少多工器的時脈限制。在多工器和資料驅動器之間的預先驅動器使用主動電感負載來增加頻寬。開汲極電流模式輸出驅動器使用預先加強電路來增加傳送資料位元轉變時期所需的電流源。接收器使用具有磁滯現象的比較器將傳送過來的資料放大成數位訊號。然後，一個操作在輸入資料頻率一半的時脈資料回復電路使用雙追蹤路徑控制機制來達到更好的時脈雜訊表現。最後，解多工器將時脈資料回復電路的輸出轉變成八個平行資料通道。

此傳送器採用0.35μm 2P4M CMOS製程技術實現。當鎖相迴路輸出時脈為125MHz時，量測結果顯示輸出時脈的方均根抖動和峰值抖動分別為11.42ps和82ps。傳送器能正常傳送出1Gbps的串列資料。在電壓電源為3.3V時，總消耗功率為141mW。

A 1Gbps Serial-Link Transceiver

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Abstract

As the IC fabrication technology advances, the need for high-bandwidth and low-latency inter-chip data transfer has also increased. This thesis describes the design of a high-speed serial link I/O interface. The transmission data rate is targeted at 1Gbps.

The transmitter uses a phase-locked loop (PLL) as a timing circuit to provide eight phases for the 8-to-1 multiplexer. The input frequency of the PLL is 31.25MHz and the output frequency is 125MHz. The pre-skew mechanism of the parallel data is used to reduce the timing constrain of the multiplexer. The pre-driver inserted between the multiplexer and the data driver uses active inductive peaking load to enhance the bandwidth. The open-drain current mode data driver uses a pre-emphasis circuit to increase the current during the data transition. The receiver uses the comparator with hysteresis to amplify the incoming data to full swing. Then, the clock and data recovery (CDR) operates at half of the input data rate and uses a dual-tracking path control mechanism to achieve better jitter performance. Finally, the de-multiplexer converts the CDR outputs to eight parallel data channels.

The transmitter is fabricated in a TSMC 0.35μm 2P4M process. The measured RMS and peak-to-peak jitter of the 125MHz output clock of the PLL are 11.42ps and 82ps, respectively. The transmitter transmits 1Gbps serial data normally. Total power consumption is 141mW at 3.3V supply voltage.

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周政賢

國立交通大學

中華民國九十三年五月

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Chapter 1

Introduction

1.1 Motivation

Recently, the advances in IC fabrication technology along with aggressive circuit design have led to an exponential growth of the speed and integration levels of digital IC's. However, these advancements have led to some chips being limited by the chip-to-chip data communication bandwidth. This limitation has motivated research in the area of high-speed links that interconnect chips [1]. Traditionally, system designers have addressed the increasing bandwidth demands by increasing the number of pins and wires interconnecting digital IC's. However, this bandwidth improvement does not come for free. Increased number of pins, printed-circuit-board (PCB) traces, connectors, and cables drive up the overall system cost. In larger scale systems, e.g., multiprocessors or communication switches, a more attractive approach is to use point-to-point links. This approach has advantages both from a circuit design and an architectural point of view. From circuit design perspective, the use of point-to-point transmission lines offers greater flexibility in the physical construction of the

system. Moreover, a point-to-point link has potential for higher communication bandwidth than a bus, due to its reduced signal integrity problems. From an architectural perspective, the bandwidth demands of high-speed systems make the shared bus medium the main performance bottleneck. Therefore, the architecture of most high performance communication switches is inherently based on point-to-point interconnections [2]. The population applications are such as optical communication, back plane interconnection, USB, IEEE1394, and TMDS. Some industrial standards of high speed link are listed in Table. 1-1.

Traditionally, high-speed links in the Gb/s range have been implemented in GaAs or bipolar technologies. The primary advantage provided by those technologies is faster intrinsic device speed (higher f_T). However, despite its slower device speed, CMOS technology is more widely available and allows higher integration than other technologies. With this availability, high-speed links built in CMOS would appeal to large-volume applications that require such high performance links. Furthermore, with higher integration, links could be built as a macro-block in a single-chip system that allows for significant cost savings in these applications.

Table. 1-1 Industrial standards for high speed link

Standard	Speed
IEEE 1394	400Mbps
USB 2.0 (High Speed)	480Mbps
RAM BUS	800Mbps
IEEE 802.3	1Gbps
TMDS (For UXGA)	1.65Gbps
SONET OC-48	2.4883Gbps

The goal of this research is to design a CMOS serial link transceiver with the data rate at 1Gbps.

1.2 Thesis Organization

The thesis is organized into six chapters. The chapter 1 introduces the motivation and the organization of this thesis. Chapter 2 describes the background behind this thesis research. It starts with an overview of a basic high-speed link and brings out signal and clocking methods in designing a high-speed serial link. Chapter 3 covers the design of the transmitter. High speed parallel to serial data conversion is achieved by means of time-division multiplexer toggled by a low jitter and 8-phases phase-locked loop. The pre-emphasis circuits adding to the output driver are realized not only to deal with high frequency attenuation of cable, but also to keep the voltage level at low frequency. Chapter 4 presents building blocks of the clock and data recovery circuit. The architecture with improved jitter performance is proposed. The frequency acquisition part design is also introduced. Chapter 5 shows the experimental results. Chapter 6 concludes this thesis and discusses the future development.

Chapter 2

Background

2.1 Basic Serial Link

A general serial link is composed of three primary components: a transmitter, a channel, and a receiver, as shown in Fig. 2-1. The data before transmission are usually parallel data stream in order to increase the bandwidth of the link. Therefore, a PISO (parallel in serial out) circuit is needed before sending to the transmitter driver. The transmitter converts digital bits into a signal stream that is propagated on the channel to the receiver.

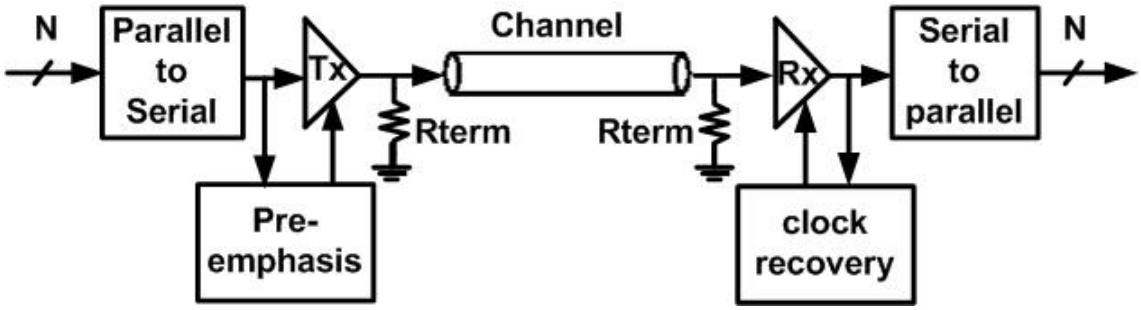


Fig. 2-1 Block diagram of the basic serial link

The channel, on which the signal travels, e.g. coaxial cable or twisted pair, is commonly called the communication channel. In this thesis, The USB cable is used as the serial link channel. The characteristic of USB cable (5m) is shown in Table. 2-1 and Fig. 2-2 [3].

Table. 2-1 Maximum allowable cable loss (5m) [3]

Frequency (MHz)	Attenuation (maximum) dB/cable
0.064	0.08
0.256	0.11
0.512	0.13
0.772	0.15
1.000	0.20
4.000	0.39
8.000	0.57
12.000	0.67
24.000	0.95
48.000	1.35
96.000	1.9
200.00	3.2
400.00	5.8

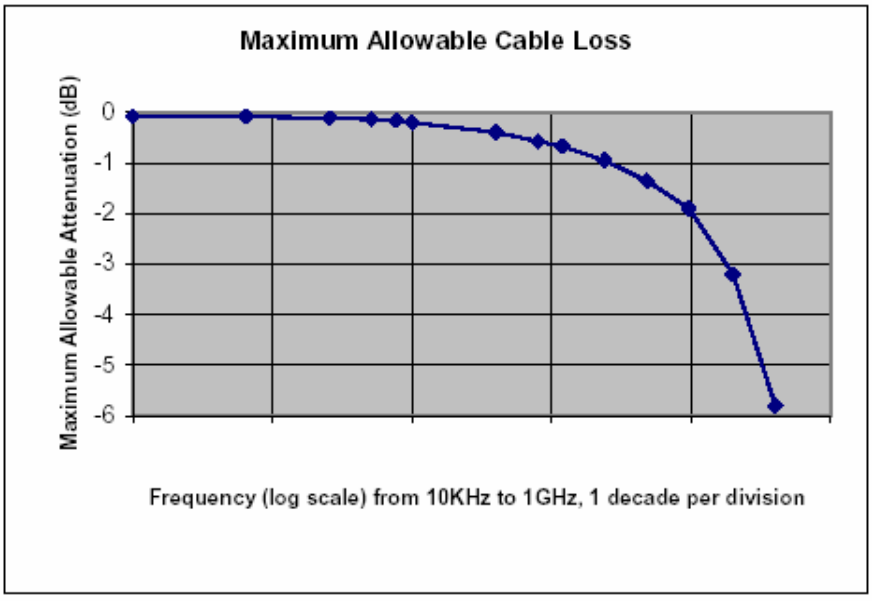


Fig. 2-2 Maximum allowable cable loss (5m) [3]

The Receiver on the other end of the channel recovers the signal to the original digital information by amplifying and sampling the signal. The clock recovery circuit embedded in the receiving side is to adjust the receiver clock based on the receiver data to let the sampling point into the center of the data eye. Then, a SIPO (serial in parallel out) circuit converts the serial data back to N parallel bits. The termination resistors, which match the impedance of the channel, can minimize signal reflection.

The performance of the serial link is mainly characterized by the data bandwidth. Another link performance metric, the bit error rate (BER), measures how many bit errors are made per second. The maximum data rate of the serial link is usually specified at a specific BER to guarantee the robustness of the overall system. BER is important not only because it reduces the effective system bandwidth, but also because in many systems, applying error correction techniques can prohibitively increase the system cost.

The errors are caused by the noises that come from each part of the system. Intrinsic noise sources are the random fluctuations due to the inherent thermal and shot noise of the passive and active system components. However, especially in VLSI applications, other non-fundamental noise sources can limit the link performance. These noise sources include coupling from other channels, switching activity from other circuits integrated with the link circuitry, and reflections induced from channel imperfections. These noise types typically have a non-white frequency spectrum, and exhibit strong data dependencies. Moreover, their overall power is often proportional to the power of the transmitted signals. Therefore, due to the noise consideration, there are two main issues in designing high-speed serial link interference circuit: signaling and clocking. The signaling issue is how to maximize the voltage margins of the interface so that the receiver could have enough voltage margins to recover the data correctly. The clocking issue is how to maximize the timing margins of the interface to transmit and receive data. In many high-speed serial link applications, latency,

power and die area are also critical issues [4].

2.2 Signaling Circuits

The transmitter drives a HIGH or LOW analog voltage onto the channel and is designed for a particular output-voltage swing based on the system specification. The design issues are to maintain small voltage noise and timing noise on the signal. There are two types of output drivers to drive the output: voltage-mode drivers and current-mode drivers. Voltage-mode drivers, as shown in Fig. 2-3 (a), are switches that switch the line voltage. Because the switches are implemented with transistors, the driver appears as a switched resistance. To switch the voltage fully, a small resistance is needed which typically requires a large switching device. In contrast, current-mode drivers, as illustrated in Figure 2-3 (b), are switching current sources. The output impedance of the driver is much higher than the line impedance. It is also called high impedance signaling. Therefore, the transmitter bandwidth is typically not an issue even with significant output capacitance. The voltage to be transmitted on the line is determined by the switched current and the line impedance or an explicit load resistor. The driver can be simply implemented by biasing the MOS transistor in its saturation region. Current-mode drivers are slightly better in terms of insensitivity to supply-power noise because they have high output impedance and hence the signal is tightly coupled only to V_{OH}, the signal return path. The output current does not vary with ground noise as long as the current source bias signal is tightly coupled to the ground signal. The disadvantage with current-mode drivers is that, in order to keep the current sources in saturation, the transmitted voltage range must be well above ground that increases power dissipation.

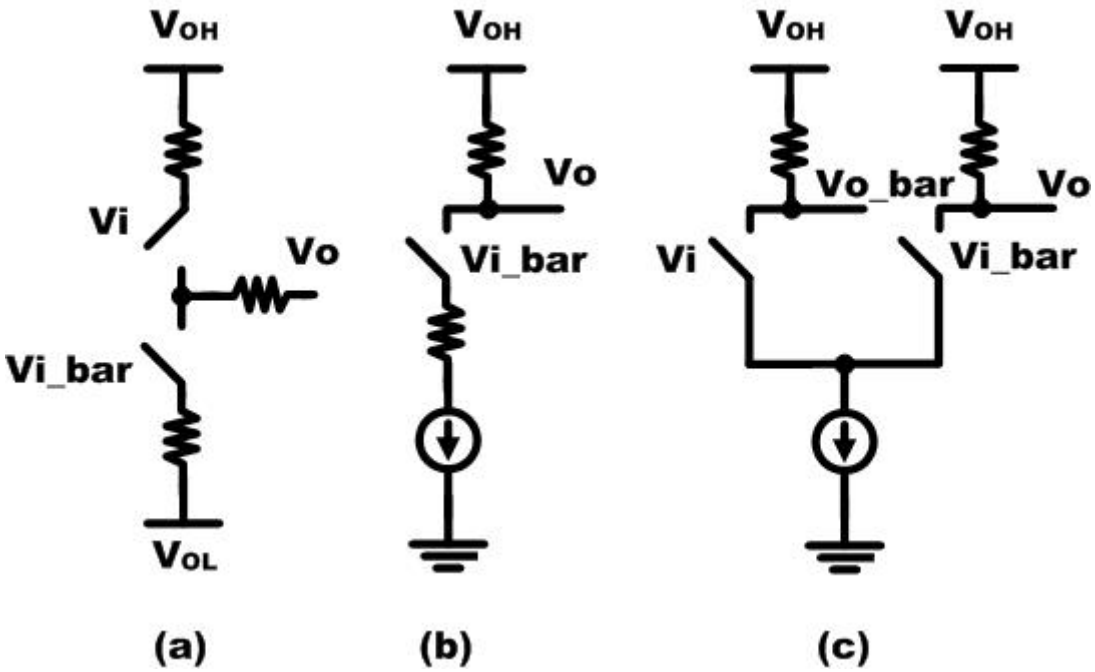


Fig. 2-3 Transmitter with different transmitter architectures: voltage-mode (a), current-mode (b), and differential (c)

For better supply-noise rejection, the differential mode can be adopted, as shown in Fig. 2-3 (c), because the supply noise is now common-mode. Since the current remains roughly constant, the transmitter induces less switching noise on the supply voltage that could benefit other transmitted or received signals on the same die. To reduce reflections at the end of the transmission line, the transmitter needs to be terminated. An off-chip termination resistor could introduce significant impedance mismatches because of the package parasitic components. To incorporate the resistor, with current-mode drivers, an explicit on-chip resistor at the driver can act as the termination resistor. If a resistive layer is not available, a transistor in its linear region can be used as the resistor. With voltage-mode drivers, the design is slightly more complex because the switch resistance should match the line impedance Z_0. This may be done either through proper sizing of the driver or by over-sizing the driver and compensating with an external series resistor, as shown in the Fig. 2-3 (a).

2.3 Timing Circuits

To properly recover the bit sequence, the receiver's sampling clock phases need to have a stable and pre-determined relationship to the phase of the incoming data, thus maximizing the timing margin. The deterministic phase relationship becomes an even more stringent requirement in higher bandwidth systems. In these systems, the bit-rate is a multiple of the on-chip clock, requiring either an explicitly faster bit-clock, or multiple phases of lower frequency clocks with well-controlled phase relationship between them. This clock position must be determined from the phase and frequency of incoming data by the timing recovery circuit. Therefore, a reliable and flexible method for dealing with the synchronization problem is to use on-chip active phase aligning circuits. Generally, these circuits fall in a class of control systems known as Phase-Locked Loops. The sampling clock quality can be characterized by phase offset and jitter. Phase offset is a static (DC) quantity that is equal to the difference between the ideal average position of a clock and the actual average position. Jitter is the dynamic (AC) variation of phase and is dominated by on-chip power-supply and substrate noise. Jitter is specified in terms of both short-term and long-term variations. Cycle-to-cycle jitter describes the short-term uncertainty on the period of a clock, while long-term jitter describes the uncertainty in the position of the clock with respect to the system clock source. In conventional digital design the most important requirement is minimizing cycle-to-cycle jitter. In high-speed links, however, both quantities can be equally important. Low frequency jitter is caused by imperfections on the system clock source and slow temperature and operating voltage variations. This type of jitter can be tracked reasonably well by employing a phase locked loop. Medium frequency and cycle-to-cycle jitter are caused by on-chip supply and substrate noise and are the major concern.

2.4 Timing Recovery Architecture

The task of the timing recovery circuit is to recover the phase and frequency information from the transition in the received data stream. The optimal sample point is midway between the possible data-transition times. Noise and mismatches inherent to the timing recovery circuit produce jitter in the sampling clocks, which degrade the timing margin. Moreover, the transmitter jitter causes uncertainty in the transition points makes clock extraction more difficult. As shown in Fig. 2-4, two types of timing recovery architectures have been used in links. One is the PLL-based (data-recovery PLL) [5] and the other is the oversampling phase-picking [6].

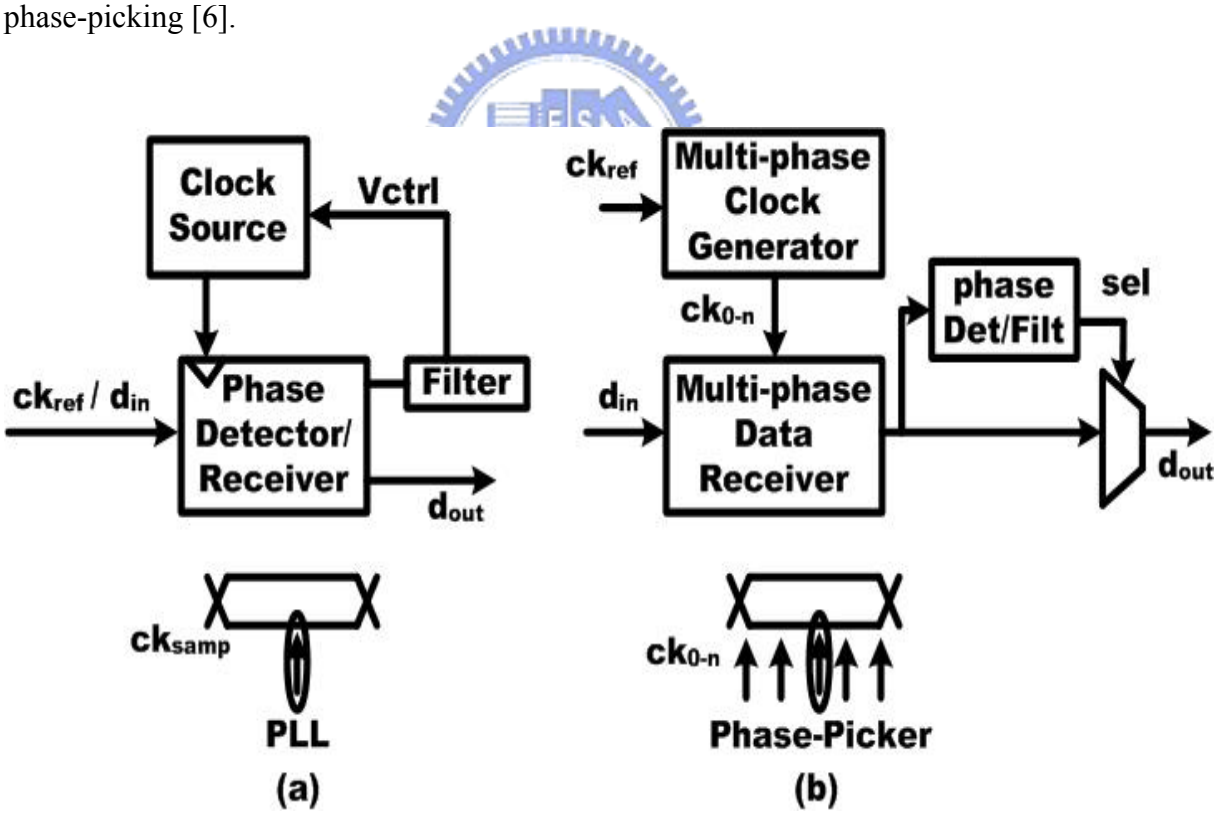


Fig. 2-4 Timing recovery architecture

(a) PLL-based (b) oversampling phase-picking

2.4.1 PLL-based Architecture

In PLL-based architecture, as shown in Fig. 2-4 (a), the negative feedback loop controls the internal phase by adjusting the frequency of the voltage controlled oscillator (VCO) with Vctrl signal until the frequency matches that of an external reference. A phase detector detects the phase difference between the sampling clock and the external input data signal, and adjusts the VCO control voltage. A phase detector generally drives a charge pump that converts the phase difference into a charge. A filtered version of this charge becomes the VCO control voltage. Based on the phase information of the data, the best sample is chosen as the data bit by some decision logic. To maintain good phase relationship between the sampling clock and the data transitions, the PLL should detect the input phase accurately and track any input jitter with a high loop bandwidth. Unfortunately, the stability limits the loop bandwidth of the system. Because the timing information is embedded in the data system, coding of the data is used to ensure a minimum and maximum transition density. High data transition density in the data stream is preferred since it could maintain the stability of the system.

PLL-based timing recovery architectures can be categorized into full-rate and half-rate architectures. In a full-rate circuit the position of the data transition is compared to the falling edge or rising edge of the clock and clock frequency is equal to the data rate as shown in Fig. 2-5 (a). Single edge triggered flip flop can be used to retime the data. On the other hand, the location of the data transition is compared to both rising and falling edges of the clock in a half-rate circuit and the clock frequency is equal to one half of the data rate as shown in Fig. 2-5 (b). Due to the one half of the clock frequency, double edge triggered flip flop is needed to perform the data retiming. The comparison between the two architectures is listed in Table. 2-2 [7] [8].

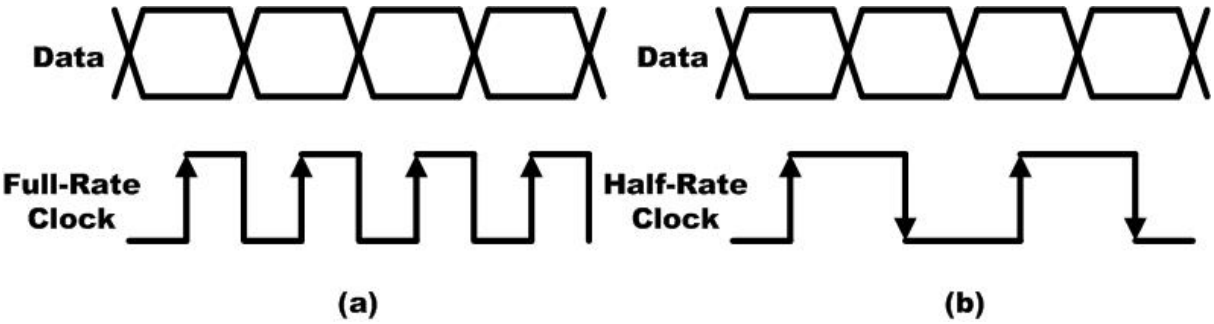


Fig. 2-5 (a) Full-rate data and clock (b) Half-rate data and clock

The most important advantage of half-rate architectures is the reduction of the circuit speed by a factor of two. This often means the reduction of the total power dissipation. In fact, as the operation speed of circuits approaches the maximum operating frequency of a particular technology, the required power consumption grows exponentially. In addition, the de-multiplexing performed simultaneously by half-rate architecture is another attractive feature that makes them suitable for serial link architecture. It can reduce the complexity, hardware, and power dissipation of the deserializer.

Table. 2-2 Comparison between full-rate and half-rate timing recovery architectures

	Full-Rate	Half-Rate
Circuit Operation Speed	Symbol Rate	Half of the Symbol Rate
Number of Clock Phase	Single Clock Phase	Dual Clock Phase
DeMux	None	Can do 1:2 DeMux
Clock Duty Cycle	Not Important	Important
Jitter Tolerance Margin	Larger	Lower due to Clock Mismatch

The duty cycle mismatch is a major concern in employing half-rate timing recovery architecture. If the spacing between the rising and falling edges of the clock signal is different from half to the clock period, the width of the data eye sampled by the rising edge is different from that sampled by the falling edge, resulting in bimodal jitter. So the duty cycle of the clock signal must be considered carefully in the design of half-rate timing recovery architecture.

The Clock and Data Recovery (CDR) architecture presented in this thesis employs half-rate architecture. Although the 0.35μm CMOS technology is fast enough to perform full-rate operation (1GHz), the resulting reduction of power consumption makes the half-rate (500MHz) approach a good candidate.

2.4.2 Oversampling Phase-picking Architecture

The second timing recovery scheme is the oversampling phase-picking as shown in Fig. 2-4 (b). Instead of using feedback loop to control the sampling phases, the data stream is sampled at multiple phase positions per bit creating an oversampling representation of the data stream. It does not require data coding or frequency acquisition since the system clock is readily available through the clock channel. What has to be handled is to adjust the skew between the clock and received data streams. Transitions in the data can be extracted from the sampled data. Based on the data transitions, the sample position nearest the center can be chosen as the data bit. The way to choose data is determined by different digital algorithms, like majority voting [9]. The phase-picking architecture has several advantages. First, it replaces the feedback loop with a feed-forward loop, allowing the selected sample to track

phase movements of the data with respect to the clock without an intrinsic bandwidth limitation. The maximum tracking rate is limited by the transition information present. This fast tracking can potentially track the transmit PLL's jitter accumulation. A second advantage of the phase-picking architecture is that long PLL phase-locking time is not needed. Phase decisions are made whenever input transitions are present. The primary disadvantage of the architecture is that there is an inherent static phase error due to the phase quantization. Higher oversampling ratios could reduces the static phase error but add significant complexity to the design. Furthermore, inherent sampler uncertainty limits the minimum quantization error. More significantly, the increased number of samplers increases the input capacitance, hence limiting the input bandwidth. Therefore, the architecture has a trade-off between the input bandwidths and static phase offsets. For high input bandwidths, the tradeoff favors a low oversampling ratio with the penalty of higher static phase offsets due to the coarse quantization. Besides, due to the open loop mechanism, an error may occurs when sampling point just stands on the data edges, which is not a good position for sampling time, This condition is usually introduced by the static phase error between clock and signal, i.e. the timing skew. However, the feed-forward loop could not offer a mechanism to eliminate the effect of timing skew, which may cause the design complexity of the decision algorithm.

Chapter 3

Transmitter

3.1 Architecture of Transmitter with Pre-emphasis

This chapter presents the transmitter design. The purpose of the transmitter is to drive the signal off chip using electrical quantities with the least power, area and noise based on the channel characteristics. Fig. 3-1 shows the block diagrams of the transmitter architecture.

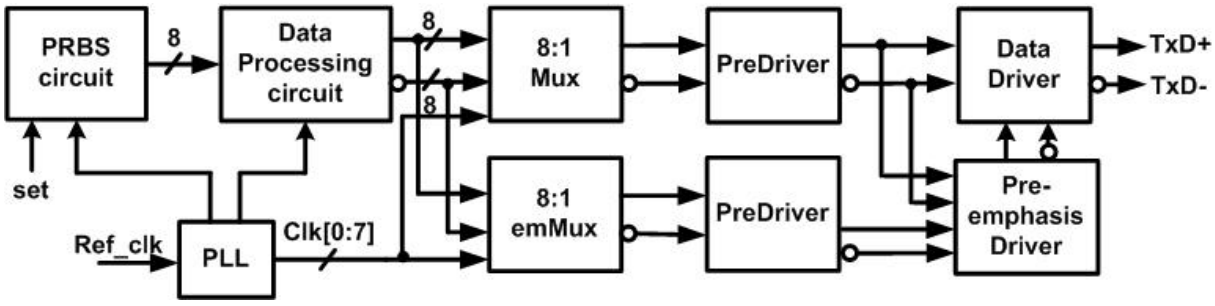


Fig. 3-1 Block diagrams of transmitter with pre-emphasis

The data input is from the PRBS (pseudo random bit sequence). The PRBS is a maximal-length sequence with polynomial $X^7 + X^6 + 1$. The data processing circuit converts the parallel data streams into differential signals and pre-skews the data before feeding them into the multiplexer. The pre-skew of parallel data are shown in Fig. 3-2 [10].

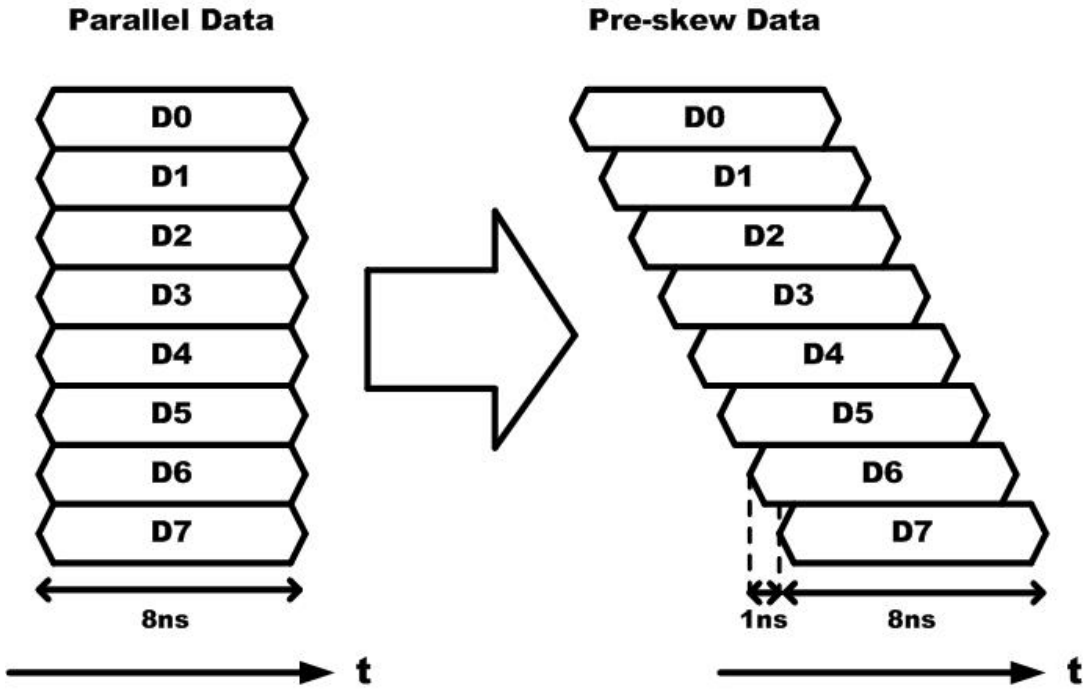


Fig. 3-2 Pre-skew of parallel data

By using 8:1 input-multiplexer to serialize low-speed eight channels parallel data on eight even-spaced phases of 125MHz which gives a bit rate 1Gbps, we can reduce the frequency requirement of the timing circuits and the digital logic. The eight even-spaced phases of frequency 125MHz is given by the PLL. Finally, the serial data are transmitted out through data driver. Furthermore, due to the ISI (Inter-Symbol-Interference) issue which reduced the transmitted signal's timing and voltage margins, a pre-emphasis circuit is applied to the data driver. In the following section, we will describe the detail circuits of the function blocks in the transmitter architecture.

3.2 Phase-Locked Loop

3.2.1 Introduction

Phase-locked loop (PLL) is an important building block used in many aspects including digital, analog and communication applications. For example, it can be used to recover clock from data signals, perform synchronization, frequency synthesizer, and generate multiple phases with equal phase resolution. Recently, as the demand for higher bandwidth data link, the PLL design plays a key part in the link performance. In the transmitter, we introduce the circuit design of a charge-pump type PLL with a reference input clock signal at 31.25MHz and output clock signal at 125MHz. By adopting four differential stages in voltage controlled oscillator, it generates eight clock phases for the use of the eight-to-one multiplexer.

3.2.2 PLL Architecture

A phase-locked loop (PLL) is basically an oscillator whose phase and frequency is locked to those of the input signal. This is done by using a negative feedback control loop, as shown in Fig. 3-3, which includes a phase/frequency detector (PFD), a charge pump circuit (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider (divided by N). The PFD is used to compare the feedback signal (Fback) from the frequency divider with the reference input signal (Fref), and generates the Up and Downb signal to the following charge pump circuit. Based on Up and Downb input signals, the charge pump

begins to charge or discharge the loop filter to change the input control voltage (Vctrl) of the VCO which varies the frequency of the output signal (Clk). The loop filter is basically a low pass filter used to filter out the high frequency component coming from the PFD and charge pump. In this way, the frequency of the feedback signal could be adjusted to be the same with the reference signal through the feedback control loop. In steady state, the frequency of the output signal will be N-times of the input signal. Moreover, the input signal (Fref) and the feedback signal (Fback) are phase-aligned.

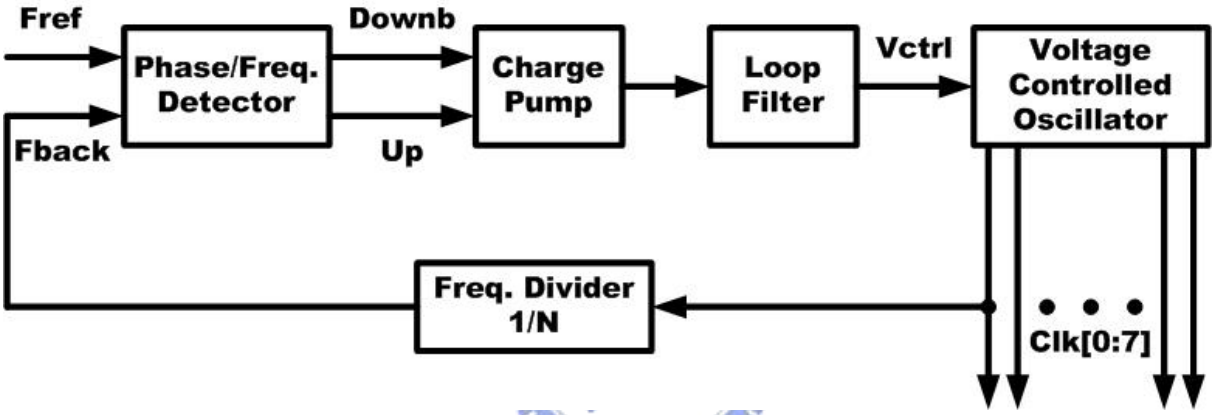


Fig. 3-3 PLL architecture

3.2.3 Circuit Implementation

3.2.3.1 Phase Frequency Detector

The phase frequency detector (PFD) is a digital sequential circuit employs a tri-state operation. It could be implemented simply by two dynamic D flip-flops and one NOR gate, as shown in Fig. 3-4. The TSPC D flip-flop schematic used in PFD is shown in Fig. 3-5 [11].

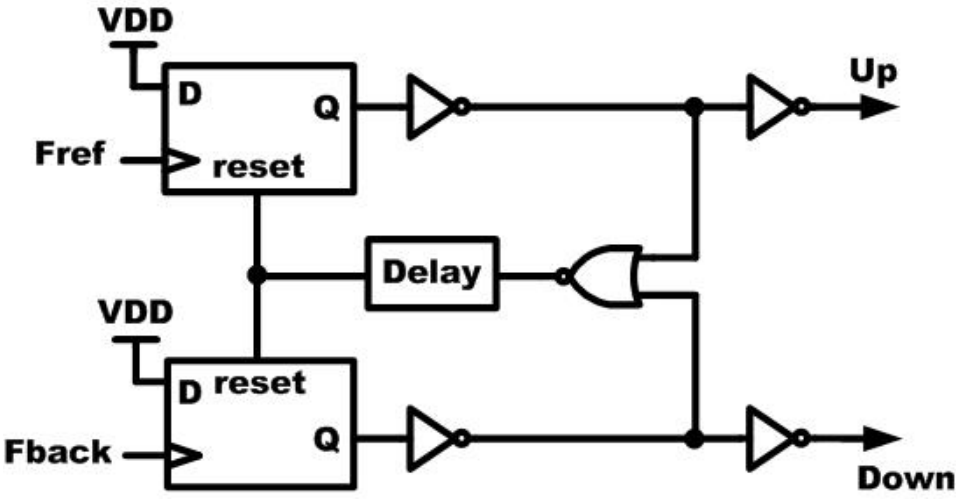


Fig. 3-4 PFD implementation

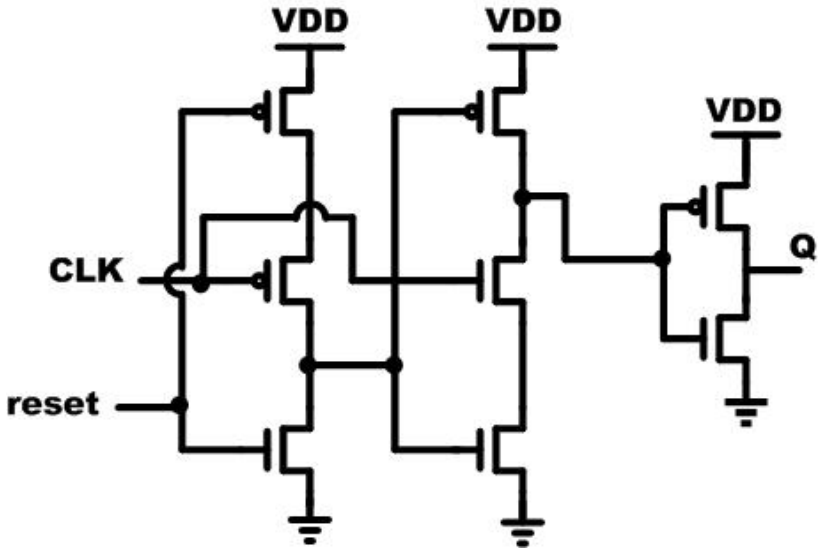
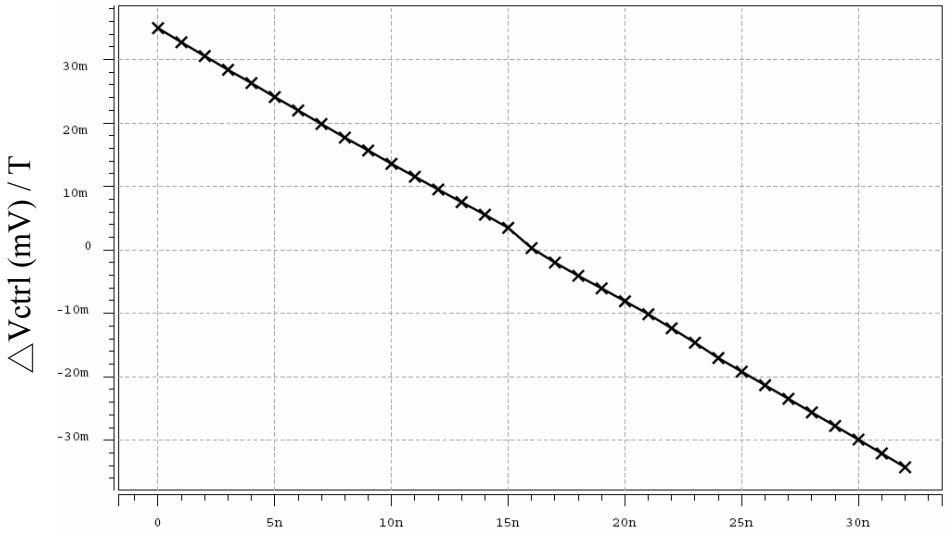


Fig. 3-5 TSPC D flip-flop used in PFD circuit

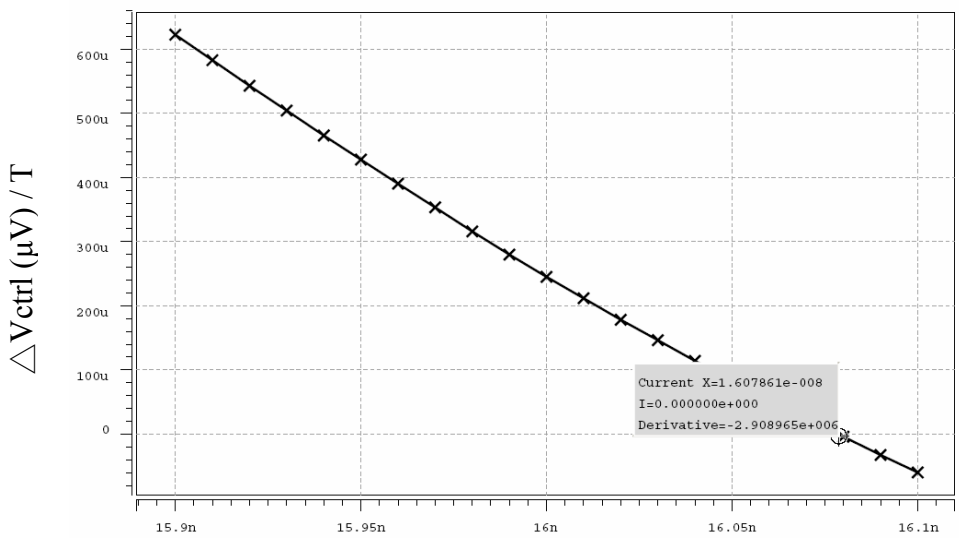
The PFD is triggered by two positive clock edges of the reference (Fref) and the feedback (Fback) signals. If the reference clock leads the feedback clock, the Up signal will be set from low to high. This will in turn increase the frequency of the voltage controlled oscillator output signal. When the feedback signal's rising edge arrives, the reset signal will be high to reset the Up signal to low. In contrast, if the reference clock lags the feedback clock, the Down signal will be set to high, until the reference signal triggers the reset signal. This

Down signal, on the contrary, is used to decrease the frequency of the voltage controlled oscillator output signal. This type of operation has a linear range of $\pm 2\pi$ and can act as both phase detector and frequency detector. This property will greatly enhance the locking range.

Ideally, the PFD should have the ability to distinguish any phase error between reference and feedback signals. In practical, when the phase error is too small, the reset signal is so fast that the following charge pump circuit will not be activated. This will result in dead zone region (undetectable phase difference range). The dead zone is highly undesirable because it allows the VCO to accumulate as much random phase error as the phase difference with respect to the input while receiving no corrective feedback. The dead zone region could be eliminated by adding extra delay cells in the reset path to ensure that when both reference and feedback signals are at the same phase, there would be equal and non-zero Up and Down pulses at the output. The elimination of the dead zone results in overall linear operating characteristics for the PFD, especially for input signals with small but finite phase difference. But inserting the delay cells will limit the maximum operation frequency that is in inverse proportion to the total reset path delay [12].



(a)



(b)

Fig. 3-6 (a) Simulation result of the PFD (b) The enlargement of the simulation result

The simulation results of the PFD, which followed by a charge pump with 150uA and 70pF load capacitor, is shown in Fig. 3-6, where △Vctrl is the voltage change on the load capacitance. Since mismatch exists in Up and Down signal path, the curve shows some offset.

3.2.3.2 Charge Pump

The schematic of the charge pump circuit is shown in Fig. 3-7 [13]. It can charge or discharge the loop filter to vary VCO center frequency according to Up and Downb from PFD. A conventional charge pump circuit has problems such as charge sharing in high impedance state, charge injection, and clock feedthrough. Charge injection is produced by the overlap capacitance of the switch devices and the capacitance at the intermediate node between the current source and switch devices. This charge injection will result in a phase offset at the input of the PFD when the PLL is locked. To eliminate the charge injection problem, the two

switch devices are separated from the output voltage. Therefore, the output voltage is now isolated from the switching noise resulting from the overlap capacitance of the two switch devices. In addition, the intermediate node between the current source and switch devices will charge to the output voltage only by the gate overdrive of the current source devices, Vgs – Vt, an amount independent of the output voltage. Moreover, since both the NMOS and PMOS current sources always turn on in each cycle, any charge injection will cancel out to first order with equal current source device sizes.

The matching between charge and discharge current is improved by balancing the loading on the charge pump control signals, Up and Downb. This is accomplished by the dummy current source path whose control signals are Upb and Down.

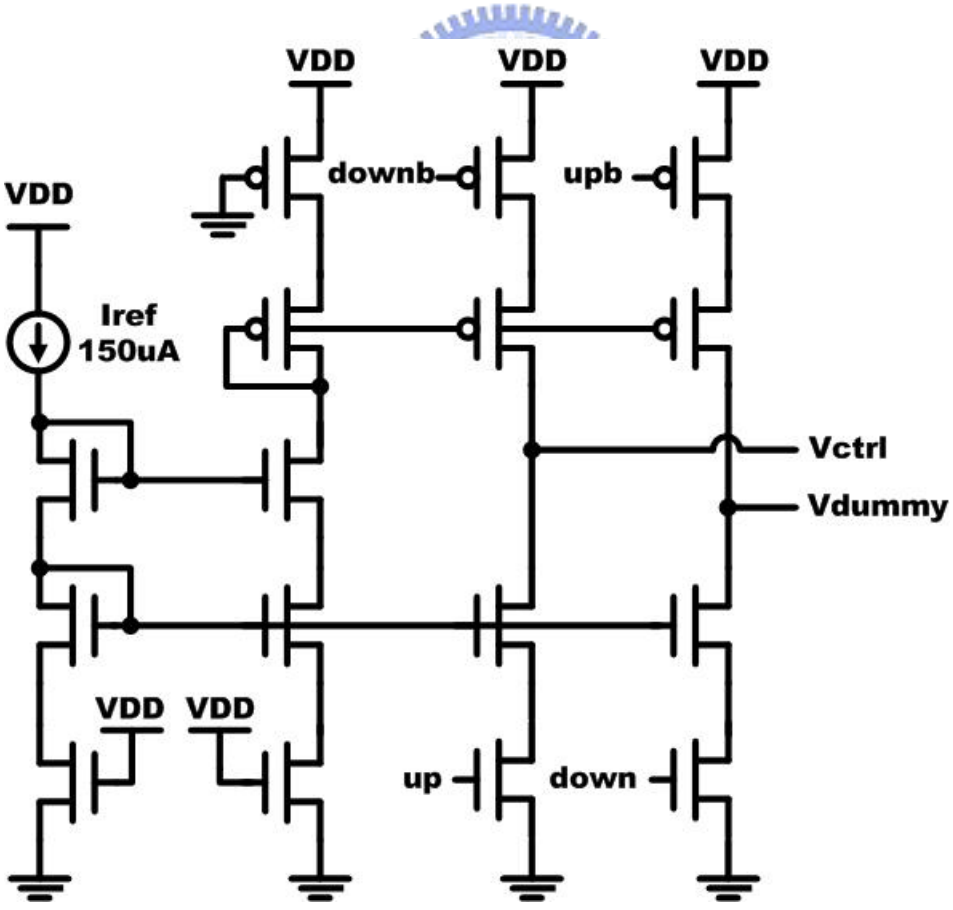


Fig. 3-7 Schematic of the charge pump

3.2.3.3 Loop Filter

A second-order on chip loop filter is designed to suppress the reference spurs. The loop filter is a low pass filter that is used to extract the average value from the PFD output. As shown in Fig. 3-8, it is composed of a resistor R_1 in series with capacitor C_1 and a capacitor C_2 in parallel.

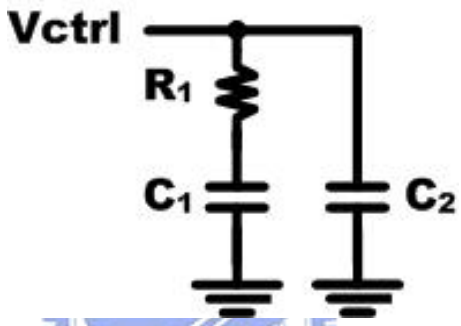


Fig. 3-8 Schematic of the loop filter

The loop filter provides a pole in the original to provide an infinite DC gain to get the zero static phase error, and a zero in the open loop response in order to improve the phase margin to ensure overall stability of the loop. Capacitance C_2 is used to provide higher-order roll off for reducing the ripple noise to mitigate frequency jump. The total transfer function of the loop filter can be expressed as

$$F(s)=\frac{1}{C_1+C_2}\frac{sR_1C_1+1}{s\left[\left(sR_1C_1C_2/C_1+C_2\right)+1\right]} \tag{3-1}$$

and hence

$$F(s)=\frac{Kh\times(S+\omega_z)}{S\times(1+S/\omega_P)} \tag{3-2}$$

where

$$\omega_z = 1/R_1C_1\,,\quad \omega_P = \omega_z \times (1 + C_1/C_2)\,,\quad Kh = \frac{R_1 \times C_1}{C_1 + C_2}$$

But the adding of the capacitance C_2 will make the overall PLL system become third-order one and affect the stability of the loop. In general, by setting C_1>20×C_2, the third-order can be approximated to second-order loop.

3.2.3.4 Voltage Controlled Oscillator

The building blocks of the VCO include a four stages ring oscillator and a self-biased replica-feedback bias generator [14] [15]. Fig. 3-9 shows the schematic of the four stages VCO and the delay cell.

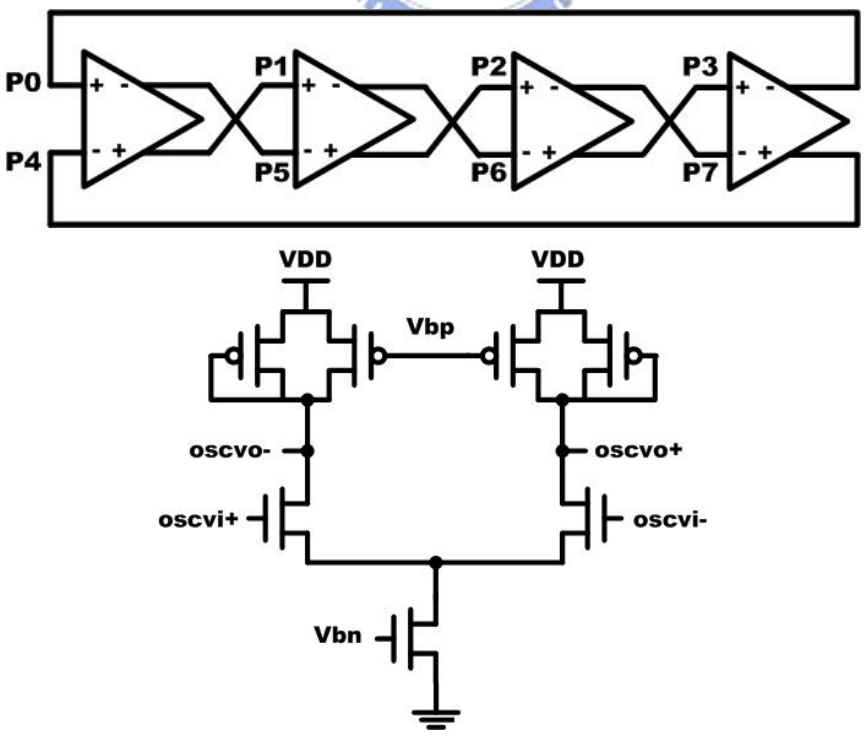


Fig. 3-9 Schematic of the four stages VCO and the delay cell

In order to have the low jitter characteristics of the output clock, the delay cell used in voltage controlled oscillator (VCO) should have low sensitivity and high noise rejection capability of the supply and substrate voltage. The supply noise can be categorized into static and dynamic noise. The architecture of the VCO used in this thesis can greatly improved the static and dynamic supply noise [16].

The delay cell of the VCO contains a source-coupled pair with diode-connected PMOS devices as resistive loads in shunt with an equally sized PMOS device. They are called symmetric loads because their I-V curve is symmetric about the center of the voltage swing, as shown in Fig. 3-10.

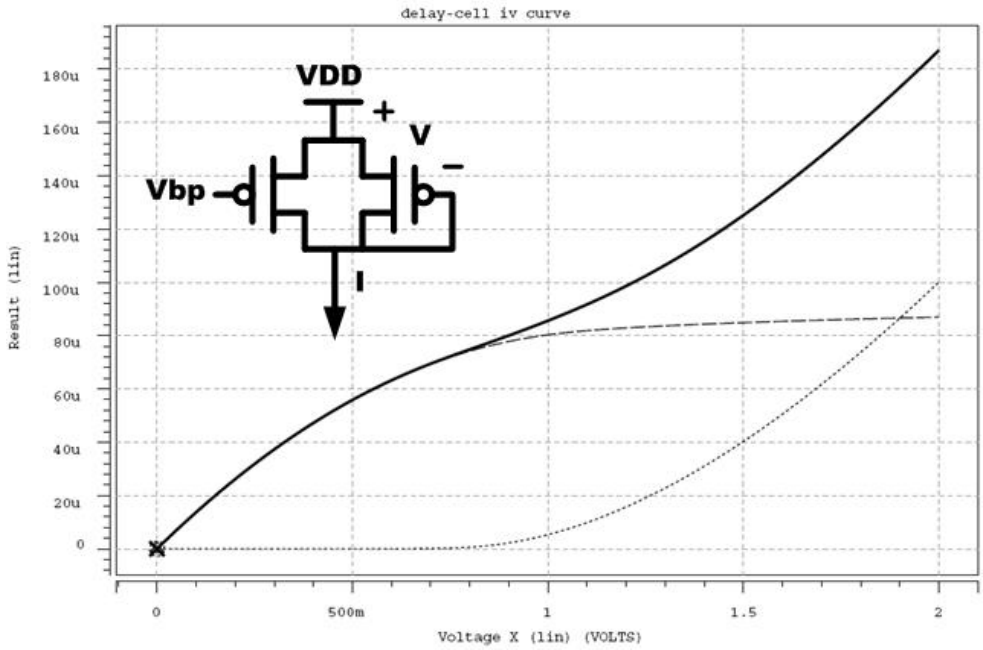


Fig. 3-10 I-V curve of the symmetric load

Basically, to get the high noise rejection capability over the supply and substrate noise, the load of the differential pair should have a linear I-V characteristic. In practice, this is difficult to use MOS device to achieve it. But the symmetric load can cancel the first order of the common mode voltage noise. Therefore, the symmetric load here, though nonlinear, could

be used to have high dynamic supply noise immunity. The control voltage, Vbp, is the bias voltage for the PMOS device. In order to provide a bias current that is independent of the static supply noise, the bias voltage of the NMOS current source, Vbn, will be continuously adjusted. As the supply voltage changes, the drain voltage of the NMOS current source also changes. However, the gate bias is adjusted by the replica-feedback bias generator to keep the output current constant. It seems that it makes the output resistance of the NMOS current source higher. Hence the static supply noise is greatly improved.

Based on the analysis of the I-V curve, it can be shown that the effective resistance of a symmetric load (R_{eff}) is directly proportional to the small signal resistance at the ends of the swing range which is just one over the transconductance (gm) for one of the two equally sized PMOS biased at Vctrl. Therefore, the buffer delay is

$$t_d = R_{eff} C_{eff} = \frac{1}{g_m} C_{eff} \tag{3-3}$$

where C_{eff} is the effective buffer output capacitance. The drain current for one of the two equally sized devices biased at Vctrl is

$$I_d = \frac{kp}{2}\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right]^2 \tag{3-4}$$

Taking derivative with respect to Vctrl, the transconductance gm is given by

$$g_m = kp\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right] \tag{3-5}$$

The buffer delay is then given by

$$t_d = \frac{C_{eff}}{kp\left[\left(V_{DD} - V_{ctrl}\right) - \left|Vtp\right|\right]} \tag{3-6}$$

Thus, for N stages of the VCO, the oscillator frequency is given by

$$f_{osc} = \frac{1}{2Nt_d} = \frac{kp\left[(V_{DD} - V_{ctrl}) - |Vtp|\right]}{2NC_{eff}} \tag{3-7}$$

The gain of the VCO is given by

$$K_{vco} = \frac{df_{osc}}{dV_{ctrl}} = \frac{-kp}{2NC_{eff}} \tag{3-8}$$

As a result, Kvco is independent of the buffer bias current and the VCO has first order tuning linearity.

The self-biased replica-feedback bias generator of the VCO delay cell is shown in Fig. 3-11. It provides the output bias voltage Vbp and Vbn from input signal Vctrl. The primary function is to continuously adjust the VCO delay buffer bias current to provide the correct lower swing limit Vctrl for the VCO delay buffer stages. As a result, it builds up a current that is held constant and independent of supply voltage.

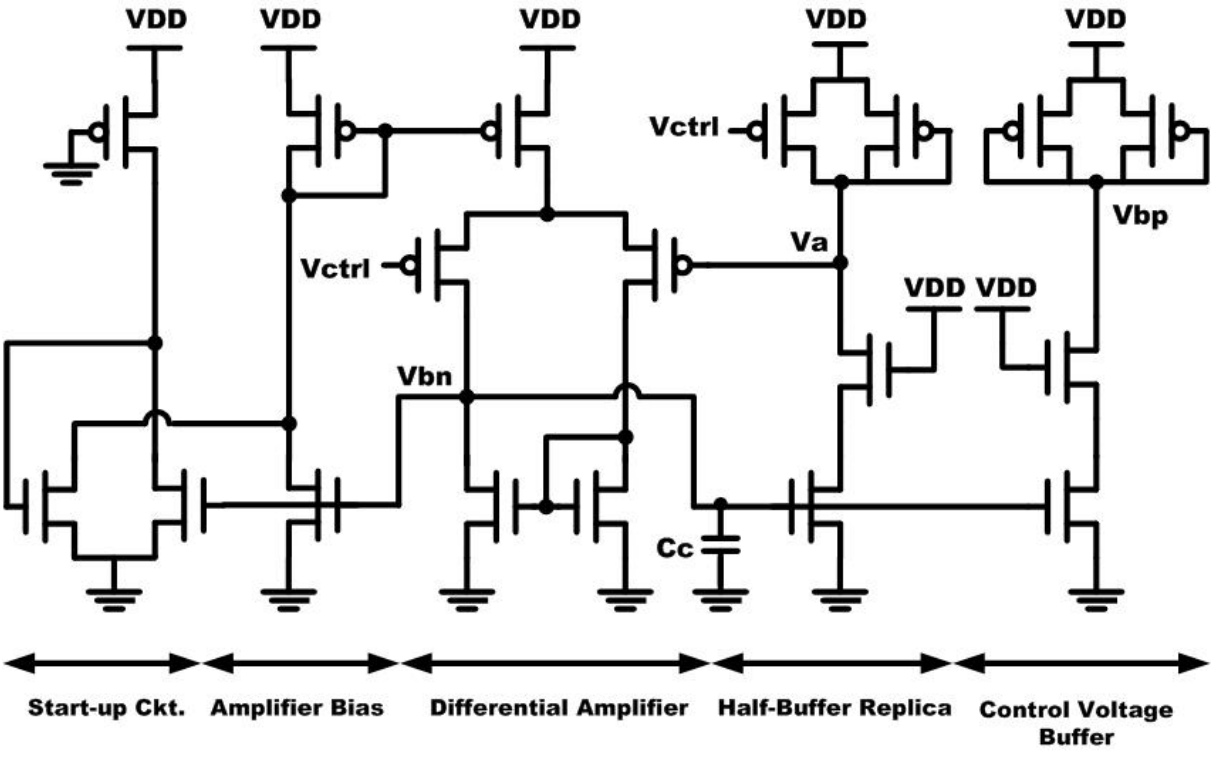


Fig. 3-11 Schematic of self-biased replica-feedback bias generator

The self-biased replica-feedback bias generator consists of a PMOS source coupled differential pair, a half-buffer replica, and a control voltage buffer. The differential amplifier is actually a unity-gain buffer which forces the voltage of node Va in Fig. 3-11 equal to Vctrl, a condition required for correct symmetric load swing limits, and provide the bias voltage Vbn for the NMOS current source. Besides, the bias voltage, Vbn, is dynamically adjusted by the differential amplifier to increase the supply noise immunity. With the half-buffer replica, the net result is that the output current of the NMOS current source is established by the load element and is independent of the supply voltage. If the supply voltage changes, the amplifier will adjust to keep the swing and the bias current constant. Because the differential amplifier utilizes the self-biased architecture, there are two stable states, one of which is unbiased. As a result, a start-up circuit is needed to bias the amplifier when power-up.

Because the differential amplifier and the half-buffer replica form a two-stage negative feedback loop, frequency response issue must be taken into consideration. Fig.3-12 shows the frequency response of the self-biased replica-feedback bias generator.

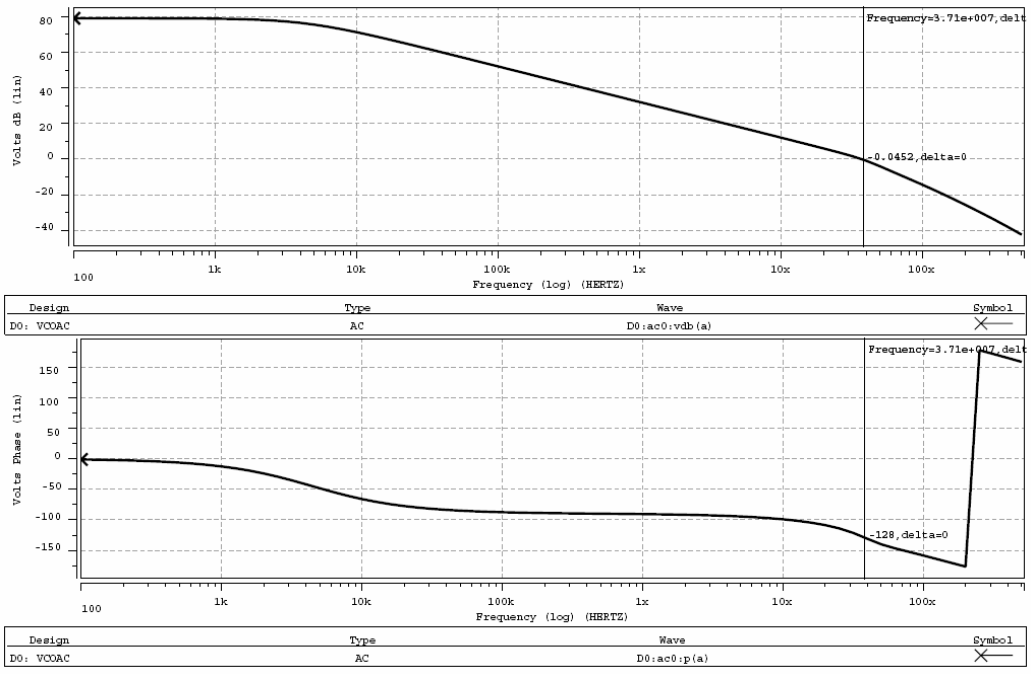


Fig. 3-12 Frequency response of the self-biased replica-feedback bias generator

Basically, there are two poles in the loop. One is at amplifier output, and the other is at the half-buffer replica output. Since the pole at the amplifier output is the dominant one, it can be moved toward origin to increase the phase margin of the loop by the capacitive load Cc of the NMOS current source gates in the VCO buffer chain. Moreover, in order to track any supply and substrate noise that affect the VCO jitter performance, the bandwidth of the self-biased circuit is usually set equal to the operation frequency of the VCO. The bias circuit also provides a buffered version of control voltage Vctrl using an extra control voltage buffer. This can isolate the control voltage Vctrl from capacitive coupling in the VCO buffer chain.

The differential oscillator output is converted to the 50% duty cycle single-ended signal used as input to the phase-frequency detector with the differential-to-single-ended converter shown in Fig. 3-13 [15] and the feed forward type duty-cycle corrector shown in Fig. 3-14 [11]. The two differential amplifiers of the differential-to-single-ended converter use the same current source bias voltage, Vbn, generated by the self-biased replica-feedback bias generator for the VCO. According to Vbn, the circuit corrects the input common-mode voltage level and provides signal amplification.

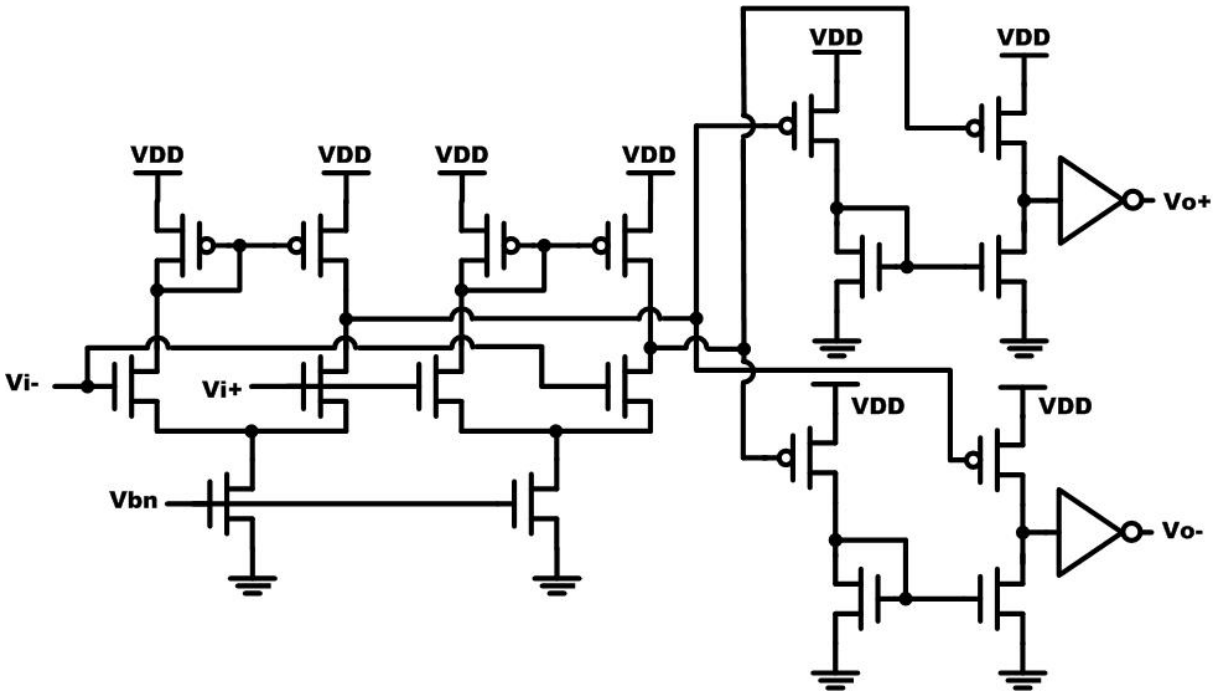


Fig. 3-13 Schematic of differential-to-single-ended converter

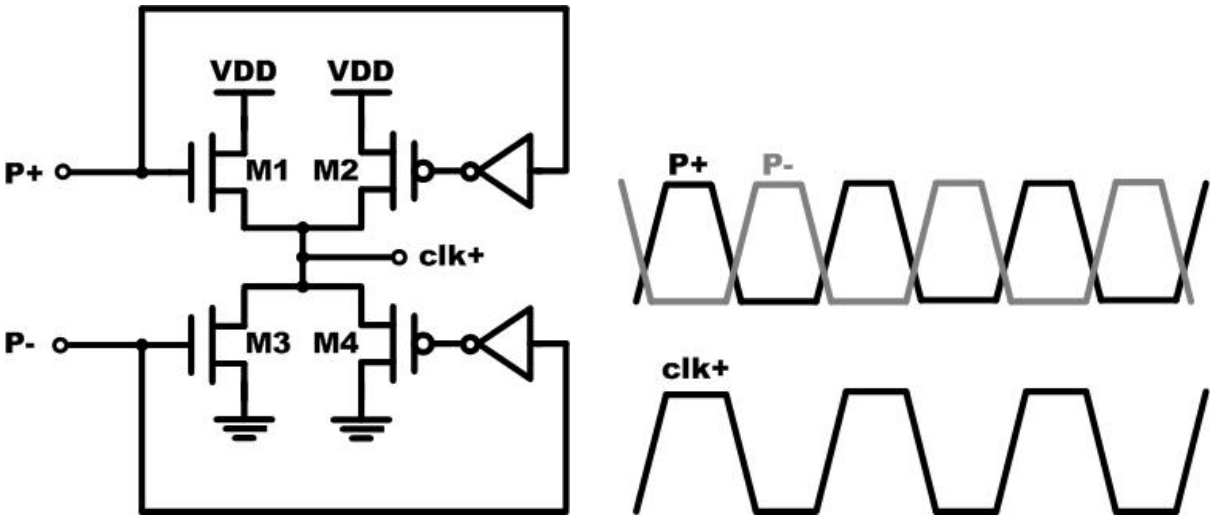


Fig. 3-14 Schematic of feed forward type duty-cycle corrector and its timing diagram

The duty-cycle corrector is connected behind the differential-to-single-ended converter to ensure that the duty-cycle of the VCO will be 50%. The signal P+ selected from the multiphase signals turn on M1 and M2, and charges the output node clk+ of the duty-cycle corrector almost instantaneously. Because the discharge path of the node clk+ is already off due to the signal P-. The signal P-, which is also selected from the multiphase signals, is the one whose rising edge is shifted by 180° in phase from that of P+. Similarly, the signal P- rapidly discharges the node clk+ and delivers the desired 50% duty-cycle signal. Since this duty-cycle correction circuit consists of only two transmission gates and two inverters, the area is minimal and the power consumption is negligible. In order to drive next stages, digital buffers are added at the output to improve the driving ability.

The PLL used in this thesis needs to generate eight phases for the transmitter multiplexer. Therefore, the VCO uses four delay buffer stages with the output frequency at 125MHz. The transfer curve simulation result of the VCO is shown in Fig. 3-15. The supply voltage is 3.3V. For Vctrl between 0.5V to 2.2V, the gain of the VCO is -118.5MHz. And the transfer curve is monotonic.

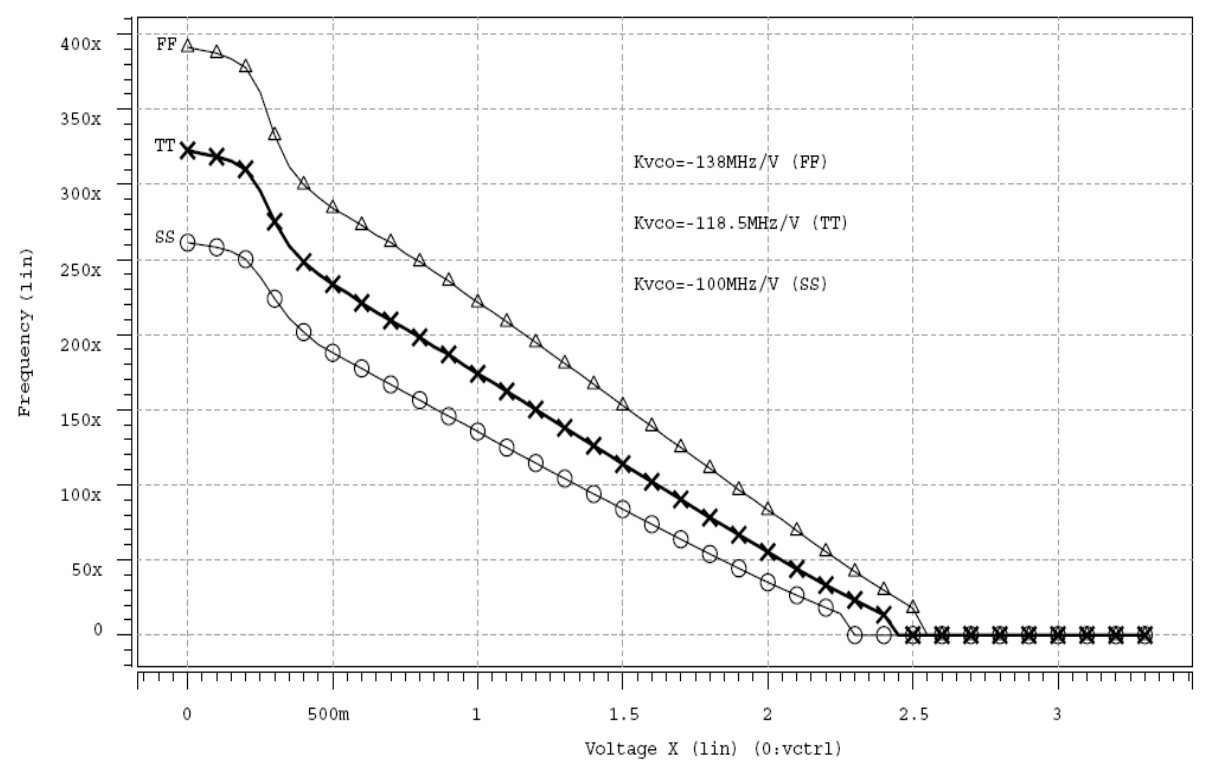


Fig. 3-15 Transfer curve of the VCO

3.2.3.5 Divider

Because the output frequency of the VCO is 125MHz and the input reference frequency is 31.25MHz. Hence a divided-by-four circuit is used. The TSPC D Flip-Flop connected its inverted output to D input is used as a divided-by-two circuit, as shown in Fig. 3-16 [17]. In this circuit we need to check input clock driving capability to assure correct operation. Then, two divided-by-two circuits are cascaded to get a divided-by-four circuit. Unfortunately, asynchronous counter will accumulate jitter stage by stage. A synchronous counter is used at the last stage to re-sample the clock, and it will eliminate the jitter accumulated in asynchronous counter, as shown in Fig. 3-17.

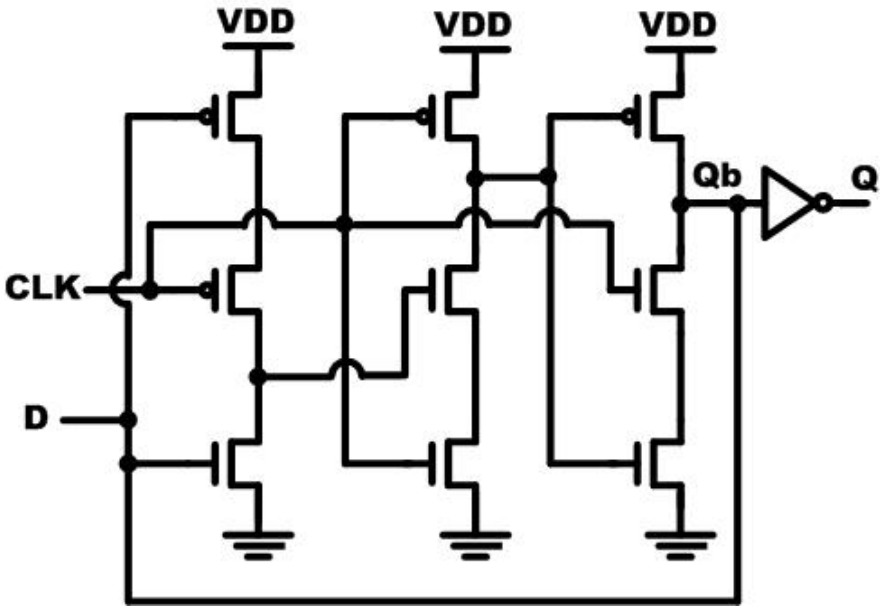


Fig. 3-16 Schematic of TSPC Asynchronous Divided-by-two circuit

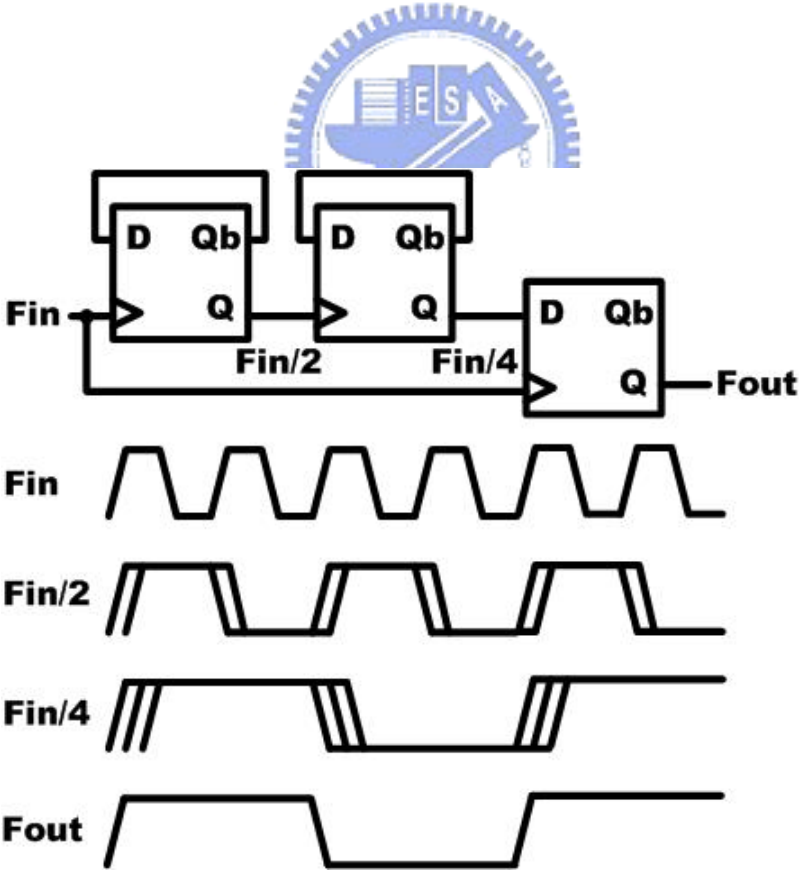


Fig. 3-17 Divider composed of asynchronous and synchronous counters and its timing diagram

3.2.4 PLL Parameter Design

Due to the charge pump switching characteristics, the PLL is generally a discrete-time domain operation that is difficult to use continuous time-domain analysis. However, if under some condition, the s-domain model could also be used to get a thorough understanding of the negative feedback loop. Fig. 3-18 shows the linear model of the PLL.

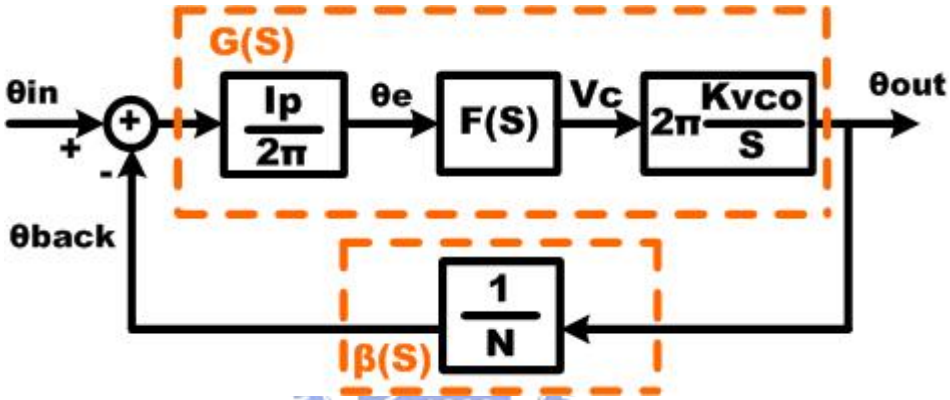


Fig. 3-18 Linear model of PLL

Assume the PLL is in lock state. The PFD and CP have a current change of Ip/2π (A/rad), the LF has a transfer function F(s) (V/A), the VCO has a gain of Kvco (Hz/v), and the feedback factor is 1/N. The conversion gain of the VCO should be changed to 2πKvco/s (rad/sec-V), because phase is the integral of the frequency. Based on the above definitions and PLL linear model, the open loop gain of the PLL can be represented as

$$G(s)\times\beta(s)=\frac{\theta_{back}(s)}{\theta_{in}(s)}=\frac{I_P\times Kvco\times F(s)}{s\times N} \tag{3-9}$$

The closed loop transfer function of the PLL is given by

$$H(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{G(s)}{1+G(s)\times\beta(s)}=\frac{N\times G(s)}{N+G(s)}=\frac{N\times K}{s+K} \tag{3-10}$$

Therefore, the 3-dB bandwidth is

$$\omega_{3dB}=K=\frac{I_P\times Kvco\times F(s)}{N} \tag{3-11}$$

From analysis of LF in section 3.2.3.3, we know that the shunt capacitance C_2 is typically much smaller than C_1. Therefore, we can neglect the capacitor C_2 and using classical two-pole system and second-order linear model of PLL to analyze the characteristic of transient response. With $F(s) = R_1 + (1/sC_1)$, the closed loop transfer function can be derived as

$$H(s)=\frac{I_P\times K_{vco}}{C_1}\cdot\frac{(1+SR_1C_1)}{S^2+\frac{I_PK_{vco}R_1}{N}S+\frac{I_PK_{vco}}{NC_1}} \tag{3-12}$$

Equation (3-12) can be compared to the classical two-pole system transfer function

$$H(s)=\frac{2\zeta\times\omega_n+{\omega_n}^2}{S^2+2\zeta\times\omega_n\times S+{\omega_n}^2} \tag{3-13}$$

Therefore, the natural frequency ω_n, and damping factor ζ can be derived as

$$\omega_n=\sqrt{\frac{I_pK_{vco}}{NC_1}} \tag{3-14}$$

$$\zeta=\frac{\omega_n}{2\omega_z} \tag{3-15}$$

In the case of the PLL design, the frequency noise of the VCO could be the dominant noise source to influence the phase noise performance. As will be seen in later section, the noise of the VCO has the high pass characteristics. Therefore, a large loop bandwidth for the PLL feedback system is better because it can enhance the tracking ability. The choice of the damping factor ζ is a trade off between acquisition time and step response stability. If larger ζ

is chosen, the system could have longer acquisition time. On the other hand, if smaller ζ is chosen, the system may be ringing for step response or become unstable.

Then, we use the loop bandwidth and the phase margin to determine the component values of the loop filter. By substituting equation (3-2) into equation (3-11), we can get

$$Loop\ BW = \frac{I_P \times Kvco}{N} \cdot \frac{R_1 C_1}{C_1 + C_2} \tag{3-16}$$

From equation (3-17), the phase term will be determined based on the pole and zero of the loop filter such that the phase margin is calculated as

$$PM = \tan^{-1}\frac{BW}{\omega_z} - \tan^{-1}\frac{BW}{\omega_p} \tag{3-17}$$

By setting the derivative of the phase margin equal to zero, the phase margin is maximum when the loop bandwidth is set to the average of pole and zero.

$$BW = \sqrt{\omega_z \omega_p} \tag{3-18}$$

We can define a new parameter, γ, as

$$\gamma = \frac{BW}{\omega_z} = \frac{\omega_p}{BW} \tag{3-19}$$

From equation (3-20), the capacitance ration of C_1 and C_2 can be represented by

$$\frac{C_1}{C_2} = \gamma^2 - 1 \tag{3-20}$$

The loop bandwidth (BW) now can be written as

$$BW = \frac{I_p \times K_{VCO}}{N} \cdot R_1 \left(1 - \frac{1}{\gamma^2}\right) \tag{3-21}$$

The design flow of a third-order PLL can be derived from equations (3-19), (3-20), and (3-21). The design flow can be summarized as follows [18]:

(1) Determine Kvco by measuring VCO test keys or simulating a VCO using in your design or referring to the data sheets of the employed commercial VCO.

(2) Depending on the desired noise and transient performance, determine the loop bandwidth BW. Usually, BW is less than 1/10 of reference clock.

(3) If the filter is off-chip, set Ip to be around 100μA to 1mA. If an on-chip filter is employed, decrease the value of Ip so that reasonable trade off between chip area and pump current could be reached.

(4) Determine the nominal value of N according to the system to be applied to.

(5) Selecting the required PM specification. The zero and pole positions are then determined by equation (3-19).

(6) With BW, Ip, PM, N, and Kvco determined, R_1 can be calculated with equation (3-21).

(7) Calculate the value of C_1 with $C_1=1/R_1\omega_z$.

(8) Calculate the value of C2 by equation (3-20).

The parameters used in the PLL are listed in Table. 3-1. The MATLAB simulation results based on equation (3-11) and (3-12) can be shown in Fig. 3-19 and Fig. 3-20. Fig. 3-21 shows PLL closed-loop control voltage of the SPICE simulation. Fig. 3-22 shows the eight even-spaced phases of frequency 125MHz.

Table. 3-1 Parameters of the PLL

Technology	0.35μm 2P4M CMOS
Function	PLL
Supply Voltage	3.3V
Input Frequency	31.25MHz
Output Frequency	125MHz
Charge Pump Current	150μA
Divided by N	N=4
VCO gain	118.5MHz/V
C_1	63.34pF
R_1	4.56kΩ
C_2	2.03pF
Phase Margin	70°
Loop Bandwidth	3.125MHz
Damping Factor	1.2
Power	24.2mW@125MHz

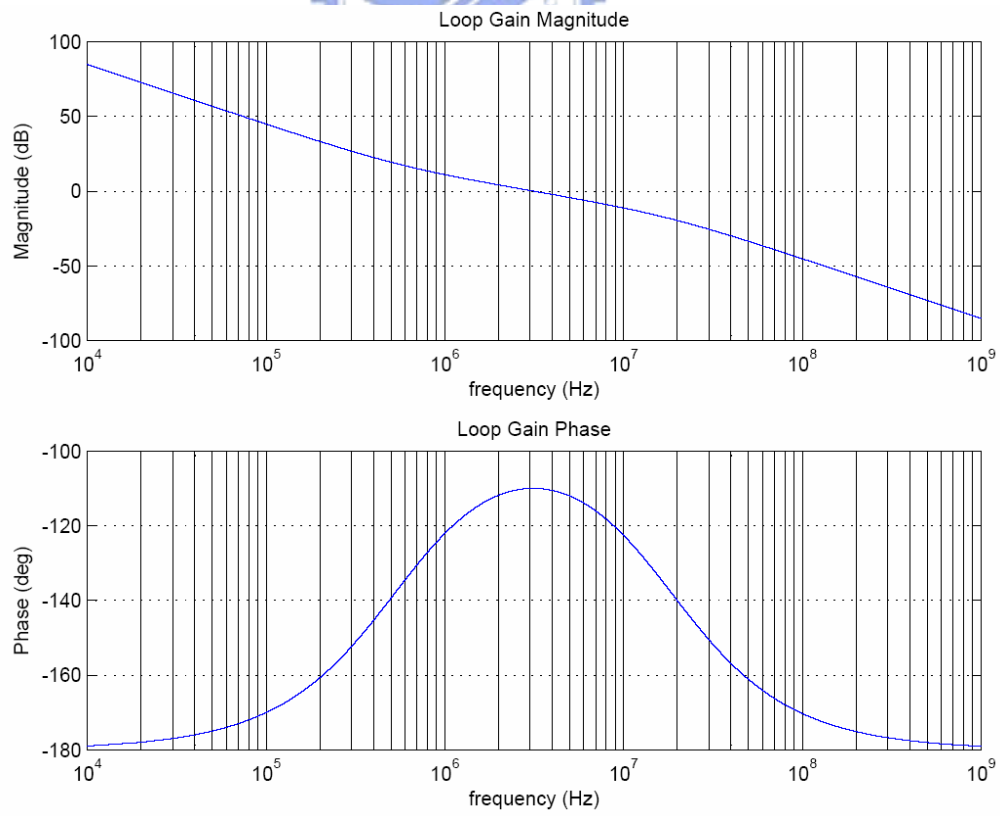


Fig. 3-19 Open loop simulation using parameter in Table. 3-1

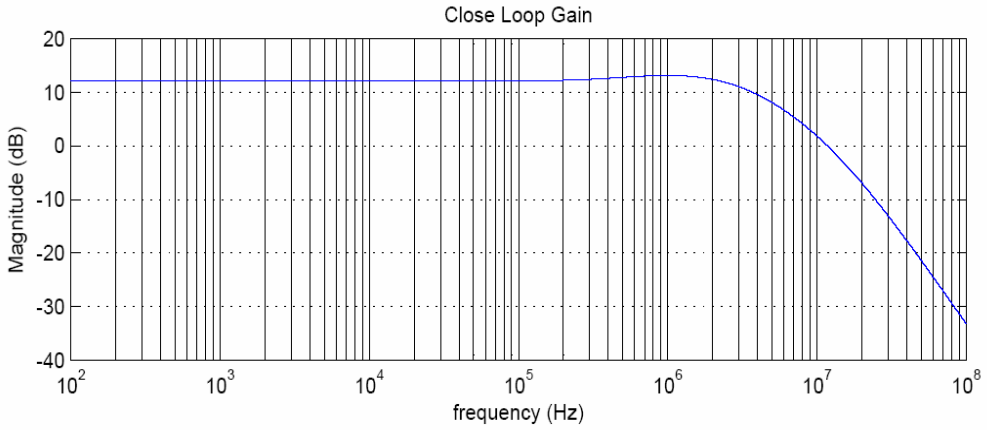


Fig. 3-20 Close loop simulation using parameter in Table. 3-1

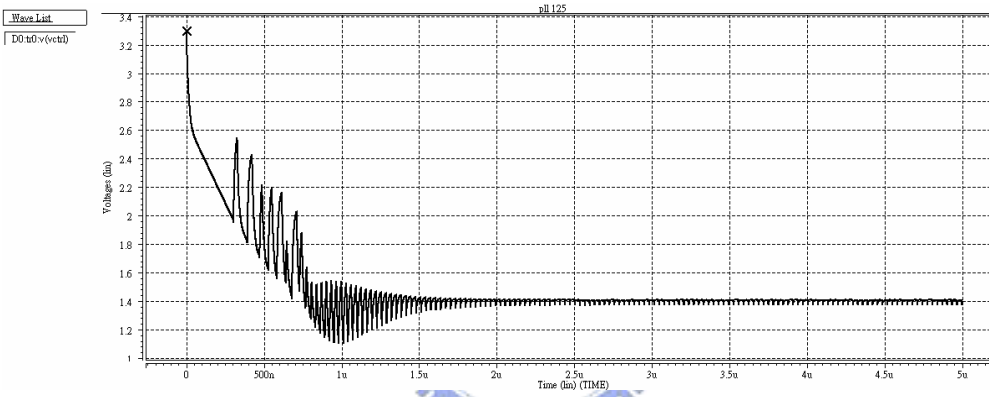


Fig. 3-21 Control voltage simulation using SPICE

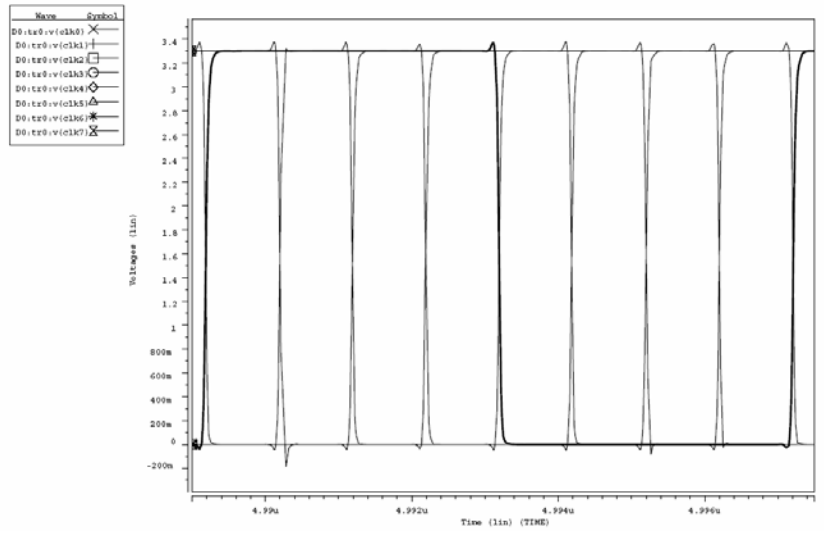


Fig. 3-22 Simulation of eight-phase of the PLL

3.2.5 PLL Noise Analysis and Stability

As mentioned in chapter 2, timing jitter could affect the maximum timing margin of the transceiver and therefore, performance of the serial link. The output clock jitter performance of the PLL depends on the jitter of the VCO, input source, and the design of the loop parameters. There are some noise sources that contribute the output jitter in PLL, as depicted in Fig. 3-23, where θ_{in} is the reference noise, θ_{pfd} is PFD and CP noise, θ_{lf} is loop filter noise, and θ_{vco} is the VCO noise.

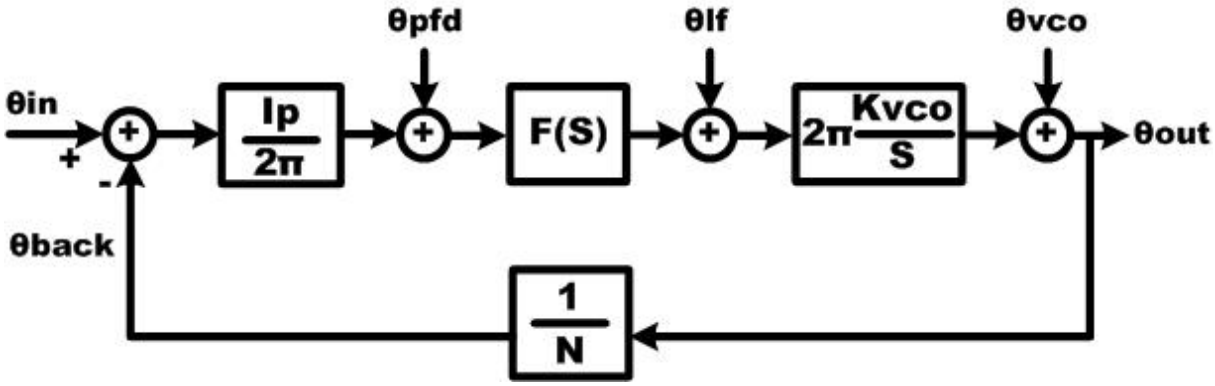


Fig. 3-23 Linear model of PLL with different noise sources

These noises introduce the phase fluctuations or timing jitter in time domain. Using closed loop analysis, the transfer functions with different noise sources can be derived as

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{N \times K}{s + K} \tag{3-22}$$

$$H_{pfd}(s) = \frac{\theta_{out}(s)}{\theta_{pfd}(s)} = 2\pi \cdot \frac{N}{I_P} \cdot \frac{K}{s + K} \tag{3-23}$$

$$H_{lf}(s) = \frac{\theta_{out}(s)}{\theta_{lf}(s)} = 2\pi \cdot \frac{K_{vco}}{s+K} \tag{3-24}$$

$$H_{vco}(s) = \frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{s}{s+K} = 1 - \frac{H(s)}{N} \tag{3-25}$$

where K and H(s) are given in (3-10) and (3-11). Each noise transfer function has its own characteristics. H(s) and $H_{pfd}(s)$ are low-pass functions, $H_{lf}(s)$ is a band-pass function, and $H_{vco}(s)$ is a high-pass function. Therefore, based on the different frequency responses of the transfer functions, there exists a trade off in choosing the wide or narrow bandwidth. Narrow bandwidth of PLL will suppress noise from the input reference source and PFD part, while wide one will suppress noise from the VCO. Most of the time, the input source of the PLL is from the crystal oscillator, which has much smaller phase noise than the one of the VCO. Therefore, the input source could be viewed as jitter-free. Based on the analysis, the loop bandwidth of the PLL should be maximized to meet the high-pass function of the VCO to reduce the timing jitter. The maximum nature frequency ω_n of the PLL is restricted of the reference clock frequency ω_{in}. Using the analysis from [19] [20], the criteria of the stability limit can be derived as

$$\omega_n^2 < \frac{\omega_{in}^2}{\pi(R_1 C_1 \omega_{in} + \pi)} \tag{3-26}$$

As a rule of thumb, stability can be assumed by keeping $\omega_n < 1/10\ \omega_{in}$. Choosing larger loop bandwidth indicates that more phase noise from the input clock will transfer to the output with larger loop bandwidth. However, it does not cause a problem when the input is a clean clock source.

3.3 Multiplexer and Pre-driver

The multiplexer is used to serialize the pre-skewed parallel data channels D0~D7. Each multiplexer is switched by two series NMOS transistors that are controlled by two adjacent clock phases. For example, as shown in Fig. 3-24, at the timing interval between the rising edge of clk4 and the falling edge of clk1, the center of the input signal D0+ and D0- starts driving the multiplexer output. The PLL generates the required phases of clk0 through clk7 with 1ns phase resolution to reach the data transfer rate of 1Gbps.

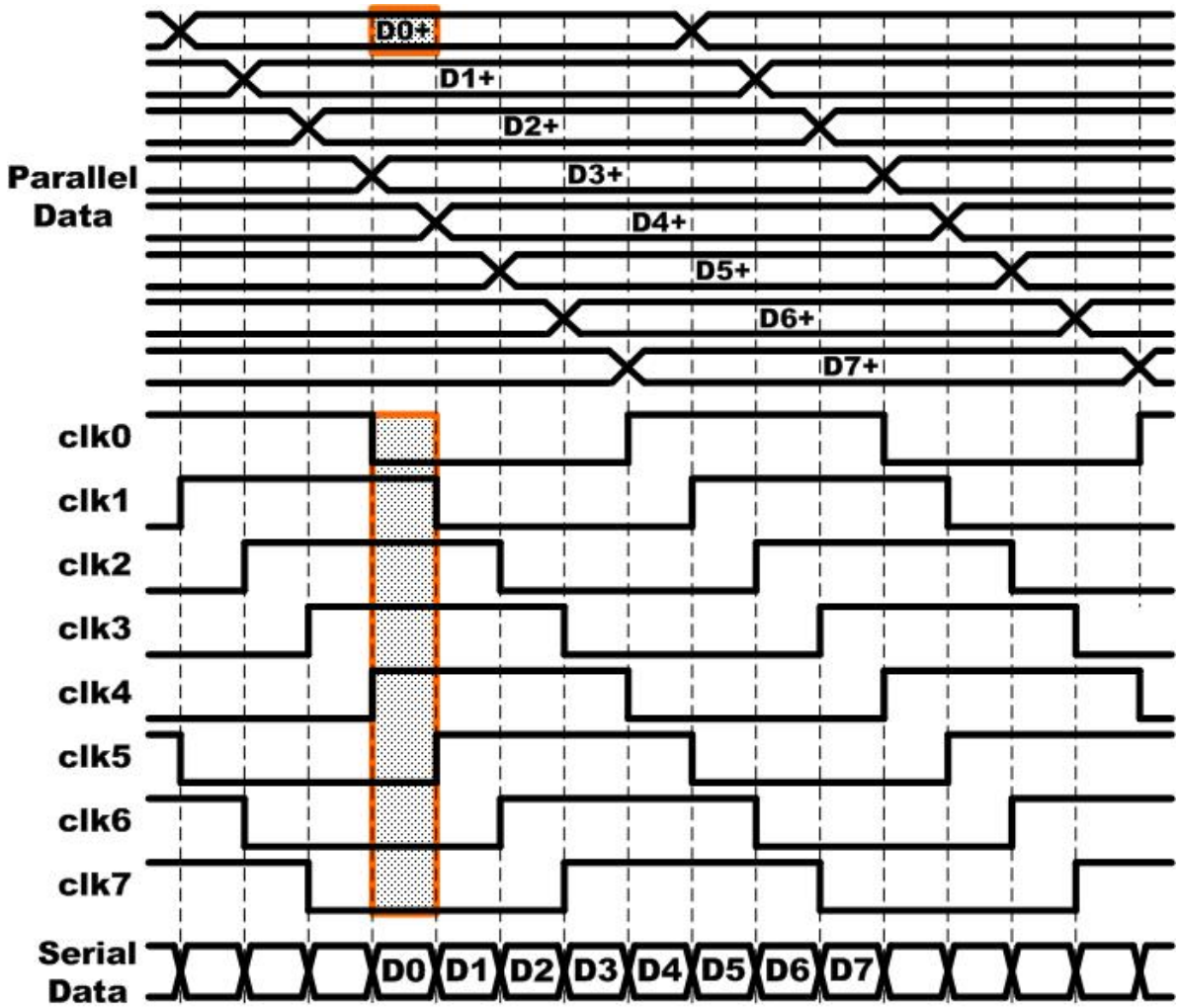


Fig. 3-24 Timing diagram of an 8 to 1 multiplexer

The schematic of the eight to one multiplexer is shown in Fig. 3-25 [21]. The speed of the multiplexer circuit is mainly determined by the resistance of PMOS and the total capacitance of the output node. Increasing the PMOS size relative to the NMOS size would increase the speed while reducing the swing of the output nodes A and B. The ratio of the PMOS and NMOS sizes has to be chosen such that the swing at the multiplexer outputs A and B are enough to switch the pre-driver in the worst case.

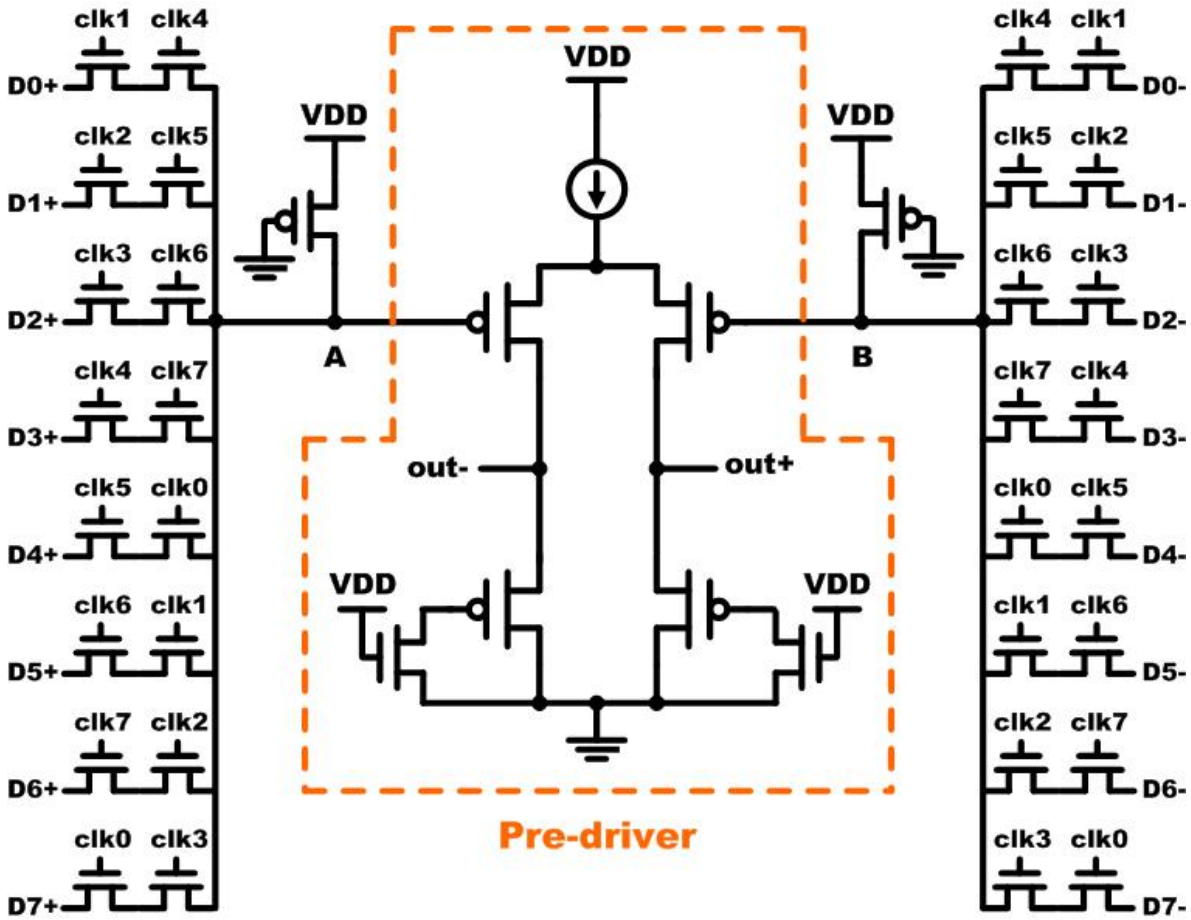


Fig. 3-25 Schematic of the 8 to 1 multiplexer and pre-driver

In order to determine pre-emphasis or not, we must know the previous bit and the current bit to control the pre-emphasis driver. The schematic of the pr-emphasis multiplexer is identical to Fig. 3-25 except it is delayed by one bit period 1ns, as shown in Fig. 3-26 [22].

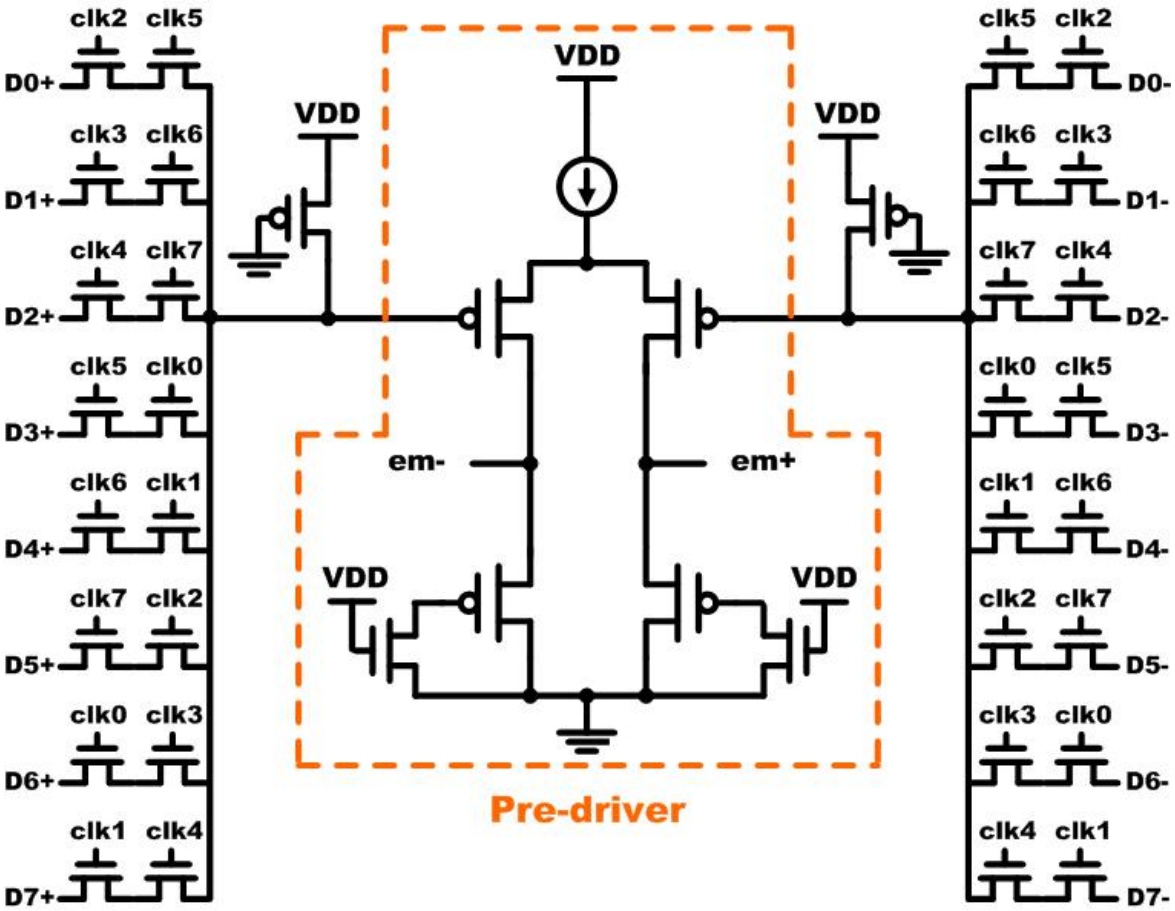


Fig. 3-26 Schematic of the 8 to 1 pre-emphasis multiplexer and pre-driver

The pre-driver is composed of a source coupled pair with active inductive peaking load. It is inserted between the multiplexer and the final output driver to reduce the size of the multiplexer. The active inductive peaking load can substantially enhance the bandwidth of gain stages [23]. The implementation of the active inductor is shown in Fig. 3-27, which consists of a PMOS device and a resistor Rs placed in series with the gate of PMOS. The PMOS device is operated in the saturation region, and the passive resistor can be realized using a NMOS operating in the triode region. The impedance looking into the source of the PMOS can be approximated by

$$Z_{out} = \frac{1}{g_m} \cdot \frac{1 + sR_s C_{gs}}{1 + sC_{gs} / g_m} \tag{3-27}$$

where gm is the transconductance of the PMOS.

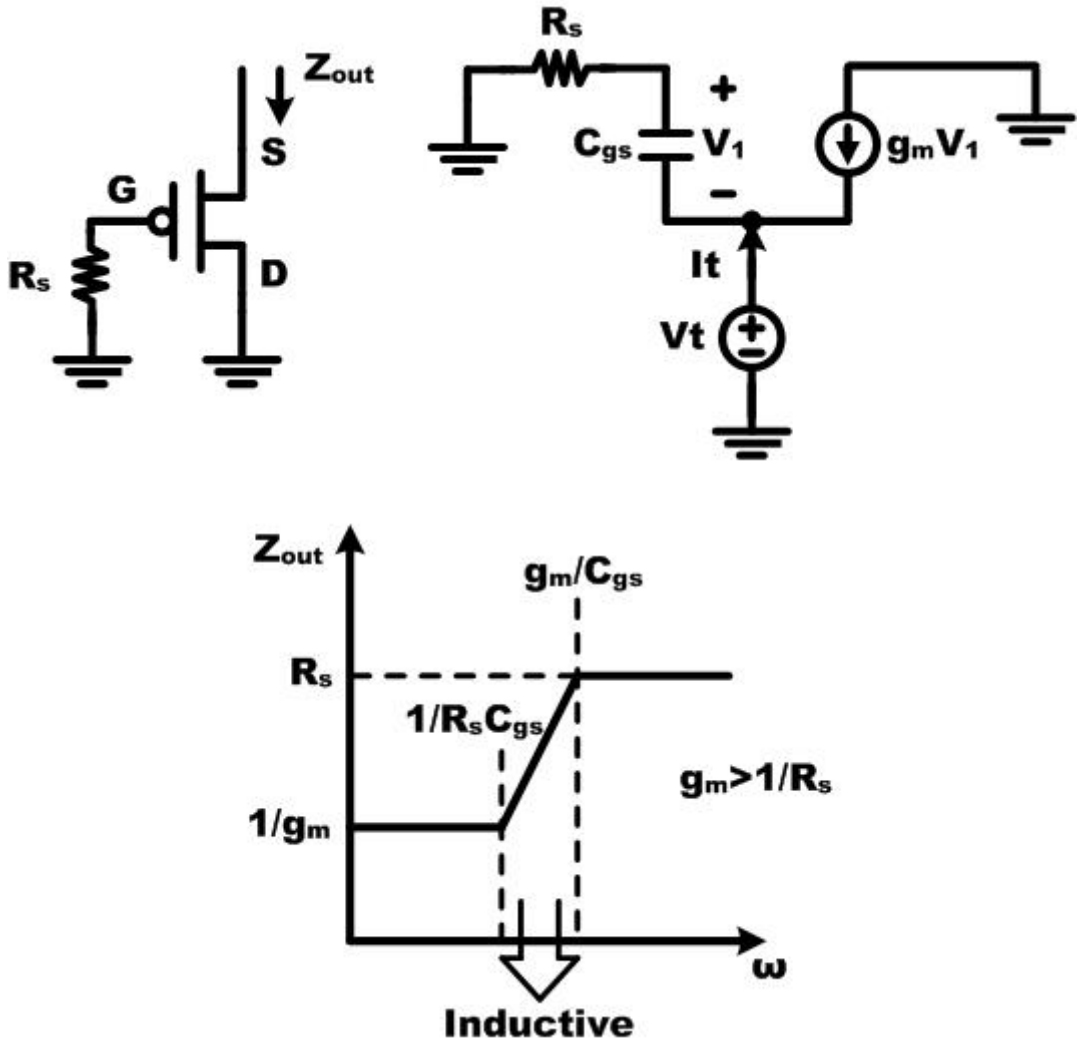


Fig. 3-27 Implementation of the active inductor peaking

Therefore, the zero and pole of the Zout is given by

$$Zero = -\frac{1}{R_s C_{gs}} \tag{3-28}$$

$$Pole = -\frac{g_m}{C_{gs}} \tag{3-29}$$

The additional zero is introduced by the resistor Rs. For Zout to behave as an inductor, it

is require that

$$Zero > Pole \Rightarrow g_m > \frac{1}{R_s} \tag{3-30}$$

The inductive region (zero < ω < pole) and the inductance can be adjusted by tuning the locations of the pole and zero. The inductive region should cover the bandwidth of the pre-driver for a better gain and bandwidth boosting performance and the frequency response of the pre-driver should has the optimum group delay.

3.4 Data Driver and Pre-emphasis Driver

The data driver, as shown in Fig. 3-28, is an open-drain current-mode driver, which is composed of a differential source coupled pair with a stable constant current source Id. The input signal out+ and out- is from the pre-driver output mentioned in section 3.3, which is the serialized data with data rate 1Gbps. The outputs of the data driver, D+ and D-, are to directly drive a differential cable line. The data driver is providing a balanced AC current drive to the cable line imposed on the DC current Id to reach the required output swing.

The main issue of the data driver is the settling time control, that is, the bandwidth limitation of the driver. When the bit time of the data is smaller than the settling time of the data driver, the values of the previously transmitted signal will affect the current bit's waveform. This interference, called inter-symbol interference (ISI), reduces the maximum frequency at which the system can operate. Therefore, as shown in Fig. 3-29, a pre-emphasis driver is applied directly on the output pins to enhance the settling ability of the data driver.

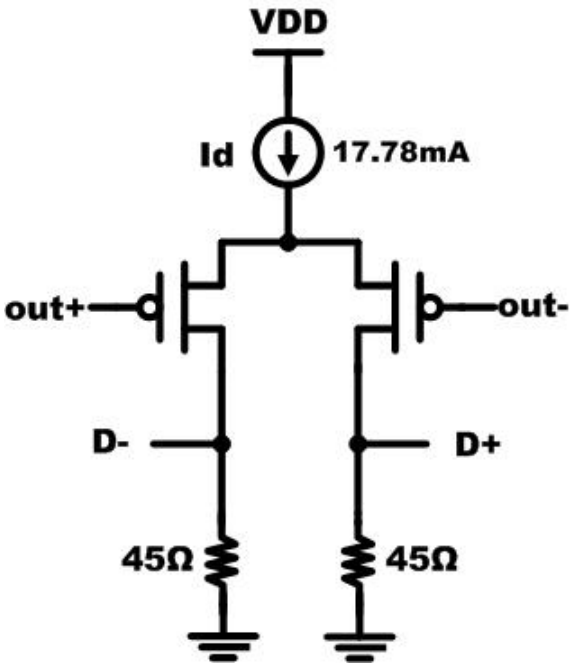


Fig.3-28 Schematic of the data driver

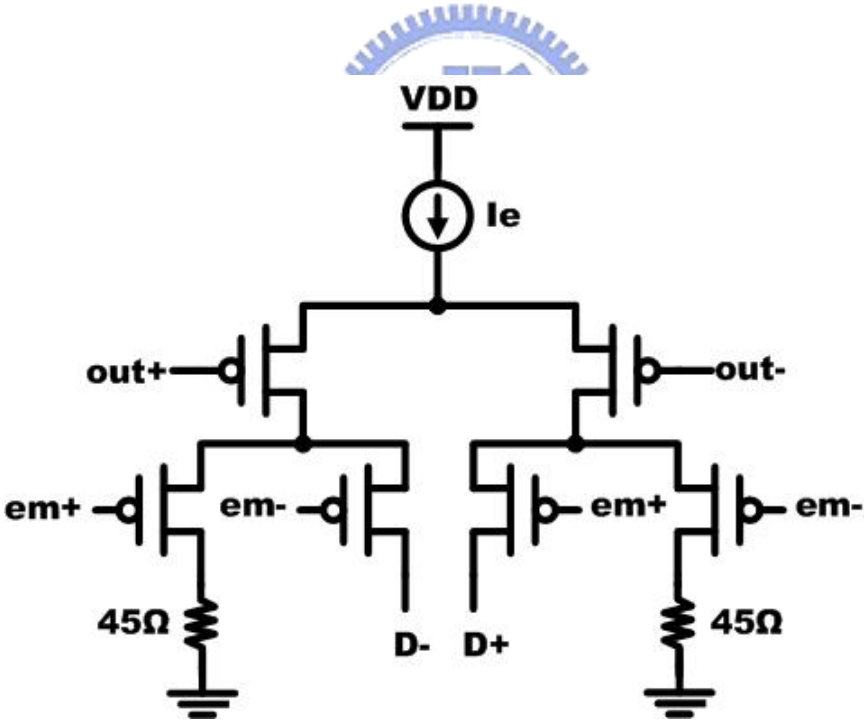


Fig. 3-29 Schematic of the pre-emphasis driver

Most of the output current comes from the data driver, controlled by the data multiplexer. The pre-emphasis multiplexer controls additional output current from the pre-emphasis driver

when the serialized data bit changes from low to high or from high to low. The operation of pre-emphasis is given as a summary in Table. 3-2.

Table. 3-2 The operation of pre-emphasis summary

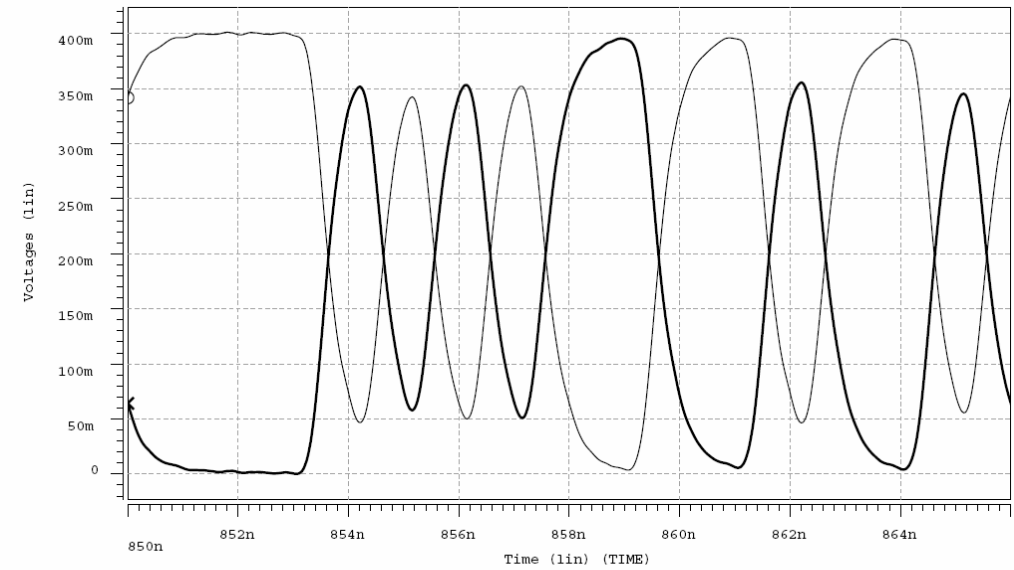
out+	out-	em+	em-	Pre-emphasis?	Id	Ie
High	Low	High	Low	No	D+	gnd
High	Low	Low	High	Yes	D+	D+
Low	High	High	Low	Yes	D-	D-
Low	High	Low	High	No	D-	gnd

3.5 Transmitter Simulation Results

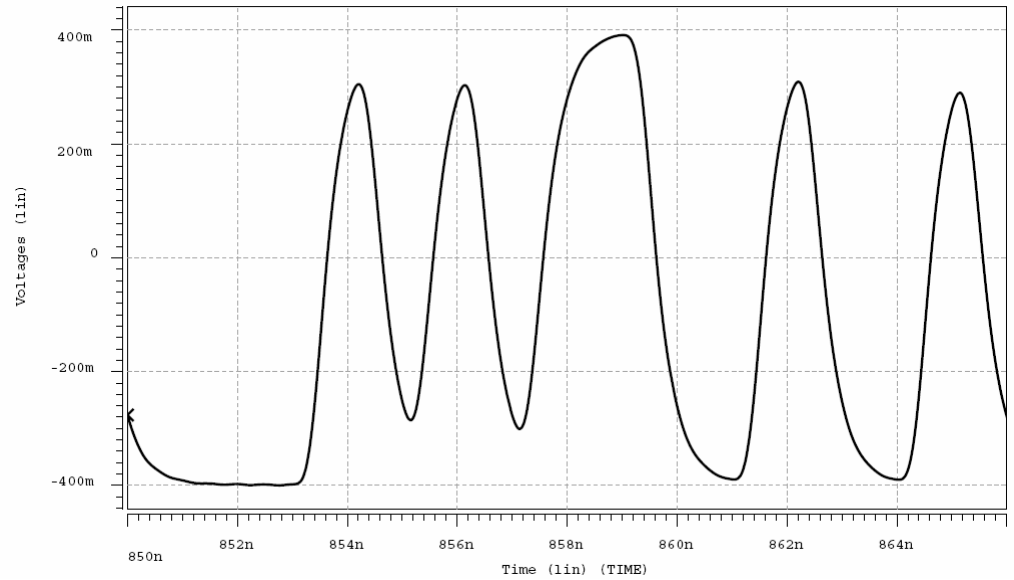
After transmitted from the transmitter circuit, the signals D+ and D- go through the bonding wire with internal bonding pad and external package pin. The thin bonding wire can be inductive, and the pad and the pin are inductive and capacitive. Then, the signals TxD+ and TxD- after going through the package transmit through the cable and arrive at the receiver termination resistor. Fig. 3-30 (a) shows the simulated waveforms of the proposed transmitter outputs TxD+ and TxD- without pre-emphasis. Fig. 3-30 (b) is the differential output. As can be seen, the high-frequency transmitted outputs TxD+ and TxD- are influenced by the past low-frequency outputs. Therefore, the high-frequency transmitted outputs could not meet the required output voltage range.

Fig. 3-31 (a) shows the simulated waveforms of the proposed transmitter outputs TxD+ and TxD- with the adding of pre-emphasis. By adding the pre-emphasis circuit, the data bit transition is now faster than that without pre-emphasis. Fig. 3-31 (b) is the differential output.

Fig. 3-32 shows the eye diagram of the signal at transmitting side without pre-emphasis. Fig. 3-33 shows the eye diagram of the signal at transmitting side with pre-emphasis.

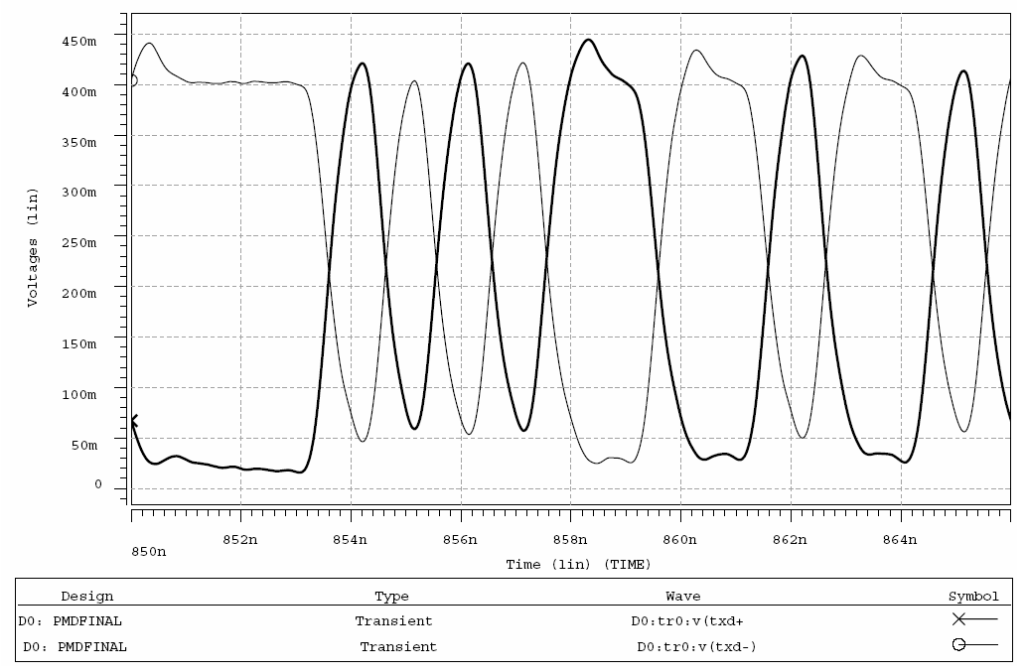


(a)

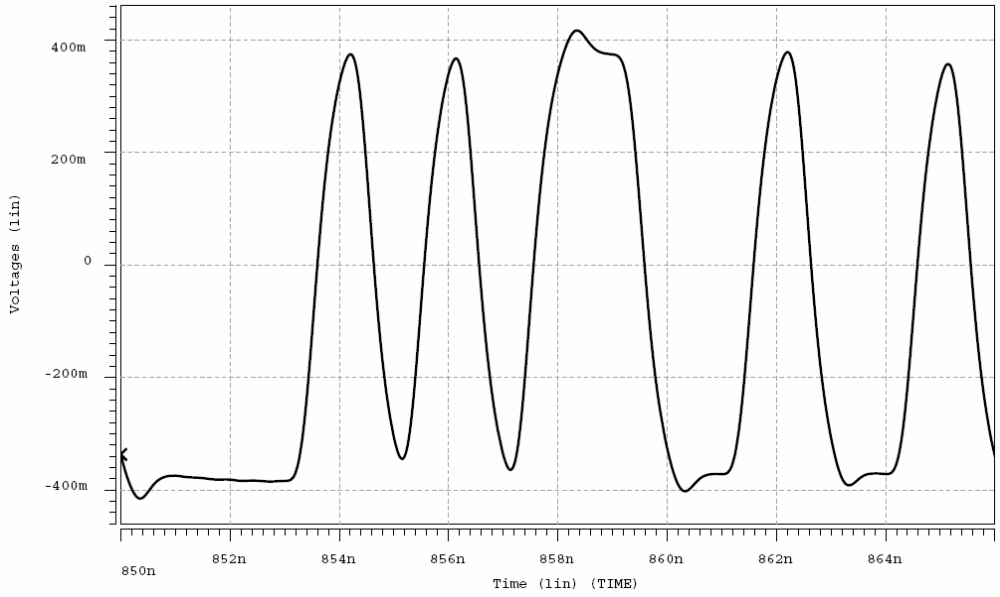


(b)

Fig. 3-30 Simulation results of (a) the driver outputs without pre-emphasis, (b) the differential output



(a)



(b)

Fig. 3-31 Simulation results of (a) the driver outputs with pre-emphasis, (b) the differential output

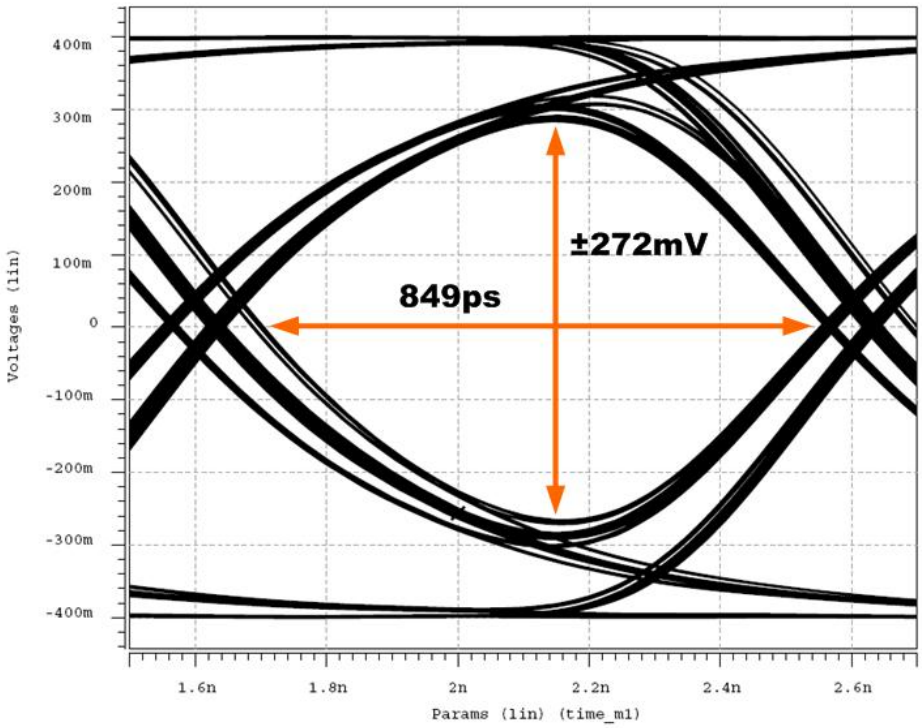


Fig. 3-32 Eye diagram of the signal at transmitting side without pre-emphasis

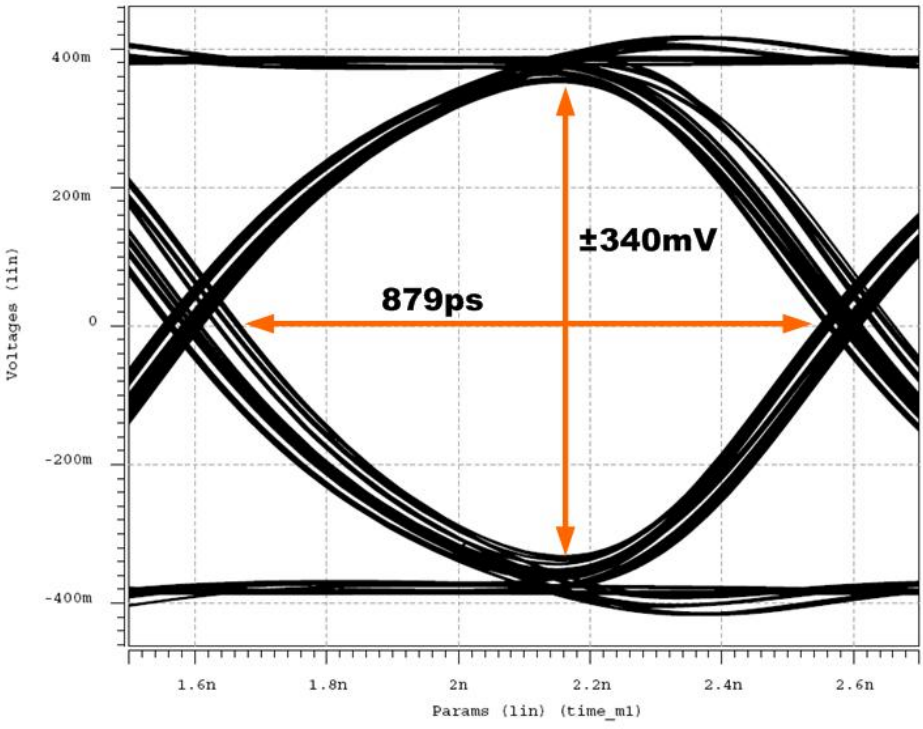


Fig. 3-33 Eye diagrams of the signal at transmitting side with pre-emphasis

Chapter 4

Receiver

4.1 Architecture of Receiver

This chapter presents the receiver design. The purpose of the receiver is to recovery the received signal to the original data by amplifying and sampling the signal. The clock and data recovery circuit embedded in the receiving side is to adjust the receiver clock based on the received data to make the sampling point into the center of the data eye. Then, the de-multiplexer makes recovered serial data become eight parallel data. Fig. 4-1 shows the block diagrams of the receiver architecture.

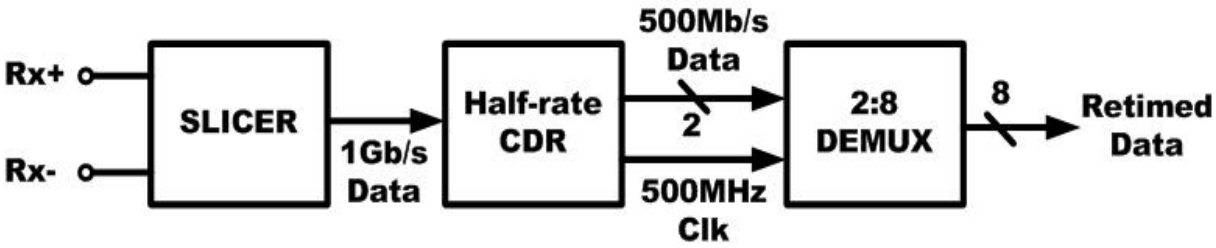


Fig. 4-1 Block diagrams of the receiver

4.2 Slicer

When the differential data enter the receiver chip, they will be distorted because of the inductance and capacitance resonance caused by bonding wire and pad. Fig. 4-2 shows the schematic of the slicer [24]. The slicer is one of the most important building blocks in the receiver circuit. It is actually an open-loop comparator. To meet the common mode voltage range, the circuit is implemented with PMOS input differential pairs with a constant current source and using NMOS crossed-coupled pairs as the load.

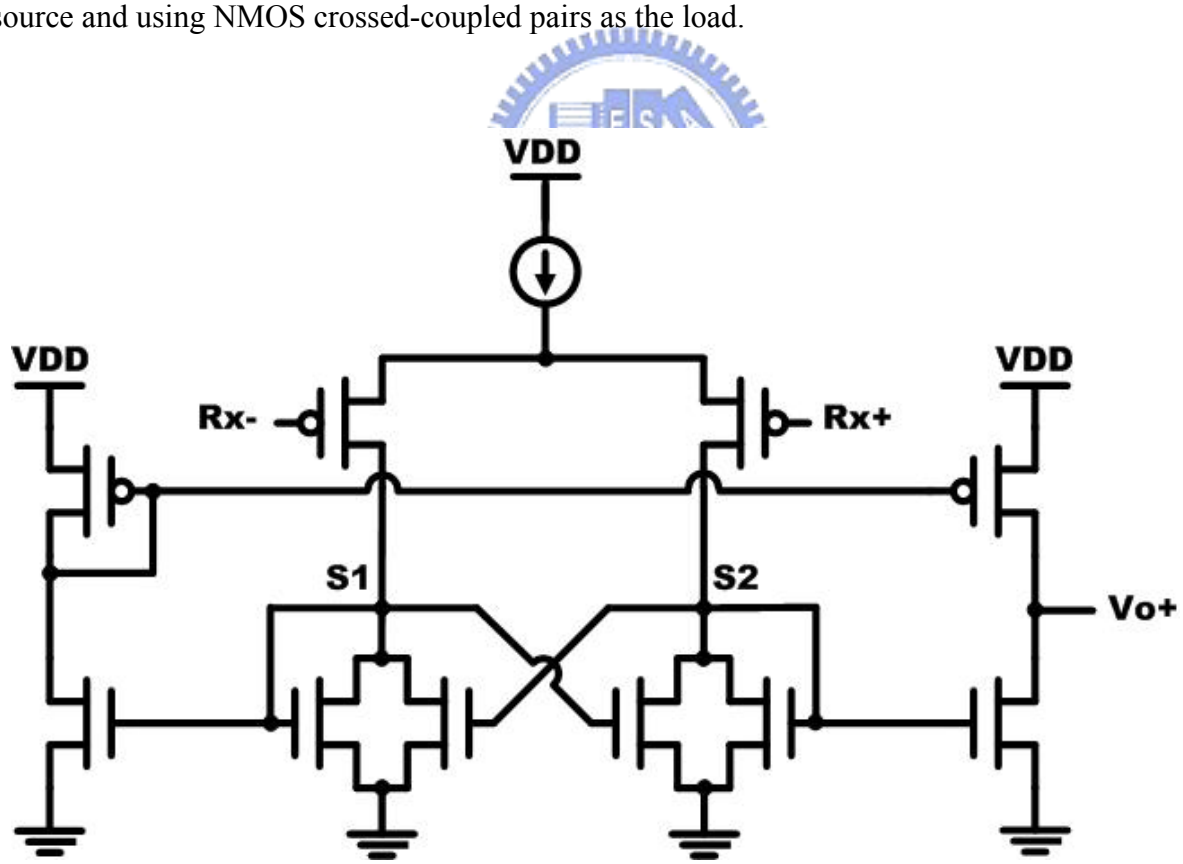
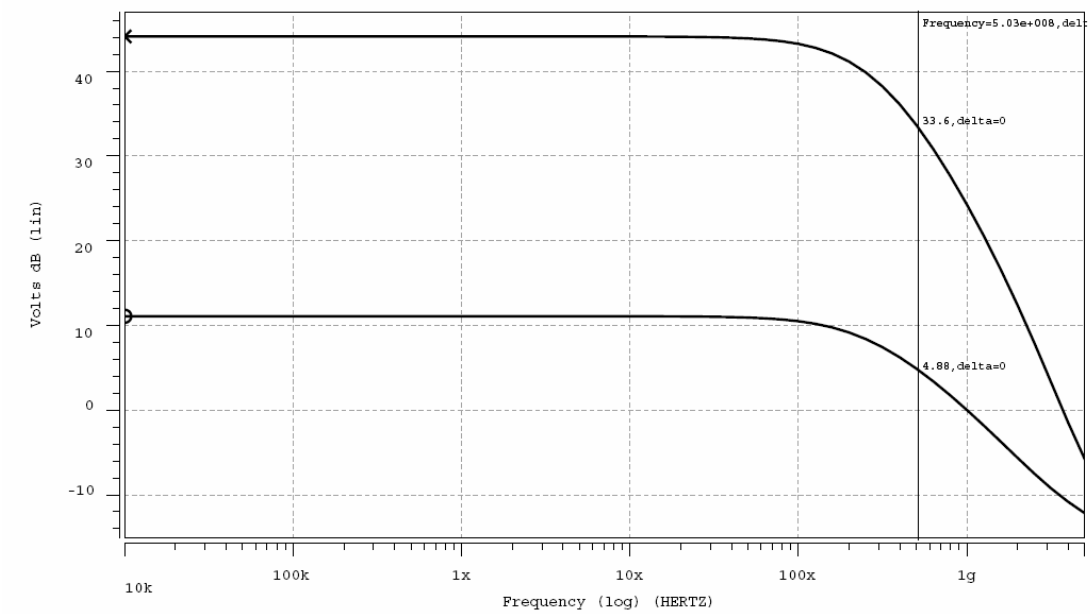


Fig. 4-2 Schematic of slicer

The slicer needs to be able to detect the received signals that were noisy and swing

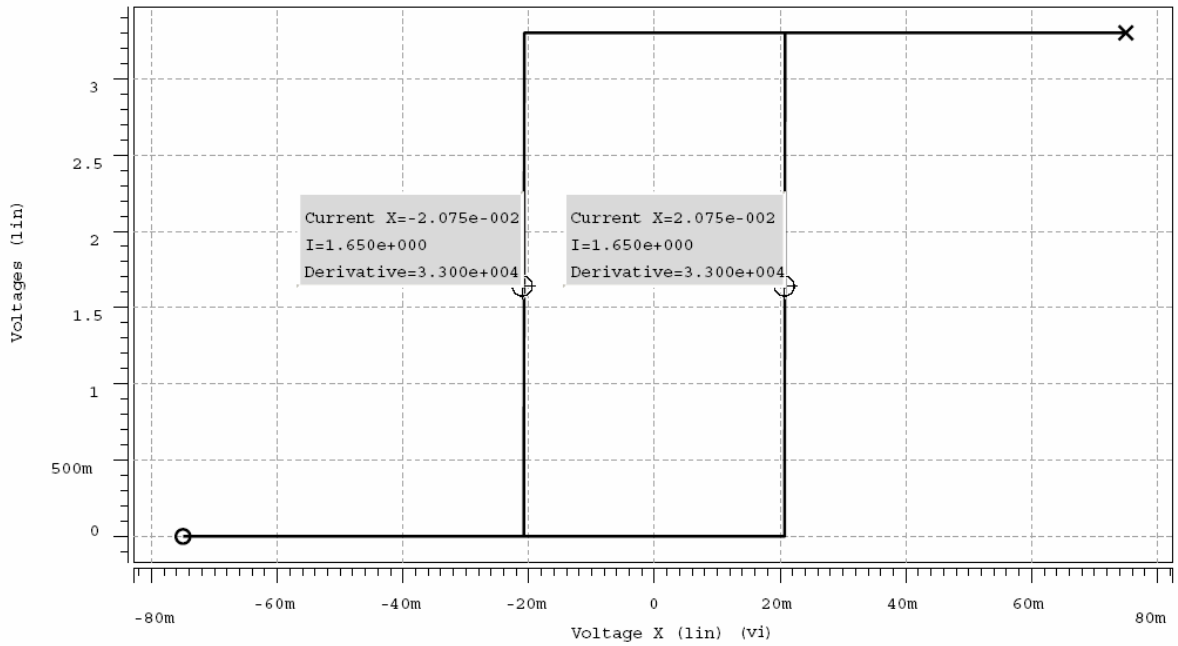
limited and amplify the signal to get the nearly full swing CMOS level at the output. Therefore, the gain and bandwidth of the slicer should be carefully designed to meet the requirement. Moreover, the offset voltage of the slicer also affects the correct operation of the receiver. The offset voltage is not only due to the mismatches in the input devices but also mismatches (both device and capacitance mismatch) within the positive-feedback structure. These errors are referred back to the input as the input-offset voltage. The slicer also consists of two on chip termination resistors to match the characteristic impedance of the channel to reduce the parasitic effect caused by the packages and reflections.

Fig. 4-3 is the frequency response of the slicer. It can be shown that within the full data rate of the transmitted NRZ signal, it still has 33.6dB gain. Fig. 4-4 shows the hysteresis window of the slicer. The advantage of this hysteresis comparator is noise immunity. The threshold voltage is determined by the system BER. Fig. 4-5 shows the corresponding output signal of the slicer, the limited received signals which are about 150mV are being amplified to the full scale. The data stream then sends to the following clock and data recovery circuit to get the data value.



Design	Type	Wave	Symbol
D0: SLICER	AC	D0:ac0:vdb(vo+)	
D0: SLICER	AC	D0:ac0:vdb(s2)	

Fig. 4-3 Frequency response of slicer



Design	Type	File	Wave	Symbol
D0: SLICER	DC	slicer.sw1	D0:sw1:v(vo)	
D0: SLICER	DC	slicer.sw2	D0:sw2:v(vo)	

Fig. 4-4 Hysteresis window of the slicer

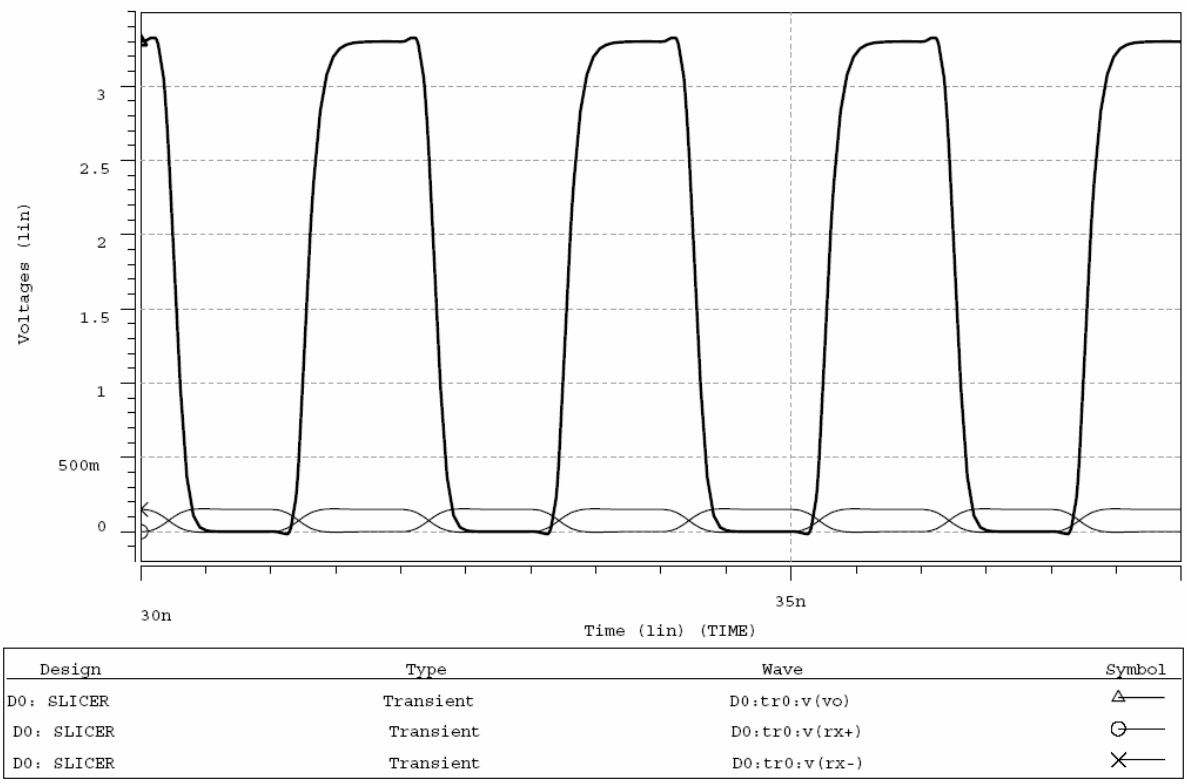


Fig. 4-5 The output of slicer when input 500MHz 150mV

4.3 Clock and Data Recovery

4.3.1 Introduction

The data stream received and amplified by the slicer is both noisy and asynchronous. The data must be retimed such that the jitter during transmission can be removed. The clock must also be extracted from the random data so as to allow synchronous operation. The task of data retiming and clock extraction is done by clock and data recovery (CDR) circuits. In the receiver, we introduce the circuit design of a PLL-based CDR. The main idea of a PLL-based CDR is the detection of the data location with respect to the clock edge during each data transition. If the data leads the clock, the clock will be sped up. If the data lags the clock, the

clock will be slowed down. Finally, the clock edge will be located at the midpoint of each bit by this feedback mechanism.

4.3.2 CDR Architecture

In this thesis, a half-rate dual-tracking loop CDR architecture with improved jitter performance and fast acquisition time is used, as shown in Fig. 4-6. As the power turn on, there may be a frequency drift in VCO due to the temperature and process variations. A frequency detector (FD) in company with a charge pump drives the VCO frequency to a value close to the half of the data rate. Then, a half-rate phase detector (PD) produces an error proportional to the phase difference between the 1Gbps data stream and the 500MHz output frequency of the VCO. Furthermore, the PD automatically retimes and de-multiplexes the data, generating two 500Mbps sequences.

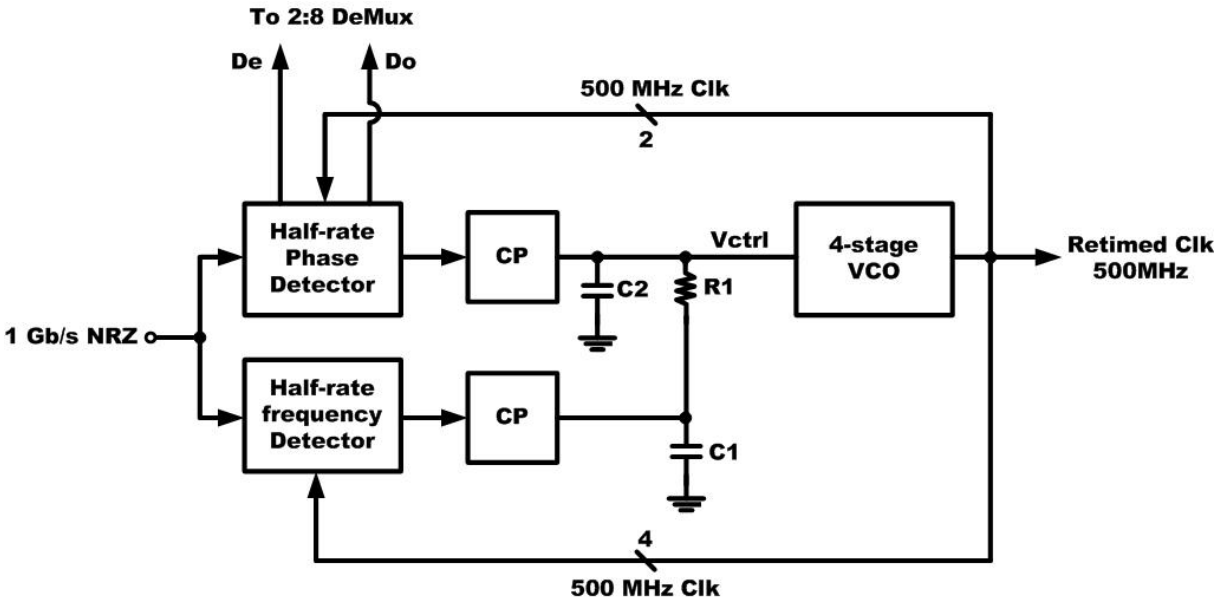


Fig. 4-6 Half-rate CDR architecture

4.3.3 Circuit Implementation

4.3.3.1 Half-rate Phase Detector

The phase detector used in CDR has more difficulties compared to the phase detector used in traditional PLL. The main reason which results in these difficulties is that PLL tracks a periodic input clock with a periodic output, while for CDR it should extract a periodic clock signal from non-periodic random data. As a result, phase detectors used in CDR should exhibit several properties. Firstly, data is encoded as NRZ format to obtain the highest throughput within a given channel bandwidth. However, the spectrum of NRZ signal does not have a frequency component at the bit rate. Therefore, nonlinear operation such as edge detection is needed in phase detectors so as to create the desired spectral line. Secondly, due to its random nature, the data may exhibit long sequences of consecutive ONEs and ZEROs which might introduce the drift in the oscillator frequency. Hence, in the absence of data transitions in the input bit stream, the phase detector must not produce any false phase comparisons in order to tolerate consecutive ONEs or ZEROs. In addition, due to unequal data-to-output and clock-to-output delays in typical flip-flops, a systematic phase offset may occur when the explicit decision circuit is used to sample the input data. In order to alleviate such skew problem, it is desired to retime the data inside the phase detector.

A half-rate phase detector is shown in Fig. 4-7 [25]. This phase detector generates an output whose average is linearly proportional to the phase error between input data and clock signal and the average output drops to zero when the loop is locked. Such linear property

makes the jitter performance of CDR better.

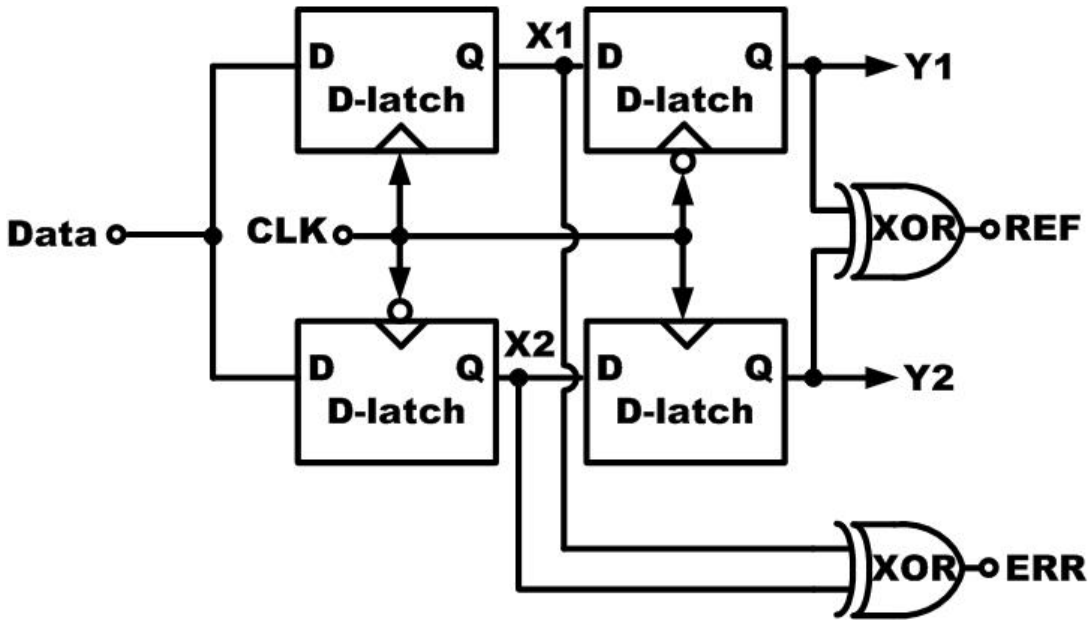


Fig. 4-7 Half-rate phase detector

Furthermore, this phase detector can sense the input random data at full rate but employ a VCO running at half of the input rate. The operation speed of other circuit can be lowered down so that the total power dissipation can be reduced.

Fig. 4-8 is the timing diagram for an arbitrary data signal with the clock properly centered within the data bit interval. While the two XOR operations provide both the ERR and the REF pulses for every data transition, the pulses in ERR are only half as wide as those in REF. This means that the amplitude of ERR must be scaled up by a factor of two with respect to REF so that the difference between their averages drops to zero when clock transitions are in the middle of the data eye. The Y1 and Y2 sequences are the de-multiplexed signals of the original input sequence.

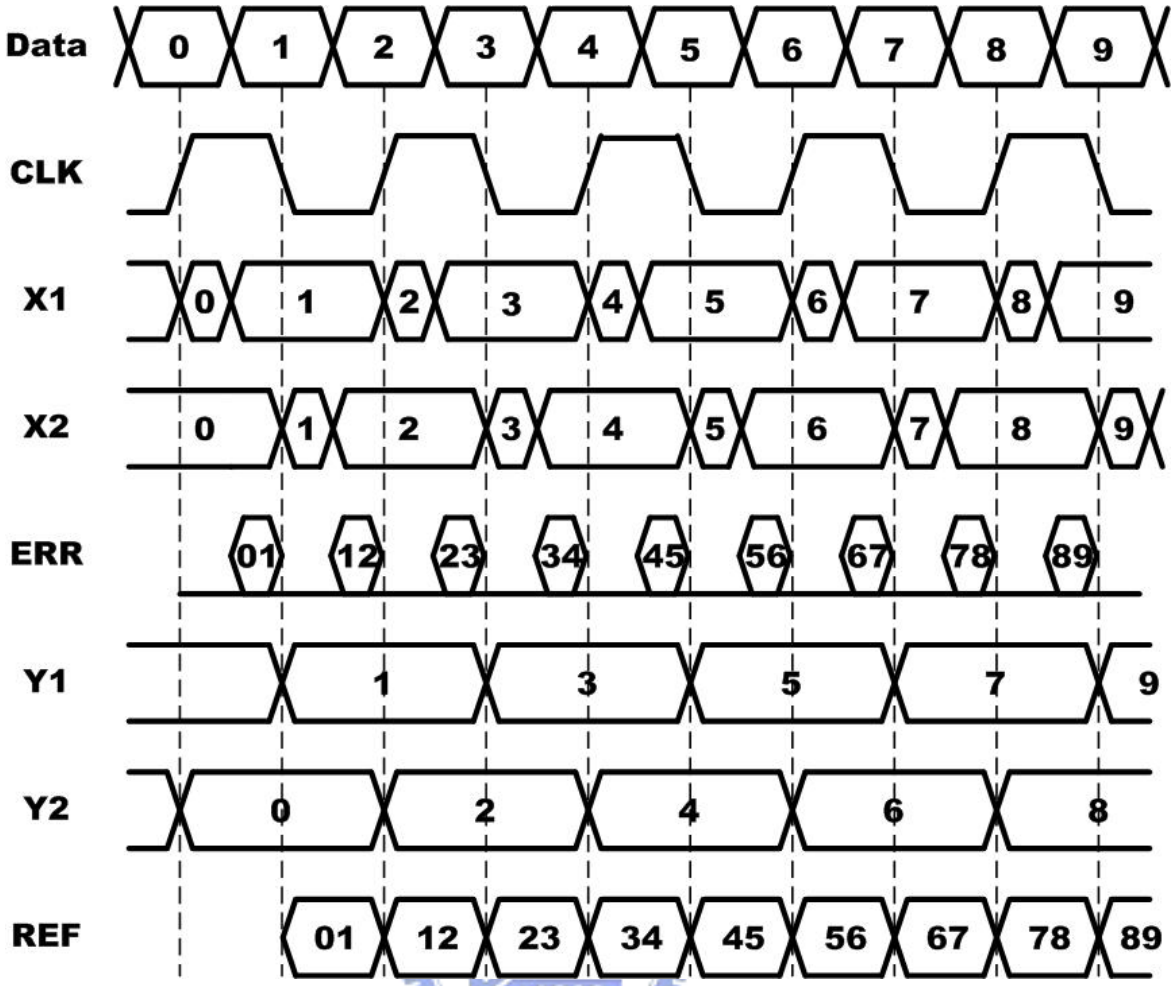


Fig. 4-8 Operation of the half-rate phase detector

Then, the ERR and REF signals are applied to the charge pump circuit similar as Fig. 3-7 mentioned in section 3.2.3.2. Since the gain of the VCO is negative in our design, the ERR part of the PD should create a discharge current scaled up by a factor of two with respect to REF charging current so that the average output voltage equal for zero phase difference.

The transfer characteristic of the phase detector is shown in Fig. 4-9 where the average current of the charge pump circuit is obtained as the phase difference varies from zero to one bit period. Based on the result shown in Fig. 4-9, the charge pump circuit has a zero current while the phase error is 475ps, indicating that the systematic offset between the data and the clock is very small.

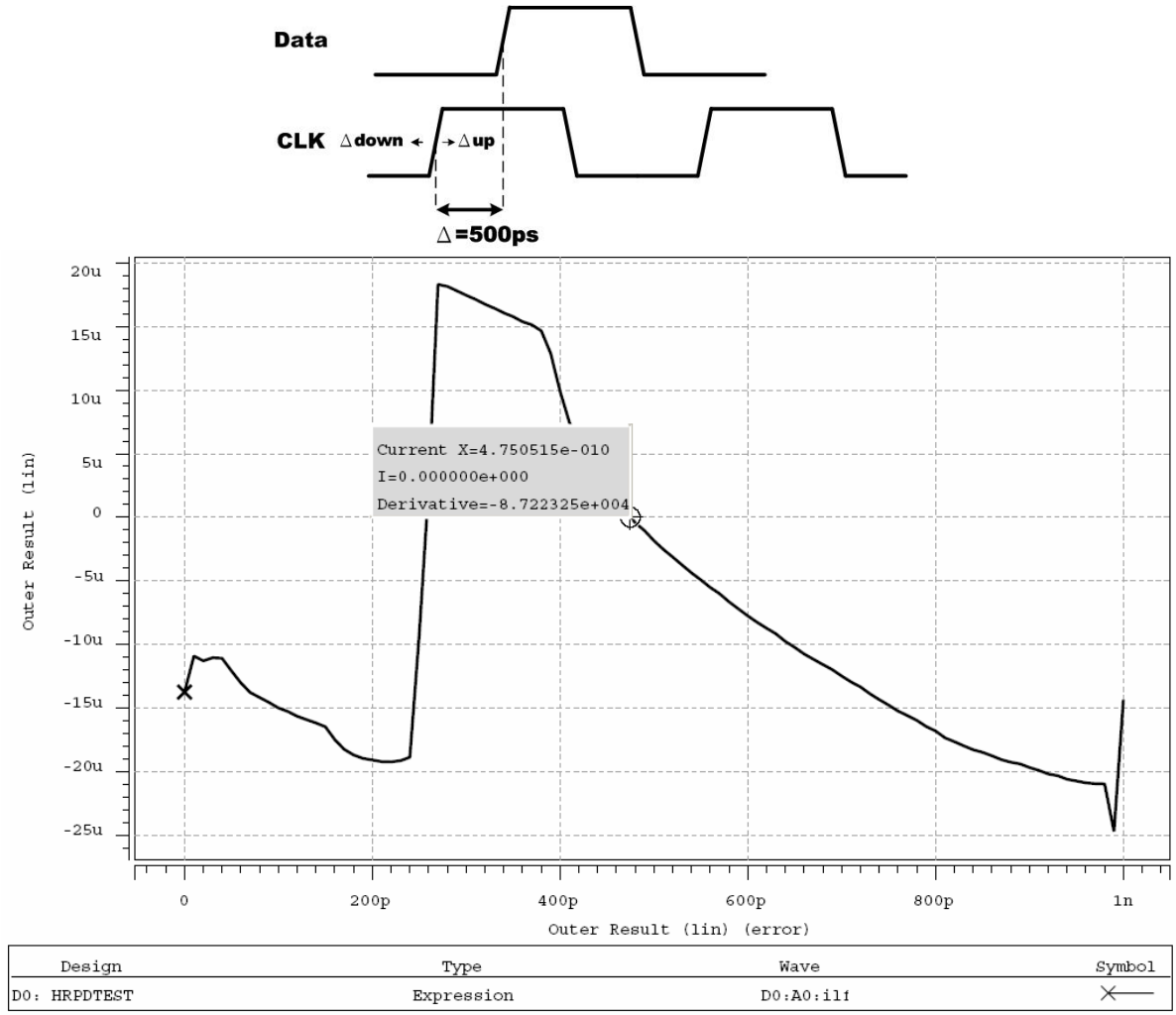


Fig. 4-9 Transfer characteristic of PD

4.3.3.2 Half-rate Frequency Detector

The circuit implementation of the half-rate frequency detector is shown in Fig. 4-10 [26] [27] [28]. At every transition of the input NRZ data, the multiple clock phases of 45° spacing, clk0, clk45, clk90, and clk135 are sampled. The D flip-flops, D5, D6, D7, and D8 play a role as registers that save the two XOR outputs X1 and X2.

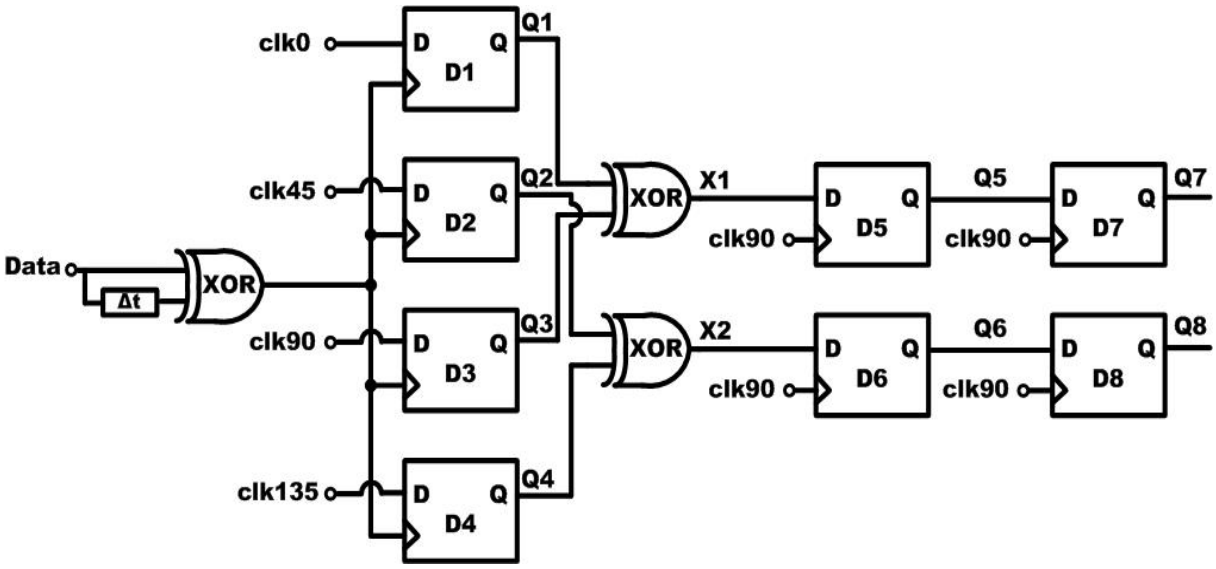
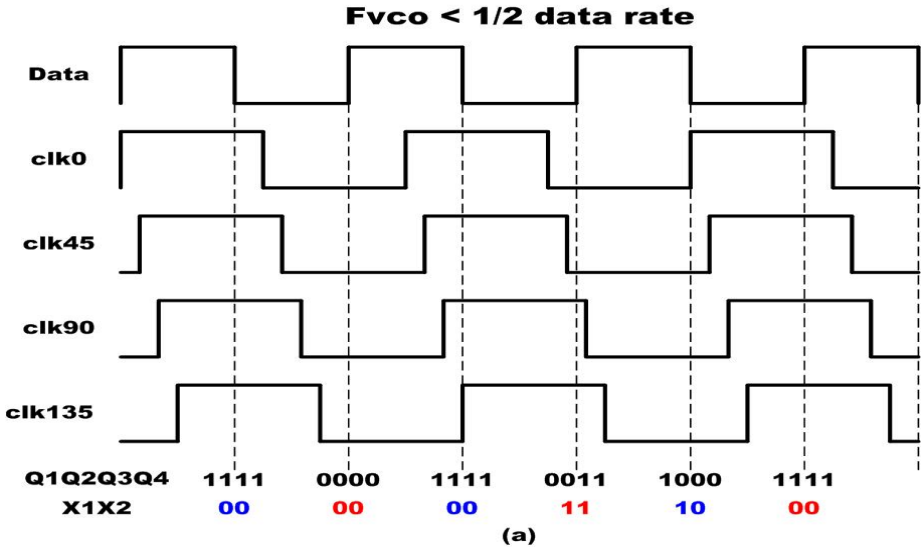


Fig. 4-10 Half-rate frequency detector

Fig. 4-11 shows the timing diagram for a periodic data signal with the clk0, clk45, clk90, and clk135. The notes X1 and X2 are needed to define four quadrants of phase which are 0,0, then 0,1, then 1,1, then 1,0, where high and low logic levels are represented by 1 and 0. When there is a frequency difference between input signal and clock output, the sampled quadrant will rotate around the circular phase diagram. Direction of this rotation determines whether half of the input signal frequency is faster or slower than the clock frequency as shown in Fig. 4-12.



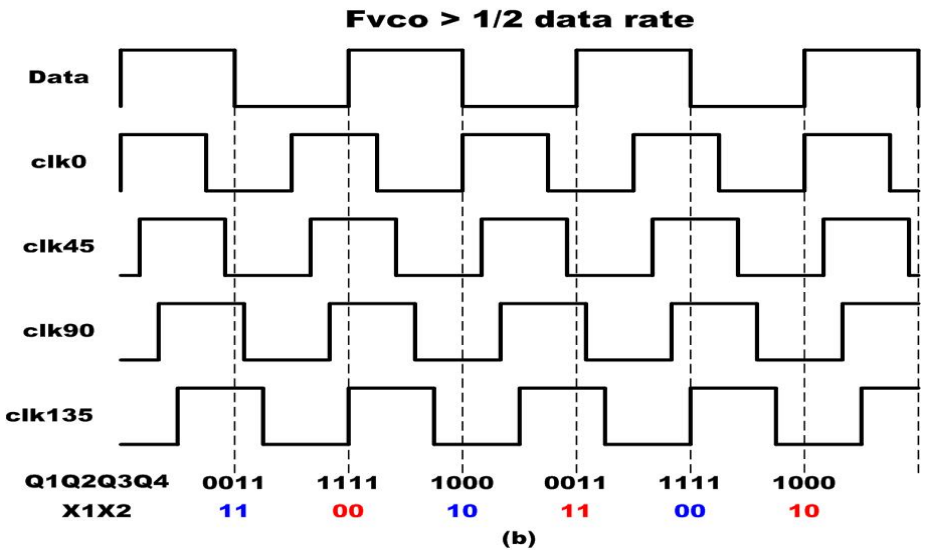


Fig. 4-11 Timing diagram of the FD (a) Fvco < 1/2 data rate (b) Fvco > 1/2 data rate

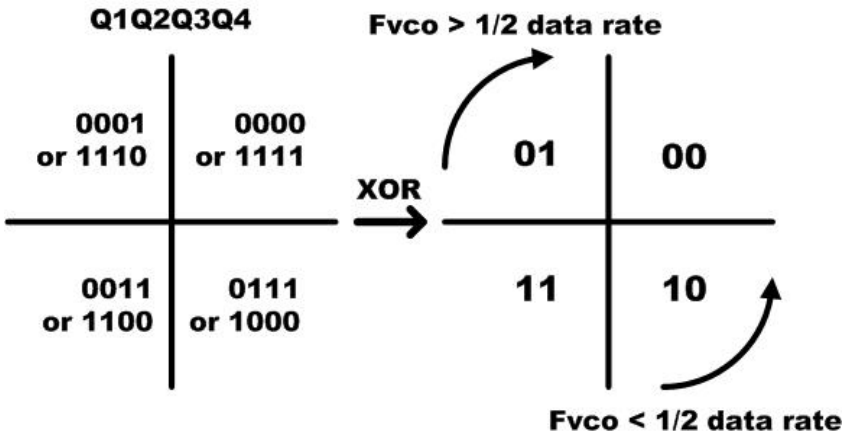


Fig. 4-12 Circular phase diagram

It can be seen from Fig. 4-12, when the clock frequency is lower than half of the input signal frequency, the sampled quadrant rotes counterclockwise and vice versa. The direction of rotation can be detected by monitoring the two consecutive quadrants like 1,0 and 0,0. If the sampled quadrant moves from the former to later, the clock is found to be slow and an up pulse is needed to speed up the clock. On the other hand, a transition from 0,0 to 1,0 quadrant denotes a fast clock and a down pulse should be generated to slow down the frequency of the clock. The up and down signals can be implemented as Fig. 4-13.

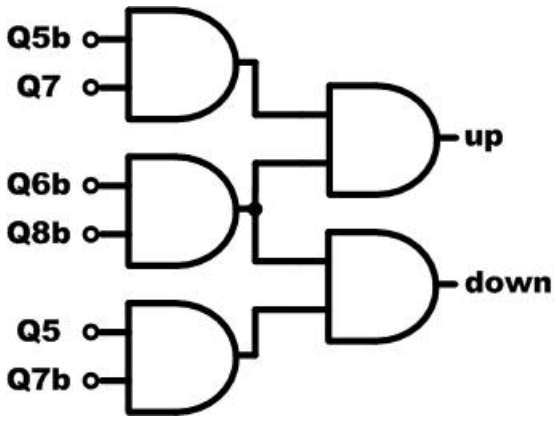


Fig. 4-13 Up and down generator

The half-rate frequency detector has two features. First, it will turn off automatically when frequency of the VCO is close to half of the input data rate. When the frequency detector turns off, the frequency error of the two signals is within a range between ±300ppm. Hence, the frequency detector does not affect the operation of the phase detector and there is no need to switch off the frequency detector in the lock state. It means that low jitter performance can be achieved. Second, the frequency detector has a large capture range for the NRZ input data. It can detect frequency derivation over ±30 percentage of the data rate. Thus, the tuning range of the VCO could be design larger.

4.3.3.3 Voltage Controlled Oscillator

A ring oscillator is implemented as VCO due to its wide tuning range. While LC topologies achieve a potentially lower jitter, their limited tuning range makes it difficult to obtain a target frequency without design and fabrication iterations. It is also important that the VCO must maintain a fixed frequency range under different process, temperature, and supply voltage variation. When VCO changes its center frequency due to above reasons, the VCO

control voltage must be able to tune it back to the desire frequency.

Since the CDR used in this thesis is operated at half rate with a frequency detector, the oscillator must generate four-phase output. A four-stage differential ring oscillator is used. Fig. 4-14 (a) shows the implementation of each delay stage [29]. Comparing to the VCO mentioned in section 3.2.3.4, the Kvco (Hz/V) is much lower when both VCO operate at 500MHz.

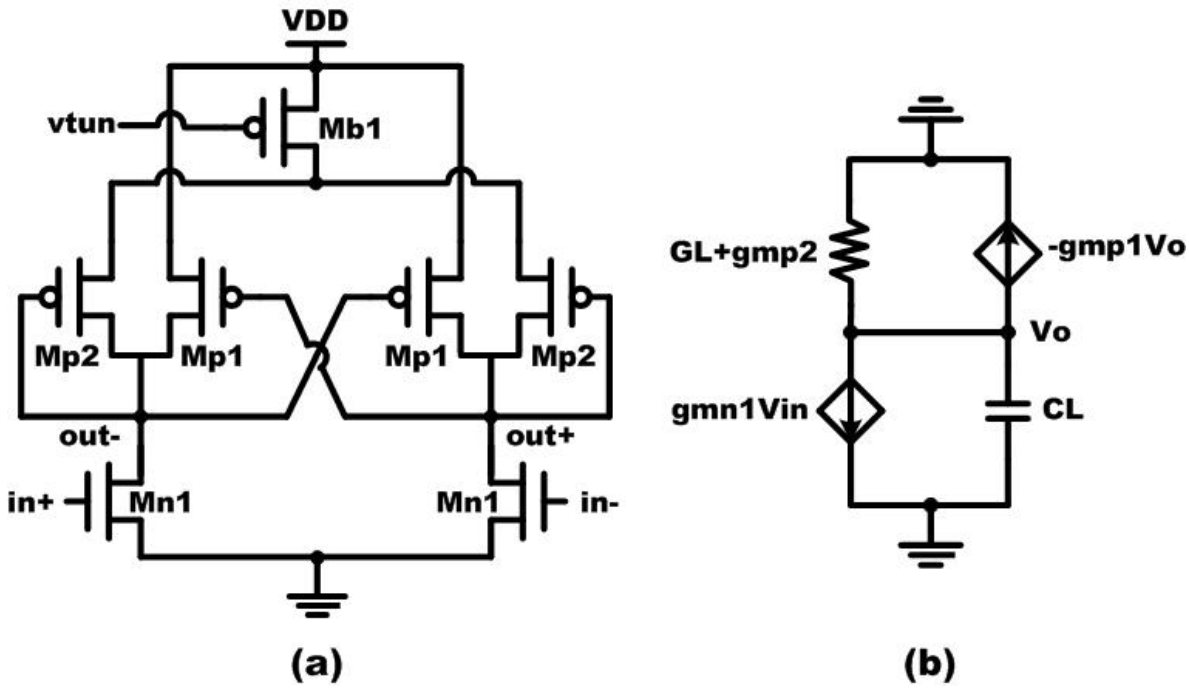


Fig. 4-14 (a) Delay cell (b) Half-circuit of the delay cell for small signal analysis

An NMOS input pair is used to achieve the high transconductance-to-capacitor (gm/C) ratio to operate at high frequency. Frequency tuning is achieved by tuning the transconductance of the diode-connected PMOS device Mp2. To derive the operating frequency of the oscillator, a half-circuit of the delay cell for small signal analysis in Fig. 4-14 (b) is considered.

The transfer function of the delay cell could be given as

$$A(s)=\frac{Vo}{Vin}=\frac{-g_{mn1}}{\left(-g_{mp1}+g_{mp2}+G_L\right)+sC_L} \tag{4-1}$$

$$G_L=g_{dn1}+g_{dp1}+g_{dp2}$$
$$C_L=C_{gsn1}+2C_{gdn1}+C_{dbn1}+C_{gsp1}+2C_{gdp1}+C_{dbp1}+C_{gsp2}+C_{dbp2}+C_{buffer}$$

where gm is the transconductance; gd is the channel conductance; Cgs is the gate-to-source capacitance; Cgd is the gate-to-drain capacitance; Cdb is the drain-to-bulk capacitance; C_{buffer} is the capacitance of output buffer.

To maintain the oscillation of a ring oscillator, the total phase shift of the delay cell chain is 180° and the overall gain is unity at the oscillation frequency. Therefore, the phase shift of each delay cell must equal to or more than 45° while the voltage gain of each delay cell is larger than $\sqrt{2}$. By equating the total voltage gain to be unity, the oscillation frequency of the ring oscillator can be derived as

$$f_{osc}=\frac{1}{2\pi}\sqrt{\frac{g_{mn1}^2-\left(-g_{mp1}+g_{mp2}+G_L\right)^2}{C_L^2}} \tag{4-2}$$

By controlling the gm of the diode-connected PMOS devices Mp2, the output frequency can be adjusted. At the maximum oscillating frequency, the negative transconductance gmp1 is just large enough to completely compensate the total load conductance (gmp1=gmp2 + G_L). At the minimum oscillating frequency, the diode-connected PMOS devices Mp2 are turned off (gmp2=0) and the drain conductance of devices Mn1 and Mp1 is much smaller than the negative transconductance (gmp1>>G_L). Consequently, the maximum frequency, minimum frequency, and operating frequency range can be calculated as follows:

$$f_{\max}\approx\frac{1}{2\pi}\frac{g_{mn1}}{C_L} \tag{4-3}$$

$$f_{\min} \approx \frac{1}{2\pi}\sqrt{\frac{g_{mn1}^2 - g_{mp1}^2}{C_L^2}} \tag{4-4}$$

$$f_{range} \approx f_{\max}\left(1-\sqrt{1-\left(\frac{g_{mp1}}{g_{mn1}}\right)^2}\right) \tag{4-5}$$

Besides, the duty-cycle of the VCO is another issue for half-rate CDR design. Thus, the duty-cycle corrector mentioned in section 3.2.3.4 is connected at the outputs of the VCO to ensure that the duty-cycle of the VCO will be 50%.

For linearity consideration, a linearization circuit is used and shown in Fig. 4-15 [28]. The input controlled voltage, Vctrl, is not directly applied to the VCO, but is converted to another voltage, Vtun, with a scaling-linear characteristic.

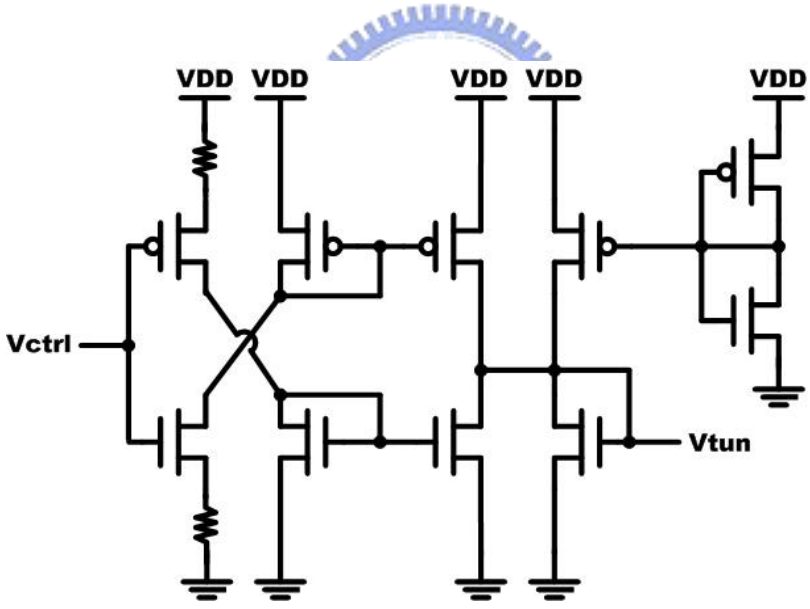


Fig. 4-15 Schematic of the linearization circuit

The product of this transfer curve with the VCO tuning sensitivity should be as constant as possible to achieve a linear overall tuning. The output voltage, Vtun, changes with the input voltage, Vctrl, which cover the linear gradation characteristic of the VCO. Fig. 4-16 shows the characteristic transfer curve of the linear circuit.

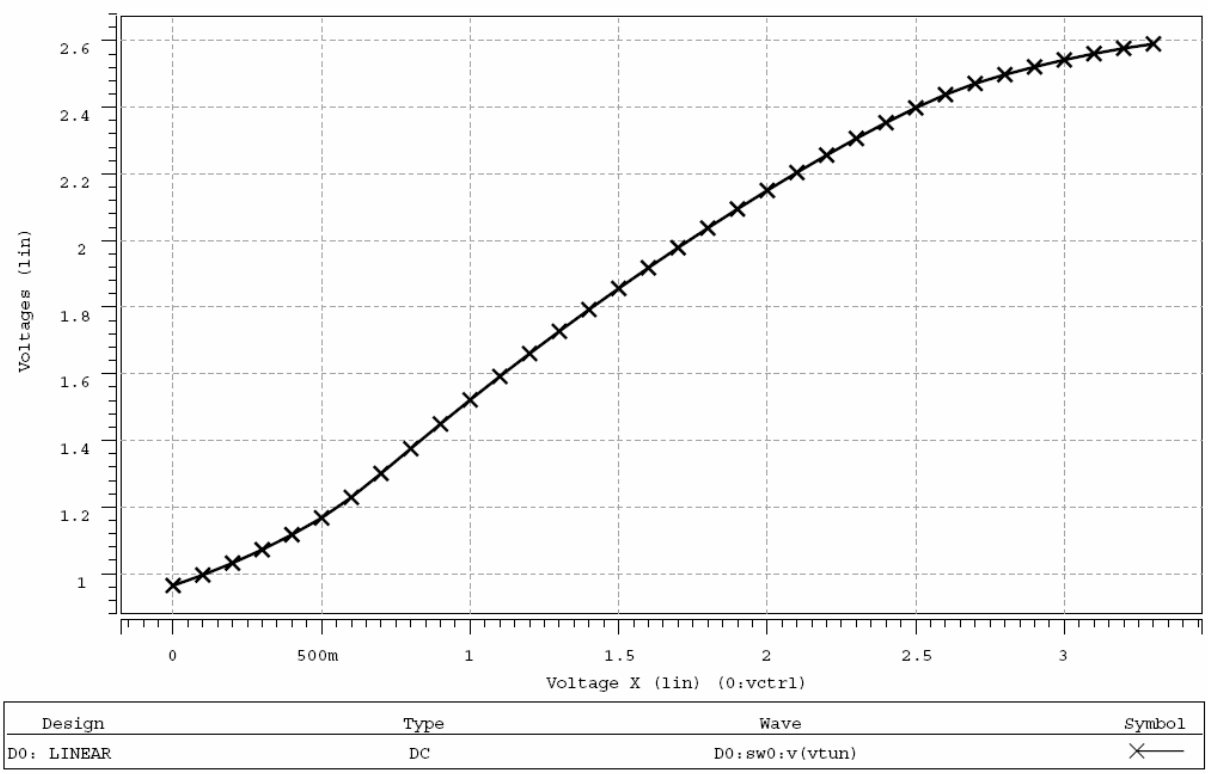


Fig. 4-16 Transfer curve of the linear circuit

The simulated transfer curve of the VCO is shown in Fig. 4-17. The VCO uses four delay buffer stages with the output frequency at 500MHz. The supply voltage is 3.3V. The gain of the VCO is -150MHz and the transfer curve is monotonic. The tuning range of the VCO is 395MHz~608MHz which falls inside the capture range of the frequency detector. It means that when power turns on, the CDR can act correctly.

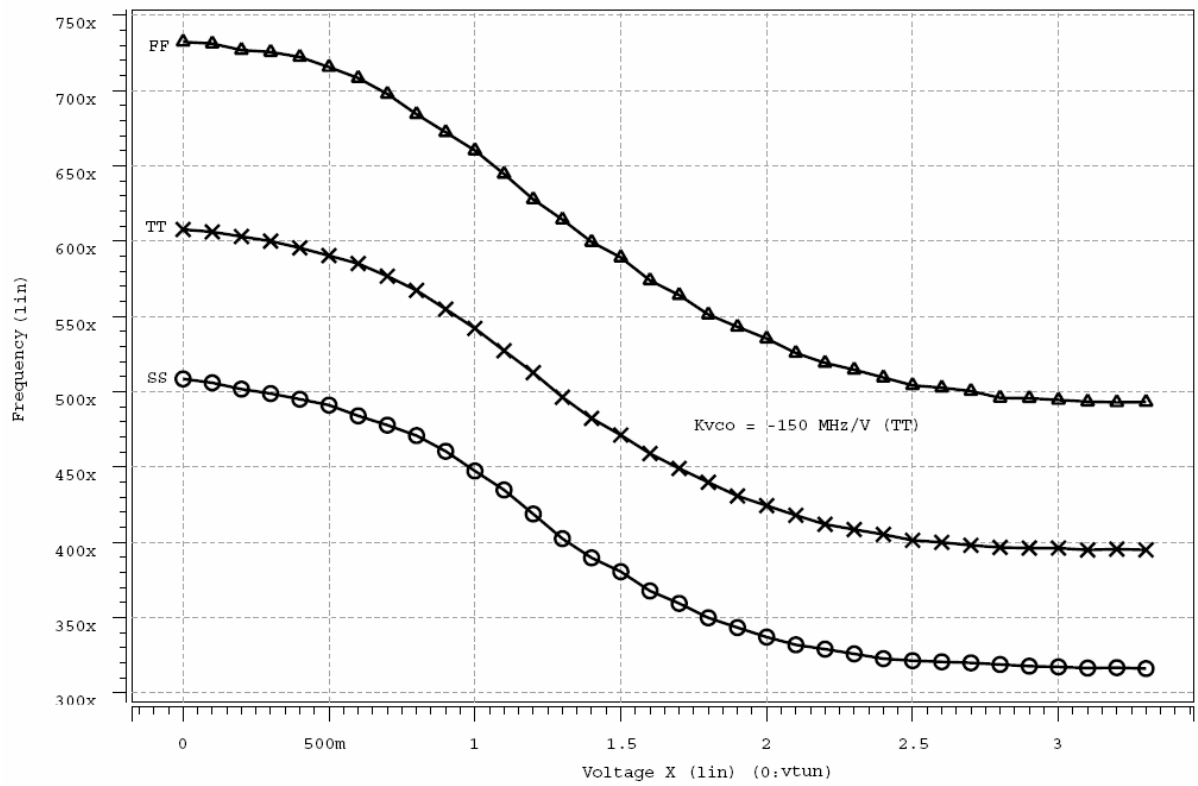


Fig. 4-17 Transfer curve of the VCO

4.3.4 CDR Parameter Design

In CDR parameter design, the frequency detector can be neglected because it dose not affect the CDR system after the lock is acquired. CDR is based on the charge pump switching characteristics as mentioned in section 3.2.4. The design flow of a CDR system can be summarized as follows [30]:

(1) Depending on the desired noise and transient performance, determine the loop bandwidth BW. Usually, BW is determined by the specification.

(2) Determine Kvco by measuring VCO test keys or simulating a VCO used in your design or referring to the data sheets of the employed commercial VCO.

(3) If the filter is off-chip, set Ipd to be around 100μA to 1mA. If an on-chip filter is employed, decrease the value of Ipd so that reasonable trade off between chip area and pump current could be reached.

(4) With BW, Ipd, and Kvco determined, R_1 can be calculated.

(5) Determine the damping factor by the jitter peaking of the jitter transfer curve. Typically, a CDR system exhibits a large damping factor. Thus, C_1 can be calculated.

(6) If a second-order loop filter is used, determine the compensation capacitor by the system phase margin.

The parameters used in the CDR are listed in Table. 4-1. The MATLAB simulation results can be shown in Fig. 4-18 and Fig. 4-19.

Table. 4-1 Parameters of the CDR

Technology	0.35μm 2P4M CMOS
Function	CDR
Supply Voltage	3.3V
VCO Frequency	500MHz
PDCP Current	50μA
FDCP Current	2mA
VCO gain	150MHz/V
Loop Bandwidth	2MHz
Damping Factor	1.5
C_1	427.46pF
R_1	1.68kΩ
C_2	11.84pF
Phase Margin	70°
Frequency Range	395MHz~608MHz
Power	135mW@500MHz

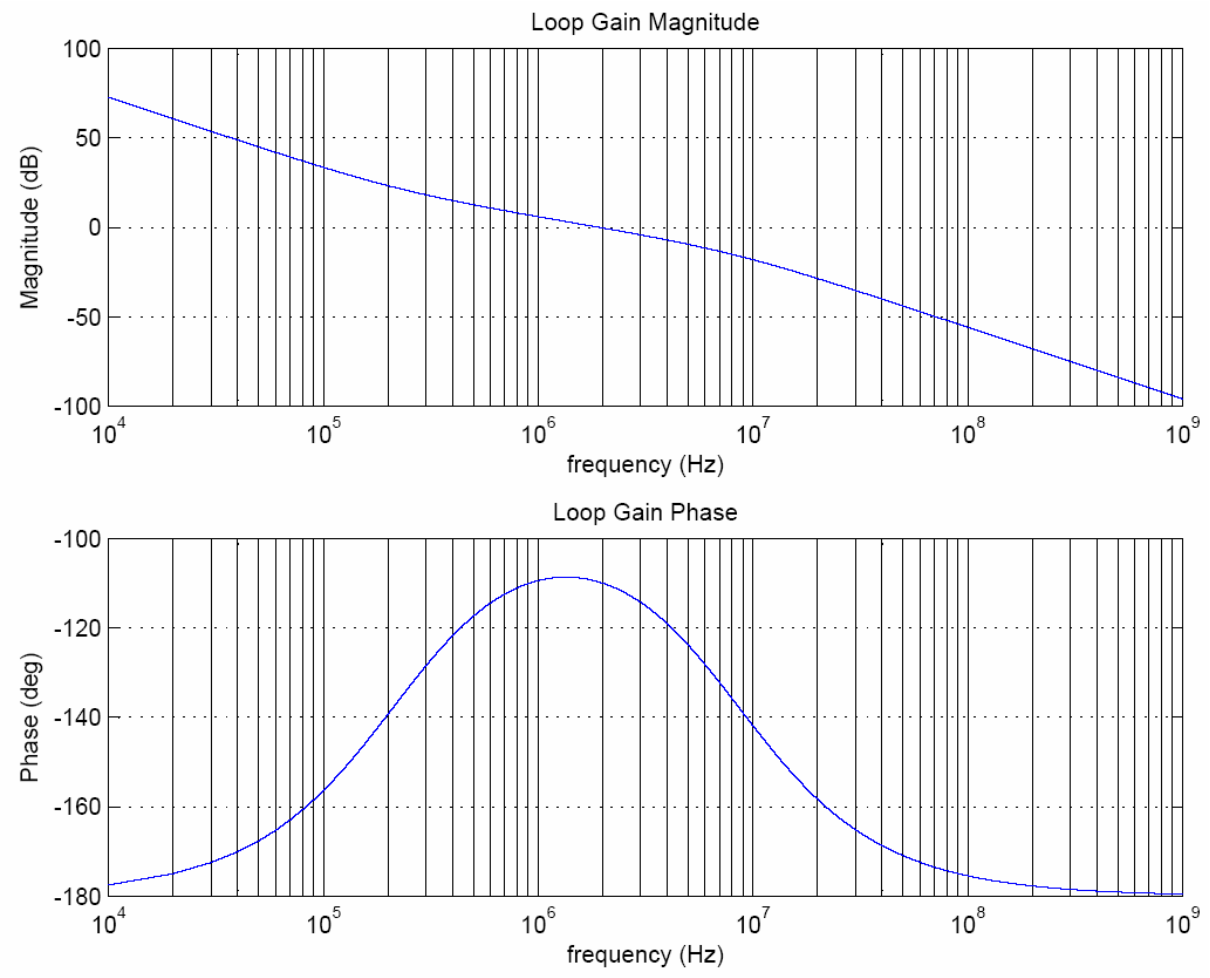


Fig. 4-18 Open loop simulation using parameter in Table. 4-1

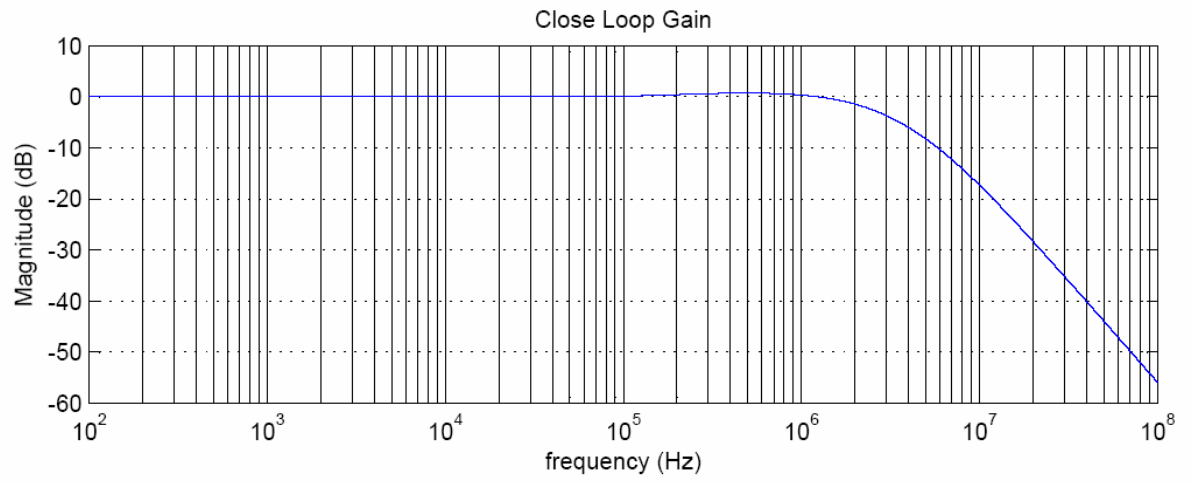


Fig. 4-19 Close loop simulation using parameter in Table. 4-1

Fig. 4-20 shows the control voltage of the VCO. It shows that the frequency detector can

pull the frequency close enough for the CDR loop to lock within 7.5μs. Fig. 4-21 shows the up and downb signals of the frequency detector. It shows that when CDR is in the lock state, the frequency detector turns off. Fig. 4-22 shows the retimed even and odd NRZ data with the maximum run length of 7 and the retimed clock at 500MHz.

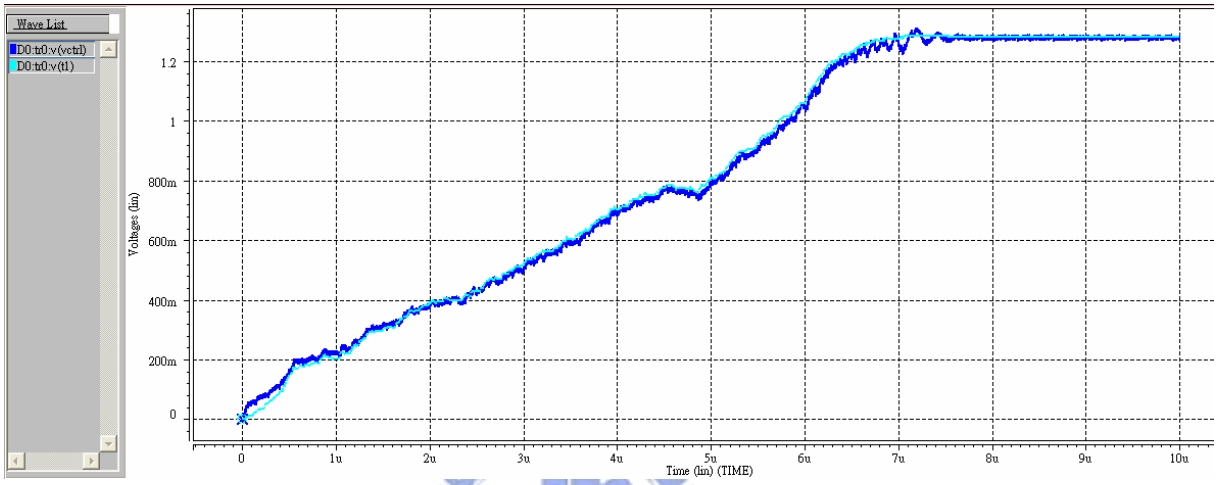


Fig. 4-20 Control voltage of the VCO

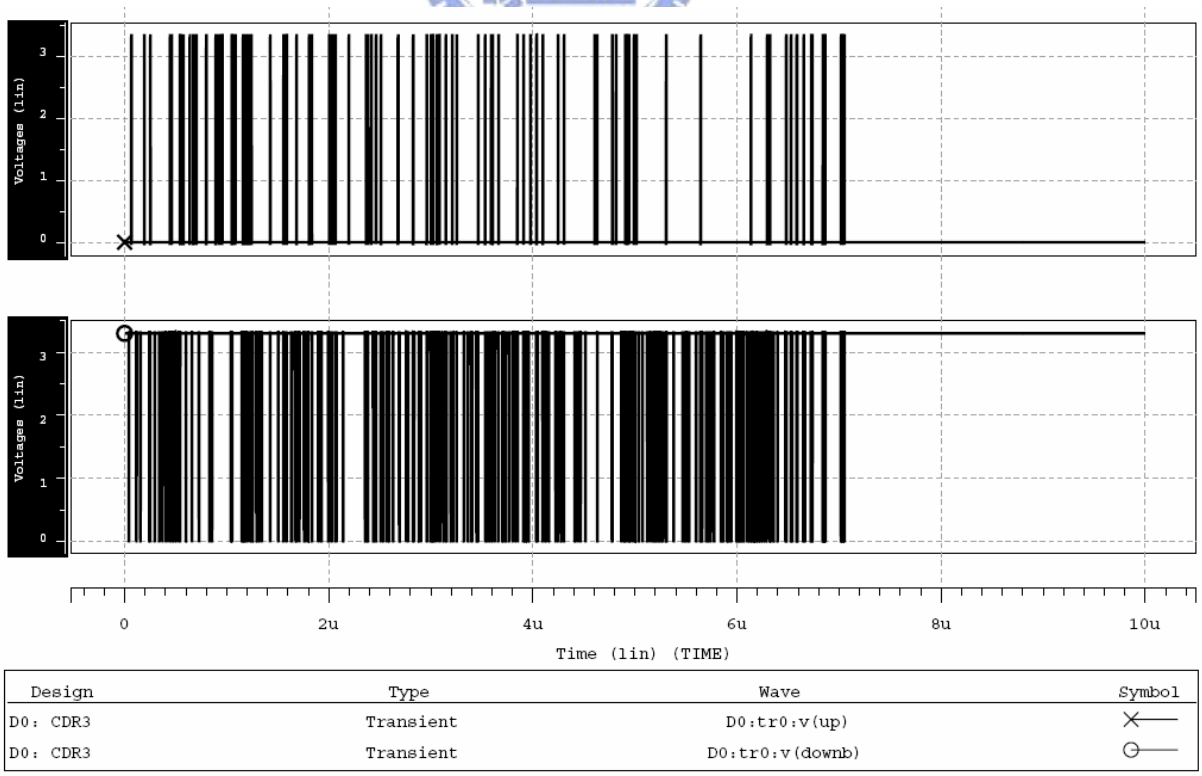


Fig. 4-21 Up and downb signals of the frequency detector

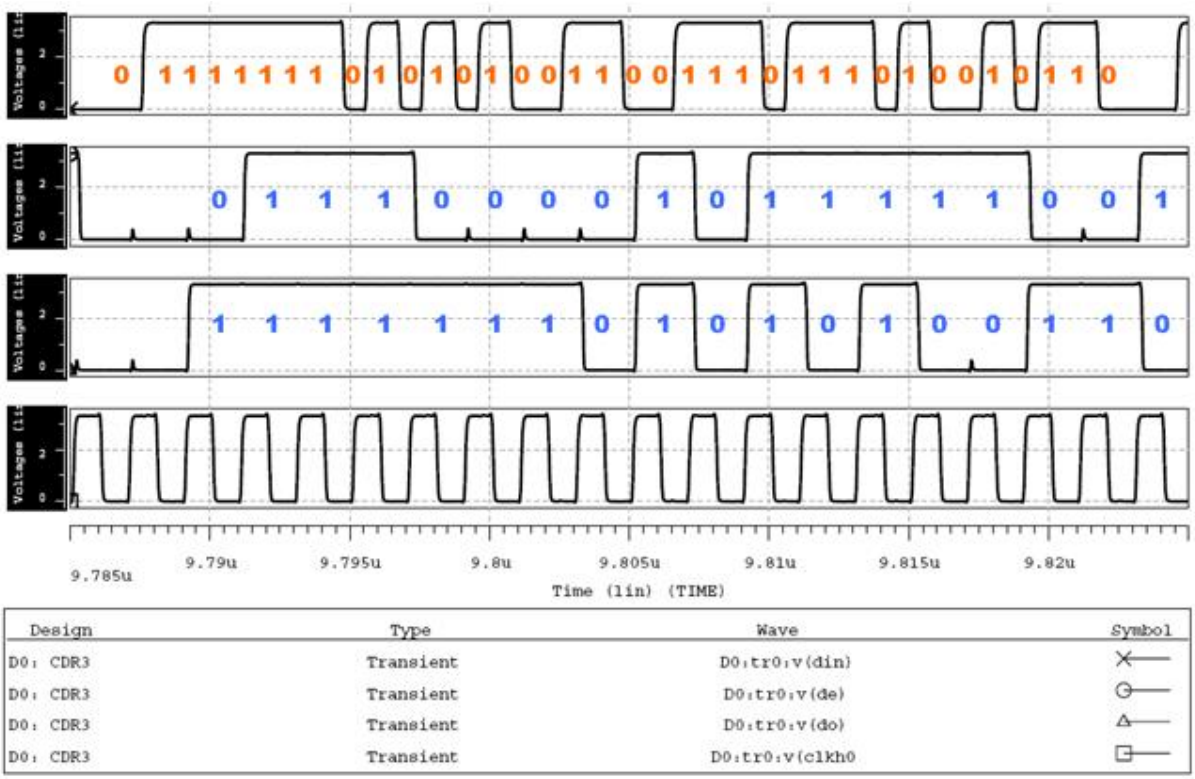


Fig. 4-22 Retimed even and odd data and Retimed clock

4.4 De-Multiplexer

The asynchronous tree-type de-multiplexer architecture overcomes device limitations by using both rising and falling clock edges, as shown in Fig. 4-23 [31]. As a result, a tree-type de-multiplexer is able to operate at half the speed of the data rate. The small numbers of high-speed-operated devices in the tree-type architecture do make it more suitable for high speed operations with low power consumption.

As shown in Fig. 4-24 (a), a 1:2 DEMUX module does not require precisely controlled clock distribution; Fig. 4-24 (b) is its timing diagram. It not only generates the output data but also an optimized clock for the next stage. An asynchronous tree-type 2:8 de-multiplexer is obtained simply by connecting such 1:2 DEMUX modules.

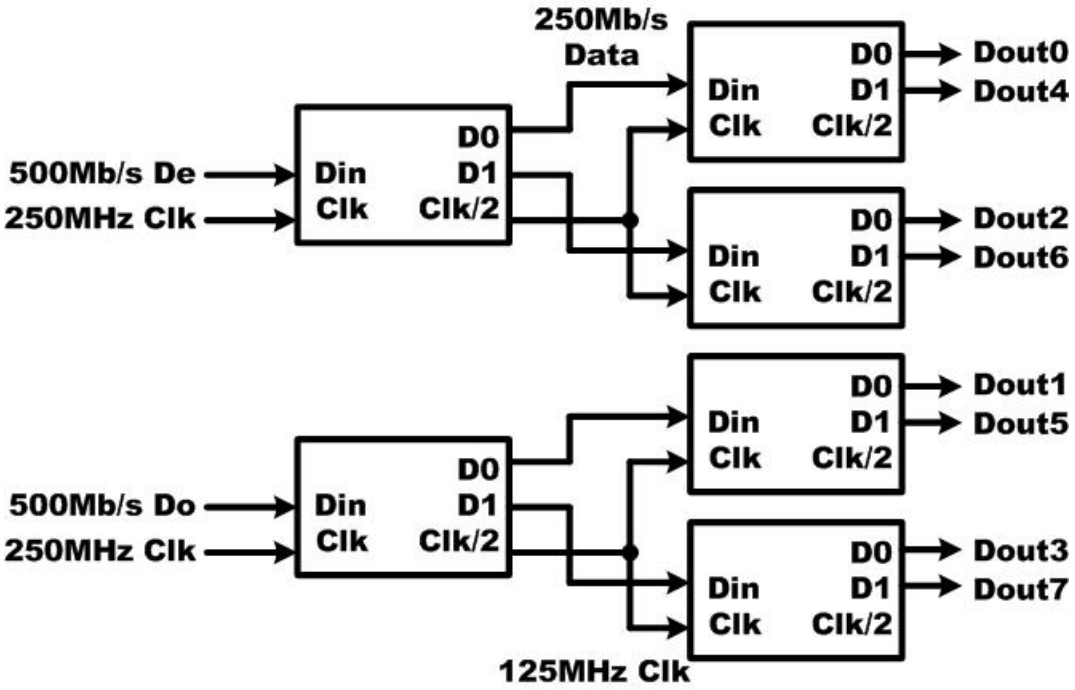


Fig. 4-23 Asynchronous tree-type 2:8 de-multiplexer

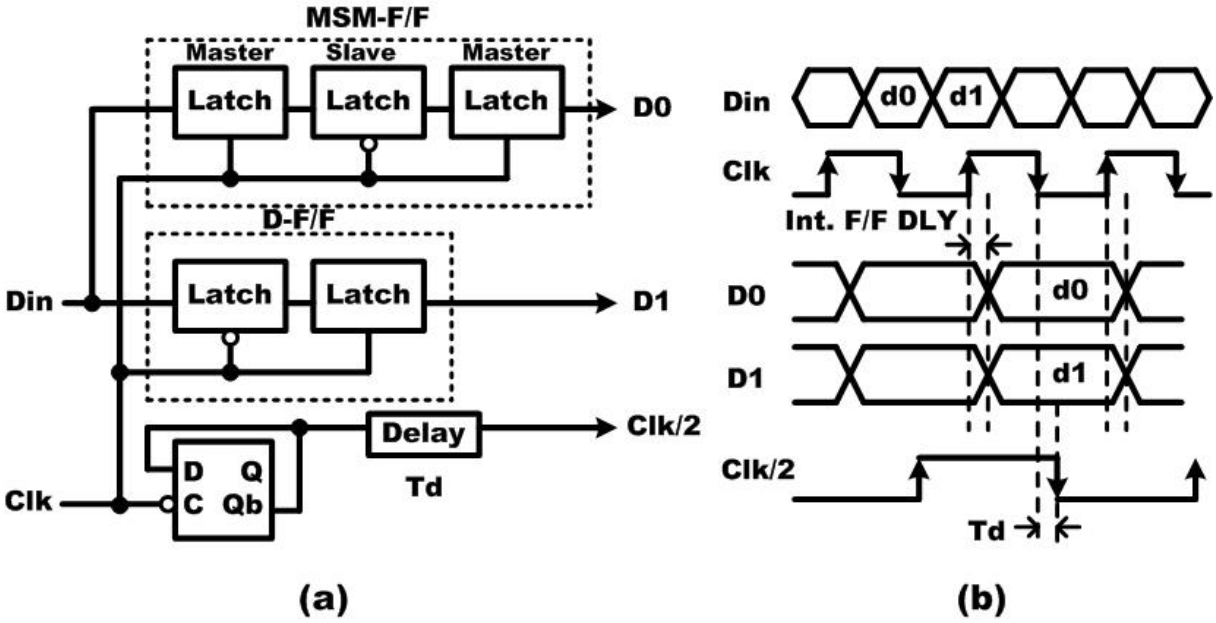


Fig. 4-24 (a) 1:2 DEMUX module and (b) timing diagram

The module contains a clock divider for the next stage, as well as a D-flip-flop (D-F/F) and a master-slave-master type flip-flop (MSM-F/F) for data. The module operates at half the

clock speed of the input data rate. This is because this module operates using both rising and falling clock edges. The D-F/F outputs odd data streams at rising edges of the clock, and the master-slave latches in the MSM-F/F latch even data streams at falling edges of the clock. These latched data are output at rising edges of the clock by the second master latch in the MSM-F/F. In this way, two bit output data D0 and D1 are synchronized with the rising edges of the input clock. A divided clock Clk/2 is generated at the falling edges of the input clock. With the delay circuit, which adjusts the timing between D0/D1 and Clk/2, the timing of the Clk/2 for each next stage is set at the precise center of each D0/D1 eye. That is to say, the 1:2 DEMUX module generates optimized timing between the divided clock and the data for the next stage DEMUX modules.

4.5 Receiver Simulation Results

Fig. 4-25 top graph is the time domain front-end received signal with transmitter pre-emphasis mentioned in chapter 3 and the differential swing is about 350 mV and down graph shows the corresponding output signal of the slicer, the limited received signals are being amplified to the full scale. Fig. 4-26 top graph shows the control voltage of the VCO in the lock state and down graph shows the CDR data input (din) with the maximum run length of 11 and the retimed clock (clkh0). Since the ripple on the control voltage is the source of the jitter, reducing the amplitude of the control voltage in the lock state is necessary. In this work, the amplitude of the control voltage is about 30mV. After the CDR is in the lock state, the input serial data stream with 1Gbps is divided into eight parallel channels with 125Mbps, as shown in Fig.4-27. It shows the CDR data input (din) and eight parallel data outputs of the de-multiplexer (Dout0~Dout7).

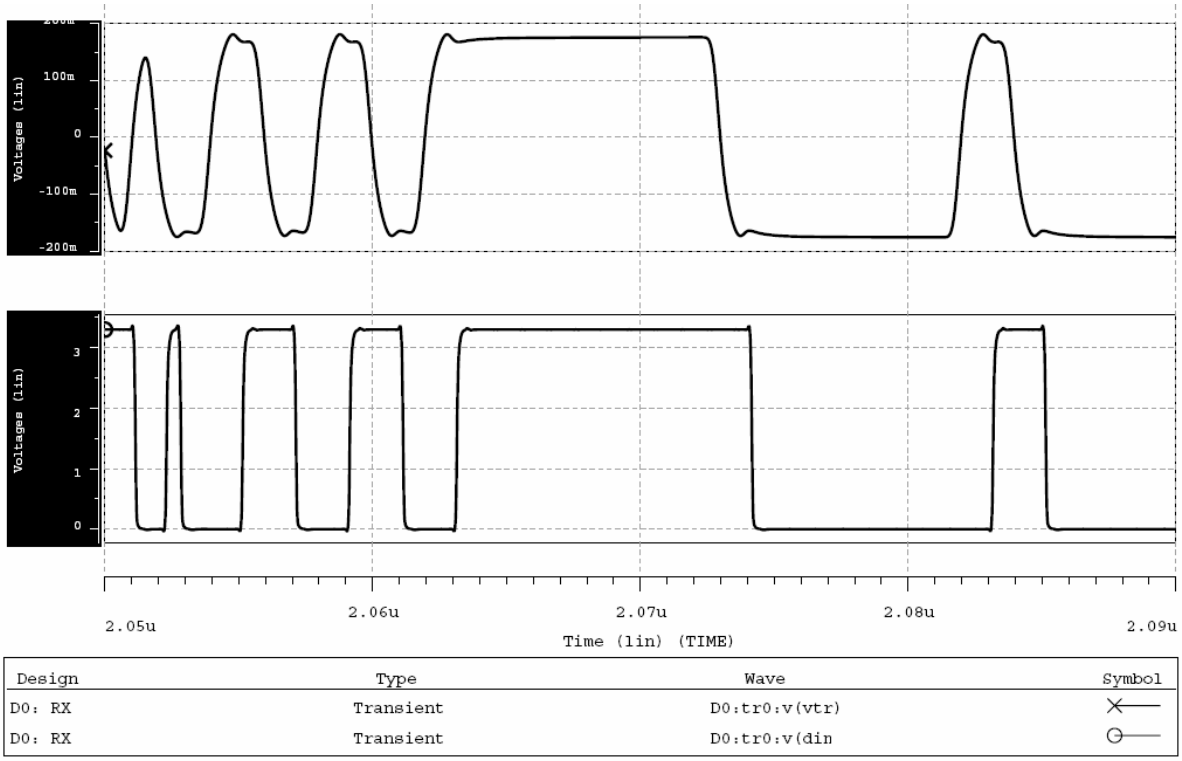


Fig. 4-25 Time domain of the received signal and output of the slicer

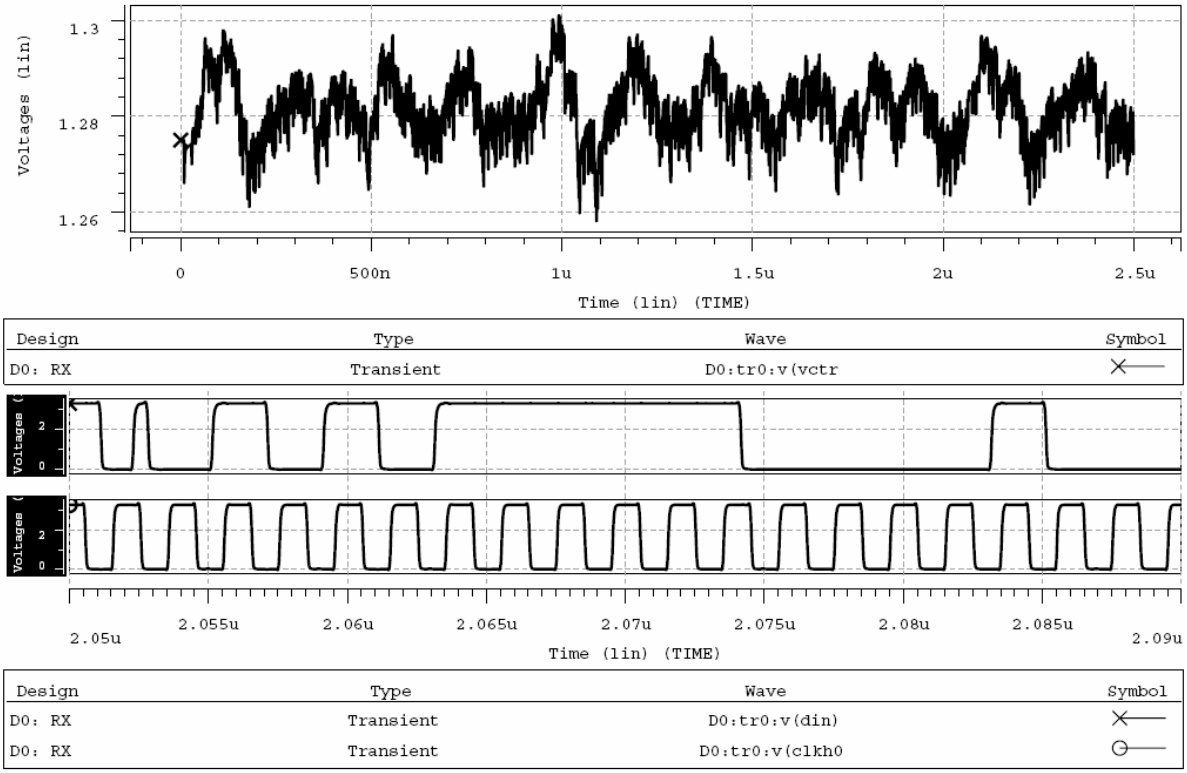


Fig. 4-26 CDR in the lock state and retimed clock

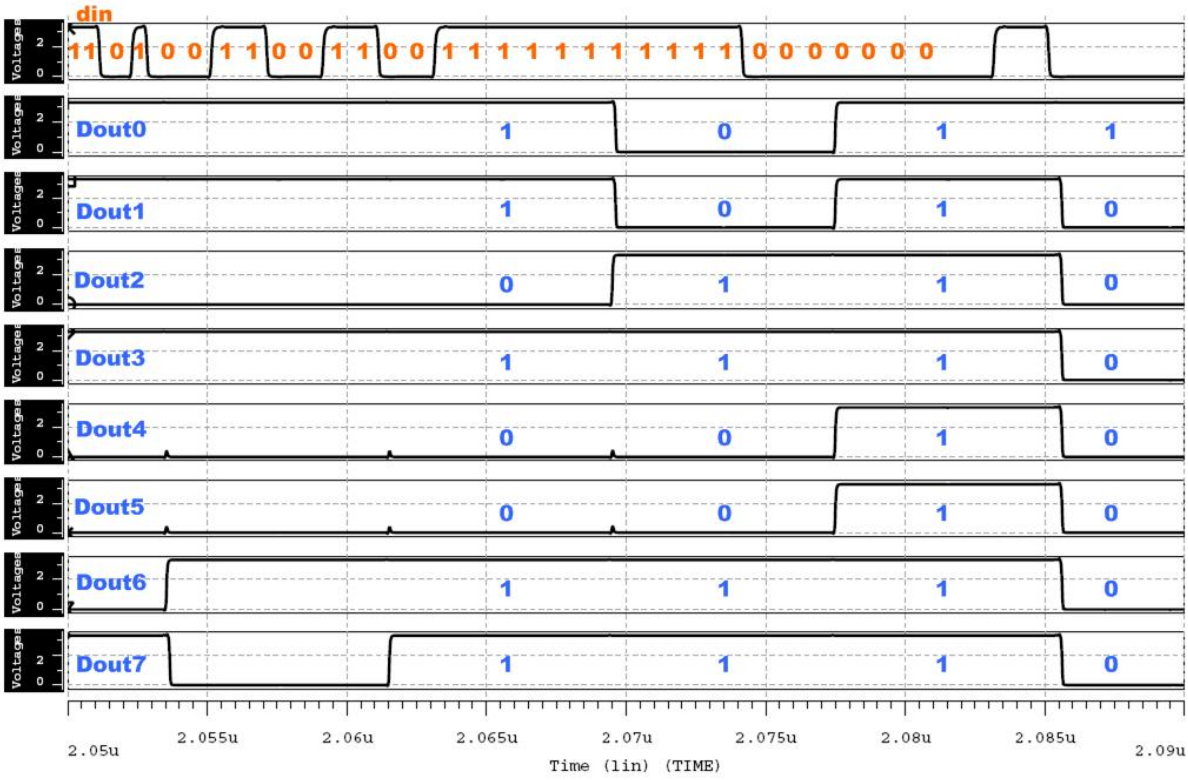


Fig. 4-27 Eight parallel data outputs of the de-multiplexer

Chapter 5

Experimental Results

5.1 Experimental Setup

The transmitter chip is implemented in a TSMC 0.35μm 2P4M CMOS process. The chip (including the bonding pads) occupies 1.5 x 1.5 mm^2. The layout has been carefully treated to reduce the noise effects. For example, the analog circuits are placed as far as possible from the digital parts. The double guardrings are added to reduce the substrate noise from the digital part. The power lines are separated from digital, analog, the mux, and the output driver. The decoupling capacitor to stabilize the power line is added as much as possible in the free spaces. Fig. 5-1 shows the chip die micrograph with the major functional blocks outlined. The block diagram of transmitter test environment is shown in Fig. 5-2. The power supply (Agilent E3614A) provides the required voltage sources, analog (Vdda), digital (Vddd), mux (Vddmux), and output driver (Vdddri) on the test board. The pulse generator (HP 8133A) provides the reference clock signal (Ref_clk) to the PLL input. The PLL output clock signal, Clk[0] , is fed to the Digital phosphor Oscilloscope (TEK TDS 754D) to view the waveform

and to the Digital Signal Analyzer (TEK DSA 601A) to monitor the jitter performance. The transmitter outputs, TxD+ and TxD-, are viewed through the Wide-Bandwidth Oscilloscope (Agilent 86100B).

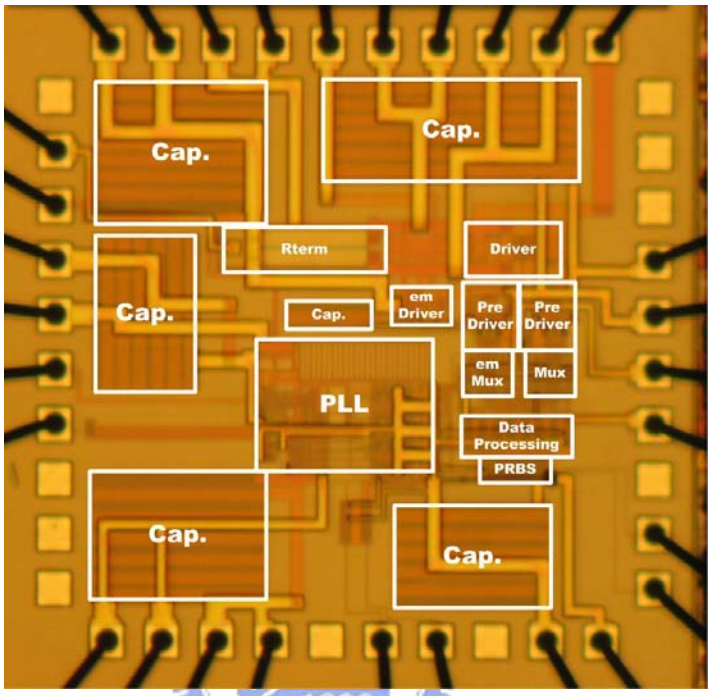


Fig. 5-1 Transmitter chip micrograph

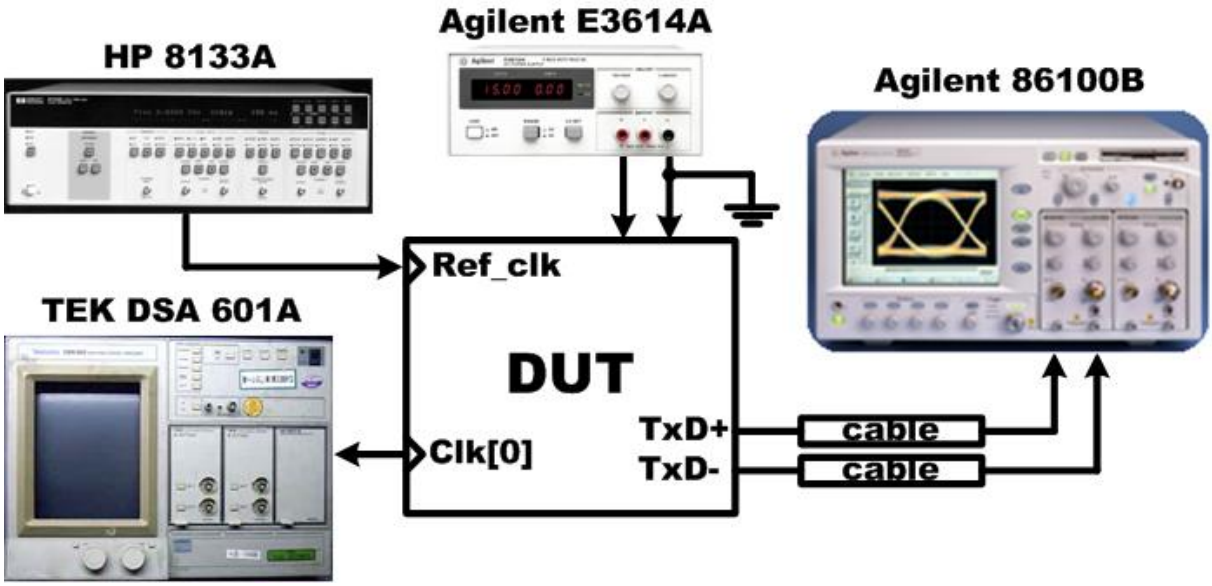


Fig. 5-2 The experimental setup of the transmitter

5.2 Print Circuit Board Layout

The print circuit board (PCB) for testing is shown in Fig. 5-3. The analog, digital, mux, and driver are powered by separate supply voltage and several capacitor arrangements provide decoupling of both low-frequency noise with large amplitudes and high-frequency noise with small amplitudes. Besides, the high-frequency signal traces are made as short as possible. Another challenge is in placing the discrete components and terminations close to the chip to reduce associated parasitic and signal reflections.

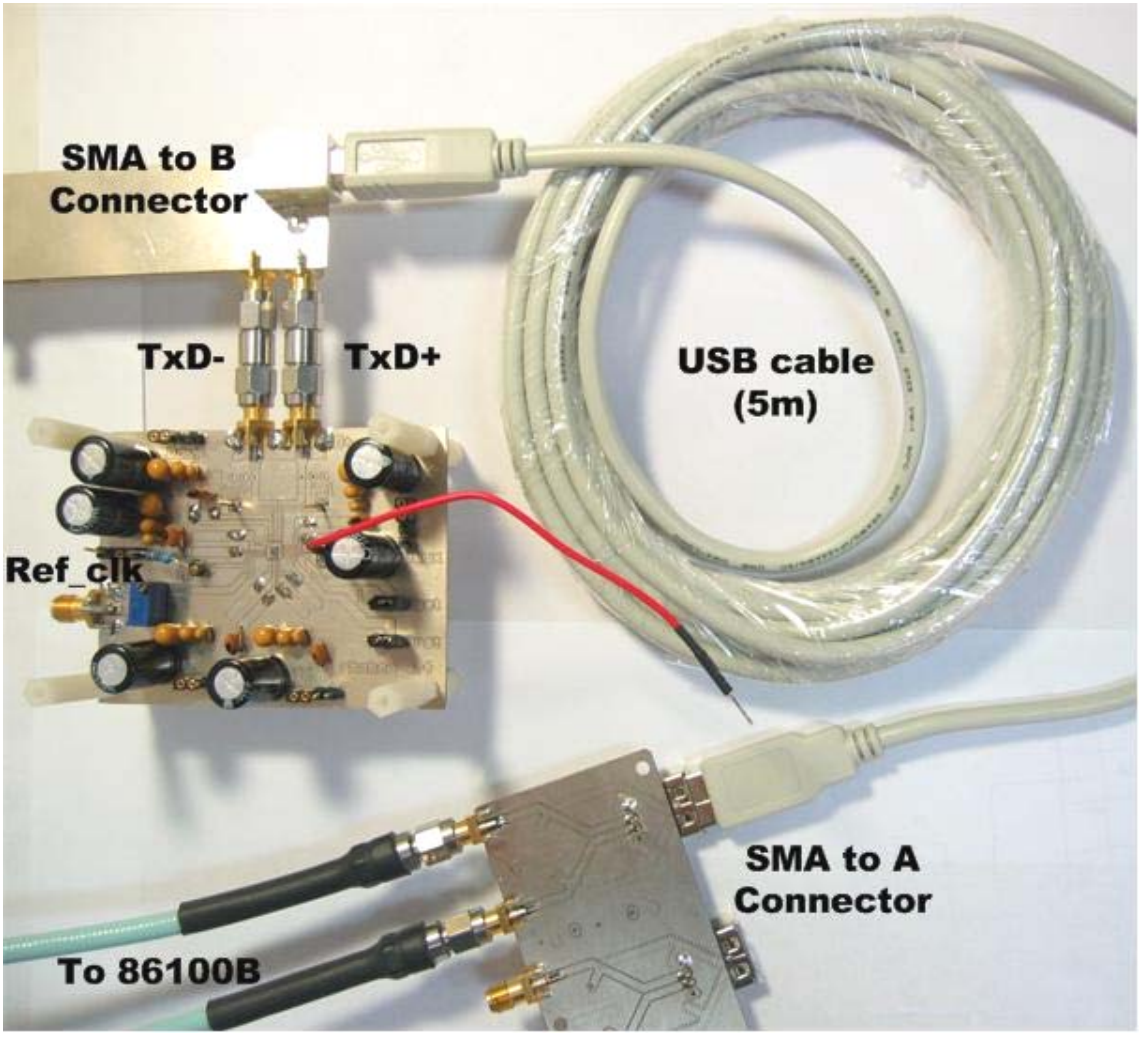


Fig. 5-3 The print circuit board for testing

5.3 Experimental Results

According to Table. 3-1, the PLL used for transmitter to generate multiple phases should have output frequency of 125MHz. Fig. 5-4 shows the measured RMS and peak-to-peak jitter of PLL output signal at 125MHz, which are 11.42ps and 82ps, respectively. Fig. 5-5 shows the time domain output clock of PLL at 125MHz. The measured output frequency range of PLL is about 23 to 268 MHz which is well within the process corner.

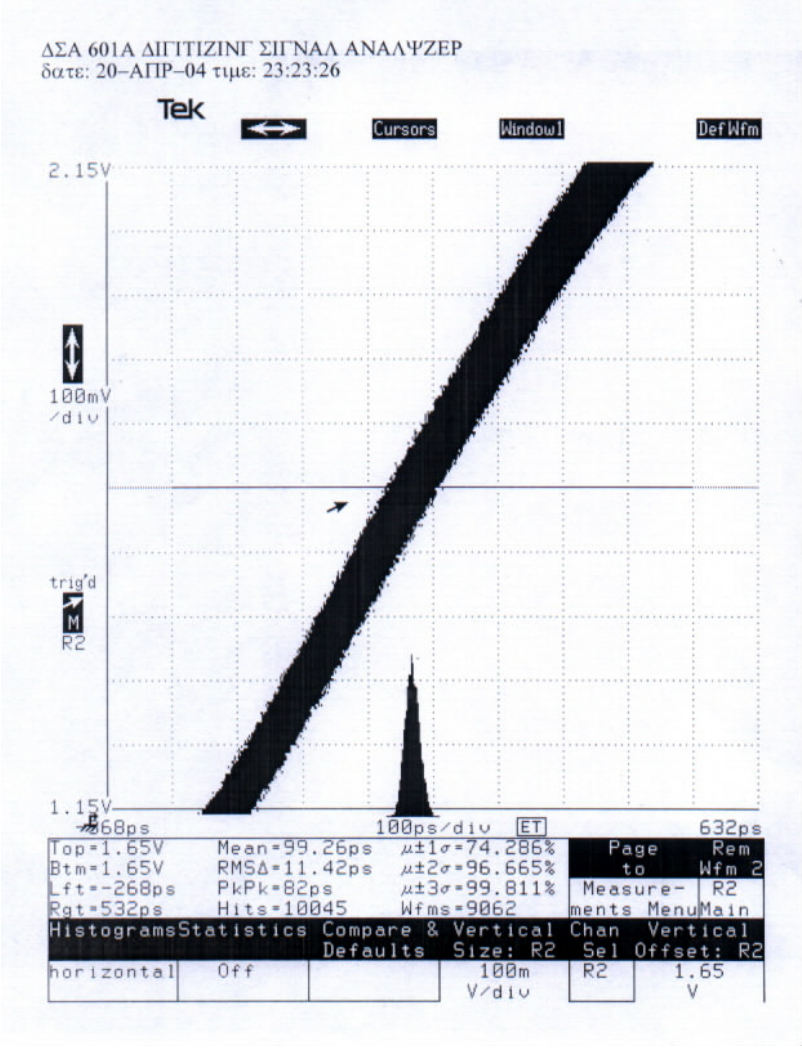


Fig. 5-4 Jitter histograms of the PLL at 125MHz

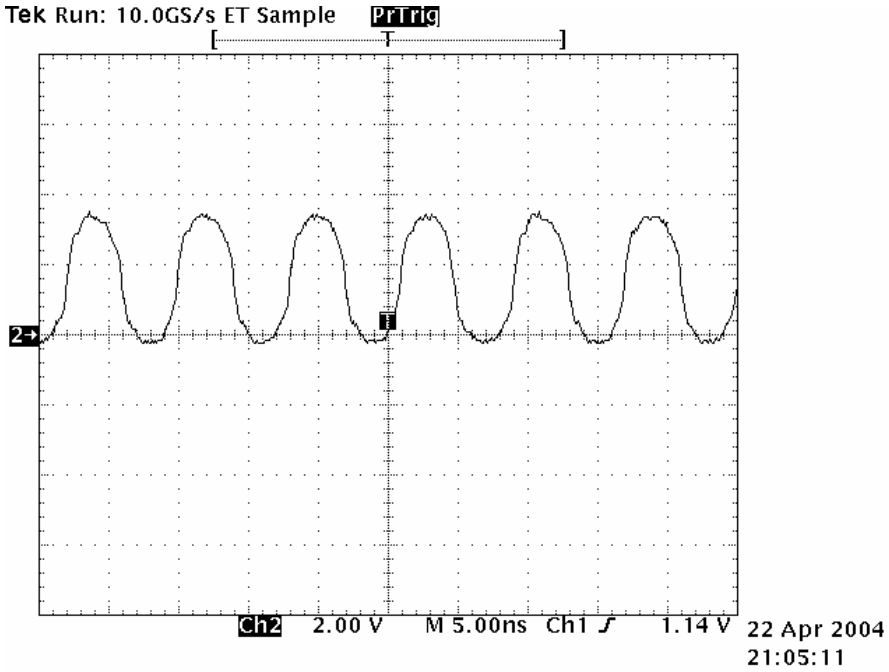
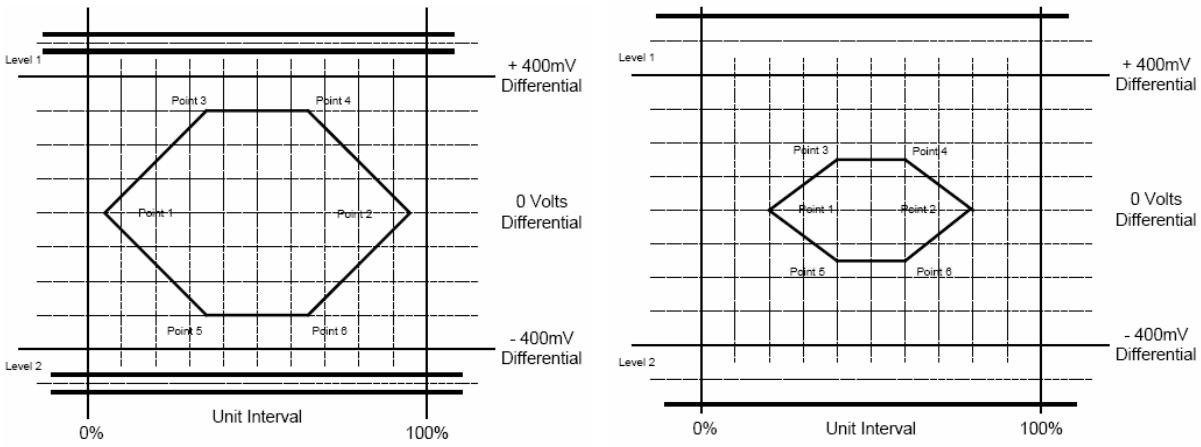


Fig. 5-5 Measured PLL output waveform

Fig. 5-6 shows the specifications apply to USB high-speed mode signaling [3]. All bits, including the first and last bit of a packet, must meet the eye pattern requirements for timing and amplitude. Fig. 5-6 (a) shows the transmitter output eye mask at near-end and Fig. 5-6 (b) shows the receiver input eye mask at far-end (through 5m USB cable).



(a) **(b)**

Fig. 5-6 (a) Transmitter output eye mask (b) Receiver input eye mask

Table. 5-1 and Fig. 5-7 show the measured cable loss of 5m USB cable. The measured results include two SMA to connector board loss. It can be shown that the USB cable is a low pass system and the attenuation at 500MHz is 7.74dB. It attenuates more compared to Table. 2-1 and Fig. 2-2.

Table. 5-1 Measured cable loss of 5m USB cable

Frequency (MHz)	Attenuation/5m cable (dB)
12 MHz	1.25
24 MHz	1.58
48 MHz	2.11
96 MHz	3.11
200 MHz	4.39
400 MHz	7.21
500 MHz	7.74
600 MHz	8.66

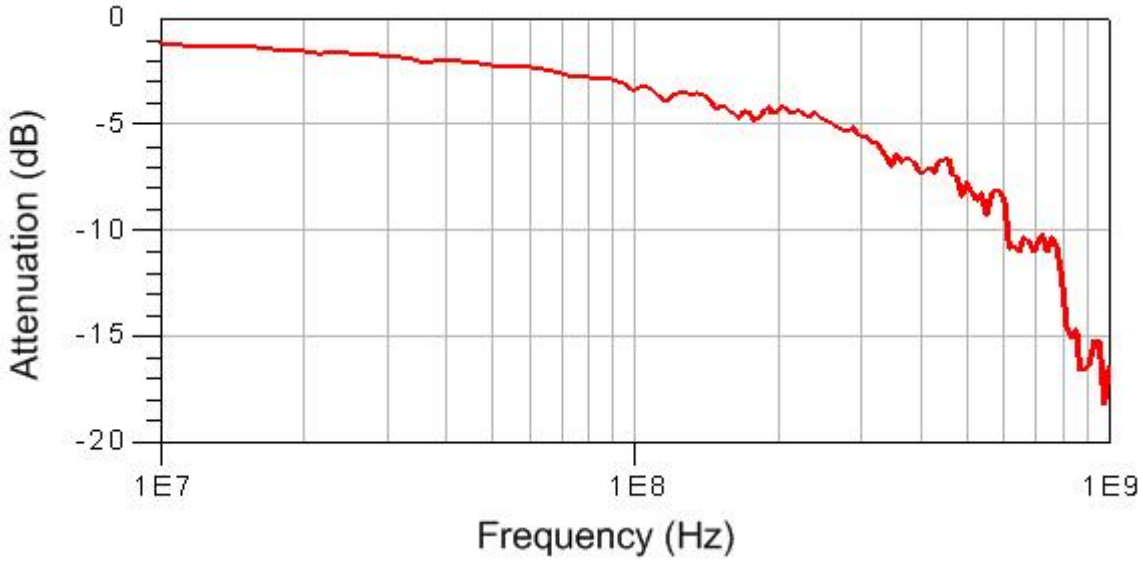


Fig. 5-7 Measured cable loss of 5m USB cable

We fixed the data rate at 1Gbps when data driver current and pre-emphasis current are equal to 13mA and 4mA, respectively. Then, we measured the eye diagram at different length of the cable, 1.8m, (1.8+1.8)m, and (1.8+1.8+1.8)m. The symbol "+" means the connector between two 1.8m USB cables, as shown in Fig. 5-8. It will introduce some loss and reflection.

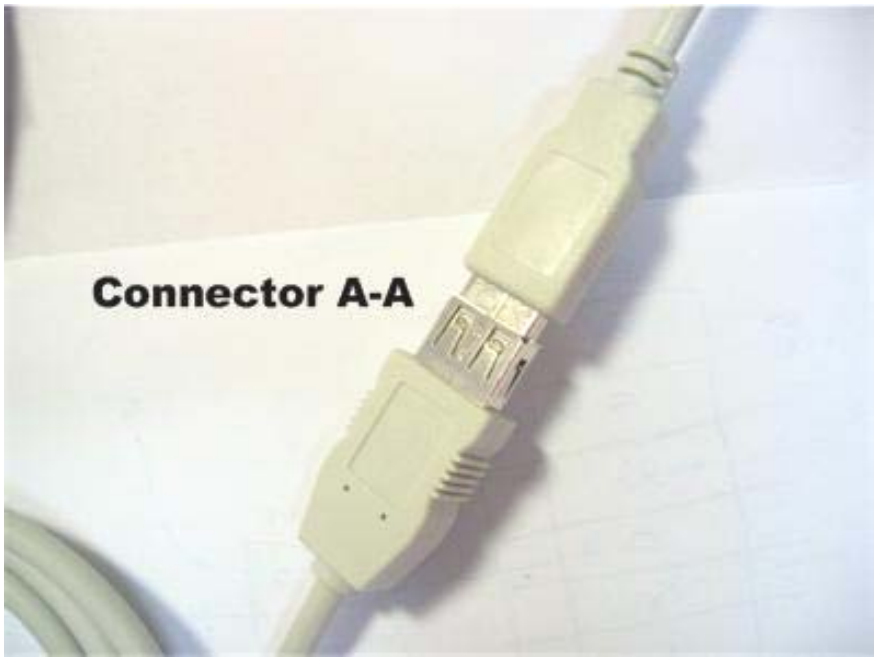


Fig. 5-8 The connector between two 1.8m USB cable

Fig. 5-9 and Fig. 5-10 show the measured eye diagram without pre-emphasis and with pre-emphasis of the transmitter operating at 1Gbps at near-end. The test pattern is a 2^7-1 bits pseudo-random-bit sequence (PRBS). Fig. 5-11 ~ Fig. 5-16 show the measured eye diagram without pre-emphasis and with pre-emphasis of the transmitter operating at 1Gbps going through 1.8m, (1.8+1.8)m, and (1.8+1.8+1.8)m USB cable, respectively. It can be shown that the eye diagram of the transmitter with pre-emphasis is bigger than that without pre-emphasis. Table. 5-2 summarizes the results of the measured transmitter performance.

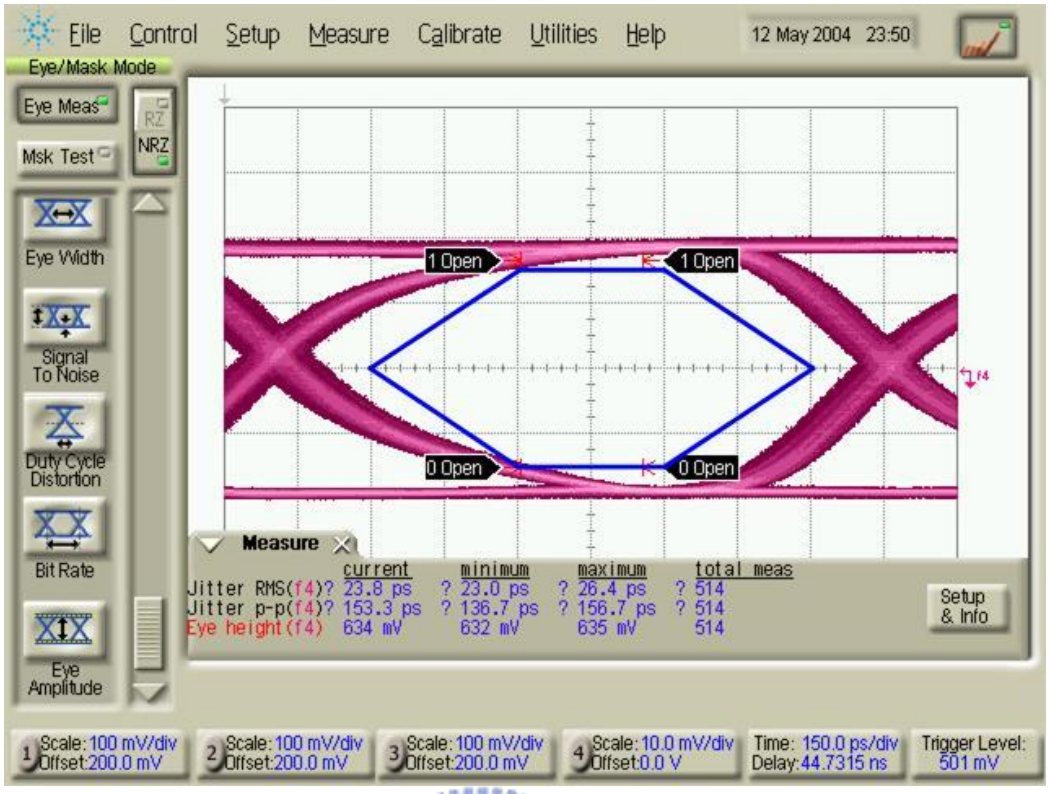


Fig. 5-9 Tx output waveform without pre-emphasis at 1Gbps

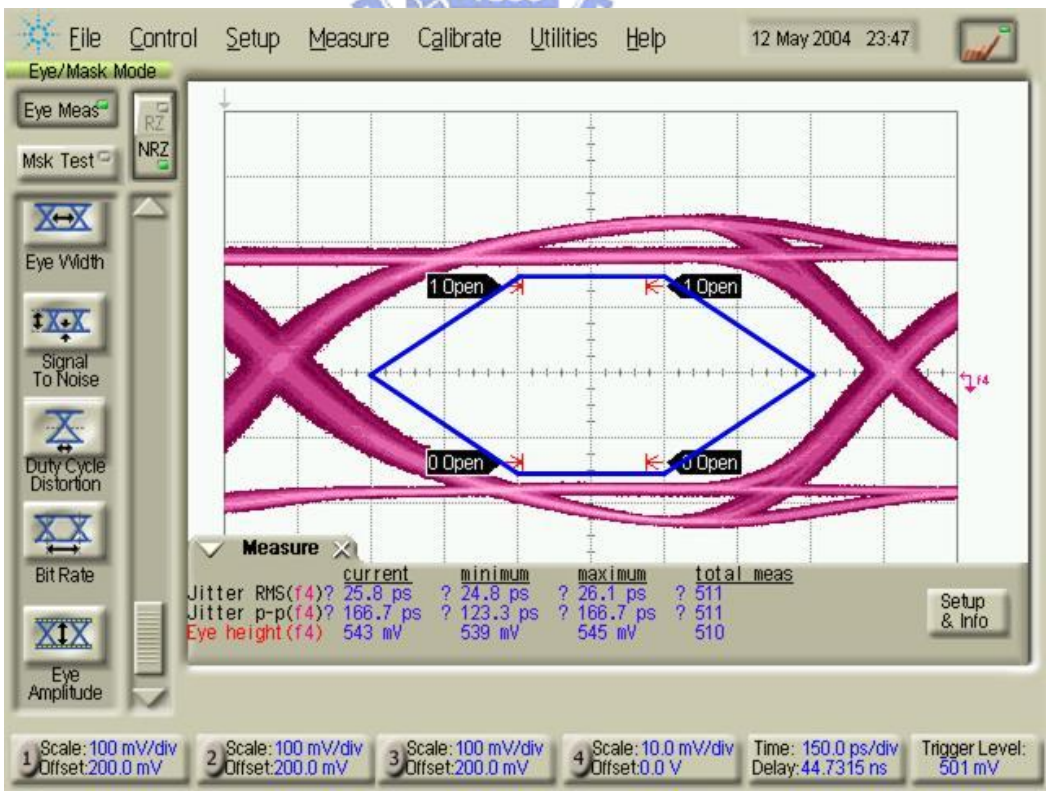


Fig. 5-10 Tx output waveform with pre-emphasis at 1Gbps

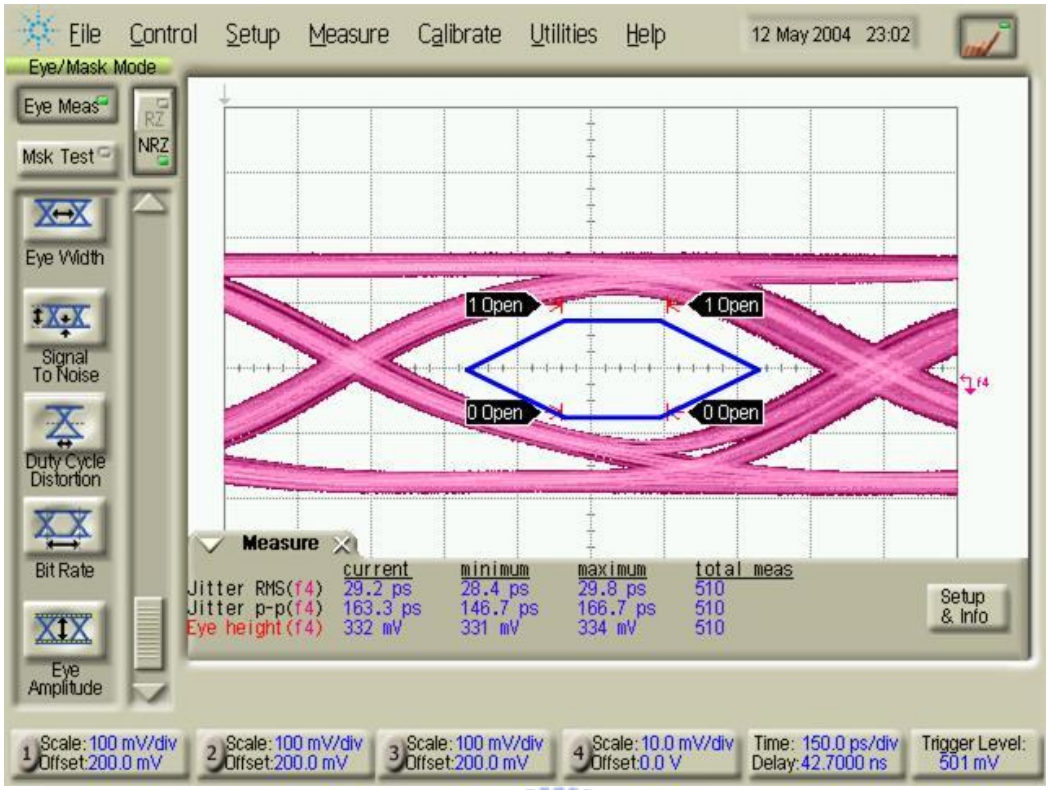


Fig. 5-11 Rx input waveform through 1.8m cable without Tx pre-emphasis at 1Gbps

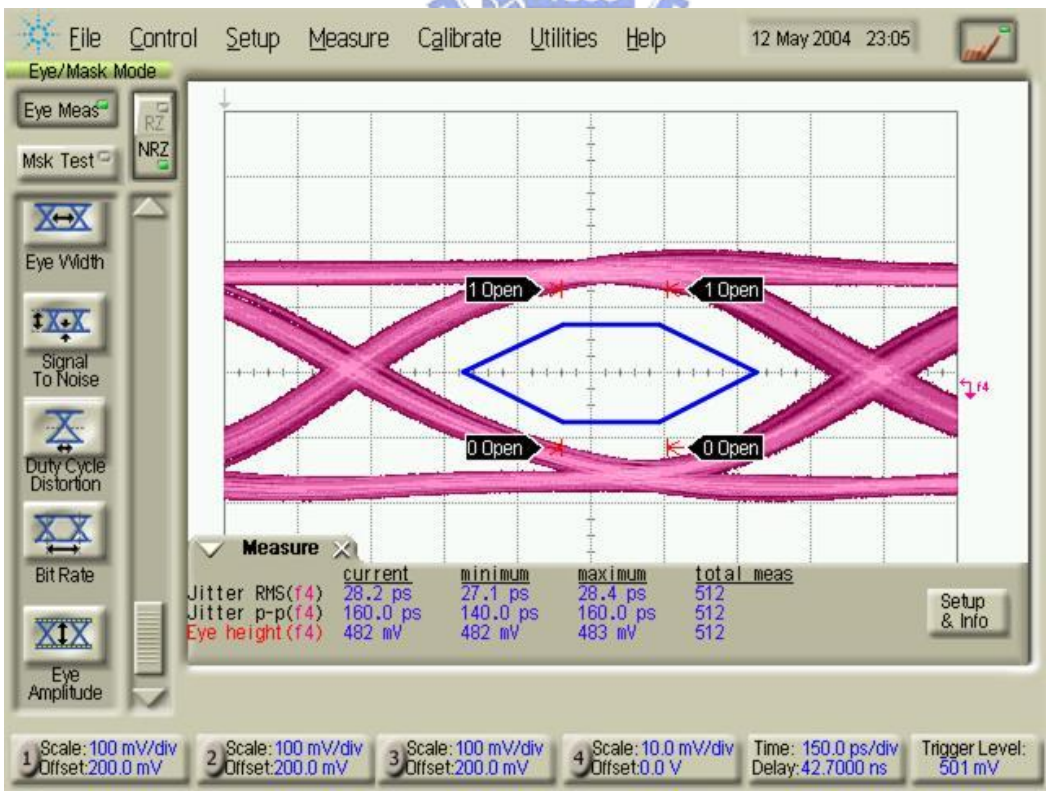


Fig. 5-12 Rx input waveform through 1.8m cable with Tx pre-emphasis at 1Gbps

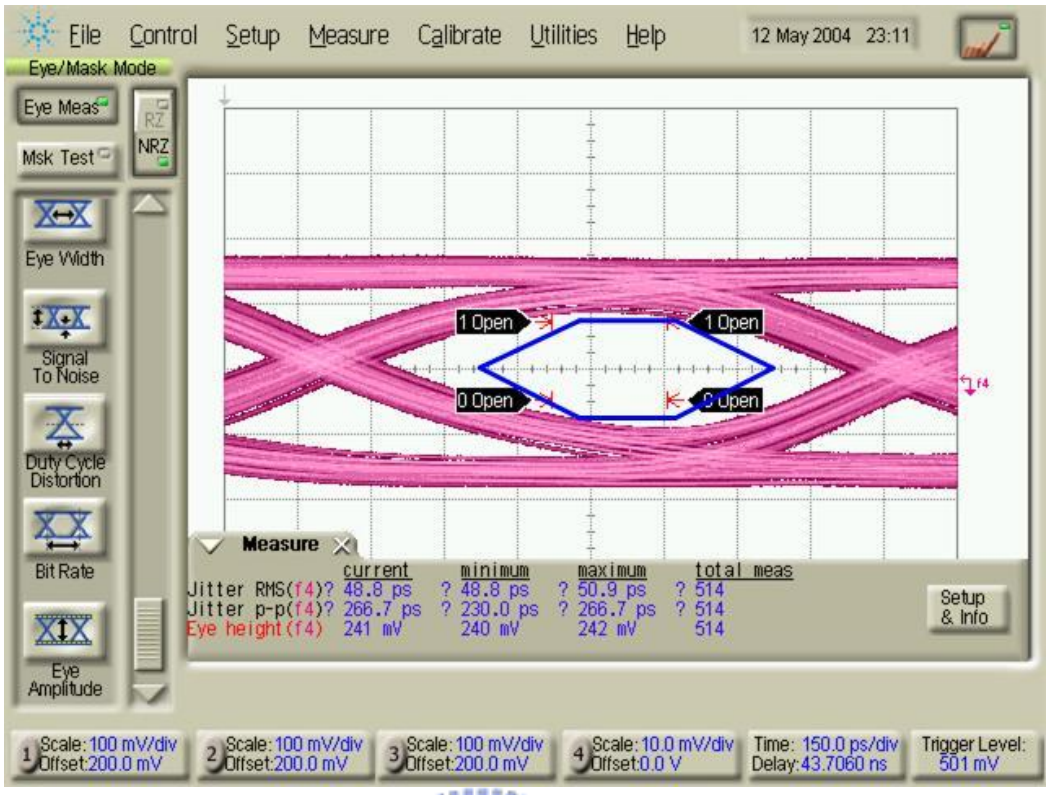


Fig. 5-13 Rx input waveform through 3.6m cable without Tx pre-emphasis at 1Gbps

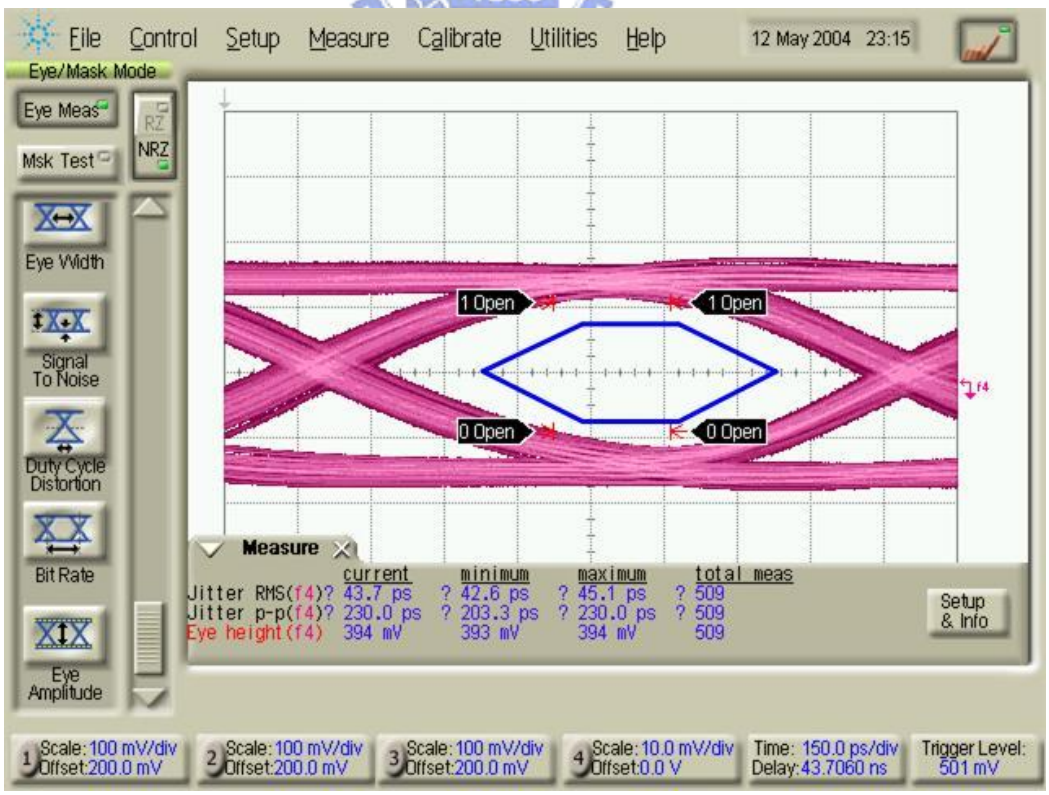


Fig. 5-14 Rx input waveform through 3.6m cable with Tx pre-emphasis at 1Gbps

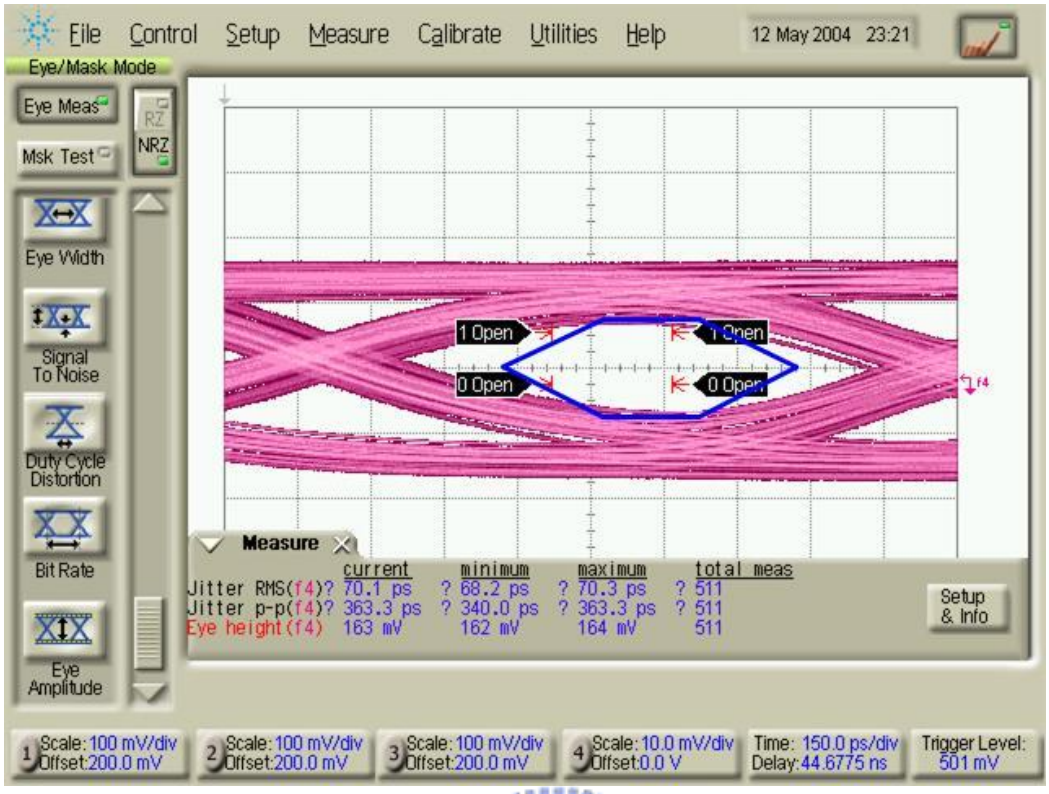


Fig. 5-15 Rx input waveform through 5.4m cable without Tx pre-emphasis at 1Gbps

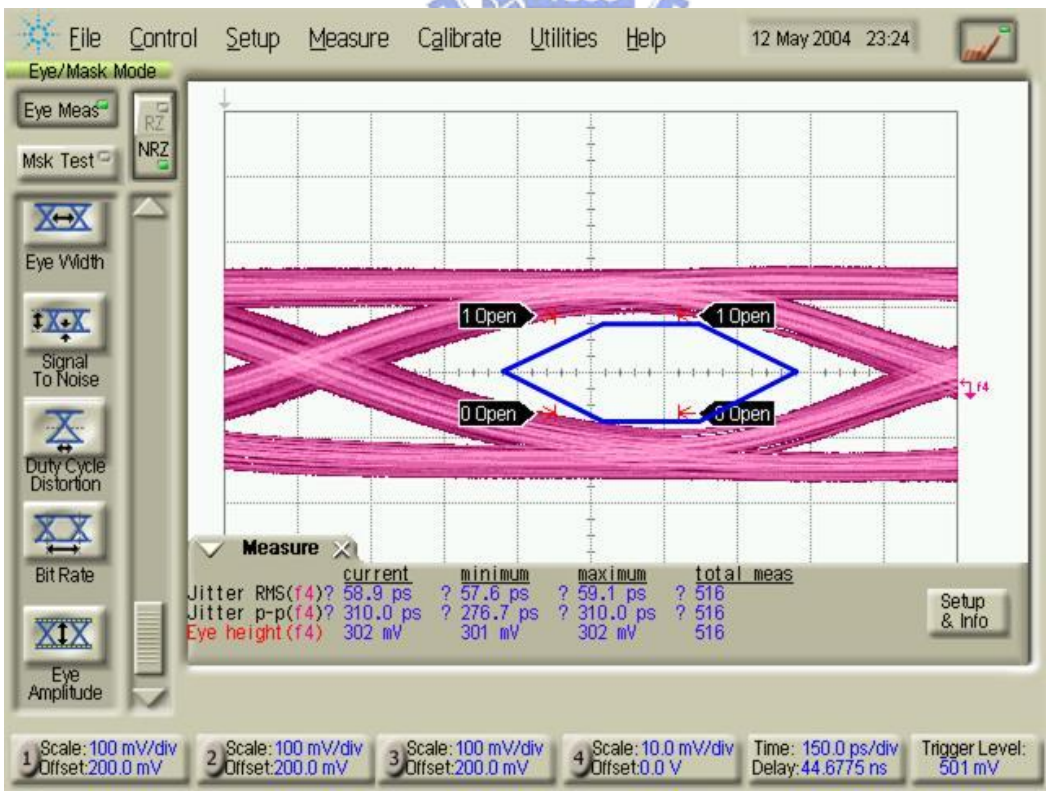


Fig. 5-16 Rx input waveform through 5.4m cable with Tx pre-emphasis at 1Gbps

Table. 5-2 Measured results summary of the Transmitter

Technology	0.35μm 2P4M CMOS		
Function	Transmitter		
Supply Voltage	3.3V		
Data Rate	1Gbps		
Data Driver Current	13mA		
Pre-emphasis Current	4mA		
without pre-emphasis	Eye Height	RMS Jitter	Pk-Pk Jitter
Near-end	634mV	23.8ps	153.3ps
1.8m cable	332mV	29.2ps	163.3ps
1.8+1.8m cable	241mV	48.8ps	266.7ps
1.8+1.8+1.8m cable	163mV	70.1ps	363.3ps
Power	122mW@1Gbps		
with pre-emphasis	Eye Height	RMS Jitter	Pk-Pk Jitter
Near-end	543mV	25.8ps	166.7ps
1.8m cable	482mV	28.2ps	160ps
1.8+1.8m cable	394mV	43.7ps	230ps
1.8+1.8+1.8m cable	302mV	58.9ps	310ps
Power	141mW@1Gbps		

Then, we fixed the length of the cable (5m) and adjusted pre-emphasis current at three different data rate, 800Mbps, 1Gbps, and 1.2Gbps. The relationship between differential output level and pre-emphasis current is shown in Fig. 5-17 and the relationship between RMS jitter and pre-emphasis current is shown in Fig. 5-18. It can be shown that more pre-emphasis current can improve both the eye height and the jitter.

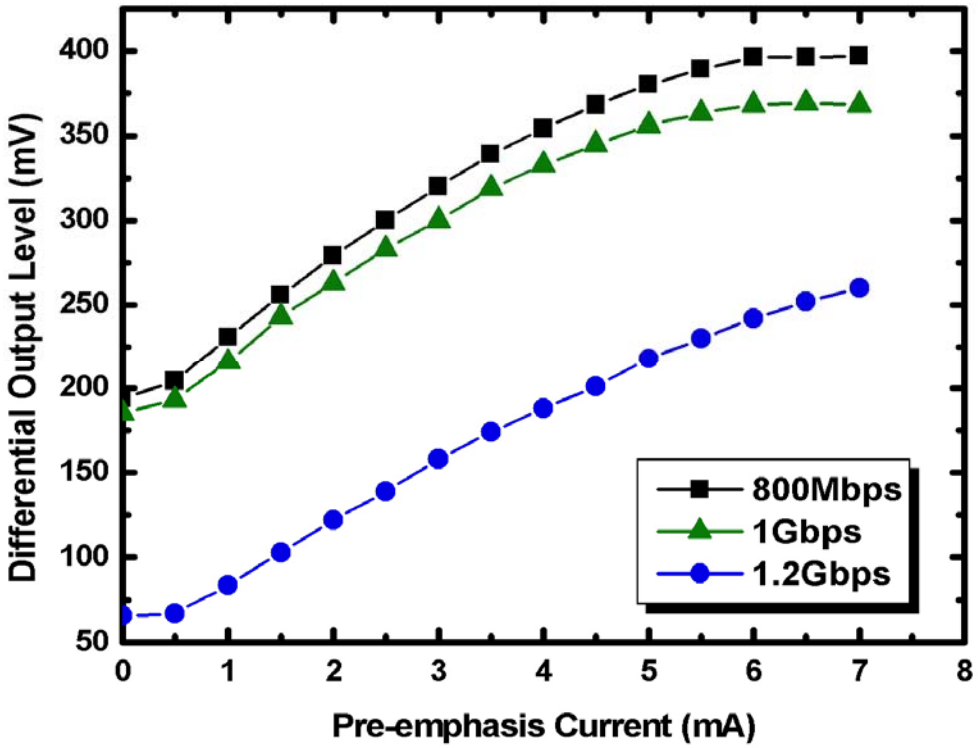


Fig. 5-17 The relationship between differential output level and pre-emphasis current

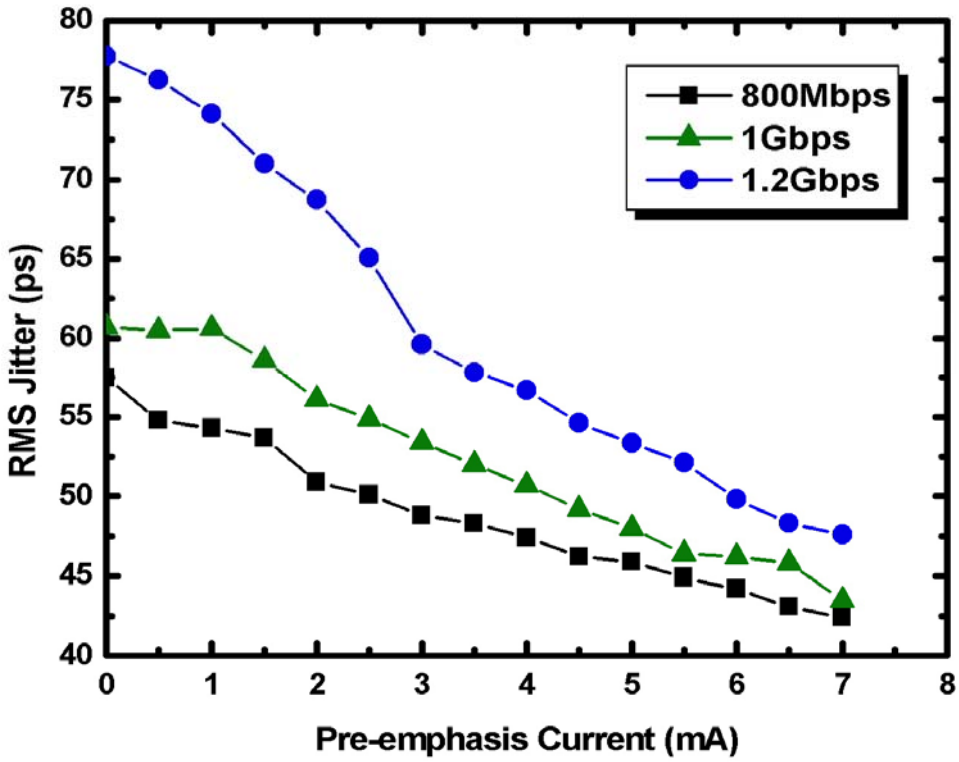


Fig. 5-18 The relationship between RMS jitter and pre-emphasis current

Chapter 6

Conclusions and Future Works

6.1 Conclusions

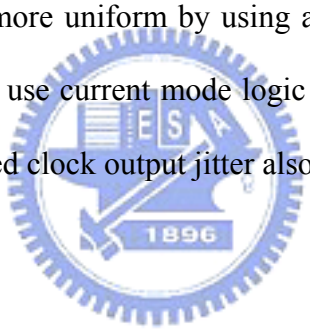
In this thesis, we had completed the design of a 1Gbps serial-link transceiver. The research results can be summarized as follows.

The first block we examined is the phase-locked loop (PLL). The main issue of the PLL is to generate the required phases used for the 8:1 multiplexer of the transmitter while making the timing jitter as small as possible. This may be done from system level to circuit level, including parameter design and layout issue. For the transmitter part, we use the 8:1 multiplexer to increase the transmitted data rate. In order to reduce the inter-symbol interference, a pre-emphasis circuit is added to increase the current during the data transition. The circuit was implemented in a TSMC 0.35μm 2P4M CMOS process. The experiment results are described in chapter 5. For the receiver part, the slicer at the receiver front-end resolves the small input at high data rates. The clock and data recovery (CDR) operates at half of the input data rate and uses a dual-tracking path control mechanism to achieve better jitter

performance. Then, the de-multiplexer converts the CDR outputs to eight parallel data. Whole design issues of the receiver are described in chapter 4.

6.2 Future Works

For the transmitter, to increase even higher data bandwidth, the bandwidth-limited channels effect should be carefully treated. Techniques such as modulation, equalization, and coding can provide significant improvement in data bandwidth through transmitting more complex symbols instead of simple bits. The PLL output jitter must be reduced and multiphase generation can be more uniform by using average resistors. For the receiver, the phase detector of the CDR can use current mode logic to reduce the switching noise and the power consumption. The retimed clock output jitter also must be reduced.



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