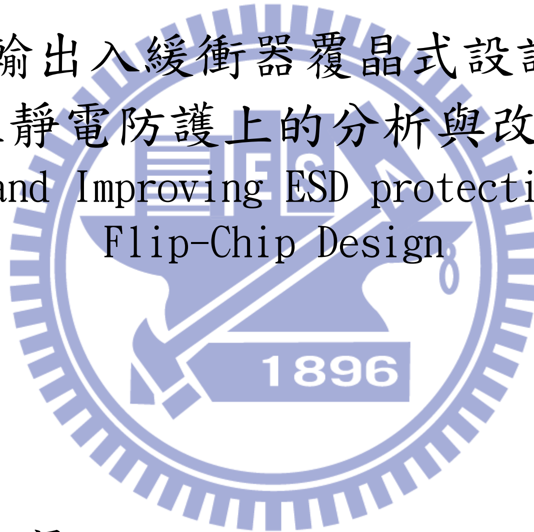
國立交通大學

電機學院　電子與光電學程

碩士論文



輸出入緩衝器覆晶式設計
在靜電防護上的分析與改進
On analyzing and Improving ESD protection in Area-I/O Flip-Chip Design

研 究 生：梁以正

指導教授：陳宏明　教授

中華民國一百年九月

輸出入緩衝器覆晶式設計在靜電防護上的分析與改進
On analyzing and Improving ESD protection in Area-I/O Flip-Chip Design

研 究 生：梁以正　　　Student：Yi-Cheng Liang

指導教授：陳宏明　　　Advisor：Hung-Ming Chen

國 立 交 通 大 學
電機學院　電子與光電學程

碩 士 論 文

A Thesis

Submitted to College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics and Electro-Optical Engineering

September 2011

Hsinchu, Taiwan, Republic of China

中華民國一百年九月

輸出入緩衝器覆晶式設計在靜電防護上的分析與改進

學生：梁以正　　　　　　　　　　　　　　　指導教授：陳宏明教授

國立交通大學 電機學院 電子與光電學程 碩士班

摘　　要

現今電子產品需求注重多功能與輕薄短小。因此，半導體封裝也朝高密度技術方向發展，而在高密度的微系統設計與封裝技術中，覆晶技術(Flip-Chip)已是一項成熟的方式，其重疊結構更利於 IC 積體化，垂直連接而非打線的方式也可減少連線距離，進而在高頻、雜訊和功率消耗上得到改善。在超大型積體電路設計中，設計者對於輸出入埠(In/Out ports)依然使用傳統環型結構(I/O ring)，它雖擁有成熟的靜電防護機制，卻增加了繞線距離，這份取捨也犧牲了原有的好處。

本文試著使用區域型輸出入元件(Area-I/O cell)配合新分佈架構去含蓋雙方優點，分析數據證明新架構在靜電防護能力上有大幅的提升，而新的排列方式在此架構上也有較佳的效果。最後此方法設計時亦考量一般設計者工作流程和習慣，實務上可輕易導入此機制。

On analyzing and Improving ESD protection in Area-I/O Flip-Chip Design

student：Yi-Cheng Liang Advisors：Dr. Hung-Ming Chen

Department Program of Electrical and Computer Engineering
National Chiao Tung University

ABSTRACT

Now the demands of electrical product are multi-function, lightweight and low profile. Based on this concept, the package methods have to meet high density trend. Flip-chip is a mature technology on high density microsystem design and packaging. This structure using vertical connection to substitute bonding wire can reduce the connection distance to get the benefits: high frequency demand, better noise control and less power consumption on metal. In general VSLI design, the circuit designers still use the I/O ring for chip design. The conventional I/O ring is the mature structure for ESD protection, but it increases the distance of connection. This trade-off loses the benefit from reducing the connection distance.

In this study, we try to use the new I/O distribution structure by Area-I/O cell to

keep the two benefits. In our analysis, this new method has a large improvement for ESD protection. And new algorithm of cell assignment on this structure can obtain better result than general assignment method. Finally, we consider the present VLSI design flow in this discussion. New method can be easily applied in the original working flow.

誌　　謝

能夠完成此篇論文，最感謝的是指導教授陳宏明老師，以及博士班的李仁傑學長。過程中不斷細心指導，也提供很多意見與方向，讓我免於論文上的白工。在準備考間期間也要感謝家人、朋友的打氣支持，才讓我有落榜後再次挑戰的信心。

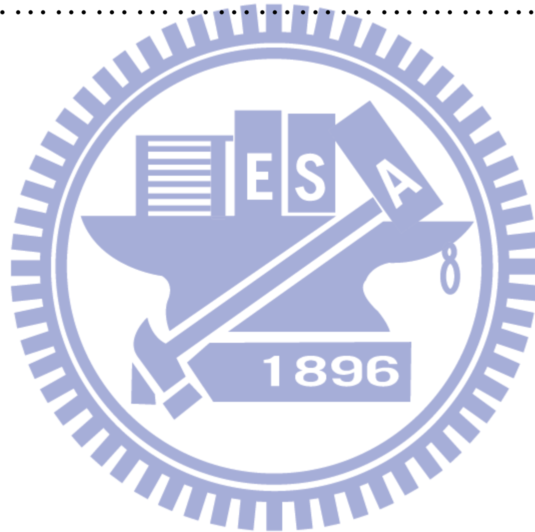
此外，也要感謝過去同事在工作上的包容，特別是之前台積的長官，也是現任清華大學教授:張彌彰教授，在我在職的這段時間，除了以身作則教導我們工作上應有的態度和責任感，更鼓勵我們這些大學畢業初進職場的小毛頭持續進修，也才有今天的機緣遇到所以遇到的一切。

也感謝在口試過程中，李毅郎老師的指教和柯明道老師在 ESD 上精闢的見解，著實令我獲益良多。最後，再次對我的指導教授還有這一路以來幫助過我的人，表達我最真誠的謝意!

CONTENT

中文提要 I
英文提要 III
誌謝 V
Content VI
List of tables VIII
List of figures IX
Chapter 1 Introduction 1
1.1 Background & Motivation 1
1.2 Organization of this thesis 3
Chapter 2 ESD protection analysis 4
2.1 ESD protection conception 4
2.2 ESD ohm's law 5
2.3 ESD protection estimation 6
2.4 Measurement model 8
2.4.1 Function cell to Function cell model 9
2.4.2 Function cell to Power/Ground cell model 10
2.4.3 Power/Ground cell to Power/Ground cell model 11
2.4.4 Power/Ground cell to Power/Ground cell between different domains model 12
Chapter 3 Proposed I/O distribution methods 13
3.1 Requirements and Manner 13
3.2 SEWER distribution structure 14
3.3 Cell assignment 16
3.3.1 Local distribution algorithm 17
3.3.2 Density distribution algorithm 19
3.3.3 Iterative improvement algorithm 21
Chapter 4 Verification result 24

4.1 Case 1 24
4.2 Case 2 28
4.3 Case 3 32
Chapter 5 Discussion 36
5.1 Impact and Benefit 36
5.2 Improvement of ESD protection 37
5.3 Latch up issue 38
Chapter 6 Conclusion & Future work 40
6.1 Conclusion 40
6.2 Future work 40
Reference 41



List of tables

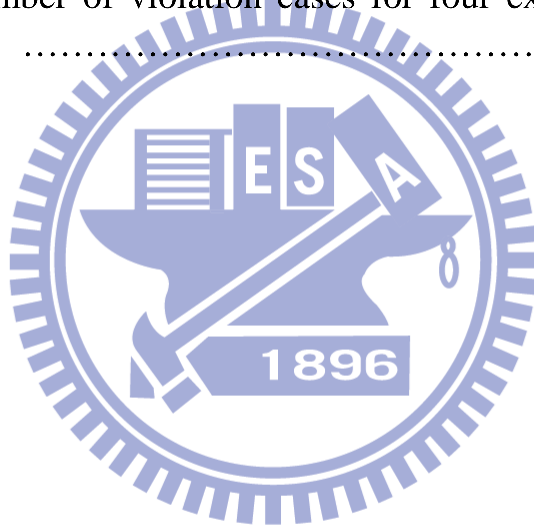
Table 3.1 The analysis table of several clamp combination in one chain 21

Table 3.2 The parameter description of iterative improvement algorithm 23

Table 4.1 The number of violation cases for four experiments of case 1 27

Table 4.2 The number of violation cases for four experiments of case 2 31

Table 4.3 The number of violation cases for four experiments of case 3 35



List of figures

Figure 1.1	Wire bond vs. Flip chip	1
Figure 1.2	Bump pads, Circuit blocks and I/O cells	2
Figure 2.1	The damage path and the ESD protection path	4
Figure 2.2	Two power domain ESD protection circuit	7
Figure 2.3	The I/O combination state of two power domains circuit…	7
Figure 2.4	The resistor model and equation for "Function cell to Function cell" measurement model	9
Figure 2.5	The resistor model and equation for "Function cell to Power/Ground cell" measurement model	10
Figure 2.6	The resistor model and equation for "Power/Ground cell to Power/Ground cell" measurement model	11
Figure 2.7	The resistor model and equation for "Power/Ground cell to Power/Ground cell between different power domains" measurement model	12
Figure 3.1	General VLSI working flow	13
Figure 3.2	I/O Ring structure vs. Sewer structure I/O	15
Figure 3.3	The states of sewer structure combination	16
Figure 3.4	Single space vs. Double space	16
Figure 3.5	The cell assignment state of local distribution algorithm …	17
Figure 3.6	Local distribution algorithm for single chain	18
Figure 3.7	The sewer structure for cell distribution	19
Figure 3.8	Density distribution algorithm	20
Figure 3.9	The sample of cell assignment by the iterative improvement algorithm	22
Figure 3.10	Iterative improvement algorithm	23
Figure 4.1	The case 1 using the conventional I/O ring	24
Figure 4.2	The case 1 using the local distribution algorithm on sewer I/O structure	25

Figure 4.3 The case 1 using the density distribution algorithm on sewer I/O structure 25

Figure 4.4 The case 1 using the iterative improvement algorithm on sewer I/O structure 26

Figure 4.5 The case 2 using the conventional I/O ring 28

Figure 4.6 The case 2 using the local distribution algorithm on sewer I/O structure 29

Figure 4.7 The case 2 using the density distribution algorithm on sewer I/O structure 29

Figure 4.8 The case 2 using the iterative improvement algorithm on sewer I/O structure 30

Figure 4.9 The case 3 using the conventional I/O ring 32

Figure 4.10 The case 3 using the local distribution algorithm on sewer I/O structure 33

Figure 4.11 The case 3 using the density distribution algorithm on sewer I/O structure 33

Figure 4.12 The case 3 using the iterative improvement algorithm on sewer I/O structure 34

Figure 5.1 The analysis results of experimental groups and control group in case 1 37

Figure 5.2 The analysis results of three experimental groups in case 1 38

Figure 5.3 The spatial variation between Ring structure and sewer structure in the verification case 2 39

Chapter 1

Introduction

1.1 Background & Motivation

Flip chip is a high density microsystem package. It supports a high-pinout structure and a shorter connection condition without bonding wire (Figure 1.1). The connection can contact with below solder ball via the bump ball and the channel in substrate by vertical direction. This benefit of reducing the distance of connection includes the higher frequency condition, better noise control, less power consumption on metal and low IR-drop.

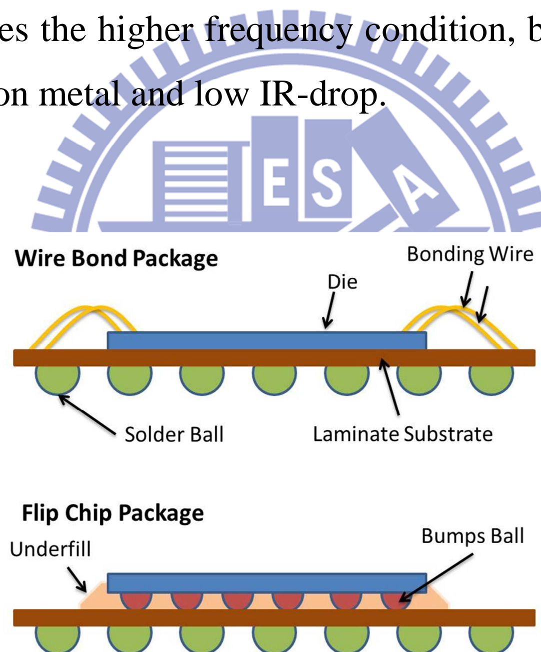


Figure 1.1 Wire bond vs. Flip chip

The I/O cells are the interfaces and contain Electrostatic discharge (ESD) protector between the bump ball and the internal circuit in die. In the wire bond package, the circuit designer usually puts I/O cells by the ring style around the chip edge. The signal is along the bonding wire and chip edge smoothly into the circuit in chip center.

I/O ring is a mature structure for the ESD protection system. It owns the enough metal width for electromigration (EM) requirement to share ESD current. But it is NOT a good layout style for flip chip package. When we make the I/O ring for flip chip package, the signal from circuit has to make a detour to the chip edge and go back to the bump pad by routing nets in redistribution layer (RDL) (Figure 1.2). This extra routing metal in RDL neutralizes the benefits of flip chip from reducing connection distance.

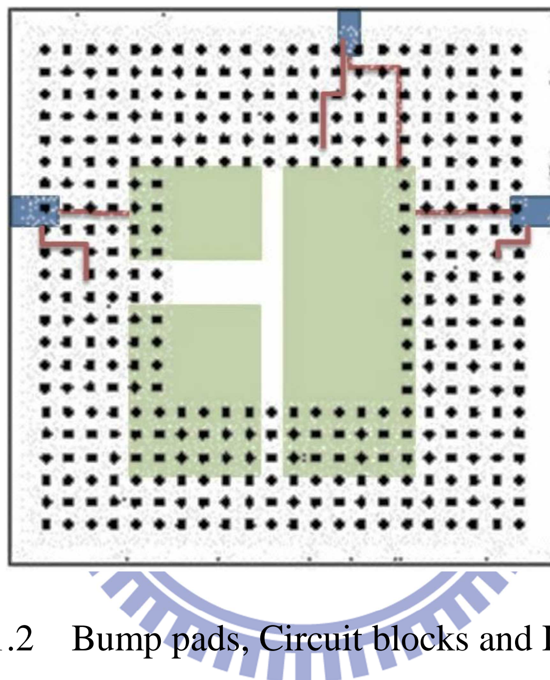


Figure 1.2 Bump pads, Circuit blocks and I/O cells

Since flip chip package was presented, there are many discussions about the Area-I/O to make a vertical conduction with solder ball. They almost focus on the wire length minimization [1] [2] and optimize the other conditions [3]. There is only a little description about the ESD [4]. There are no methods to distribute about the Area-I/O and ESD, and guarantee that they have enough ESD protection capability. Certainly, we can still follow these descriptions to make a high quality and high performance design. But it has the risk of yield degradation from the ESD damage problems. Based on the demand of mass product, the general circuit designer usually still makes the I/O cells by a ring

structure. It means that they make a trade-off to keep the ESD protection capability but loss the benefits of shorter connection. For this reason, we try to find the solution for this dilemma. It has to place the I/O cells in core area of chip to solve the detour issue, and provides the enough ESD protection for internal circuit.

Finally, we simultaneously consider the general VLSI design flow in this study. New method should be convenient to replace the present integration step in VLSI design flow.

1.2 Organization of this thesis

The remainder of this thesis is organized as follows. Chapter 2 describes the ESD protection analysis. We explain the principle of ESD protection and use four measurement models to estimate whole protection system. The protection capability of testing cases would be estimated by this measurement method. In chapter 3, we provide a new I/O distribution structure which placed the I/O cells in core area of chip to solve the detour issues of package. This structure owns the enough metal width as conventional I/O ring and keeps the relationship of original internal circuits. The circuit designer can easily adopt this method to replace original integration flow. In chapter 4, we verify the real cases by new distribution structure for I/O cells and provide some new algorithms on this structure. In chapter 5, we analyze the effect of the new structure and algorithms. This new structure has good improvement on ESD protection, and the new algorithms we provide can get more improvement on this issue. Finally, we list the benefits of these methods and list the future works in chapter 6.

Chapter 2

ESD protection analysis

2.1.ESD protection overview

In Figure 2.1, there are two ESD current paths between the one pin pair. We design an ESD protection path to avoid the ESD current attacks the internal circuit. The key-point of ESD protection is that the ESD device can be turned on faster in order not to damage the internal circuit. The damaged path is very difficult to forecast. So we just concentrate on the protection path design and follow the ESD guideline to build the protection system. This guideline can make sure that the ESD device can turn on in time to avoid internal circuits from damage.

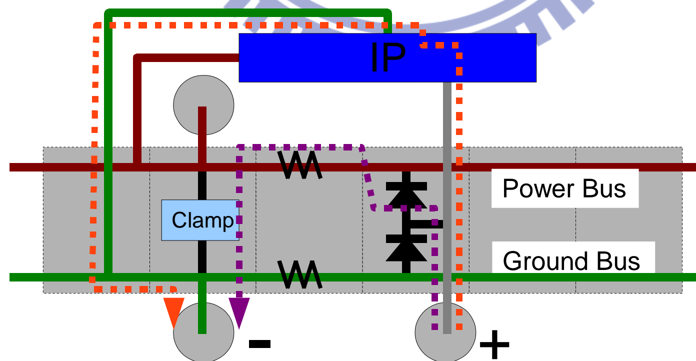


Figure 2.1 The damage path and the ESD protection path

The impedance on the ESD protection path includes the ESD devices and the metal resistance between two terminal pins. In equation (2.1), where ΔV_{ESD} is the ESD voltage drop. This voltage drop will be distributed on the ESD devices and its connecting metal bus. The $\Delta V_{ESD-devices}$ can reach the turn-on voltage very quickly due to a lower bus resistance. We assume that there is a maximum R limit value for $R_{metal\ on\ ESD\ protection\ path}$, and this R value can make guarantee that the ESD device would be turned on faster in order not to damage the internal circuit. We can build the ESD protection system and assume that the all of metal resistance between each pin pairs is less than this maximum R value. This ESD protection system will completely protect our internal circuit.

$$\Delta V_{ESD} = \Delta V_{ESD-devices} + \Delta I_{ESD} \times R_{metal\ on\ ESD\ protection\ path} \tag{2.1}$$

The semiconductor material and ESD device size have the major impact on this R value in ESD protection system. The foundry will offer this R value and basic design rule about ESD protection design for each semiconductor process they provided.

2.2. ESD ohm's law

In general condition, the ESD problem is usually solved by buying the solution from the I/O provider in foundry. The provider offers a simple guideline called the "ESD Ohm's law" [5] for the user. The circuit designer only needs to concentrate on the combination relationship between all sub-blocks to complete the whole function circuit. When they integrate all sub-blocks, they just need to build the I/O ring, assign the cells location by ESD guidelines and connect with circuits to complete the design of this chip.

The clamp cell is the main element in ESD protection system. It exists on each ESD protection path. So the I/O cell provider provides a simple guideline how to build the I/O chain and this method can meet aforementioned maximum R requirement automatically. Circuit designers have to appropriately place the clamp cells when they are integrated with the function cells. The metal resistance of the function cell to the nearest clamp cells is less than the certain value provider given. This guideline is called ESD Ohm's law. If the designer follows this guideline to build the I/O chain, they can get the guarantee from the I/O provider to avoid the damage of internal circuit.

2.3. ESD protection estimation

We design a two-power domain module as a sample to analyze multiple power domains (Figure 2.2).

There are three kinds of basic ESD protection elements in this design:

1. Clamp cell(maybe with an auxiliary diode)：It is a dual-directional structure circuit to conduct ESD current between power and ground bus.
2. Function cell：There are two unidirectional diodes to conduct ESD current to power or ground bus.
3. Back-to-back diodes： It is a dual-directional structure circuit between the two ground buses of different voltage domains. It conducts the ESD current and cuts the noise between two ground buses.

1896

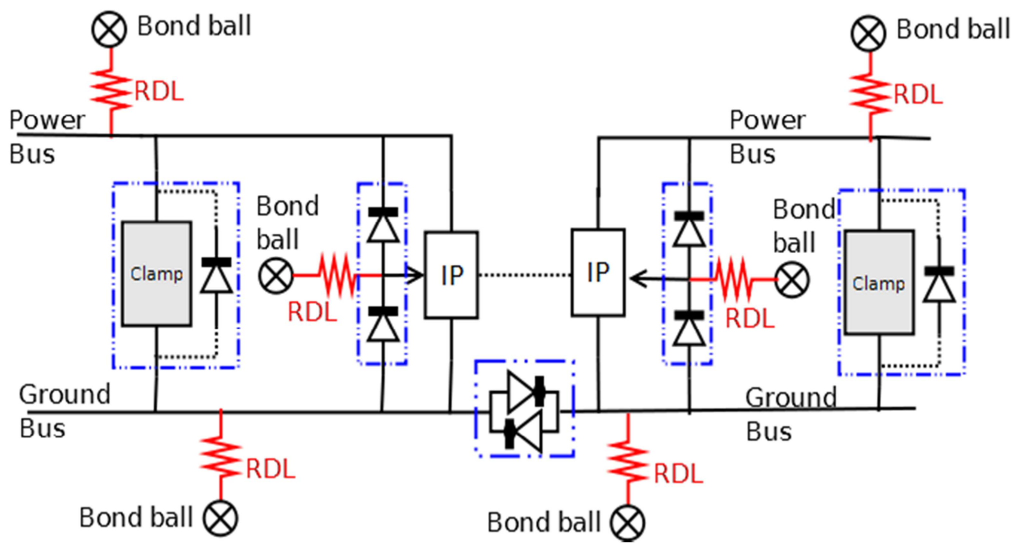


Figure 2.2 Two power domain ESD protection circuit

In Figure 2.2, the multiple power domains can be built and connected by the back-to-back diodes.

As shown in Figure 2.3, we build the I/O chain as the interface between the bump pads and internal circuit for the circuit in Figure 2.2. They can support the signal communication and ESD protection. The ESD current will be conducted to the metal bus on I/O chain to avoid the current to damage the internal circuit.

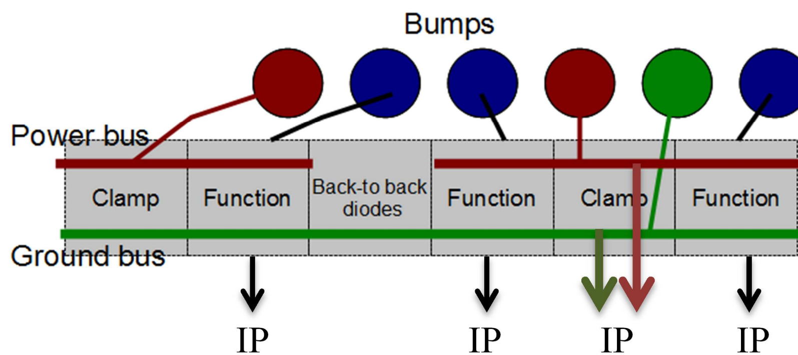


Figure 2.3 The I/O combination state of two power domains circuit

2.4. Measurement model

The relationship of ESD protection system and protected circuit is dependent, thus it is not necessary to measure all pin pairs of the chip. We can ignore the part of pin pairs which show the high impedance of damaged path in protected circuit. In practice, we only focused on the real failure cases for our ESD verification. These four kinds of measurement model can completely verify the whole ESD protection system.

1. Function pin to function pin
2. Function pin to Power/Ground pin
3. Power pin to Ground pin
4. Power pin to Ground pin for different power domains

For the ESD protection capability measurement, we still need to use the detail resistance model of ESD protection system for our estimation. In addition, the best conduct point for power supply is the metal on the clamp cell. The ESD current can be conducted directly to another metal bus by the ESD device turned on. So we assume the clamp cell has to be the first conducted point of power/ground signal, and the clamp cell can represent the measurement point for power/ground pin. We can use the function cell to represent the measurement point as well. As shown in Figure 2.2, based on the current divider rule between the damage path and ESD protection path, using the I/O cells as the measurement points for ESD estimation is a feasible approach.

2.4.1. Function cell to Function cell model

In Figure 2.2 & Figure 2.3, we have an I/O chain with two main function cells and four near clamp cells. The resistance model could be mapped to this chain (Figure 2.4). We assume that the ESD devices are no impedance and try to measure the resistance between the pin pair to get an R value for our ESD protection capability estimation. This R value is the pure resistance of metal bus between the pin pair. The ESD current be conducted via the diodes in function cell and at least one clamp cell. More clamp cells can reduce the total resistance by parallel connection. Finally, the resistance model can be transformed to the two equations by different current directions. We would analyze the degree of protection capability by these equations.

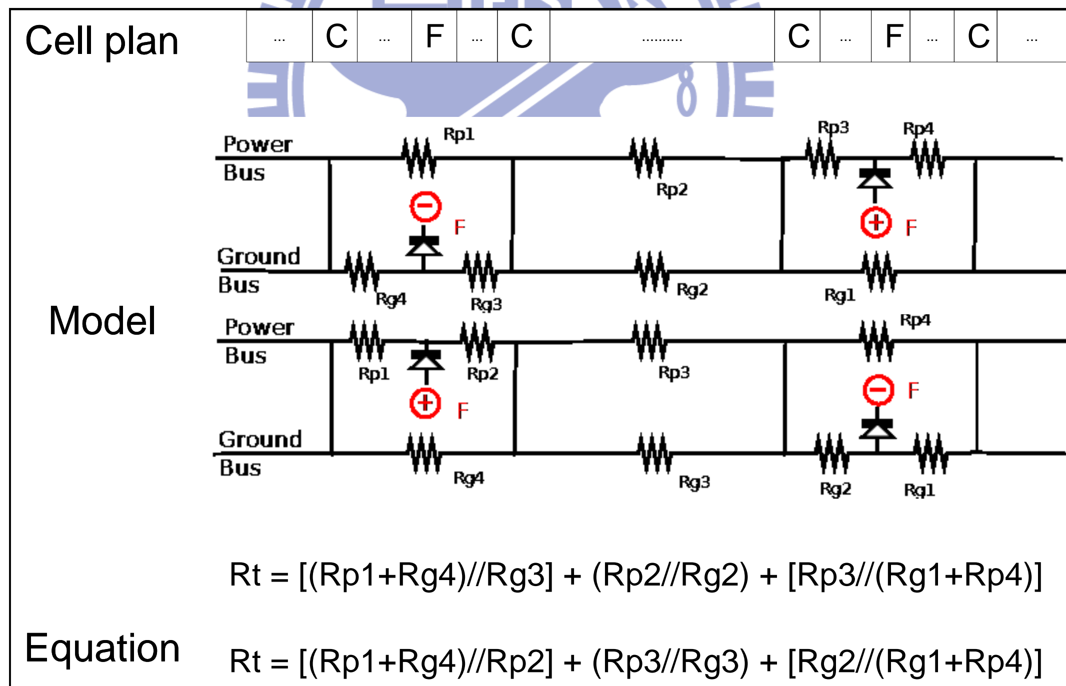


Figure 2.4 The resistor model and equation for "Function cell to Function cell" measurement model

2.4.2. Function cell to Power/Ground cell model

We pick a function cell with two near clamp cells as the one measurement point, and pick another clamp cell as another measurement point. By the same manner, we could get the resistance model and two equations from this cell plan. These two equations are the measurement basis of this model (Figure 2.5).

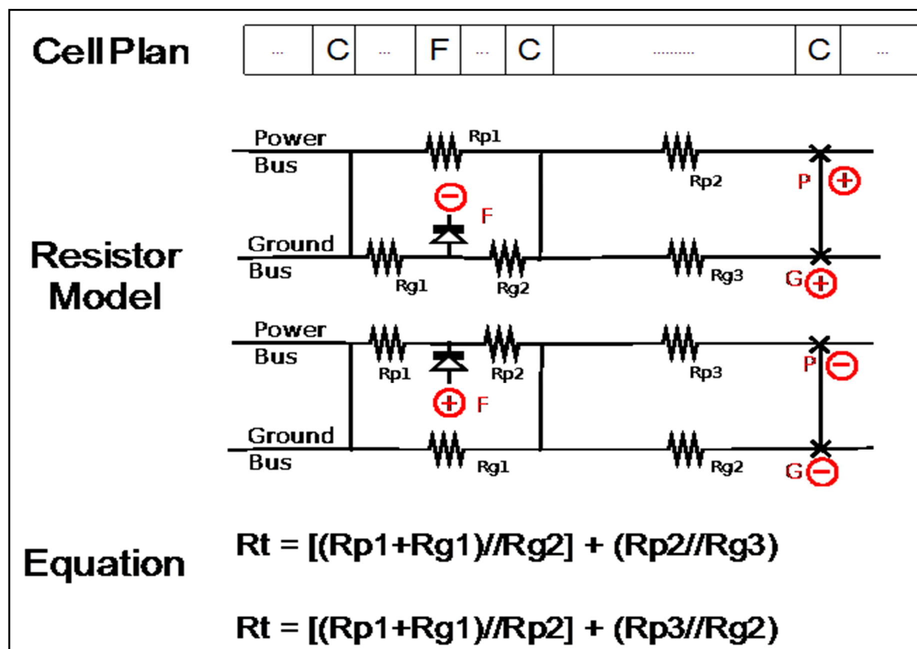


Figure 2.5 The resistor model and equation for "Function cell to Power/Ground cell" measurement model

2.4.3. Power/Ground cell to Power/Ground cell model

Using the same manner, we combine several clamp cells and pick the suitable clamp cells as the measured points to get the model and equation. There are two points worth noting about this measurement model. The first point is that the major factor of resistance module is the distance between two measured cells. The total resistance will not be affected by how many auxiliary clamp cells we use. Second, we assume that the clamp cell is the first conducted cell of power / ground signal in Section 2.4. In the resistor model shown in Figure 2.6, if we allow the conducted point on non-clamp cell, the total resistance would be increased by the other parallel resistor (ex: Rp1+Rg1). The power supply has to go through power/ground cell which is a correct assumption. And it is a common rule in the practice VLSI industry.

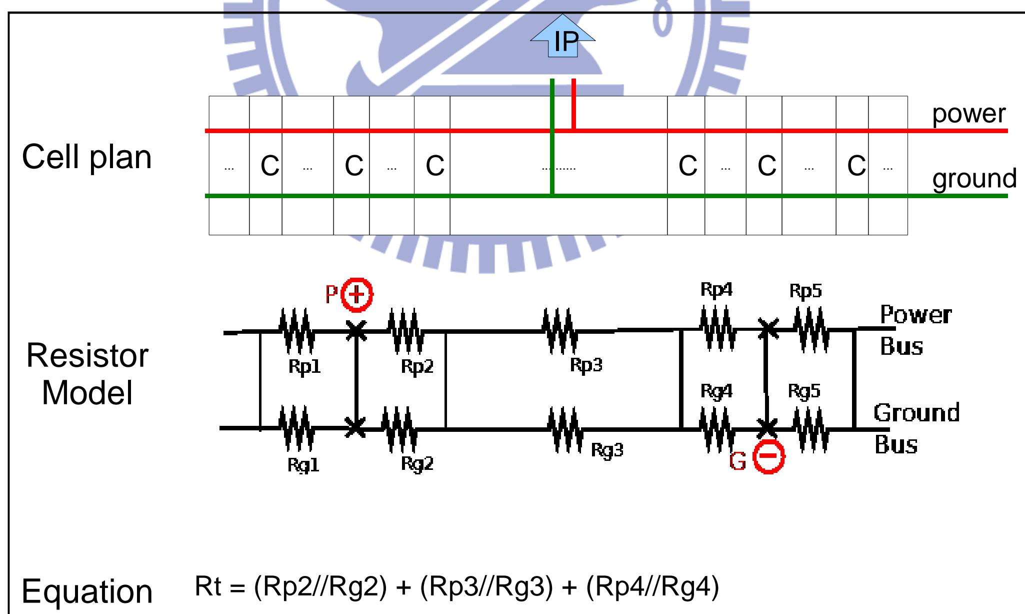


Figure 2.6 The resistor model and equation for "Power/Ground cell to Power/Ground cell" measurement model

2.4.4. Power/Ground cell to Power/Ground cell between different power domains model

It is only one measurement model between two different power domains. In practice, the damaged device is usually found on the interface of two blocks with the different power supply. The model is via the back-to-back diodes to share the ESD current between two ground buses.

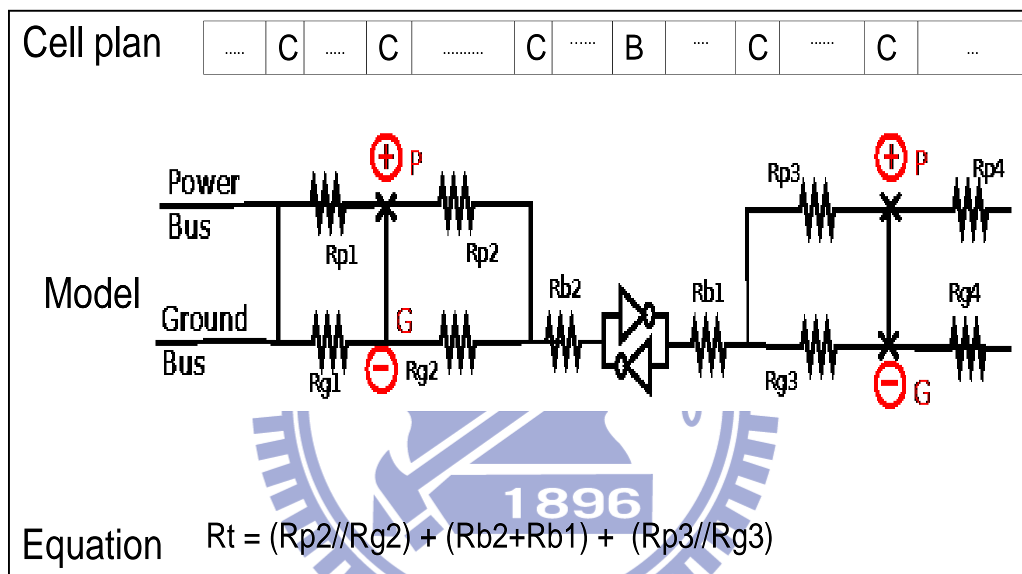


Figure 2.7 The resistor model and equation for "Power/Ground cell to Power/Ground cell between different power domains" measurement model

Chapter 3

Proposed I/O distribution methods

3.1 Requirements and Manners

The development and verification of ESD protection have to spend large cost and time on the repeated tape-out. In general conditions, the ESD problem is usually solved by buying the solution from the I/O provider. The circuit designer only needs to concentrate on the company's product function design before the I/O ring is built (Figure 3.1). If we hope to put the I/O cells in the core area of chip, the circuit designer's working habits must be considered.

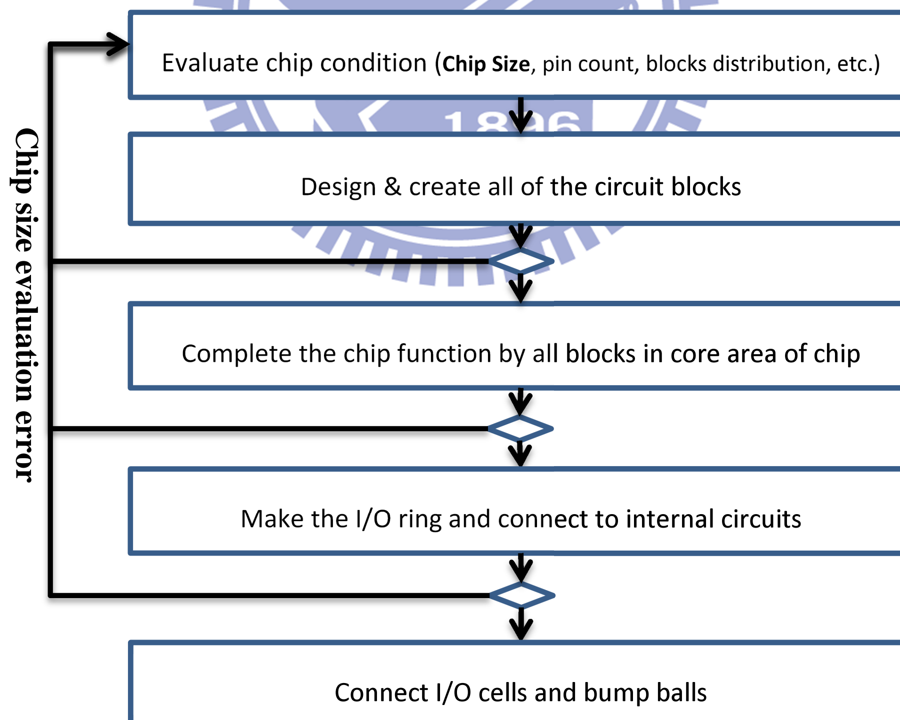


Figure 3.1 General VLSI working flow

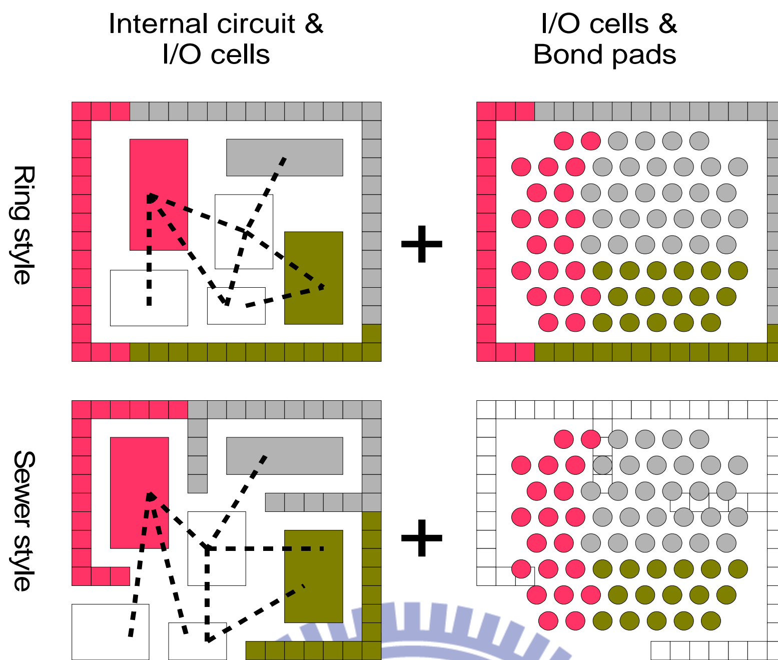
Therefore, we arrange the some basic requirements of our distribution method:

1. Put the I/O cells in the core area to solve the detour issue
2. Consider the construction of center function circuits
3. Make sure to have enough ESD protection capability

For this purpose, we propose two steps. First, we provide a new distribution structure for I/O cell. This structure has to meet above three requirements. Second, we provide the some algorithms of cell assignment, which are based on this new structure to assign the cell type location.

3.2 SEWER distribution structure

We propose a new distribution structure for I/O cell planning. First, we separate all circuit blocks into the I/O blocks and non-I/O blocks, Based on whether the blocks have connected with I/O cells. Second, we still keep the connection relationship of all sub blocks and put the I/O cells close to the I/O blocks. I/O cells can easily connect to these blocks. In this step, the I/O cells must be combined as a chain for supplying enough metal width for the EM consideration. The internal circuit blocks have to be connected by signal routing nets. If the I/O chains have to be crossed with these signal nets, we can appropriately insert the dummy cells which are drawn the power metal only. The circuits can be connected through these dummy cells. Finally, all of the I/O chain will be connected together like a city sewer system for ESD current shared and cut the different power domains by back-to-back diodes. We can observe the difference between the conventional I/O ring and our new structure in Figure 3.2.



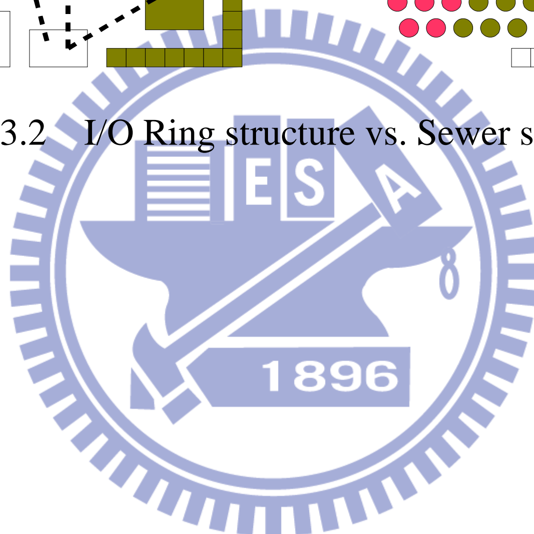


Figure 3.2 I/O Ring structure vs. Sewer structure I/O

3.3 Cell assignment

All of I/O chains have to be connected together. Considering the difficulties in connection, we allow up to the one chain combined by two rows of I/O cells (Figure 3.3). This limit can avoid the excessive squeeze routing in RDL or chip area.

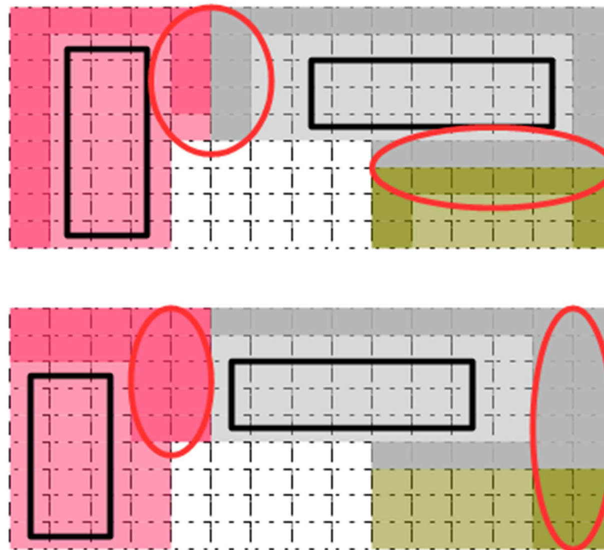


Figure 3.3 The states of sewer structure combination

Based on this structure, we have proposed the three algorithms for the cell type assignment on the new structure. The double space has the better sharing effect than single space. The non-clamp cells have closer to the clamp cells based on the same condition (Figure 3.4).

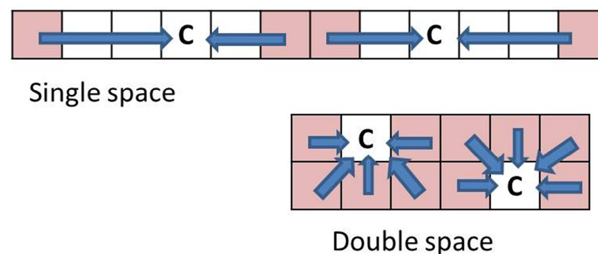


Figure 3.4 Single space vs. double space

3.3.1. Local distribution algorithm

In previous section, we had seen the states of I/O cells which are made by several connected groups. The area combined by two rows cells is called double space (Figure 3.5). This space owns the better sharing effect, so we can reduce the clamp density of double space.

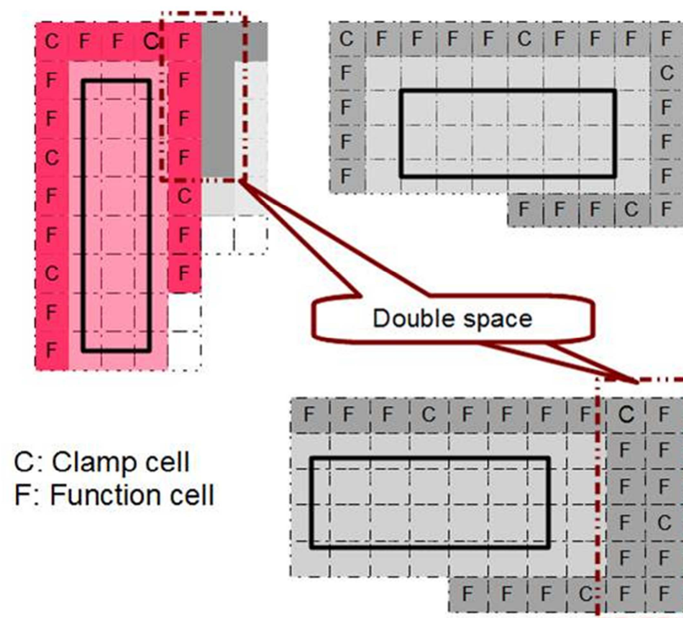


Figure.3.5 The cell assignment state of local distribution algorithm

We put the function cells in sequence and appropriately insert clamp cells. In double space, we use double density value to determine that whether the clamp cell should be inserted. Finally, each group can be completed in accordance with this method.

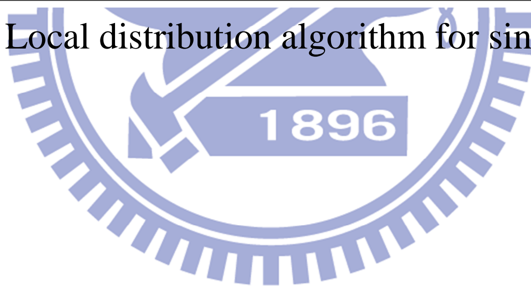
As shown in Figure 3.6, we set the basic density parameter for counter in step 1&2. The clamp cells will be assigned when the counter reach the limit values

which are the multiples of density value. In double space, we raise the limit values to reduce clamp density in this area. We process each chain independently (Figure 3.5). It is a simple algorithm for cell assignment.

```
1  density = clamp cells / [total cells – (0.5 X abutting-cells)]
2  density_limit = $density
3  foreach i = 1 : total cells
4        if ( $i >= $density-limit )
5              space(i) = clamp cell
6              density_limit = $density_limit + $density    // set the next
                                                             // limit of clamp
         else
7              space(i) = function cell
         end

8        if ( space($i) is in abutting area )    // extend limit value for double
                                                 //the density in abutting area
9              density_limit = $density_limit + 0.5
         end
   end
```

Figure 3.6 Local distribution algorithm for single chain



3.3.2. Density distribution algorithm

Local distribution algorithm processes each group independently. If the double space is composed by two independent chains, it can NOT consider the effect of distribution locations from different group chains. For this reason, we develop an algorithm which calculates the densities of each space before the cell assignment.

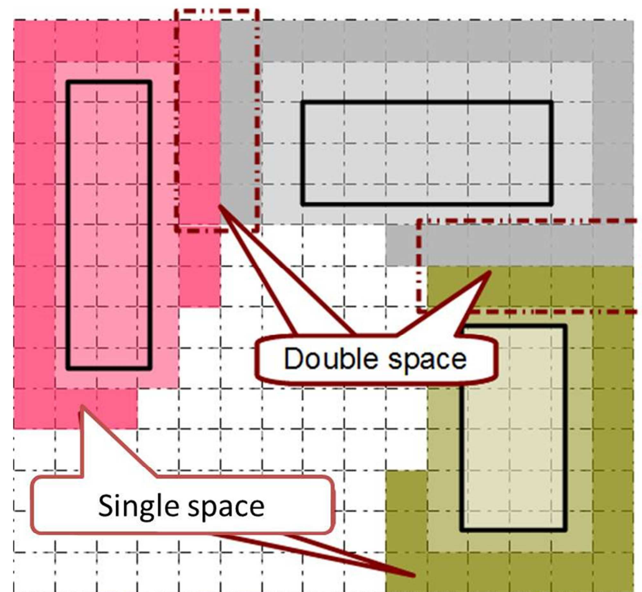
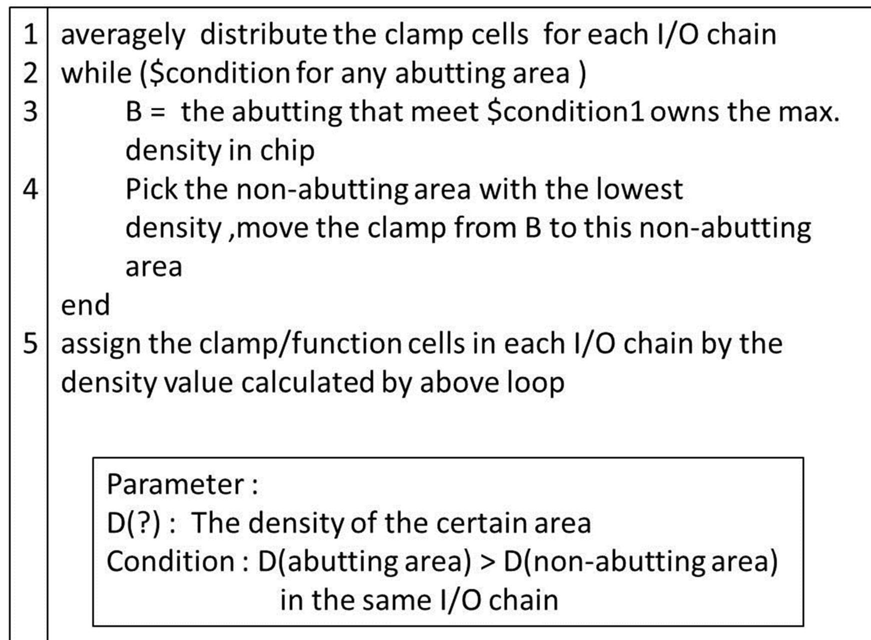


Figure.3.7 The sewer structure for cell distribution

1896

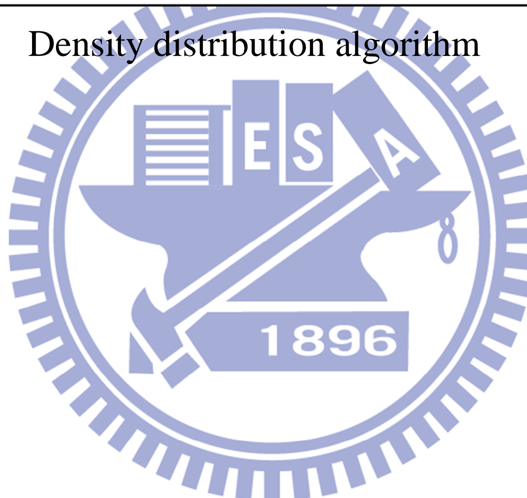
We averagely distribute the clamp cells for each I/O chain to get the initial density value of all areas. The double area will have the higher density because of clamp sharing effect. For average density request, we move the clamp cells from double area to single area in the same group chain until we get the average density of each area in the chip (Figure 3.7). As shown in Figure 3.8, the loop of step 2 will find the density values of each are. Finally, we redistribute the clamp cell by these density values.



```
1  averagely  distribute the clamp cells  for each I/O chain
2  while ($condition for any abutting area )
3          B =  the abutting that meet $condition1 owns the max.
           density in chip
4          Pick the non-abutting area with the lowest
           density ,move the clamp from B to this non-abutting
           area
   end
5  assign the clamp/function cells in each I/O chain by the
   density value calculated by above loop

     Parameter :
     D(?) :  The density of the certain area
     Condition : D(abutting area) > D(non-abutting area)
                 in the same I/O chain
```

Figure 3.8 Density distribution algorithm



3.3.3. Iterative improvement algorithm

In previous two sections, we had presented two algorithms based on the average purpose which is from the concept of ESD ohm's law. Are the averagely distribute clamp cells getting the best ESD protection effect?

We analyze a design with an I/O chain with 28 function cells and 2 clamp cells. We put the clamp cells in the two terminals of chain and changed the clamp location toward to chain center in sequence. After that, we can get the 15 sets of combinations with different clamp locations, and verify those combinations with different ohm limit value. As shown in Table 3.1, there is NO best combination for a fixed ESD protection system. For example in Table 3.1, if the condition of choice is the sum of 13~16 unit resistances. We can get the best choice is the combination (3,28). So we should pick the appropriate combination for different ESD Specifications (SPEC).

Table 3.1 The analysis table of several clamp combination in one chain

Ohm limit value \ Violation case / combination	1,30	2,29	3,28	4,27	5,26	6,25	7,24	8,23	9,22	10,21	11,20	12,19	13,18	14,17	15,16
1.5	378	378	378	378	378	378	378	378	378	378	378	378	378	378	378
2	378	376	376	376	376	376	376	376	376	376	376	376	376	375	378
2.5	378	376	376	376	376	376	376	376	376	376	376	374	372	373	378
3	376	372	370	370	370	370	370	370	370	370	370	368	366	371	377
3.5	376	372	368	368	368	368	368	366	366	366	366	356	360	367	375
4	374	368	362	360	360	360	360	360	360	356	356	347	356	364	373
4.5	374	368	362	354	354	354	354	352	352	348	336	339	350	360	371
5	370	362	354	348	346	346	342	342	342	334	324	333	345	356	368
5.5	366	358	350	340	336	336	336	328	328	304	312	323	337	350	364
6	366	356	346	330	324	322	320	314	306	289	304	316	331	345	360
6.5	360	348	338	326	312	308	308	296	268	275	292	306	323	339	356
7	354	342	330	316	306	292	288	268	250	265	283	298	316	333	351
7.5	354	340	318	304	290	274	260	220	232	249	269	286	306	325	345
8	346	330	316	292	278	256	238	199	220	238	259	277	298	318	339
8.5	338	322	304	278	260	236	174	179	202	222	245	265	288	310	333
9	328	310	292	262	234	204	154	167	189	210	234	255	279	302	326
9.5	328	298	278	246	214	132	134	147	169	192	218	241	267	292	318
10	318	284	264	228	178	113	124	136	157	179	206	230	257	283	310
10.5	306	270	248	194	102	97	106	118	139	161	190	216	245	273	302
11	294	254	216	156	82	87	97	108	128	149	177	204	234	263	293
11.5	280	238	196	72	68	73	81	92	110	131	159	188	220	251	283
12	266	220	156	53	58	64	73	81	100	120	147	175	208	240	273
12.5	234	184	50	39	46	52	59	69	86	104	131	159	194	228	263
13	216	144	30	33	37	44	52	59	75	94	120	147	181	216	252
13.5	178	28	18	21	27	34	40	49	63	80	104	131	165	202	240
14	136	11	14	16	21	27	34	40	53	71	94	120	153	189	228
14.5	14	1	4	8	13	19	26	34	45	61	82	108	139	175	216
15	0	1	3	6	10	15	21	28	38	53	73	98	128	163	203
15.5	0	1	3	6	10	15	21	28	36	49	67	90	118	151	189
16	0	0	1	3	6	10	15	21	28	40	57	79	106	138	175

We analyze another case with more clamp cells, and find that the clamp cell close to the chain terminal will be better than cell in chain center. So we deliver a new algorithm based on this observation (Figure 3.9).

First, we must determine the condition of choice. Second, we design a sample with three steps in Figure 3.8 for the description of iterative improvement algorithm. In step 1, we have several combinations by changing the clamp location in moveable area and pick the N sets of combinations with the best condition from them. In step 2, we can set the N sets of combinations from step1 as basis states, and based on these different states to get the more combinations by executing the aforementioned manner. We can get the (N1*N2) sets of combinations in this time. After that, we pick the N sets of combinations with the best condition from these mixed combinations again. Repeat this until we find the best combination of the whole chain.

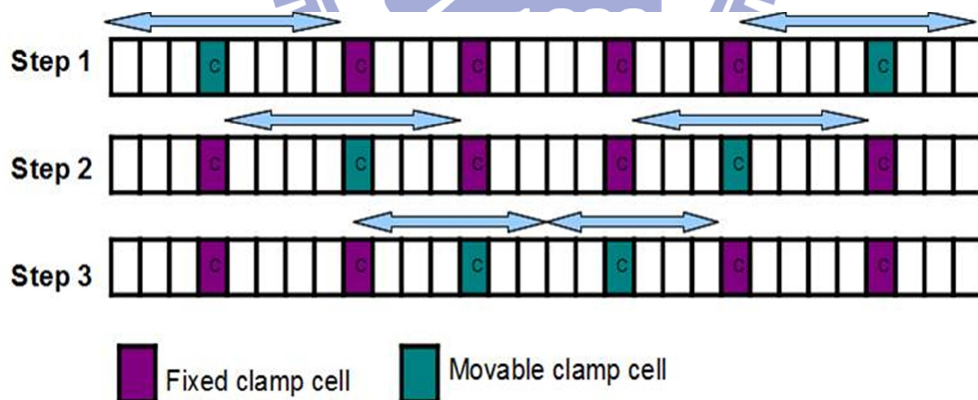


Figure 3.8 The sample of cell assignment by the iterative improvement algorithm

The behavior of sample in Figure 3.8 is described in the step 3 to 7 of iterative improvement algorithm (Figure 3.9). Based on the sewer structure (Figure 3.6), we can process each group chains by the step 3 to 7 of this algorithm. Finally, the double space is formed by two independent groups. This method has the same defect with local distribution Algorithm. So we have to re-execute the step 3 to 7 again for these double spaces to correct this defect.

```
1 | foreach (c = 1 : the number of the chain)
2 |       cb_list  = initial state of the $chain(c)  // for first execution
3 |       foreach (rp @ $chain(c) )
4 |             foreach  (cb @cb_list)
5 |                   Base on parameter rp, to get the $CombiPari ($cb)
6 |                   Saving $CombiPair to $CombiDatabase
  |             end
7 |             pick the $cb_list from $CombiDatabase
  |       end
  | end
8 | re-execute step 3~7 for double space made by 2 groups
```

Figure.3.9 Iterative improvement algorithm

Table 3.2 The parameter description of iterative improvement algorithm

Parameter :	
chain :	The I/O chains in the chip
rp :	The order of clamp pairs, this order is from the two terminal sides to center in the chain
cb_list:	The N sets of combinations of the best condition
CombiPair(cb) :	Base on the certain of combination(cb), we moved the clamp pair in moveable area to create the more different combinations
CombiDatabase:	We used each combinations of cb_list, to create more combinations by moving the clamp pair. This database include those mixed combinations from this $cb_list for the next $cb_list's picking.

1896

Chapter 4

Verification result

In this study, we verify three real industry chips. The original state with conventional I/O ring would be set to the control group. And we use the same bases to build several experimental groups by the methods we provide.

4.1. Case 1

Chip size： 2400um X 2400um

I/O cell size： 60um X 60um

Pin count： 140

Number of function cell： 127

Number of clamp cell： 23 (10 cells for ESD protection enhancing)

Power structure： two power domains

Condition of ESD estimation： Minimum of sum of violation cases

- Conventional I/O Ring

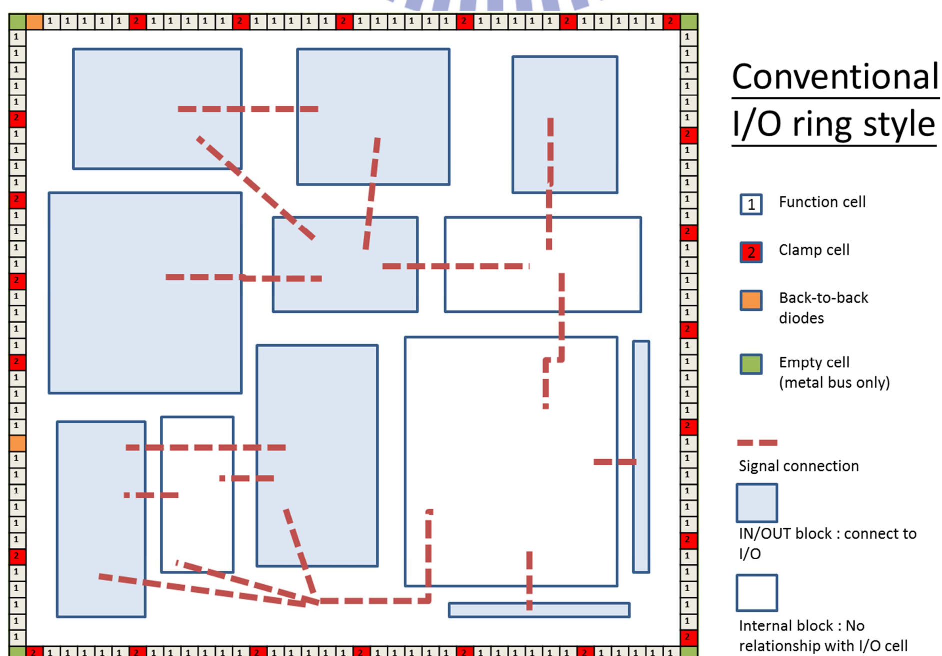


Figure 4.1 The case 1 using the conventional I/O ring

- Local distribution algorithm on sewer style I/O

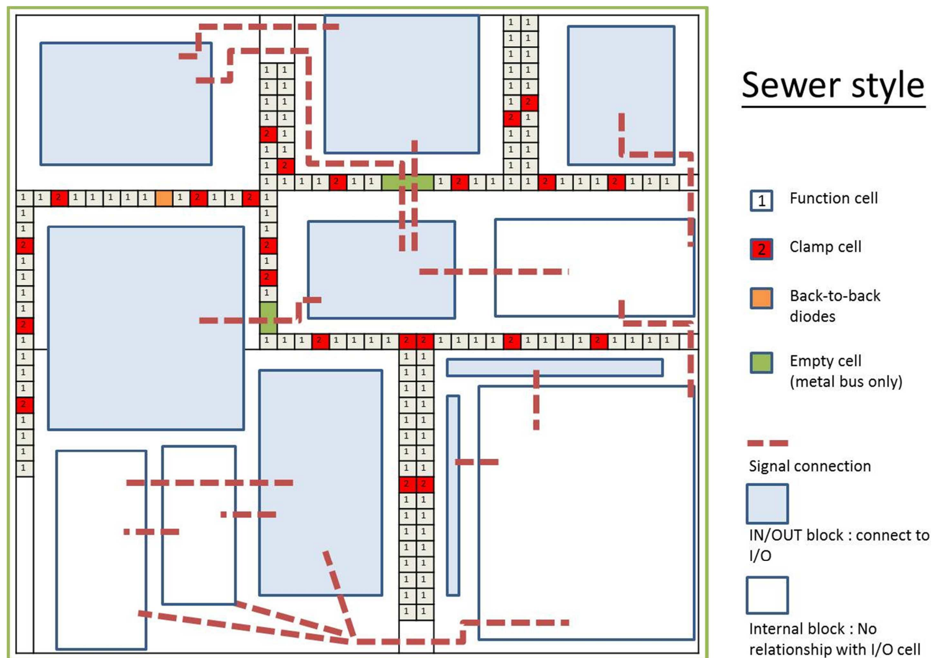


Figure 4.2 The case 1 using the local distribution algorithm on sewer I/O structure

- Density distribution algorithm on sewer style I/O

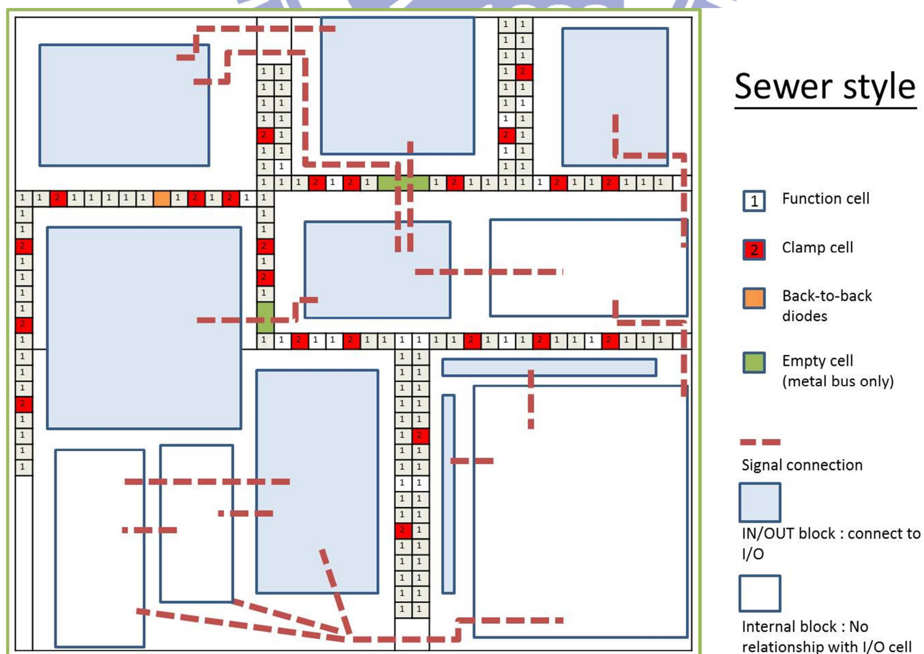


Figure 4.3 The case 1 using the density distribution algorithm on sewer I/O structure

- Iterative improvement algorithm on sewer style I/O

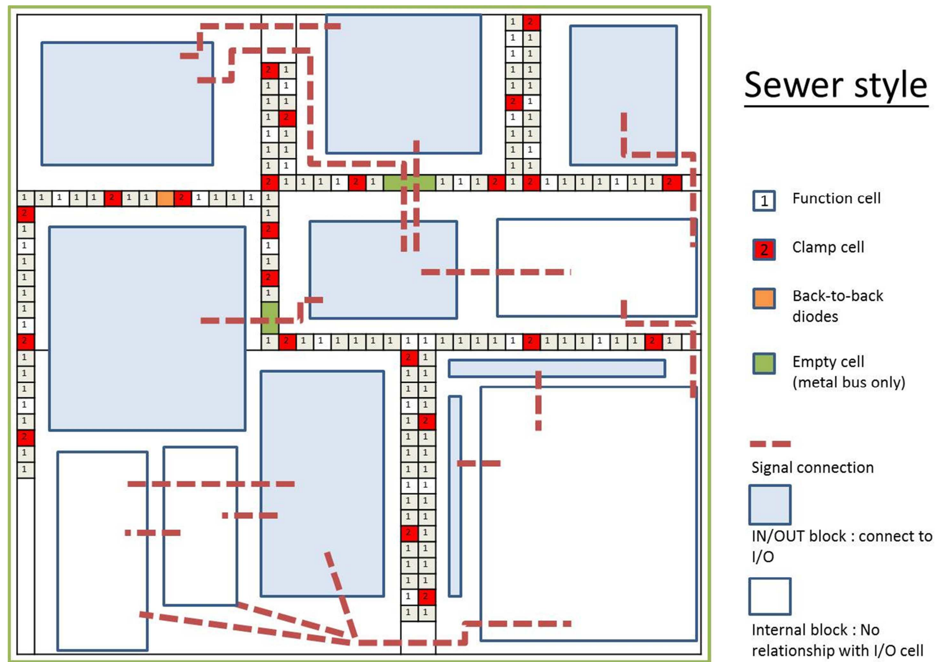
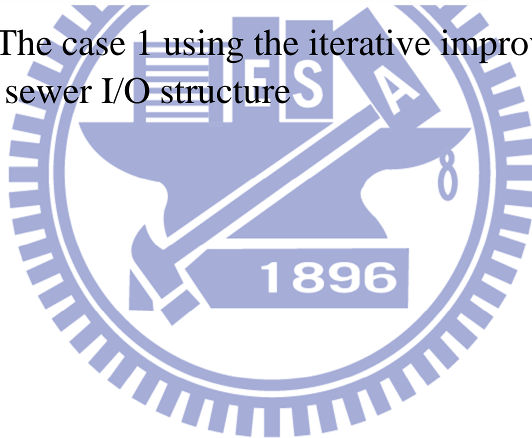


Figure 4.4 The case 1 using the iterative improvement algorithm on sewer I/O structure



- All verification results for case1

Column 1:

Violation resistance limit

Unit: metal bus resistance / cell

Column 2:

The number of violation case by using the I/O ring

Column 3:

The number of violation case by using local distribution algorithm on sewer I/O structure

Column 4:

The number of violation case by using density distribution algorithm on sewer I/O structure

Column 5:

The number of violation case by using iterative improvement algorithm on sewer I/O structure

Table 4.1 The number of violation cases for four experiments of case 1

Violation resistance limit

1	2	3	4	5
0	8126	8126	8126	8126
1	8006	7985	7984	7953
2	7881	7807	7803	7728
3	7677	7569	7540	7442
4	7451	7240	7196	7089
5	7217	6866	6805	6704
6	6931	6538	6430	6339
7	6669	6198	6080	5954
8	6448	5827	5716	5611
9	6196	5478	5359	5252
10	5934	5109	4999	4873
11	5739	4730	4642	4514
12	5520	4337	4251	4122
13	5278	3980	3864	3714
14	5099	3621	3475	3314
15	4910	3266	3131	2958
16	4688	2920	2823	2671
17	4519	2639	2519	2421
18	4354	2381	2258	2154
19	4150	2145	2023	1890
20	3974	1895	1799	1654
21	3823	1660	1544	1444
22	3642	1421	1308	1231
23	3461	1178	1078	1036
24	3325	963	853	822
25	3158	792	659	613
26	2979	638	480	441
27	2854	494	349	271
28	2709	372	246	140
29	2541	276	155	57
30	2414	200	98	15
31	2291	136	55	2
32	2139	88	28	0
33	2021	56	12	0
34	1912	32	3	0
35	1781	16	0	0
36	1662	6	0	0
37	1566	1	0	0
38	1453	0	0	0
39	1332	0	0	0
40	1243	0	0	0
41	1152	0	0	0
42	1044	0	0	0
43	965	0	0	0
44	891	0	0	0
45	801	0	0	0
46	730	0	0	0
47	667	0	0	0
48	590	0	0	0
49	526	0	0	0
50	472	0	0	0
51	412	0	0	0
52	353	0	0	0
53	312	0	0	0
54	266	0	0	0
55	221	0	0	0
56	190	0	0	0
57	155	0	0	0
58	120	0	0	0
59	95	0	0	0
60	74	0	0	0
61	57	0	0	0
62	42	0	0	0
63	30	0	0	0
64	21	0	0	0
65	15	0	0	0
66	10	0	0	0
67	6	0	0	0
68	3	0	0	0
69	1	0	0	0
70	0	0	0	0
71	0	0	0	0

As shown in Table 4.2, it is quite obvious that the case 2~3 have good improvement than the conventional I/O ring, and the iterative improvement algorithm even owns the best result in any condition of ohm limit.

4.2. Case 2

Chip size：	2400um X 2400um
I/O cell size：	60um X 60um
Pin count：	140
Number of function cell：	130
Number of clamp cell：	22 (12 cells for ESD protection enhancing)
Power structure：	one power domain
Condition of ESD estimation：	Minimum of sum of violation cases

- Conventional I/O Ring

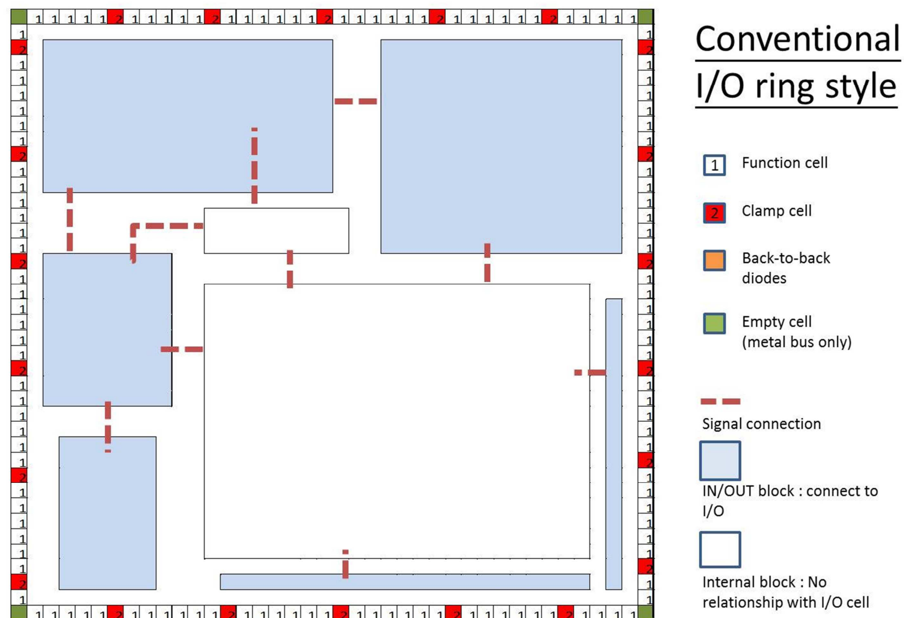


Figure 4.5 The case 2 using the conventional I/O ring

- Local distribution algorithm on sewer style I/O

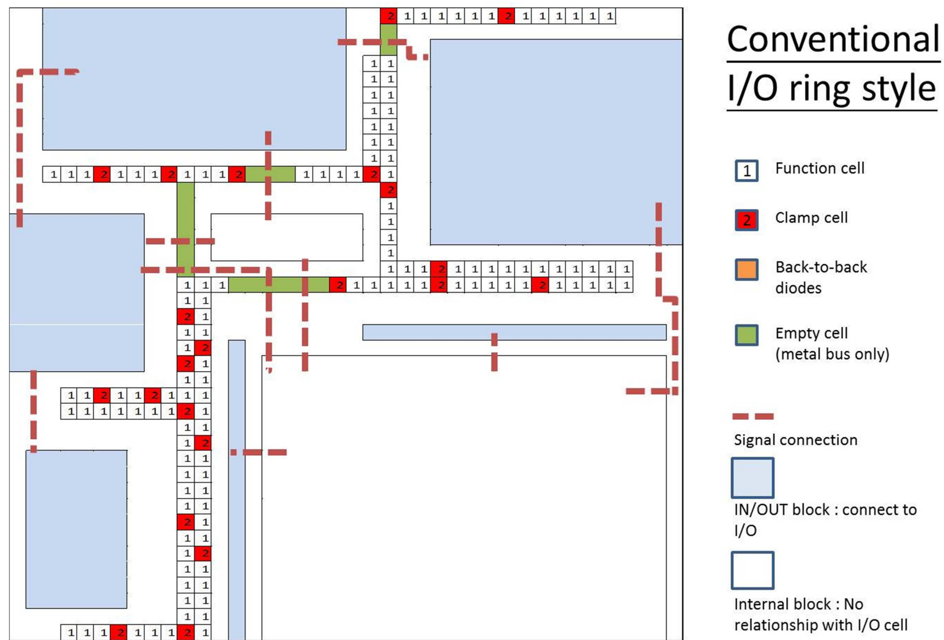


Figure 4.6 The case 2 using the local distribution algorithm on sewer I/O structure

- Density distribution algorithm on sewer style I/O

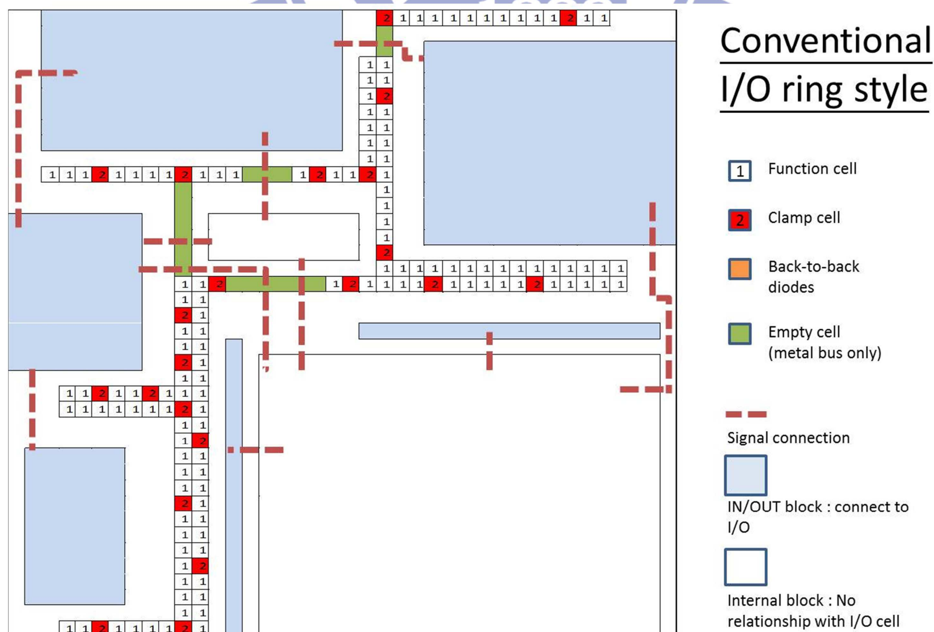
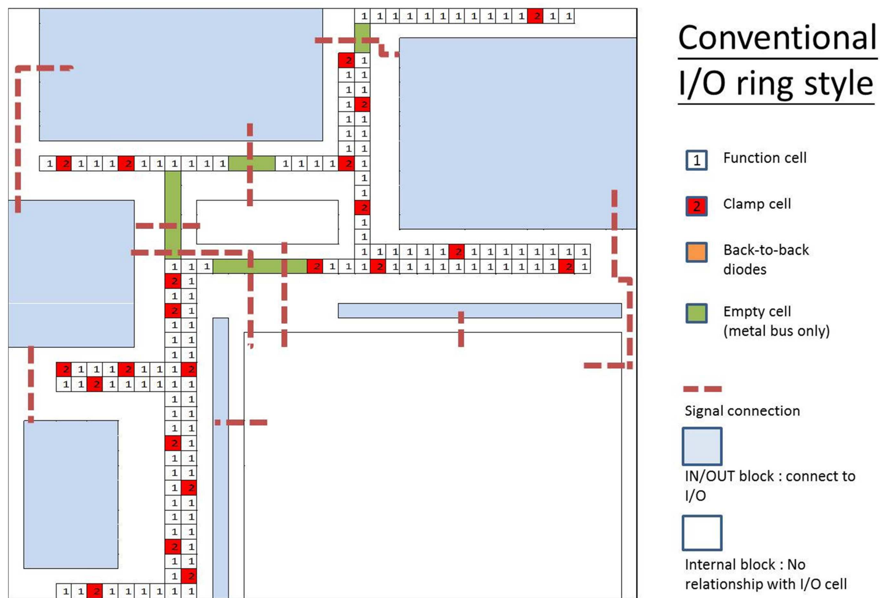


Figure 4.7 The case 2 using the density distribution algorithm on sewer I/O structure

- Iterative improvement algorithm on sewer style I/O



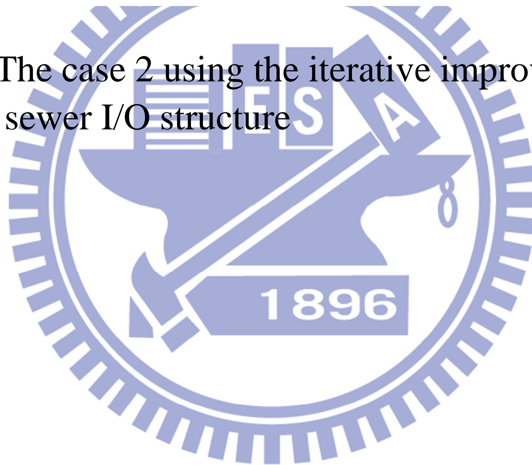


Figure 4.8 The case 2 using the iterative improvement algorithm on sewer I/O structure

- All verification results for case2

Column 1:

Violation resistance limit

Unit: metal bus resistance / cell

Column 2:

The number of violation case by using the I/O ring

Column 3:

The number of violation case by using local distribution algorithm on sewer I/O structure

Column 4:

The number of violation case by using density distribution algorithm on sewer I/O structure

Column 5:

The number of violation case by using iterative improvement algorithm on sewer I/O structure

Table 4. 2 The number of violation cases for four experiments of case 2

1 (Violation resistance limit)	2	3	4	5
0	11476	11476	11476	11476
1	11334	11336	11331	11329
2	11189	11147	11134	11118
3	10971	10856	10813	10801
4	10723	10474	10399	10414
5	10468	10064	9963	9965
6	10189	9627	9531	9540
7	9843	9195	9081	9083
8	9608	8725	8605	8590
9	9369	8204	8112	8098
10	9071	7718	7621	7616
11	8793	7210	7094	7111
12	8571	6676	6554	6572
13	8325	6170	6047	6025
14	8029	5662	5539	5484
15	7813	5147	5027	4989
16	7598	4618	4510	4503
17	7338	4128	4010	3984
18	7082	3655	3541	3469
19	6886	3181	3063	2970
20	6668	2739	2641	2507
21	6384	2331	2223	2131
22	6193	1947	1846	1799
23	6010	1599	1509	1474
24	5778	1288	1217	1205
25	5559	1020	957	956
26	5375	800	733	714
27	5181	612	549	518
28	4932	466	408	383
29	4767	336	283	281
30	4602	245	199	197
31	4406	167	130	141
32	4196	112	85	94
33	4045	74	53	55
34	3887	48	29	28
35	3689	30	14	12
36	3538	19	4	3
37	3394	11	1	1
38	3232	6	0	0
39	3040	3	0	0
40	2916	1	0	0
41	2781	0	0	0
42	2611	0	0	0
43	2481	0	0	0
44	2358	0	0	0
45	2223	0	0	0
46	2067	0	0	0
47	1961	0	0	0
48	1850	0	0	0
49	1711	0	0	0
50	1607	0	0	0
51	1511	0	0	0
52	1404	0	0	0
53	1286	0	0	0
54	1202	0	0	0
55	1119	0	0	0
56	1015	0	0	0
57	936	0	0	0
58	861	0	0	0
59	786	0	0	0
60	686	0	0	0
61	627	0	0	0
62	568	0	0	0
63	496	0	0	0
64	437	0	0	0
65	384	0	0	0
66	333	0	0	0
67	270	0	0	0
68	233	0	0	0
69	197	0	0	0
70	157	0	0	0
71	124	0	0	0
72	97	0	0	0
73	74	0	0	0
74	49	0	0	0
75	34	0	0	0
76	23	0	0	0
77	15	0	0	0
78	8	0	0	0
79	3	0	0	0
80	1	0	0	0
81	0	0	0	0

In the Table 4.2, the sum of all violation cases on chips using the sewer structure are 169123, 166332 and 165636. The iterative improvement algorithm still owns best result in this verification case.

4.3. Case 3

Chip size：	2160um X 2160um
I/O cell size：	60um X 60um
Pin count：	120
Number of function cell：	111
Number of clamp cell：	23 (14 cells for ESD protection enhancing)
Power structure：	two power domains
Condition of ESD estimation：	Minimum of sum of violation cases

- Conventional I/O Ring

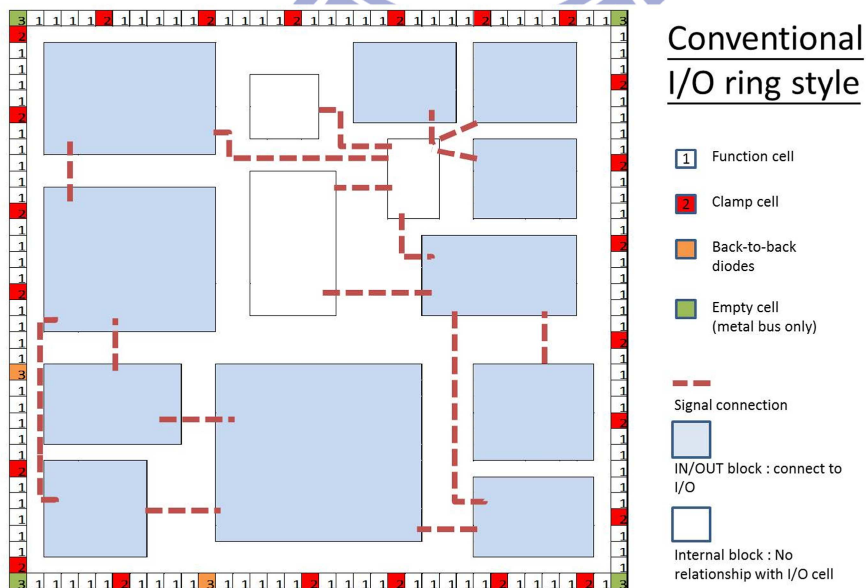


Figure 4.9 The case 3 using the conventional I/O ring

- Local distribution algorithm on sewer style I/O

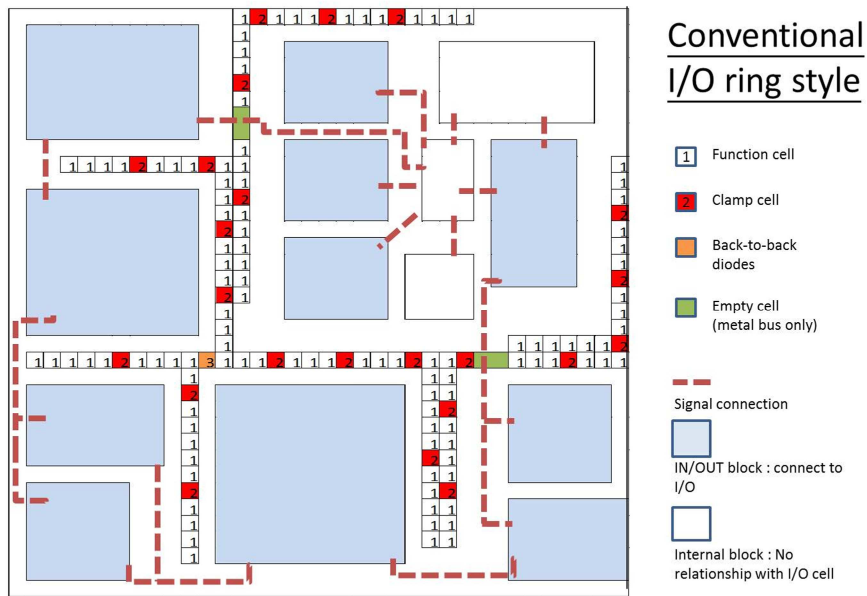


Figure 4.10 The case 3 using the local distribution algorithm on sewer I/O structure

- Density distribution algorithm on sewer style I/O

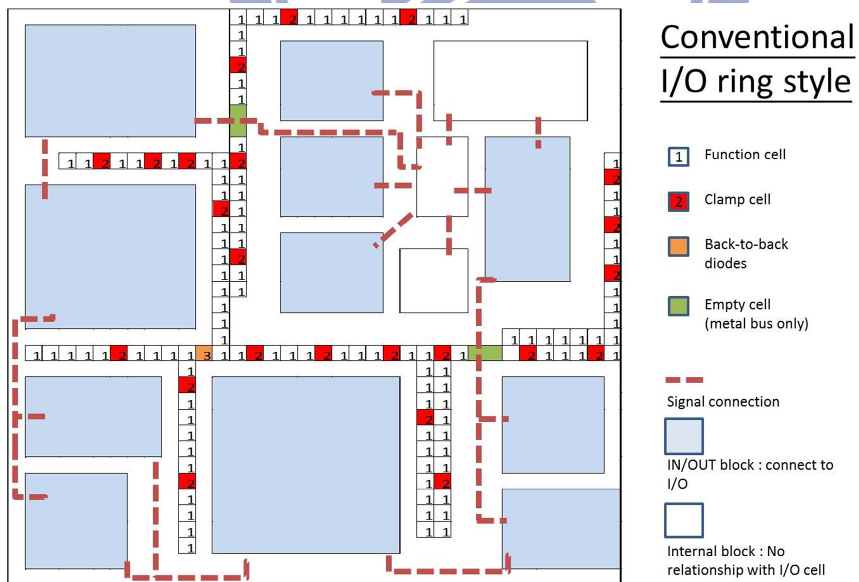


Figure 4.11 The case 3 using the density distribution algorithm on sewer I/O structure

- Iterative improvement algorithm on sewer style I/O

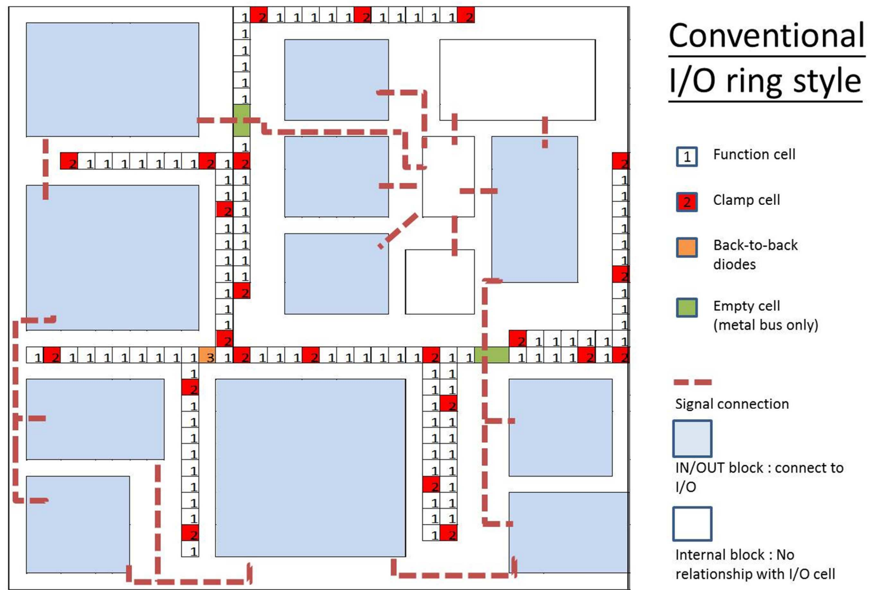
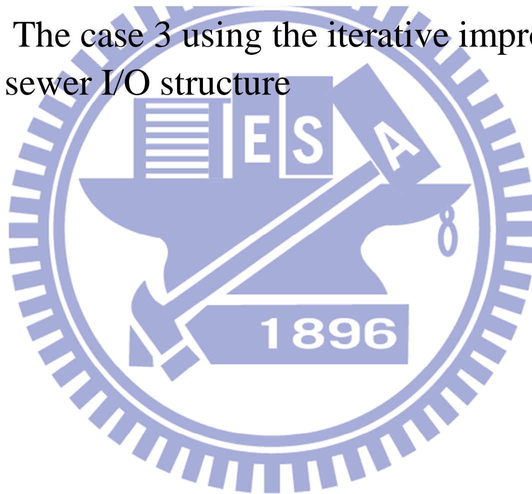


Figure 4.12 The case 3 using the iterative improvement algorithm on sewer I/O structure



- All verification results for case3

Column 1:

Violation resistance limit

Unit: metal bus resistance / cell

Column 2:

The number of violation case by using the I/O ring

Column 3:

The number of violation case by using local distribution algorithm on sewer I/O structure

Column 4:

The number of violation case by using density distribution algorithm on sewer I/O structure

Column 5:

The number of violation case by using iterative improvement algorithm on sewer I/O structure

Table 4. 3 The number of violation cases for four experiments of case 3

Violation resistance limit

1	2	3	4	5
0	6507	6507	6507	6507
1	6398	6399	6395	6380
2	6283	6243	6235	6219
3	6089	6007	5983	5966
4	5874	5711	5678	5682
5	5655	5373	5346	5354
6	5405	5028	5009	5028
7	5199	4709	4670	4708
8	4970	4395	4358	4388
9	4759	4102	4057	4054
10	4581	3805	3767	3743
11	4360	3517	3483	3462
12	4169	3229	3200	3173
13	4009	2947	2913	2879
14	3803	2661	2629	2579
15	3635	2379	2358	2300
16	3491	2124	2110	2034
17	3316	1873	1865	1796
18	3169	1653	1651	1588
19	3010	1442	1452	1417
20	2852	1249	1242	1246
21	2718	1067	1061	1057
22	2562	895	895	867
23	2424	738	736	711
24	2306	604	604	585
25	2165	485	485	463
26	2035	378	373	360
27	1927	291	280	278
28	1796	217	206	183
29	1683	159	146	114
30	1581	111	97	85
31	1468	77	68	62

Violation resistance limit

1	2	3	4	5
32	1373	52	44	37
33	1258	34	23	26
34	1158	21	13	14
35	1074	12	7	1
36	969	6	3	0
37	886	3	1	0
38	816	1	0	0
39	734	0	0	0
40	662	0	0	0
41	601	0	0	0
42	536	0	0	0
43	477	0	0	0
44	424	0	0	0
45	371	0	0	0
46	325	0	0	0
47	272	0	0	0
48	231	0	0	0
49	195	0	0	0
50	154	0	0	0
51	124	0	0	0
52	98	0	0	0
53	74	0	0	0
54	55	0	0	0
55	39	0	0	0
56	27	0	0	0
57	17	0	0	0
58	10	0	0	0
59	6	0	0	0
60	3	0	0	0
61	1	0	0	0
62	0	0	0	0

In the Table 4.3, the sum of all violation cases on chips using the sewer structure are 86504, 85950 and 85346. So we proved the concept of iterative improvement algorithm owns the better impact than the concept of average distribution from the ESD ohm’s law.

Chapter 5

Discussion

In this chapter, we analyze the impact and list benefits for our improvement method. The verification results of experiment cases transform to the curve graph to explain the impact of ESD protection in Section 5.2

5.1.Impact and Benefit

➢ Not pad-limit

In the general VLSI working flow (Figure 3.1), the evaluation of chip size is usually big to avoid the turn-around. And I/O ring structure only allows I/O cells placed around the chip edge. For these reasons, we can only insert the Decap (Decoupling Capacitance) in unused space after we completed the main chip layout and found unused space. Now, we have a new option using more clamp cells to enhance the ESD protection capability.

➢ Low detour issue

Solving the detour issue in RDL is the one of our initial propose. Sewer structure moves I/O cells to the core area of chip. The distance of routing nets in RDL can be effectively reduced. The limit of that one chain which allow up to combined by two rows of I/O cells can avoid the excessive squeeze routing in RDL as well.

➢ Low impact to original design style

Shown in section 3.1, the sewer I/O structure has low impact to the relationship

of each sub blocks. The states of all blocks still keep original structure approximately. The circuit designer can keep his working habits when he use this new I/O structure for his job.

5.2. Improvement of ESD protection

- Structure

The state of chain on sewer I/O structure has kept the enough current bases for the ESD current share. Putting the I/O cells in the core area of chip can reduce the distance between the two cell pins. Reducing the distance of pins means that improving the congenital condition of ESD protection. Sewer structure has large improve on ESD protection capability than conventional ring structure (Figure 5.1).

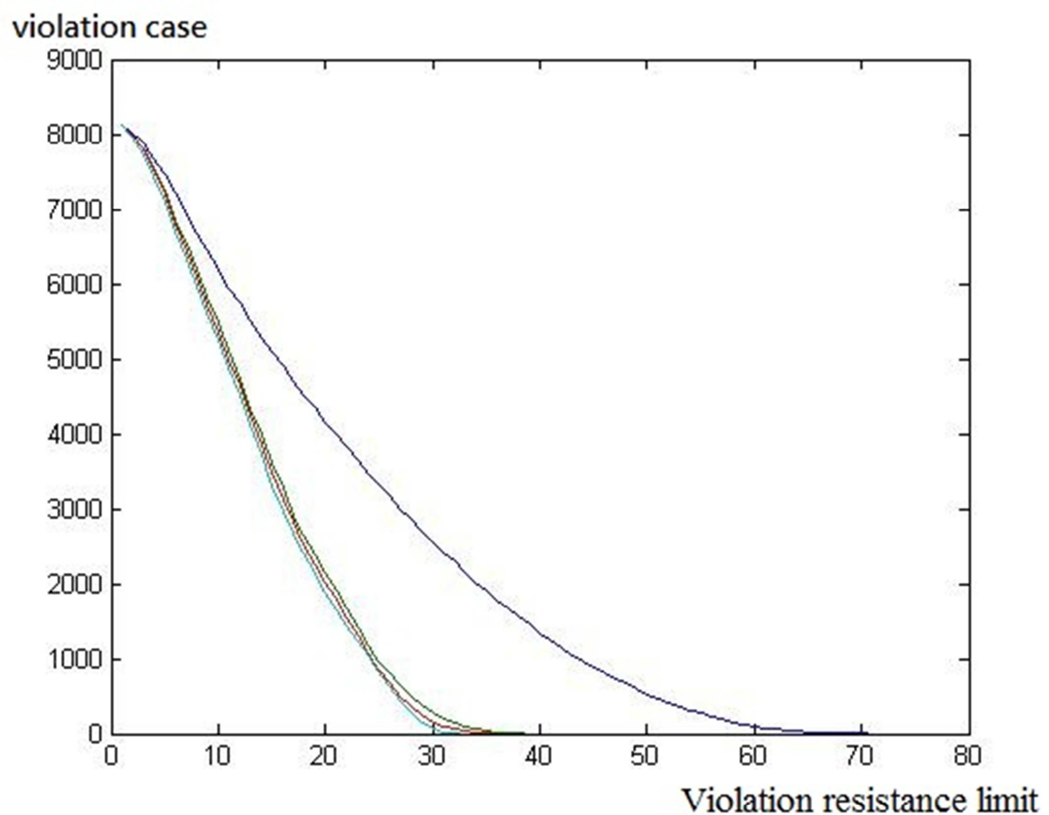


Figure 5.1 The analysis results of experimental groups and control group in case 1

➢ Distribution algorithm

In case 1 and the other cases, the cell assignment using the iterative improvement algorithm can get the best result in our experimental groups (Figure5.2).

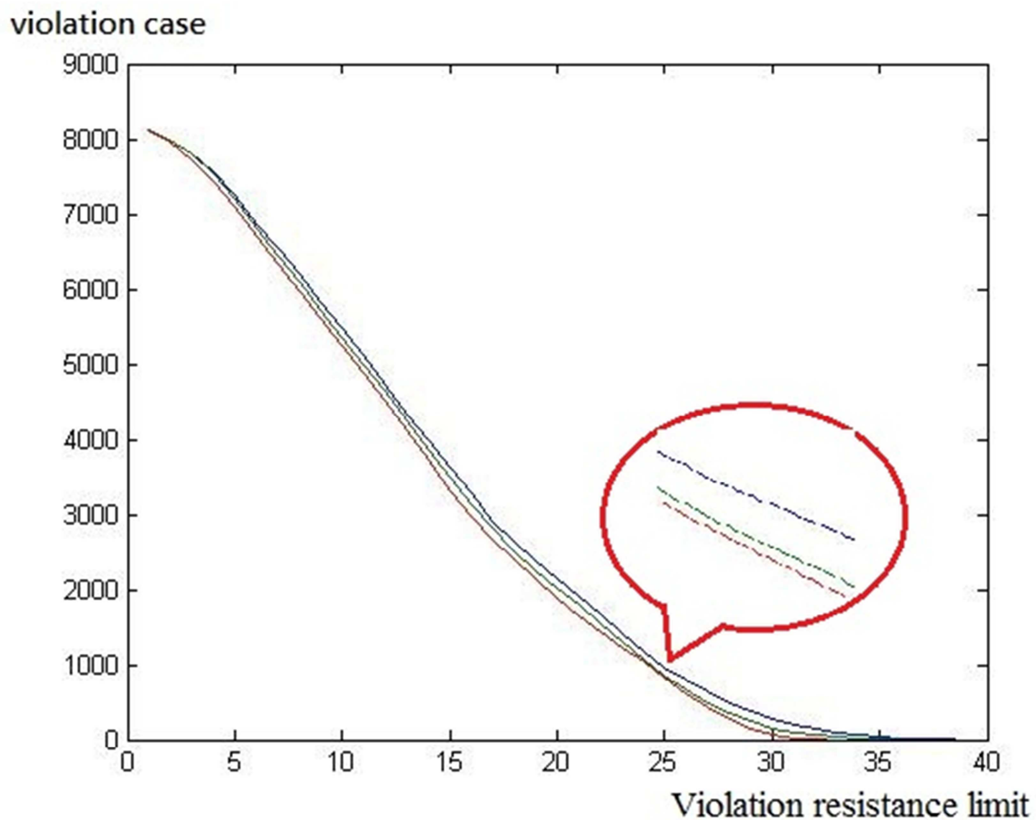


Figure 5.2 The analysis results of three experimental groups in case 1

5.3. Latch up issue

In our study, we assume that the diodes are the ESD devices in function cell. If we set the driving devices in function cell, and use the parasitic BJTs of them as the ESD devices [7], the latch up issue from driving devices has to be

considered [8].

There are two impacts of cell planning from latch up in sewer structure. First, to avoid the latch up from I/O cells, the internal circuits have to keep the appropriate distance from I/O cells. As shown in Figure 5.3, I/O ring structure owns two clearance areas on vertical direction. But there are five clearance areas on vertical direction in sewer structure of this case. The clearance areas will reduce the usable space on chip. Second, when we build the protective mechanism for latch up in I/O cells, the only direction which is chip edge to chip center should be considered. In sewer structure, there are more impacts from different directions (Figure 5.3). The I/O cell size will be increased because of this cause. Those two impacts will increase the chip size and cost when we consider the latch up issue.

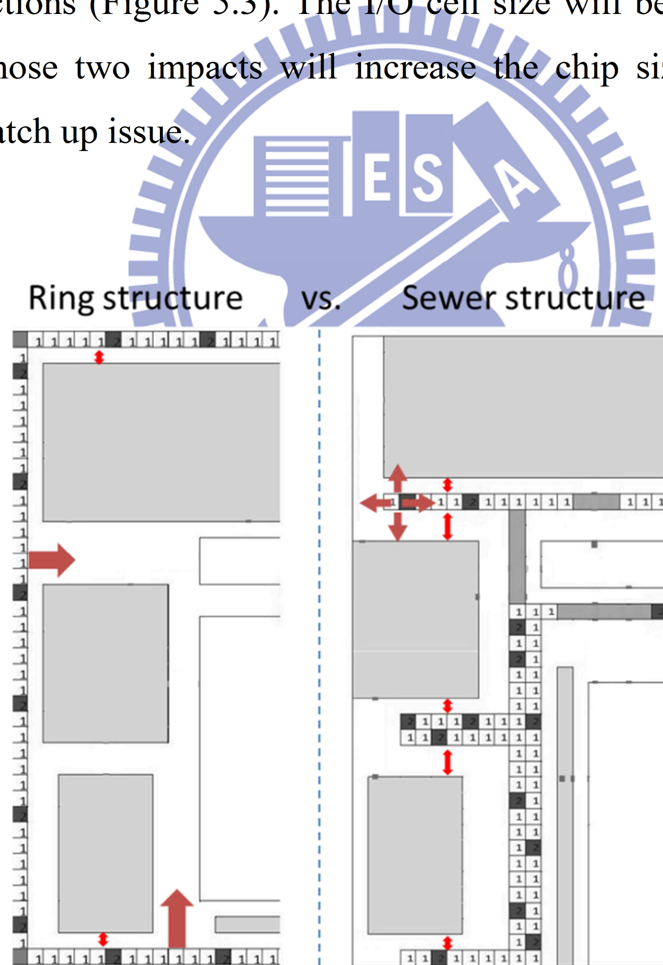


Figure 5.3 The spatial variation between Ring structure and sewer structure in the verification case 2

Chapter 6

Conclusion & future work

6.1. Conclusion

Flip chip is a mature package technology. Area-I/O is the best choice for this package. But there is few discussions using the ESD protection as the main purpose of research. In this thesis, we deliver a new sewer I/O structure as a starting point to make a research about ESD protection. After that, we refer the concept of ESD ohm's law to propose two algorithms and another whole new algorithm for cell type assignment. Finally, we provide that there are a lot of benefits in this method and it can be easily imported to general VLSI working flow.

6.2. Future work

- In this thesis, there is no discussion about the routing method in RDL [6]. We only limit the combining method of chains to avoid the intensive I/O cells increasing routing problems in RDL and internal chip space. The routing research between the bump pad array and IO cells on sewer I/O structure will be an interesting topic in the future.
- In Section 5.3, we have some discussions about the impact of latch up issue in sewer structure. For the better cost control, the I/O cell layout and distribution method based on sewer structure for latch up considerations will be a good topic as well.

References

[1] J.-W. Fang, and Y.-W. Chang, “Area I/O flip-chip routing algorithm for chip-package co-design, ” Proc. of ICCAD, pp.518-522, 2008.

[2] J.-W. Fang, D. F. Wong, and Y.-W. Chang, “Flip-chip routing with unified area-I/O pad assignments for package-board co-design,” in Proceedings of ACM/IEEE Design Automation Conference, pp. 336--339, San Francisco, CA, July 2009.

[3] J.-W. Fang , I.-J. Lin , P.-H. Yuh , Y.-W. Chang and J.-H. Wang “A routing algorithm for flip-chip design”, Proc. IEEE/Assoc. Computer Machinery Int. Conf. Computer-Aided Design, p.753 , 2005.

[4] R.-J Lee, and H.-M. Chen, “Algorithms for Chip-Package-Board Co-design ", PhD. Dissertation, National Chiao Tung University, 2011

[5] S. Voldman, John Wiley & Sons, “ESD : Circuits and Devices, ” 2006.

[6] Jia-Wei Fang; I-Jye Lin; Yao-Wen Chang, Jyh-Herng Wang, “A Network-Flow-Based RDL Routing Algorithmz for Flip-Chip Design”, IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems Vol. 26, No 8 , pp.1417 – 1429, Aug. 2007.

[7] T. Li, Y. J. Huh, and S. M. Kang, "Automated Extraction of Parasitic BJTs for CMOS I/O Circuits under ESD Stress," IEEE Int. Integrated Rel. Wkshp., Lake Tahoe, NV, October 1997, pp. 103-109.

[8] E. Haseloff, Latch-up ESD and other phenomena, Texas Instruments, application report SLYA014A, 2000.

個人簡歷

姓名：梁以正

性別：男

出生日期：1979/01/10

出生地：台中市

學習經歷：

2000 ~ 2002 : 國立雲林科技大學

2007 ~ 2011 : 國立交通大學

工作經歷：

2002 ~ 2009 : 台灣積體電路製造股份有限公司