國立交通大學

電機學院　電機與控制學程

碩士論文

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Dual Side Dual Output Switching Capacitor Voltage Converter for TFT-LCD Driver IC

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摘　要

近年來，薄膜電晶體液晶顯示面板已經成為移動或手持式電子，諸如行動電話、MP3 播放器、數位像機、PDA 以及筆記型電腦等，最重要的螢幕顯示元件。薄膜液晶顯示面板以高亮度、高彩度、反應速度快、低成本以及長壽命等優點擊敗了許多諸如超扭轉向列型以及有機發光二極體等顯示面板。因此薄膜液晶顯示驅動積體電路產業非常充滿活力。

切換電容式電壓轉換器又稱為充電幫浦，是最常應用在手持薄膜電晶體液晶顯示驅動積體電路的電源產生器。電壓轉換器是用來將系統輸入電壓轉換成高電壓，或甚至是負電壓，以供薄膜電晶體液晶顯示驅動積體電路的閘級驅動電路、源級驅動電路以及面板共電極參考電壓驅動電路等使用。

傳統的雙邊兩倍壓電壓轉換器利用兩個機動電容器來產生系統的兩倍電壓，傳統的雙邊電壓反向轉換器也是利用兩個機動電容器來產生系統的負一倍電壓。本論文提出了一個雙邊雙輸出電壓轉換器，並且成功的應用在以 SilTerra 0.13um 1.8V/5V/32V CMOS 1P5M 製程實現的 QVGA 解析度的薄膜電晶體液晶顯示驅動積體電路。這個新提出的電壓轉換器只需使用兩個機動電容器來同時產生兩倍以及負一倍的系統電壓。同時，此電壓轉換器比傳統的電壓轉換器節省了超過 27%的積體電路佈局面積、四個積體電路輸出入阜以及兩個外部電容元件，降低了生產成本。

關鍵字：液晶顯示器、切換電容式、充電幫浦

Dual Side Dual Output Switching Capacitor Voltage Converter for TFT-LCD Driver IC

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Abstract

In recent years, as a display screen, the thin film transistor-liquid crystal display (TFT-LCD) panel becomes the most popular element for mobile or handheld devices such as cell phones, mp3 players, digital cameras, PDAs, laptops, …etc. With the advantages of high brightness, rich color depth, fast response time, low cost and long life time, the TFT-LCD panel had defeated many competitors such as the super twisted nematic (STN) and the organic light emitting diode (OLED) display panel. As a result, the industry of TFT-LCD Driver is full of vigor and vitality.

The switching capacitor voltage converters which are also named the charge pumps are most commonly used in the hand-held TFT-LCD drivers for generating the power supply. The voltage converters are used to transform the system input voltage level into a higher voltage level or even a negative voltage for the use of some function blocks of the TFT-LCD drivers such as the gate drivers, the source drivers and the VCOM drivers.

The conventional dual side voltage doubler uses two flying capacitors to generate two times the system input voltage and the conventional dual side voltage inverter also uses two flying capacitors to generate negative time the system input voltage. In this thesis, a dual side dual output voltage converter is proposed. This new voltage converter is successfully implemented in a QVGA resolution TFT-LCD and is fabricated with SilTerra 0.13um 1.8V/5V/32V CMOS 1P5M process. This new proposed voltage converter uses only two flying capacitors to generate two times and negative time the system input voltage, and in the meantime, the new voltage converter saves over 27% IC layout area, 4 IC pin outs and 2 external capacitors than the conventional converters and reduces the cost.

Keywords: Liquid Crystal Display (LCD), Switching Capacitor, Chargepump

誌謝

唐代青原惟信禪師曾云：「老僧三十年前來參禪時，見山是山，見水是水；及至後來親見知識，有個入處，見山不是山，見水不是水；而今得個休歇處，依然見山只是山，見水只是水。」

在「見山是山」，追求知識的初期，人都只是看到了事物的表象，見到了什麼就認為是什麼，由於缺乏知識，判斷真假是非對錯的能力不足。到了「見山不是山」，追求知識的中期，由於得到了一些知識，開始學習如何判斷真假是非對錯，人就開始對事物充滿了懷疑，不再相信眼前所見到的事物。到了「見山依然是山」，追求知識的後期，人經歷過了對事物的懷疑與格物致知後，由於得到了許多知識並加以融會貫通，可以透徹了解事物的本質。

在職場奮鬥數年的我，正處於「見山不是山」這個十分需要良師的的階段。非常感謝指導教授　陳科宏博士在我人生的這個階段給予細心的指導與諄諄的教誨，讓我在茫茫學海中，找到了一盞明燈。俗話說「師父引進門，修行靠個人」。雖然我距離「見山依然是山」的境界尚遠，但仍感謝教授這三年的指導，給予了我一個明確的方向，讓我可以朝著目標前進。

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Contents

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Chapter 1
Introduction of TFT-LCD Driver

The evolution of thin film transistor-liquid crystal display (TFT-LCD) has four waves [1]. The first wave is the product introduction, making the world flat with the help of TFT-LCD! The application of TFT-LCD ranges from small size hand-held device to TV application from 1990 till now. The second wave is the performance enrichment, making the world gorgeous! The performance of TFT-LCD is getting more colorful, brighter, longer lifetime and faster display speed. The third wave is power and material utilization, making the world green! As the size of the display panel increases, the power consumption becomes much larger. The technology nowadays focuses to lower the power consumption of the TFT-LCD device. The fourth wave is the functions for human interface, making the world without gap! The consumers expect more functions and better performance with the improvement of the human interface technology. As a result, the TFT-LCD becomes the most glory star of the flat display panel (FDP) industry.

This chapter will show the basic topology of the TFT-LCD driver, especially applied to mobile or handheld in section 1.1 firstly. And the main function blocks of the TFT-LCD driver will be showed in section 1.2. The Power Stage, the muscle of the TFT-LCD driver in will be shown in section 1.3. Finally, the power specification of the TFT-LCD driver will be revealed in section 1.4.

1.1 TFT-LCD Driver

As shown in Fig. 1, there are several function blocks in the TFT-LCD driver. These function blocks are realize within a system on chip (SOC) for the sake of power saving and area saving.

All the function block diagrams of the TFT-LCD driver need different power sources. From Fig. 1, the Display Driver IC (DDI) inputs system power VCI into the power generation unit to generate the VCORE voltage for the timing control (TCON), VGH and VGL voltages for the gate driver, DDVDH and VCL voltages for the gamma reference circuit, the common plate voltage (VCOM) reference voltage circuit and the source driver separately. The methods of generating these analogy voltages needed in the TFT-LCD driver will be explained more detail in the later chapter. This work proposes a method to decrease the IC layout area and the number of the external flying capacitors for generating DDVDH and VCL voltages.

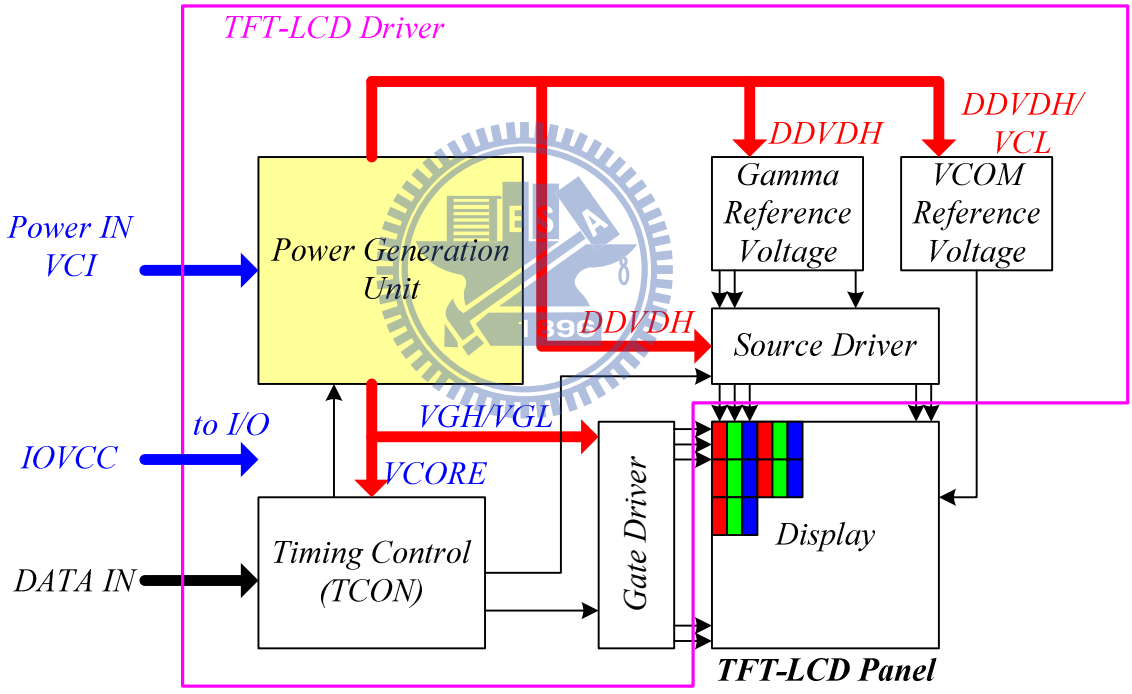


Fig. 1. TFT-LCD Driver.

The timing control unit controls all of the timing of the DDI by receiving data signals from the interface input, transfers into the gate driver, the source driver and even the power block control signals.

The gate driver is responsible for the on and off control of the thin film transistor (TFT). By receiving the control signals from the TCON, the gate driver turns on each gate line of the

TFT-LCD panel sequentially.

The source driver is responsible to charge (or discharge) the analogy voltage inside the sub-pixels of the TFT-LCD panel. The gamma reference voltage circuit generates the gamma voltage levels to the source driver. The VCOM reference voltage circuit generates the common plate voltage for the TFT-LCD panel, this voltage may be dc or ac voltage, and normally can be adjusted the voltage value by the registers in the system.

Let's gain further insight into the relationship between the gate driver, the source driver and the TFT-LCD panel. Fig. 2 is an equivalent circuit of a panel for Quarter Video Graphics Array (QVGA) resolution.

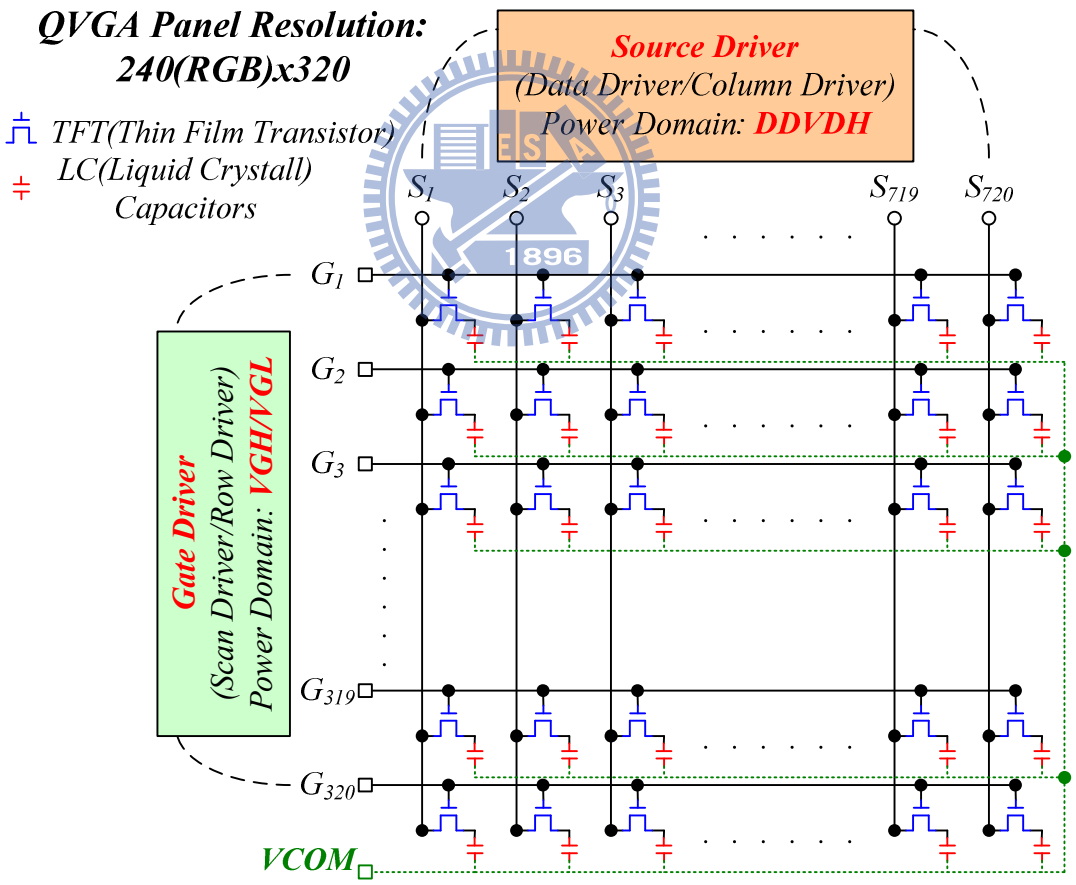


Fig. 2. Equivalent Circuit of a Panel.

A TFT-LCD panel with QVGA resolution, which is 240RGB*320, means there are total

720 source drivers and 320 gate drivers. The RGB means one pixel that includes the red, the green and the blue sub-pixels. The power domain of the source driver (also named data driver or column driver) is DDVDH. The power domain of the gate driver (also named scan driver or row driver) is VGH/VGL.

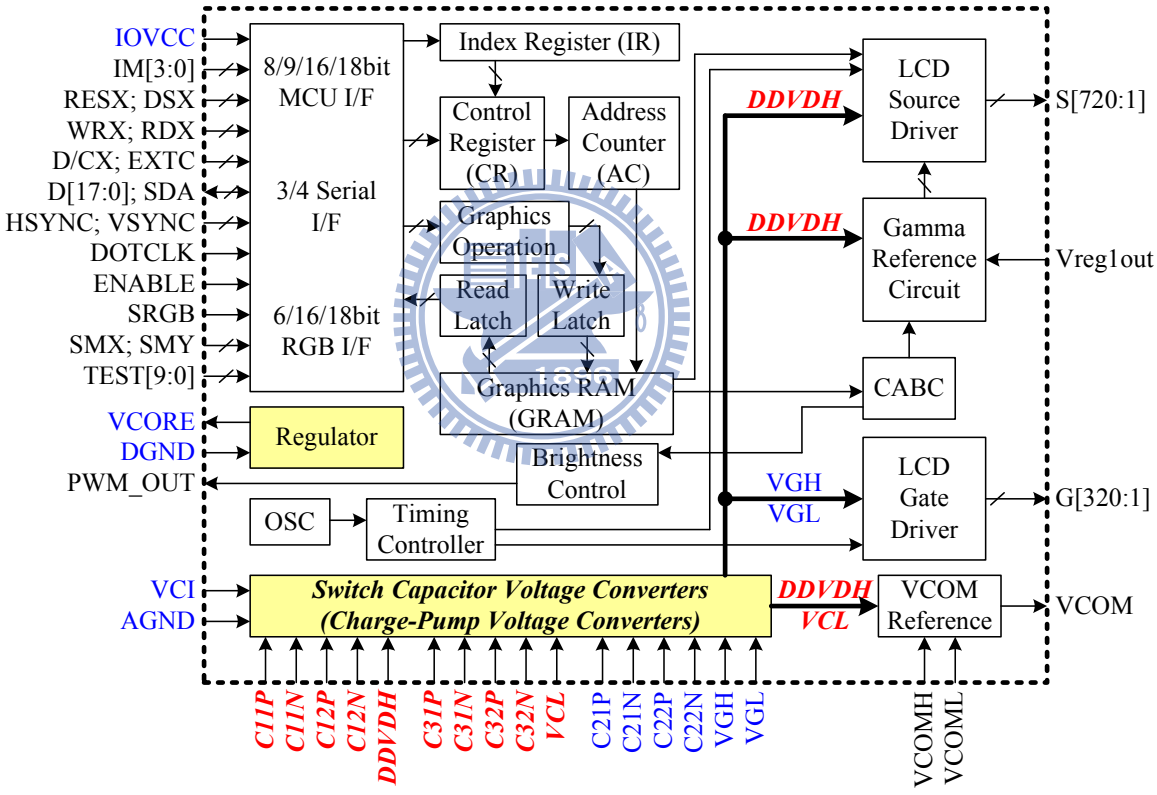
From Fig. 2, we can see each TFT is responsible for one single sub-pixel LC capacitor. The other $G_{2\sim320}$ output VGL voltage when the gate driver G_1 outputs VGH voltage. Those TFTs along G_1 direction are turned on. At the same time, source drivers $S_{1\sim720}$ output their own gray scale voltages through each TFT of the sub-pixel that G_1 turns on, and store the gray scale voltage into each sub-pixel LC capacitor before G_1 outputs VGL, turning those TFTs along G_1 direction off. And then, as G_2 outputs VGH voltage, those TFTs along G_2 direction are turned on. All source drivers $S_{1\sim720}$ output the gray scale voltages as well. After that, G_2 output VGL, turning off all TFTs. So at this time, the sub-pixels of two gate lines are charged to the desired voltage levels. By this means, $G_{3\sim320}$ are turned on or off sequentially, completing to store all sub-pixels of the TFT-LCD panel in one frame. Frame rate of 60Hz means completing update 60 frames per one second.

1.2 Block Diagram

In this keen competition industry, how to produce the lowest cost without suffer the quality of a product is a big challenge. For the TFT-LCD driver IC vendors, providing with a lower price and less external components can create a win-win situation of both the IC vendors and the module manufacturers. The conventional work uses a dual side method by two flying capacitors to generate DDVDH and VCL separately, but this work proposes a new method with dual side dual output, successfully reduces 4 IC pin outs, 2 flying capacitors and 4 power switches without sacrificing the display quality.

Fig. 3 is a traditional 262,144 colour single chip SOC driver for amorphous silicon (a-Si)

TFT-LCD panel with the resolution of 240RGB*320 dots, comprising 720 channel source drivers, 320 channel gate drivers, 172,800 bytes Graphic Random Access Memory (GRAM) for graphic data of 240RGB*320 dots, and the power supply source generation circuit. This power supply source generation circuit utilizes switching capacitor voltage converters to generate DDVDH, VCL, VGH and VGL voltage for the source driver, the gamma reference circuit, the gate driver and the VCOM reference circuit. Let's gain more insight into the TFT-LCD driver.



Traditionally: **8 pin outs** (C11P,C11N,C12P,C12N,C31P,C31N,C32P,C32N)
Proposed: **4 pin outs** (C11P,C11N,C12P,C12N)

Fig. 3. TFT-LCD Driver Block Diagrams.

1.2.1 Gate Driver

The TFT arrays of liquid crystal display panel are drive by the gate driver as Fig. 4 [2]. A

TFT-LCD gate driver is composed of the shift registers, a level shifter and a digital output buffer. The gate drivers use vertical clock (V_Clock) and vertical synchronize signal (VSYNC) to control the turn on and turn off timing of each gate driver. The level shifters are responsible for change the low dc voltage level of signals to high voltage level VGH/VGL domain. The digital buffers are responsible for the output driving capability of the gate drivers.

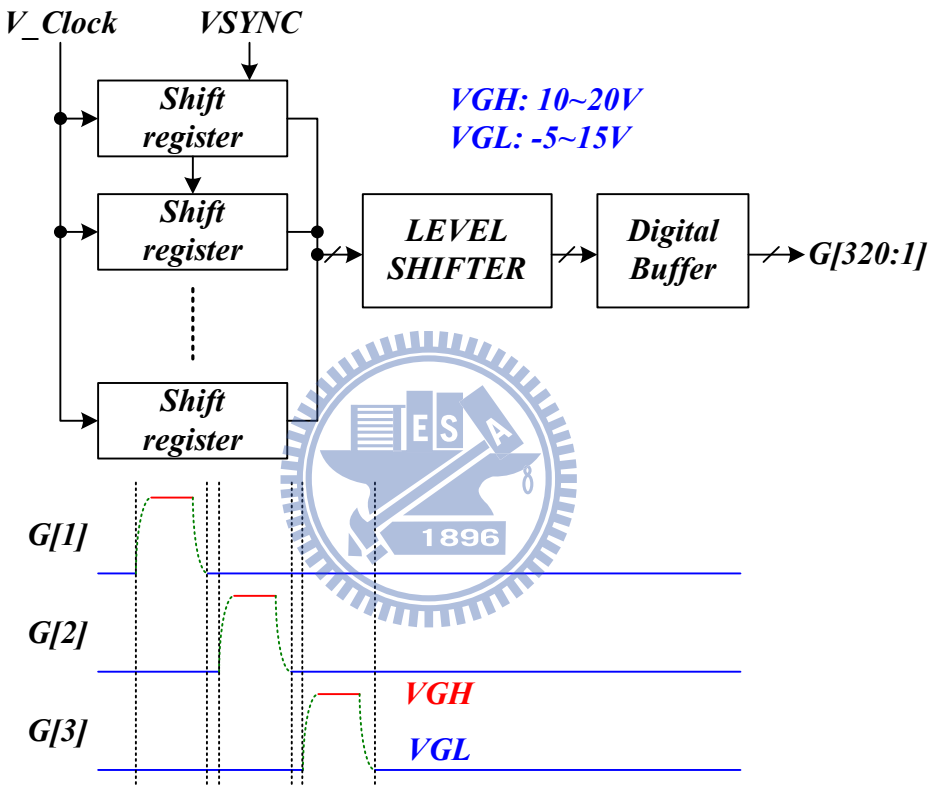


Fig. 4. TFT-LCD Gate Driver.

As in Fig. 4, the gate drivers output VGH or VGL voltage to control the on or off state of these TFT arrays. Different TFT-LCD panels possess different I-V curves of the thin-film transistors. So the switching capacitor converter generating VGH and VGL voltage should keep the elasticity of different voltage level settings.

A QVGA resolution the TFT-LCD panel comprises 240RGB*320 dots. A gate driver G[1] outputs voltage VGH to turn on the TFT array of G[1], then all source drivers S[720:1] begin

to charge each sub-pixels to the gamma voltage levels being set individually. After all the sub-pixels finish the charging action, the gate driver G[1] outputs voltage VGL to turn off the TFT array of G[1].

And then gate driver G[2] outputs voltage VGH to turn on the TFT array of G[2], then all source drivers S[720:1] begin to charge each sub-pixels to the gamma voltage levels being set individually. After all the sub-pixels finish the charging action, the gate driver G[2] outputs voltage VGL to turn off the TFT array of G[2].

Following this rule, after the last gate driver G[320] finishes this action, a frame picture is written and displayed on the TFT-LCD panel. Frame rate 60Hz means the TFT-LCD driver updates 60 frame data per one second.

1.2.2 Gamma Voltage Generator

Vreg1out is an important power source in the TFT-LCD driver. It plays the role of a power source of the gamma voltage generator circuit. Fig. 5 shows a linear regulator that produces a voltage power Vreg1out. This regulator would adopt a cap-free [12] design in some low cost solution projects.

This linear regulator is composed of a VREFGEN circuit, an error amplifier, a pass element and a feedback network. The VREFGEN circuit provides various reference voltage levels. As to the error amplifier, it amplifies the error amount of the reference voltage and the feedback voltage. After receiving the amplified error voltage, the pass element of Vreg1out regulator as a PMOS, adjusts the output Vreg1out voltage to a suitable level. Finally is the feedback network, comprising of resisters, is responsible for providing the weight of Vreg1out as the feedback voltage.

In real case application, Vreg1out power source should keep the elasticity of a wide voltage range as Fig. 5 showed. We can count on the registers VRH[5:0] to select the exact

reference voltage levels from the VREFGEN circuit for the Vreg1out regulator.

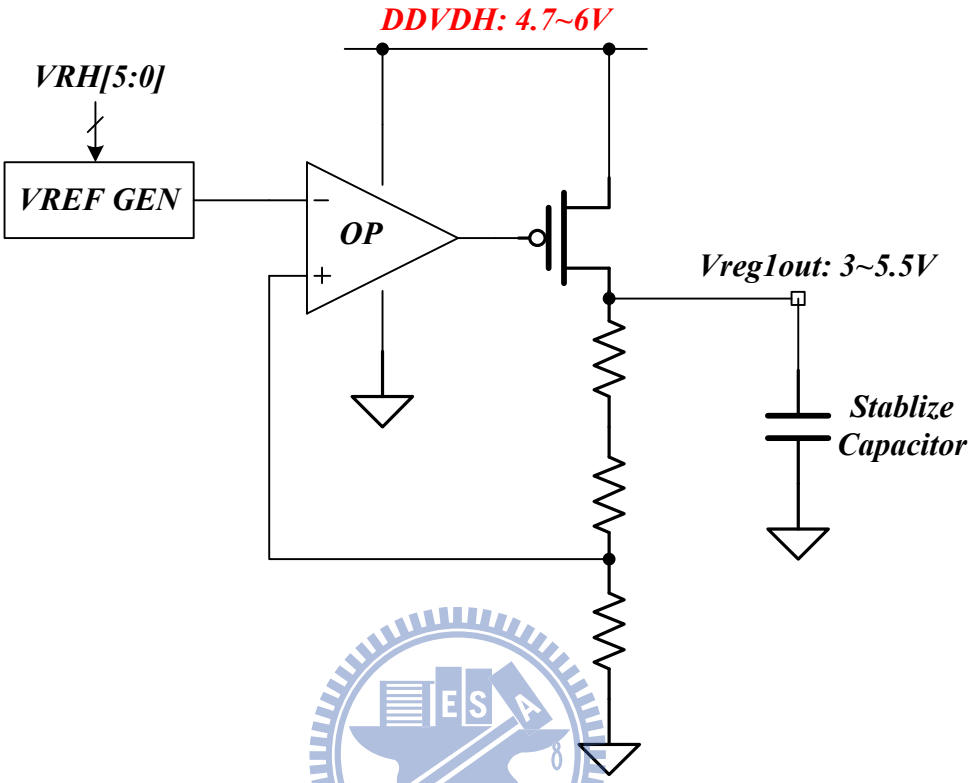


Fig. 5. Vreg1out regulator: Reference Power of Gamma Voltage Generator.

The simplest distinction of brightness and darkness is binary level. It means just only bright and dark. For a RGB sub-pixel display, if all RGB sub-pixels only exists two states of bright and dark state, the display color depth equals to 2 bits. That is to say, the panels can only display 8 kinds of color. In the real world, even mono color such as black, exists different gray levels. And each gray level exhibits a different shading value to human eyes. In order to realize the nature images seen by the human eyes, the need of gray levels is necessary.

This work utilizes 6 bits color depth. That means R or G or B color exists 64 gray levels individually. That is to say, the TFT-LCD driver can display 262,144 kinds of color on the TFT-LCD panel.

In Fig. 6, we can realize that the Gamma Voltage Generator circuit is used to generate 64 gray levels of voltage for 6 bits color depth.

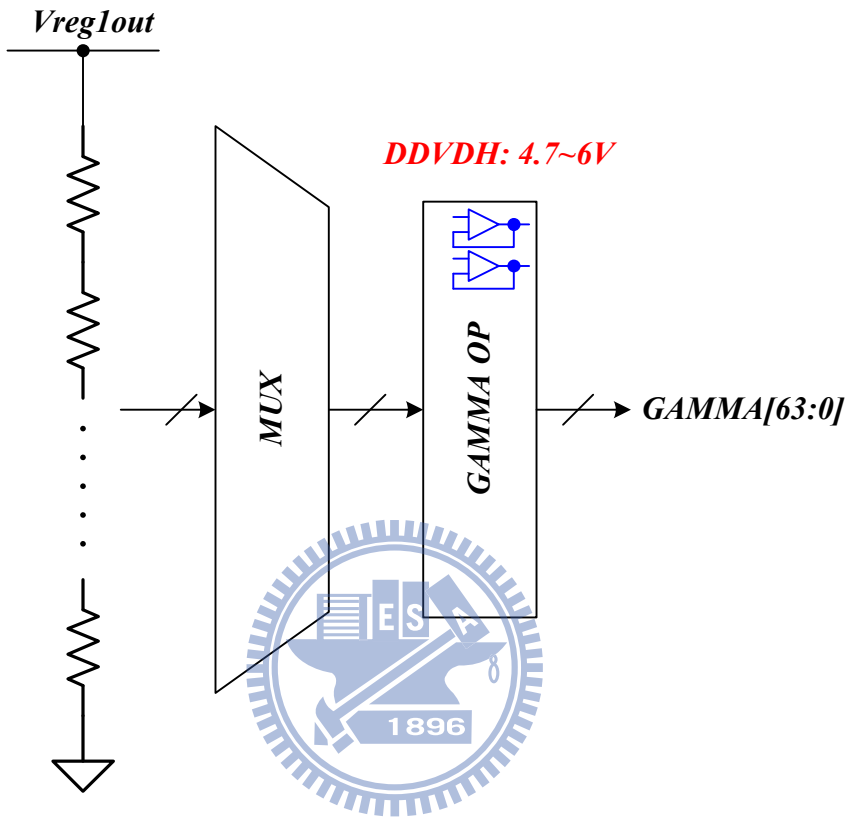


Fig. 6. Gamma Voltage Generator.

The generator circuit comprises a resister type voltage divider, a mux, and the gamma operation amplifiers. The resister type voltage divider uses Vreg1out as a reference power source, and divides various sets of reference voltage as the reference voltage of the gamma operation amplifiers. The mux circuits select the relative reference voltage by the registers for the gamma operation amplifiers. The gamma operation amplifier always configures as an unity gain topology and plays the role of an analogy output buffer of the 64 gray levels.

The liquid crystal is a kind of a light gate. The transmitted luminance depends on the rotate angle of the liquid crystal molecules controlled by the voltage applied across the top

plate and bottom plate of the TFT-LCD panel. As in Fig. 7, the LC voltage means the voltage applied across the TFT-LCD panel. Each voltage level relates to different transmitted luminance.

An opposite sign of the LC voltage results in an opposite rotate angle, but however, relates to the same transmitted luminance. We will introduce in the later section. This is what the polarity change method does. The polarity change method must be applied to increase the lifetime of a TFT-LCD panel and prevents it from dc residue effect.

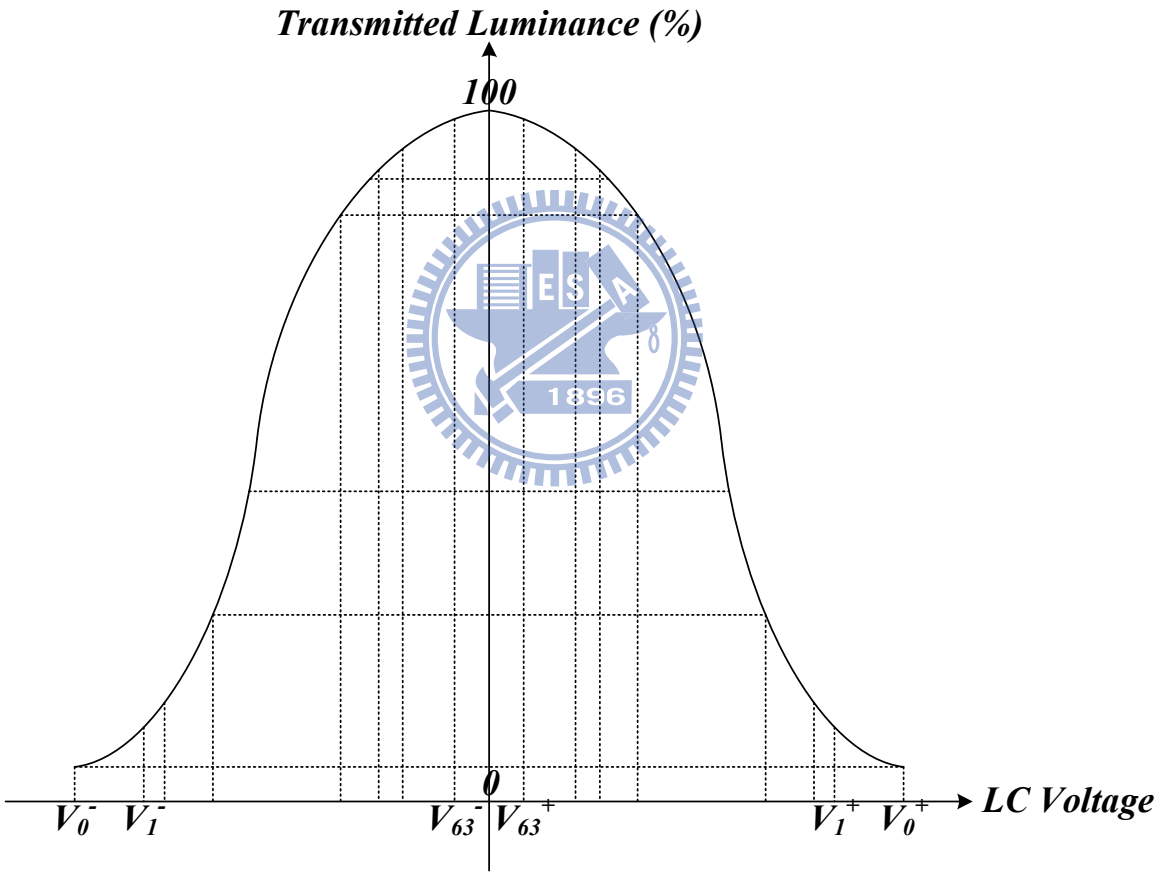


Fig. 7. LC Gamma Curve.

1.2.3 Source Driver

The source drivers charge display data voltage to the selected liquid crystal storage

capacitors and liquid crystal capacitors of a TFT array on a TFT-LCD panel, which is turned on by the selected gate driver. For a resolution of QVGA 240RGB*320, the source drivers S[720:1] need to charge 320 sub-pixels individually and sequentially to complete one single frame data. For 60 Hz frame rate, the source drivers need to drive 60 frame data in one second.

In Fig. 8, the TFT-LCD source drivers [2] are composed of the shift registers, the latches, the level shifters, the DACs (digital to analogy converter) and the source operation amplifiers.

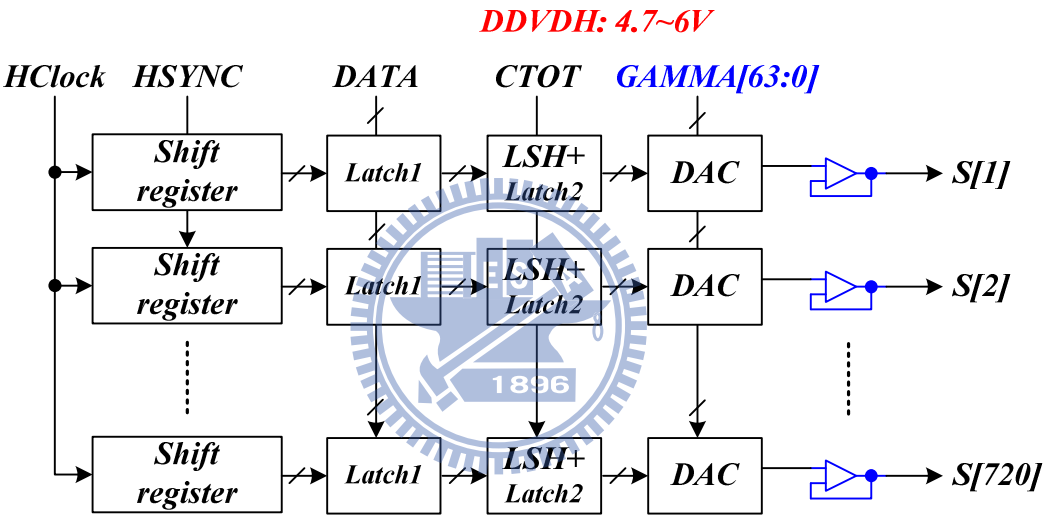


Fig. 8. TFT-LCD Source Driver.

The display DATA are latched in latch1 through the shared 18 bits data bus. The source drivers use HClock (horizontal clock signal) and HSYNC (horizontal synchronize signal) to control the shifter registers to store the display DATA sequentially into each latch1 of the source drivers. Then the display DATA are stored into the latch2 and the level shifter by the CTOT signal. The CTOT signal is a signal similar to the HSYNC signal. After that, the display DATA select the desired gamma gray level voltages by DAC circuit, and at last, the source operation amplifiers which are configured as analogy unity gain output buffers, are

responsible for driving the desired gamma gray level voltages into the selected sub-pixels.

Fig. 9 shows a self-biased folded cascode rail-to-rail operation amplifier [13]. The source op-amplifiers are used to drive 64 gamma gray scale voltage levels into the TFT-LCD panel. The op-amplifiers should be able to drive signals range within full range from DDVDH to ground because of the voltage range of 64 gamma gray scale voltage levels are almost full range from DDVDH to ground. For a QVGA resolution with 240RGB*320, there must exist 720 source drivers which contain 720 source op-amplifiers. The total dc static operation current for source op-amplifiers is very large if we use the conventional two-stage op-amplifier. A Self-biased and class AB folded cascode op-amplifier is a very suitable solution to the source drivers.

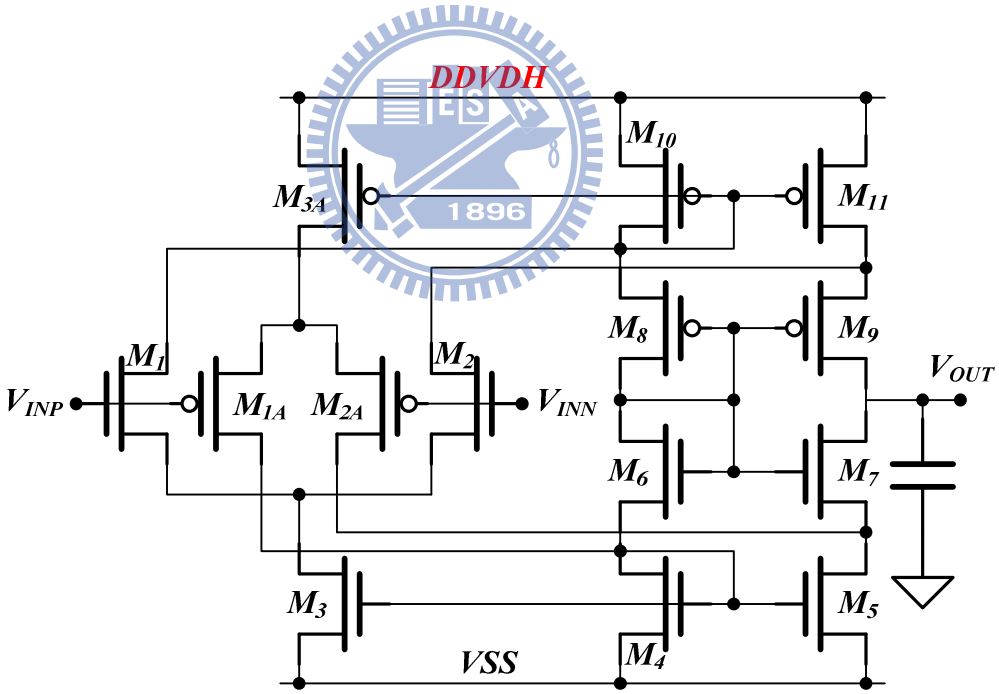


Fig. 9. Self-biased Folded Cascode Rail-to-rail Op-amplifier.

1.2.4 Data Driving Method

Before introducing the VCOM driver, we need to discuss the data driving method of the

TFT-LCD driver first. The liquid crystal acts like the light gate, controlled by the voltage across it, to adjust the angle of the liquid crystals, resulting in brightness control. Unlike the spontaneous light emitting display panel, the TFT-LCD panel need extra backlight source such as Cold Cathode Fluorescent Light (CCFL) or Light Emitting Diode (LED) to display a picture.

The electric field applied to the liquid crystals is oriented. If we change the electric field with an opposite direction, that is so-called polarity change [2]. This polarity change would not and should not result in the transmitted luminance of the liquid crystals, but the angles of them. Because the DC blocking effect of the orientation layer and the dc residue effect of TFT-LCD panel, we must apply polarity change by line or by frame.

There are two methods of polarity change, which will be explained in the following contexts. Fig. 10 shows the inversion types adopted in the TFT-LCD driver to do the polarity change for preventing the liquid crystals from dc residue effect and increase life time.

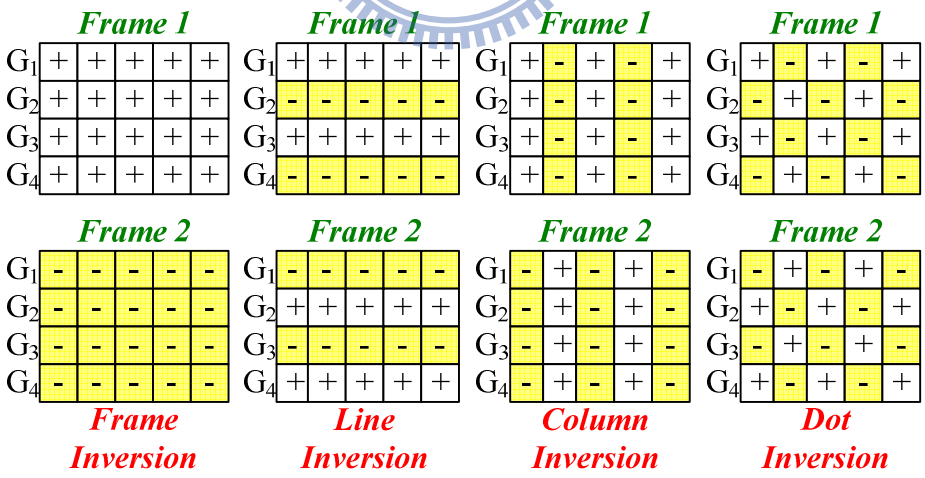


Fig. 10. Inversion Types of TFT-LCD Driver.

Frame inversion updates the pixel voltage polarity in the form of frame. We can see all of the sub-pixels in frame 1 are positive, and in frame 2 are negative.

Line inversion updates the pixel voltage polarity in the form of line (gate driver

direction). We can see in frame 1, the sub-pixels of G_{ODD} are positive and those of G_{EVEN} are negative. But in frame 2, the sub-pixels of G_{ODD} are negative and those of G_{EVEN} are positive.

Column inversion updates the pixel voltage polarity in the form of column. We can see in frame 1, the sub-pixels of S_{ODD} are positive and those of S_{EVEN} are negative. But in frame 2, the sub-pixels of S_{ODD} are negative and those of S_{EVEN} are positive.

Dot inversion updates the pixel voltage polarity in the form of pixel. We can see in frame 1, all of the polarity of the sub-pixel is contrary to the neighbor ones. And in frame 2, all of the polarity of the sub-pixel change.

AC VCOM Data Driving Method

VCOM voltage is a reference common electro plate voltage inside the panel. AC VCOM means the VCOM voltage level changes polarity by line or by frame to avoid the dc residue effect of the liquid crystals. In Fig. 11, VCOM voltage changes polarity by line or by frame between the voltage level VCOMH and VCOML. The VCOMH and VCOML voltage depend on the LC characteristics for the different panel makers.

In the positive polarity period, the voltages across the liquid crystals are gray scale voltages ($V_0^+ \sim V_{63}^+$) minus VCOML, these voltages are the positive sign voltages, and then, in the negative polarity period, the voltages across the liquid crystals are gray scale voltages ($V_0^+ \sim V_{63}^+$) minus VCOMH, these voltages are the negative sign voltages.

If we well adjust VCOMH and VCOML voltage level to let the positive sign voltage just equal to the absolute value of the negative sign voltage, by doing so can prevent the liquid crystals from dc voltage residue and increase their life time.

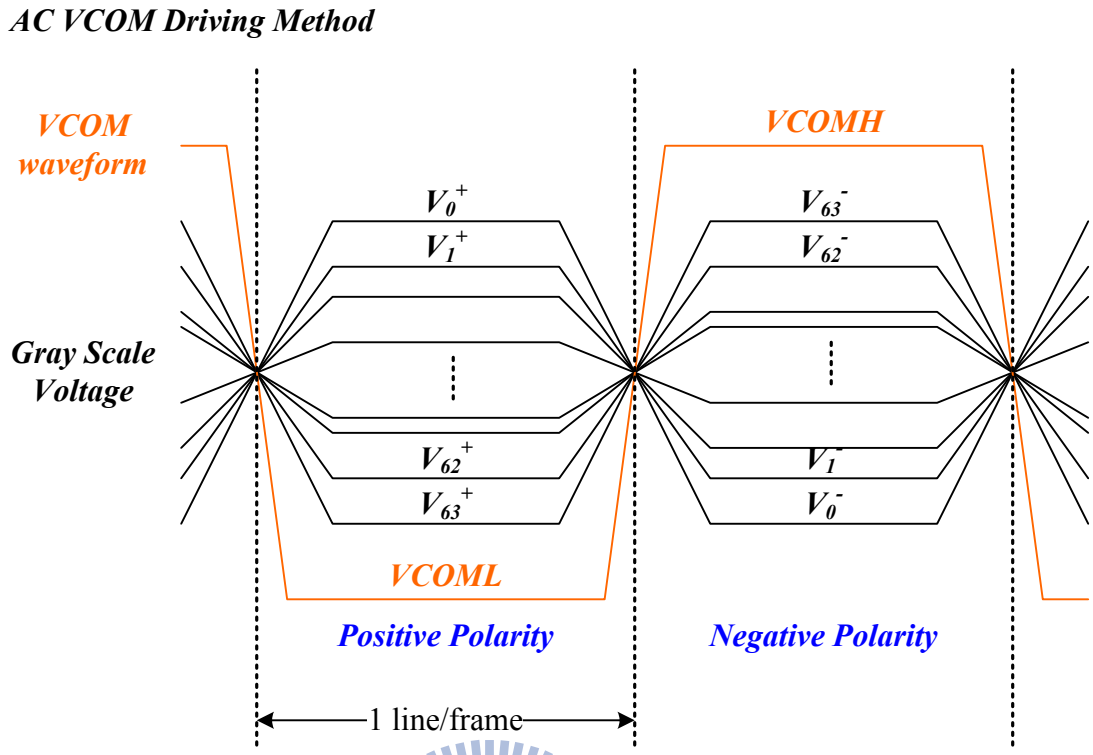


Fig. 11. AC VCOM Driving Method.

DC VCOM Data Driving Method

Fig. 12 shows the DC VCOM driving method. DC VCOM means the VCOM voltage level always keeps a dc value at anytime. By this way, the job of polarity change is controlled only by the source drivers.

In the positive polarity period, the voltages across the liquid crystals are gray scales voltage (V_0^+ ~ V_{63}^+) minus VCOM, these voltages are the positive sign voltages, and then, in the negative polarity period, the voltages across the liquid crystals are gray scale voltages (V_0^+ ~ V_{63}^+) minus VCOM, these voltages are the negative sign voltages.

If we well adjust VCOM voltage level to let the positive sign voltage just equal to the absolute value of the negative sign voltage, by doing so can prevent the liquid crystals from dc voltage residue and increase their life time. But different from the AC VCOM, the gray scale voltages range (V_0^+ ~ V_{63}^+) of the DC VCOM method must large than the AC VCOM to

maintain the same voltage levels across the liquid crystals.

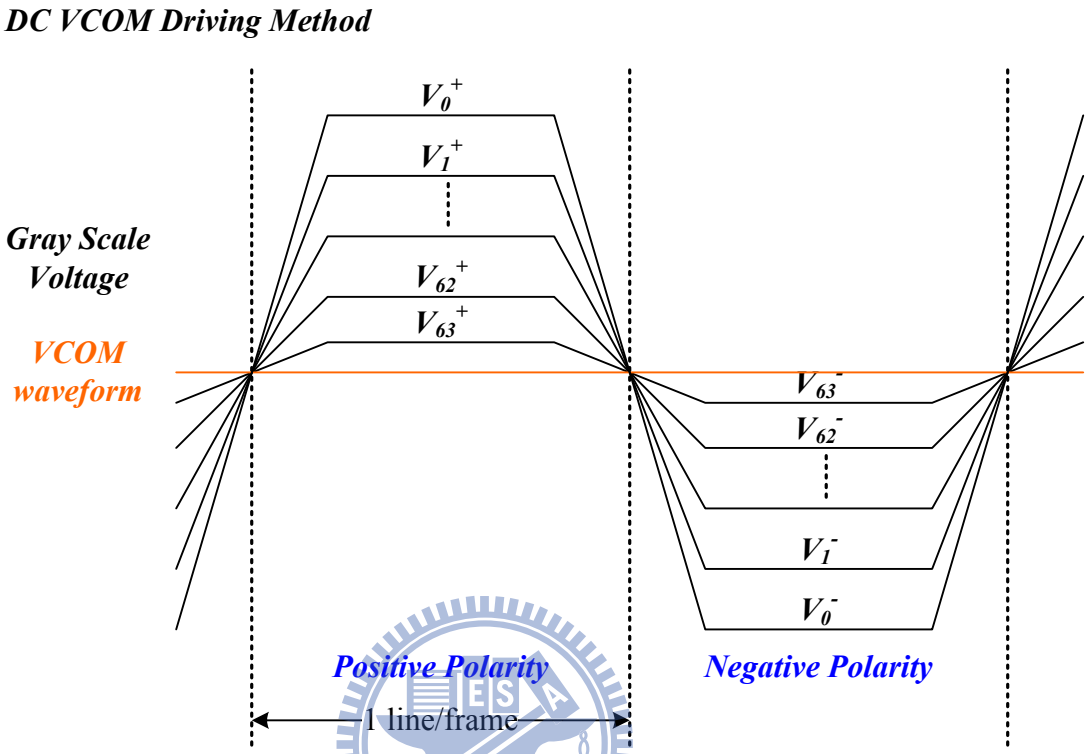


Fig. 12. DC VCOM Driving Method.

Comparison Between AC VCOM and DC VCOM

TABLE I. shows the advantages and disadvantages comparisons of AC VCOM and DC VCOM. Let's gain further insight into the differences between the AC VCOM and the DC VCOM data driving method.

For example, in AC VCOM case, assume

Gray scale voltage $V_0^+ = 4V$

Gray scale voltage $V_0^- = 0.5V$ (1)

VCOML voltage $VCOML = -0.5V$

VCOMH voltage $VCOMH = 5V$

In the positive polarity, the voltage across the liquid crystal is 4.5V, and in the negative polarity, the voltage across the liquid crystal is -4.5V. Because the Gray scale voltage range is 4V to 0.5V, the source driver only need the 5V device for this design.

In DC VCOM case, assume

$$\text{Gray scale voltage } V_0^+ = 4V$$

$$\text{Gray scale voltage } V_0^- = -5V \quad (2)$$

$$\text{VCOM voltage } VCOM = -0.5V$$

In the positive polarity, the voltage across the liquid crystal is 4.5V, and in the negative polarity, the voltage across the liquid crystal is -4.5V. Because the Gray scale voltage range is 4V to -5V, the 5V device can not meet this design in the source driver. In this case, the source driver needs the 12V device and this will increase the wafer cost.

In TABLE I, the image quality of DC VCOM is better than AC VCOM, but the cost of DC VCOM is more than AC VCOM because the higher voltage process is needed. This work uses AC VCOM for design because the cost of AC VCOM is lower than DC VCOM.

TABLE I. COMPARISONS OF DATA DRIVING METHODS

Characteristics	*AC VCOM*	*DC VCOM*
Inversion Type	***Frame, Line inversion***	***Frame, Line, Column, Dot inversion***
Image quality	***Poor***	***Better***
Power dissipation	***Higher***	***Lower***
Process	***Lower voltage process***	***Higher voltage process***
Cost	***Lower***	***Higher***

1.2.5 VCOM Driver

The liquid crystals of the sub-pixel, as a light gate of TFT-LCD panel can be regarded as a capacitor with two parallel electrode plates. Inside a sub-pixel of TFT-LCD panel, one of the electrode plates is isolated individually with the other sub-pixels, connects to the thin film transistor and expands to two-dimensional arrays together with all the other sub-pixels. Another electrode plate of the sub-pixel, named as VCOM (the common electrode plate) is actually shared with all sub-pixels of the panel. The VCOM voltage level plays the role of the reference voltage of all liquid crystals of a TFT-LCD panel. We can change the VCOM voltage level to eliminate the flicker effect of a TFT-LCD panel [14]. The voltage difference across the two plates of a sub-pixel is direct proportional to the electric field intensity be applied to the liquid crystal, and is also proportional to the transmitted luminance of the liquid crystal.

The VCOM driver is used to provide the reference common electrode plate voltage of the TFT-LCD panel. As mentioned in the last section, there are two methods to fulfil the liquid crystal polarity change in LCD driving. The liquid crystal polarity change is responsible for increasing the lifetime of the liquid crystal, and also preventing the liquid crystal from the dc residue effect. This work utilizes AC VCOM driving method for polarity change.

Fig. 13 shows the structure of the VCOM driver. The VCOM driver is composed of a reference voltage generation circuit, two operation amplifiers and an analogy output buffer.

The reference voltage generation circuit is responsible for providing the reference voltages for VCOMH and VCOML, controlled by VMH[6:0] and VML[6:0] registers. OP1 is a p-type (PMOS as input device) folded cascode operation amplifier, generates VCOMH voltage for the VCOM driver. OP1 uses DDVDH and VSS as power and ground because of the VCOMH voltage specification range is between 2.7V to 5.875V. OP2 is a n-type (NMOS

as the input device) folded cascode operation amplifier, generates VCOML voltage for the VCOM driver. OP2 uses VCI and VCL as power and ground because of the VCOML voltage specification range is between 0V to -2.5V. At last, the analogy buffer is responsible for output the AC VCOM voltage level into the TFT-LCD panel. The POL (polarity) signal is used to control the analogy buffer to output the VCOMH voltage level when the POL signal at high level, and when the POL signal is at low level, the analogy buffer outputs the VCOML voltage level.

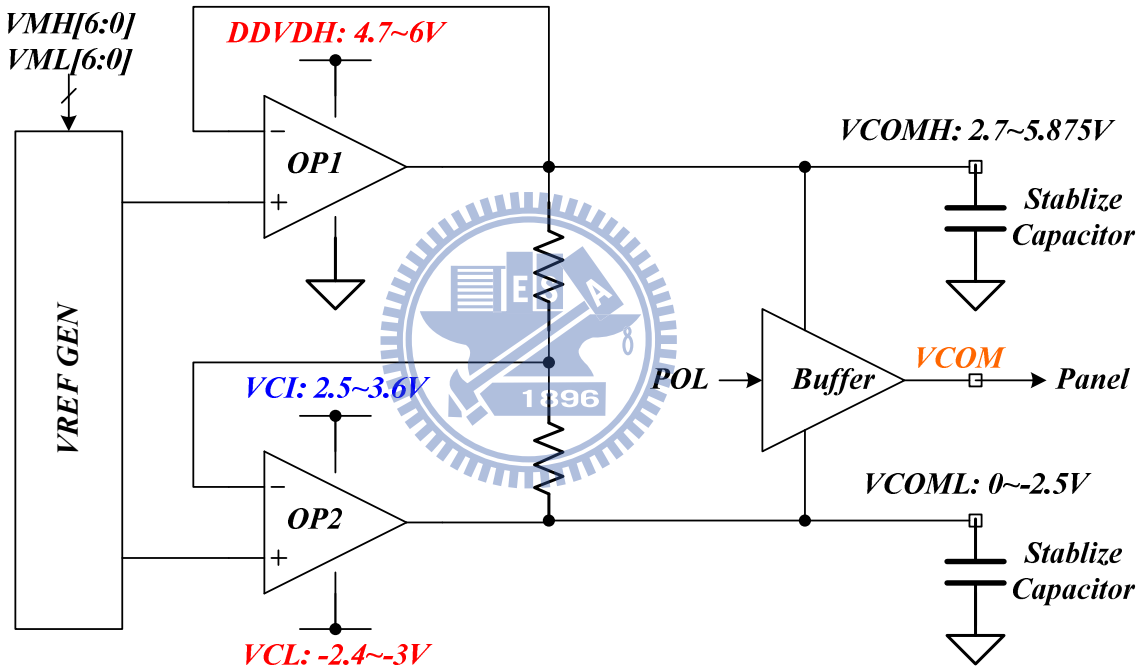


Fig. 13. TFT-LCD VCOM Driver.

1.3 Power Stage Selection

In Fig. 14 [3], in a cell phone module system, the system power supply comes from the battery. Function blocks such as PA (power amplifier), LNA (low noise amplifier), Analogy R/F (radio frequency), Baseband, Display (TFT-LCD), Audio and Interface, need different power supply sources. And there are 4 choices of power supply: 1) nothing, directly from

battery, 2) LDO, 3) switching capacitor, 4) inductor switching regulator.

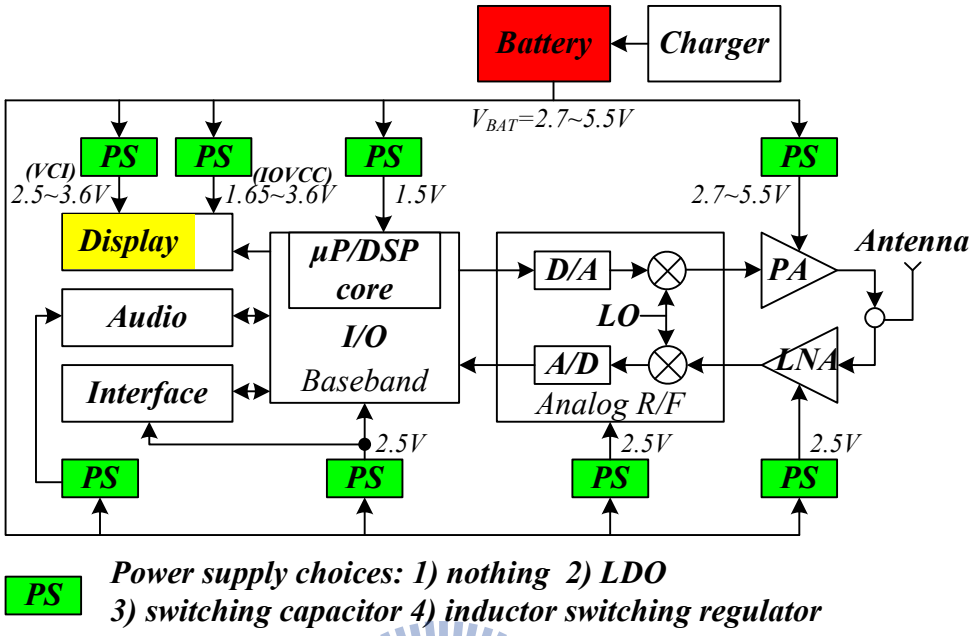


Fig. 14. Power supply of Cell Phone System.

Based on the functions and the power consumption budgets, every power supply sources may have different choices.

1.3.1 Linear Regulator

Linear Regulator as Fig. 15 [4] shown, is composed of a reference voltage circuit, an error amp, a pass element and a feedback element. Early days architectures need an extra stabilize capacitor, but nowadays, many new proposed architectures with multi-stage design, miller compensation, and nested miller compensation had been accomplished cap-free design [12].

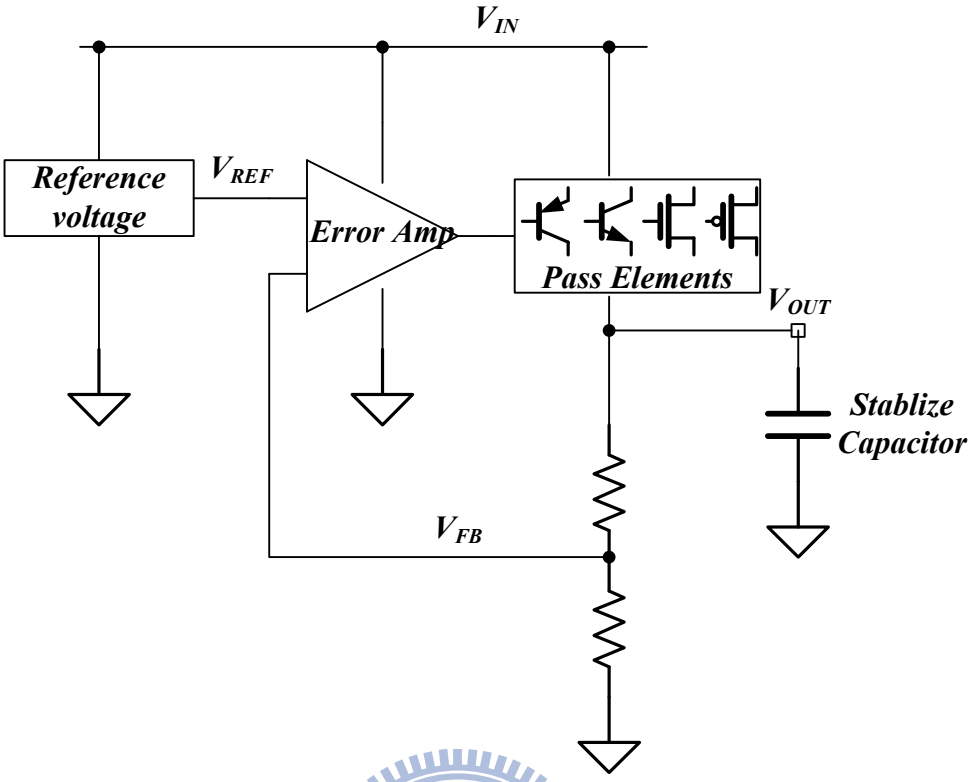


Fig. 15. Linear Regulator.

The advantages of the linear regulator: circuit structure simple, low cost, low footprint area, low output voltage ripple, fast line response time and fast load response time.

The disadvantage of the linear regulator: can only generate output voltage lower than input voltage, lower efficiency when the voltage drop between the input voltage and the output voltage increase and thermal dissipation large.

The reference voltage circuit is used to generate a reference voltage that is independent of process, voltage and temperature.

The error amp is an error operation amplifier that amplifies the error voltage between the reference voltage V_{REF} and the feedback voltage V_{FB} for controlling the pass elements. For the system stability consideration, an error amp usually applies some ac compensation method. Normally if an error amp with large dc gain, the accuracy of output voltage will be better.

There are many types of pass elements, such as BJT (NPN or PNP) or MOSFET (NMOS

or PMOS). The choices of pass elements are often depend on the application, specification and cost. Pass elements maybe external discrete components or built-in SOC devices.

The feedback element is often composed of a resistor network, sometimes may need extra capacitors for ac compensation. The main job of a feedback element is to generate feedback voltage for error amp.

1.3.2 Switching Capacitor Converter

Fig. 16 is a typical voltage doubler of switching capacitor converter [5] [6]. A switching capacitor converter can generate an output voltage larger (boost) or smaller (buck) than the input voltage, and even more, a negative voltage.

In many applications, the boosted voltage or the bucked voltage or even the buck-boost voltage are needed in the system, but when the footprint area or the cost are issue, switching capacitor converter is a practical solution. Handheld or mobile application often chooses this method as a solution, this work (TFT-LCD Driver) is a good example.

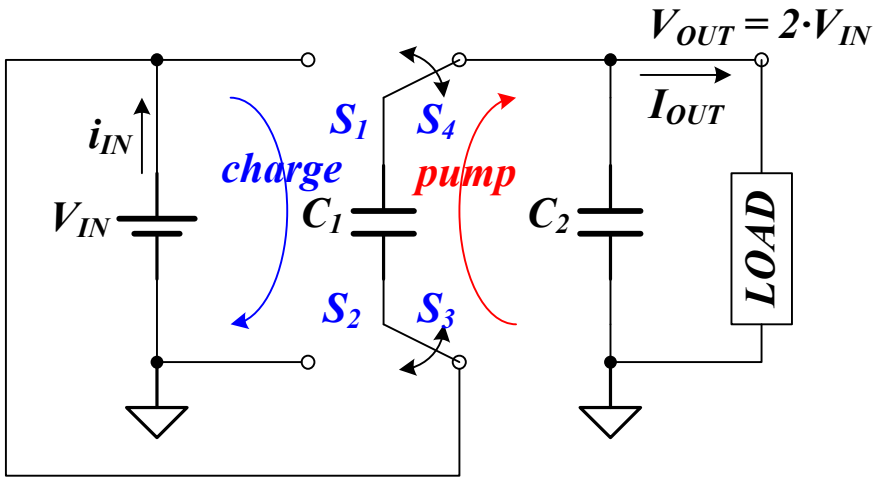


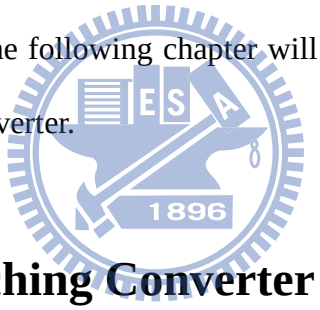
Fig. 16. Switching Capacitor Converter: Voltage Doubler.

The advantages of switching capacitor converter: efficiency higher, low EMI and

medium cost.

The disadvantages of switching capacitor converter: output driving capability small, output ripple high, layout area large.

Generally speaking, the switching capacitor converters, also named the charge pumps, are composed of the power switches and the capacitors. As shown in Fig. 16, there are two phase timing for the voltage doubler operation. During the charge phase, switch S_1 and S_2 are closed, but S_3 and S_4 are opened. Top plate of the capacitor C_1 is charged to V_{IN} by S_1 and bottom plate of it is charged to GND by S_2. During the pump phase, switch S_1 and S_2 are opened, but S_3 and S_4 are closed. Bottom plate of the capacitor C_1 is charged to V_{IN} by S_3 and because the charge conservation theorem, the top plate of C_1 is now $2 \cdot V_{IN}$, and be connected to V_{OUT} by S_4. After several repeated operations of charge and pump phase, V_{OUT} will generally increases to $2 \cdot V_{IN}$. The following chapter will have more detail descriptions of the switching capacitor voltage converter.



1.3.3 Inductor Switching Converter

This type of voltage converter needs at least one inductor as an electric energy storage component. Compared with the linear regulator and the switching capacitor converter, the inductor switching converter provides highest efficiency. A higher efficiency can minimize thermal dissipation issue, and also increases lifetime of the battery in the handheld or the mobile application. Besides, inductor switching converters also support inverting (negative voltage), buck (lower voltage than input), boost (higher voltage than input), and even buck-boost topology [7].

The Inductor switching converters usually apply the pulse width modulation (PWM) by changing the duty cycle to control the on/off of Power MOSFET. By doing so, we can change the amount of the electric energy stored inside the inductor to control the output voltage. The

R_{DSON} (on resistance) of the Power N-MOSFET lower, the power loss will be smaller, resulting in higher power conversion efficiency. However, when the output current loading becomes smaller, the efficiency of the PWM control method will lower. This is because the switching loss dominates at small output current. Some control mechanisms such as pulse frequency modulation (PFM) [8] or pulse skipping modulation (PSM) [9] will have better efficiency at the smaller output current loading condition by reducing the operation frequency or skipping some on pulses to minimize the switching loss.

The advantages of inductor switching converter: highest conversion efficiency and large output driving capability.

The disadvantages of inductor switching converter: high cost, complex design, large output voltage ripple, large layout area and EMI issue.

Fig. 17 shows the asyncronize boost type of the inductor switching converter [10]. This converter is composed mainly by a driver circuit, a feedback network and an inductor L_1, a Power NMOS T_1 and a diode D_1. In the synchronize boost design, D_1 will be replaced by a Power PMOS.

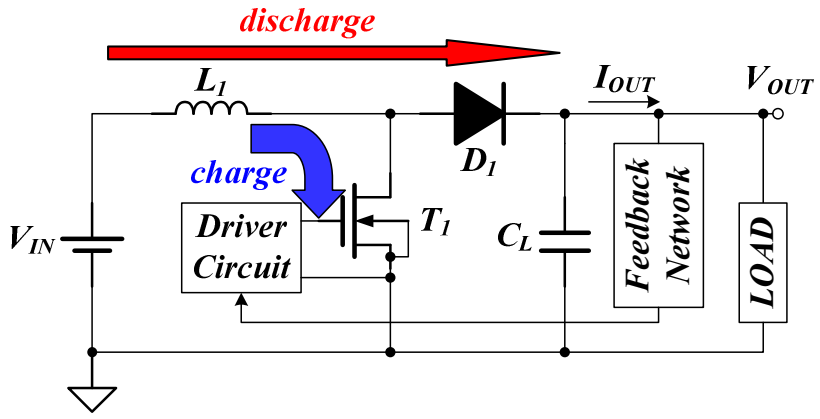


Fig. 17. Inductor Switching Converter: Boost.

The driver circuit contains an error amp, which amplifies the error voltage between the

reference voltage and the feedback voltage and a PWM generation circuit, which turns the amplified error voltage into a PWM signal, then modulates the duty cycle of the Power NMOS T1. The feedback network is responsible for monitor the output voltage and returns a feedback voltage, and even in a current mode operation, it will returns an output current loading information to the control driver circuit.

The operation theory of a boost inductor switching converter is as below:

First, the Power NMOS T_1 turns on, the drain of T_1 equals almost to ground, D_1 is reverse biased and turns off, then the input voltage V_{IN} stores energy into the inductor L_1 and the inductor current ramps up and the capacitor C_L supplies current to output load. Assuming the R_{DSON} of the Power NMOS is very small to be ignored,

Increased inductor current $\Delta I_L(+) = \frac{V_{IN} - 0}{L} T_{ON}$ (3)

Second, the Power NMOS T_1 turns off, the drain of T_1 equals to V_{IN}, D_1 is forward biased and turns on, then the energy stored in the inductor L_1 begins to discharge through D_1 toward V_{OUT}, and the inductor current ramps down. Assuming the forward voltage of D_1 is small enough to be ignored,

Decreased inductor current $\Delta I_L(-) = \frac{V_{OUT} - V_{IN}}{L} T_{OFF}$ (4)

Since the inductor current can not be changed abruptly, Eq. 3, must equals to Eq. 4.

$$V_{OUT} = V_{IN}(1 + \frac{T_{ON}}{T_{OFF}}) = V_{IN} \frac{T_{ON} + T_{OFF}}{T_{OFF}} \quad (5)$$

$$T_S = T_{ON} + T_{OFF}, \quad D = \frac{T_{ON}}{T_S}, \quad (1 - D) = \frac{T_{OFF}}{T_S} \quad (6)$$

After replacing Eq. 6 into Eq. 5, we can derive the relation of V_{OUT} and V_{IN},

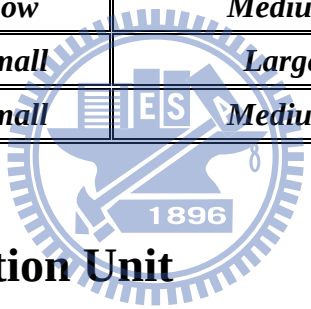
$$V_{OUT} = \frac{V_{IN}}{1 - D} \quad (7)$$

From Eq. 7, $0 < D < 1$, so the output voltage V_{OUT} must be larger than the input voltage V_{IN}. This is why we call the boost type inductor switching converter because it can generate a larger output voltage V_{OUT} than the input voltage V_{IN}.

Table II shows the comparison of the linear regulator, the switching capacitor converter, and the inductor switching converter.

TABLE II. COMPARISONS OF DC/DC VOLTAGE CONVERTERS

Characteristics	*Linear Regulator*	*Switching Capacitor Converter*	*Inductor Switching Converter*
Conversion Type	***Buck***	***Buck, Boost, Buck-Boost, Inverting***	***Buck, Boost, Buck-Boost, Inverting***
Efficiency	***Low***	***Medium***	***High***
Output Voltage Ripple	***Low***	***High***	***High***
Output Driving Capability	***Medium***	***Low***	***High***
Cost	***Low***	***Medium***	***High***
Layout Area	***Small***	***Large***	***Large***
Footprint Area	***Small***	***Medium***	***Large***



1.3.4 Power Generation Unit

After comprehending sections 1.3.1 to 1.3.3, let's move into the power generation unit of the TFT-LCD driver. As shown in Fig. 14, the power supply system of a cell phone provides two power sources to the TFT-LCD driver. That is, the power source, VCI, is the main analogy system power and the other power source, IOVCC, is the I/O (input/output pad) interface power as depicted in Fig. 18, the power generation unit of the TFT-LCD driver.

VCORE voltage ranges from 1.6V to 1.9V, generated by LDO and is responsible for the TCON and the SRAM power. This voltage is always determined by the low voltage device of the silicon process.

DDVDH voltage ranges from 4.7V to 6.0V, generated by charge pump and is responsible for the power of the source driver and the VCOM driver. This voltage is always determined by the characteristics of the liquid crystals for the different panel makers.

VCL voltage ranges from -2.4V to -3V, generated by charge pump and is responsible for the VCOM driver's power. This voltage is also determined by the characteristics of the liquid crystals for the different panel makers.

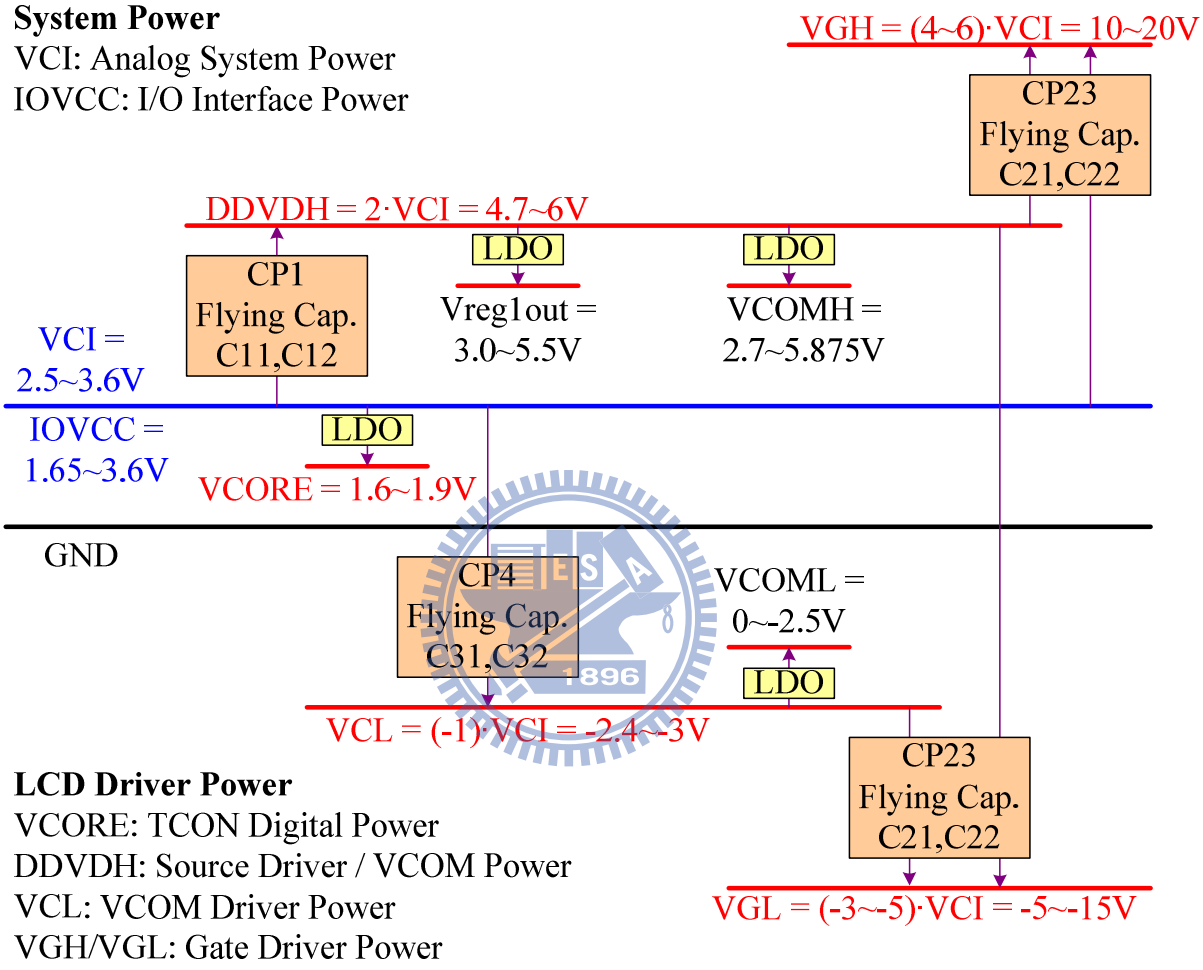


Fig. 18. Power Generation Unit of TFT-LCD Driver.

VGH voltage ranges from 10V to 20V, generated by charge pump and is responsible for the gate driver's power. This voltage is always determined by the characteristics of the TFTs for the different panel makers.

VGL voltage ranges from -5V to -15V, generated by charge pump and is also responsible for the gate driver's power. This voltage is also determined by the characteristics of the TFTs

for the different panel makers.

Vreg1out voltage ranges from 3.0V to 5.5V, generated by LDO and is responsible for the reference power of the gamma voltage generator. This voltage is always determined by the characteristics of the liquid crystals for the different panel makers.

VCOMH voltage ranges from 2.7V to 5.875V, generated by LDO and is responsible for the VCOM driver's power. This voltage is always determined by the characteristics of the liquid crystals for the different panel makers.

VCOML voltage ranges from 0V to -2.5V, generated by LDO and is responsible for the VCOM driver's power. This voltage is also determined by the characteristics of the liquid crystals for the different panel makers.

From Fig. 18 and Fig. 19, the DDVDH voltage is generated by charge pump (CP_1) with two flying capacitors (C_{11}, C_{12}).

The charge pump (CP_1) with two flying capacitors is a so-called dual side charge pump. A dual side charge pump can reduce the voltage ripple by the dual side operation [11].

VCL is generated by charge pump (CP_4) with two flying capacitors (C_{31}, C_{32}). This is also a dual side charge pump.

VGH and VGL are generated by charge pump (CP_{23}) with two flying capacitors (C_{21}, C_{22}). This charge pump is not a dual side charge pump because the two flying capacitors are needed to generate higher level voltage of VGH and VGL as shown in Fig. 19.

This work proposes a new voltage converter using only two flying capacitors to generate DDVDH and VCL power sources, saving the footprint area by reducing the number of the external flying capacitors, and at the same time, saving the layout area by reducing the IC pin outs and the number of the power switches. Later chapter will have more detail contents for it.

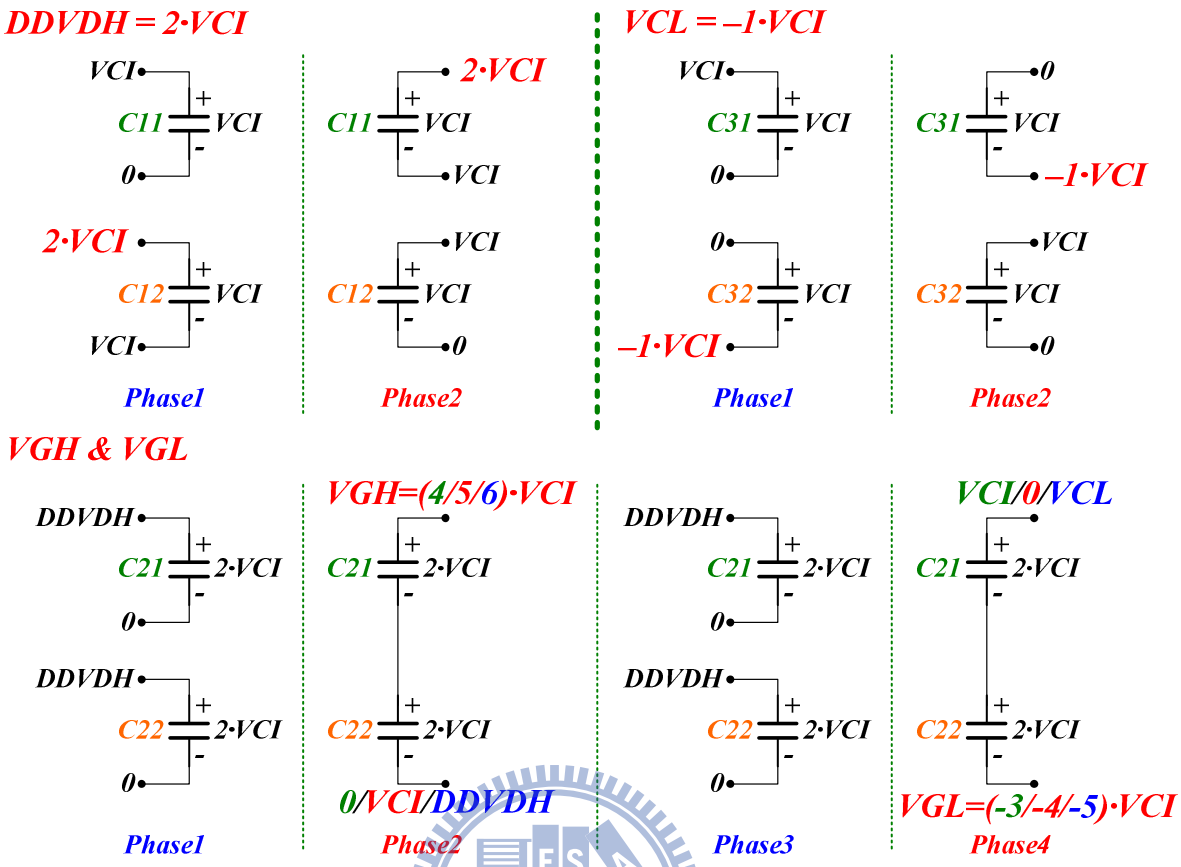


Fig. 19. Simple Operation Principle of CP_1, CP_4 and CP_{23} in TFT-LCD Driver.

1.4 Power Specification

The power management unit is a very important function block in every different application integrated circuits. Fig. 18 showed the TFT-LCD driver's power generation unit that is composed of various types of linear regulators and switching capacitor converters. Let us review the power budgets of every function blocks of this work. For a QVGA 240RGB*320 resolution, frame rate 60Hz, the inversion types chooses line inversion as the worst case:

Source driver power consumption: Based on the regular source panel loading ranges from 10pF to 20pF, the source driver output voltage changes from 0.5V to 4.5V.

$$I_{DDVDH\_SRC} = (240 \cdot 3 \cdot 320) \cdot 60 \cdot 20p \cdot (4.5 - 0.5) = 1.106mA \quad (8)$$

VCOM driver power consumption: Based on the regular VCOM panel loading ranges from 5nF to 15nF, the VCOM driver output voltage changes from 4V to -1V.

$$I_{DDVDH\_VCOM} = (\frac{1}{2} \cdot 320) \cdot 60 \cdot 15n \cdot [4-(-1)] = 0.72mA$$
$$I_{VCL\_VCOM} = (\frac{1}{2} \cdot 320) \cdot 60 \cdot 15n \cdot [4-(-1)] = 0.72mA \quad (9)$$

Gate driver power consumption: Based on the regular gate panel loading ranges from 20pF to 40pF, the gate driver output voltage changes from 15V to -10V.

$$I_{VGH\_GATE} = 320 \cdot 60 \cdot 40p \cdot [15-(-10)] = 19.2uA$$
$$I_{VGL\_GATE} = 320 \cdot 60 \cdot 40p \cdot [15-(-10)] = 19.2uA \quad (10)$$

TCON and SRAM power consumption: This item varies with process and various digital functions and typically 1mA to 2mA current budget comes from the VCORE linear regulator.

Vreg1out power consumption: Vreg1out is the reference power of the gamma resistors, normally consumes current less than 50uA, this current comes from DDVDH.

VCOMH power consumption: As Eq. 9 showed, the average current consumption of VCOMH is 0.72mA and this current comes from DDVDH.

VCOML power consumption: As Eq. 9 showed, the average current consumption of VCOML is 0.72mA and this current comes from VCL.

Let's summarize the current budgets as follow:

DDVDH is generated by CP_1 and the current budget is:

$$I_{DDVDH\_total} = 1.106m + 0.72m + 0.05m = 1.876mA \quad (11)$$

VCL is generated by CP_4 and the current budget is:

$$I_{VCL\_total} = 0.72mA \quad (12)$$

VGH and VGL is generated by CP_{23} and the current budget is:

$$I_{VGH\_total} = 19.2uA \quad (13)$$

$I_{VGL\_total} = 19.2uA$

In Fig. 20, the conventional dual side CP_1 use two flying capacitors to generate DDVDH, and the conventional dual side CP_4 use two flying capacitors to generate VCL, too. This work proposes a new dual side dual output CP_{14} as Fig. 20 shows that uses only two flying capacitors to generate DDVDH and VCL.

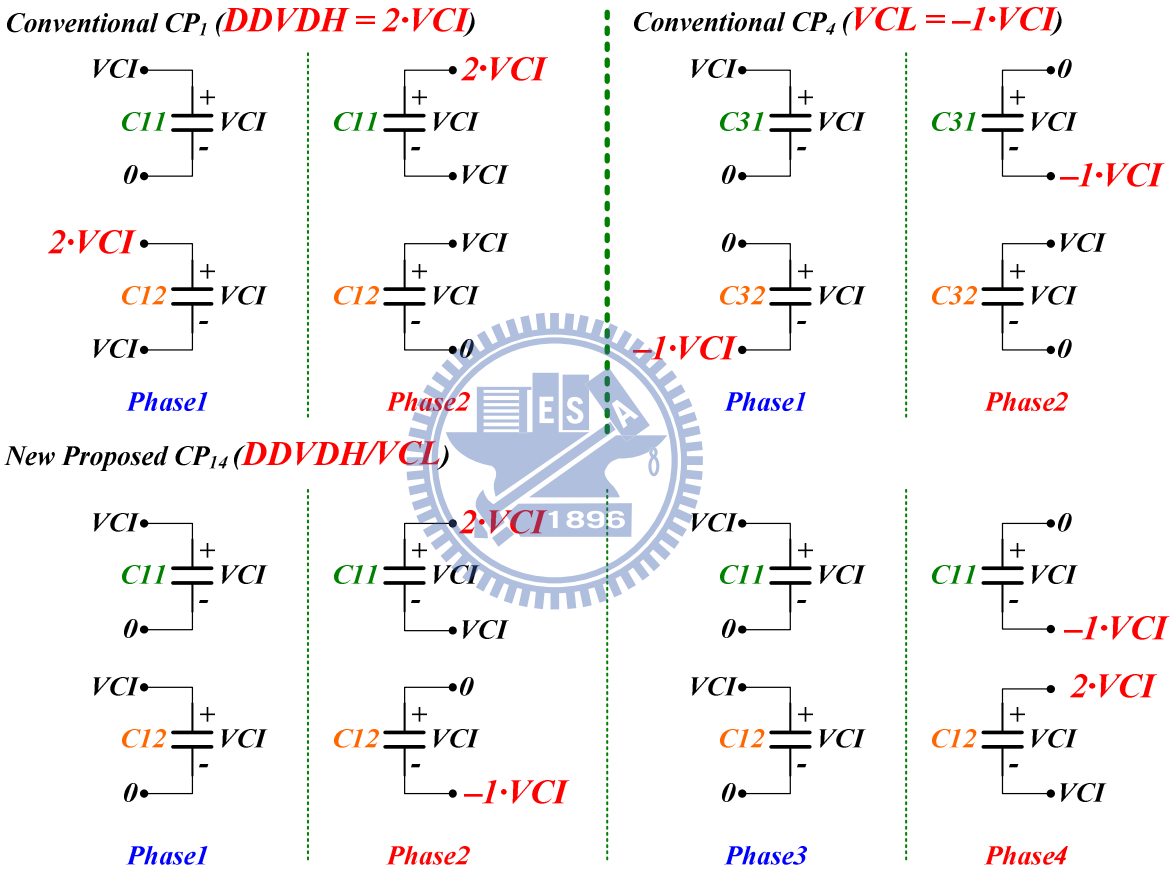


Fig. 20. New Proposed Dual Side Dual Output Charge Pump

The new proposed method saves two flying capacitors, 4 pin outs and 4 power switches for generating DDVDH and VCL. The IC layout area of the new proposed method saves more than 27% than the traditional method without sacrificing the display quality.

Table III shows several system voltage specifications of the TFT-LCD driver. As

introduced in section 1.2, the source driver, the Vreg1out regulator, the VCOMH and the VCOML generator use op-based structure to achieve high line regulation performance.

The source drivers are responsible for driving 64 gamma gray levels into the TFT-LCD panel. The voltage steps between each gamma gray levels are not equal because of the gamma correlation of the human eyes. The minimum gamma voltage step is around 15mV and that means if the voltage difference is smaller than 15mV, the human eyes may not be able to recognize the difference of the gamma level. The line regulation of source driver is 0.74mV/V in DDVDH power domain and that means if DDVDH voltage changes abruptly 20.27V, the source driver output voltage will change 15mV. We can figure out if DDVDH voltage changes abruptly 33.33V, the output voltage of Vreg1out regulator will change one step 50mV. Also if DDVDH voltage changes abruptly 7.35V, the output voltage of VCOMH will change one step 25mV. We can come out a summary for DDVDH voltage that the voltage ripple of DDVDH should be smaller than 7.35V to meet the specifications of the source driver, the Vreg1out regulator and the VCOMH voltage generator.

We can also figure out that if VCL voltage changes abruptly 3.65V, the output voltage of VCOML will change one step 25mV. So VCL voltage ripple should be smaller than 3.65V to meet the specification of the VCOML voltage generator.

All of these voltage specifications are listed in TABLE III. From Table III, we can get the maximum output impedance specifications for DDVDH and VCL,

$$R_{OUT\_DDVDH\_MAX} = (2 \cdot VCI_{MIN} - DDVDH_{MIN}) / I_{DDVDH\_MAX} = (2 \cdot 2.5 - 4.7) / 2mA = 150\Omega$$

$$R_{OUT\_VCL\_MAX} = [VCL_{MAX} - (-1) \cdot VCI_{MIN}] / I_{VCL\_MAX} = [-2.4 - (-1) \cdot 2.5] / 0.8mA = 125\Omega$$

The smaller the output impedance, the larger driving ability the voltage converter has.

TABLE III. TFT-LCD DRIVER SYSTEM VOLTAGE SPECIFICATIONS.

Line Regulation		*Voltage Spec*	
Source driver	***0.74 mV/V (DDVDH)***	*Gamma step*	***Min 15mV***
Vreg1out	***1.5mV/V (DDVDH)***	*Vreg1out*	***3.0V~6.0V, step 50mV***
VCOMH	***3.4mV/V (DDVDH)***	*VCOMH*	***2.7V~5.875V, step 25mV***
VCOML	***6.85mV/V (VCL)***	*VCOML*	***-2.5V~0V, step 25mV***
Power Spec			
VCI	***2.5V~3.6V***		
DDVDH	***4.7V~6.0V, ripple < 1V, max current 2mA***		$R_{OUT\_DDVDH\_MAX}$***=150 Ω***
VCL	***-2.4V~-3V, ripple < 1V, max current 0.8mA***		$R_{OUT\_VCL\_MAX}$***=125 Ω***
VGH	***10V~20V, max current 25uA***		
VGL	***-5V~-15V, max current 25uA***		

Chapter 2
Performance Checking of Switching Capacitor Voltage Converter

With the progress of semiconductor process from submicron meter to deep submicron meter such as 0.35um, 0.25um, 0.18um, 0.13um and even 45nm, the devices are made smaller generation by generation, and the power supply voltage levels for the smaller devices also drop generation by generation for solving power dissipation issues. But some special application ICs such as the electrically erasable programmable read-only memory (EEPROM), the flash memories, the dynamic random access memory (DRAM) and the TFT-LCD drivers need high voltages for normal function operation. Charge pumps have been used to generate voltages higher than the system power supply voltage for these applications. Charge pumps characterized with low EMI (electro magnetic interference), inductor-less, high efficiency larger than 90%, low cost, low profile and compact are often the best choice of the handheld TFT-LCD drivers. The charge pumps have many different topologies [15] [16] [17]. In this chapter, we will introduce the voltage doubler and the voltage inverter. Gaining more insight into the theory of the charge pump is the goal of this chapter. Section 2.1 introduces some basic concepts about the switching capacitor [18], section 2.2 shows the voltage doubler converter and at last, section 2.3 explains the theories of the voltage inverter converter.

2.1 Basic Concepts about Switching Capacitor

2.1.1 Charge Transfer of Capacitors

Capacitors are energy storage materials. The energy is stored in the capacitor in the form of electric charge. From the formula of below, if a capacitor with capacitance C_1 is charged to

a voltage V_{IN}, then the charge Q_1 stored in the capacitor is given by

$$Q_1 = C_1 \cdot V_{IN} = I_{IN} \cdot t \tag{14}$$

In Fig. 21, for the ideal case, the charge Q_1 is stored in the capacitor instantaneously, and that means t approaches zero. From Eq. 14, if t approaches zero, the charging current I_{IN} approaches infinity.

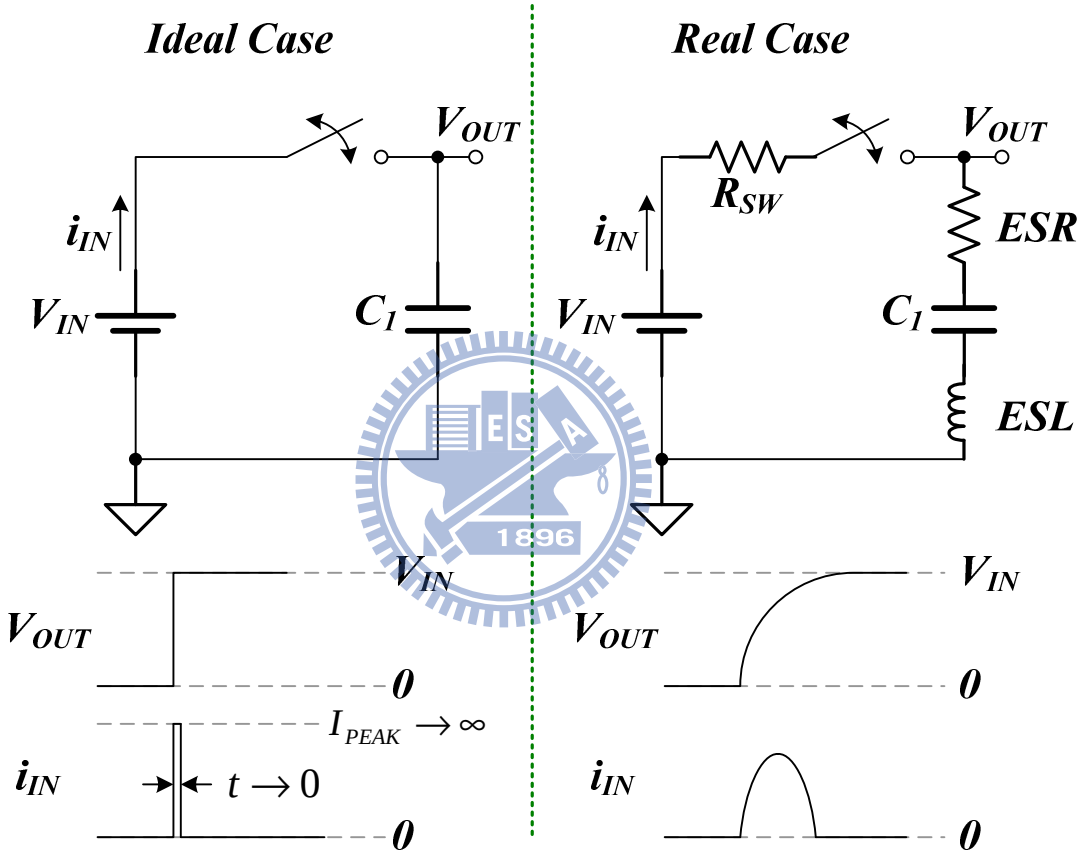


Fig. 21.Waveforms of Charging a Capacitor.

But in real case, the capacitors have the equivalent series resistance (ESR) and the equivalent series inductance (ESL); meanwhile, the power switch has an intrinsic resistance R_{SW}. These resistances and inductance will not only result in energy loss when storing energy in the capacitor but also increase the time of storing the energy in the capacitor. In other words, the charging current I_{IN} will be suppress to a limited value instead of infinity.

From the law of charge conservation, if two capacitors C_1 and C_2 with voltage V_1 and V_2 are connected together, the charge Q_1 of C_1 and Q_2 of C_2 will re-distribute between these two capacitors, but the total charge Q_T will be,

$$Q_T = Q_1 + Q_2 = C_1V_1 + C_2V_2 = (C_1 + C_2)V_{EQ} \tag{15}$$

Then the equivalent voltage of the parallel capacitors will be,

$$V_{EQ} = \frac{Q_T}{C_1 + C_2} = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} = \frac{C_1}{C_1 + C_2}V_1 + \frac{C_2}{C_1 + C_2}V_2 \tag{16}$$

2.1.2 Switching Capacitor Principle

Fig. 22 shows a simple switching capacitor voltage converter circuit.

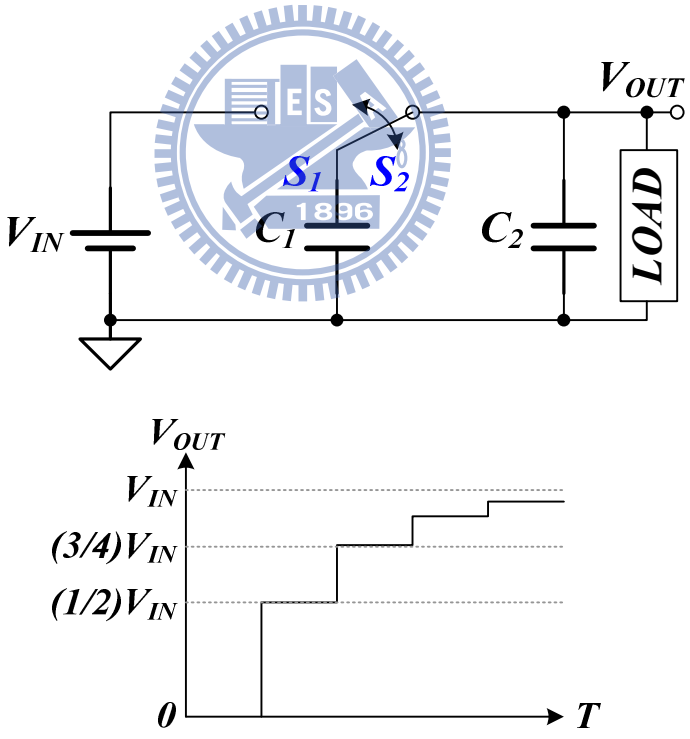


Fig. 22.Waveforms of Switching Capacitor Operation.

The simple switching capacitor circuit composing of two switches S_1, S_2 and two capacitors C_1, C_2. When S_1 is closed and S_2 is opened, then V_{IN} is connected to C_1 which will

be charged to V_{IN}. When S_1 is opened and S_2 is closed, then C_1 is connected to C_2, and the charge of C_1 and C_2 will re-distribute between each other. Assuming the initial charge of C_2 is zero and the capacitance of C_1 and C_2 are equal. In phase1, C_1 is charged to V_{IN}, and in phase2, the charge of C_1 and C_2 re-distribute,

$$V_{OUT} = \frac{C_1}{C_1 + C_2} V_{IN} + \frac{C_2}{C_1 + C_2} 0 = \frac{1}{2} V_{IN} \tag{17}$$

After the first cycle, $\boldsymbol{V_{OUT} = (1/2)\cdot V_{IN}}$, then $\boldsymbol{V_{OUT} = (1/2)\cdot V_{IN} + (1/4)\cdot V_{IN} = (3/4)\cdot V_{IN}}$ after the second cycle. It's not hard to understand that after infinite cycles, V_{OUT} will approach V_{IN} very closely.

In the steady state, assuming the switching frequency in Fig. 22 is f. The charge being transferred of each cycle is $\boldsymbol{C_1\cdot(V_{IN}-V_{OUT})}$ and results in an average current,

$$I_{avg} = fC_1(V_{IN} - V_{OUT}) = \frac{V_{IN} - V_{OUT}}{1/fC_1} = \frac{V_{IN} - V_{OUT}}{R_{EQ}} \tag{18}$$

$$R_{EQ} = \frac{1}{fC_1} \tag{19}$$

From Eq. 18 and 19, the switching operation results in an additional equivalent resistance R_{EQ} connecting V_{IN} and V_{OUT}. This equivalent resistance leads to an extra power loss beyond the switch resistances and ESR resistance of capacitors.

2.2 Voltage Doubler

The voltage doubler plays a role of generating the DDVDH voltage of 2 times the system power VCI. As Fig. 1 shown, DDVDH is the power supply for the source drivers, the gamma voltage generator and the VCOM driver in the TFT-LCD driver. This voltage is always determined by the characteristics of the liquid crystals for the different panel makers.

2.2.1 Operation of Voltage Doubler

Reminds we had introduced the operation principle of voltage doubler in section 1.3.2, Fig. 16 shown the circuit of the voltage doubler. The capacitor C_1 is the pump capacitor, also named the flying capacitor, and the capacitor C_2 is the load capacitor, also named the stabilize capacitor.

One complete operation cycle of the switching capacitor converter contains charge phase (phase1) and pump phase (phase2). As we discussed before, there are many energy loss such as the switch resistances, ESR and ESL, and with these resistances the charge or discharge of capacitors need some time.

Assuming the charge pump is at the steady state. During the charge phase (phase1), switches S_1 and S_2 are closed, S_3 and S_4 are opened. At this time, C_1 is charged to V_{IN}, the top and bottom plate of C_1 is connected to V_{IN} and ground individually in order to store energy. During the pump phase (phase2), switches S_1 and S_2 are opened, S_3 and S_4 are closed. At this time, C_1 transfers energy to C_2, the top and bottom plate of C_1 is connected to V_{OUT} and V_{IN} individually. The voltage drop of C_1 equals to V_{IN} because the voltage drop of a capacitor can not change instantaneously. So when S_3 is closed, the voltage of C_1's bottom plate equals to V_{IN} and the voltage of C_1's top plate connected to V_{OUT} by S_4 equals to $2V_{IN}$.

2.2.2 Voltage Ripple of Voltage Doubler

Fig. 23 shows the steady state waveforms of the voltage doubler. Assuming the output load current is I_{OUT}. The average value of input current i_{IN} is equal to $2I_{OUT}$.

A charging current around $2I_{OUT}$ flows when the flying capacitor C_1 is connected to the input V_{IN}. The initial value of this charging current depends on the initial voltage across C_1, the ESR_{C1} which is the ESR resistance of C_1, and the resistances of the power switches.

The current i_{OUT} increases abruptly from zero to $2I_{OUT}$ when the flying capacitor C_1 is

connected to the output V_{OUT}. Half of this current supports the output current and half of it begins to charge the stabilize capacitor C_2.

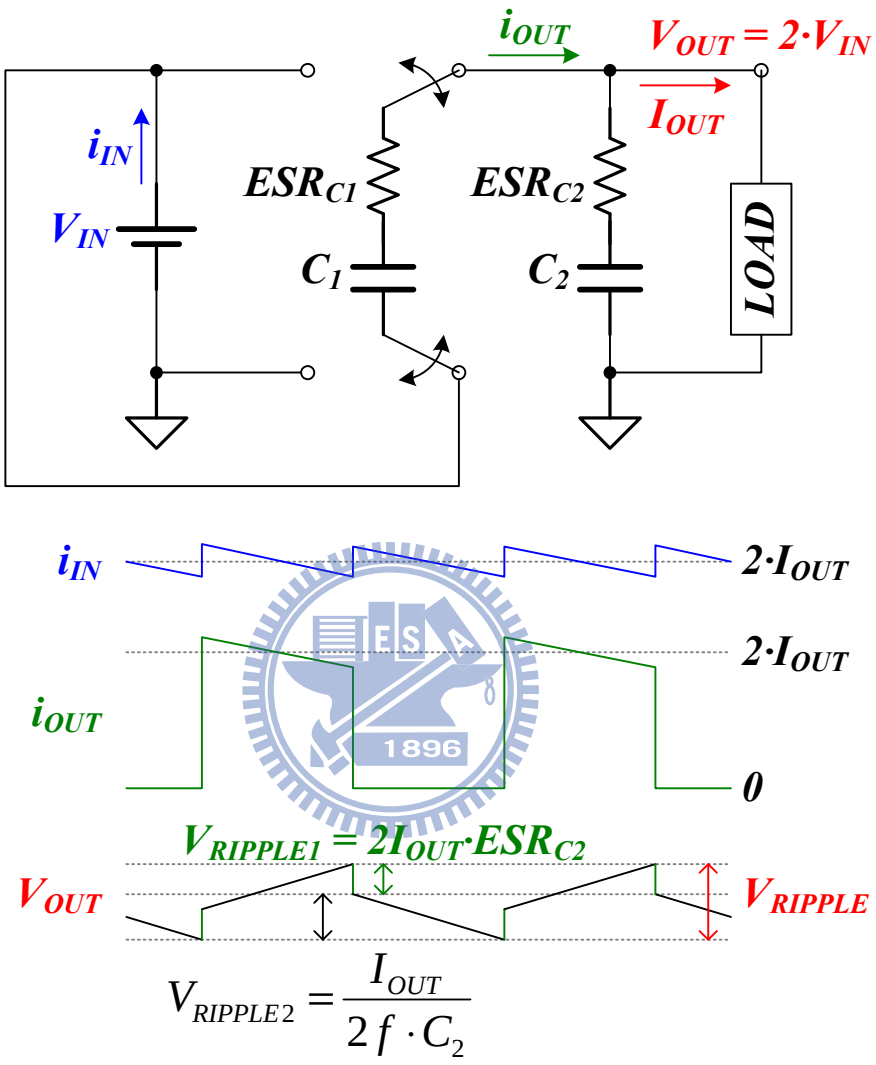


Fig. 23. Voltage Ripple of Voltage Doubler.

When the flying capacitor C_1 is disconnected from the output V_{OUT} and connected to input V_{IN}, the current i_{OUT} decreases abruptly from $2I_{OUT}$ to zero. The current of C_2 change from I_{OUT} (charging C_2) to $-I_{OUT}$ (discharging C_2), and then:

$$V_{RIPPLE1} = I \cdot R = [I_{OUT} - (-I_{OUT})] \cdot ESR_{C2} = 2I_{OUT} \cdot ESR_{C2} \quad (20)$$

And this $-I_{OUT}$ (discharging C_2) current results in,

$$V_{RIPPLE2} = \frac{I \cdot t}{C} = \frac{I_{OUT} \frac{T}{2}}{C_2} = \frac{I_{OUT}}{2f \cdot C_2} \quad (21)$$

From Eq. 20 and 21, the voltage ripple of V_{OUT} is:

$$V_{RIPPLE} = V_{RIPPLE1} + V_{RIPPLE2} = 2I_{OUT} \cdot ESR_{C2} + \frac{I_{OUT}}{2f \cdot C_2} \quad (22)$$

From Eq. 22, we can minimize V_{RIPPLE} by two means. The first method is the design method. By using dual side operation, we can minimize the factor $2I_{OUT}$ of $V_{RIPPLE1}$ to I_{OUT}. And we can also increase operation frequency f to reduce $V_{RIPPLE2}$. The second method is the external component selection. By selecting the C_2 capacitor with smaller ESR can minimize $V_{RIPPLE1}$. And we can also choose larger C_2 capacitor to minimize $V_{RIPPLE2}$. These two methods have some tradeoffs between minimizing V_{RIPPLE} and the costs.

2.2.3 Power Loss of Voltage Doubler

The power loss of the switching capacitor voltage doubler can be divided into 3 types, the static power loss, the switching power loss and the conduction power loss.

As Fig. 24 shows, I_q is the quiescent operation current of the voltage doubler. The static power loss is:

$$P_{STATIC} = I_q \cdot V_{IN} \quad (23)$$

From section 2.1.2 and Eq. 19, we had learned that the switching operation of the switching capacitor voltage converter results in an additional switching power loss with an equivalent resistance $\boldsymbol{1/f \cdot C_1}$.

$$P_{SWITCHING} = I_{OUT}{}^2 \cdot R = I_{OUT}{}^2 \frac{1}{f \cdot C_1} \quad (24)$$

If the operation frequency f is faster or the capacitance of the flying capacitor C1 is larger, the switching power loss can reduced.

Let's review the conduction loss of the voltage doubler. During the charging phase, a

current of $2I_{OUT}$ flows through the resistance of two of the power switches and ESR_{C1} of C_1, when C_1 is connected to the input V_{IN} and ground. During the pumping phase, a current of $2I_{OUT}$ flows through the resistance of the other two of the power switches and ESR_{C1} of C_1 with opposite direction, when C_1 is connected to the output V_{OUT}.

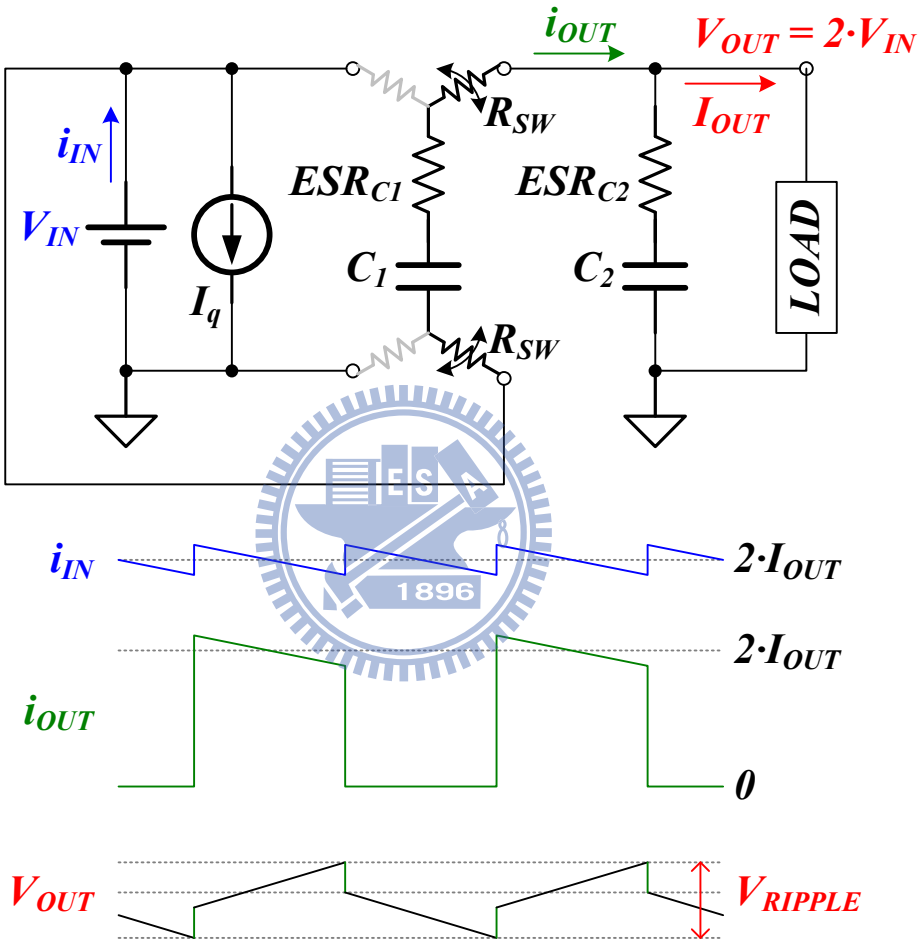


Fig. 24. Steady State Waveforms of Voltage Doubler.

There always exists an rms current of $2I_{OUT}$ flowing through the resistances of $2R_{SW}$ and ESR_{C1}.

$$P_{CONDUCT1} = (2I_{OUT})^2 \cdot (2R_{SW} + ESR_{C1}) = I_{OUT}{}^2 \cdot (8R_{SW} + 4ESR_{C1}) \quad (25)$$

From Eq. 25, assuming ESR_{C1} is smaller enough to be ignored than R_{SW}. We can use two

methods to reduce the conduction power loss $P_{CONDUCT1}$. The first method is to reduce the R_{SW} value by increase the size of the power switches. The second method is to use the dual side operation to minimize the factor $2I_{OUT}$ to I_{OUT}. Both of these two methods reduce the conduction power loss by increasing the layout area, and the second method may have higher cost for requiring an extra external flying capacitor.

During the charging phase, a current of I_{OUT} flows out from the capacitor C_2 through ESR_{C2} when C_1 is connected to the input V_{IN} and ground. During the pumping phase, a current of I_{OUT} flows into the capacitor C_2 through ESR_{C2} when C_1 is connected to the output V_{OUT}. There is always an rms current of I_{OUT} flowing through the resistance ESR_{C2} of the capacitor C_2.

$$P_{CONDUCT2} = I_{OUT}^{\ 2} \cdot ESR_{C2} \tag{26}$$

We can reduce $P_{CONDUCT2}$ by choosing the C_2 capacitor with the smaller ESR.

Therefore, the power loss of the voltage doubler comes out:

$$\begin{aligned} P_{LOSS} &= P_{STATIC} + P_{SWITCHING} + P_{CONDUCT1} + P_{CONDUCT2} \\ &= I_q \cdot V_{IN} + I_{OUT}^{\ 2} \cdot \left(\frac{1}{f \cdot C_1} + 8 \cdot R_{SW} + 4 \cdot ESR_{C1} + ESR_{C2}\right) = I_{OUT}^{\ 2} \cdot R_{OUT} \end{aligned} \tag{27}$$

We can always use R_{OUT} to judge the driving ability of a switching regulator. Assuming I_q is small enough to be ignored,

$$R_{OUT} \approx \frac{1}{f \cdot C_1} + 8R_{SW} + 4ESR_{C1} + ESR_{C2} \tag{28}$$

The smaller R_{OUT} means the larger driving ability and higher efficiency of a switching regulator, and on the contrary, the larger R_{OUT} means the smaller driving ability and lower efficiency of a switching regulator.

2.3 Voltage Inverter

The voltage inverter plays a role of generating the VCL voltage of a negative time the

system power VCI. As Fig. 1 shown, VCL is always the power supply for the VCOM driver in the TFT-LCD Drivers. This voltage is always determined by the characteristics of the liquid crystals for the different panel makers.

2.3.2 Operation of Voltage Inverter

Fig. 25 shows the circuit of the voltage inverter. The capacitor C_1 is the pump capacitor, also named the flying capacitor, and the capacitor C_2 is the load capacitor, also named the stabilize capacitor.

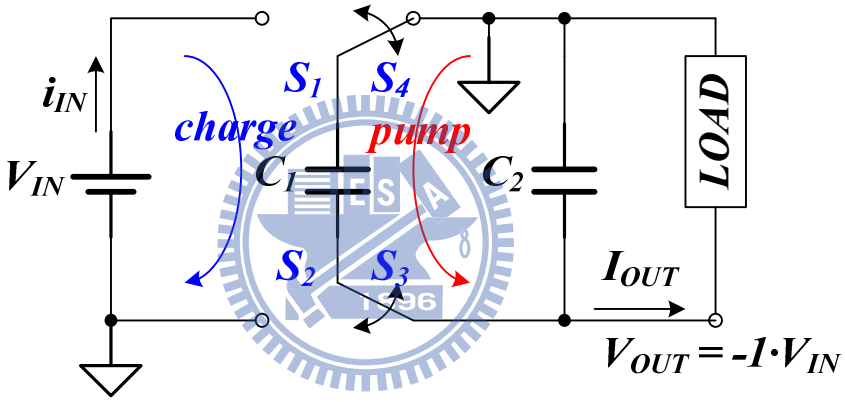


Fig. 25. Switching Capacitor Voltage Converter: Voltage Inverter.

One complete operation cycle of the switching capacitor converter contains the charge phase (phase1) and the pump phase (phase2). As we discussed before, there are many energy loss such as the switch resistances, ESR and ESL, the charge or discharge of capacitors need some time.

Assuming the charge pump is at the steady state. During the charge phase (phase1), switches S_1 and S_2 are closed, S_3 and S_4 are opened. At this time, C_1 is charged to V_{IN} and the top and bottom plate of C_1 is connected to V_{IN} and ground individually. During the pump phase (phase2), switches S_1 and S_2 are opened, S_3 and S_4 are closed. At this time, C_1 transfers

energy to C_2 and the top and bottom plate of C_1 is connected to ground and V_{OUT} individually. The voltage drop of C_1 equals to V_{IN} because the voltage drop of capacitor can not change instantaneously. So when S_4 is closed, the voltage of C_1's top plate equals to zero and the voltage of C_1's bottom plate connected to V_{OUT} by S_3 equals to $-1 \cdot V_{IN}$.

2.3.1 Ripple of Voltage Inverter

Fig. 26 shows the steady state waveforms of voltage inverter. Assuming the output load current is I_{OUT}. The average value of input current i_{IN} is equal to I_{OUT}.

A charging current around $2I_{OUT}$ flows when the flying capacitor C_1 is connected to the input V_{IN}. The initial value of this charging current depends on the initial voltage across C_1, the ESR_{C1} which is the ESR resistance of C_1, and the resistance of the power switches.

The current i_{OUT} increases abruptly from zero to $2I_{OUT}$ when the flying capacitor C_1 is connected to the output V_{OUT}. Half of this current supports the output current and half of it begins to charge the stabilize capacitor C_2, resulting in

$$V_{RIPPLE2} = \frac{I \cdot t}{C} = \frac{I_{OUT} \frac{T}{2}}{C_2} = \frac{I_{OUT}}{2f \cdot C_2} \tag{29}$$

When the flying capacitor C_1 is disconnected from the output V_{OUT} and connected to input V_{IN}, the current i_{OUT} decreases abruptly from $2I_{OUT}$ to zero. The current of C_2 change from I_{OUT} (charging C_2) to $-I_{OUT}$ (discharging C_2), and then:

$$V_{RIPPLE1} = I \cdot R = [I_{OUT} - (-I_{OUT})] \cdot ESR_{C2} = 2I_{OUT} \cdot ESR_{C2} \tag{30}$$

From Eq. 29 and 30, the voltage ripple of V_{OUT} is:

$$V_{RIPPLE} = V_{RIPPLE1} + V_{RIPPLE2} = 2I_{OUT} \cdot ESR_{C2} + \frac{I_{OUT}}{2f \cdot C_2} \tag{31}$$

From Eq. 31, we can minimize V_{RIPPLE} by two means. The first method is the design method. By using dual side operation, we can minimize the factor $2I_{OUT}$ of $V_{RIPPLE1}$ to I_{OUT}. And we can also increase operation frequency f to reduce $V_{RIPPLE2}$. The second method is the

external component selection. By selecting the C_2 capacitor with smaller ESR can minimize $V_{RIPPLE1}$. And we can also choose larger C_2 capacitor to minimize $V_{RIPPLE2}$. These two methods have some tradeoffs between minimizing V_{RIPPLE} and the costs.

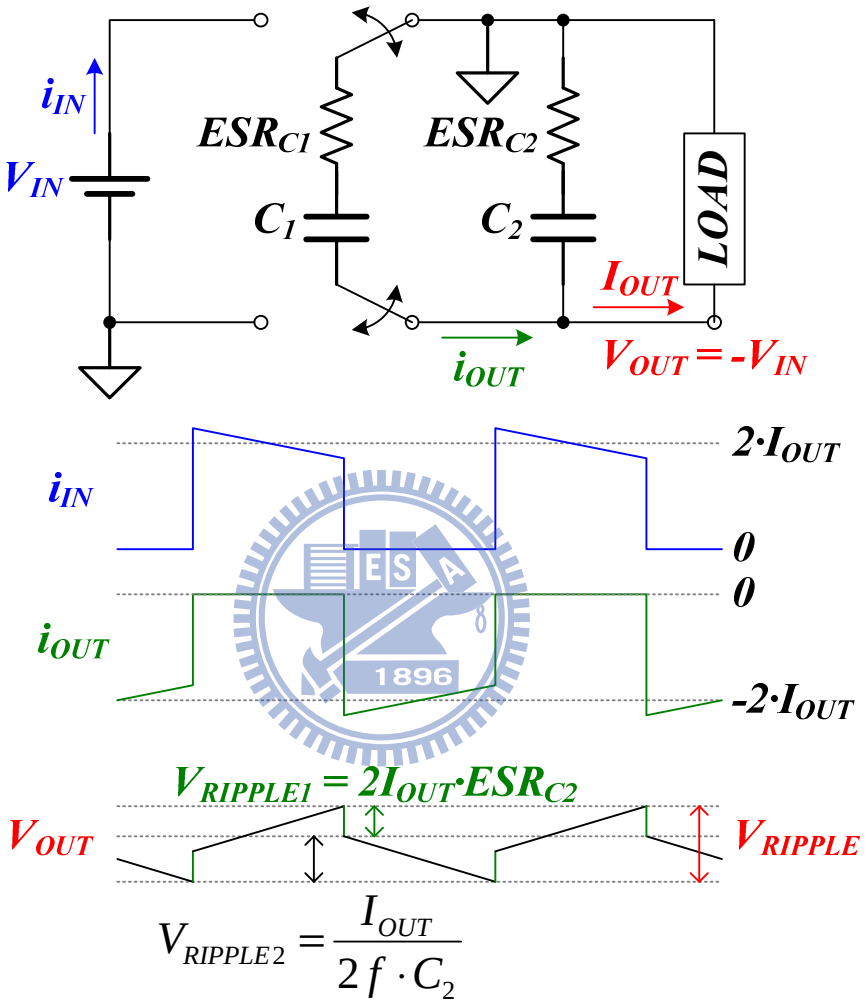


Fig. 26. Voltage Ripple of Voltage Inverter.

2.3.2 Power Loss of Voltage Inverter

The power loss of the switching capacitor voltage inverter can be divided into 3 types, the static power loss, the switching power loss and the conduction power loss.

As Fig. 27 shows, I_q is the quiescent operation current of the voltage inverter. The static

power loss is:

$$P_{STATIC} = I_q \cdot V_{IN} \tag{32}$$

From section 2.1.2 and Eq. 19, we had learned that the switching operation of the switching capacitor voltage converter results in an additional switching power loss with an equivalent resistance ***1/f·C₁***.

$$P_{SWITCHING} = I_{OUT}{}^2 \cdot R = I_{OUT}{}^2 \frac{1}{f \cdot C_1} \tag{33}$$

If the operation frequency f is faster or the capacitance of the flying capacitor C_1 is larger, the switching power loss can reduced.

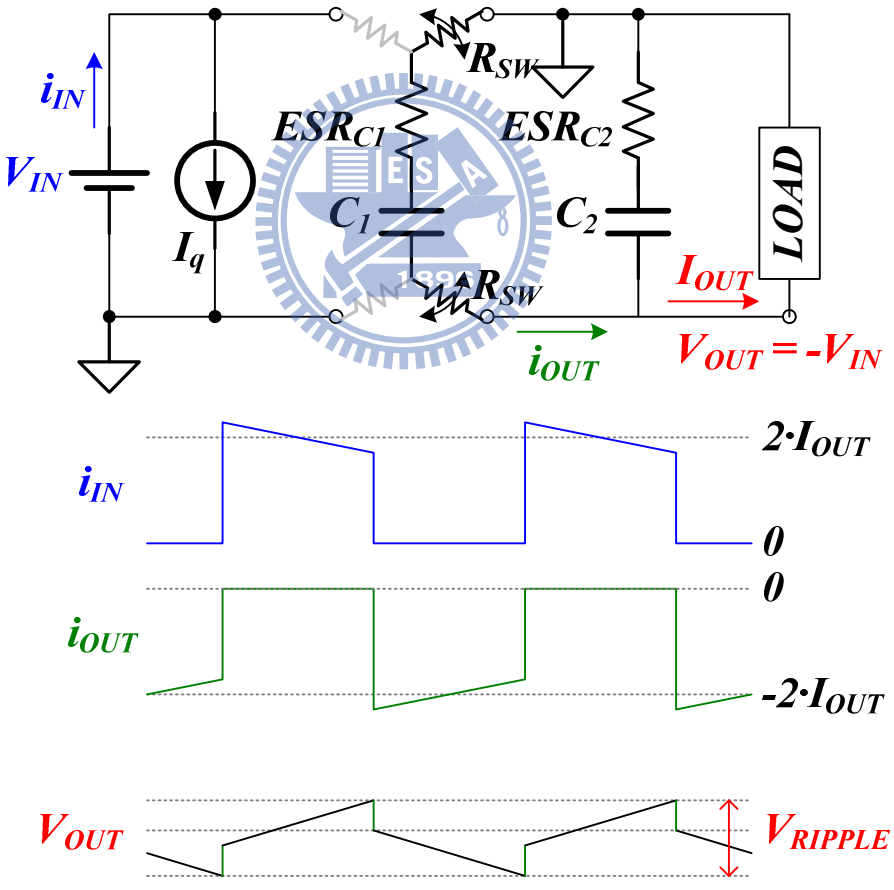


Fig. 27. Power Loss of Voltage Inverter.

Let's review the conduction loss of the voltage inverter. During the charging phase, a

current of $2I_{OUT}$ flows through the resistance of two of the power switches and ESR_{C1} of C_1, when C_1 is connected to the input V_{IN} and ground. During the pumping phase, a current of $2I_{OUT}$ flows through the resistance of the other two of the power switches and ESR_{C1} of C_1 with an opposite direction, when C_1 is connected to the output V_{OUT}. There always exists an rms current of $2I_{OUT}$ flowing through the resistances of $2R_{SW}$ and ESR_{C1}.

$$P_{CONDUCT1} = (2I_{OUT})^2 \cdot (2R_{SW} + ESR_{C1}) = I_{OUT}{}^2 \cdot (8R_{SW} + 4ESR_{C1}) \quad (34)$$

From Eq. 34, assuming ESR_{C1} is smaller enough to be ignored than R_{SW}. We can use two methods to reduce the conduction power loss $P_{CONDUCT1}$. The first method is to reduce the R_{SW} value by increase the size of the power switches. The second method is to use the dual side operation to minimize the factor $2I_{OUT}$ to I_{OUT}. Both of these two methods reduce the conduction power loss by increasing the layout area, and the second method may have higher cost for requiring an extra external flying capacitor.

During the charging phase, a current of I_{OUT} flows out from the capacitor C_2 through ESR_{C2} when C_1 is connected to the input V_{IN} and ground. During the pumping phase, a current of I_{OUT} flows into the capacitor C_2 through ESR_{C2} when C_1 is connected to the output V_{OUT}. There is always an rms current of I_{OUT} flowing through the resistance ESR_{C2} of the capacitor C_2.

$$P_{CONDUCT2} = I_{OUT}{}^2 \cdot ESR_{C2} \quad (35)$$

We can reduce $P_{CONDUCT2}$ by choosing the C_2 capacitor with the smaller ESR.

Therefore, the power loss of the voltage inverter comes out:

$$\begin{aligned} P_{LOSS} &= P_{STATIC} + P_{SWITCHING} + P_{CONDUCT1} + P_{CONDUCT2} \\ &= I_q \cdot V_{IN} + I_{OUT}{}^2 \cdot \left(\frac{1}{f \cdot C_1} + 8 \cdot R_{SW} + 4 \cdot ESR_{C1} + ESR_{C2}\right) = I_{OUT}{}^2 \cdot R_{OUT} \end{aligned} \quad (36)$$

We can always use R_{OUT} to judge the driving ability of a switching regulator. Assuming I_q is small enough to be ignored,

$$R_{OUT} \approx \frac{1}{f \cdot C_1} + 8R_{SW} + 4ESR_{C1} + ESR_{C2} \quad (37)$$

The smaller R_{OUT} means the larger driving ability and higher efficiency of a switching regulator, and on the contrary, the larger R_{OUT} means the smaller driving ability and lower efficiency of a switching regulator.

Chapter 3

Switching Capacitor Voltage Converters in TFT-LCD Driver

In this chapter, the detailed circuit implementations and simulation results of the switching capacitor voltage converters in the TFT-LCD driver will be showed. Section 3.1 will discuss the conventional voltage converters of the voltage doubler and the voltage inverter, including the structure and the real implementation of them. The dual side voltage doubler generates the DDVDH voltage which is the power supply of the source drivers, the gamma gray level generator and the VCOM driver. The dual side voltage inverter generates VCL voltage which is the power supply of the VCOM driver. Section 3.1 uses the conventional methods for generating DDVDH and VCL with 4 flying capacitors and 16 power switches. A new proposed method of the dual side dual output switching capacitor voltage converter that generates DDVDH and VCL with only 2 flying capacitors and 12 power switches will be discussed in section 3.2. Without sacrificing the display quality of the TFT-LCD panel, this new method successfully reduces the IC circuit layout area, external components, external FPC (Flexible Printed Circuit) footprint and costs which is a very important topic in this keen competition industry.

3.1 Conventional Voltage Converters

Circuit Structure and Implementation

Fig. 28 illustrates the conventional charge pump voltage converters. The conventional dual side voltage doubler is composed of three parts. The CLK_PHASE_GEN circuit

generates the phase clocks to control this charge pump. The LSH_P6V transforms the signal voltage level from 3V to 6V domain. The DDVDH POWER SWITCH block contains the power switches needed for this charge pump. This dual side voltage doubler utilizes two flying capacitors C_{11} and C_{12} to generate small ripple DDVDH voltage. The flying capacitors C_{11}, C_{12} and the stabilize capacitor are all external components.

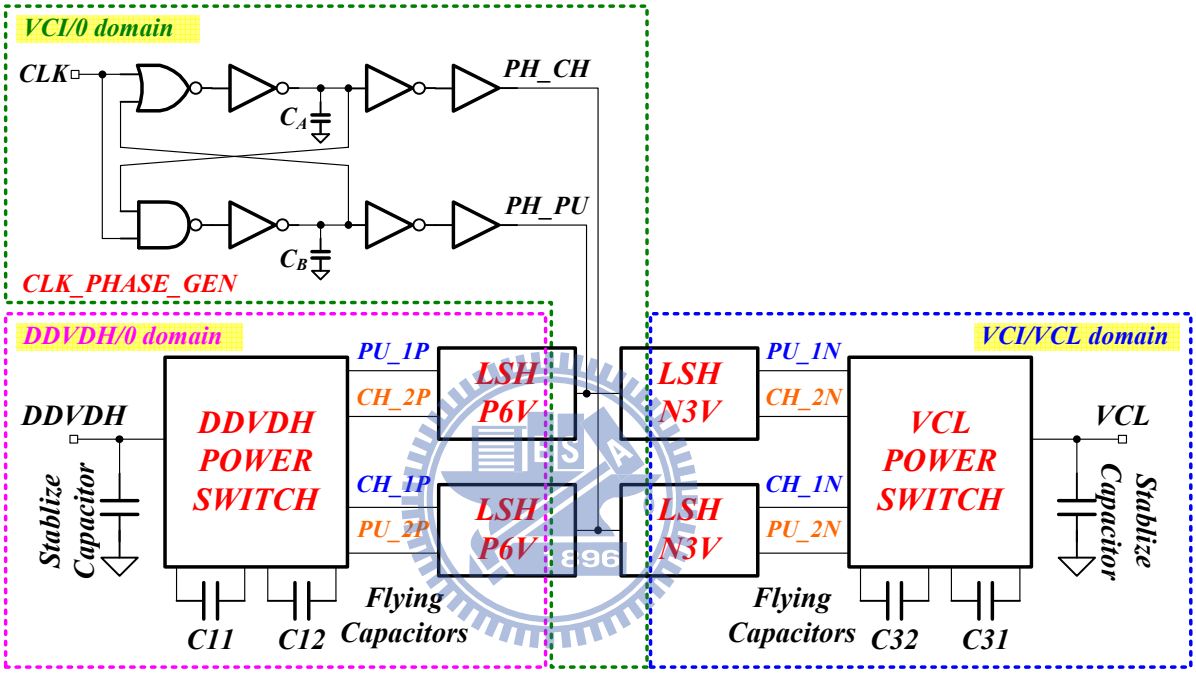


Fig. 28. Conventional Voltage Converters.

The conventional dual side voltage inverter is also composed of three parts. The CLK_PHASE_GEN circuit which is the same as the one of the voltage doubler, generates the phase clocks to control this charge pump. The LSH_N3V transforms the signal voltage level from 3V to 3V/-3V domain. The VCL POWER SWITCH block contains the power switches needed for this charge pump. This dual side voltage inverter utilizes two flying capacitors C_{31} and C_{32} to generate small ripple VCL voltage. The flying capacitors C_{31}, C_{32} and the stabilize capacitor are all external components.

Clock Phase Generation Circuit

The clock phase generation circuit [19] is used to generate the charge phase and pump phase for the dual side voltage doubler. As in Fig. 29, CLK is the clock signal coming from the TCON. PH_CH is the phase control signal for the charge phase and PH_PU is the phase control signal for the pump phase. The internal capacitors C_A and C_B are used to adjust non-overlap timing which can prevent from the possible occurring leakage currents during phase change.

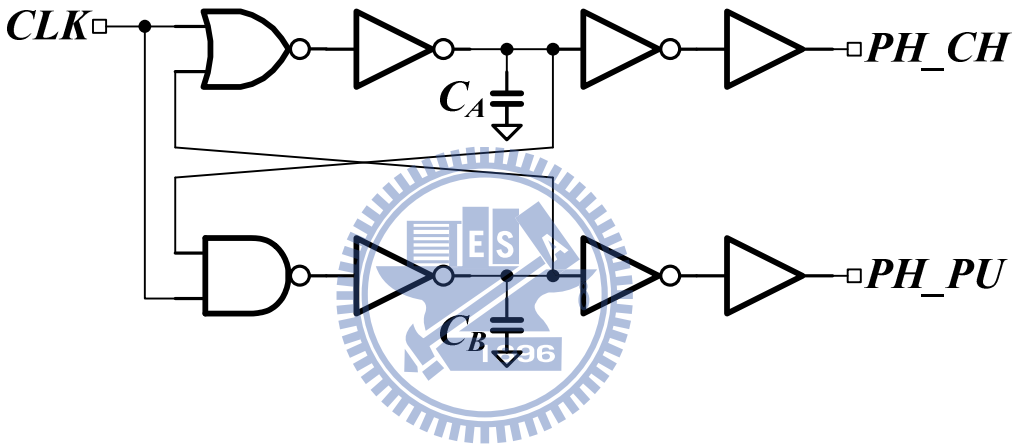


Fig. 29. Clock Phase Generation Circuit.

Fig. 30 shows the simulation results of clock phase generator. The $T_{non\text{-}overlap}$ is the non-overlap time between the charge phase and the pump phase control signals. With a proper design, this non-overlap time can prevent the leakage current when the different phase changes.

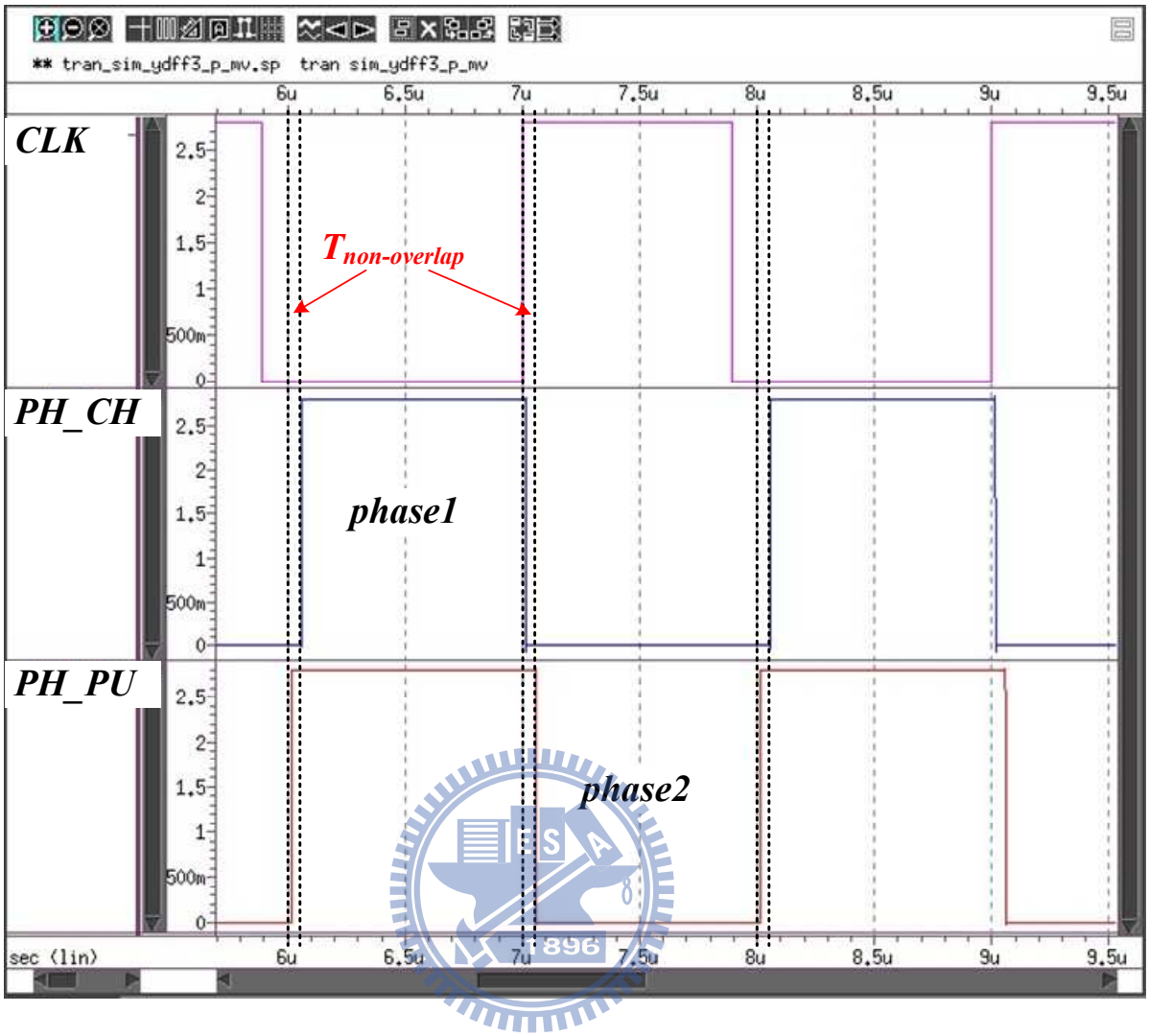


Fig. 30. Simulation Results of Clock Phase Generator.

LSH_P6V Level Shifter

Level shifters are quite frequently used in various application ICs. Fig. 31 is a typical level shifter that transforms the signals of VCI domain into DDVDH domain.

The logic high of the signals IN and INB are as high as VCI which ranges from 2.5V to 3.6V. The logic high of the signals OUT and OUTB are as high as DDVDH which ranges from 4.7V to 6V.

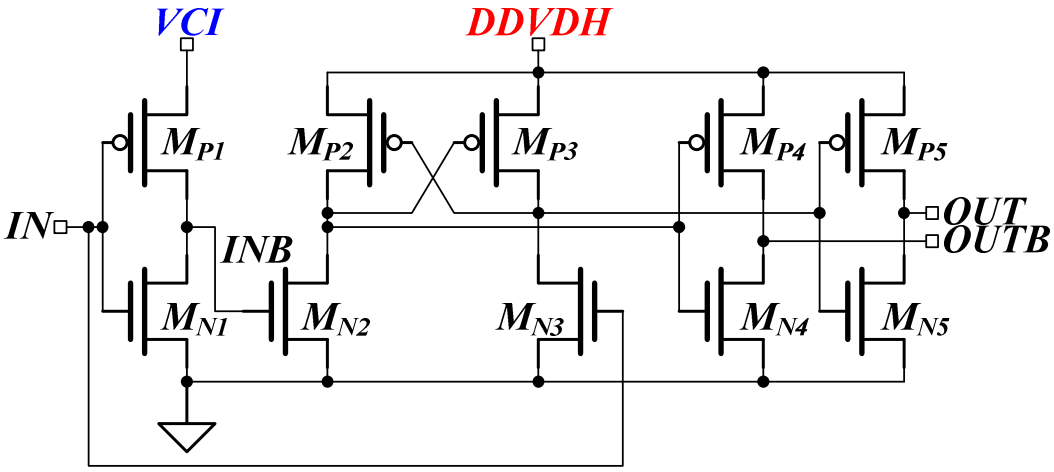


Fig. 31. LSH_P6V Level Shifter.

If the IN signal is equal to VCI, then the INB signal is equal to zero. At this time, the drain voltage of M_{N3} is pulled to ground because the M_{N3} is turned on, and this zero voltage being applied to the gate of M_{P2} turns M_{P2} on, resulting in a logic high level up to DDVDH. The DDVDH voltage of both the drain side of M_{P2} and M_{N2} turns M_{P3} off.

The key design point of M_{N2}, M_{N3}, M_{P2} and M_{P3} is that M_{P2} and M_{P3} should be designed weaker enough than M_{N2} and M_{N3}. The gate to source voltages of M_{N2} and M_{N3} are only up to VCI, but the gate to source voltages of M_{P2} and M_{P3} are up to DDVDH. So M_{P2} and M_{P3} should be designed weaker than M_{N2} and M_{N3}, and how weak design is depends on the specification of VCI and DDVDH voltage range.

Fig. 32 shows the simulation results of the level shifter. Assuming the VCI voltage is 3V, and the DDVDH voltage is 6V. As we can see in this figure, when the signal IN is equal to 3V, the OUT signal is equal to 6V and the OUTB signal is equal to 0V. On the contrary, when the signal IN is equal to 0V, the OUT signal is equal to 0V and the OUTB signal is equal to 6V. The level shifter successfully transforms the IN signal from 3V (VCI) domain into 6V (DDVDH) domain.

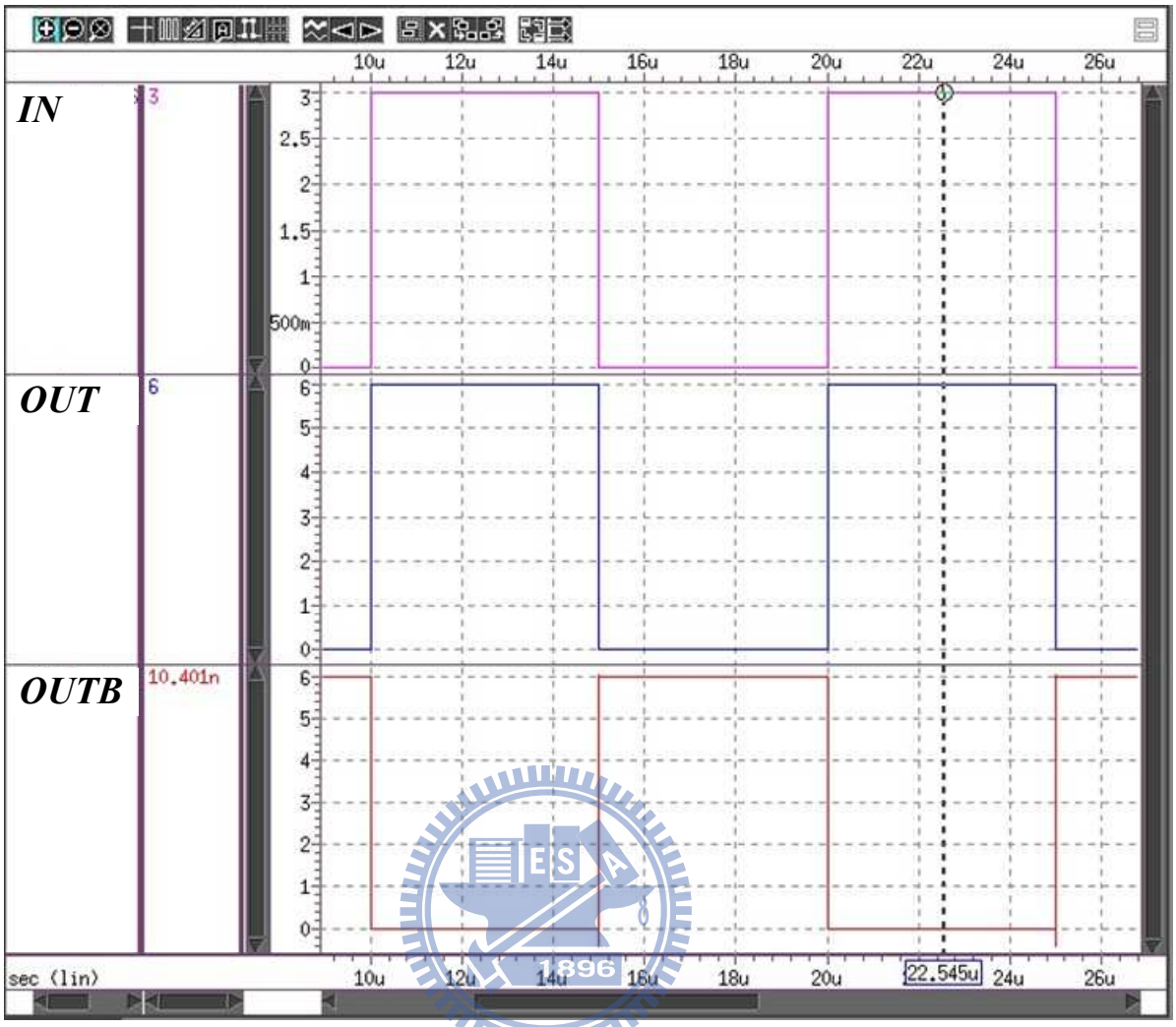


Fig. 32. Simulation Result of LSH_P6V Level Shifter.

LSH_N3V Level Shifter

Level shifters are quite frequently used in various application ICs. Fig. 33 is a typical level shifter that transforms the signals of VCI domain into VCI/VCL domain.

The logic high of the signals IN and INB are as high as VCI which ranges from 2.5V to 3.6V. The logic high of the signals OUT and OUTB are as high as VCI whether the logic of the signals OUT and OUTB are as low as VCL which ranges from -2.4V to -3V.

If the IN signal is equal to VCI, then the INB signal is equal to zero. At this time, the drain voltage of M_{N3} is pulled to ground because the M_{N3} and M_{N3A} are turned on, and this zero voltage being applied to the gate of M_{N2A} turns M_{N2A} off. And the zero voltage of the

INB signal turns off the M_{N2} but turns on the M_{P2} resulting in a logic high level up to VCI, turning M_{N3A} on.

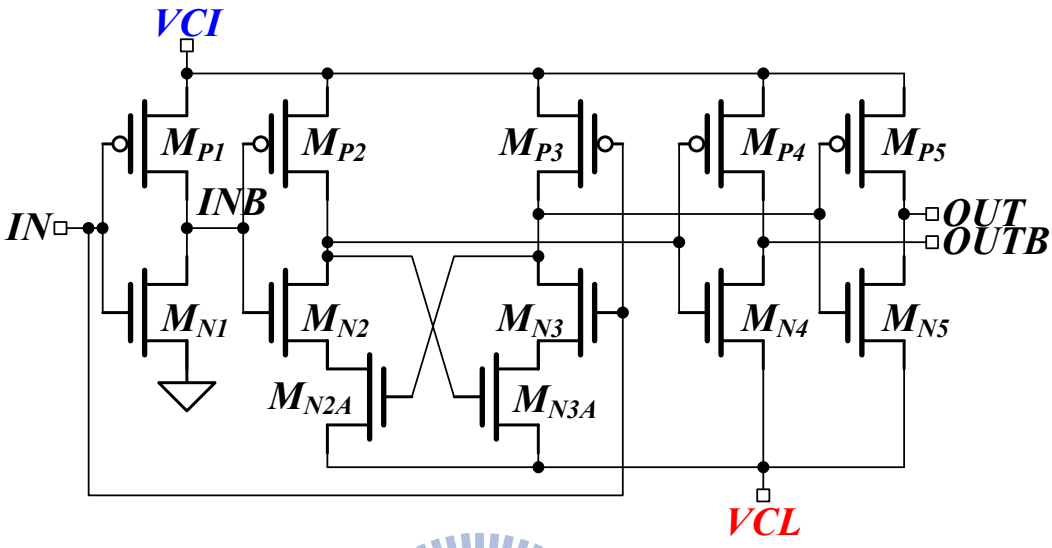


Fig. 33. LSH_N3V Level Shifter.

Fig. 34 shows the simulation results of the level shifter. Assuming the VCI voltage is 3V, and the VCL voltage is -3V. As we can see in the figure, when the signal IN is equal to 3V, the OUT signal is equal to 3V and the OUTB signal is equal to -3V. On the contrary, when the signal IN is equal to 0V, the OUT signal is equal to -3V and the OUTB signal is equal to 3V. The level shifter successfully transforms the IN signal from 3V (VCI) domain into 3V/-3V (VCI/VCL) domain.

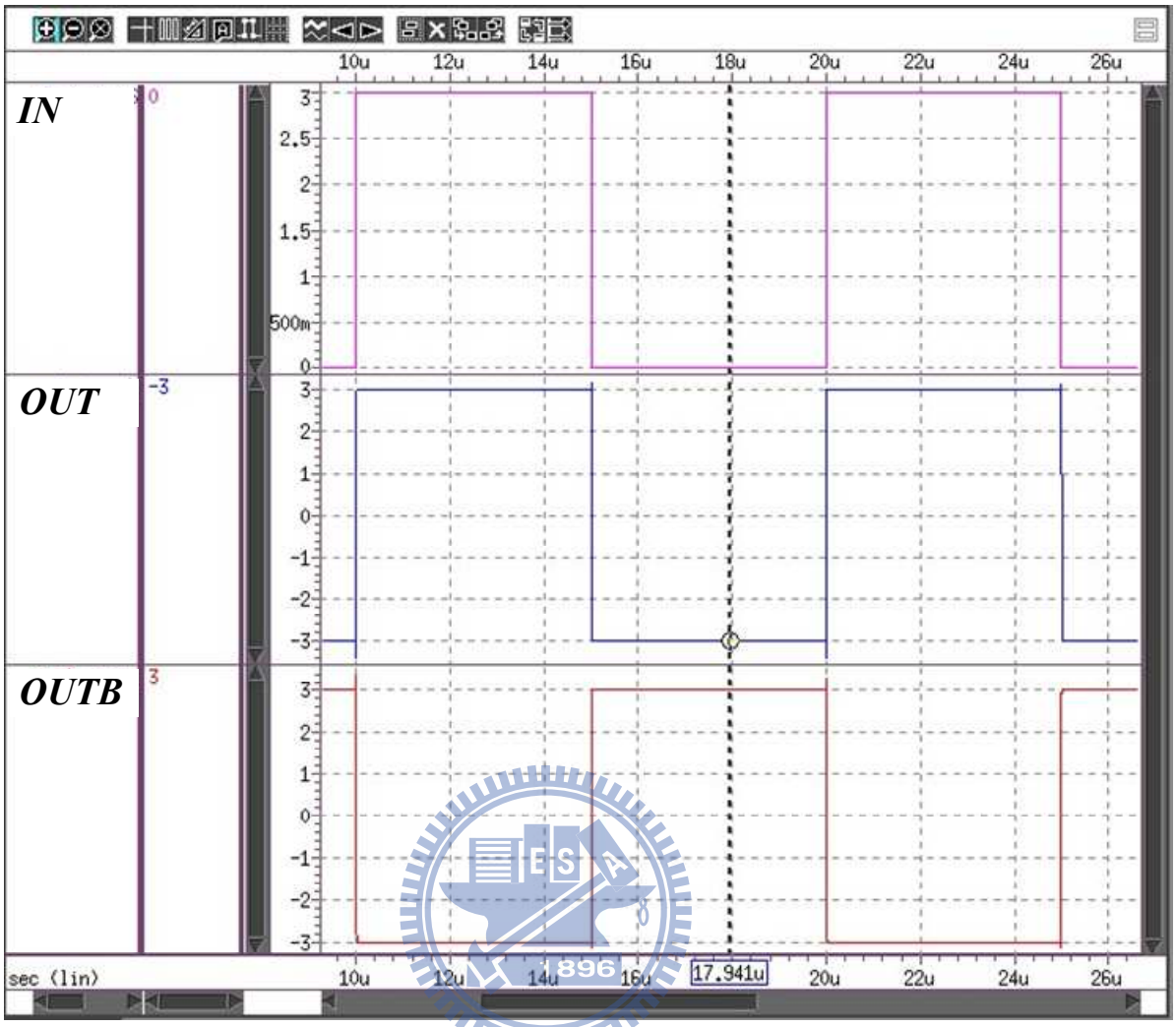


Fig. 34. Simulation Results of LSH_N3V Level Shifter.

3.1.1 Dual Side Voltage Doubler

Power Switches

Fig. 35 illustrates the power switches of the dual side voltage doubler with 8 power switches, 7 pin outs and 2 flying capacitors. The dual side voltage doubler is composed of two single side voltage doublers. The flying capacitor C_{11} and 4 power switches M_{11A}, M_{12A}, M_{13A} and M_{14A} realize a single side voltage doubler, while the flying capacitor C_{12} and 4 power switches M_{11B}, M_{12B}, M_{13B} and M_{14B} realize another single side voltage doubler.

The 2.1Ω turning on resistance R_{DSON} of the power switch M_{11A} is listed in Fig. 33 and we symbolize it as R_{SWM11A}. In the following discussions, we will use R_{SWMxx} as the

resistances R_{DSON} of all other power switches. The resistors R_{M11A}, R_{M12A}, R_{M13A}, R_{M14A}, R_{M11B}, R_{M12B}, R_{M13B} and R_{M14B} represent the IC layout metal routing resistances between the power switches and DDVDH, VCI and DGND pin outs. The resistors $R_{itoC11N}$, $R_{itoC11P}$, $R_{itoC12N}$, $R_{itoC12P}$ represent the TFT-LCD panel ITO (Indium Tin Oxide) parasitic resistances of the pin outs C_{11N}, C_{11P}, C_{12N} and C_{12P} individually. The resistors R_{itoVCI}, $R_{itoDGND}$ and $R_{itoDDVDH}$ represent the TFT-LCD panel ITO parasitic resistances of the pin outs VCI, DGND and DDVDH individually.

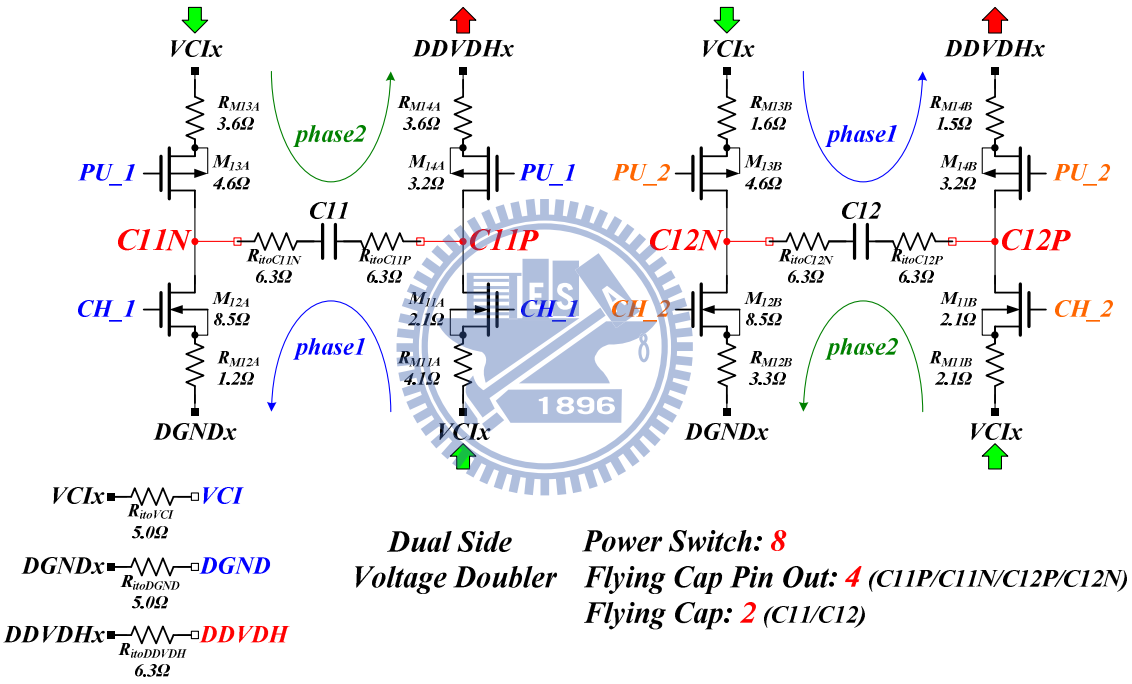


Fig. 35. Power Switches of Dual Side Voltage Doubler.

Fig. 36 is the simulation results of the dual side voltage doubler. During the phase1, C_{11} is in the charging phase, being connected to V_{IN}, while C_{12} is in the pumping phase, being connected to DDVDH. As in Fig. 36, the output current I_{OUT} of DDVDH is 2mA. During the phase1, a current of I_{OUT} flows from the VCI pin through M_{11A}, C_{11} and M_{12A} to the DGND pin, and there is also a current of I_{OUT} flows from the VCI pin through M_{13B}, C_{12} and M_{14B} to the DDVDH pin.

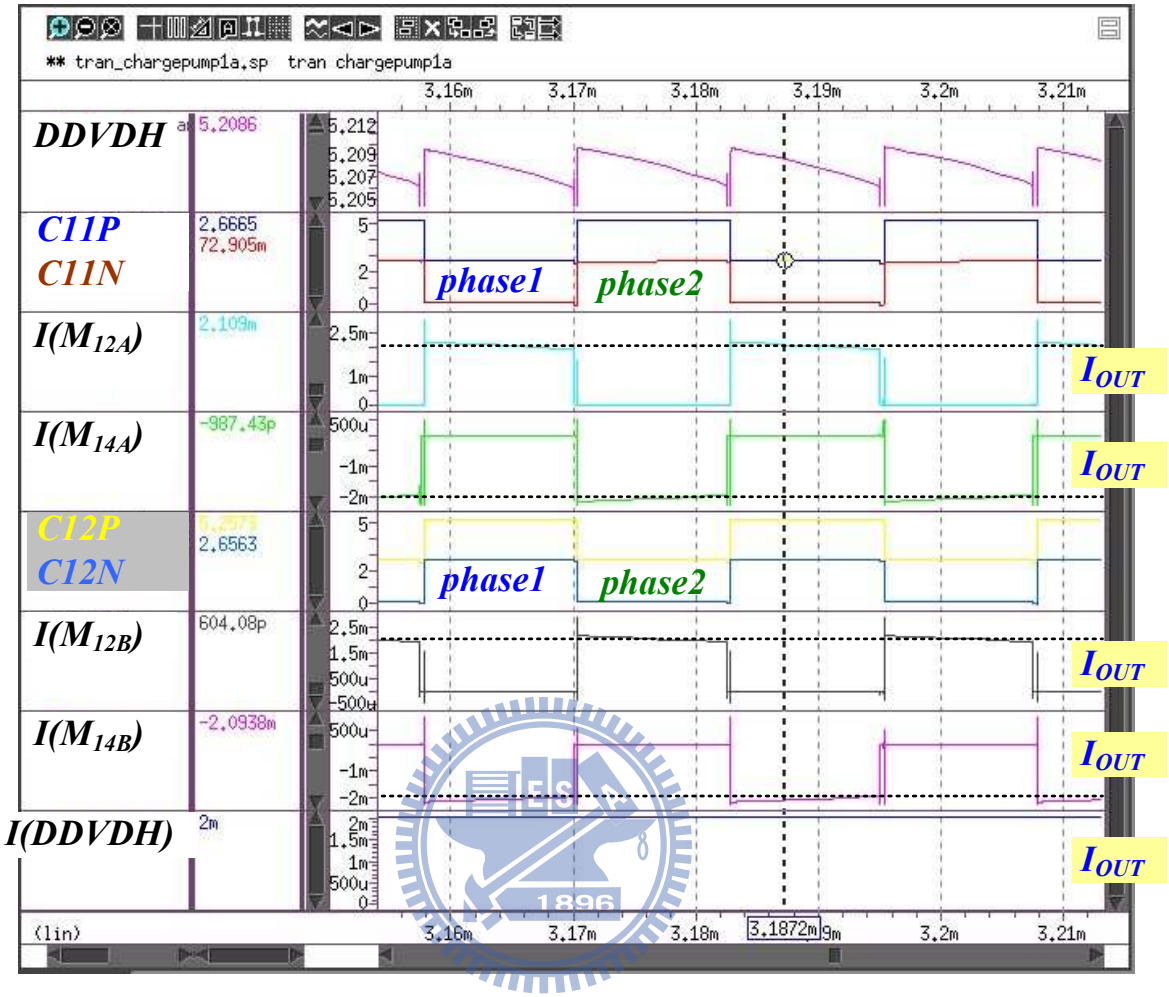


Fig. 36. Simulation Result of Dual Side Voltage Doubler.

During the phase2, C_{11} is in the pumping phase, being connected to DDVDH, while C_{12} is in the charging phase, being connected to VCI. A current of I_{OUT} flows from the VCI pin through M_{13A}, C_{11} and M_{14A} to the DDVDH pin, and there is also a current of I_{OUT} flows from the VCI pin through M_{11B}, C_{12} and M_{12B} to the DGND pin. There is always an rms current of IOUT flowing through R_{PH1A_SW1}, R_{PH1A_SW2}, R_{PH2A_SW1}, R_{PH2A_SW2} for C_{11}, and R_{PH2B_SW1}, R_{PH2B_SW2}, R_{PH1B_SW1}, R_{PH1B_SW2} for C_{12}. Assuming the switching frequency is 40kHz.

For C_{11},

$$R_{PH1A\_SW1} = R_{itoVCI} + R_{M11A} + R_{SWM11A} + R_{itoC11P} = 5 + 4.1 + 2.1 + 6.3 = 17.5\Omega \quad (38)$$

$$R_{PH1A\_SW2} = R_{itoC11N} + R_{SWM12A} + R_{M12A} + R_{itoDGND} = 6.3 + 8.5 + 1.2 + 5 = 21\Omega$$

$$R_{PH2A\_SW1} = R_{itoVCI} + R_{M13A} + R_{SWM13A} + R_{itoC11N} = 5 + 3.6 + 4.6 + 6.3 = 19.5\Omega$$

$$R_{PH2A\_SW2} = R_{itoC11P} + R_{SWM14A} + R_{M14A} + R_{itoDDVDH} = 6.3 + 3.2 + 3.6 + 6.3 = 19.4\Omega$$

$$R_{SWITCHING\_C11} = \frac{1}{f \cdot C_{11}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For C_{12},

$$R_{PH2B\_SW1} = R_{itoVCI} + R_{M11B} + R_{SWM11B} + R_{itoC12P} = 5 + 2.1 + 2.1 + 6.3 = 15.5\Omega$$

$$R_{PH2B\_SW2} = R_{itoC12N} + R_{SWM12B} + R_{M12B} + R_{itoDGND} = 6.3 + 8.5 + 3.3 + 5 = 23.1\Omega$$

$$R_{PH1B\_SW1} = R_{itoVCI} + R_{M13B} + R_{SWM13B} + R_{itoC12N} = 5 + 1.6 + 4.6 + 6.3 = 17.5\Omega \quad (39)$$

$$R_{PH1B\_SW2} = R_{itoC12P} + R_{SWM14B} + R_{M14B} + R_{itoDDVDH} = 6.3 + 3.2 + 1.5 + 6.3 = 17.3\Omega$$

$$R_{SWITCHING\_C12} = \frac{1}{f \cdot C_{12}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For the R_{OUT} of the dual side voltage doubler,

$$R_{OUT\_dual\_side\_doubler} = [0.5 \cdot (17.5 + 21) + 0.5 \cdot (19.5 + 19.4)] + [0.5 \cdot (15.5 + 23.1) + 0.5 \cdot (17.5 + 17.3)] + 25 // 25 = 87.9\Omega \quad (40)$$

Comparing to TABLE III, Eq. 40, the R_{OUT} of the dual side voltage doubler is much smaller than the output impedance specification of DDVDH $\boldsymbol{R_{OUT\_DDVDH\_MAX}=150\Omega}$. That means the driving ability of the designed dual side voltage doubler can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side voltage doubler,

$$V_{RIPPLE\_dual\_side\_doubler} = 2m / (2 \cdot 40k \cdot 1u) = 25mV \quad (41)$$

Comparing to TABLE III, Eq. 41, the output voltage ripple of the dual side voltage doubler is much smaller than the output voltage ripple specification 1V.

3.1.2 Dual Side Voltage Inverter

Power Switches

Fig. 37 illustrates the power switches of the dual side voltage inverter with 8 power switches, 7 pin outs and 2 flying capacitors. The dual side voltage inverter is composed of two single side voltage inverters. The flying capacitor C_{31} and 4 power switches M_{31A}, M_{32A}, M_{33A} and M_{34A} realize a single side voltage inverter, while the flying capacitor C_{32} and 4 power switches M_{31B}, M_{32B}, M_{33B} and M_{34B} realize another single side voltage inverter.

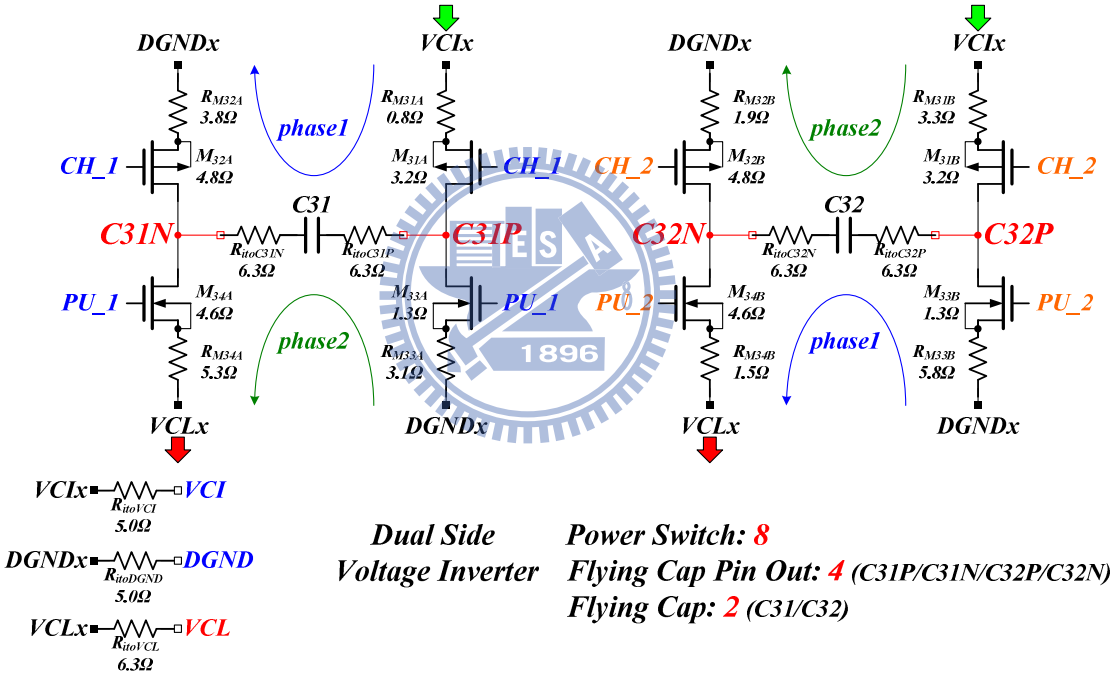


Fig. 37. Power Switches of Dual Side Voltage Inverter.

The 3.2Ω turning on resistance R_{DSON} of the power switch M_{31A} is listed in Fig. 38 and we symbolize it as R_{SWM31A}. In the following discussions, we will use R_{SWMxx} as the resistances R_{DSON} of all other power switches. The resistors R_{M31A}, R_{M32A}, R_{M33A}, R_{M34A}, R_{M31B}, R_{M32B}, R_{M33B} and R_{M34B} represent the IC layout metal routing resistances between the power switches and VCI, DGND and VCL pin outs. The resistors $R_{itoC31N}$, $R_{itoC31P}$, $R_{itoC32N}$,

$R_{itoC32P}$ represent the TFT-LCD panel ITO parasitic resistances of the pin outs C_{31N}, C_{31P}, C_{32N} and C_{32P} individually. The resistors R_{itoVCI}, $R_{itoDGND}$ and R_{itoVCL} represent the TFT-LCD panel ITO parasitic resistances of the pin outs VCI, DGND and VCL individually.

Fig. 38 is the simulation results of the dual side voltage inverter.

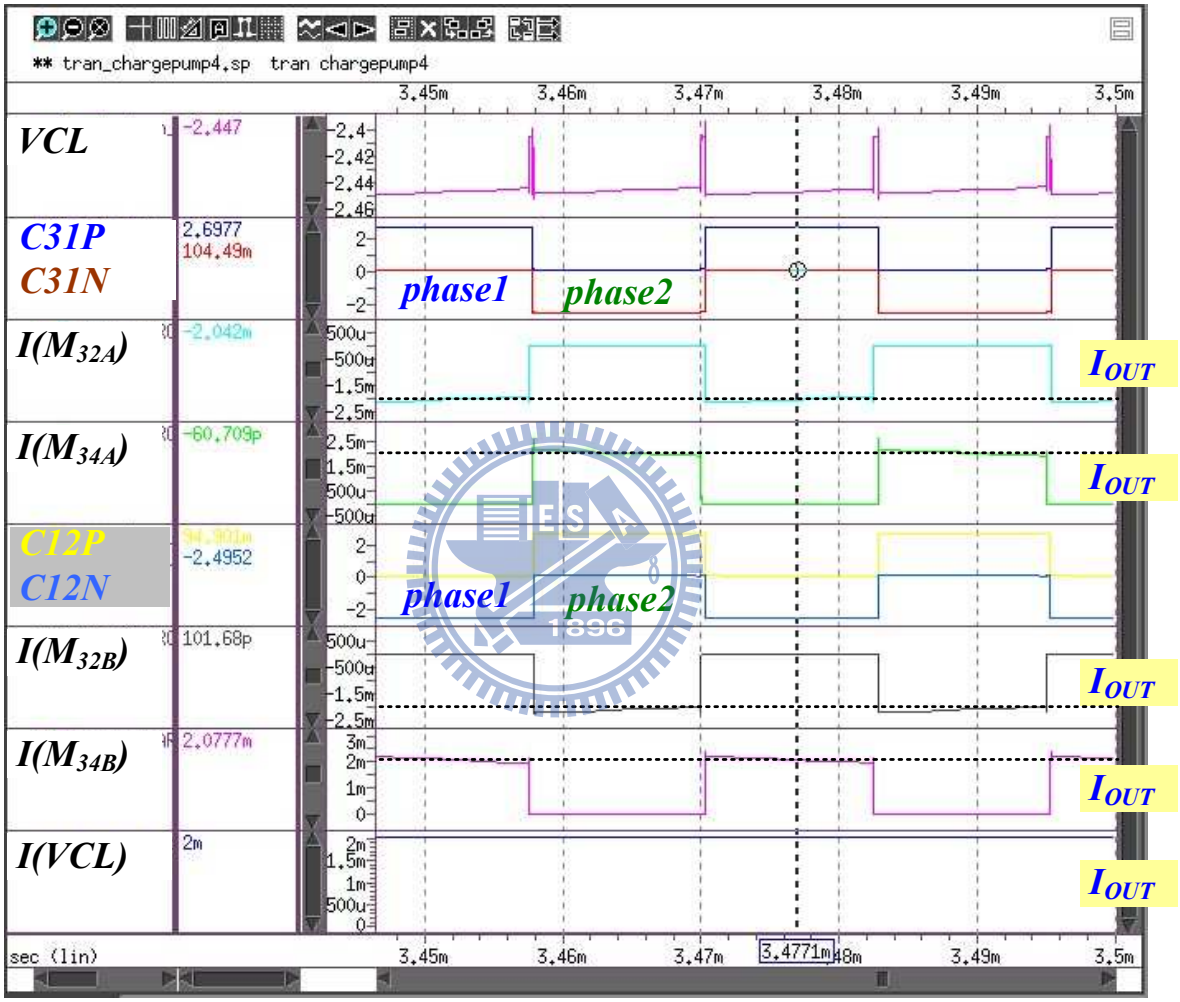


Fig. 38. Simulation Result of Dual Side Voltage Inverter.

During the phase1, C_{31} is in the charging phase, being connected to V_{IN}, while C_{32} is in the pumping phase, being connected to VCL. As in Fig. 39, the output current I_{OUT} of VCL is 2mA. During the phase1, a current of I_{OUT} flows from the VCI pin through M_{31A}, C_{31} and M_{32A} to the DGND pin, and there is also a current of I_{OUT} flows from the DGND pin through M_{33B}, C_{32} and M_{34B} to the VCL pin.

During the phase2, C_{31} is in the pumping phase, being connected to VCL, while C_{32} is in the charging phase, being connected to VCI. A current of I_{OUT} flows from the DGND pin through M_{33A}, C_{31} and M_{34A} to the VCL pin, and there is also a current of I_{OUT} flows from the VCI pin through M_{31B}, C_{32} and M_{32B} to the DGND pin. There is always an rms current of IOUT flowing through R_{PH1A_SW1}, R_{PH1A_SW2}, R_{PH2A_SW1}, R_{PH2A_SW2} for C_{31}, and R_{PH2B_SW1}, R_{PH2B_SW2}, R_{PH1B_SW1}, R_{PH1B_SW2} for C_{32}. Assuming the switching frequency is 40kHz.

For C_{31},

$$R_{PH1A\_SW1} = R_{itoVCI} + R_{M31A} + R_{SWM31A} + R_{itoC31P} = 5 + 0.8 + 3.2 + 6.3 = 15.3\Omega$$

$$R_{PH1A\_SW2} = R_{itoC13N} + R_{SWM32A} + R_{M32A} + R_{itoDGND} = 6.3 + 4.8 + 3.8 + 5 = 19.9\Omega$$

$$R_{PH2A\_SW1} = R_{itoDGND} + R_{M33A} + R_{SWM33A} + R_{itoC31P} = 5 + 3.1 + 1.3 + 6.3 = 15.7\Omega \quad (42)$$

$$R_{PH2A\_SW2} = R_{itoC31N} + R_{SWM34A} + R_{M34A} + R_{itoVCL} = 6.3 + 4.6 + 5.3 + 6.3 = 22.5\Omega$$

$$R_{SWITCHING\_C31} = \frac{1}{f \cdot C_{31}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For C_{32},

$$R_{PH2B\_SW1} = R_{itoVCI} + R_{M31B} + R_{SWM31B} + R_{itoC32P} = 5 + 3.3 + 3.2 + 6.3 = 17.8\Omega$$

$$R_{PH2B\_SW2} = R_{itoC32N} + R_{SWM32B} + R_{M32B} + R_{itoDGND} = 6.3 + 4.8 + 1.9 + 5 = 18\Omega$$

$$R_{PH1B\_SW1} = R_{itoDGND} + R_{M33B} + R_{SWM33B} + R_{itoC32N} = 5 + 5.8 + 1.3 + 6.3 = 18.4\Omega \quad (43)$$

$$R_{PH1B\_SW2} = R_{itoC32N} + R_{SWM34B} + R_{M34B} + R_{itoVCL} = 6.3 + 4.6 + 1.5 + 6.3 = 18.7\Omega$$

$$R_{SWITCHING\_C32} = \frac{1}{f \cdot C_{32}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For the R_{OUT} of the dual side voltage inverter,

$$R_{OUT\_dual\_side\_inverter} = [0.5 \cdot (15.3 + 19.9) + 0.5 \cdot (15.7 + 22.5)] + [0.5 \cdot (17.8 + 18) + 0.5 \cdot (18.4 + 18.7)] + 25 // 25 = 85.65\Omega \quad (44)$$

Comparing to TABLE III, Eq. 44, the R_{OUT} of the dual side voltage inverter is much

smaller than the output impedance specification of DDVDH $\boldsymbol{R_{OUT\_VCL\_MAX}=125\Omega}$. That means the driving ability of the designed dual side voltage inverter can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side voltage inverter,

$$V_{RIPPLE\_dual\_side\_inverter} = 1m/(2 \cdot 40k \cdot 1u) = 12.5mV \quad (45)$$

Comparing to TABLE III, Eq. 45, the output voltage ripple of the dual side voltage inverter is much smaller than the output voltage ripple specification 1V.

The conventional voltage doubler and voltage inverter need 4 flying capacitors which are C_{11}, C_{12}, C_{31} and C_{32}; 12 pin outs which are VCI, DGND, DDVDH, VCL, C_{11P}, C_{11N}, C_{12P}, C_{12N}, C_{31P}, C_{31N}, C_{32P} and C_{32N}; 16 power switches which are M_{11A}, M_{12A}, M_{13A}, M_{14A}, M_{11B}, M_{12B}, M_{13B}, M_{14B}, M_{31A}, M_{32A}, M_{33A}, M_{34A}, M_{31B}, M_{32B}, M_{33B} and M_{34B}. We are going to see the differences between the conventional converters and the proposed converter in the following section.

3.2 New Proposed Voltage Converter

The new proposed dual side dual output switching capacitor voltage converter can generate DDVDH and VCL voltage by assert two more phase clocks. Let's gain more insight in the following sections.

3.2.1 Dual Side Dual Output Switching Capacitor Voltage Converter

Circuit Structure and Implementation

Fig. 39 illustrates the proposed dual side dual output voltage doubler. The proposed charge pump is composed of three parts. The CLK_PHASE_GEN circuit generates four phase

clocks to control this charge pump. The LSH_P6V and LSH_N3V transforms the signal voltage level from 3V to 6V domain and to 3V/-3V domain. The POWER SWITCH block contains the power switches needed for this charge pump. This dual side dual output voltage converter utilizes two flying capacitors C_{11} and C_{12} to generate small ripple DDVDH voltage and VCL voltage. The flying capacitors C_{11}, C_{12} and the stabilize capacitors are all external components.

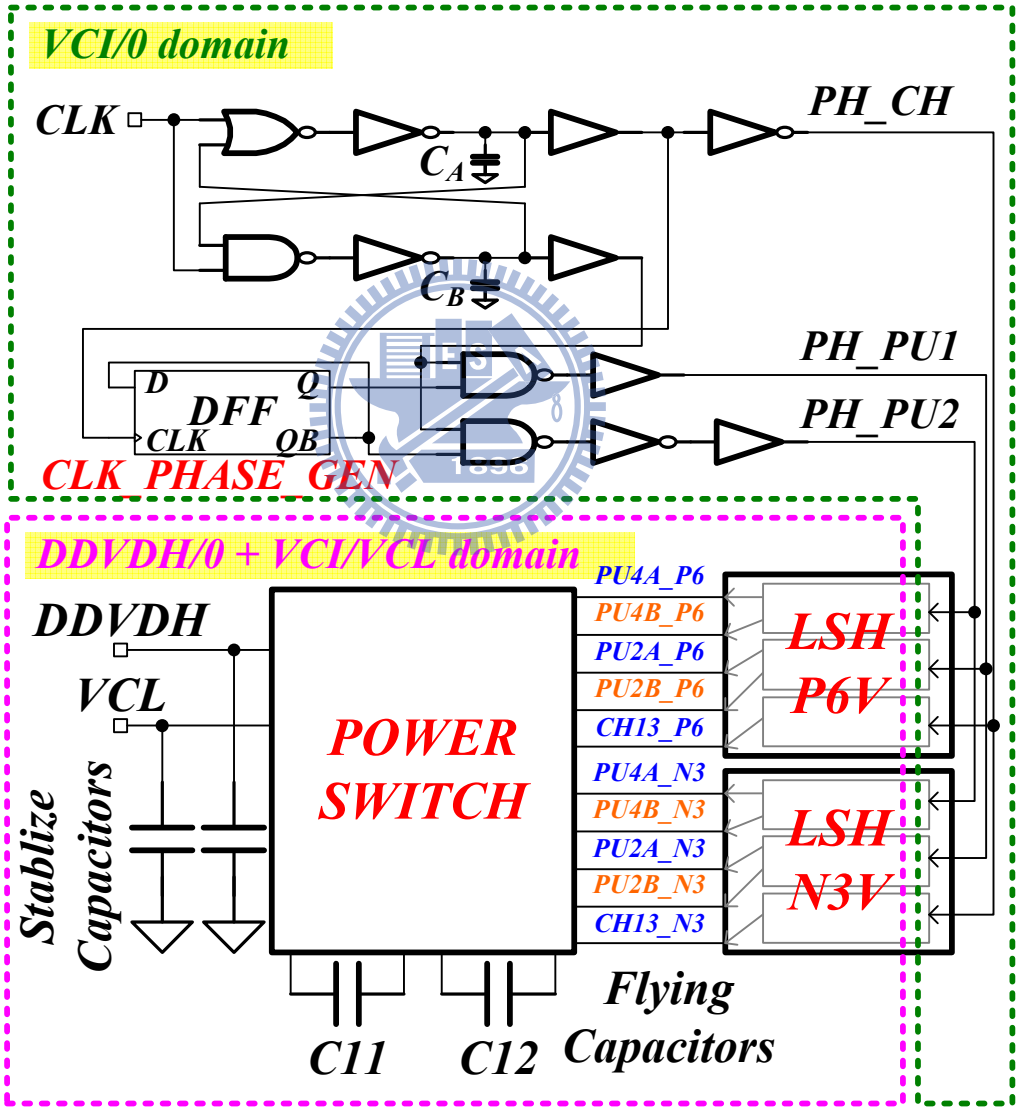


Fig. 39. Dual Side Dual Output Voltage Converter.

Clock Phase Generation Circuit

Fig. 40 is the clock phase generation circuit of the proposed voltage converter. The clock phase generation circuit is used to generate the charge phases and pump phases for the dual side dual output voltage converter. As in Fig. 40, CLK is the clock signal coming from the TCON. PH_CH is the phase control signal for the charging phases. PH_PU1 is the phase control signal for the pumping phase. PH_PU2 is also the phase control signal for the pumping phase. The internal capacitors C_A and C_B are used to adjust non-overlap timing which prevents from the possible occurring leakage currents during phase change as we mentioned before. As to the DFF, it is used to insert two more inter-leave phases for the dual side dual output voltage converter.

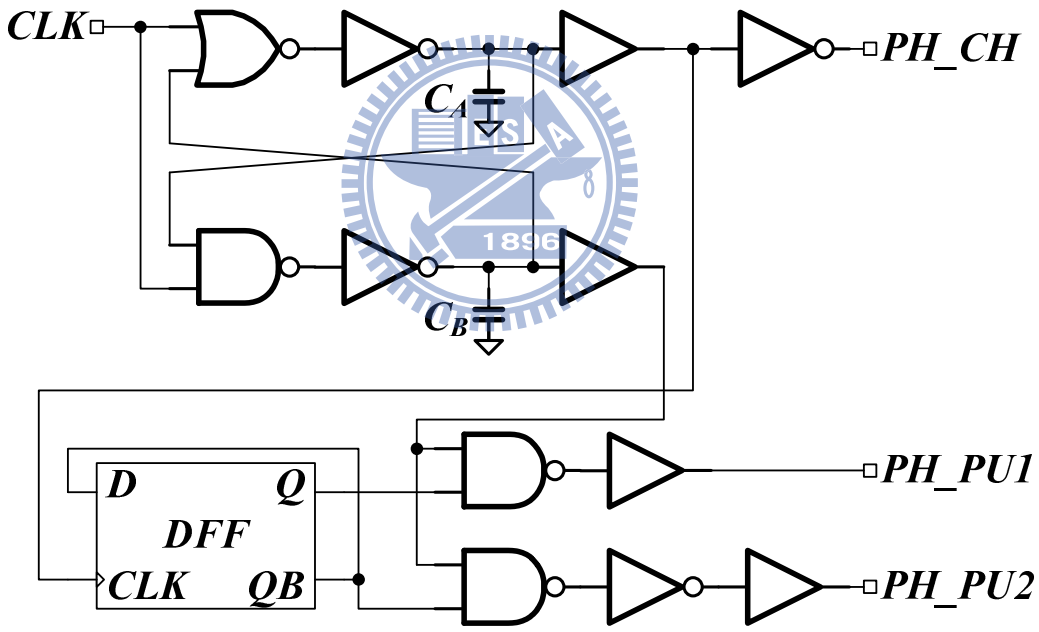


Fig. 40. Clock Phase Generation Circuit.

Fig. 41 shows the simulation results of clock phase generator. The $T_{non\text{-}overlap}$ is the non-overlap time between the phase1, phase2, phase3 and phase4. With proper design, this non-overlap time can prevent the leakage current when the different phase changes.

There are four phases for the new proposed charge pump. Phase1 and phase3 are responsible for the charging phase. Phase2 is responsible for the pumping phase which pumps

DDVDH or VCL voltage. Phase4 is also responsible for the pumping phase which pumps DDVDH or VCL voltage. Phase 3 and phase 4 are new extra charging and pumping phase clocks for the dual side dual output operation.

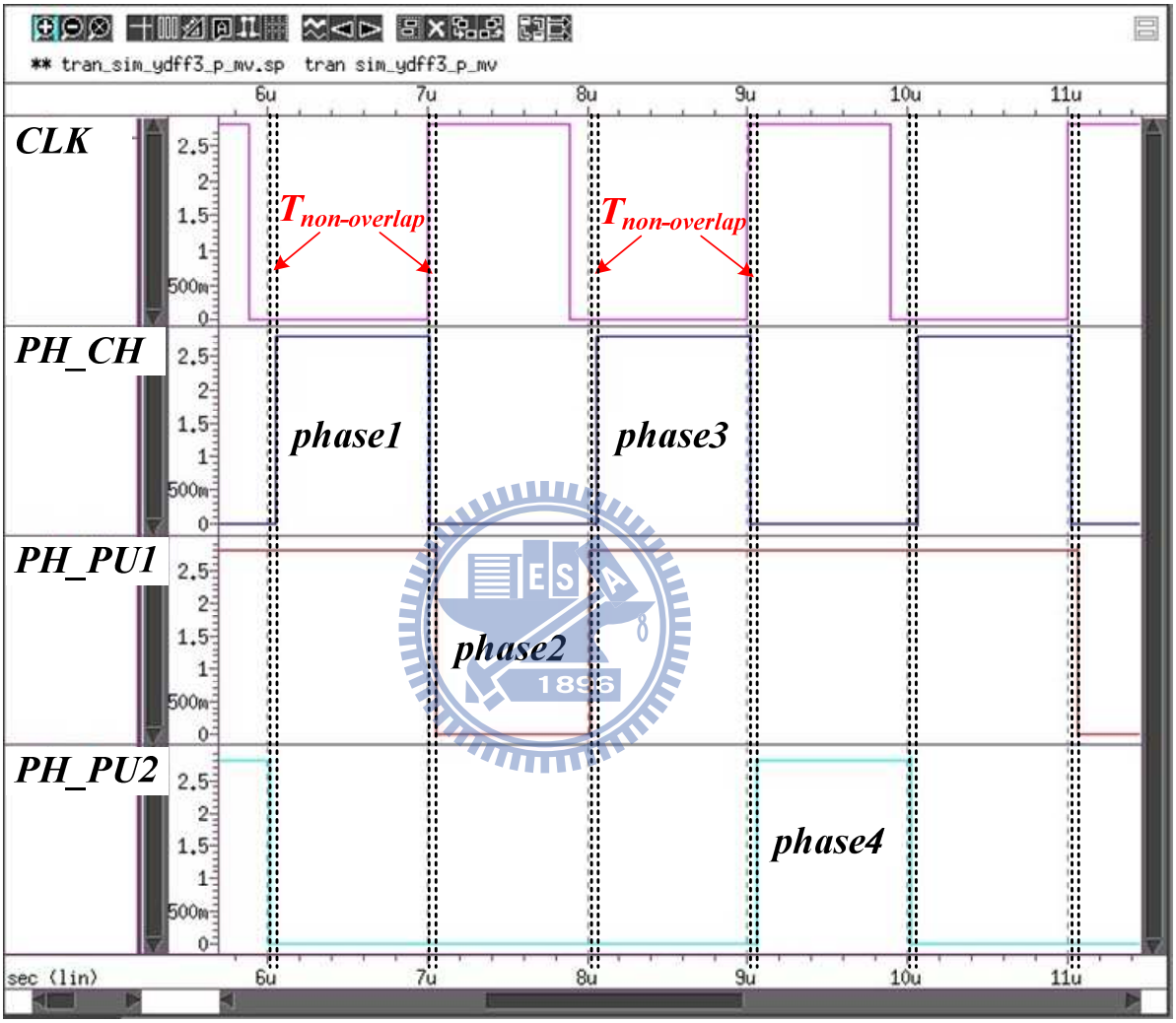


Fig. 41. Simulation Result of Clock Phase Generation Circuit.

Power Switches

Fig. 42 illustrates the power switches of the dual side dual output voltage converter with 12 power switches, 8 pin outs and 2 flying capacitors.

The dual side dual output voltage converter is composed of two single side dual output voltage converters. The flying capacitor C_{11} and 6 power switches M_{1A}, M_{2A}, M_{3A}, M_{4A}, M_{5A}

and M_{6A} realize a single side dual output voltage converter, while the flying capacitor C_{12} and the other 6 power switches M_{1B}, M_{2B}, M_{3B}, M_{4B}, M_{5B} and M_{6B} realize another single side dual output voltage converter.

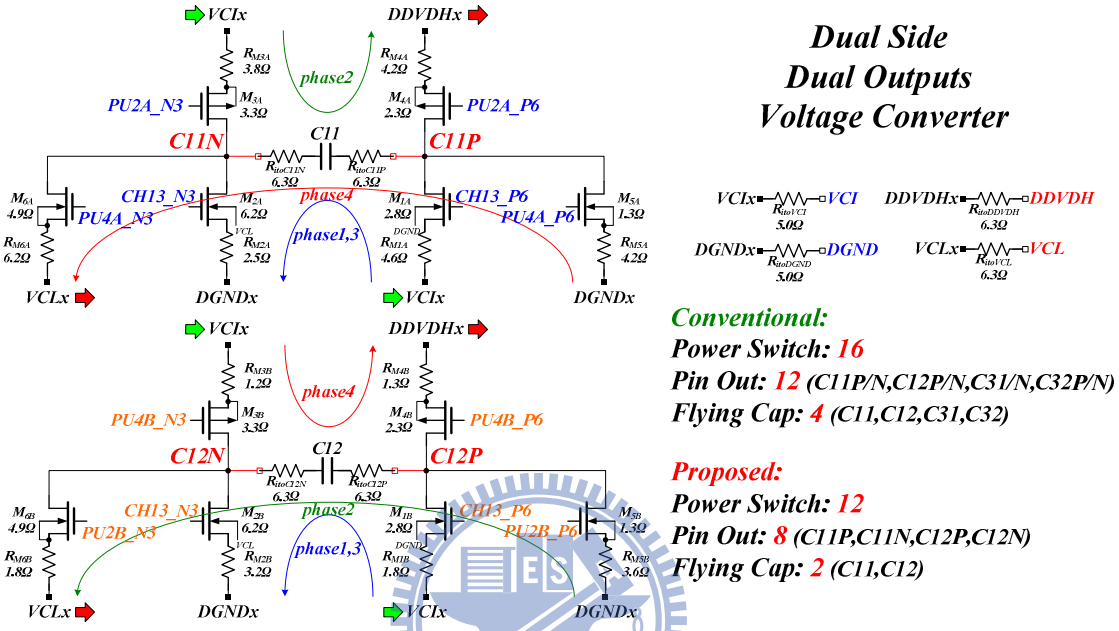


Fig. 42. Power Switches of Dual Side Dual Output Voltage Converter.

The 2.8Ω turning on resistance R_{DSON} of the power switch M_{1A} is listed in Fig. 42 and we symbolize it as R_{SWM1A}. In the following discussions, we will use R_{SWMxx} as the resistances R_{DSON} of all other power switches. The resistors R_{M1A}, R_{M2A}, R_{M3A}, R_{M4A}, R_{M5A}, R_{M6A}, R_{M1B}, R_{M2B}, R_{M3B}, R_{M4B}, R_{M5B} and R_{M6B} represent the IC layout metal routing resistances between the power switches and DDVDH, VCI, DGND and VCL pin outs. The resistors $R_{itoC11N}$, $R_{itoC11P}$, $R_{itoC12N}$ and $R_{itoC12P}$ represent the TFT-LCD panel ITO parasitic resistances of the pin outs C_{11N}, C_{11P}, C_{12N} and C_{12P} individually. The resistors R_{itoVCI}, $R_{itoDGND}$, $R_{itoDDVDH}$ and R_{itoVCL} represent the TFT-LCD panel ITO parasitic resistances of the pin outs VCI, DGND, DDVDH and VCL individually.

Fig. 43 shows the simulation results of dual side dual output voltage converter. In this simulation, the load currents of both DDVDH and VCL are 2mA. During the phase1 and

phase3, both C_{11} and C_{12} are in the charging phase, being connected to V_{IN}. During the phase2, C_{11} is in the pumping phase, being connected to DDVDH, while C_{12} is in the pumping phase, being connected to VCL. During the phase4, C_{11} is in the pumping phase, being connected to VCL, while C_{12} is in the pumping phase, being connected to DDVDH.

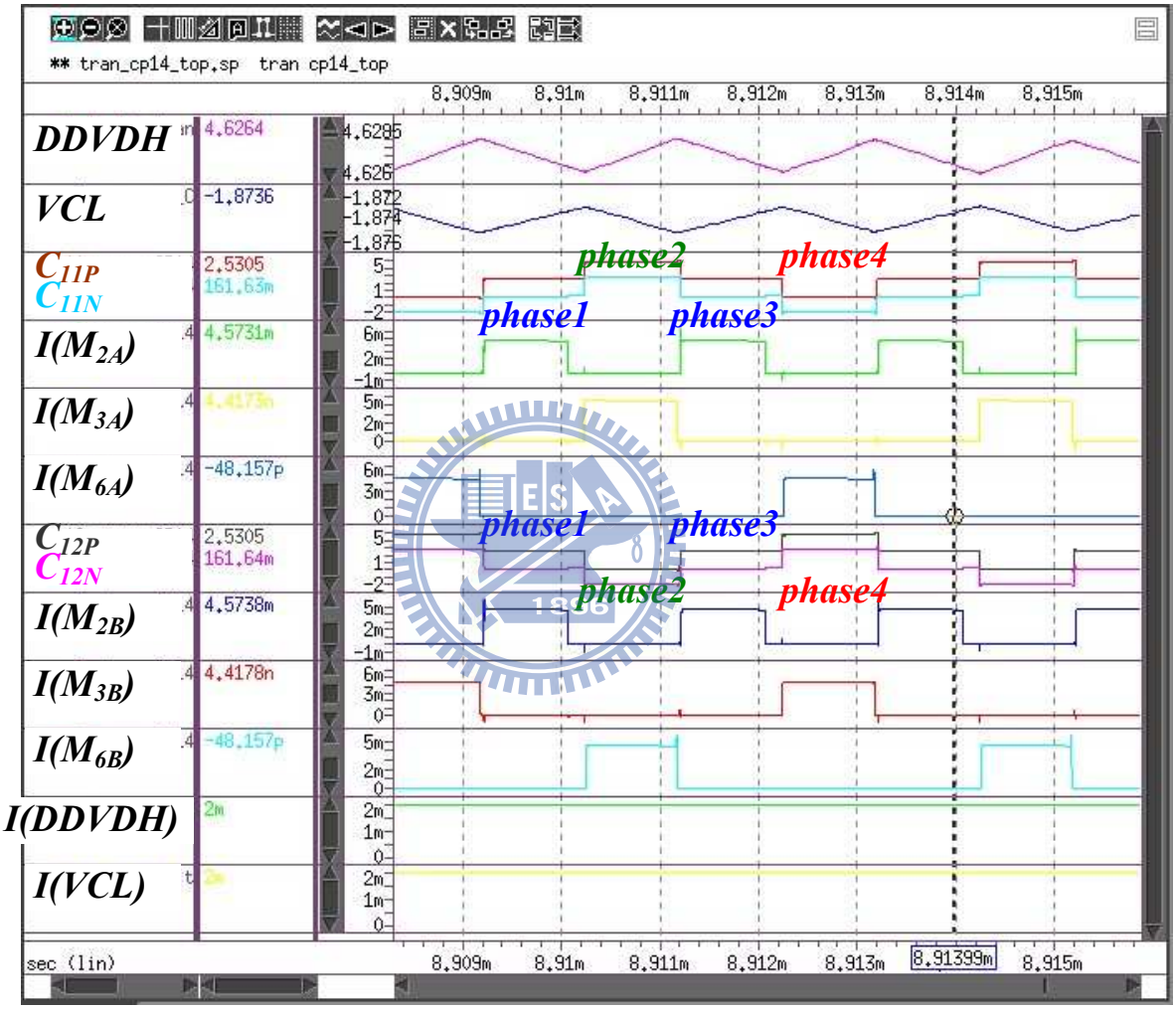


Fig. 43. Simulation Results of Dual Side Dual Output Voltage Converter.

Output Loading for DDVDH Only

To simplify and to distinguish the difference of the performance of DDVDH between the conventional doubler and the proposed converter, we are going to discuss the output current loading occurring only at DDVDH. Let's review the output impedance R_{OUT} and the output

voltage ripple of DDVDH of the dual side dual output voltage converter.

During the phase1 and phase3, both C_{11} and C_{12} are in the charging phase, being connected to V_{IN}. As in Fig. 44, the I_{OUT} output current of DDVDH is 2mA. During the phase1 and phase3, a current of I_{OUT} flows from the VCI pin through M_{1A}, C_{11} and M_{2A} to the DGND pin, and there is also a current of I_{OUT} flows from the VCI pin through M_{1B}, C_{12} and M_{2B} to the DGND pin. There is always an rms current of I_{OUT} flowing through $R_{PH1,3A\_SW1}$ and $R_{PH1,3A\_SW2}$ for C_{11}, and $R_{PH1,3B\_SW1}$ and $R_{PH1,3B\_SW2}$ for C_{12}.

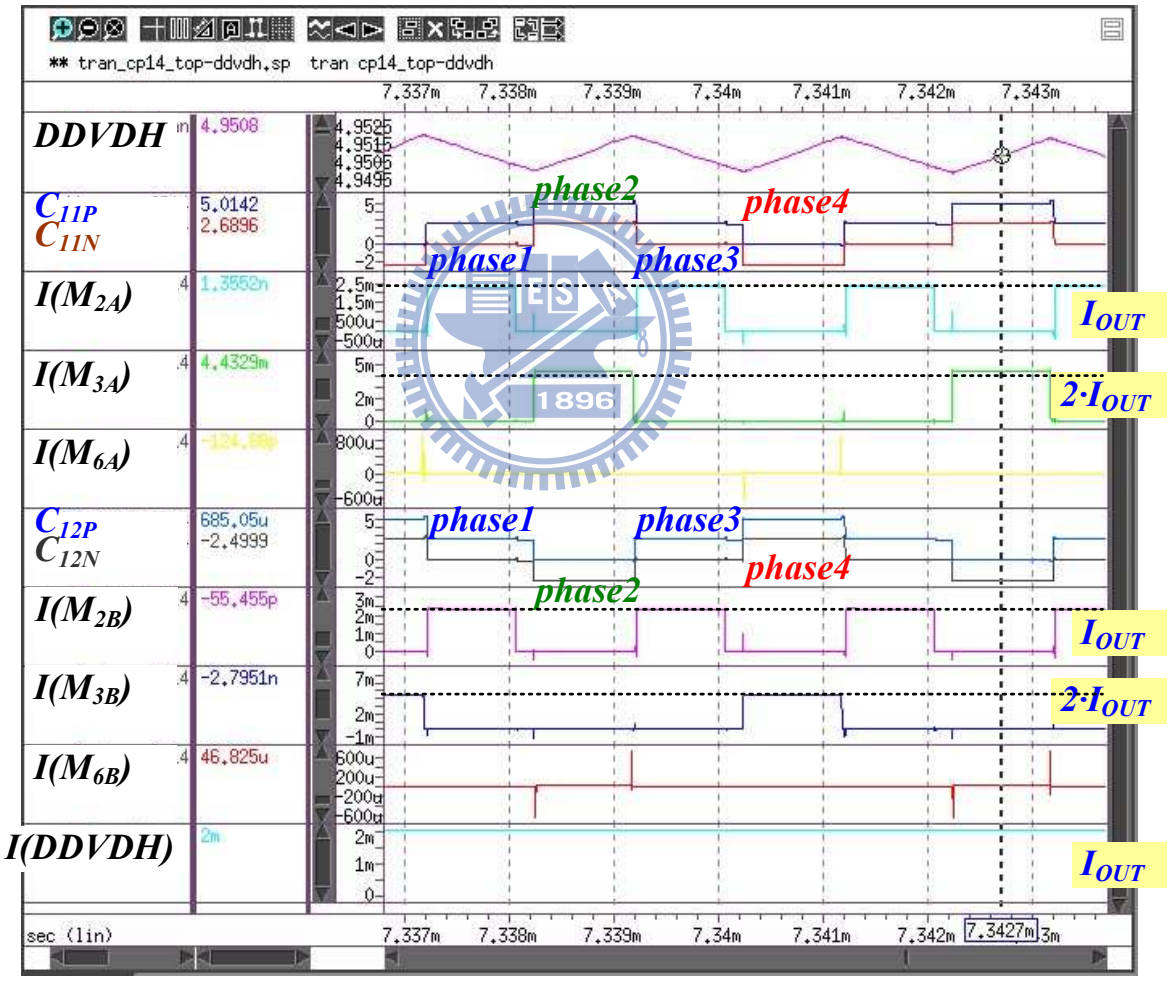


Fig. 44. Simulation Results of Dual Side Dual Output Voltage Converter: DDVDH only.

During the phase2, C_{11} is in the pumping phase, being connected to DDVDH, while C_{12} is in the pumping phase, being connected to VCL. A current of $2I_{OUT}$ flows from the VCI pin

through M_{3A}, C_{11} and M_{4A} to the DDVDH pin, and there is also a current of $2I_{OUT}$ flows from the DGND pin through M_{5B}, C_{12} and M_{6B} to the VCL pin. There is always an rms current of $2I_{OUT}$ flowing through R_{PH2A_SW1} and R_{PH2A_SW2} for C_{11}, and R_{PH2B_SW1} and R_{PH2B_SW2} for C_{12}.

During the phase4, C_{11} is in the pumping phase, being connected to VCL, while C_{12} is in the pumping phase, being connected to DDVDH. A current of $2I_{OUT}$ flows from the DGND pin through M_{5A}, C_{11} and M_{6A} to the VCL pin, and there is also a current of $2I_{OUT}$ flows from the VCI pin through M_{3B}, C_{12} and M_{4B} to the DDVDH pin. There is always an rms current of $2I_{OUT}$ flowing through R_{PH4A_SW1} and R_{PH4A_SW2} for C_{11}, and R_{PH4B_SW1} and R_{PH4B_SW2} for C_{12}.

Assuming the switching frequency is 40kHz. For C_{11},

$$R_{PH1,3A\_SW1} = R_{itoVCI} + R_{M1A} + R_{SWM1A} + R_{itoC11P} = 5 + 4.6 + 2.8 + 6.3 = 18.7\Omega$$

$$R_{PH1,3A\_SW2} = R_{itoC11N} + R_{SWM2A} + R_{M2A} + R_{itoDGND} = 6.3 + 6.2 + 2.5 + 5 = 20\Omega$$

$$R_{PH2A\_SW1} = R_{itoVCI} + R_{M3A} + R_{SWM3A} + R_{itoC11N} = 5 + 3.8 + 3.3 + 6.3 = 18.4\Omega$$

$$R_{PH2A\_SW2} = R_{itoC11P} + R_{SWM4A} + R_{M4A} = 6.3 + 2.3 + 4.2 = 12.8\Omega \quad (46)$$

$$R_{PH4A\_SW1} = R_{itoDGND} + R_{M5A} + R_{SWM5A} + R_{itoC11P} = 5 + 4.2 + 1.3 + 6.3 = 16.8\Omega$$

$$R_{PH4A\_SW2} = R_{itoC11N} + R_{SWM6A} + R_{M6A} = 6.3 + 4.9 + 6.2 = 17.4\Omega$$

$$R_{SWITCHING\_C11} = \frac{1}{f \cdot C_{11}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For C_{12},

$$R_{PH1,3B\_SW1} = R_{itoVCI} + R_{M1B} + R_{SWM1B} + R_{itoC12P} = 5 + 1.8 + 2.8 + 6.3 = 15.9\Omega$$

$$R_{PH1,3B\_SW2} = R_{itoC12N} + R_{SWM2B} + R_{M2B} + R_{itoDGND} = 6.3 + 6.2 + 3.2 + 5 = 20.7\Omega$$

$$R_{PH2B\_SW1} = R_{itoDGND} + R_{M5B} + R_{SWM5B} + R_{itoC12P} = 5 + 3.6 + 1.3 + 6.3 = 16.2\Omega \quad (47)$$

$$R_{PH2b\_SW2} = R_{itoC12N} + R_{SWM6B} + R_{M6B} = 6.3 + 4.9 + 1.8 = 13\Omega$$

$$R_{PH4B\_SW1} = R_{itoVCI} + R_{M3B} + R_{SWM3B} + R_{itoC12N} = 5 + 1.2 + 3.3 + 6.3 = 15.8\Omega$$

$$R_{PH4B\_SW2} = R_{itoC12P} + R_{SWM4B} + R_{M4B} = 6.3 + 2.3 + 1.3 = 9.9\Omega$$

$$R_{SWITCHING\_C12} = \frac{1}{f \cdot C_{12}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For the R_{OUT} of the dual side dual output voltage converter for DDVDH,

$$R_{OUT\_DDVDH\_dual\_output} = [0.5 \cdot (18.7 + 20) + 0.25 \cdot 4 \cdot (18.4 + 12.8)] + [0.5 \cdot (15.9 + 20.7) + 0.25 \cdot 4 \cdot (15.8 + 9.9)] + 25 // 25 + 6.3 // 6.3 = 110.2\Omega \quad (48)$$

Comparing to TABLE III, Eq. 48, the R_{OUT} of the dual side dual output voltage converter for DDVDH is much smaller than the output impedance specification of DDVDH ***$R_{OUT\_DDVDH\_MAX}$=150Ω***. That means the driving ability of the designed dual side dual output voltage converter for DDVDH can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side dual output voltage converter for DDVDH,

$$V_{RIPPLE\_DDVDH\_dual\_output} = 2m / (2 \cdot 20k \cdot 1u) = 50mV \quad (49)$$

Comparing to TABLE III, Eq. 49, the DDVDH output voltage ripple of the dual side dual output voltage converter is much smaller than the output voltage ripple specification 1V.

Output Loading for VCL Only

To simplify and to distinguish the difference of the performance of VCL between the conventional inverter and the proposed converter, we are going to discuss the output current loading occurring only at VCL. Let's review the output impedance R_{OUT} and the output voltage ripple of VCL of the dual side dual output voltage converter.

During the phase1 and phase3, both C_{11} and C_{12} are in the charging phase, being connected to V_{IN}. As in Fig. 45, the I_{OUT} output current of VCL is 2mA. During the phase1 and phase3, a current of I_{OUT} flows from the VCI pin through M_{1A}, C_{11} and M_{2A} to the DGND pin, and there is also a current of I_{OUT} flows from the VCI pin through M_{1B}, C_{12} and M_{2B} to

the DGND pin. There is always an rms current of I_{OUT} flowing through $R_{PH1,3A\_SW1}$ and $R_{PH1,3A\_SW2}$ for C_{11}, and $R_{PH1,3B\_SW1}$ and $R_{PH1,3B\_SW2}$ for C_{12}.

During the phase2, C_{11} is in the pumping phase, being connected to DDVDH, while C_{12} is in the pumping phase, being connected to VCL. A current of $2I_{OUT}$ flows from the VCI pin through M_{3A}, C_{11} and M_{4A} to the DDVDH pin, and there is also a current of $2I_{OUT}$ flows from the DGND pin through M_{5B}, C_{12} and M_{6B} to the VCL pin. There is always an rms current of $2I_{OUT}$ flowing through R_{PH2A_SW1} and R_{PH2A_SW2} for C_{11}, and R_{PH2B_SW1} and R_{PH2B_SW2} for C_{12}.

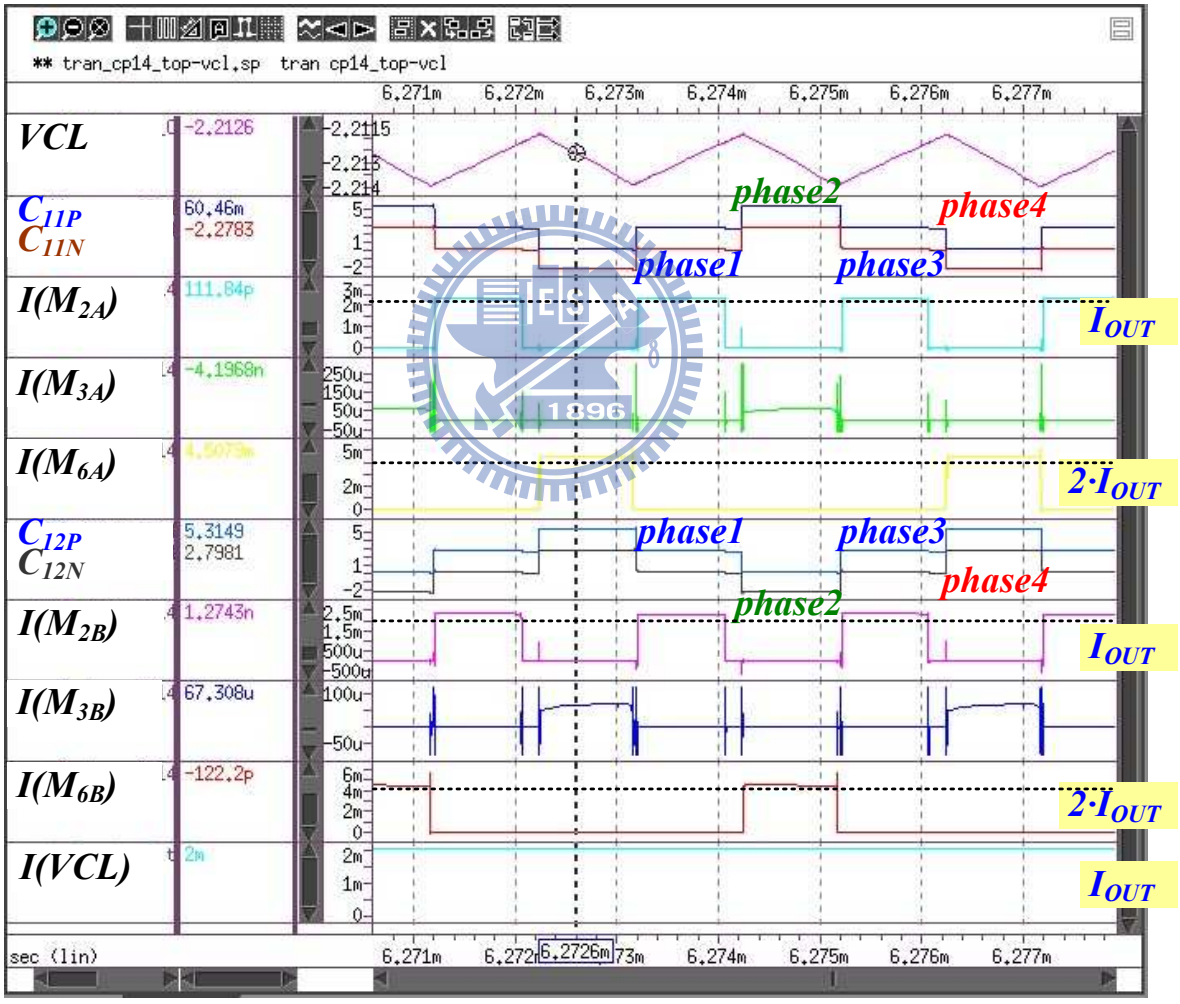


Fig. 45. Simulation Results of Dual Side Dual Output Voltage Converter: VCL only.

During the phase4, C_{11} is in the pumping phase, being connected to VCL, while C_{12} is in the pumping phase, being connected to DDVDH. A current of $2I_{OUT}$ flows from the DGND

pin through M_{5A}, C_{11} and M_{6A} to the VCL pin, and there is also a current of $2I_{OUT}$ flows from the VCI pin through M_{3B}, C_{12} and M_{4B} to the DDVDH pin. There is always an rms current of $2I_{OUT}$ flowing through R_{PH4A_SW1} and R_{PH4A_SW2} for C_{11}, and R_{PH4B_SW1} and R_{PH4B_SW2} for C_{12}.

Assuming the switching frequency is 40kHz. For C_{11},

$$R_{PH1,3A\_SW1} = R_{itoVCI} + R_{M1A} + R_{SWM1A} + R_{itoC11P} = 5 + 4.6 + 2.8 + 6.3 = 18.7\Omega$$

$$R_{PH1,3A\_SW2} = R_{itoC11N} + R_{SWM2A} + R_{M2A} + R_{itoDGND} = 6.3 + 6.2 + 2.5 + 5 = 20\Omega$$

$$R_{PH2A\_SW1} = R_{itoVCI} + R_{M3A} + R_{SWM3A} + R_{itoC11N} = 5 + 3.8 + 3.3 + 6.3 = 18.4\Omega$$

$$R_{PH2A\_SW2} = R_{itoC11P} + R_{SWM4A} + R_{M4A} = 6.3 + 2.3 + 4.2 = 12.8\Omega \quad (50)$$

$$R_{PH4A\_SW1} = R_{itoDGND} + R_{M5A} + R_{SWM5A} + R_{itoC11P} = 5 + 4.2 + 1.3 + 6.3 = 16.8\Omega$$

$$R_{PH4A\_SW2} = R_{itoC11N} + R_{SWM6A} + R_{M6A} = 6.3 + 4.9 + 6.2 = 17.4\Omega$$

$$R_{SWITCHING\_C11} = \frac{1}{f \cdot C_{11}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For C_{12},

$$R_{PH1,3B\_SW1} = R_{itoVCI} + R_{M1B} + R_{SWM1B} + R_{itoC12P} = 5 + 1.8 + 2.8 + 6.3 = 15.9\Omega$$

$$R_{PH1,3B\_SW2} = R_{itoC12N} + R_{SWM2B} + R_{M2B} + R_{itoDGND} = 6.3 + 6.2 + 3.2 + 5 = 20.7\Omega$$

$$R_{PH2B\_SW1} = R_{itoDGND} + R_{M5B} + R_{SWM5B} + R_{itoC12P} = 5 + 3.6 + 1.3 + 6.3 = 16.2\Omega$$

$$R_{PH2b\_SW2} = R_{itoC12N} + R_{SWM6B} + R_{M6B} = 6.3 + 4.9 + 1.8 = 13\Omega \quad (51)$$

$$R_{PH4B\_SW1} = R_{itoVCI} + R_{M3B} + R_{SWM3B} + R_{itoC12N} = 5 + 1.2 + 3.3 + 6.3 = 15.8\Omega$$

$$R_{PH4B\_SW2} = R_{itoC12P} + R_{SWM4B} + R_{M4B} = 6.3 + 2.3 + 1.3 = 9.9\Omega$$

$$R_{SWITCHING\_C12} = \frac{1}{f \cdot C_{12}} = \frac{1}{40k \cdot 1u} = 25\Omega$$

For the R_{OUT} of the dual side dual output voltage converter for VCL, from Eq. 46 and 47,

$$R_{OUT\_VCL\_dual\_output} = [0.5 \cdot (18.7 + 20) + 0.25 \cdot 4 \cdot (16.8 + 17.4)] + [0.5 \cdot (15.9 + 20.7) + 0.25 \cdot 4 \cdot (16.2 + 13)] + 25 // 25 + 6.3 // 6.3 = 116.7\Omega \quad (52)$$

Comparing to TABLE III, Eq. 52, the R_{OUT} of the dual side dual output voltage converter for VCL is much smaller than the output impedance specification of VCL $\boldsymbol{R_{OUT\_VCL\_MAX}=125\Omega}$. That means the driving ability of the designed dual side dual output voltage converter for VCL can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side dual output voltage converter for VCL,

$$V_{RIPPLE\_VCL\_dual\_output} = 1m/(2 \cdot 20k \cdot 1u) = 25mV \quad (53)$$

Comparing to TABLE III, Eq. 41, the VCL output voltage ripple of the dual side dual output voltage converter is much smaller than the output voltage ripple specification 1V.

3.2.2 Comparisons of Conventional and Proposed Voltage Converters

Table IV shows the performance comparisons of the conventional and the proposed voltage converters.

TABLE IV. PERFORMANCE COMPARISONS OF VOLTAGE CONVERTERS BY HAND CALCULATIONS

Hand Calculations		*Output Impedance*	*Output Voltage Ripple*
Conventional	***Doubler (DDVDH)***	***87.9 Ω***	***25mV***
	Inverter (VCL)	***85.65 Ω***	***12.5mV***
Proposed	***Doubler (DDVDH)***	***110.2 Ω***	***50mV***
	Inverter (VCL)	***116.7 Ω***	***25mV***

As we can see, although the DDVDH and VCL output impedances of the proposed dual side dual output voltage converter are larger than the conventional voltage doubler and the conventional voltage inverter, but the area, external components, pin outs of it gain more merits for the costs. And comparing to TABLE III, the output impedance and output voltage ripple of the conventional or the proposed voltage converters can meet the specifications of the TFT-LCD driver.

Table V shows the difference comparisons of the conventional and the proposed voltage converters. The new proposed dual side dual output voltage converter reduces 4 power switches, 4 pin outs and 2 flying capacitors. The proposed voltage converter is very suitable for lowering the costs of the TFT-LCD driver.

TABLE V. COMPARISONS OF VOLTAGE CONVERTERS

Voltage Converters		*Power Switches*	*Pin Outs*	*Flying Capacitors*
Conventional	***Doubler (DDVDH)***	***16***	***12***	***4***
	Inverter (VCL)			
Proposed	***Doubler (DDVDH)***	***12***	***8***	***2***
	Inverter (VCL)			

Chapter 4

Measurements of Switching Capacitor Voltage Converters in TFT-LCD Driver

In this chapter, measurements of the switching capacitor voltage converters that we mentioned in the last chapter will be presented. Section 4.1 shows the measurements of the conventional dual side voltage doubler that generates DDVDH for the TFT-LCD driver. Also in section 4.1 shows the measurements of the conventional dual side voltage inverter that generates VCL for the TFT-LCD driver. Section 4.2 shows the measurements of the new proposed dual side dual output voltage converter that generates DDVDH and VCL for the TFT-LCD driver. All the measurements include IC layout areas, waveforms, load regulations and voltage ripples.

The conventional dual side voltage doubler and dual side voltage inverter are fabricated with SilTerra 0.18um 1.8V/5V/32V CMOS 1P5M process. Fig. 46 shows the IC layout of the prior TFT-LCD driver with the total chip area equal to 19800*880um^2.

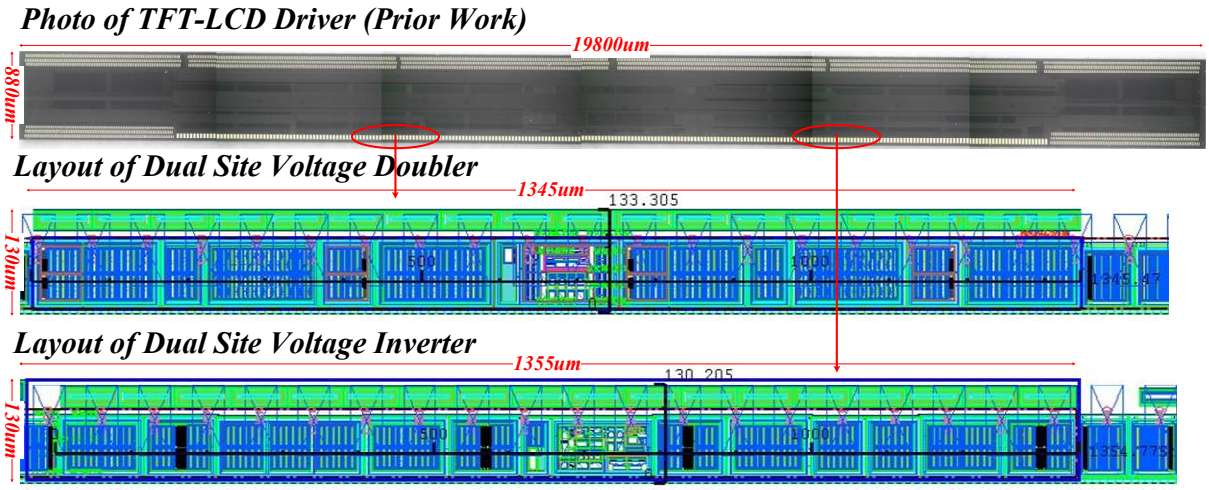


Fig. 46. Layout of the Conventional Voltage Doubler and Voltage Inverter.

The layout area of the dual side voltage doubler is 1345*130um^2. The layout area of the dual side voltage inverter is 1355*130um^2. As mentioned in section 3.1, the conventional dual side voltage doubler and the dual side voltage inverter use 16 power switches, 12 pin outs and 4 flying capacitors.

4.1 Conventional Voltage Converters

4.1.1 Dual Side Voltage Doubler

Fig. 47 shows the waveform of the conventional voltage doubler.

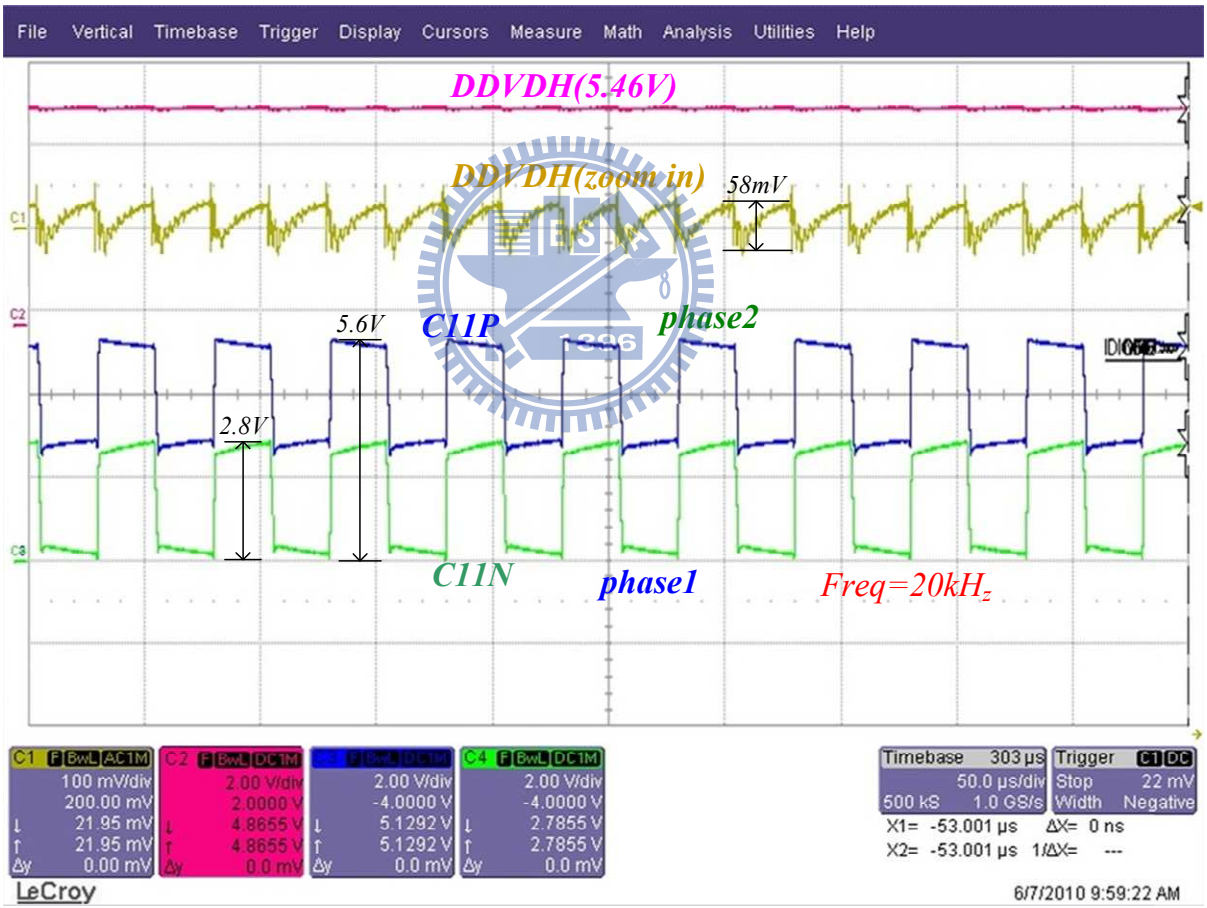


Fig. 47. Waveform Measurements of the Conventional Dual Side Voltage Doubler.

During the phase1, charging phase of C_{11}, C_{11P} is charged to VCI and C_{11N} is pulled to ground. During the phase2, pumping phase of C_{11}, C_{11P} is pumped to DDVDH and C_{11N} is

connected to VCI. The DDVDH zoom in waveform shows that DDVDH voltage is pumped whether in phase1 or phase2.

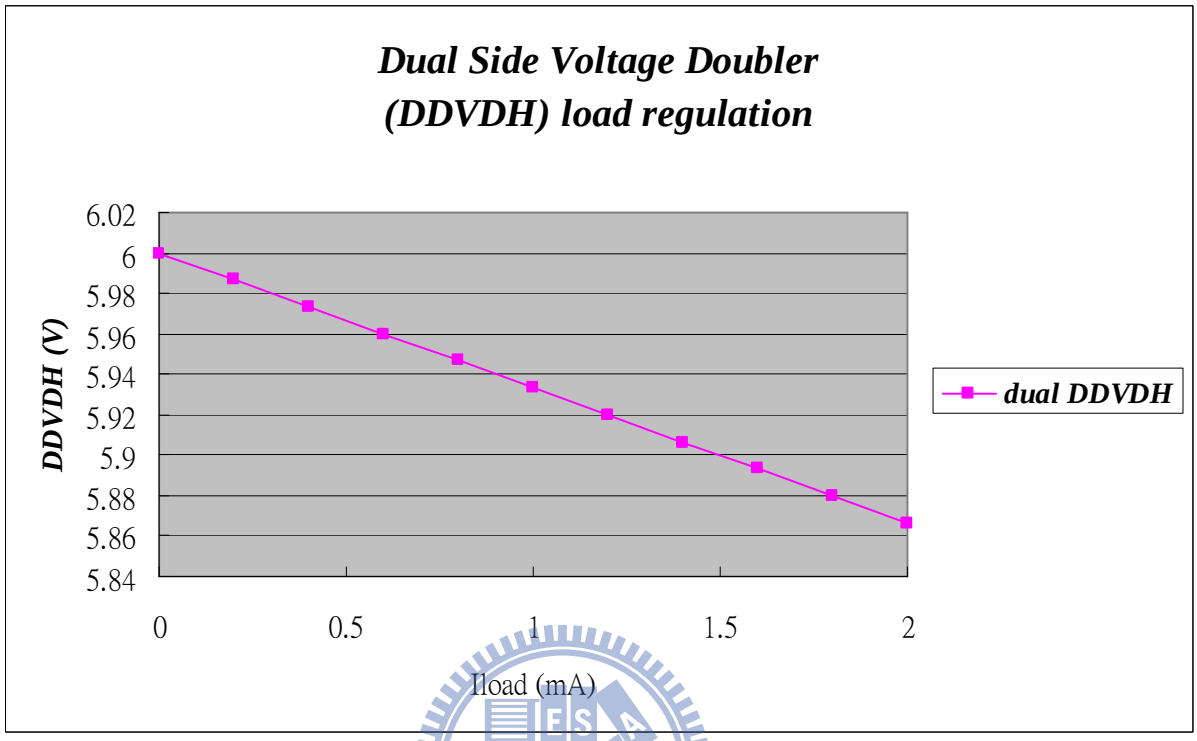


Fig. 48. DDVDH Load Regulation of the Conventional Dual Side Voltage Doubler.

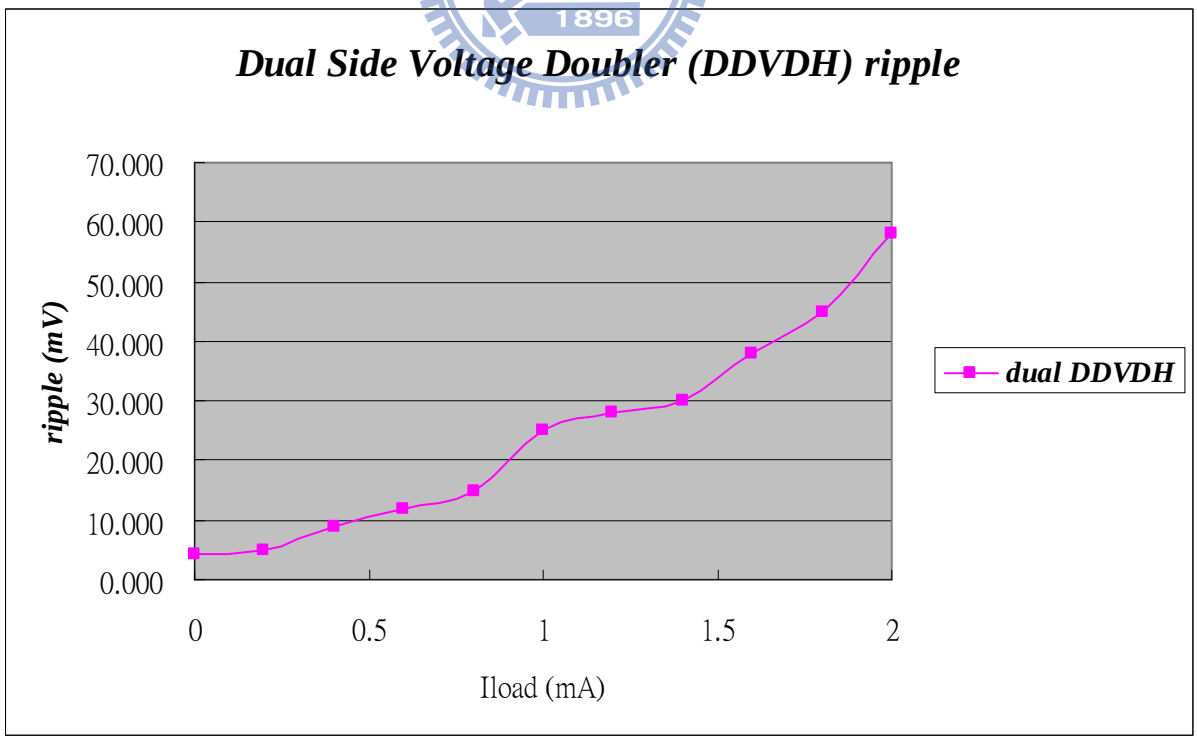


Fig. 49. DDVDH Voltage Ripple of the Conventional Dual Side Voltage Doubler.

Fig. 48 and 49 illustrates the load regulation and the voltage ripple of the conventional voltage doubler. We can figure out that

$$R_{OUT\_dual\_side\_doubler} = (5.9599 - 5.8797)V / (1.8 - 0.6)mA = 66.8\Omega \quad (54)$$

Comparing to TABLE III, Eq. 54, the R_{OUT} of the dual side voltage doubler is much smaller than the output impedance specification of DDVDH $\boldsymbol{R_{OUT\_DDVDH\_MAX}=150\Omega}$. That means the driving ability of the designed dual side voltage doubler can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side voltage doubler in Fig. 49, comparing to TABLE III, the output voltage ripple of the dual side voltage doubler is much smaller than the output voltage ripple specification 1V.

4.1.2 Dual Side Voltage Inverter

Fig. 50 shows the waveform of the conventional voltage inverter.

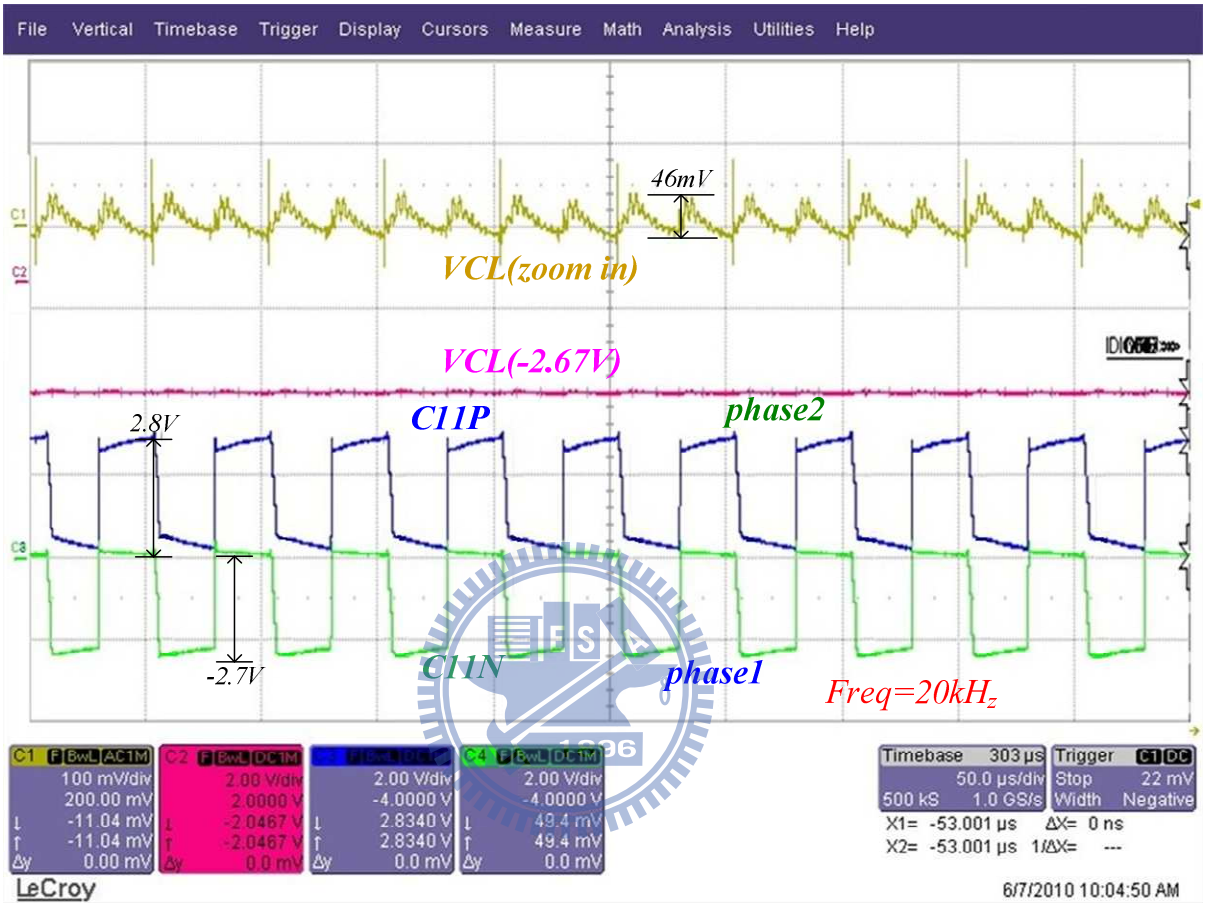


Fig. 50. Waveform Measurements of the Conventional Dual Side Voltage Inverter.

During the phase1, charging phase of C_{31}, C_{31P} is charged to VCI and C_{31N} is pulled to ground. During the phase2, pumping phase of C_{31}, C_{31P} is pulled to ground and C_{13N} is pumped to VCL. The VCL zoom in waveform shows that VCL voltage is pumped whether in phase1 or phase2.

Fig. 51 and 52 illustrates the load regulation and the voltage ripple of the conventional voltage inverter.

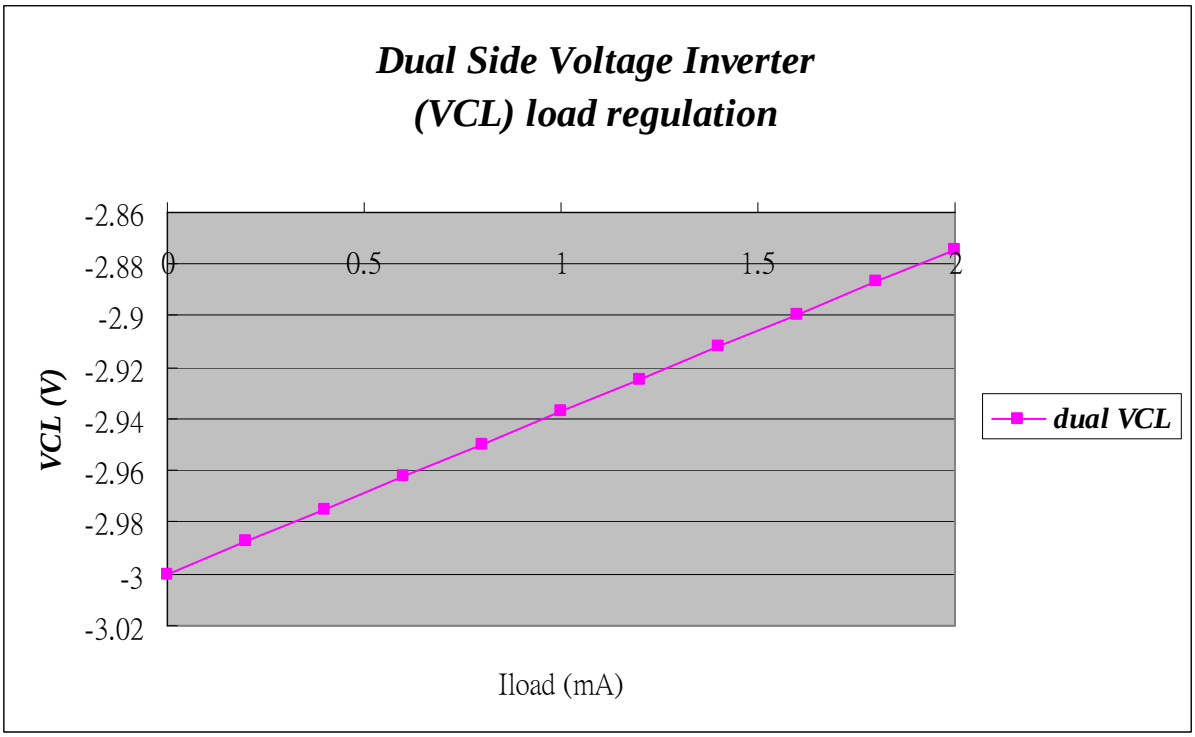


Fig. 51. VCL Load Regulation of the Conventional Dual Side Voltage Inverter.

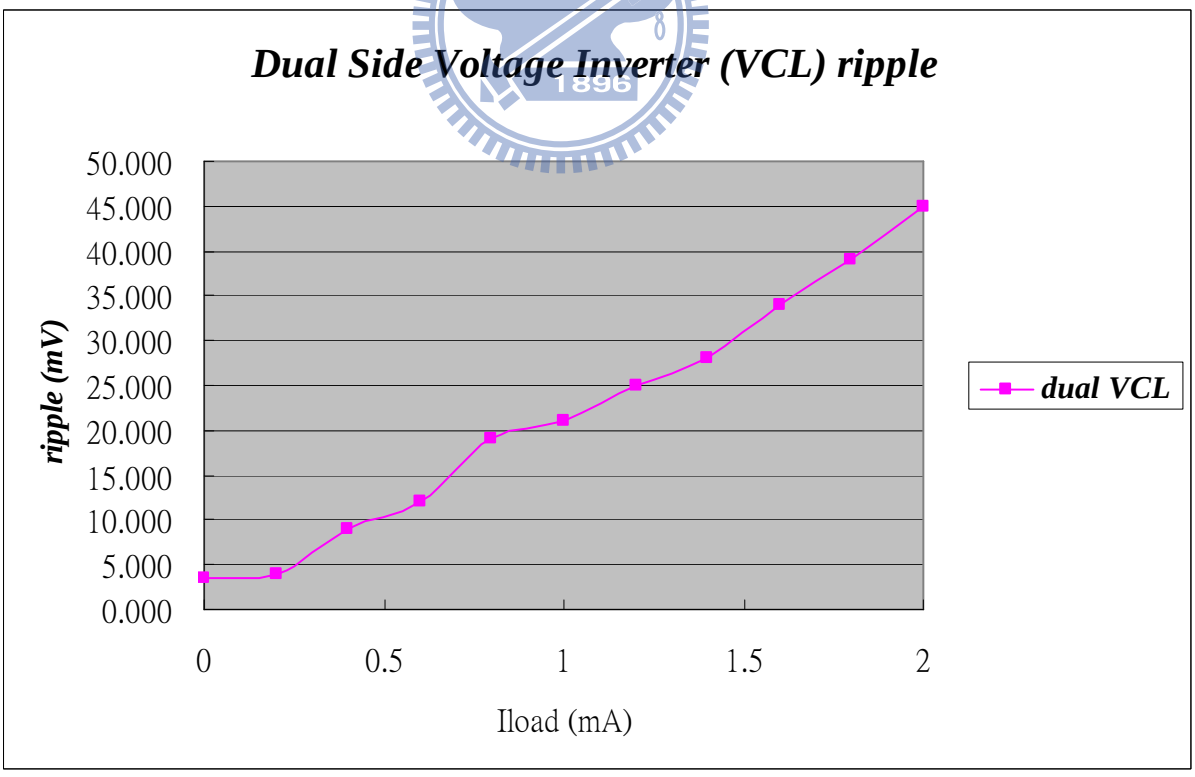


Fig. 52. VCL Voltage Ripple of the Conventional Dual Side Voltage Inverter.

In Fig. 51 and 52, we can figure out that

$$R_{OUT\_dual\_side\_inverter} = (-2.8868 + 2.9623)V/(1.8 - 0.6)mA = 62.9\Omega \quad (55)$$

Comparing to TABLE III, Eq. 55, the R_{OUT} of the dual side voltage inverter is much smaller than the output impedance specification of VCL $\boldsymbol{R_{OUT\_VCL\_MAX}=125\Omega}$. That means the driving ability of the designed dual side voltage inverter can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side voltage inverter in Fig. 52, comparing to TABLE III, the output voltage ripple of the dual side voltage inverter is much smaller than the output voltage ripple specification 1V.

4.2 New Proposed Voltage Converter

The new proposed dual side dual output voltage converter is fabricated with SilTerra 0.13um 1.8V/5V/32V CMOS 1P5M process. Fig. 53 shows the IC layout of the TFT-LCD driver with the total chip area equal to 16500*700um^2. The layout area of the dual side dual output voltage converter is 1955*130um^2. As mentioned in section 3.2, the new proposed dual side dual output voltage converter uses 12 power switches, 8 pin outs and 2 flying capacitors.

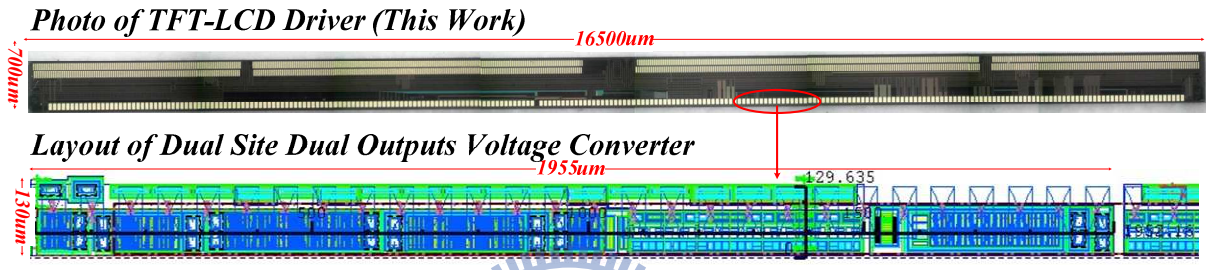


Fig. 53. Layout of the Proposed Dual Side Dual Output Voltage Converter.

Fig. 54 shows the waveform of the proposed dual side dual output voltage converter. During the phase1 and the phase3, the charging phase of C_{11}, C_{11P} is charged to VCI and C_{11N} is connected to ground. During the phase2, the pumping phase of C_{11}, C_{11P} is pumped to DDVDH and C_{11N} is connected to VCI. During the phase4, the pumping phase of C_{11}, C_{11P} is connected to ground and C_{11N} is pumped to VCL. The DDVDH and VCL zoom in waveforms shows that VCL voltage is pumped whether in phase2 or phase4 because of the dual side operation.

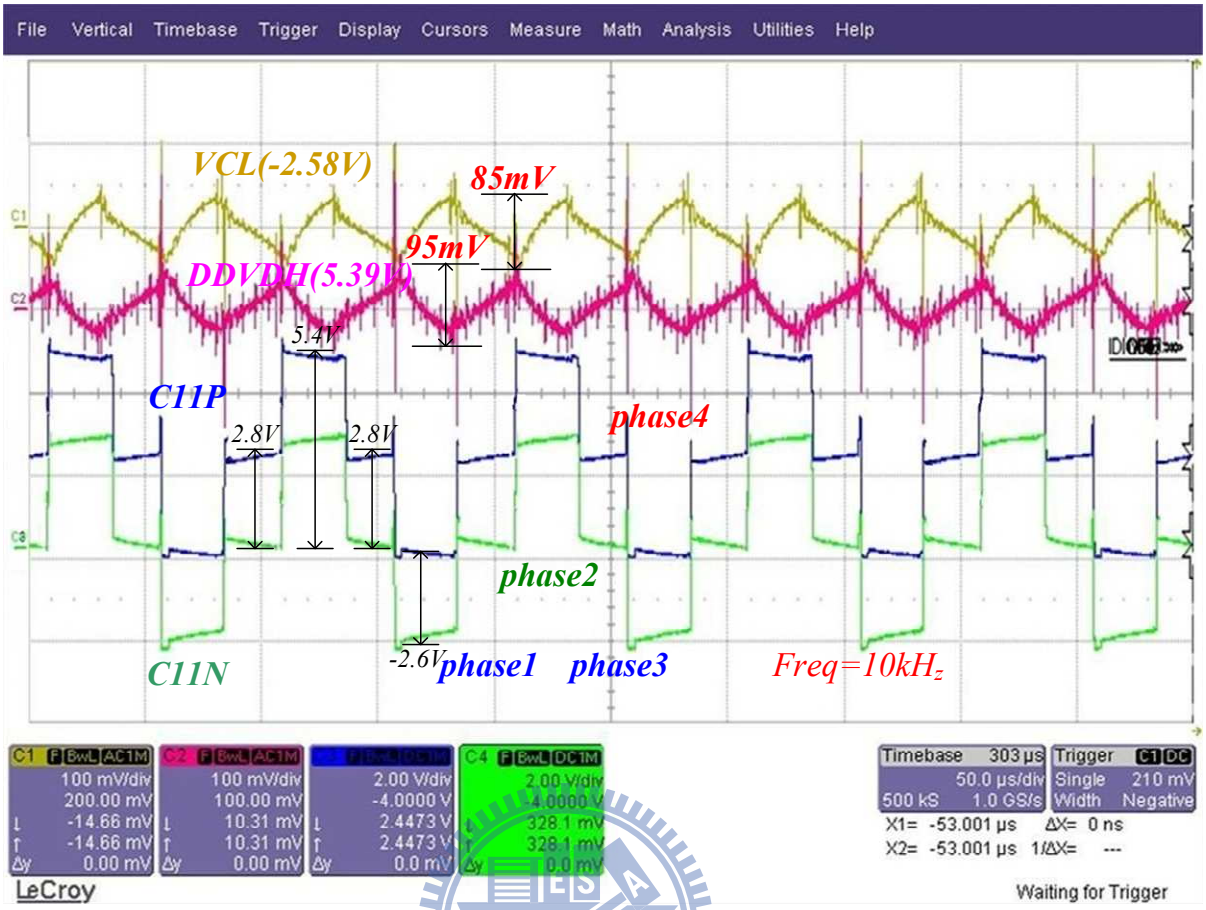


Fig. 54. Waveform Measurements of the Proposed Dual Side Dual Output Voltage Converter.

Table VI shows the IC layout area comparisons of conventional and proposed voltage converters. The total layout area of the dual side voltage doubler and the dual side voltage inverter is 351,000um^2 while the layout area of the proposed dual side dual output voltage converter is 254,150um^2. More than 27% layout area is reduced.

TABLE VI. IC LAYOUT AREA COMPARISONS OF VOLTAGE CONVERTERS.

		Area(um^2)	*Percentage (%)*
Convential	*Dual Side Voltage Doubler*	***130*1345***	***100***
	Dual Side Voltage Inverter	***130*1355***	
New Proposed Dual Side Dual Output Voltage Converter		***130*1955***	***72.41***

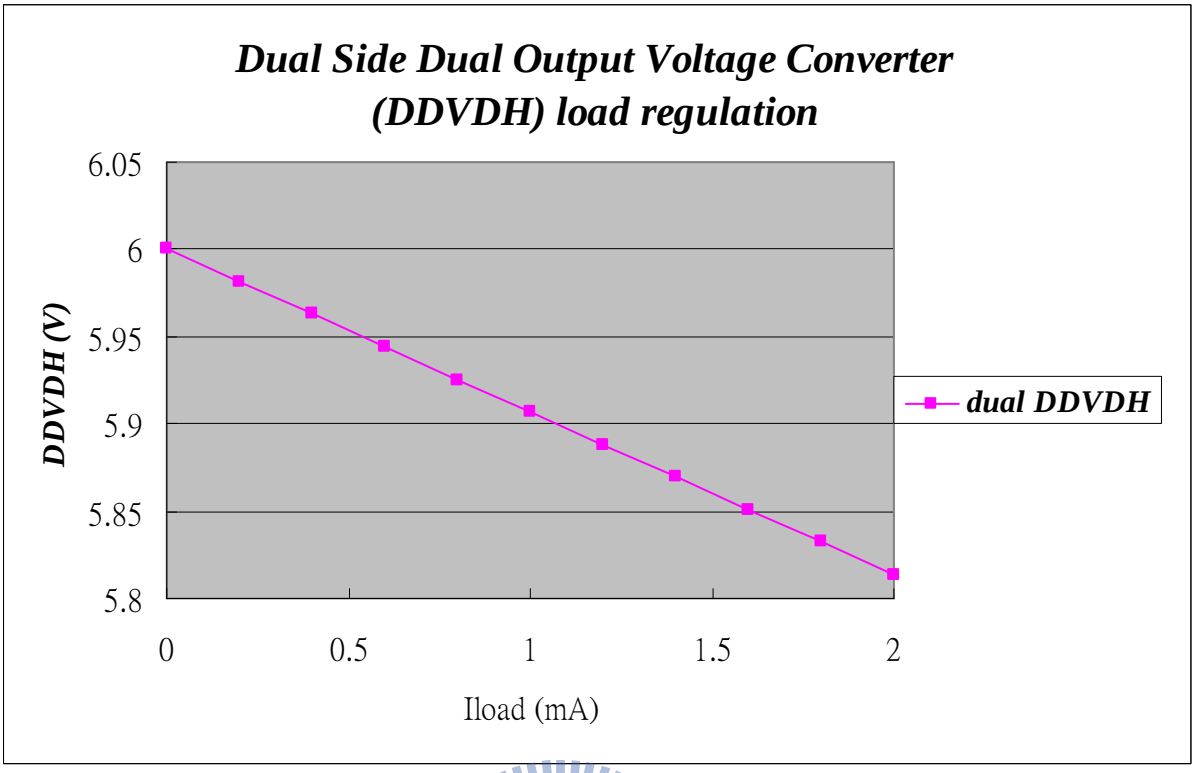


Fig. 55. DDVDH Load Regulation of the Proposed Voltage Converter.

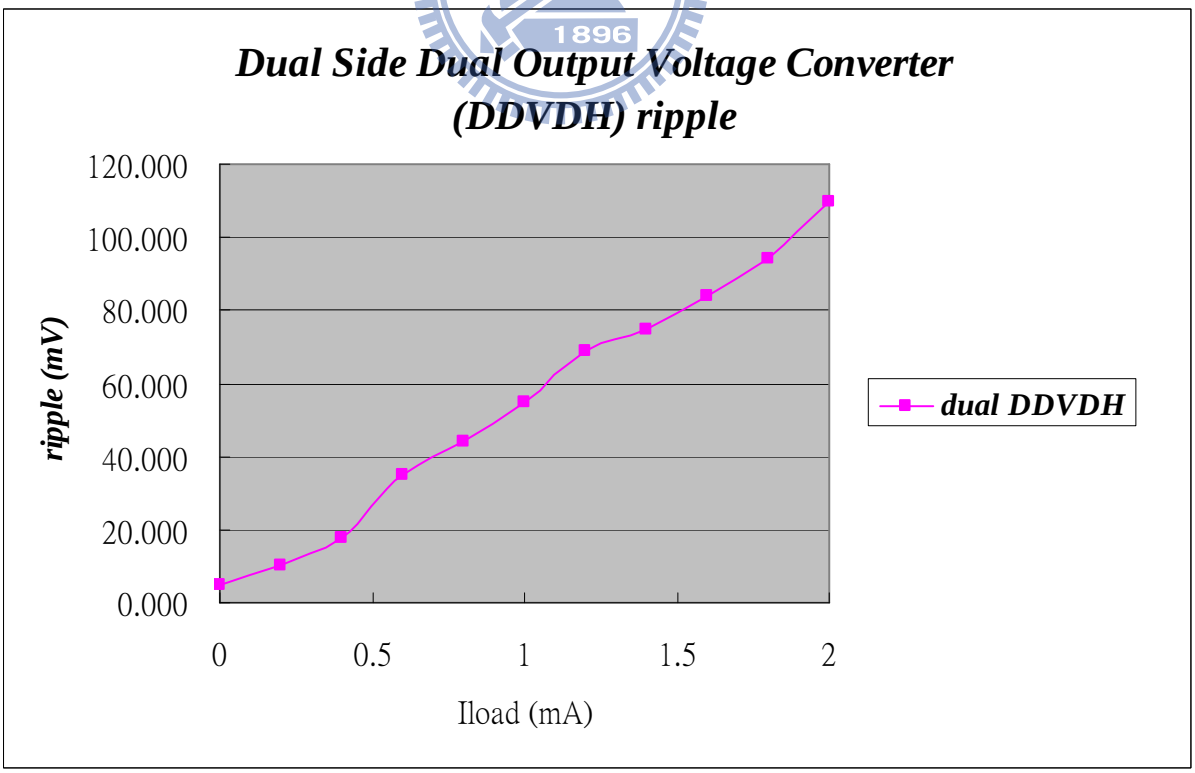


Fig. 56. DDVDH Voltage Ripple of the Proposed Voltage Converter.

Fig. 55 and 56 illustrates the load regulation and the voltage ripple of the proposed dual side dual output voltage converter for DDVDH. We can figure out that

$$R_{OUT\_DDVDH\_dual\_output} = (5.9411 - 5.8324)V / (1.8 - 0.6)mA = 93.08\Omega \quad (56)$$

Comparing to TABLE III, Eq. 56, the R_{OUT} of the dual side dual output voltage converter for DDVDH is much smaller than the output impedance specification of DDVDH $\boldsymbol{R_{OUT\_DDVDH\_MAX}=150\Omega}$. That means the driving ability of the designed dual side dual output voltage converter for DDVDH can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side dual output voltage converter for DDVDH in Fig. 56, comparing to TABLE III, the DDVDH output voltage ripple of the dual side dual output voltage converter equals to 110mV, and is much smaller than the output voltage ripple specification 1V.

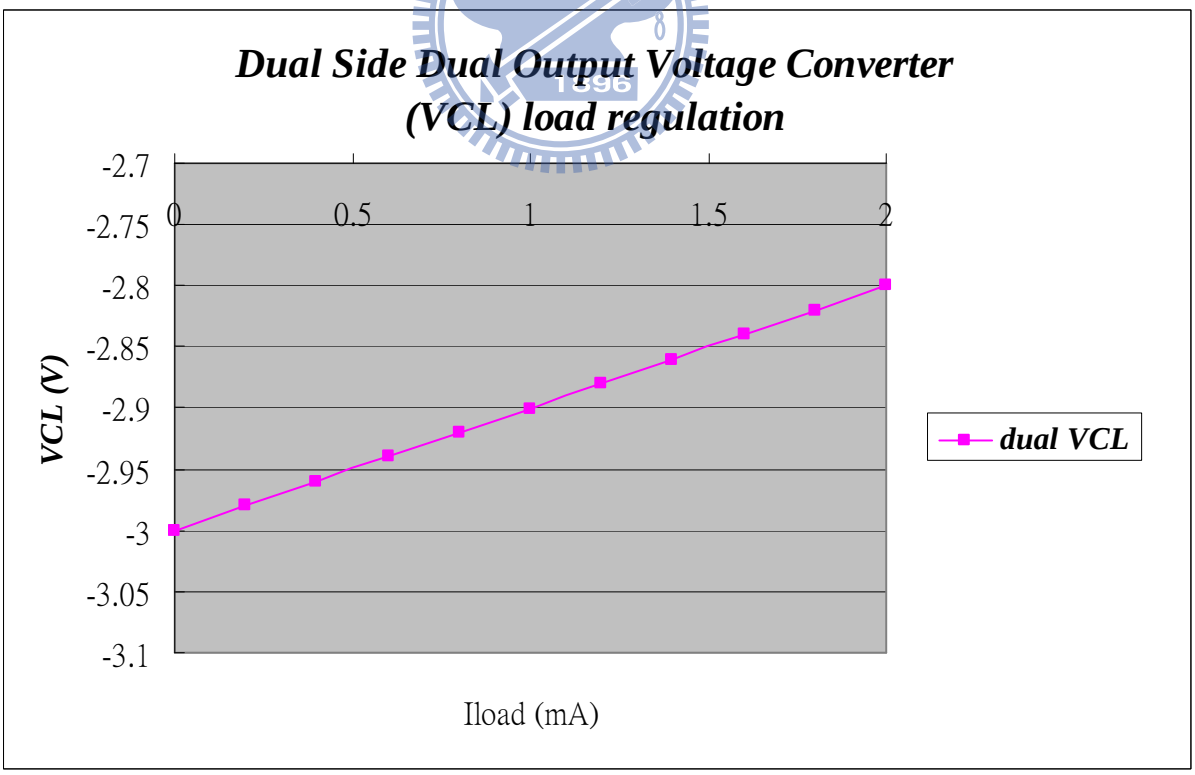


Fig. 57. VCL Load Regulation of the Proposed Voltage Converter.

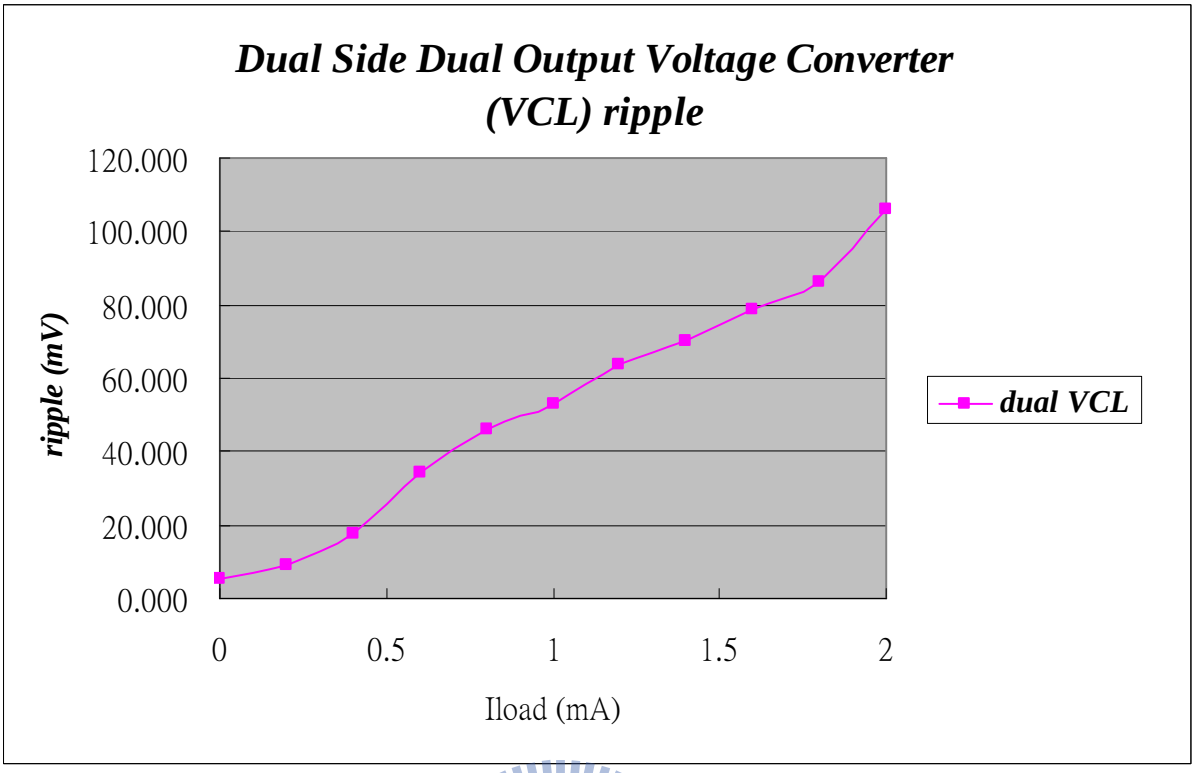


Fig. 58. VCL Voltage Ripple of the Proposed Voltage Converter.

Fig. 57 and 58 illustrates the load regulation and the voltage ripple of the proposed dual side dual output voltage converter for VCL. We can figure out that

$$R_{OUT\_VCL\_dual\_output} = (-2.8201 + 2.94)V / (1.8 - 0.6)mA = 99.92\Omega \quad (57)$$

Comparing to TABLE III, Eq. 57, the ROUT of the dual side dual output voltage doubler for VCL is much smaller than the output impedance specification of VCL $\boldsymbol{R_{OUT\_VCL\_MAX}=125\Omega}$. That means the driving ability of the designed dual side dual output voltage converter for VCL can meet the need of the TFT-LCD driver.

For the output voltage ripple of the dual side dual output voltage converter for VCL in Fig. 58, comparing to TABLE III, the VCL output voltage ripple of the dual side dual output voltage converter equals to 53mV, and is much smaller than the output voltage ripple specification 1V.

Table VII shows the performance comparisons of conventional and proposed voltage

converters by measurements. The performance of the new proposed dual side dual output voltage converter can meet the specifications of output impedance and output voltage ripple for DDVDH and VCL, and the IC layout area is minimized and more compact without sacrificing the display quality of the TFT-LCD panel. The proposed charge pump's DDVDH and VCL output impedances are larger than the conventional charge pumps. This means the efficiency of the proposed charge pump is lower than the conventional charge pumps.

TABLE VII. PERFORMANCE COMPARISONS OF VOLTAGE CONVERTERS BY MEASUREMENTS

Measurements		*Output Impedance*	*Output Voltage Ripple*
Specification	***Doubler (DDVDH)***	***150 Ω***	***1V***
	Inverter (VCL)	***125 Ω***	***1V***
Conventional	***Doubler (DDVDH)***	***66.8 Ω***	***58mV***
	Inverter (VCL)	***62.9 Ω***	***21mV***
Proposed	***Doubler (DDVDH)***	***93.08 Ω***	***110mV***
	Inverter (VCL)	***99.92 Ω***	***53mV***

The main reason of the new proposed charge pump is to find a good trade-off between the specification over-designed and the costs. From table V, VI and VII, the new proposed charge pump reduces over 27% IC layout area than the conventional charge pumps by reducing 4 power switches and 4 IC pin outs. And in the mean time, the proposed charge pump also reduces 2 external flying capacitors to lower the costs and making a smaller footprint area on the FPC.

Fig. 59 shows relationship between the DDVDH output impedance of the conventional and proposed charge pumps and the operation frequency. The DDVDH output impedance of

the proposed charge pump is higher than the conventional charge pump, but still lower than the maximum specification of 150Ω in the operation frequency range of 10kHz to 200kHz. The best operational frequency of the proposed charge pump is around 40kHz, because the minimum output impedance value occurs around this frequency. The highest efficiency of this charge pump is also occurs around the best operational frequency.

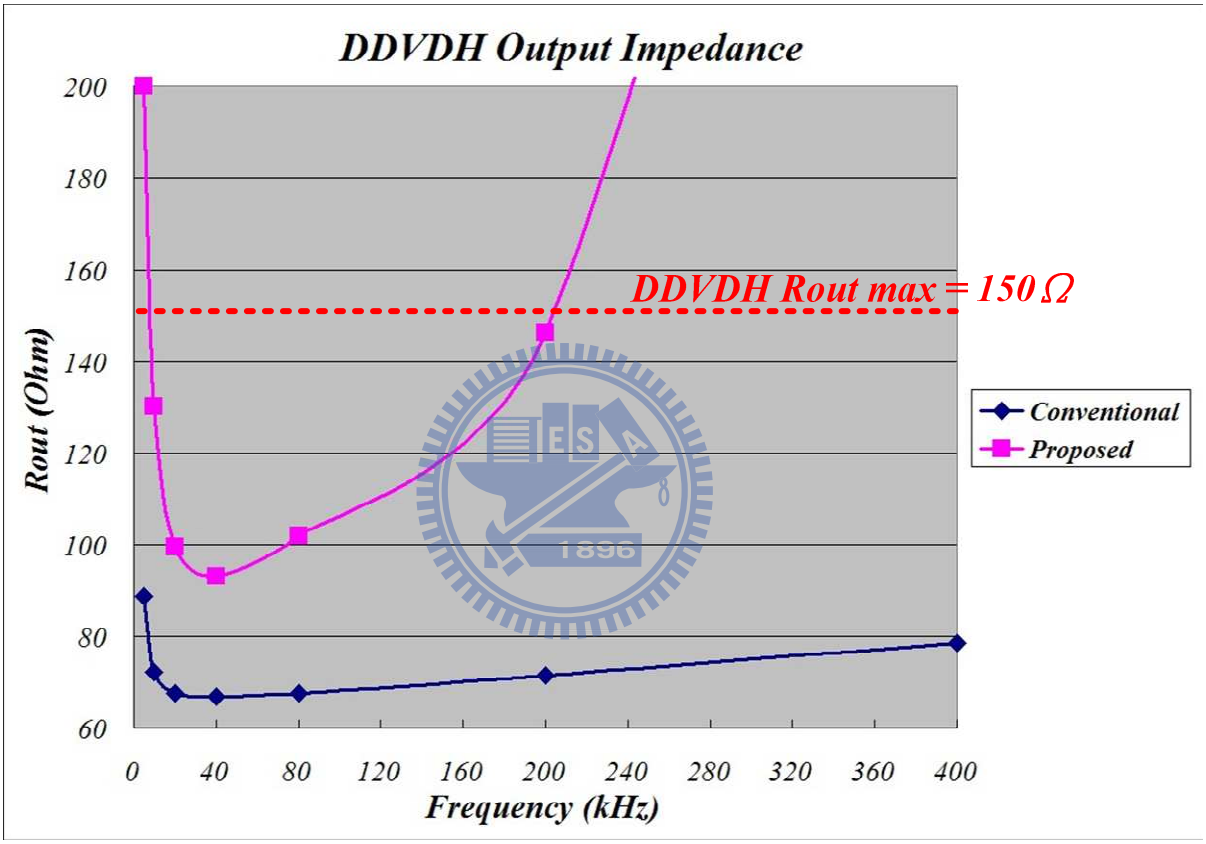


Fig. 59. DDVDH Output Impedance versus Operation Frequency

Fig. 60 shows relationship between the VCL output impedance of the conventional and proposed charge pumps and the operation frequency. The VCL output impedance of the proposed charge pump is higher than the conventional charge pump, but still lower than the maximum specification of 125Ω in the operation frequency range of 20kHz to 180kHz. The best operational frequency of the proposed charge pump is around 60kHz, because the minimum output impedance value occurs around this frequency. The highest efficiency of this

charge pump is also occurs around the best operational frequency.

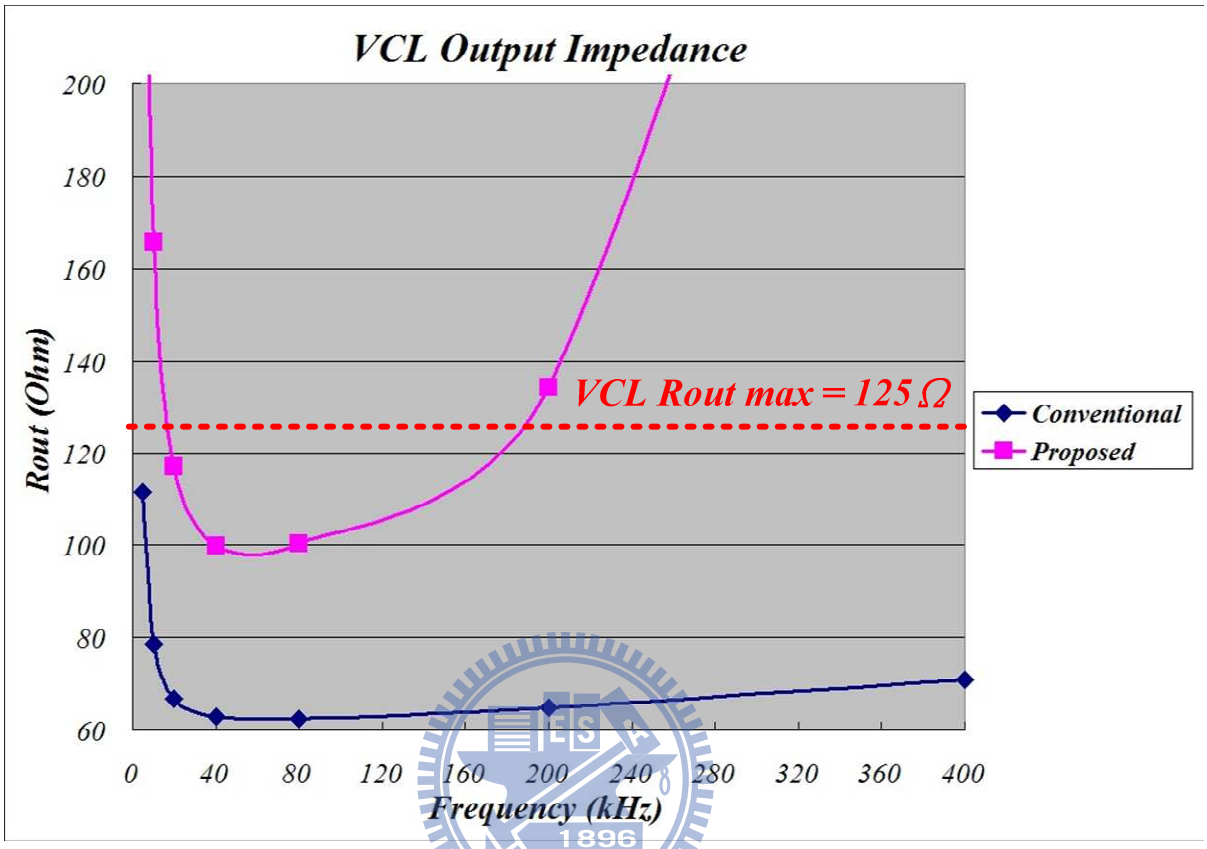


Fig. 60. VCL Output Impedance versus Operation Frequency

Fig. 61 illustrates the test board of the TFT-LCD module of this work. The driver IC is attached on the glass with the COG (chip on glass) method. The signals for the TFT-LCD panel come out from the driver IC through the ITO metal lines on the glass and go into the panel. And the signals from the baseband must go through the FPC. The external components needed for the driver IC are all placed on the FPC. The FPC is a flexible printed circuit that can be easy fabricated. The IC die size of the TFT-LCD driver is 16500x700um^2 and be fabricated with SilTerra 0.13um 1.8V/5V/32V CMOS 1P5M process The new proposed dual side dual output voltage converter occupies 130x1955um^2 layout area and works well within this driver IC in Fig. 61.

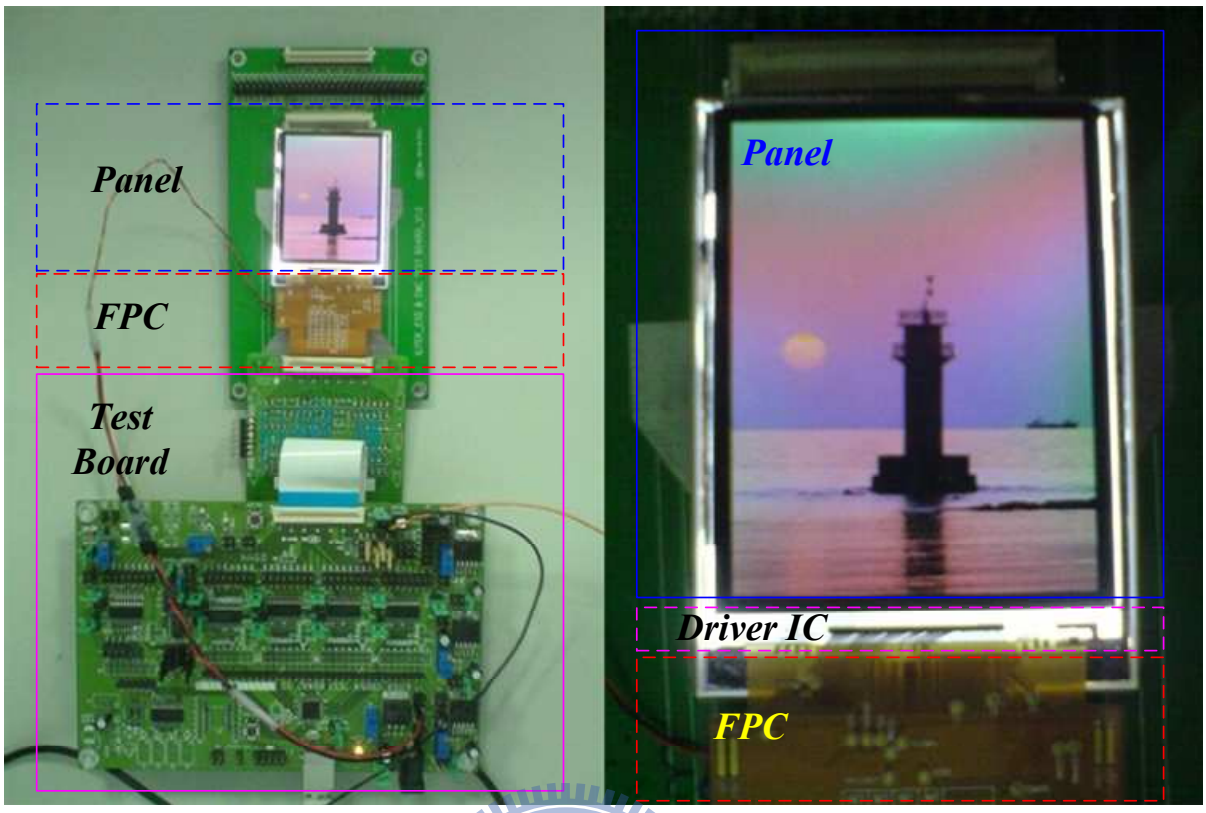


Fig. 61. TFT-LCD Test Board and TFT-LCD Panel Module

Chapter5

Conclusions and Future Work

5.1 Conclusions

In this thesis, the dual side dual output switching capacitor voltage converter is proposed, fabricated with SilTerra 0.13um 1.8V/5V/32V CMOS 1P5M process, measured and utilized in the TFT-LCD driver IC. Compared to the conventional dual side voltage doubler and the conventional dual side voltage inverter, the new proposed dual side dual output switching capacitor voltage converter reduces 4 power switches, 4 pin outs, 2 flying capacitors. This new voltage converter not only saves more than 27% layout area than the conventional voltage converters, but also reduces the cost of the external components. Besides that, the footprint area on the FPC can also be reduced. This new dual side dual output switching capacitor voltage converter works well without sacrificing the display quality of the TFT-LCD panel.

5.2 Future Work

With the tremendous competition, the cost down pressure of the TFT-LCD driver is very large. How to lower the cost further is an important issue.

From Table III, we can learned that the output impedance specifications of DDVDH and VCL are 150Ω and 125Ω separately.

In Table VII, the output impedances of DDVDH and VCL of the new proposed dual side dual output voltage converter are much smaller than those in Table III. That means we can still try to shrink the layout area of the new proposed dual side dual output voltage converter

further. We can also try to reduce the maximum current requirements of DDVDH and VCL by utilizing some new approaches [20] [21] [22] such as charge recycle and pre-charge or the line inversion-based method when driving the Source drivers and the VCOM driver. By doing so, we can not only shrink the area of the voltage converters that generate DDVDH and VCL but also increase the possibility of removing the external flying capacitors and stabilizing capacitors.

Reference

[1] C. T. Liu, “Revolution of the TFT LCD Technology,” *Journal of Display Technology*, Vol. 3, No. 4, December 2007.

[2] Ya-Hsiang Tai, “Design and Operation of TFT-LCD Panels,” *Wunan Publishers*, 2006.

[3] D. Maksimovic, “Power management model and implementation of power management ICs for next generation wireless applications,” *Tutorial presented at the International Conference on Circuits and System (ISCAS)*, 2002.

[4] G.A. Ricon-Mora and P.E. Allen, “A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator,” *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 33, No. 1, pp. 36-44, Jan. 1998.

[5] P. Favrat, P. Deval and M.J. Declercq, “A high-efficiency CMOS Voltage Doubler,” *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 33, No. 1, pp. 410-416, March 1998.

[6] J.A. Starzyk; Ying-Wei Jan; Fengjing Qiu, “A DC-DC Charge Pump Design Based on Voltage Doubler,” *IEEE Transactions On Circuits And Systems I: Fundamental Theory And Applications*, Vol. 48, No. 3, pp. 350-359, March 2001.

[7] Robert W. Erickson and Dragan Maksimovic, “Fundamentals of Power Electronics,” *2nd ed., Norwell, MA: Kluwer Academic Publishers*, 2001.

[8] Chi-Lin Chen, Wei-Lun Hsieh, Wei-Jen Lai, Ke-Horng Chen and Ching-Sung Wang, “A New PWM/PFM Control Technique for Improving Efficiency Over Wide Load Range,” *the 15th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 962-965, Sept. 2008.

[9] Hong-Wei Huang, Hsin-Hsin Ho, Chieh-Ching Chien, Ke-Horng Chen, Gin-Kou Ma, and Sy-Yen Kuo, “Dithering Skip Modulator with a Width Controller for Ultra-Wide-Load High-Efficiency DC-DC Converters,” *2006 IEEE Custom Integrated*

Circuits Conference (CICC), pp. 643-646, Sept. 2006.

[10] "Understanding Boost Power Stages in Switchmode Power Supplies," *Texas Instruments Incorporated, Dallas, TX*, March 1999.

[11] Chun-Yu Hsieh, Po-Chin Fan, and Ke-Horng Chen, "A Dual Phase Charge Pump with Compact Size," *the 14th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 202-205, Dec. 2007.

[12] G. Palumbo, and S. Pennisi, "Design Methodology and Advances in Nested-Miller Compensation," *IEEE Transactions on, Circuits System I: Fundamental Theory and Applications*, VOL. 49, pp. 893-903, Jul. 2002.

[13] B.G. Song, O.J. Kwon, I.K. Chang, H.J. Song, and K.D. Kwack, **"**A 1.8V Self-Biased Complementary Folded Cascode Amplifier,**"** *The First IEEE Asia Pacific Conference on, ASICs*, 1999. AP-ASIC '99.

[14] "LCD screens don't flicker – or do they?," *Application Note of Intersil Americas Incorporated*, September 26, 2005.

[15] J.K. Dicson, "On-Chip High Voltage Generation in NMOS Integrated Circuits Using An Improved Voltage Multiplier Technique," *IEEE Journal of Solid-State Circuits (JSSC)*, VOL. SC-11, pp. 374-378, June 1976.

[16] Chi-Chang Wang, and Jiin-Chuan Wu, "Efficiency Improvement In Charge Pump Circuits," *IEEE Journal of Solid-State Circuits (JSSC)*, VOL. 32, pp. 852-860, June 1997.

[17] Min-Hsin Huang, Po-Chin Fan, and Ke-Horng Chen, "Low-Ripple and Dual-Phase Charge Pump Circuit Regulated by Switched-Capacitor-Based Bandgap Reference," *IEEE Transactions on, Power Electronics*, Vol. 24, No. 5, pp. 1161-1172, May 2009.

[18] Walt Kester, Brian Erisman, and Gurjit Thandi, "Switched Capacitor Voltage Converters," *Analog Devices Incorporated*

[19] R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation," *2nd IEEE Press Series*

on Microelectronic Systems, 2005.

[20] Inseok Choi, Hojun Shim, and Naehyuck Chang, "Low-Power Color TFT LCD Display for Hand-Held Embedded Systems," *Proceedings of the 2002 International Symposium on, Lower Power Electronics and Design*, 2002. *ISLPED* '02

[21] Shao-Sheng Yang, Pao-Lin Guo, Tsin-Yuan Chang, and Jin-Hua Hong, "A Multi-Phase Charge-Sharing Technique without External Capacitor for Low-Power TFT-LCD Column Drivers," *Preceedings of the 2003 International Symposium on, Circuits and Systems, 2003. ISCAS '03*, Vol. 5, pp. 365-368, 2003.

[22] Jae-Hyuck Woo, Jae-Goo Lee, Young-Hyun Jun, and Bai-Sun Kong, "A Line Inversion-Based Stepwise Data Driving for Low-Power Mobile TFT-LCDs," *IEEE Transactions on, Consumer Electronics*, Vol. 56, Issue 2, pp. 1002-1009, May 2010.