

# 更小擺幅差動訊號傳輸模式之收發器

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## 摘要

本篇論文是設計一個應用於更小擺幅差動訊號傳輸模式之收發器，其中包含了傳送器以及擁有自動回復資料的接收器，這是一種使用很小擺幅的差動訊號（約 200mV）在兩個印刷電路板或是平衡的電纜線資料傳輸的方式，我們致力於設計此收發器能操作在 1.2Gbps，且此收發器是在台積電 0.35um2p4m 的製成下製造。

此傳送器是由虛隨機位元串列、八相位鎖相迴路、八對一多工器以及資料驅動器所組成，八相位鎖相迴路的輸入頻律為 75MHz，提供八個平均分佈在 150MHz 的相位，其中包含的電路有相位偵測器、電荷幫浦、迴路濾波器、壓控震盪器和一個除二的除頻器。此八相位的鎖相迴路產生的平均分佈時脈提供給八對一的多工器將一組並列資料轉換成串列資料，此傳送器再將此串列資料送至傳輸線上，此電路的總功率消耗為 128mW。

接收器是由一個擁有遲滯現象的比較器，三倍超取樣技術之追溯資料回復的系統所組成，其中利用比較器將小擺幅資料放大成完整擺幅資料，而追溯資料回復的系統是將資料做正確的取樣，最後此接受器會將序列資料再轉換成八個並列資料，總功率消耗為 960mW。

# **A Reduced Swing Differential Signaling (RSDS) Transceiver**

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## **Abstract**

The goal of this thesis is to design a CMOS transceiver, including a transmitter and a tracking data recovery receiver, which is based on the RSDS<sup>TM</sup> interface. RSDS stands for Reduced Swing Differential Signaling. It is a way to communicate data using a very low voltage swing (about 200mV) differentially over two printed circuit board (PCB) traces or a balanced cable. We have devoted to design a transceiver with the data rate at 1.2Gbps. And, the transceiver is fabricated in 0.35um 2P4M process.

Transmitter is composed of PRBS, eight-phases PLL, 8-to-1 multiplexer and data driver. The input reference of eight phases PLL is 75MHz; it outputs a uniformly distributed 150MHz clock. The PLL is composed of Phase Detector, Charge Pump, Loop Filter, Voltage Control Oscillator and a divided-by-two. Eight phases PLL output a uniform distributed clock for multiplexer to convert parallel data to serial data. The transmitter drives the serial data on to the bus. Total power is 128mW.

Receiver is composed of a comparator with hysteresis, tracking data recovery system with 3 times oversampling technique. It uses the comparator to amplify incoming small signal to full swing, and tracking data recovery system to sample data correctly. Finally, the receiver converts serial data to eight parallel data channel. Total power is 960mW.

# 致謝

首先，我要特別感謝我的指導教授吳錦川教授，在此先致上最誠摯的謝意，感謝在這兩年的碩士研究生涯中對我耐心指導以及叮嚀，並且在適當的時機下也會提供許多人生的經驗，讓我從中學到了做事精神與處事態度。當然還有要感謝我的口試委員，陳巍仁教授，呂良鴻教授，藍正豐學長的指導我以及很多中肯的建議。

其次我要感謝我的父母姊弟以及女朋友張婕伶，全力的在我背後支援我，才能夠使我專心一志的在研究所認真研究。還要感謝各位 307 實驗室的學長姐，同學，學弟妹們的支持鼓勵與指導，特別要感謝，左仲先學長、林子超學長、馬鳳飛學長、王文傑學長、蔡淑惠學姊、尤寶勳學長、陳相志學長、李柏儒學長、范姜朝馨學長在我碰到問題時皆能不吝給我指導，當然也感謝實驗室一起努力的各位同學，在我遇到瓶頸時給我鼓勵以及指導，特別感謝莊凱嵐、張瑋仁、林棋樺、周政賢、陳正瑞、黃如琳、林韋霆、蘇紀豪、陳旻琄，謝致遠、李宗霖、蕭聖文、丁彥、等等，另外還有我的好友們，明城、宜霖、宗苗、俊甫、老麥、庚釗、誠旭、右承、櫻峯、蕙茹、是方、昱璇，在此也祝福你們。另外還有可能有一時未想到的，總而言之，很感謝所有我認識的人以及關心我的朋友們，當然還有教授課業的老師們，若是少了你們任何一個人的出現，也許現在我就不能站在這裡了，最後，這論文之中也許會有疏忽謬誤之處，也請各位大德多多包含。

僅以此篇論文獻給所有關心我以及我關心的人。

2004/05/25 權哲

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