Chapter 1

Introduction

1.1 Motivation

Recently, for maximum performance, all high-speed components of a system have to be integrated into a single die. However, technological difficulties prevent the implementation of SOC(System-On-a-Chip). Therefore, it indicates such high-speed links will play a key role since the performance of many digital systems is limited by the interconnection bandwidth between different modules and chips. While high-speed transmission data rates are important to improve I/O performance, keeping the circuit area small and power consumption low are also important in order to be able to integrate transmitter and receiver into a single chip and to integrate protocol controllers on the same die [1].

The primary components of a data link are transmitter, receiver, and channel. The transmitter sends the data as analog quantities and converts digital bits into a data stream propagated on the channel to the receiver. The analog values are simply either a high-level or a low-level. In order to detect the logic level of an analog waveform in the presence of noise from the channel, the analog waveform at the receiving end has to be amplified and sampled. The receiver may also need an additional circuit, the timing recovery circuit, to resolve small inputs at very high rates correctly and reliably. Finally, transceivers must perform all of these duties while meeting specifications for delay, cost, data mapping, power consumption, and logic threshold variation, which contribute to skew.

The goal of this thesis is to design a CMOS serial link transceiver, including a transmitter and a tracking data recovery receiver, which is based on the RSDS™ interface. RSDS stands for Reduced Swing Differential Signaling. It is a way to communicate data using a very low voltage swing (about 200mV) differentially over two printed circuit board (PCB) traces or a balanced cable. The goal of this thesis is to design a transceiver with the data rate of 1.2Gbps.

1.2 Why RSDS?

1.2.1 The Trend of RSDS

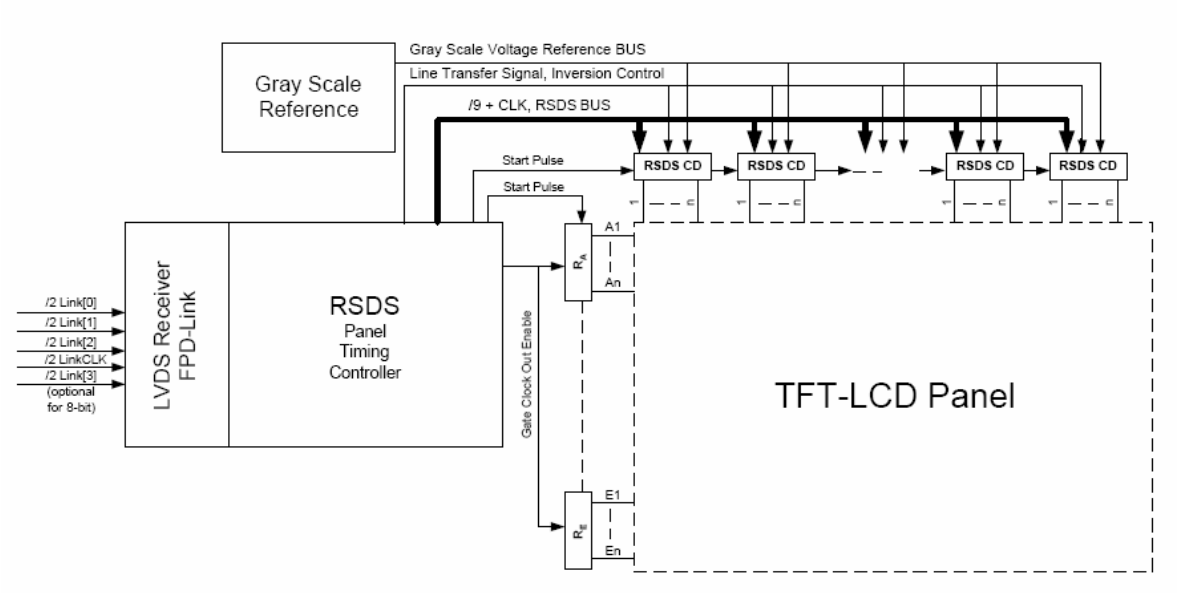


Fig.1-1 Block Diagram of the LCD Module [2]

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics and photo-realistic image data from camera to PCs and printers through LAN, and satellite systems to home set top boxes and digital VCRs. However, moving this data from board –to-board requires an extremely high-performance solution that must consume minimum

of power and generate less noise. Fig.1-1 illustrates a typical application block diagram of the LCD module. The RSDS^{TM} bus is located between the Panel Timing Controller (TCON) and the Column Drivers. This bus is typically nine pair wide plus clock and is a multidrop bus configuration [3].

1.2.2 RSDS Advantages

- **Current-mode, low-swing outputs, and high-speed differential design:**

  If RSDS current-mode, low-swing outputs, and high-speed differential design techniques are use, signal noise and electromagnetic interference (EMI) can also be reduced because of the low output voltage swing, relatively slow edge rates, and minimum I_{CC} spikes due to low current-mode operation [4]. And, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

- **Easy termination and saving power:**

  In order to prevent reflections, RSDS also requires a terminating resistor that is matched to the PCB traces differential impedance. This resistor is placed across the differential signal lines as close as possible to the receiver input. More importantly, the simplicity of the termination scheme is easy to implement in most applications. RSDS devices are also fabricated in CMOS processes, which provide low static power consumption. Because of low-swing outputs in the data driver, the I_{CC} does not exponentially as switching frequency is increased. The power consumed by the load is very small in magnitude.

- **Cost effective:**

  Because RSDS™ is a low noise producing, noise tolerant technology, power supply and EMI noise headaches are minimized. And, the transceiver based on RSDS™ can also be integrated around digital cores providing a higher level of integration. Here is summary of RSDS™ advantages [4].

Advantages	RSDS	PECL	Optics	TTL
Very low skew	o	o	o	X
Low dynamic power	o	X	o	X
Low noise/EMI	o	o	o	X
Simple termination	o	X	X	o
Process independent	o	X	o	o
Allows integration	o	X	X	o
High data rate (>1Gbps)	o	o	o	X
Cost effective	o	o	o	X
Single power supply	o	X	o	o
Wide common-mode range	X	o	o	X
Long distance transmission	X	o	o	X

Table.1-1 comparison with other data link technologies

1.2.3 RSDS/LVDS Applications

RSDS™ interface is similar to LVDS interface. The disparity between RSDS™ and LVDS is that RSDS has the lower signal swing of 200mV than LVDS. It can help reduce noise/EMI significantly and save money too. The chart below shows some applications based on RSDS/LVDS interface.

PC/Computing	**Telecom/Datacom**	**Consumer**
Flat panel displays	Switches	Home/office
Monitor link	Add/drop multiplexers	Set top boxes
System clustering	Box-to-Box	
Printer engine link	Routers	Game displays/controls
SCI processor interconnect	Hubs	In-flight entertainment

Table.1-2 RSDS/LVDS applications

1.3 Thesis Organization

This thesis is organized into seven chapters and Introduction is the first one. Chapter 2 introduces background including RSDS^{TM} specification and basic serial link design. In chapter 3, the Phase-Locked Loop architecture will be described to deal with system timing in this transceiver. The transmitter architecture is discussed in chapter 4 and simulation result is shown. In chapter 5, the building block of receiver and some simulation results are given. Chapter 6 not only gives the experimental results of PLL, transmitter, and receiver but also compared those with simulation result above. Finally, chapter 7 summaries this work and discusses the further development.

Chapter 2

Background

Chapter 2 presents an overview of the RSDS™ specification and main concepts about design. This chapter still has explained how it has high speed and low swing. Then the noise considerations are discussed in order to establish a low-noise environment. System timing also plays an important role in high-speed serial link design. Finally, some opinions are brought up for performance enhancement.

2.1 RSDS™ Specification [4]

2.1.1 Scope

Reduced Swing Differential Signaling (RSDS™) is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between flat panel timing controllers and column drivers. RSDS™ which is a differential interface with a nominal signal swing of 200mV tend to be used in display applications. It retains the many benefits of the LVDS interface commonly used between host and the panel for a high bandwidth, robust digital interface. The RSDS™ bus provides many benefits to the applications which include:

- Reduced bus width – enables smaller thinner column driver boards.
- Low power dissipation – extends system rum time.
- Low EMI generation – eliminates EMI suppression components and shielding.
- High noise rejection – maintains signal image.
- High throughput – enables high resolution display.

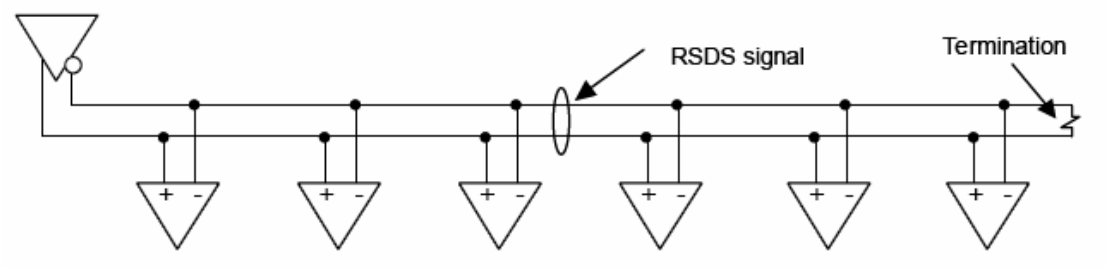


Fig.2-1 RSDS™ interface

2.1.2 Electrical Specification

An RSDS™ interface circuit is shown in figure 2-1. The circuit contains three parts: a transmitter (TX), receiver (RX), and balanced interconnecting medium with a termination. The transmitter and receiver are defined in terms of direct electrical measurements in Table 2-1.

TX/RX	Parameter	Definition	Condition	MIN	TYP	MAX	Units
TX	VOD	Differential output voltage	RL=100Ω	100	200	400	$\|mV\|$
TX	VOS	Offset voltage	VOD=200mV	1.1	1.3	1.5	*V*
TX	trise, tfall	Transition time	--	--	<2	--	*ns*
RX	VTH	Differential threshold	--	--	--	+/-100	*mV*
RX	VIN	Input voltage range	VID=200 mV	0.1	--	1.4	*V*
--	RT	Termination	--	95	100	105	*ohm*
--	Zo	Differential impedance of interconnect	--	90	100	110	*ohm*

Table.2-1 Electrical specifications of RSDS™ transmitters and receivers

2.1.3 Bus Configurations

The RSDS™ is a versatile interface that may be configured differently depending upon the end application requirements. Considerations include the location of the TCON, the resolution of the panel, and the color depth for example.

- Type 1 – Multidrop bus with double terminations.

In a Type 1 configuration, shown in Fig.2-2, the source is located in the middle of the bus via a short stub. The bus is terminated at both ends with a nominal termination of 100Ω. The interconnecting media is a balanced coupled pair with nominal differential impedance of 100Ω. In this application the RSDS™ driver will see a DC load of 50Ω instead of 100Ω. For this case, output driver of the RSDS™ driver must be adjusted to comply to the VOD specification with the 50Ω load presented by the Type 1 configuration.

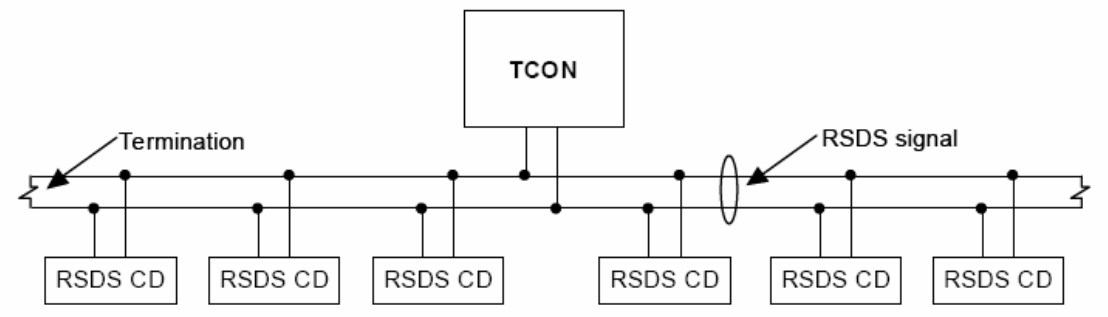


Fig.2-2 Type 1 bus configuration

- Type 2 – Multidrop bus with single end termination.

In a Type 2 configuration, shown in Fig.2-3, the source is located at one end of the bus. The bus is terminated at the far end with a nominal termination of 100Ω. The interconnecting media is a balanced coupled pair with nominal differential impedance of 100Ω. The bus may be a single or dual bus depending

upon the resolution of panel.

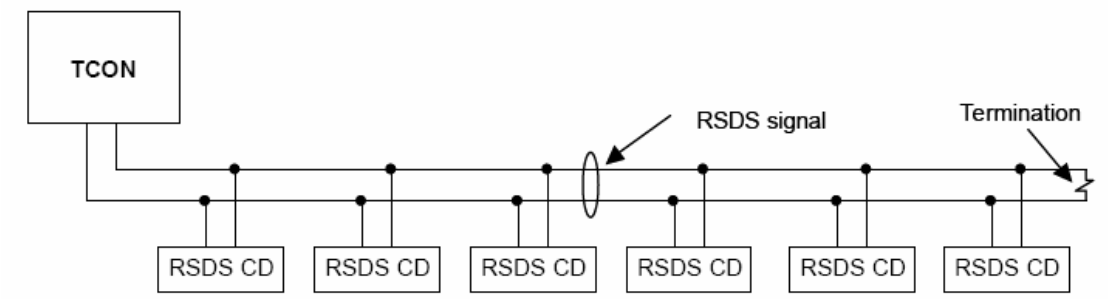


Fig.2-3 Type 2 bus configuration

- Type 3 – Double multidrop bus with single termination.

In a Type 3 configuration, shown in Fig.2-3, the source is located in the center of the application. There are two buses out of the TCON that run to the right and left respectively. Each bus is terminated at the far end with a nominal termination of 100Ω. The interconnecting media is a balanced coupled pair with nominal differential impedance of 100Ω. Note that the connection of the TCON to the main line is not a stub in this configuration, but rather is part of the main line. This helps to improve signal quality.

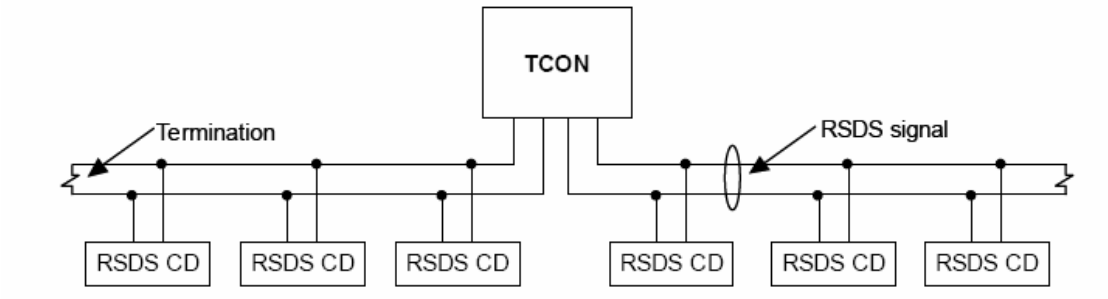


Fig.2-4 Type 3 bus configuration

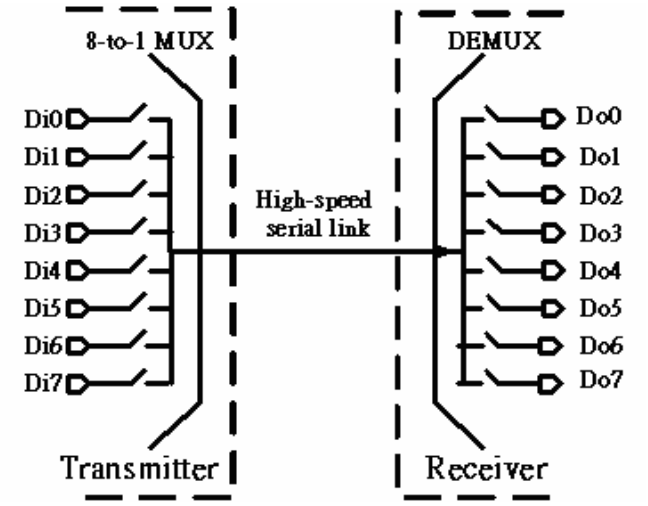


Fig.2-5 serial link using multiplexed transceiver

2.2 Basic Link Design Concept

As the demand for off-chip bandwidth grows with on-chip operating frequency, high bit-rate I/O pins become increasingly necessary for inter-chip signaling interfaces in VLSI systems. While it is always possible to increase off-chip bandwidth by making buses wider with more I/O pins, it is often impractical due to cost and limits in packaging technology. This suggests a chip design should efficiently utilize its existing I/O pins by driving them at higher bit rates [5]. The data before transmitted are usually parallel data stream in order to increase the bandwidth of the link. Therefore, a parallel to serial interface circuit is needed before sending to the transmitter. Fig.2-5 shows a typical high-speed link that multiplexes and demultiplexes data unto a serial bus. During a single cycle, all of the switches in the multiplexer are sequentially enabled and eight data bits (Di0~Di7) are transmitted on the serial bus. Similarly at the receiver, the switches in the demultiplexer sequentially sample the serial bus and decode all of the eight transmitted data bits (Do1~Do7) in a single on-chip cycle.

A typical high-speed link can be divided into two kinds, serial links and parallel links. Serial links extract the clock from the data, while parallel links use an explicit clock associated with a number of data pins. Because many of these parallel links need to be integrated into a single system, the overall overhead of the increased communication bandwidth is a dominate constraint. These constraints govern a simpler design for the transmitter and receiver circuit and lower bandwidth per communication channel. Generally speaking, in the serial link case, the transmitter and receiver chips use different clock sources that have the same nominal clock frequency. As a result, in order to lock both frequency and phase, the clock recovery circuit has to perform both frequency and phase detection. The most important design goal is to maximize the data rate across each link, and in some cases to extend the transmission range.

In addition to good understandings of transmitter and receiver, a great cognition of transmission line is essential to the design of high-speed circuits. A transmission line is an interconnect whose length is a significant fraction of the wavelength of interest or, equivalently, whose end-to-end delay is not negligible with respect to other time scales in the environment. Because many interconnects are dominated by long runs over unbroken ground planes, they can be accurately modeled as transmission lines, and much of signal integrity analysis is based on them. If a short length of a transmission line is considered, then the lumped approximation applies and the transmission line can be modeled with series inductance and resistance and with shunt capacitance and conductance, as shown in Fig.2-6.

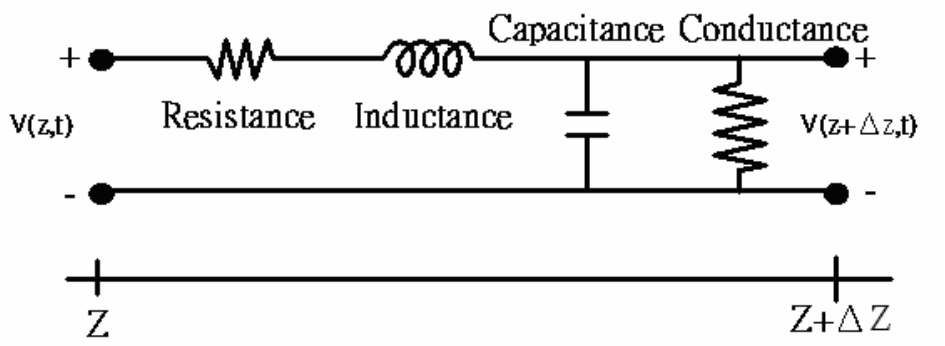


Fig.2-6 Lumped model of a short length of a transmission line

2.3 Noise Considerations

One key challenge for any high speed link is to overcome the noise present in the transmission medium, the packages, and the chips themselves, and still able to transmit and receive data at a fast rate. The noise must be minimized or cancelled by careful design. The study of noise is important because it represents a lower limit to the size of electrical signal that can be amplified by a circuit without significant deterioration in signal quality. Another motivation to study noise analysis is to learn basic concepts of random signals for a proper understanding of oversampling converters.

2.3.1 Noise Margins

Noise margins are usually defined by the signaling standard. Assume that the desired voltage levels for logic high and logic low are V_H and V_L, respectively. Also assume, for convenience of discussion, that $V_H > V_L$, although signaling could easily be worked the other way around. For logic high, the driver is specified to reach and exceed a minimum output voltage. Then the receiver must accept as logic high any

voltage above $V_{IH} < V_{OH}$ in order to communicate successfully. The noise margin is $NM_H = V_{OH} - V_{IH}$. On the other hand, for logic low, the driver is specified to fall and hold below a maximum output voltage. The receiver must accept as logic low any voltage below $V_{IL} > V_{OL}$, so the noise margin is $NM_L = V_{IL} – V_{OL}$. The logic family specifies how quickly the voltages must transition between valid logic levels. All digital signals are analog in nature fundamentally. If the ring back violates the signaling specification, additional time must be allowed so that the waveform can settle within the specification. Setting time reduces the maximum clock rate of the system.

2.3.2 Crosstalk

Crosstalk is the coupling of energy from one line to another. In parallel data channels, flux coupling to and from nearby signals due to mutual capacitance and mutual inductance leads to cross talk. The size of this cross talk depends largely in the signal layout geometry. And, the capacitance allows displacement current to cross the gap and inject into the victim line. Since the impedance is equal looking both ways up and down the line, the current splits equally and sends waves propagating in each direction. The coupling is showed in Fig.2-7, where capacitance is distributed along the length of two transmission lines. Once a crosstalk signal has been launched on the victim line, it can also create crosstalk back onto the aggressor line, where it can upset the waveform there and complicate further computations of crosstalk. When the secondary crosstalk is negligible, then the coupling is said to be weak. Otherwise, the coupling is strong. If the near-end is not properly terminated, the near-end crosstalk will also reflect and appear at the far-end of the line [6].

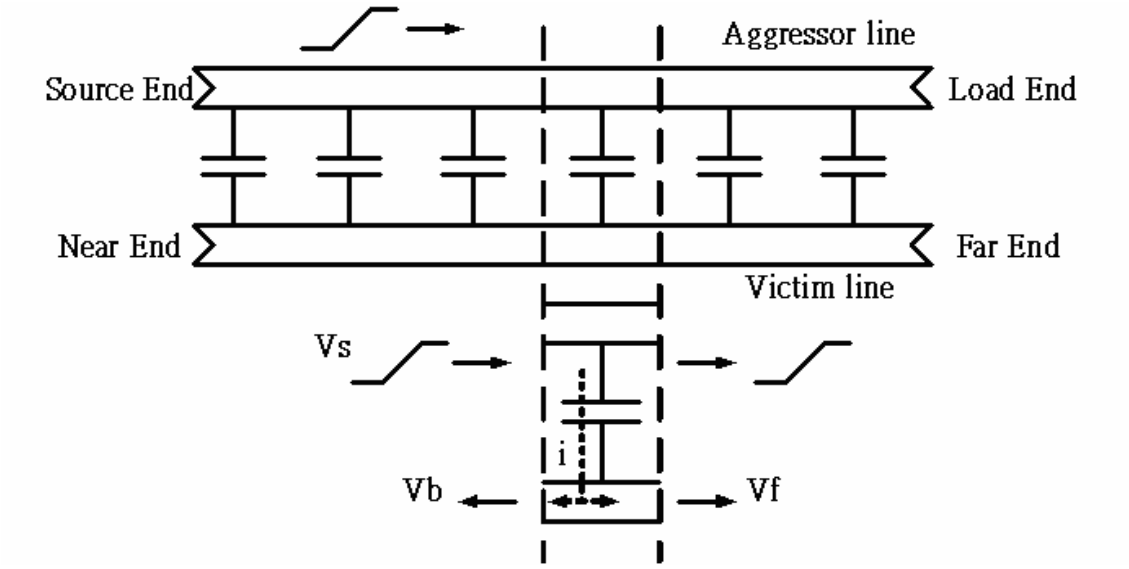


Fig.2-7 Sketch of capacitive coupling producing crosstalk

In order to reduce the effect of this reduced noise margin, conservative designs can minimize the interference by physically and electrically isolating the transmitted and received signals from other signals, and properly shielding the signal. But, constructive designs will separate sensitive signals from full-swing signals to minimize the capacitive coupling from signals with large ΔV. The far-end signal grows in amplitude with longer lines, while near-end noise grows in width with longer lines. The crosstalk noise is positive for low-to-high transitions and negative for high-to-low.

2.3.3 Intersymbol Interference

Intersymbol interference (ISI) sources are reflections of previous bits due to termination mismatches of impedance discontinuities in the channel and incomplete settling of the transmit signal within one bit time, which needs to be resolved at the circuit level by speeding up the transmit datapath or damping any ringing at the

transmit output. ISI is the most common type of systematic noise. In order to avoid reflections in a transmission line, signal lines need to be terminated. And, the termination circuit impedance absorbs the transmitted signal energy, and prevents it form being reflected back into the transmission line. The reflection of a signal is given by

$$V_{reflected} = \Gamma \cdot V_{incident} \quad \textbf{(2-1)}$$

Where Γ, the reflection coefficient, is related to Z_L, the load impedance at the reflection point, and Z_O, the characteristic impedance of the line, by

$$\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O} \quad \textbf{(2-2)}$$

Terminating both at the source and destination ends of the transmission medium can be used to alleviate this problem at the expense of increased power dissipation. Automatic impedance control can also be used to reduce reflection noise by dynamically adjusting the termination resistor to match the interconnection characteristic impedance [7]. Frequency-dependent attenuation also causes ISI. The unattenuated low-frequency component of the signal causes the isolated high-frequency pulse to barely reach the midpoint of the signal swing, given no eye opening.

2.3.4 Power Supply Noise and Switching Noise

Ideally, every signal should be provided with separate and isolated power and ground connections. Power noise, also called dI/dt noise, is induced by switching large current in short durations across the parasitic inductance in power distribution network. When the output signal switches, the current drawn from the external supply of the chip changes at a rate equal to dI/dt. The inductance L of the supply voltage

bonding wire will then cause the on-chip power supply voltage to drop by a voltage $\Delta V = L\frac{di}{dt}$. This drop of the voltage could be seen as a noise on both the switching and quiescent signal. In order to minimize this self-induced power supply noise, minimizing the power supply network inductance, and using a signaling method that draws constant current from the external supply are two good ways.

Shared ground and power pins enable coupling from the signal line to another. Because the power distribution inductance is small, the coupled noise is small if few drivers are switching at any given time. However, the level of coupled noise increases with the number of switching output, and when the whole bus is switching, the noise level can become excessive. For this reason, this noise mechanism is called simultaneous switching noise.

2.4 System Timing

2.4.1 Maximum Clock Rate

The maximum clock rate of a synchronous system is of primary interest, and the waveform in Fig.2-8 shows the major components that set the upper limit on the clock rate, including driver propagation delay (t_p), TOF on the interconnect, and the setup and hold times at the receiver. Assume that the data is sampled on next the rising clock edge, then before the next rising clock edge, it must satisfy

$$P > t_p + \mathrm{TOF} + t_s \qquad (2\text{-}3)$$

After the rising clock edge, it must satisfy

$$t_H < t_p + \text{TOF} \tag{2-4}$$

Normally, short driver delay is desired to help maximize the system clock frequency. However, for very short and fast interconnects, the TOF is very small and longer t_p may be needed to satisfy the receiver hold time. Or, the hold time must be reduced.

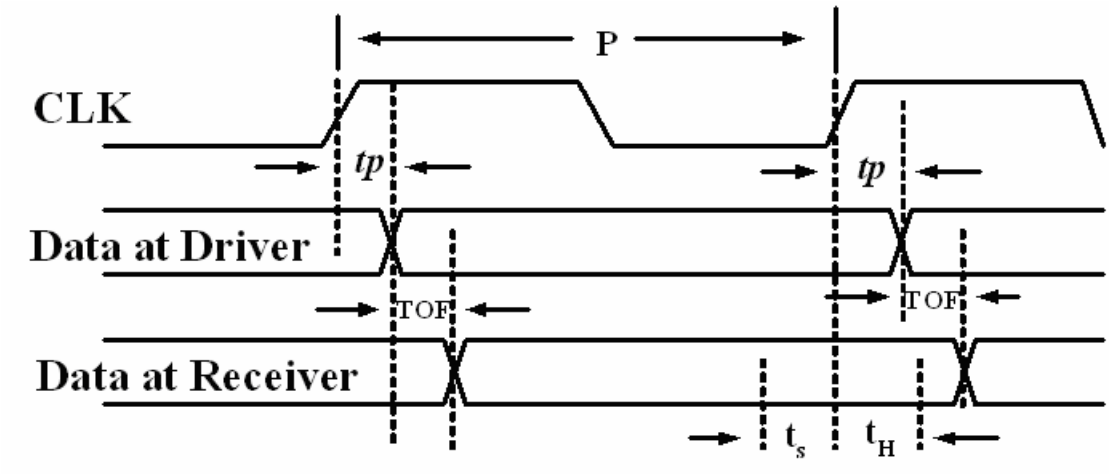


Fig.2-8 Timing diagram for determining maximum clock rate

2.4.2 Eye diagrams

Whether a long stream of bits or not, signaling specifications must be met for every signal at every clock. But it is difficult to tell if the signal meets the specifications, especially for a long stream of bits. In order to facilitate analyses, the bits can be superimposed to create a plot form which all of the signaling specifications can be checked. A good plot results when the waveform is plotted for one clock period before and after the edge, then the full data bits, plus half the one before and half one after, are captured. The eye diagrams for each line can be superimposed to

examine the signal specifications for the whole interconnect. One bit of data is often called a symbol. In a single stream of data, if the waveform of one bit is not completely settled by the time of the clock transition for the next bit, it will affect the shape of the following bit. Then this case leads to lower eye quality. When one symbol affects the next, intersymbol interference (ISI) is said to occur. In addition to limited circuit bandwidth, any imperfection that affects the magnitude or phase response of a system may result in intersymbol interference. Signal quality only really matters at receivers, where the signal is interpreted according to the logic specifications. Consider the representative eye diagram shown in Fig.2-9. The input specification is superimposed onto the eye diagram. Assuming that the signal is sampled at the clock edge, then the receiver specifications will be satisfied when t1 > t_s and t2 > t_H, the setup time and hold time.

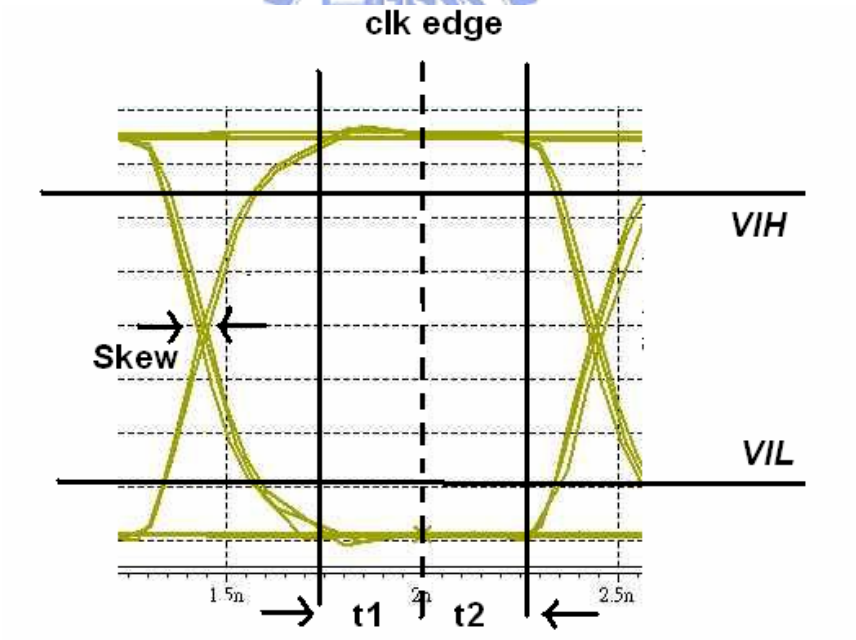


Fig.2-9 representative eye diagram

2.4.3 Data Skew, Clock Jitter, and Timing Margin

Refer to Fig.2-9, data edge falls along a range of times due to the influences of noise, crosstalk, TOF variations, and other effects. The uncertainty in the arrival time of a signal edge is the signal skew, and all sources of skew must be taken into account to ensure reliable operation of the system. If eye diagrams are not available, skew can be estimated from peak noise and the signal slew rate. In-phase noise pushed a waveform higher, so the rising edge arrives at the load earlier. Similarly, out-of-phase noise pushes a waveform lower for later arrival of rising edges. Therefore, additive noise directly causes skew in the timing of the rising and falling edges. There is a tradeoff between noise and timing skew. There is no benefit to reducing noise below a certain level because digital signaling operates with noise margins. Since lowering the noise through reduced edge rate pays a penalty in timing, an optimal system will utilize the fastest edge rates consistent with an acceptable noise level.

Clock generators inherently produce some variation in the timing of clock edges at their outputs, and this variation is called clock jitter. In a system driven by a single clock generator, all components see the same variation in the timing of the clock edge, so the timing budget is not directly affected by clock jitter. Jitter is also specified in terms of both short-term and long-term variations. Cycle-to-cycle jitter describes the short-term uncertainty of the period of a clock, while long-term jitter describes the uncertainty in the position of the clock with respect to the system clock source. In conventional digital design the most important requirement is minimizing cycle-to-cycle jitter. However, in high-speed links, both quantities can be equally important.

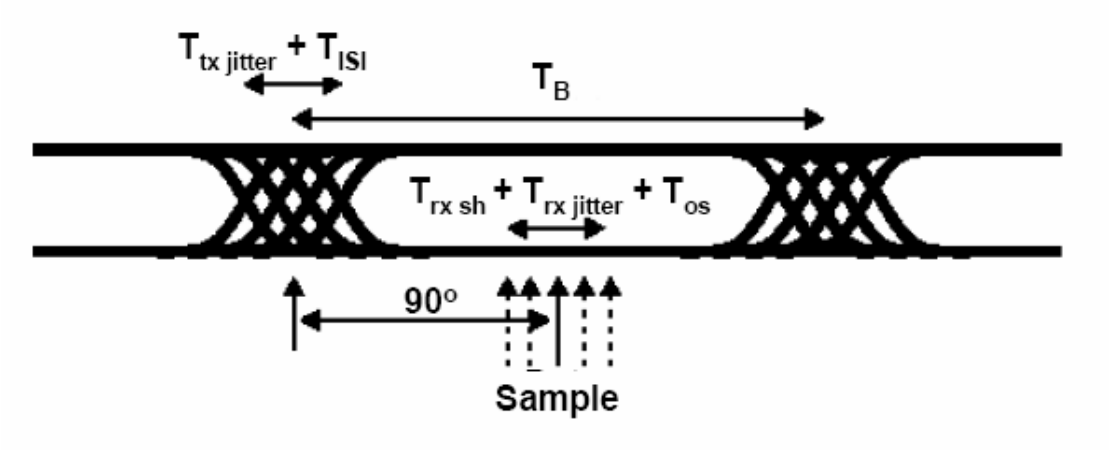


Fig.2-10 timing margin

Refer to Fig.2-10, the timing margin of the clocking scheme T_{margin}, which can be viewed as the tolerance to additional delay uncertainty, is given by:

$$T_{margin} = T_B - (T_{tx\ jitter} + T_{ISI}) - (T_{rx\ sh} + T_{rx\ jitter} + T_{OS}) \qquad (2\text{-}5)$$

Where T_B is the bit time, $T_{tx\ jitter}$ is the transmitter induced timing uncertainty and its clock jitter, which introduced by the noise on the transmitter chip. T_{ISI} is its intersymbol interference. $T_{rx\ sh}$ is setup and hold time of the sampler in the receiver. $T_{rx\ jitter}$ is the sampling clock jitter at the receiver clock generator. And. T_{os} is systematic clock skew deviates the average positions of the sampling points from the center of the data eye.

With ideal square pulses, as long as the sum of the magnitudes of the static and dynamic phase error is less than a bit-time, the sampled value will always be the correct bit. However, because of finite signal slew rate, timing errors that are less than a bit-time can reduce the amplitude of the signal at the sample point thus affecting the BER.

2.5 Tradeoffs for Performance Enhancement

In order to increase the performance of an interface system, the basic approach is to make changes that enable faster clocking, more processing, less noise, less power dissipation, and more data transfer per clock. A few of the factors at the disposal of the system designer are architectural tradeoffs. These issues must be balanced to achieve the required performance at a suitable cost within the allowed time frame and within regulatory limits on radiated electromagnetic emissions. Systems are best partitioned so that high performance can be achieved using high-speed interconnects. Another direct way to increase the information carrying capacity of interconnect is to simply make the bus wider of faster. Doubling the bus width gives an immediate doubling of the bus bandwidth. However, wider buses require more package pins and more PCB real estate, and the extra drivers use more silicon area, dissipate more power, and create more noise. High-speed circuit generate considerable levels of parasitic effects help block their access to the system level where electromagnetic interference (EMI) is more easily launched due to the larger circuit dimensions. High-speed circuits create a tradeoff between power supply ripple and EMI suppression. Bypass capacitance can help smooth the ripple and suppress EMI. Loading is the next most critical aspect regulating clock speeds on interconnects. Each input of a device adds capacitive loading to the net, so large numbers of devices result in large loadings and slow speeds due to RC charging times. Terminations can be used to dramatically enhance signal quality for higher speeds by dissipating unwanted reflections. The level of power dissipation can become a limiting factor in high-speed link design. Finally, differential signaling with terminated current-mode drivers can minimize the dependence of power dissipation on frequency. In contrast,

power dissipation for unterminated voltage-mode signaling increases linearly with frequency. For minimization of power dissipation, unterminated voltage-mode signaling is preferred at low frequency, while terminated current-mode signaling is preferred at high frequency. That is why RSDS interface is discussed in this thesis and employed in many applications.

Chapter 3

Phase-Locked Loop

3.1 Introduction

A phase-locked loop (PLL) is an analog building block used widely in many applications including analog, digital, and communication systems. For example, it can be used in demodulation of frequency-modulation signal. Another application area is frequency synthesizers used in televisions or wireless communication systems. And, it recovers clock and data from transmission signals at receiving end. These are a few of application areas. In this thesis, in order to produce the frequency and phase that the transceiver needs, the PLL circuit that synchronizes an output signal with a reference input signal is used necessarily. This chapter will introduce PLL with the 75 MHz input reference frequency which can form two different reference clock used in transmitter and receiver. In transmitter, it provides a 150 MHz frequency and generates eight clock phases to support the 8-to-1 multiplexer with four differential stages. In receiver, it provides a 600 MHz frequency and generates twelve clock phases to support the 12-to-1 phase selector with six differential stages.

3.2 Phase-Locked Loop Architecture

Fig.3-1 shows the block diagram of a typical PLL circuit that consists of a Phase-Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF), a Voltage-Controlled Oscillator (VCO), and a divided-by-N (Divider). In this thesis, the PLL output frequency must be twice as fast as input reference frequency, so a

divided-by-2 is used. The internal feedback signal, called f_{fb}, from the divider is compared to an external reference signal, called f_{ref}, by the phase detector that also generates error signals to charge pump. The phase detector develops output signal UP and DOWN that are proportional to the phase error. When charge pump receive the error signal, it will begin to charge or discharge loop filter to vary VCO output frequency via the control voltage change. This loop filter is typically a low pass filter used to filter out the high frequency component coming from the phase detector and charge pump. In such system, it is readily seen here that the phase-locked loop stays in lock because of the negative feedback of the loop in which the phase of the divider's output is subtracted form the phase of the input signal.

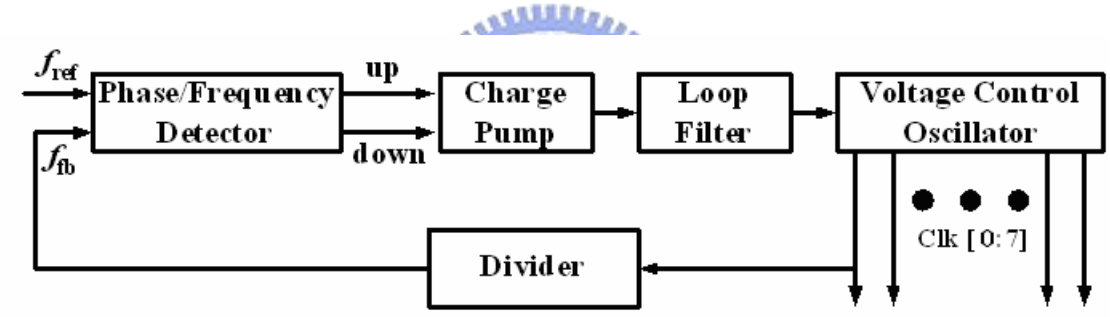


Fig.3-1 phase-locked loop architecture

3.3 Circuit Implementation

3.3.1 Phase Frequency Detector

The input phase errors between f_{fb} and f_{ref} are detected by phase detector. It is a logic circuit that generates two outputs, Up and Down, depending on its inputs, f_{fb} and f_{ref}.

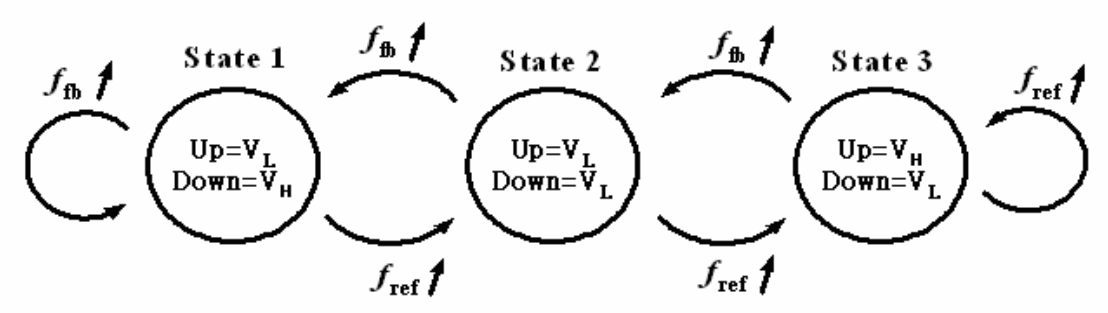


Fig.3-2 Phase detector tri-state diagram

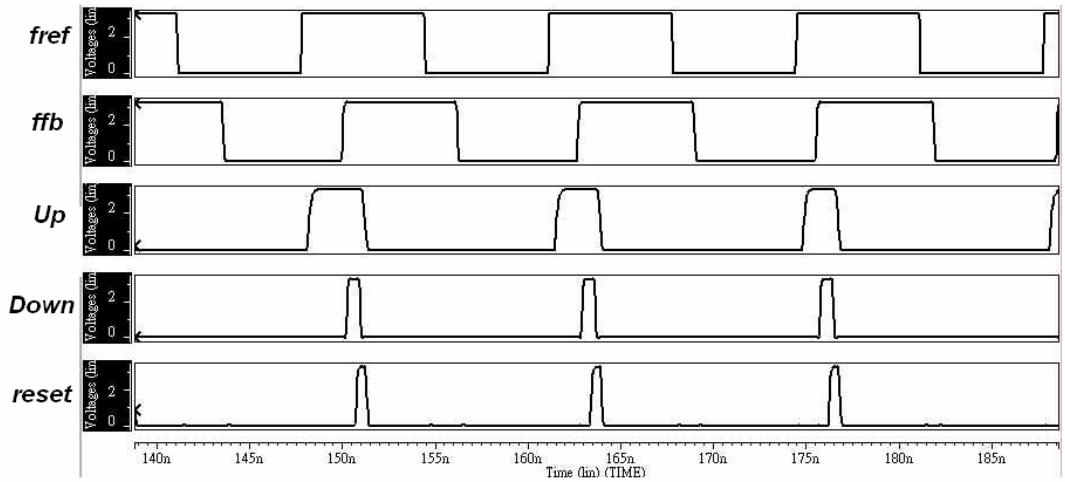


Fig.3-3 Reference signal comes before feedback signal

The phase detector creates three-state operation shown in Fig.3-2, while the state Up = Down = 1 never occurs. The two signals, Up and Down, signify how feedback signal should do. For example, shown in Fig.3-3, if reference signal leads feedback signal, Up will be set to high from low, and on the rising edge of feedback signal arrives, reset signal will be high to pull Up low. In contrast, if reference signal lags feedback signal, Down will be set to high from low, and at the arrival of the rising edge of reference signal, Down will be discharged. The three-state operation allows a wide range of detection for $\Delta\phi = \pm 2\pi$. It detects both phase error and frequency error.

Conventionally, the PFD can be implemented with two D flip-flops and one

NOR gate structure as shown in Fig.3-4. The TSPC D flip-flop implementation of PFD is showed in Fig.3-5 [8].One of the contribution to the output jitter is due to the dead zone (range of phase difference where no PFD output is generated) of the PFD in equilibrium [9]. Its characteristic curve with dead zone is shown in Fig.3-6. Because it allows the VCO to accumulate as much random phase error as the extent of the dead zone while receiving no corrective feedback to change the control voltage. Dead zone occurs when the loop is in a lock mode and the output of the charge pump does not charge for small changes in input signals at the phase detector. In order to eliminate the dead zone, the extra delay is added in the reset path. Seeing Fig.3-4, although the phase difference is really small, Up or Down has enough time to turn on the next stage of charge pump by adding this delay cell. But the PFD will have limit on the maximum operation frequency that is in inverse proportion to total reset path delay [10]. From [10], the maximum operation frequency is given by $f\max = 1/2\Delta R$, where ΔR is total delay of the reset path through the delay cells. In addition to dead zone, the PFD has an offset as a result of the loading mismatches between Up and Down pulse.

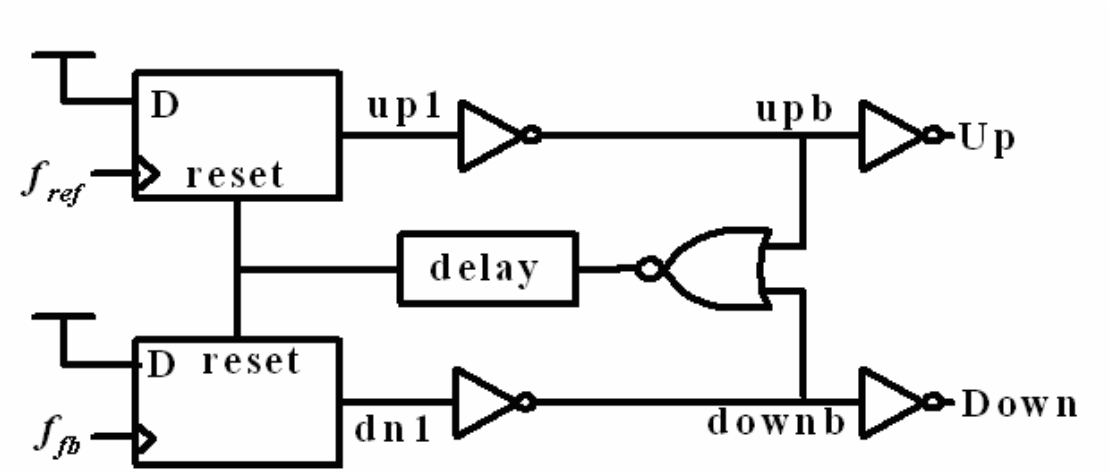


Fig.3-4 Block Scheme of PFD

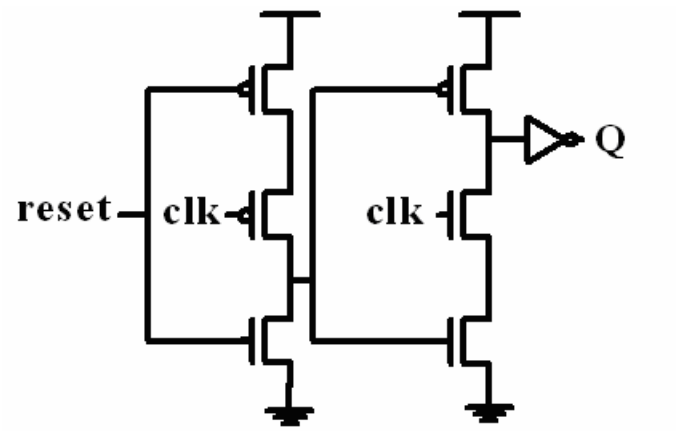


Fig.3-5 TSPC Dynamic D Flip-Flop

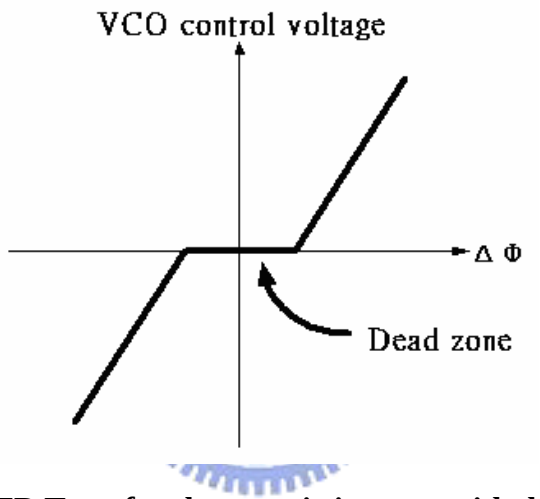


Fig.3-6 PFD Transfer characteristic curve with dead zone

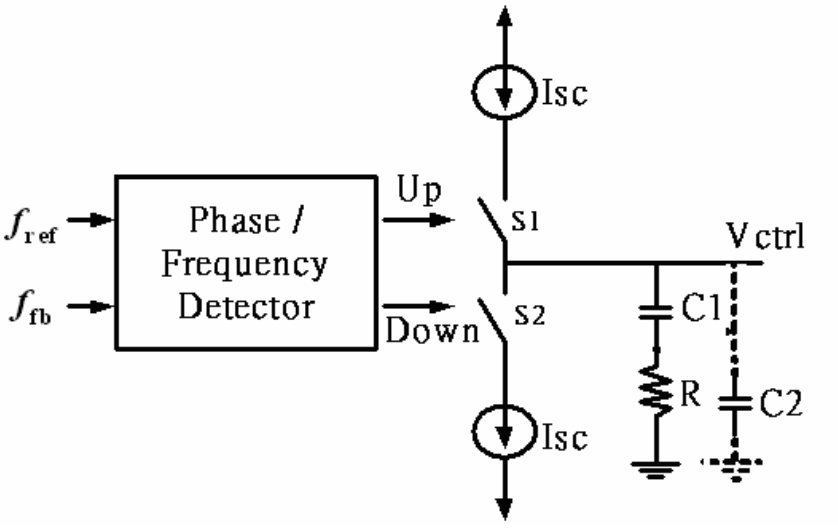


Fig.3-7 Charge pump phase comparator

3.3.2 Charge Pump

Charge pump is a circuit that supplies current to the loop filter to produce the control voltage that can vary VCO output frequency. When designing a charge pump circuit, it is important to choose Isc based on practical considerations such as power dissipation and speed. A typical charge pump is shown in Fig.3-7. When S1 is closed, Isc flows into the low-pass filter, increasing the control voltage into the VCO; when S2 is closed, Isc flows out of the low-pass filter, decreasing the control voltage of the VCO. When both switches are open, the top plate of C1 is open circuited and the output voltage remains constant in the steady state. The resistor, R, has been included to realize a zero in the low-pass filter's transfer function. And, the capacitor, C2, is included to suppress glitches.

As showed in Fig.3-8, some undesirable features of charge pumps are the charge injection and sharing produced by the overlap capacitance of the switch devices and by the capacitances at the intermediate node between the current source and switch devices. These phenomena will result in a phase offset at the input of the phase detector when PLL is in lock mode. This phase offset will increase as the charge pump current is reduced. In order to solve these problems, the control voltage must be isolated from the switching noise resulting from the overlap capacitance of the switch devices. And, in order to fix the charge-sharing problem, an operation amplifier can be adopted to buffer the output voltage to let the intermediate nodes switch to the output of the amplifier while the switches are off [11].

The charge pump used in this thesis is shown in Fig.3-9. The switches Mp1 and Mn2 are on the side of the current source devices Mp2 and Mn1 in order to reduce any switching error that will affect the sensitive output node Vctrl directly. So, the

control voltage Vctrl is isolated from the switching noise. When switching devices are off, the intermediate nodes between Mp1、Mp2 and Mn1、Mn2 will be charged toward the Vctrl by the gate overdrive of the current source devices. In order to make sure the matching between current *Ip* and *In*, the cascode current mirror circuit is used.

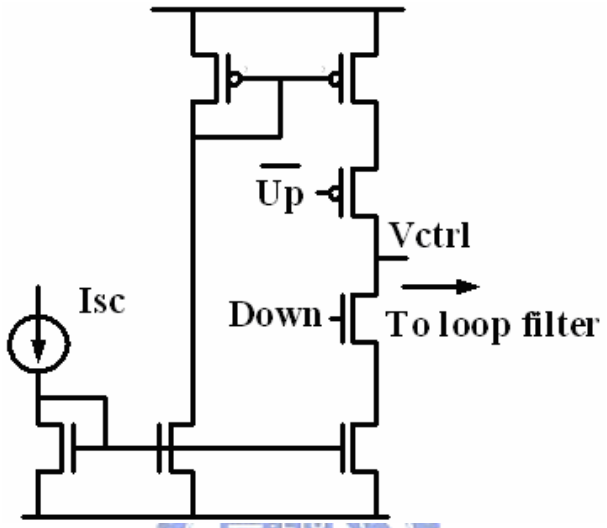


Fig.3-8 Charge pump with charge injection effect

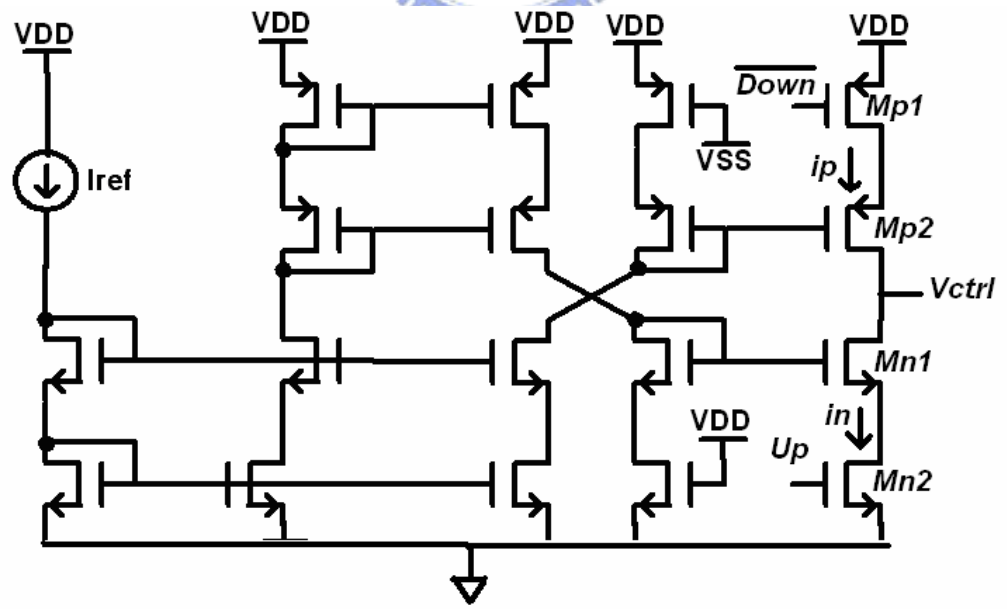


Fig.3-9 Schematic of charge pump

3.3.3 Voltage Control Oscillator (VCO)

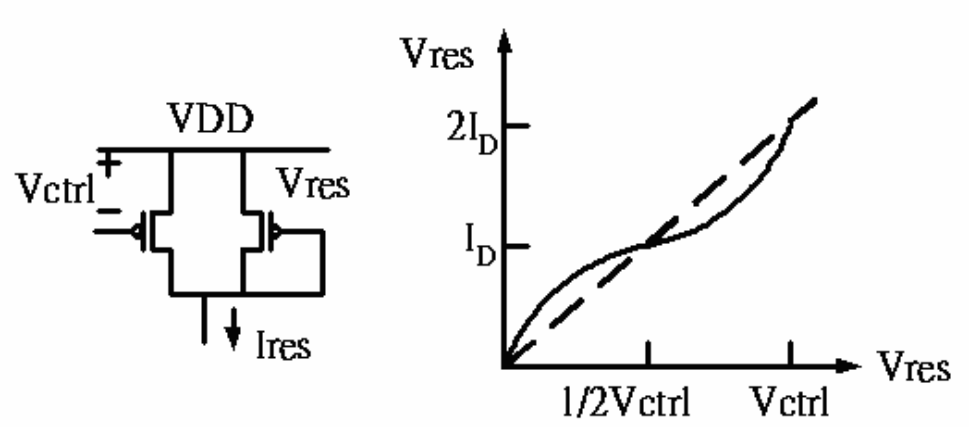


Fig.10 The symmetric load I-V curve

The voltage control oscillator is a critical building block in PLL design due to their relevant dependency on output jitter performance. In the mixed mode circuit system, the digital circuits in operation produce very large switching currents that perturb supply and substrate voltage, and in turn the noises from supply and substrate dominate the overall jitter performance. Therefore, the basic building block of the VCO used in this thesis is based on the differential delay stages with symmetric loads [12]. With symmetric loads, because the I-V curve is symmetrical to the center of the output voltage swing, the first order noise coupling terms cancel out, leaving only the higher order terms and substantially reducing the jitter caused by common mode noise present on the supplies. The symmetric load I-V curve is shown in Fig.3-10. The current of the MOS device biased by Vres = Vctrl is $I_D = \frac{k}{2}(Vctrl - |V_T|)^2$, so the buffer bias current is $2I_D$.

The VCO consists of a N-stage differential ring oscillator according to its applications. The differential delay cell based on symmetric loads is adopted for its lower sensitivity to supply and substrate noise, as shown in Fig.3-11 [13]. It can be shown that the effective resistance of the symmetric load, R_{eff}, is directly proportion to

the small signal resistance at the ends of the swing range that is one over the transconductance g_m for one of the two equally sized devices when biased at control voltage. Thus, the delay per stage can be expressed by the equation

$$t_d = R_{eff} \times C_{eff} = \frac{1}{gm} \times C_{eff} \quad \textbf{(3-1)}$$

where C_{eff} is the effective delay cell output capacitance, R_{eff} is the effective resistance of delay cell. The drain current for one of the two equally sized devices at Vctrl is given by

$$I_d = \frac{k}{2}[(Vdd - Vctrl) - |Vtp|]^2 \quad \textbf{(3-2)}$$

where k is the device transconductance of the PMOS device. Taking the derivative with respect to (Vdd - Vctrl), the transconductance is given by

$$gm = k[(Vdd - Vctrl) - |Vtp|] \quad \textbf{(3-3)}$$

Combining (3-1) with (3-3), the delay of each stage can be written as

$$td = \frac{Ceff}{k[(Vdd - Vctrl) - |Vtp|]} \quad \textbf{(3-4)}$$

The period of a ring oscillator with N delay stages is approximately 2N times the delay per stage. This translates to a center frequency of

$$f_{vco} = \frac{1}{2Nt_d} = \frac{k[(Vdd - Vctrl) - |Vtp|]}{2NC_{eff}} \quad \textbf{(3-5)}$$

Thus, the gain of the VCO is given by

$$K_{vco} = \left| \frac{\partial f_{vco}}{\partial Vctrl} \right| \quad \textbf{(3-6)}$$

As a result, K_{vco} is independent of buffer bias current and the VCO has first order tuning linearity. The f_{vco} is also directly proportional to (Vdd - Vctrl) and has no relationship to supply voltage.

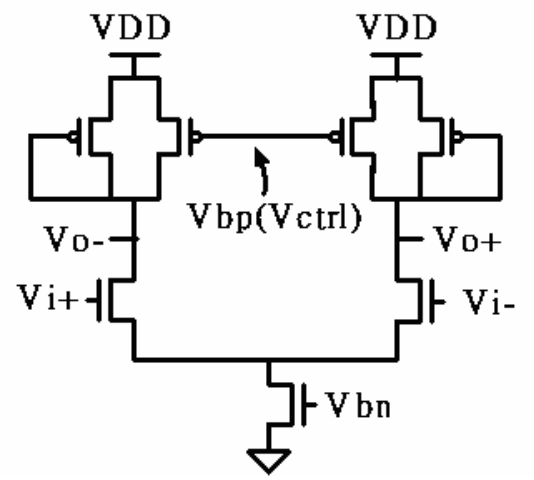


Fig.3-11 Schematic of VCO delay cell with symmetric load elements

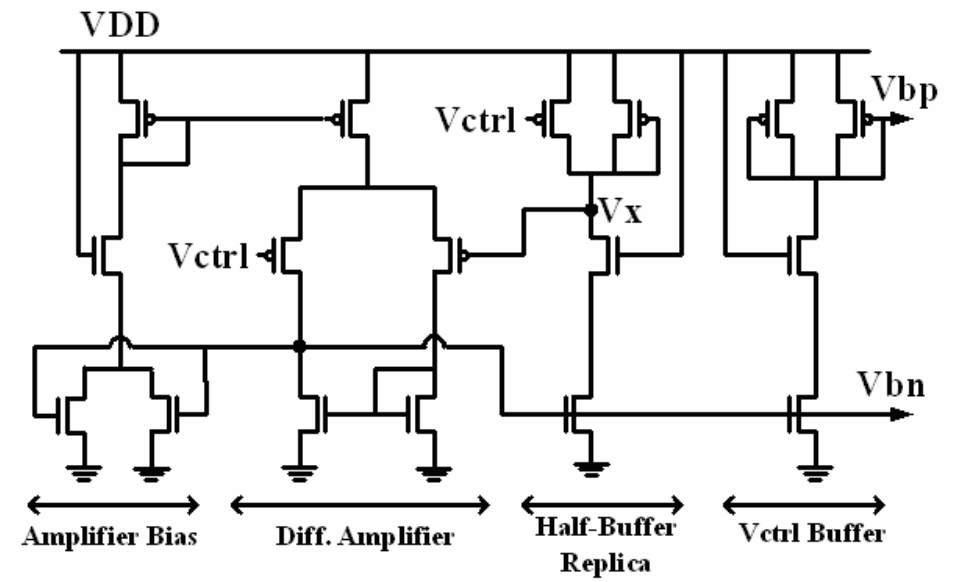


Fig.3-12 Replica-feedback current source bias circuit

As shown in Fig.3-12, the bias generator that produces the bias voltages Vbp and Vbn from Vctrl consists of a amplifier bias, a differential amplifier, a half-buffer replica, and a control voltage buffer. Its primary function is to continuously adjust the buffer bias current in order to provide the correct lower swing limit of Vctrl for the buffer stages. In doing this, it establishes a current that is held constant and independent of supply voltage. It accomplishes this task by using a differential

amplifier. Then, the amplifier adjust Vbn so that the voltage at the output of the half-buffer replica, Vx, is equal to Vctrl. The bias generator also provides a buffered version of Vctrl at the the Vbp output using an additional half-buffer replica. This output isolates Vctrl from potential capacitive coupling in the buffer stages and play a key role in the self-biased PLL design. With this bias generator, the buffer stages achieve a static supply noise rejection while operating over a broad delay range with low supply voltage requirements that scale with the operating delay [13].

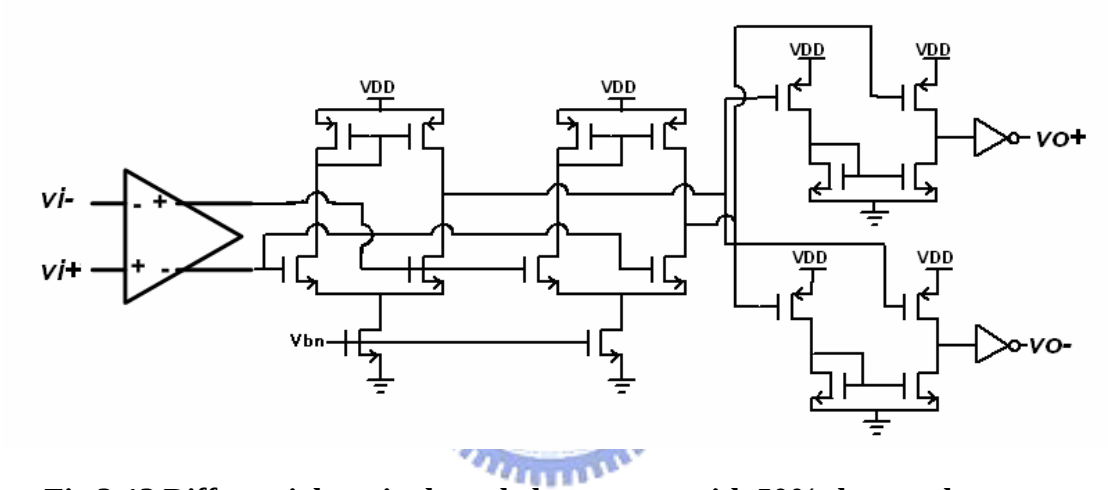


Fig.3-13 Differential-to-single-ended converter with 50% duty cycle output

PLLs are typically designed to operate at twice the chip operating frequency so that their outputs can be divided by two in order to guarantee a 50% duty cycle [14]. The differential-to-single-ended converter circuit shown in Fig.3-13 can produce such a 50% duty cycle output. It is composed of two opposite phase NMOS differential amplifiers driving two PMOS common-source amplifiers connected by an NMOS current mirror. The two NMOS differential amplifiers are constructed from symmetric load buffer stages using the same NMOS current source bias voltage as the driving buffer stages so that they receive the correct common-mode input voltage level. The PMOS common-source amplifiers provide additional signal amplification and

conversion to a single-ended output through the NMOS current mirror. Because the two level of amplification are differentially balanced with a wide bandwidth, the opposing differential input transitions have equal delay to the output. According to Vbn, the circuit corrects the input common-mode voltage level. The inverters are also added at the output in order to improve the driving ability.

3.3.4 Loop Filter and Divider

The passive loop filter configuration used in this thesis is shown in Fig.3-14. Resistor R_2 in series with capacitor C_2 provides a zero in the open loop response that improves the phase margin and the overall stability of the loop. The shunt capacitor C_1 is used to avoid discrete voltage steps at the control part of the VCO due to the instantaneous changes in the charge pump current output. But it can adversely affect the overall stability of the loop. In this thesis, as shown in Fig.3-15 [15], the TSPC D-Flip-Flop, a divided-by-2 circuit, is used to double input reference frequency. In order to make this circuit have correct operation, the input clock driving capability must be checked.

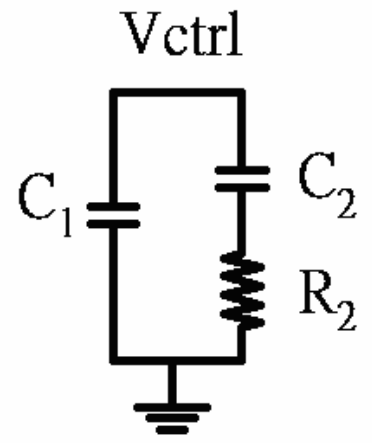


Fig.3-14 2nd order passive loop filter

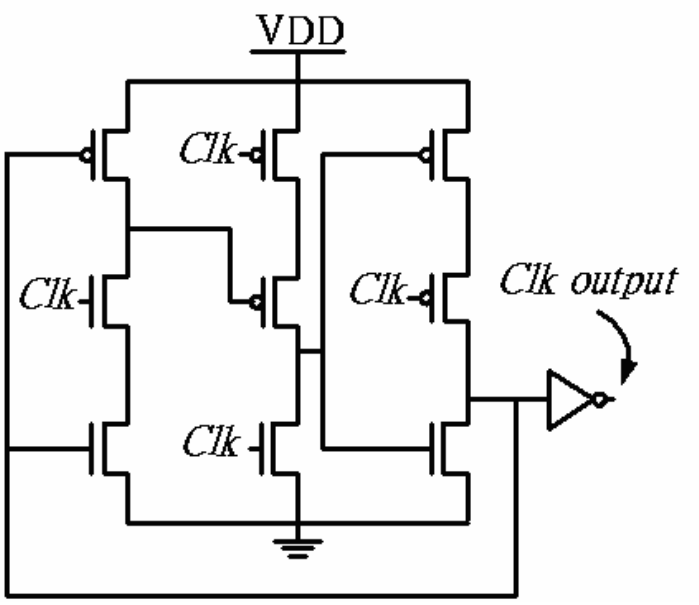


Fig.3-15 TSPC asynchronous divided-by-two circuit

3.4 Fundamentals of PLL

3.4.1 PLL Linear Model

The phase-locked loop is a highly nonlinear system. Fortunately, once a PLL is in lock, its dynamic response to input-signal phase and frequency changes can be well approximated by a linear model, as long as these changes are slow and small about their operating or bias point. A linear mathematical model representing the phase of the PLL in the locked stage is presented in Fig.3-16 [16].

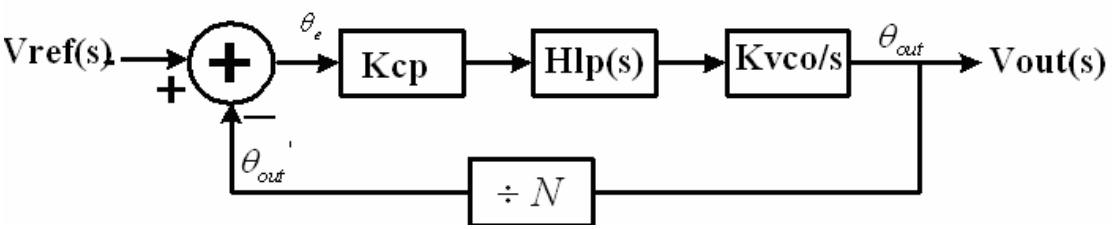


Fig.3-16 PLL linear model

When the loop is locked, the PFD, represented by a subtractor, has the output voltage proportional to the difference in phase between its inputs, defined as $\theta_e = \theta_{ref} - \theta_{out}$. The average error current within a cycle is $i_d = I_p \frac{\theta_e}{2\pi}$. The ratio of the current output to the input phase differential, *K*cp, is defined as $\frac{I_p}{2\pi}$ (A/rad). The loop filter has a transfer function *Hlp*(s) (V/A). The ratio of the VCO frequency to the control voltage is *K*v (Hz/V). N is the divider ratio. N=2, then the output frequency of the VCO is twice the reference input frequency. Similarly, if N is equal to eight, the output frequency of the VCO is eight times the reference input frequency. Since phase is the integral of frequency over time, *K*v (Hz/V) should be changed to $\frac{2\pi K_v}{s} = \frac{K_{vco}}{s}$ (rad/sec.V).

The open-loop transfer function of the PLL can be represented as

$$G(s) = \frac{\theta_{out}'(s)}{\theta_{in}(s)} = \frac{IpKvHlp(s)}{sN} \qquad \textbf{(3-7)}$$

From the feedback theory, the close-loop transfer function of the PLL can be found as

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = N\frac{G(s)}{1+G(s)} \qquad \textbf{(3-8)}$$

In order to keep the mathematics simple, the parasitic capacitance shunting the loop filter to ground, C_1, may be omitted. With $Hlp(s) = R_2 + \frac{1}{sC_2}$, as shown in Fig.3-15, the close-loop transfer function of the PLL can be expressed by the equation

$$H(s) = N\frac{(\frac{IpKv}{NC_2})(1+sR_2C_2)}{s^2 + s(\frac{IpKv}{N})R_2 + \frac{IpKv}{NC_2}} \qquad \textbf{(3-8)}$$

This can be compared with the classical two-pole system transfer function

$$H(s) = N\frac{\omega_n{}^2(1+\frac{s}{\omega_z})}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \qquad \textbf{(3-9)}$$

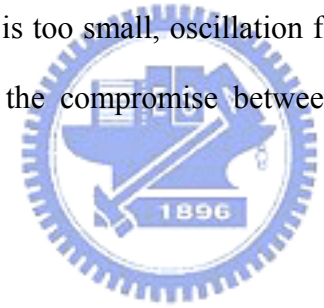
Then, the parameters natural frequency ω_n , zero of the LP ω_z and damping factor ζ can be derived as

$$\omega_n = \sqrt{\frac{IpKv}{NC_2}} = \sqrt{\frac{kcpKvco}{NC_2}} \quad \textbf{(3-10)}$$

$$\omega_z = \frac{1}{R_2 \times C_2} \quad \textbf{(3-11)}$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{R_2}{2}\sqrt{\frac{KcpKvcoC_2}{N}} = \frac{R_2}{2}\sqrt{\frac{IpKvC_2}{N}} \quad \textbf{(3-12)}$$

In a 2nd-order system, the loop bandwidth of the PLL is determined by ω_n . But the -3dB bandwidth should be $K = \frac{IpKvcoR_2}{N}$ (Hz). As for the value chosen for damping factor, a larger one will result in sluggish response and longer lock acquisition time. To the other end, if its value is too small, oscillation for step response will occur and the system is unstable. For the compromise between the two ends, ζ = 1.414 is adopted for this work.



3.4.2 PLL Noise Analysis and Stability

The transfer function can be derived for disturbances injected at various points in the PLL, such as those in Fig.3-17. The response to current variation injected at the output of the charge pump and the phase detector can be derived as

$$H_i(s) = \frac{\theta_{out}(s)}{i_n(s)} = \frac{(\frac{Kvco}{C})(1+sRC)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textbf{(3-13)}$$

where the loop filter has been assumed. The response to voltage noise injected at the output of the filter, for example is

$$H_v(s) = \frac{\theta_{out}(s)}{v_n(s)} = \frac{sKvco}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textbf{(3-14)}$$

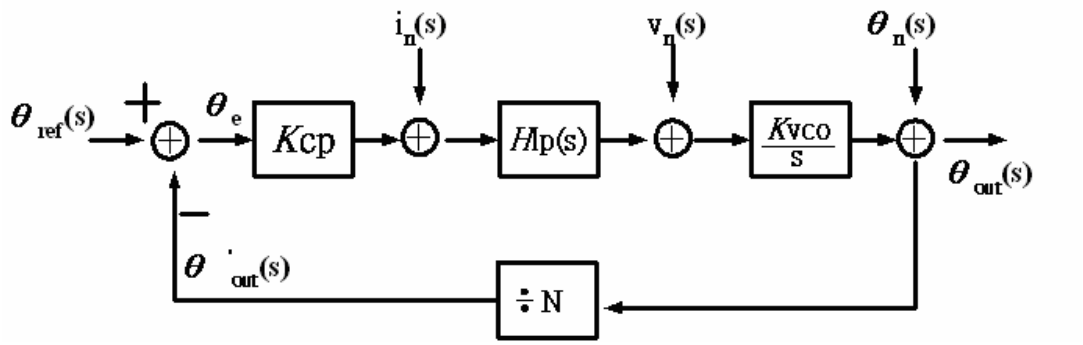


Fig.3-17 PLL linear model with various equivalent noise sources

Also, the response to phase errors injected by the VCO can be determined from

$$H_\theta(s) = \frac{\theta_{out}(s)}{\theta_n(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \textbf{(3-15)}$$

The transfer functions $H_i(s)$, $H_v(s)$ and $H_\theta(s)$ are low-pass, band-pass and high pass respectively [17][18]. One way to reduce the phase noise is to increase the loop bandwidth ω_n by increasing the value of *K*cp. When ω_n and Kcp are increased by the same factor, the phase noise transferred from i_n, v_n and θ_n is reduced. The maximum ω_n is restricted by the update rate ω_{ref} of the phase detector. Using such an analysis form [19], the criteria of the stability limit can be derived as:

$$\omega_n^2 < \frac{\omega^2_{ref}}{\pi(RC\omega_{ref} + \pi)} \qquad \textbf{(3-16)}$$

In general, it has approximately to be less than 1/10 of the phase detector update rate to avoid instability or $\omega_n < \frac{1}{10}\omega_{ref}$.

3.5 Loop Parameters Considerations

After the detail description of each building block, loop parameters and correlated system performance issues need to be considered carefully. Refer to the linear model and the derivation of transfer function, there are two additional terms needed to be satisfied for the system to be stable, and for the simplification of system order from third order to second order to be accurate. First, as mentioned before, the capacitor in loop filter shunted on control voltage for ripple suppression purpose must be much smaller than the filtering capacitor, $C_1 > 20C_2$, a condition to ignore the higher frequency pole induced by C_2. Second, as proposed in [19], the (3-16) must be satisfied for the system stability issues. As a rule of thumb, it is true that by keeping $\omega_{ref} > 10\omega_n$, stability in discrete-time model as well as in continuous-time model can be assumed. Under such a premise, the remaining loop parameters are be taken into consideration, specifically, natural frequency ω_n, damping factor ζ, and the most important one: phase margin of the open loop system.

3.6 Specification and Simulations of Transmitter PLL

Fig.3-18 shows the curve for open loop PLL frequency response. This curve gives the phase margin of approximately 70° .The simulation results of the VCO transfer characteristics are shown in Fig.3-19 and Fig.3-20. The supply voltage is 3.3V. For Vctrl between 1.0V and 2.0V, the gain of the VCO, Kvco, is 101 MHz/V. Total PLL parameter is listed in Table.3-1.

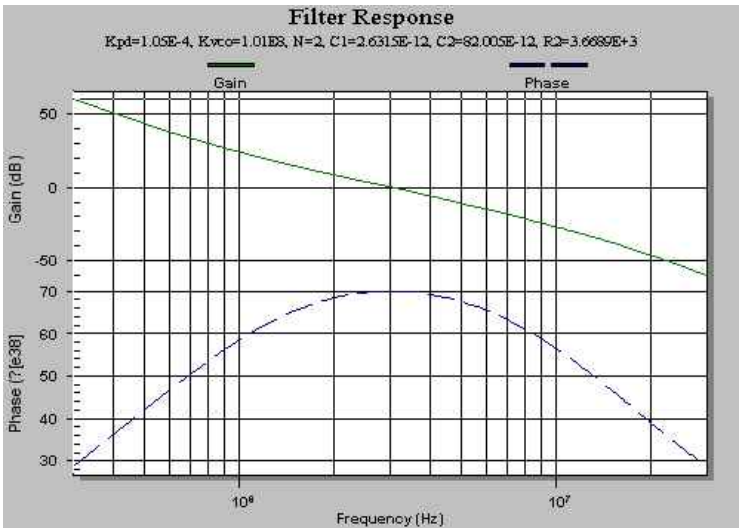


Fig.3-18 open loop PLL frequency response

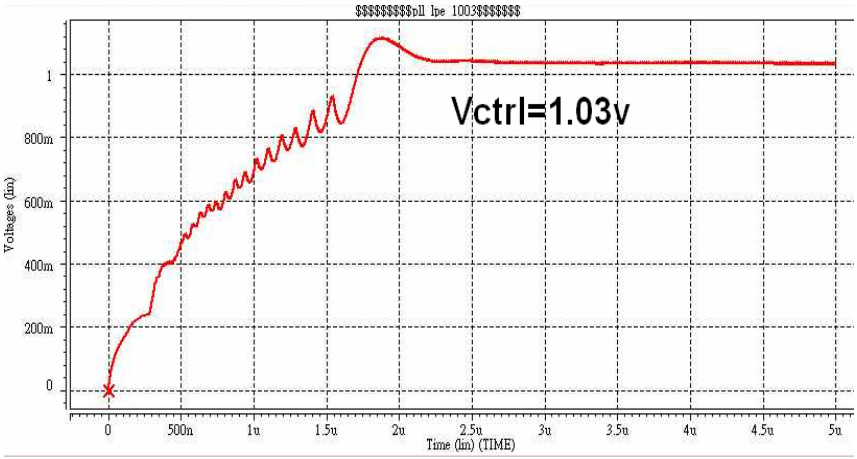


Fig.3-19 Vctrl timing diagram

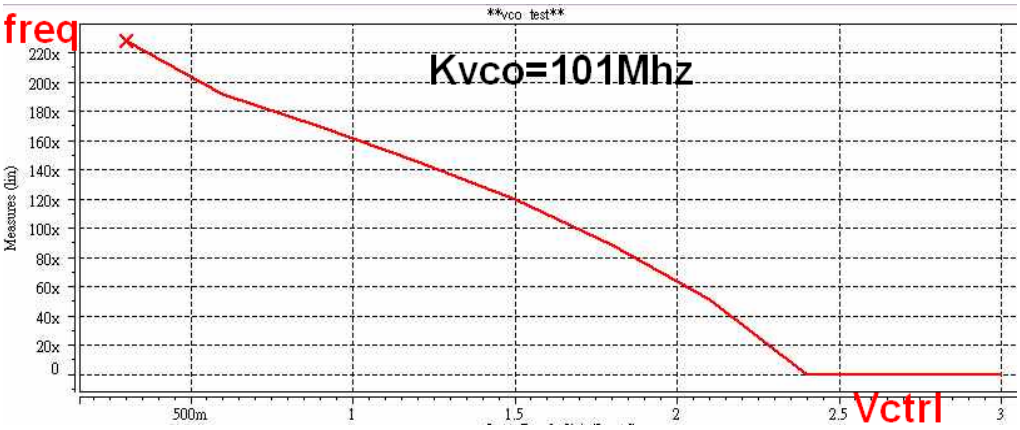


Fig.3-20 Kvco = 101MHz/V when Vctrl = 1.03v

Charge pump current (I_{cp})	**105 uA**
VCO center frequency (f_{vco})	**150Mhz**
Kvco	**101Mz/v**
Divider (N)	**2**
Loop bandwidth	**3000khz**
Phase margin	**70 degrees**
Loop filter	**C1=82p F**
	C2=2.63p F
	R1=3.67k ohm

Table.3-1 PLL specification of transmitter

3.7 Specification and Simulations of Receiver PLL

Fig.3-21 shows the curve for open loop PLL frequency response. This curve gives the phase margin of approximately 65° .The simulation results of the VCO transfer characteristics are shown in Fig.3-22 and Fig.3-230. The supply voltage is 3.3V. For Vctrl between 0.5V and 1.5V, the gain of the VCO, Kvco, is 227 MHz/V. Total PLL parameter is listed in Table.3-1.

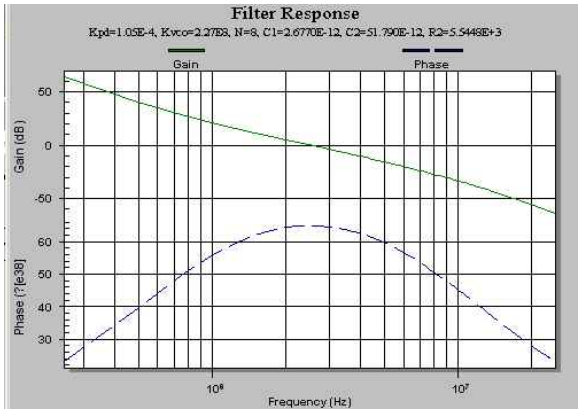


Fig.3-21 open loop PLL frequency response

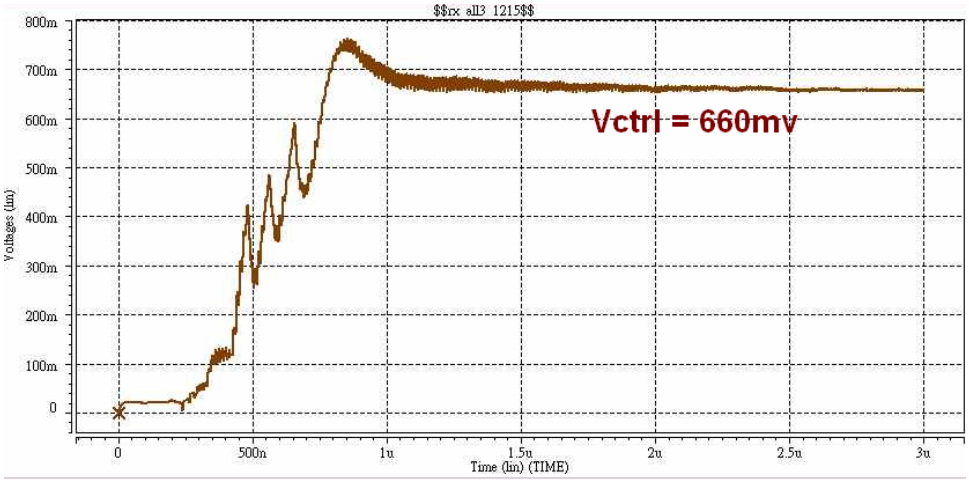


Fig.3-22 Vctrl timing diagram

Fig.3-23 Kvco = 227MHz/V when Vctrl = 0.66v

Charge pump current (I_{cp})	**105 uA**
VCO center frequency (f_{vco})	**600Mhz**
Kvco	**227Mz/v**
Divider (N)	**8**
Loop bandwidth	**2500khz**
Phase margin	**65 degrees**

Loop filter	**C1=57.8p F**
	C2=2.67p F
	R1=5.54k ohm

Table.3-2 PLL specification of receiver

Chapter 4

Transmitter

4.1 Architecture of Transmitter

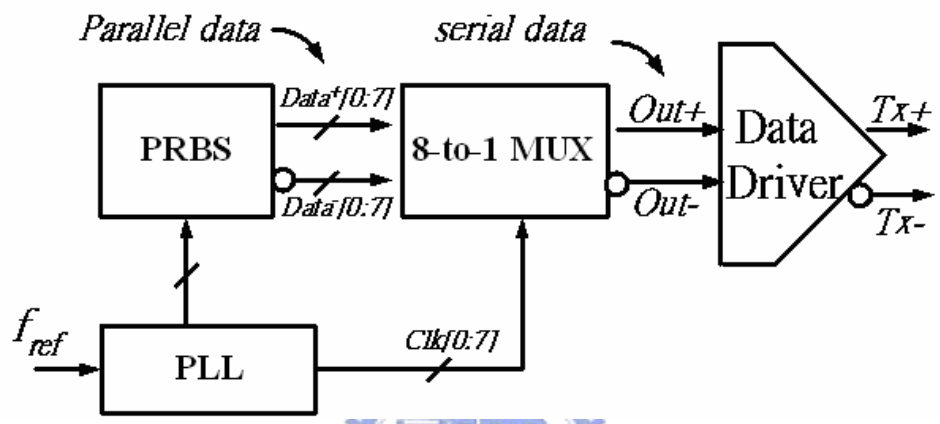


Fig.4-1 Block diagram of the transmitter

The block diagram of this transmitter is shown in Fig.4-1. It consists of a PRBS circuit, a PLL, an 8-to-1 data multiplexer and a data driver. For testing, the Pseudo Random Bit Sequence (PRBS) is utilized to generate data pattern. There is still a data capture logic circuit between PRBS and multiplexer in order to convert single-ended data into differential data and feed it into 8-to-1 multiplexer. We can reduce the frequency requirement of the timing circuits by using 8-to-1 input-multiplexer to serialize low-speed eight channels parallel data on eight even-spaced phases of frequency 150MHz which gives a bit rate of 1200Mbps. The eight even-spaced phases of frequency 150MHz is generated by PLL mentioned in chapter 3. Then, through the data driver, the data stream is transmitted out with a nominal swing of 200mV. In the following section, we will describe the detail circuits of the function blocks in the transmitter architecture.

4.2 Pseudo Random Bit Sequence (PRBS)

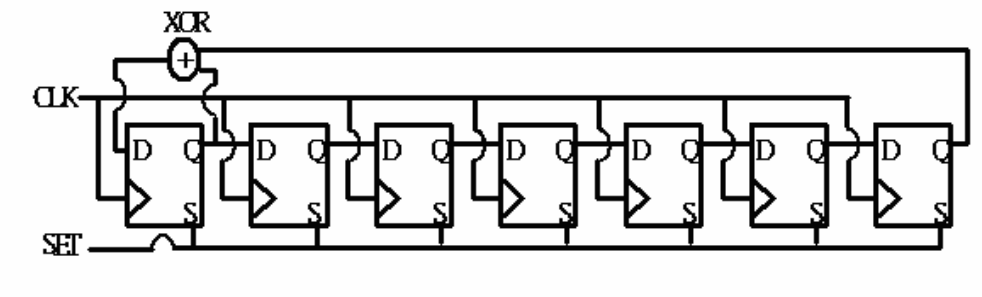


Fig.4-2 block diagram of Pseudo Random Bit Sequence (PRBS)

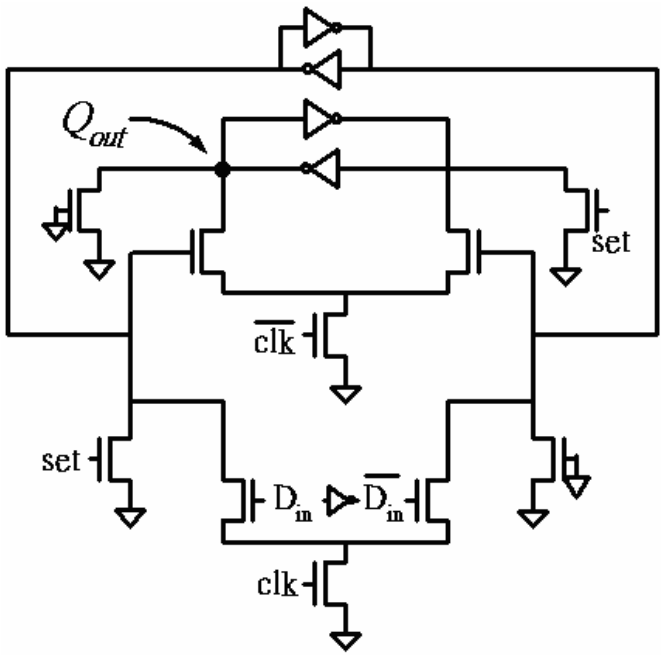


Fig.4-3 PRBS delay cell circuit

As shown in Fig.4-2, the Pseudo Random Bit Sequence is designed for testing. It is in fact a repetition of a pattern that itself consists of a random sequence of a number of bits. The pattern repeats every 2^7-1=127 clock cycles. We also note that if the initial condition is zero, the delay cells remain in a degenerate state. Therefore, the SET signal must be used to solve this problem. The XOR is the speed-critical part in the

circuit. Then, we can use the outputs of seven delay cells and XOR gate as 8-parallel data inputs of transmitter. Every delay cell is shown in Fig.4-3.

4.3 8:1 Multiplexer

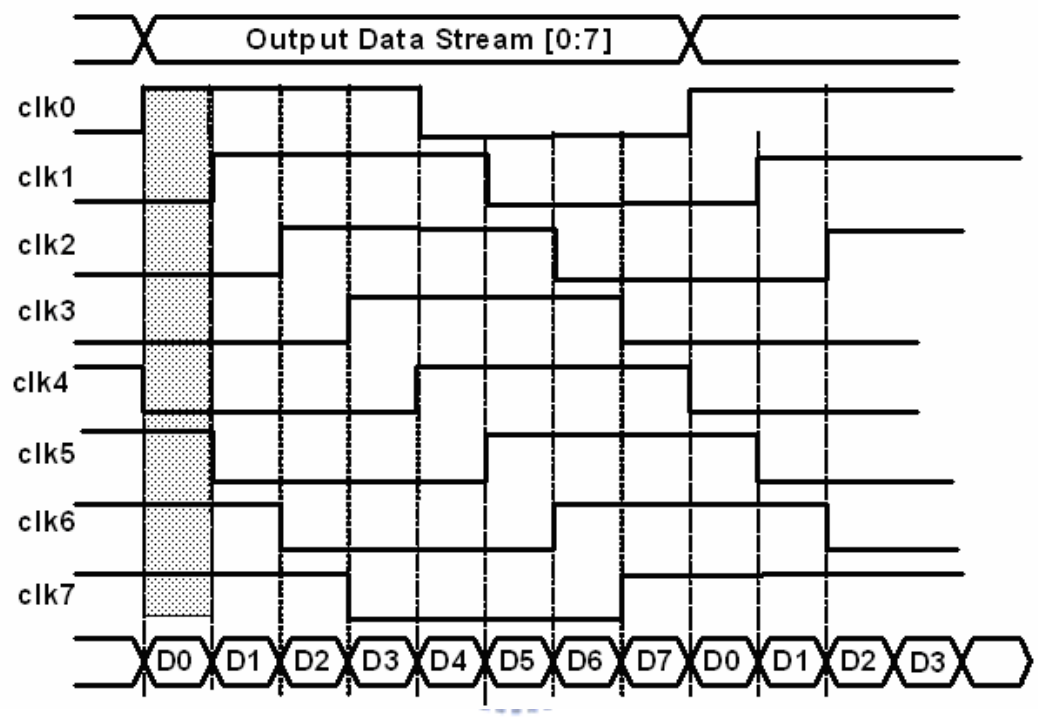


Fig. 4-4 Timing diagram of 8:1 multiplexer

When the transmitter transfers the data stream with 1.2Mbps, the PLL must produce eight-phases with 150MHz. The relationship between input data, D0~D7, and clock, clk0~clk7, is shown in Fig.4-4. For example, at the timing interval between the rising edge of clk0 and the falling edge of clk5, the input signal starts driving the multiplexer output. In order to achieve this algorithm, the multiplexer, as shown in Fig.4-5 [20][21], is used to serialize the parallel eight data channel input D0~D7. Each multiplexer is switched by two series NMOS transistors that are controlled by two specific clock signals.

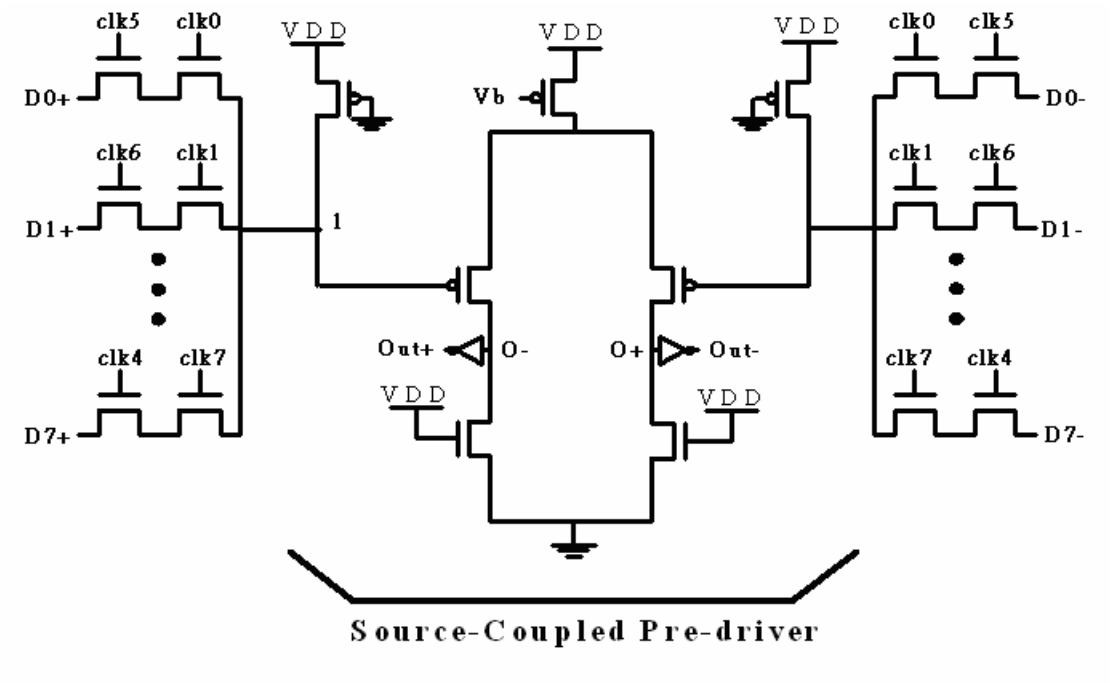


Fig.4-5 Schematic of data multiplexer

A more cost-effective method is to perform multiplexing at the input of the transmitter before the signal is buffered up. The speed of the input multiplexer circuit is mainly determined by the resistance of PMOS and the total capacitance of the output node. In other words, high multiplexer fan-in becomes the bottleneck and the achievable speed gradually decreases. This speed limitation is not an inherent property of the process technology but of the circuit topology [20]. Increasing the PMOS size relative to the NMOS size would increase the speed while reducing the swing of the output nodes 1. The power overhead for the increased speed compared to a static implementation is small since low energy signals are multiplexed before the preamplifier and final driver.

4.4 Data driver

As shown in Fig.4-6, the simplified RSDS outputs consist of a current source which drives the differential pair line. Because the basic receiver has high DC input impedance, the majority of driver current flows across the termination resistor generating about 200mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state. A differential load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time. However, an additional termination resistor is usually placed at the source end to suppress reflected waves caused by crosstalk or by imperfect termination, due to package parasitics and component tolerance [22]. The implemented transmitter data driver shown in Fig.4-7 uses the typical configurations with four MOS switches in bridge configuration. In order to define the correct output levels, a feedback loop across a replica of the transmitter circuit may be used, but in this case the effect of component mismatches between the transmitters and the replica should be carefully taken into account [23].

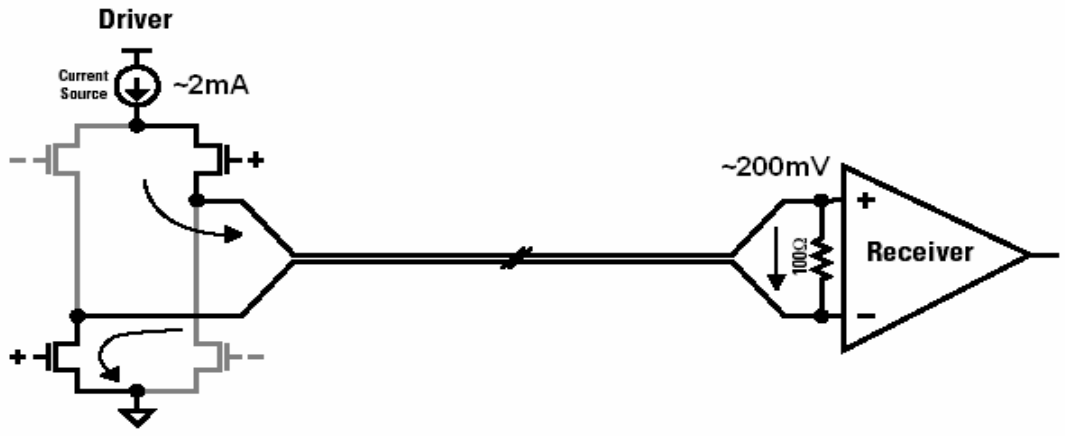


Fig.4-6 The simplified diagram of RSDS link with termination at the receiver

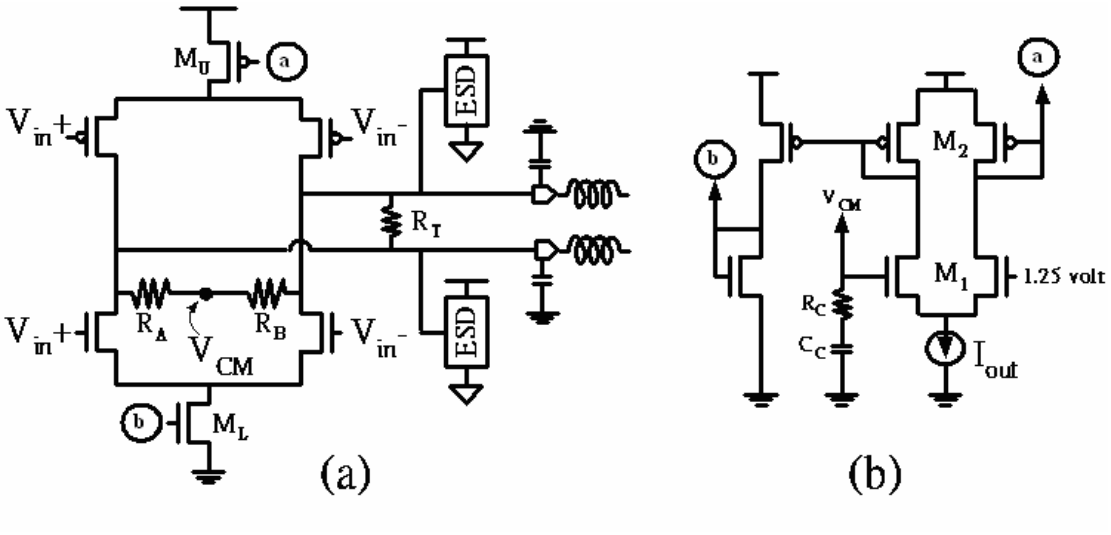


Fig.4-7 (a) Schematic diagram of the RSDS transmitter data driver. (b) Common mode feedback circuit.

As shown in Fig.4-7(b), a simple low-power common-mode feedback control was implemented in the transmitter to achieve higher precision and lower circuit complexity. The common-mode output voltage is sensed by means of a high resistive divider R_A and R_B (=50kΩ) and compared with a 1.25-V reference by the differential amplifier. The fraction of the tail current I_{out} flowing across M_1 and M_2 is mirrored to M_U and M_L, respectively, thus forcing $V_{CM} \approx 1.25V$. In order to develop the correct voltage swing on the 50- load resistance (R_T-transmitter//R_T-receiver), the bridge must be biased at I_{out}=400mA. A large stability margin over PVT variations is achieved for the common-mode feedback by means of a pole-zero compensation network, R_C-C_C [23]. This data driver must be designed as a pad-cell with custom electrostatic discharge (ESD) protections. And, the simulated typical capacitance contributed by the pad is about 3pF.

4.5 Simulation Result

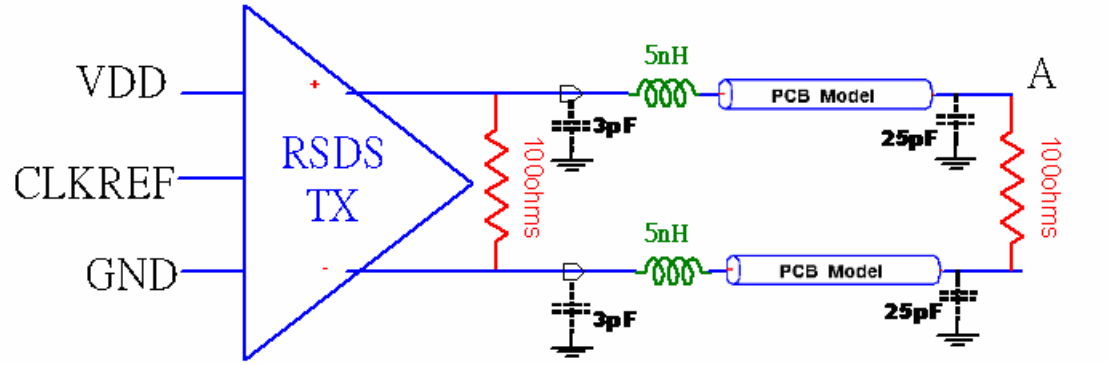


Fig.4-8 testing environment on board

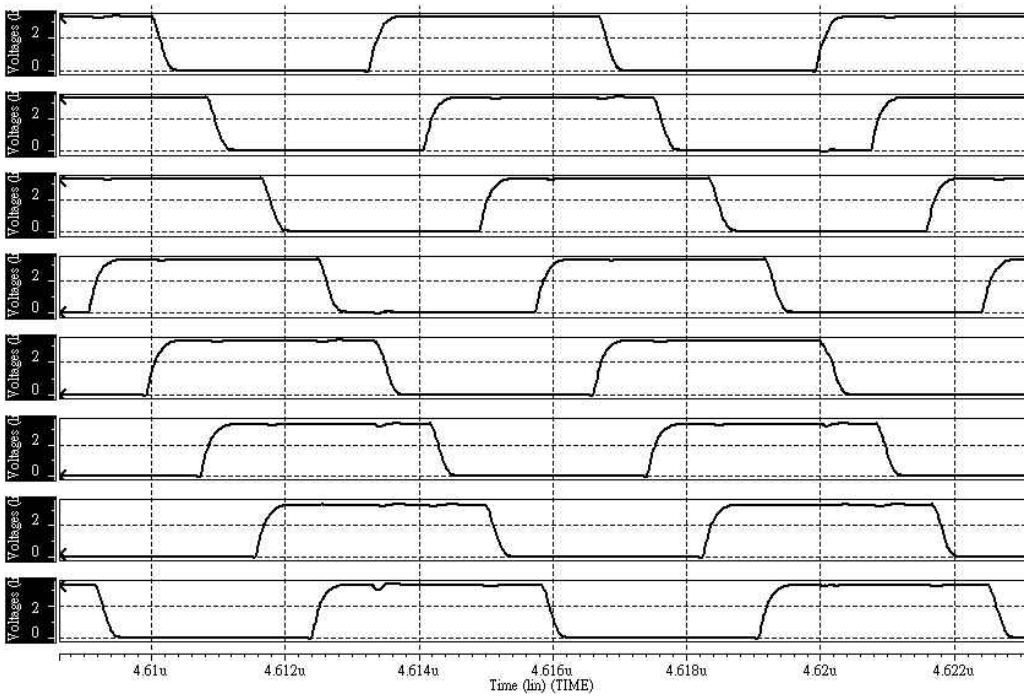


Fig.4-9 The result of eight-phase clock of PLL

In real IC, the die will be packaged and we should take it into consideration, as shown in Fig.4-8. Fig.4-9 is the result of the eight-phase clock of PLL, described in chap 3, used for multiplexer, and the frequency is 150MHz. Fig.4-10 and Fig.4-11 show the transmitter output data stream with the data rate at the 1.2Gbps and its eye

diagram.

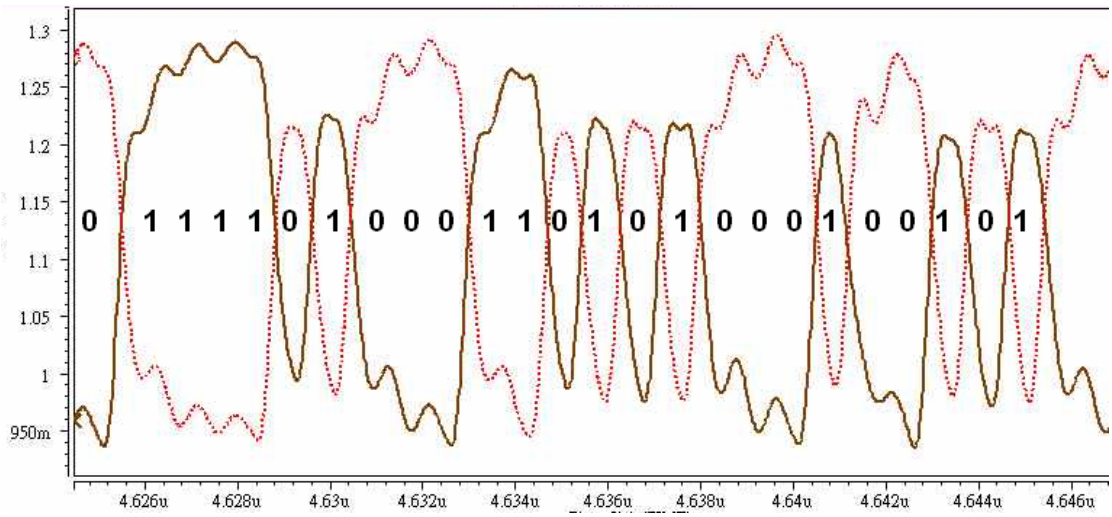


Fig.4-10 Simulation result of the transmitter output waveform

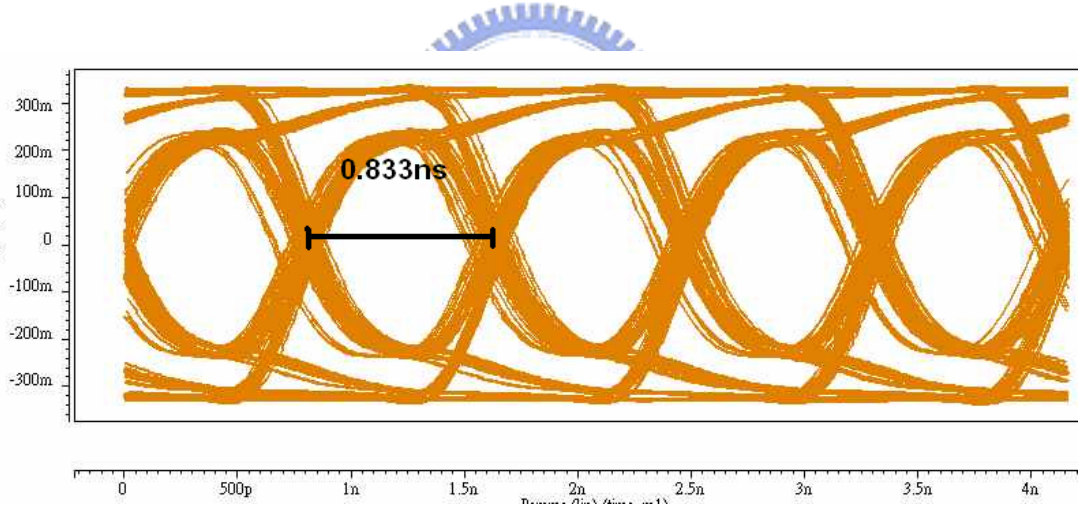


Fig.4-11 eye diagram

Chapter 5

Receiver

5.1 Tracking Data Recovery System Architecture Overview

The tracking clock recovery is an evolution from the PLL-based clock recovery. Generally speaking, there are two ways which can be adopted to recover the system clock, including oversampling and tracking schemes. Oversampling receivers in this thesis require three samples per bit. The samples are compared with neighboring samples to indicate whether a data transition occurs or not. After that, the bit boundary and also, the bit value, can be determined according to the decision, which is made based on the information from a set of data transitions. Oversampling receiver has several advantages compared to the tracking receiver. First, they are somewhat simpler to implement since there is no need for summing networks and phase interpolators. Second, they could reject high frequency jitter because they determine the bit value by comparing it directly with its nearest neighbor [24]. However, oversampling receiver requires a faster sampling rate and the chip area occupied by the decision logic block is significant. Besides, quantization jitter, which is the uncertainty in the position of each detected transition, is also introduced by the oversampling receiver.

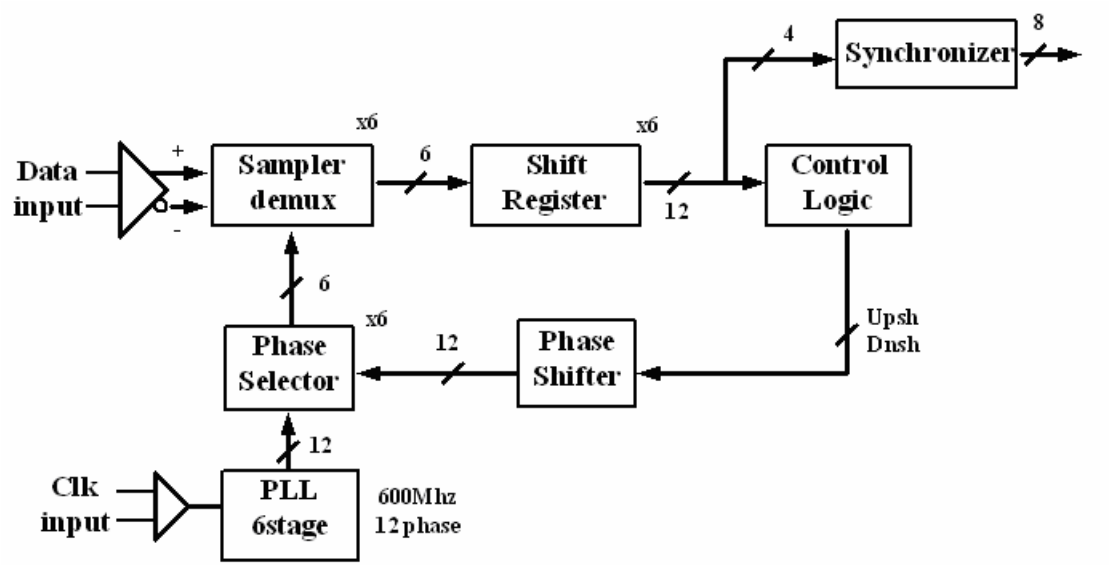


Fig.5-1 Block diagram of the tracking data recovery receiver

In general, the incoming data value has to be decided by adopting the sampler circuit. In order to accurately sample the incoming data with the maximum timing margin, the sampling clock phase need to be positioned at the center of the received data eye. Therefore, it is necessary to adjust the phase of the sampling clock to overcome the uncertainly delay between the clock and signal in the circumstance of interconnection delay and low-pass characteristic of the channel, transceiver characteristics variations to gain the maximum timing budget. This can be done in a closed-loop manner to continuously optimize the timing margin between clock and data stream. Fig. 5-1 shows the block diagram of the tracking data recovery receiver. It consists of demultiplexing samplers, shift registers, a control logic circuit, a synchronizer, a phase shifter, phase selectors, a PLL and two interface circuits. The tracking receiver system operates as follows. At the first, the input data stream and system clock are received and amplified by the front-end amplifier and only the system clock is converted to single-ended. The sampling clock phases provided by PLL are use to oversample incoming data stream three times per bit in the demultiplexing sampler band. Based on the oversampling mechanism, we need

6-stage PLL to produce 12 clock phases at 600 MHz because the resolution of sampling clock we expect is 1/6 bit time. Then, according to the decision made by the phase shifter, the phase selectors pick up six of twelve clock phases from PLL outputs. These six phases are used to sample the incoming data stream three times per bit in the sampler band. Therefore, shifter registers accumulate four sets of oversampling data and sent them to following control logic to decide whether the sampling clock phases align the data or not. After the sampling clock phases are locked with the data signal stream, the middle data in each of the 3X oversample group is chosen as the recovered data. However, these data are sampled by different phases, and would be asynchronous. Therefore, a re-timing circuit, two-step synchronizer, is needed.

Fig. 5-2 shows three different cases of the alignment, including LOCK, LEAD, and LAG. These three states are the basis of the mechanism in adjusting phases and design of the control logic. The control logic has two output signals, Upsh and Dnsh. Based on the control logic outputs, the phase shifter will send a twelve-bit code to the phase selector band to adjust the sampling clock phases. For example, when the sampling clocks lag the input data stream as in Fig. 5.2 (b), data transitions might occur between the second and the third sampling phases in each group of the oversampling data, and the control logic will send an Upsh signal to the phase shifter. According to the Upsh signal, the phase selector band will select the earlier clock phase relative to the original one. On the contrary, as in Fig. 5-2 (c), when the sampling clocks lead the input data stream, data transitions might occur between the first and second sampling phases, and Dnsh signal will be sent to the phase shifter and the phase selector band will select the later phase relative to the original one. This process will continuously be repeated until no data transition is detected, as shown in Fig.5-2 (a). By this kind of tracking data feedback loop, the system is locked and any

skew could be detected and calibrated. The advantage of employing digital control logic approach to adjust the phase of receiver system clock lies in its better noise margin than conventional analog summing network. When the system is in lock state, the second data in each group, that is, D1b, D2b, D3b, D4b are the transmitted data value which will be sent out through the synchronizer circuit. Compared with the majority voting algorithm proposed in [24][25], the central picking method is simpler and more adequate in the case of bandwidth-limited signal.

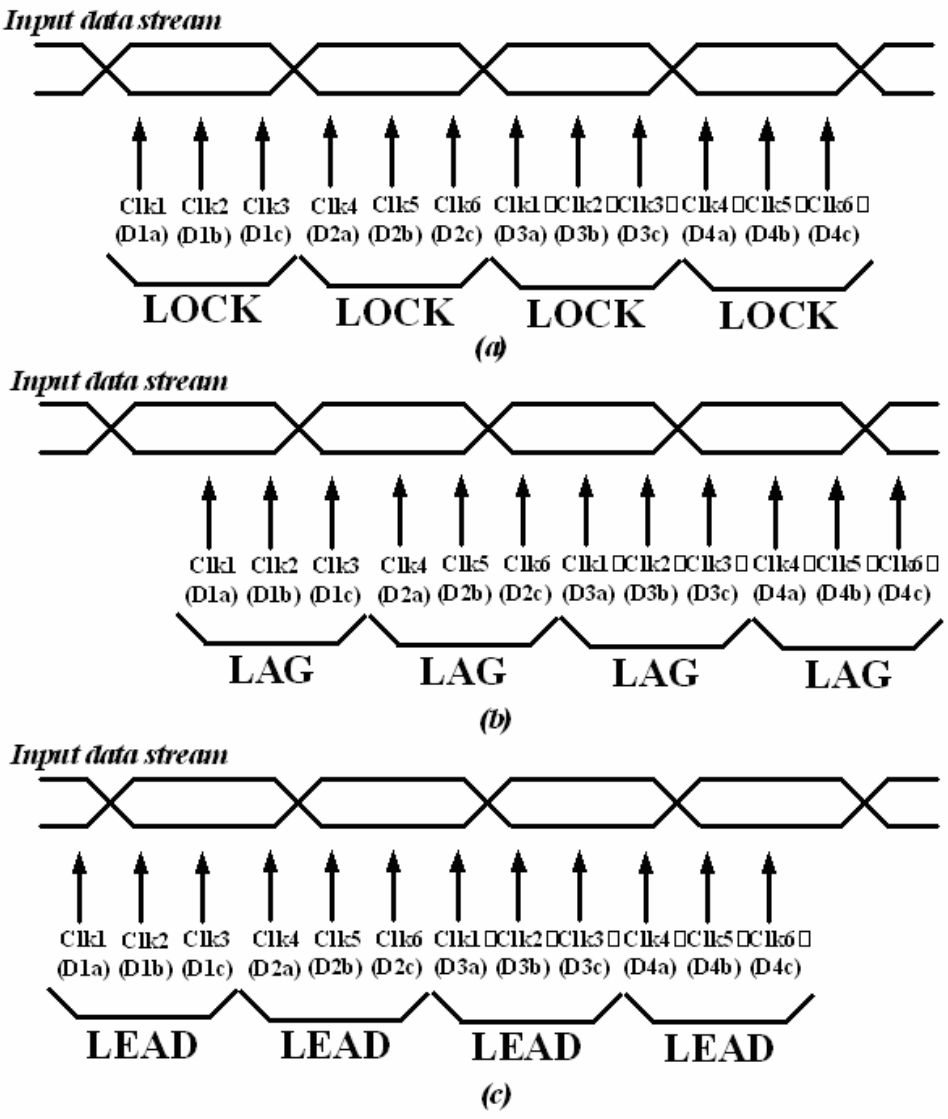


Fig.5-2 (a)LOCK, (b)LAG and (c) LEAD states of the tracking data recovery receiver

5.2 Front-end Amplifier

Front-end amplifier is used to recovery several hundred mV input signal to full swing. Fig.5-3 shows the circuit diagram of the front-end interface amplifier [26]. It plays a key role to sense received signals, either from system clocks or input data stream, therefore input sensitivity, symmetry and bandwidth are major concerns. In order to meet the common-mode voltage range, the circuit is implemented with PMOS differential pairs with a constant current source. The differential voltage signal at the input is detected by a Schmitt trigger m1-m6 which ensures a 27mV hysteresis, and full-swing CMOS level are obtained at the output, Vop and Von, by inverter pairs m7-m8 and m9-m10. Moreover, the offset voltage of the amplifier also affects the correct operation of the circuit. The offset voltage is not only due to the mismatches in the input devices but also mismatches within the positive-feedback structure. The advantage of this hysteresis circuit is noise immunity.

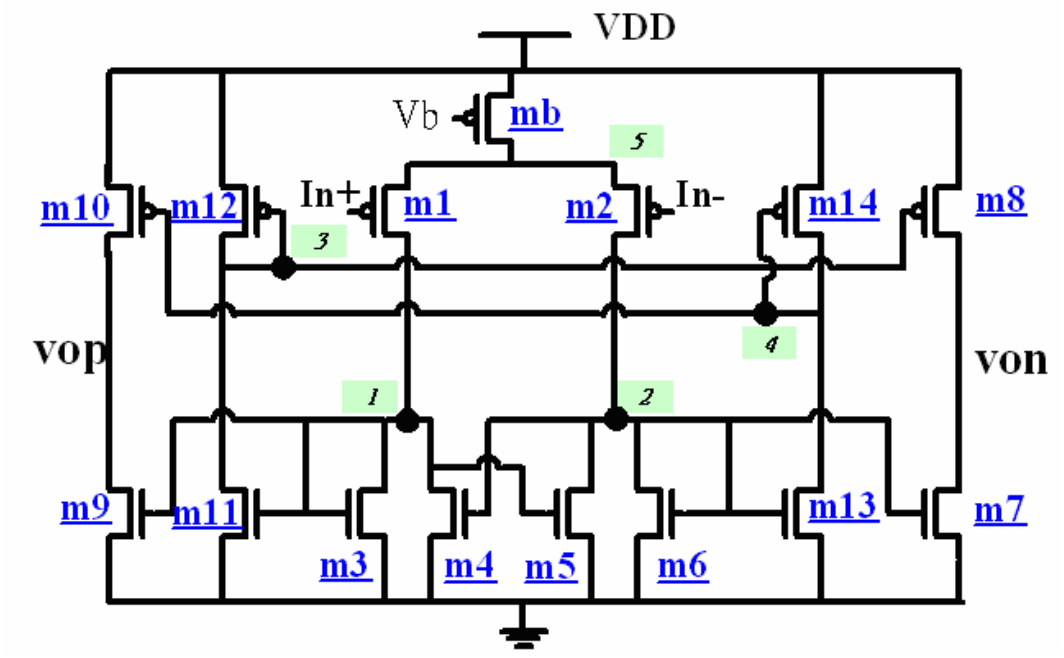


Fig.5-3 Schematic diagram of front-end amplifier

We define the size ratio A= $(W/L)_5/(W/L)_6=(W/L)_4/(W/L)_3$. The threshold voltage depends on not only the bias current but also the size ratio of the lower two current mirrors. If A<1, there is no hysteresis in transfer function, when A>1, hysteresis will result as Fig.5-4. Fig.5-5 shows the frequency response of the front-end amplifier. It can be shown that it still has about 20dB gain at the data rate (1.2Gbps) of the transmitted signal.

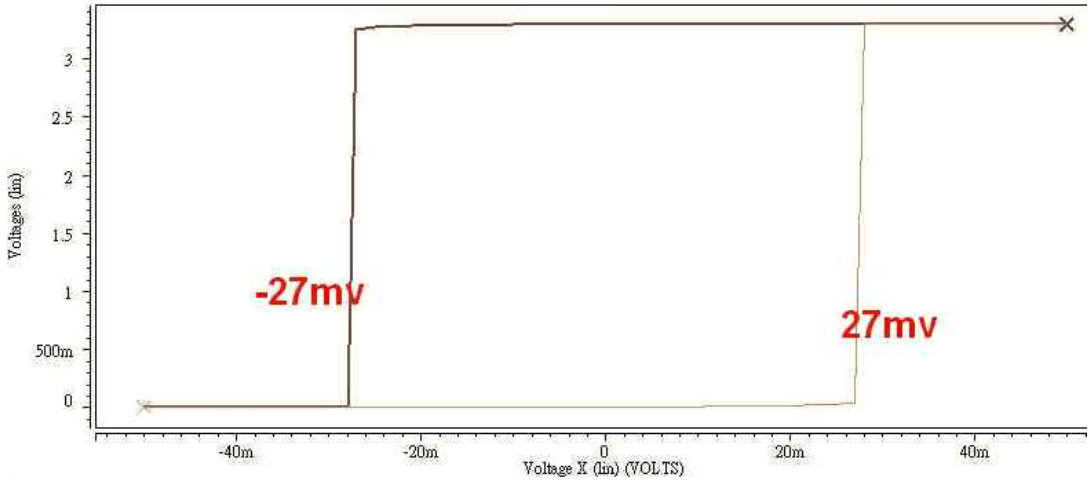


Fig.5-4 Simulation of hysteresis comparator

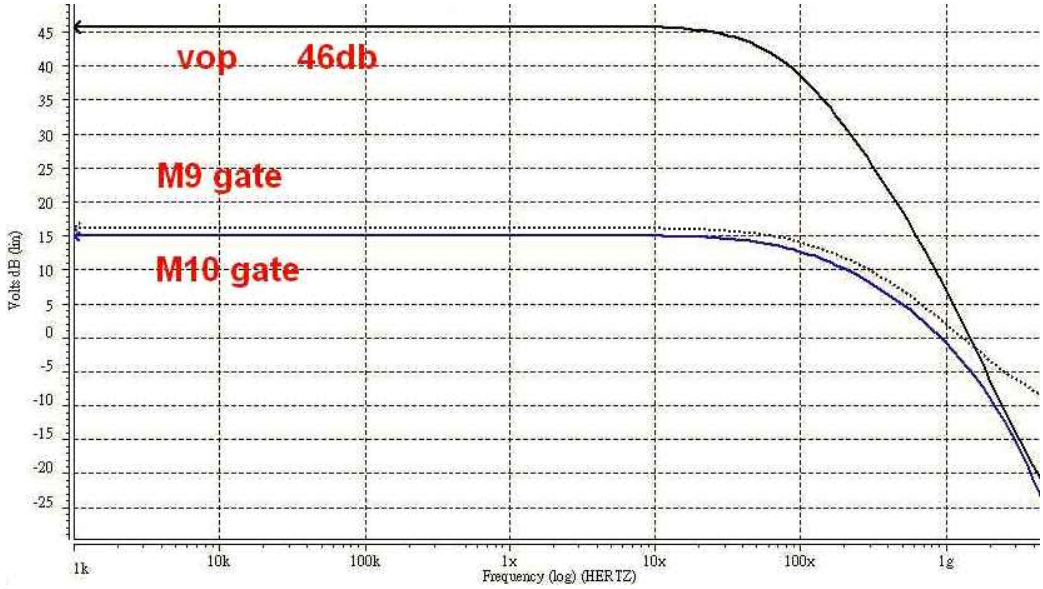


Fig.5-5 The frequency response of front-end amplifier

5.3 Sampler

After regenerating by the front-end amplifier, the output vop (In+) and von (In-) are sent to the sampler band to sample the data value. Due to the 3*X* oversampling mechanism, there are six samplers in the sampling band. The sampler circuit diagram is shown in Fig. 5-6. The important characteristics of the sampler are the aperture, input capacitance and the input-referred offset voltage [27]. It consists of a pair of cross-coupled inverters with variable-strength pull-down paths controlled by data input devices. In order to minimize input capacitance, the size of data input devices must be small. However, small device size exhibits poor matching characteristics that cause timing error. Therefore, the size of the input transistors should be designed carefully. With outputs precharged high during CLKi low, the addition of an R-S latch at the outputs cause this sense amplifier to behave as edge triggered Flip-Flop.

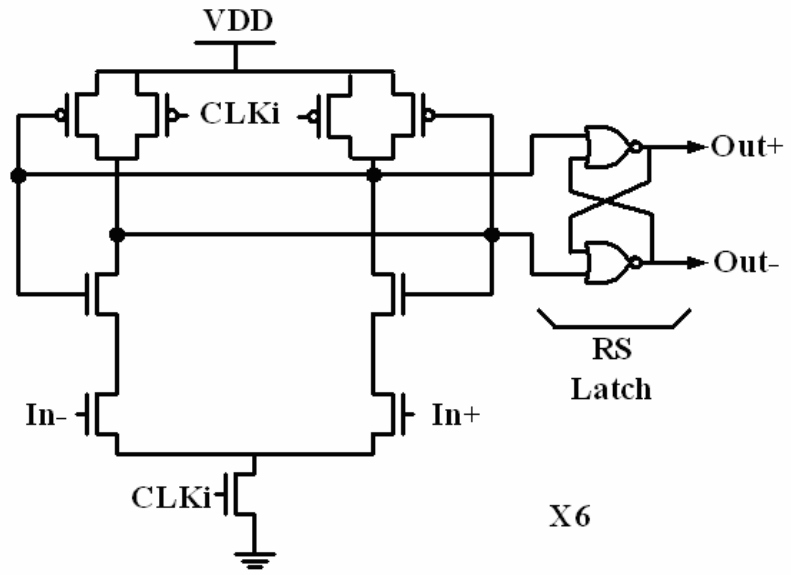


Fig.5-6 The demultiplexing sampler

5.4 Control Logic

As shown in Fig.5-7, the control logic is composed of four sets of edge detector, a latch band and an UP/DN decision logic. The function of the control logic is to process the 3X oversampled data value and indicate whether to shift up or down of the sampling clock phases. These four sets of sampled data value are fed into four edge detectors to check if any value transition occurs within the same set. The truth table and circuit of the edge detector is shown in Fig.5-8 [28]. If a data transition occurs between the first and second sampling phases, as shown in Fig.5-2(c), the edge detector would send a “dn” signal to the UP/DN decision logic. Contrarily, if a data transition occurs between the second and third sampling phases, as shown in Fig.5-2(b), the edge detector would send an “up” signal to the UP/DN decision logic.

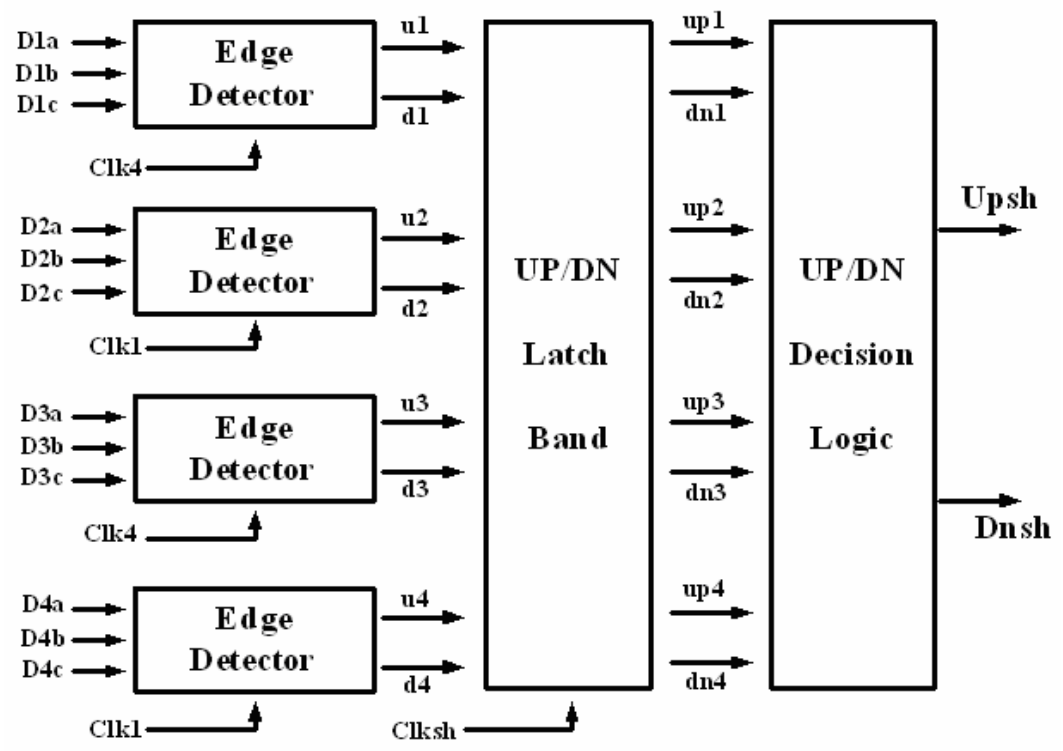
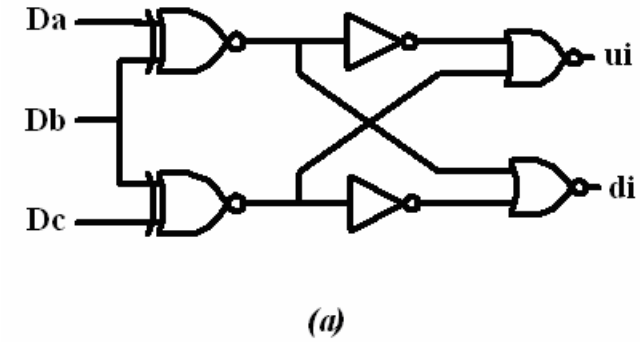


Fig.5-7 The block diagram of control logic



(a)

Da	Db	Dc	ui	di
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	0

(b)

Fig.5-8 (a) The circuit of the edge detector and (b) its truth table

The function of the UP/DN decision logic block is to compare the number of the upi and dni signals generated from the previous four sets of edge detector circuit. If the number of the upi signals is larger than the dni signals and least, simultaneously, the output signal Upsh will be set high. Contrarily, if the number of the dni signals is at least two and larger than the upi signals, Dnsh signal will be set high. Therefore, it must satisfy

$$Upsh = up1 \cdot up2 + up1 \cdot up3 + up1 \cdot up4 + up2 \cdot up3 + up2 \cdot up4 + up3 \cdot up4 \qquad \textbf{(5-1)}$$

$$Dnsh = dn1 \cdot dn2 + dn1 \cdot dn3 + dn1 \cdot dn4 + dn2 \cdot dn3 + dn2 \cdot dn4 + dn3 \cdot dn4 \qquad \textbf{(5-2)}$$

According to the UPsh and DNsh signal, the phase shifter will send the control signals to the phase selector band to adjust the sampling clock phases. This calibration of phase between data stream and sampling clocks would continue until no transition is detected within data information sets. And, both the Upsh and Dnsh signals would be kept low to maintain the phase condition of the sampling phases. At the same time, the tracking system is locked. In order to leave larger timing margin for logic operation of edge detectors and to alleviate operation speed requirement of the UP/DN decision, a signal latch band is adopted.

5.5 Phase Shifter

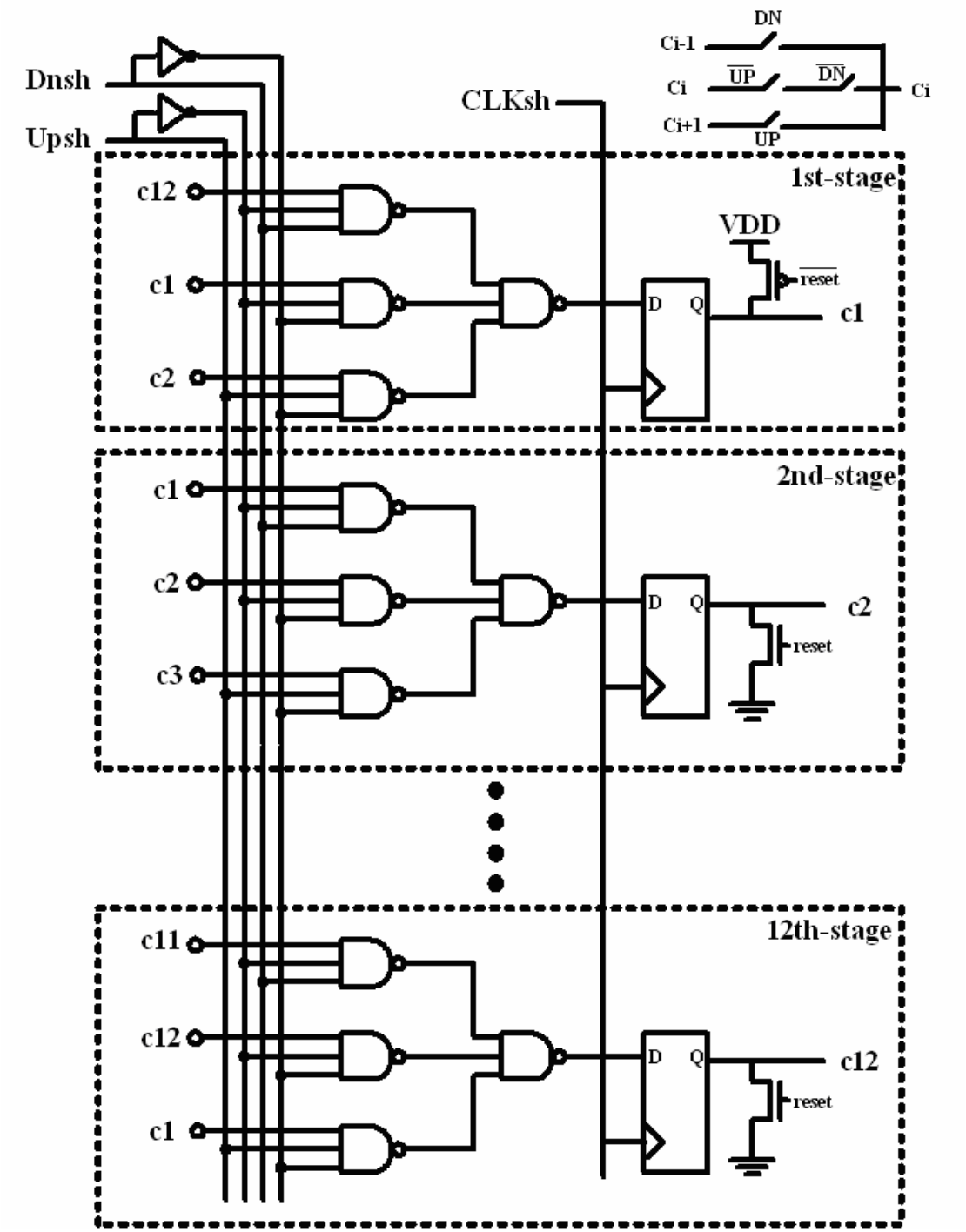


Fig.5-9 The phase shifter

As shown in Fig.5-9, the phase shifter is actually a cyclic shifter register with 12 stages. The twelve signals, c1~c12, would be sent to phase selector band to adjust correct phase, and feed themselves into phase shifter as input signals. Phase shifting right or left is determined by input signals, Upsh and Dnsh. Initially, only c1 is precharged to high from reset signal. When the trigger source CLKsh rising edge comes, the output of the previous stage will be set to high if Upsh is high and Dn is low. On the contrary, the output of the next stage will be high if Upsh is low and Dn is high. When Upsh and Dnsh are both low, the output value will be maintained, and selected reference clock phase is hold. In order to get right data in the next cycle, the trigger signal, CLKsh, of the phase shifter that come form the PLL output clock should be divided.

5.6 Phase Selector

Fig.5-10 shows the implementation of phase selector circuits, where c1 through c12 are the input signals from the phase shifter, clk1 through clk12 are from the outputs of 6 stages VCO of PLL. The output signals, sampler clk1 through sampler clk6, are the sampling phases used for the six input samplers. They both are based on pseudo-NMOS NAND type architectures. For example, when c1 is high and other control codes are low, the output signals are generated by clk1, clk3, clk5, clk7, clk9, and clk11. If the sampling clocks are late as shown in Fig.5-2(b), the system will shift the clocks left one unit time step, one-sixth bit time. Then, c1 is discharged to low and c12 is charged to high in order to pass clk12, clk2, clk4, clk6, clk8, and clk10 as output signals. Contrarily, if the sampling clocks are early as shown in Fig.5-2(c), the system will shift the clocks right one unit time step, one-sixth bit time. Then, c1 is

discharged to low and c2 is charged to high in order to pass clk2, clk4, clk6, clk8, clk10, and clk12 as output signals. Due to the cyclic property, we can make use of these twelve-bit control codes from the phase shifter to accomplish it. This calibration of phases between data stream and sampling clocks would continue until the system is locked.

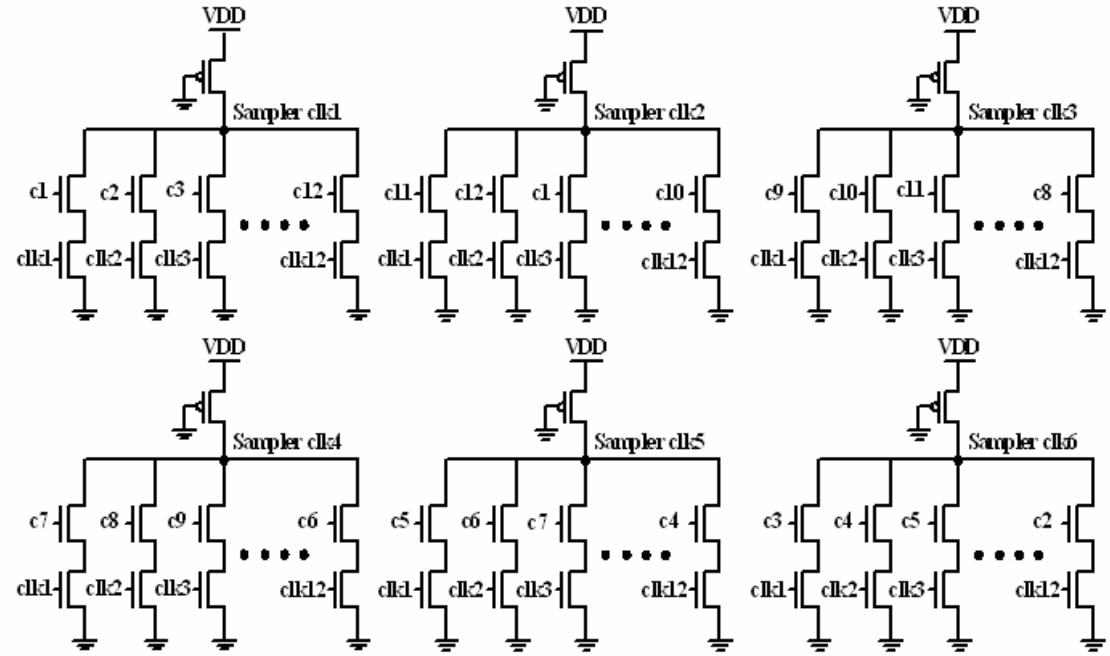


Fig.5-10 The phase selectors

5.7 Synchronizer

The basic building block of synchronizer is simply D Flip-Flop. The synchronizer is responsible for retiming all the sampled data. In order to align the timing of all the sampled data, a two-stage retiming D Flip-Flop is used as shown in Fig.5-11. The reason to use two-stage configuration is to increase the timing margins for the D Flip-Flop when the sampling phases are changed by the phase selector band.

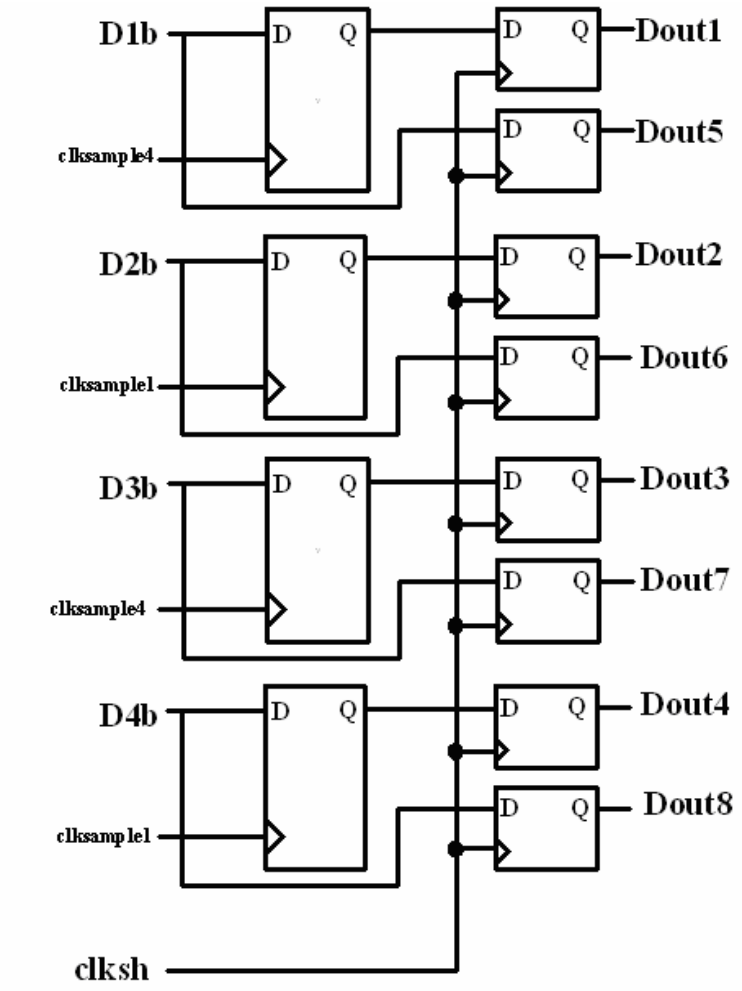


Fig.5-11 synchronizer

5.8 System Simulation Result

The circuit level simulations of the tracking receiver are made in order to ensure the proper operation under a specified skew amount between data and clock channels. The maximum data rate condition is demonstrated to make sure that this three-times oversampling method is sufficient for the loop to take a correct phase adjustment. Fig.5-12 shows the timing diagram of the system with the 600MHz (1.6675ns) operation frequency of PLL. And, the input data stream is assigned with an operation period of 1.67ns. Initially, the reset signal is high until 1.5us in order to check the

sampler clock generated from PLL is in lock. When the reset is low, the receiver tracking loop would adjust the p1 through p12 according to the sampled data in the control logic circuit. Although the output data corresponding to the input data is correct, the sampling position could be moved to better one, reducing the static timing offset to the center of data eyes. Because the period of input data stream is always longer than the sampling clock from PLL, the control signal dn would be set to high repeatedly. As shown in Fig.5-13, we connect the transmitter differential outputs and the receiver differential inputs. The receiver outputs, data2, data3, and data4, are three of the eight signals generated from PRBS in transmitter. According to the architecture of PRBS, data3 has to lag data2 one bit time.

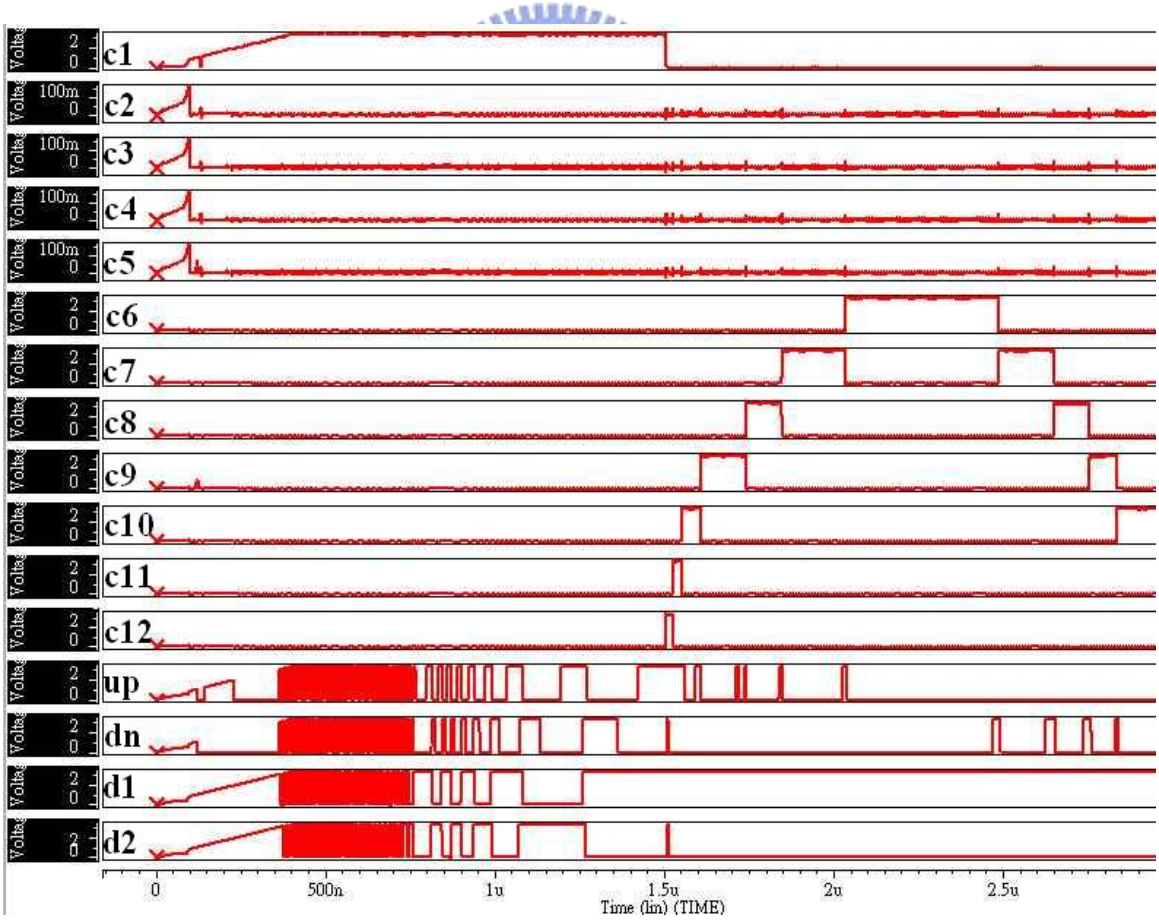


Fig.5-12 Receiver tracking loop simulation

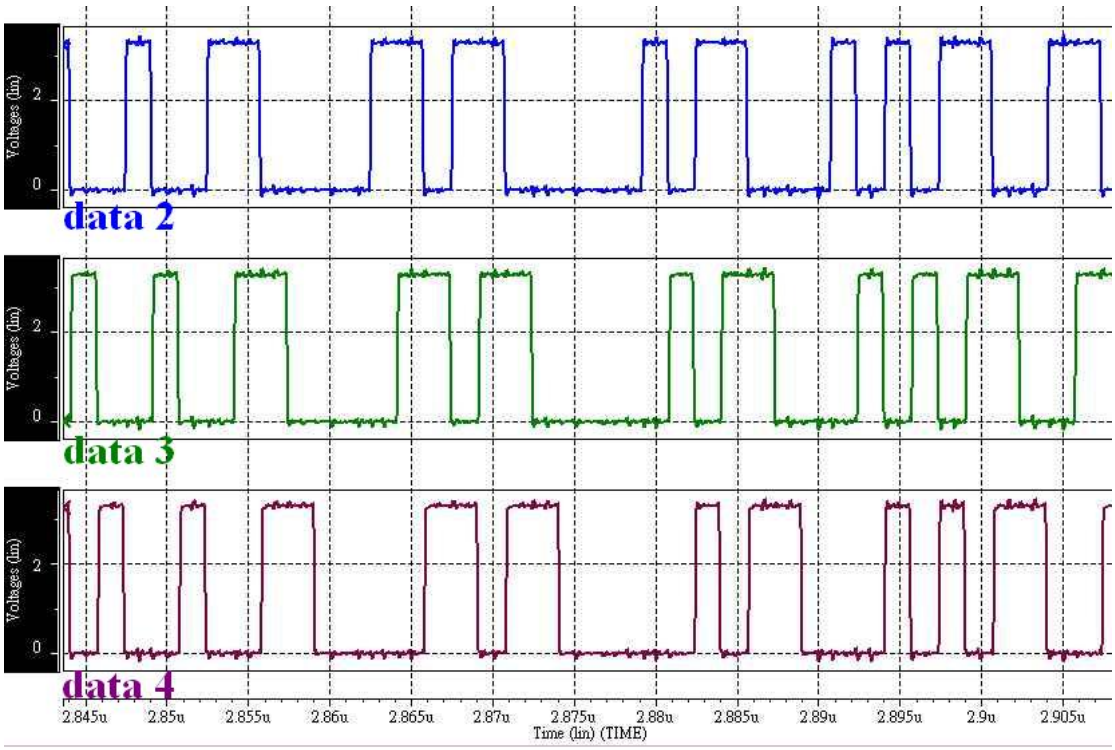
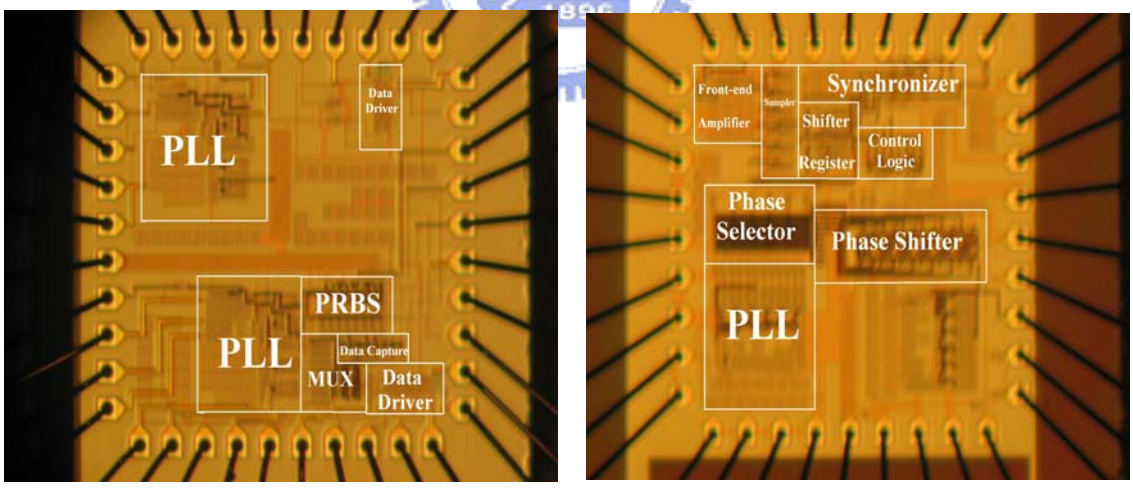


Fig.5-13 the data outputs of the transceiver

Chapter 6

Experimental Result

The transmitter and receiver are implemented in a 0.35um 2p4m CMOS process form TSMC. We will describe the measurement result of the transmitter and receiver. They also include the PLL described in chapter 3. Fig.6-1(a) shows the chip layout micrograph of the transmitter. In order to avoid influencing the node loading when it is measured, we copy the PLL and the Data Driver layout and set them in the corner of the chip for measurement single-handedly. And, Fig.6-1(b) depicts the chip layout micrograph of the receiver.



(a) **(b)**

Fig.6-1 chip layout micrograph of the transmitter (a) and the receiver (b)

Fig.6-2 is the measurement setup of the transceiver. The input clock f_{ref} is generated form a pulse generator (HP8133A) through a SMA connector. The output of

PLL is fed to a digital phosphor oscilloscope (TEK TDS754D). It is also monitored by a digitizing signal analyzer (TEK DSA601A) to evaluate the jitter performance. The differential serial-link output TX+ and TX- are fed to a digital phosphor oscilloscope (TEK TDS754D) and then we observe the data eye pattern. Finally, the receiver data outputs are also fed to a digital phosphor oscilloscope (TEK TDS754D) to check if this transceiver does work or not.

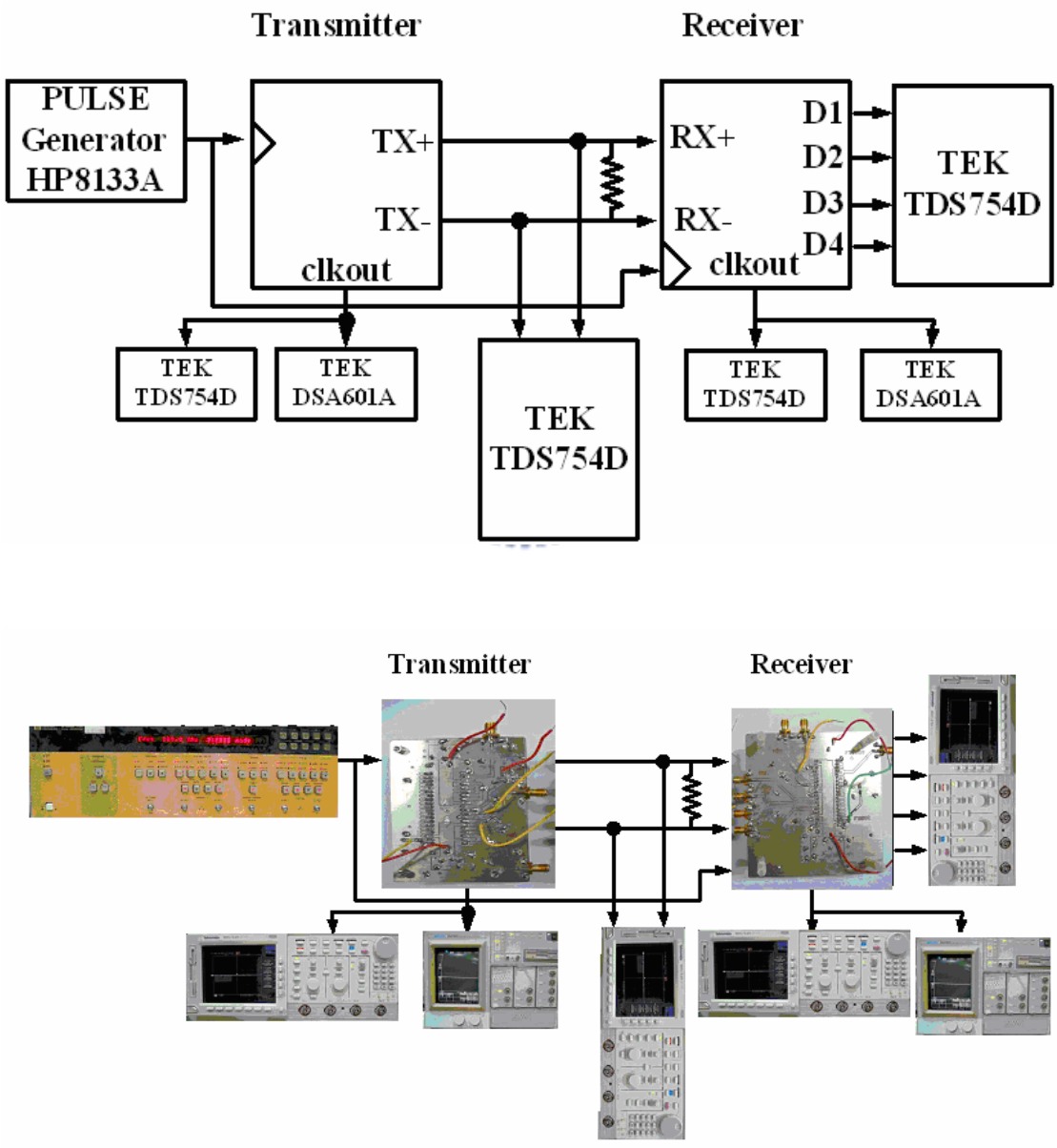


Fig.6-2 The measurement setup of the transceiver

6.1 Layout consideration

There are some special and important techniques need to be considered in our layout implementation to make sure that the circuits work correctly. First, in order to minimize the effect of substrate noise, the guard ring can be employed to isolate the sensitive sections from the substrate noise produced by other sections. And, the analog part utilizes its clean individual supply and ground to suppress the switching noise. Second, the effect of self-inductance must also be considered for input signals. Therefore, we use multiple wires to reduce overall inductance, as shown in Fig.6-3. Finally, on-chip capacitors must be used to lower supply-ground noise voltage.

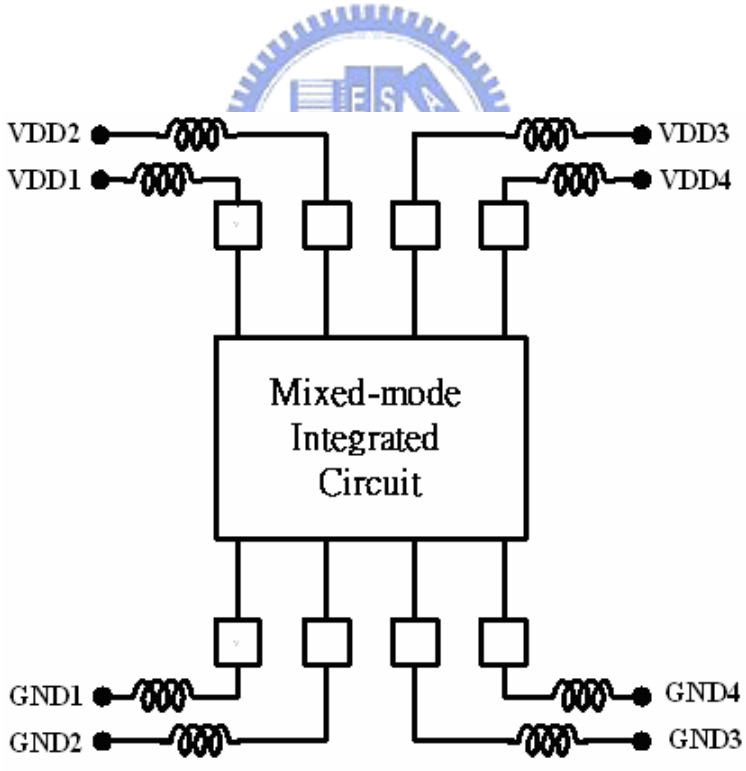


Fig.6-3 Use of multiple wires to reduce overall inductance

6.2 PLL Measurement Result

The transmitter PLL and receiver PLL used in this work are fabricated individually and also tested to determine the locked situation and the jitter performance. As shown in Fig.6-4, the input reference clock signal (1) at 75MHz is generated from a waveform generator (HP8133A) through a SMA connector. The feedback signal, f_{fb}(2), and clk4(3) are fed to an oscilloscope (TDS754D). In order to improve these outputs driving capability, we add some buffers between output signals and pads. That is why f_{fb} always lags the reference input signal(1). We use Tek DSA601A to measure PLL output jitter of r.m.s 10.76ps, peak-to-peak 84ps as in Fig.6-5. The output clock of the transmitter PLL at 150MHz is also shown in Fig.6-4. Fig.6-6 shows the CLK3(2) and CLK4(3) output signals of the receiver PLL. And, Fig.6-7 illustrates the measure rms and peak-to-peak jitters of 600MHz output clock of the receiver PLL.

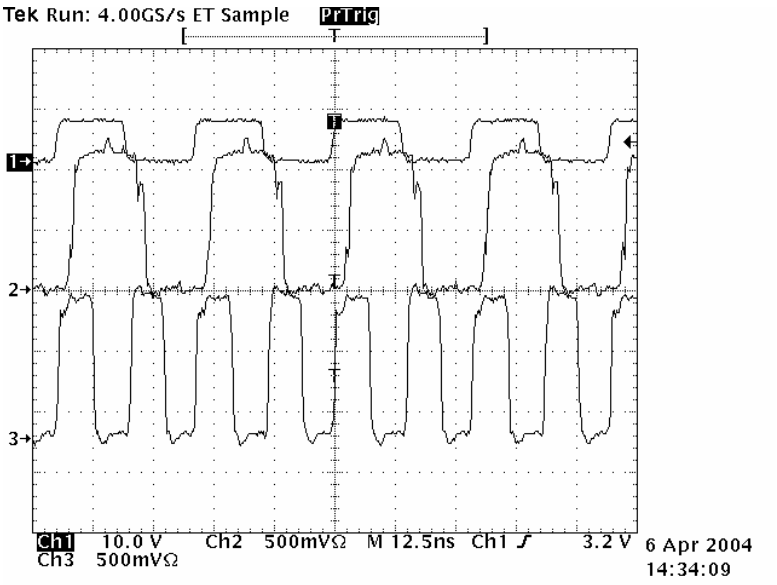
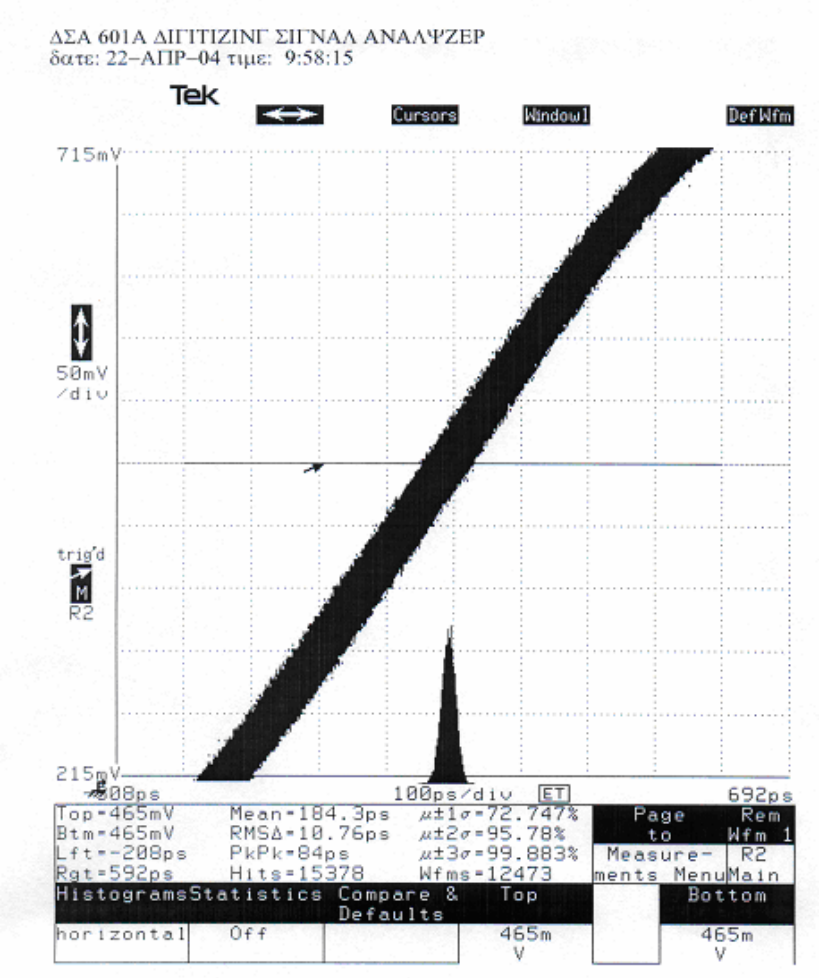


Fig.6-4 The TX PLL waveforms of f_{fb} (75MHz) and CLK4 (150MHz)



. **Fig.6-5 Measured jitter histogram of clk4 signal under 150MHz**

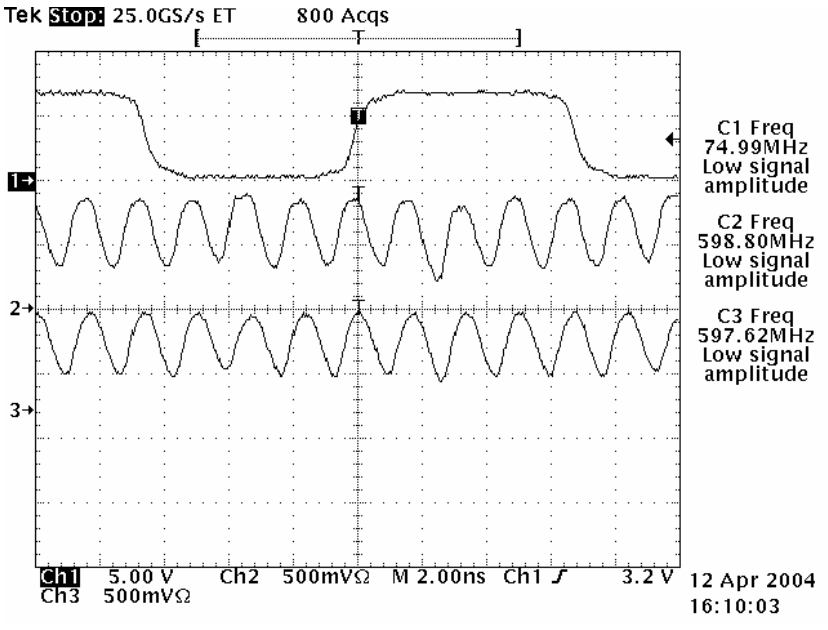


Fig.6-6 The RX PLL waveforms of CLK3 and CLK4

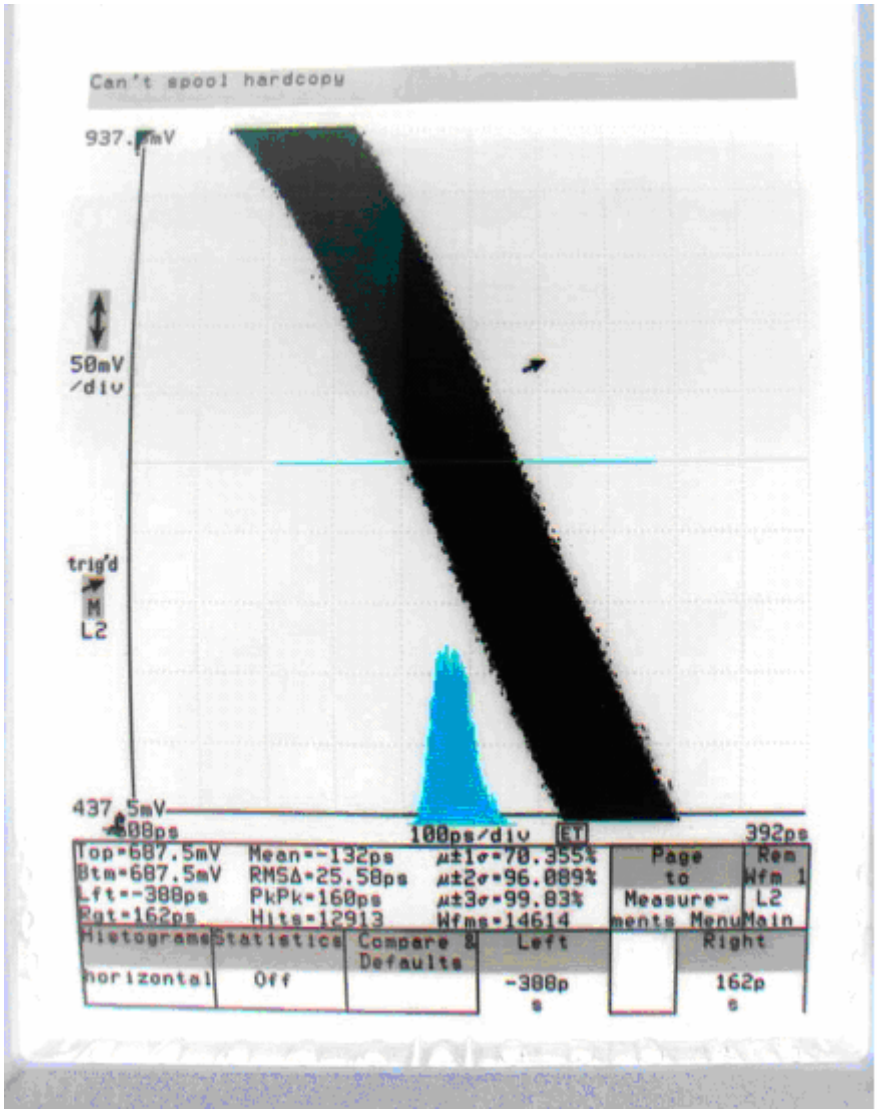


Fig.6-7 Measured jitter histogram of RX PLL output signal under 600MHz

6.3 TX System Measurement Result

Fig.6-8, Fig.6-9, and Fig.6-10 are the eye diagrams of the data driver differential outputs at different data rate. The random data input stream is generated from a pulse generator (HP8133A) through a SMA connector. And, we use an oscilloscope (Tek TDS754D) to observe these outputs and their eye diagrams.

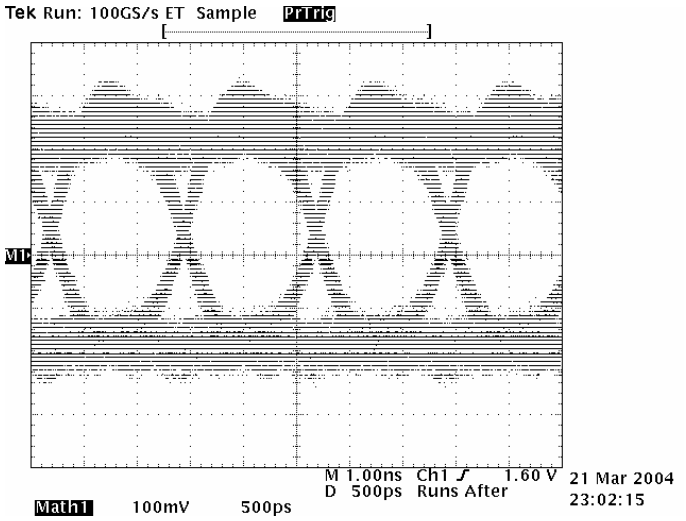


Fig.6-8 The eye diagram of the data driver differential outputs at 800Mbps

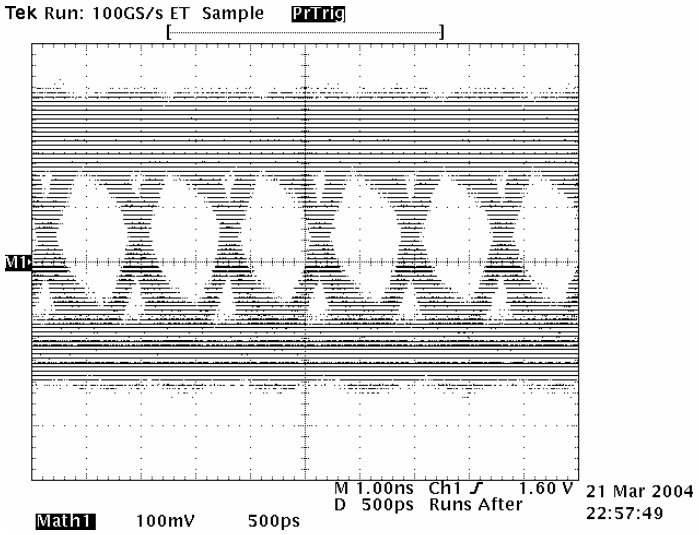


Fig.6-9 The eye diagram of the data driver differential outputs at 1.2Gbps

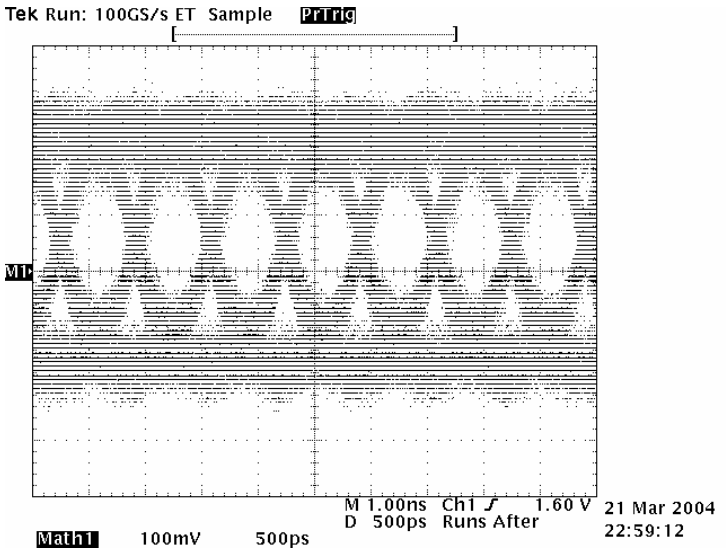


Fig.6-10 The eye diagram of the data driver differential outputs at 1.5Gbps

Fig.6-11 ~ Fig.6-13 are the eye diagrams of the transmitter differential outputs at different data rate. In order to check if the receiver in this these does work or not easily, the data0 of multiplexer in transmitter is always set to high. Because the external trigger source in oscilloscope is transmitter input reference clock, it will result in a "1" occurrence in particular cases shown in Fig.6-12, Fig.6-13, and Fig.6-14. We can compare it with the simulation result shown in Fig.6-11. We use an oscilloscope (Tek TDS754D) to observe these outputs. The performance summary of transmitter is listed in Table.6-1.

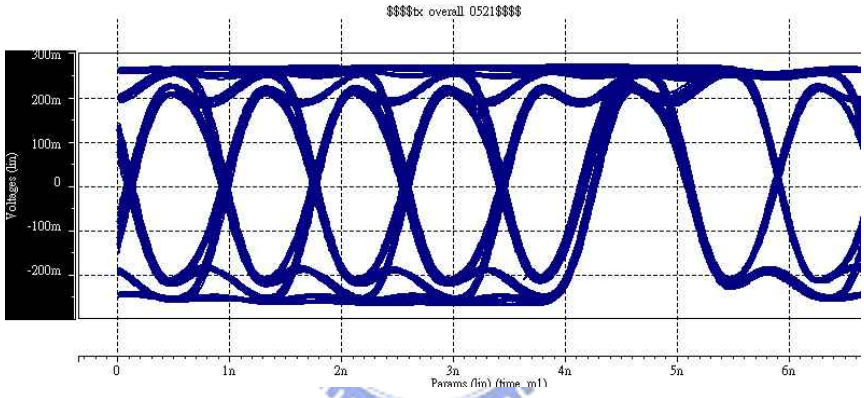


Fig.6-11 The simulation eye diagram of the transmitter at 1.2Gpbs

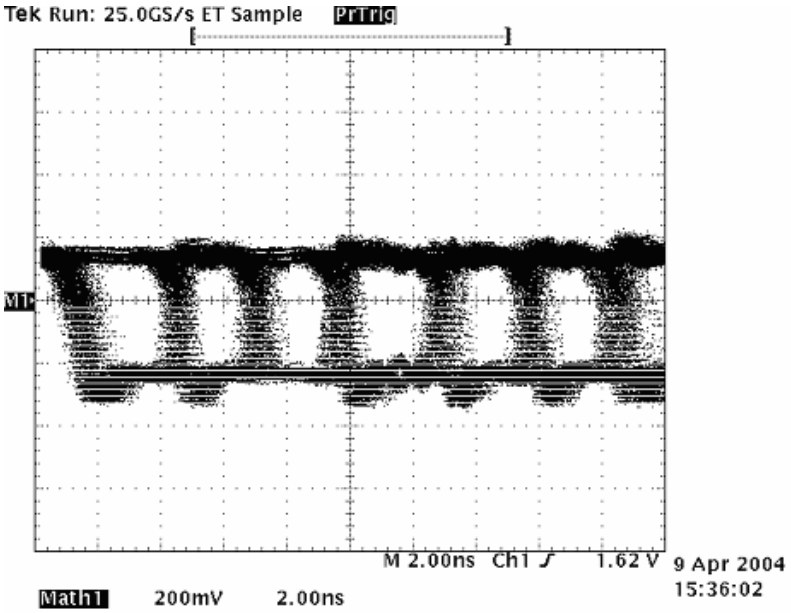


Fig.6-12 The eye diagram of the transmitter differential outputs at 560Mbps

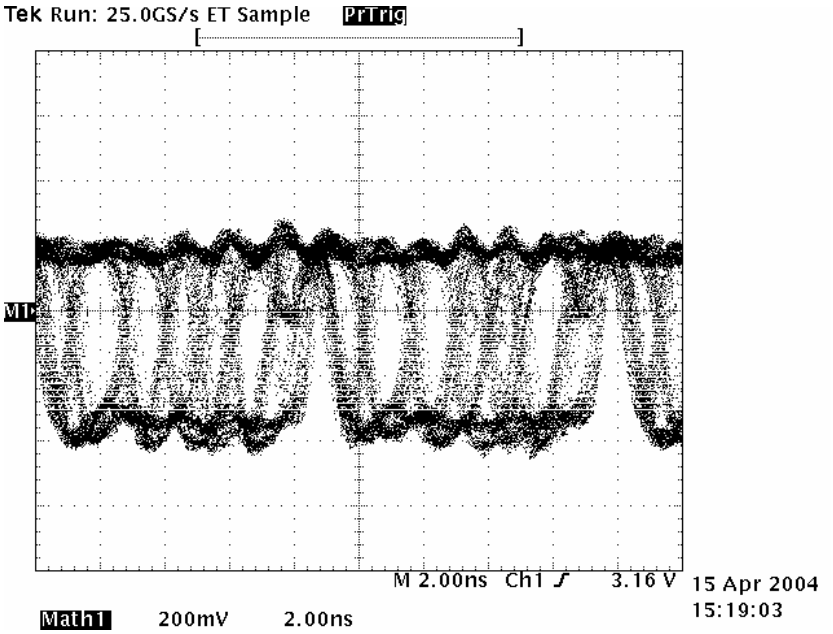


Fig.6-13 The eye diagram of the transmitter differential outputs at 880Mbps

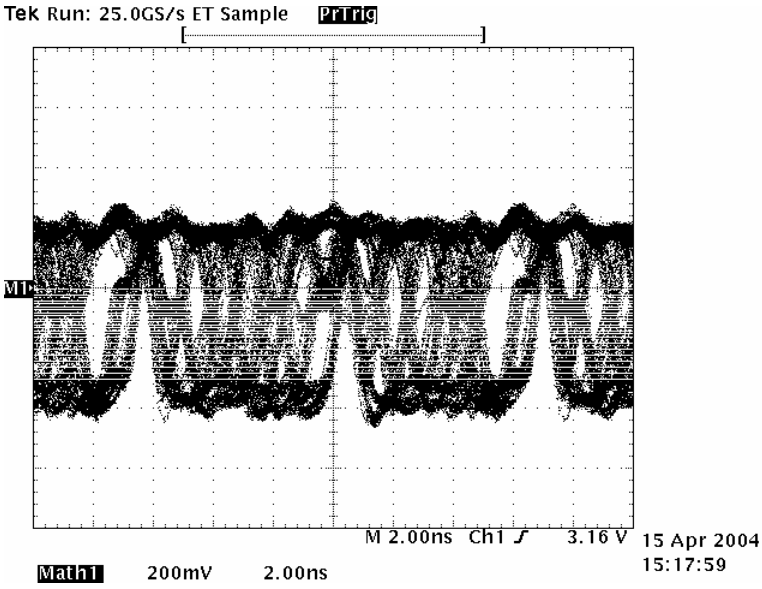


Fig.6-14 The eye diagram of the transmitter differential outputs at 1.2Gbps

As shown in Fig.6-15~6-19, we measure the transmitter chip again without package. We reduce the package partial self-inductances for the power and ground paths. Lower inductance can be achieved by adding power and ground pins and by shortening the length of the power and ground path. Adding capacitors to the circuit enables rapidly changing current components to be supplied close to the circuits. In

conclusion, we have to eliminate the package inductance entirely by directly attaching the chip to the oscilloscope. We can still compare these illustrations with those shown in Fig.6-12~Fig.6-14.

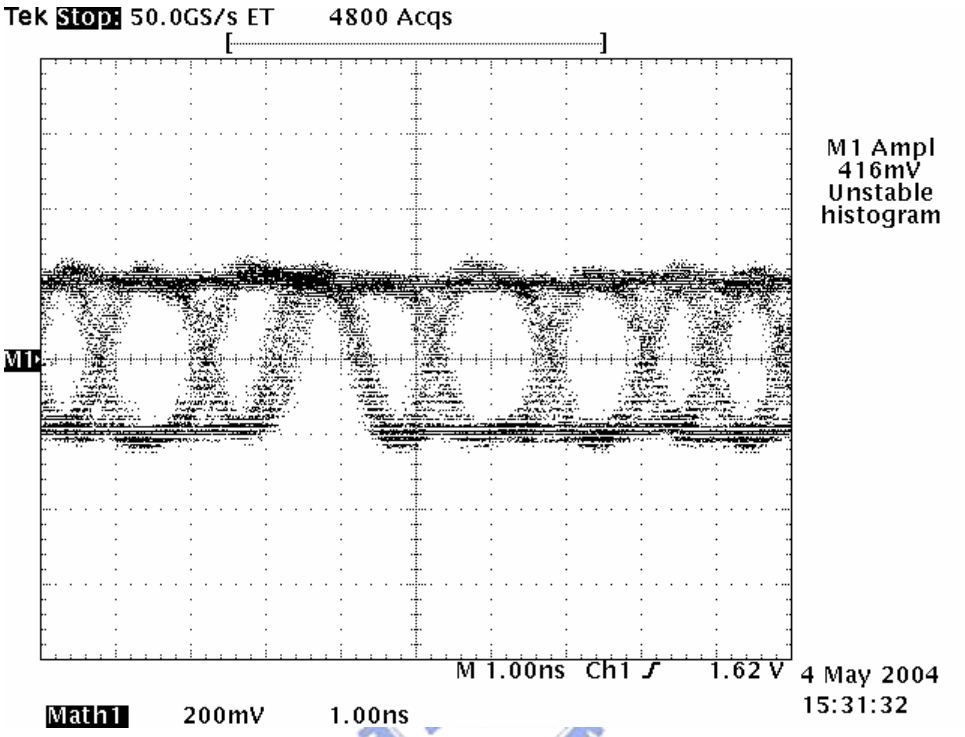


Fig.6-15 The eye diagram of the transmitter differential outputs at 560Mbps

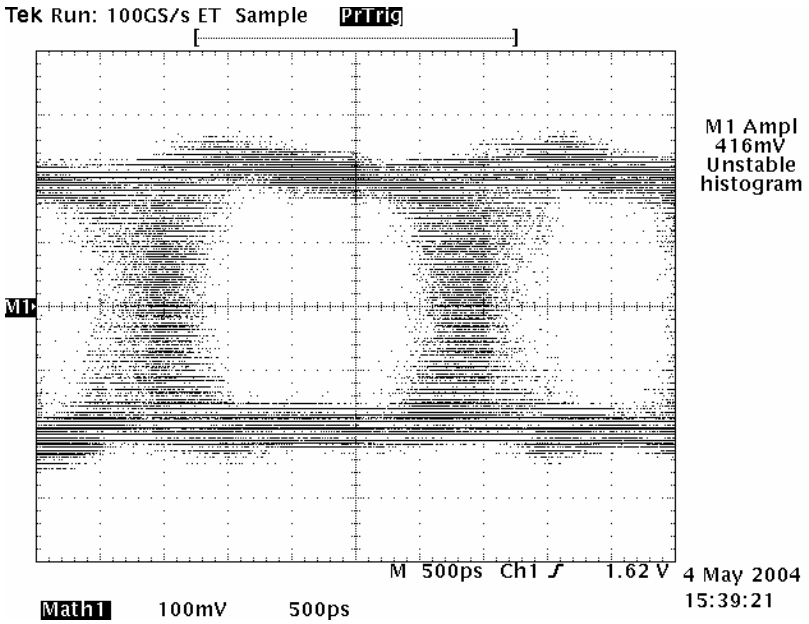


Fig.6-16 The eye diagram of the transmitter differential outputs at 624Mbps

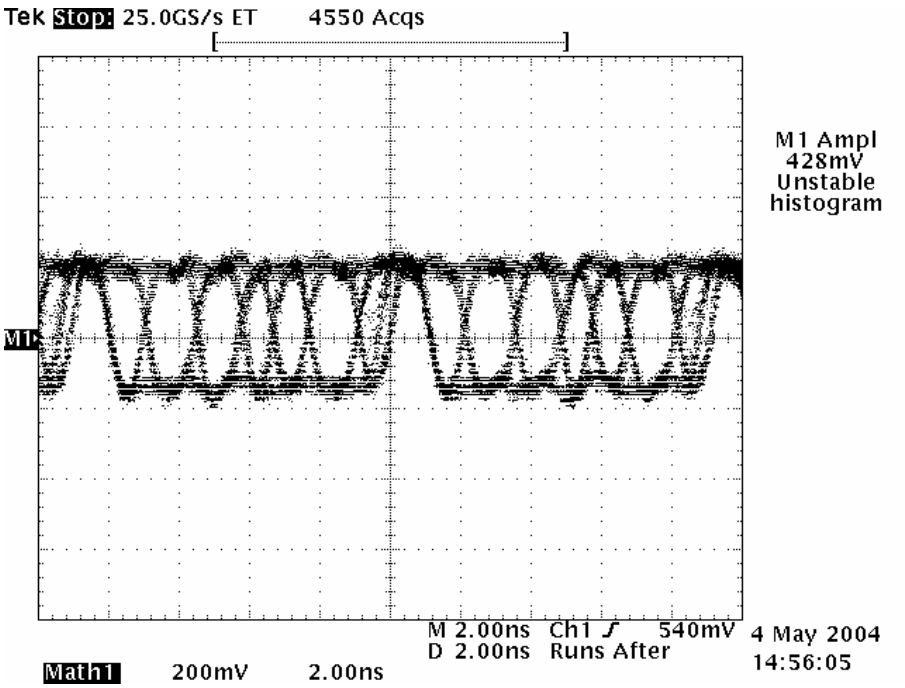


Fig.6-17 The eye diagram of the transmitter differential outputs at 880Mbps

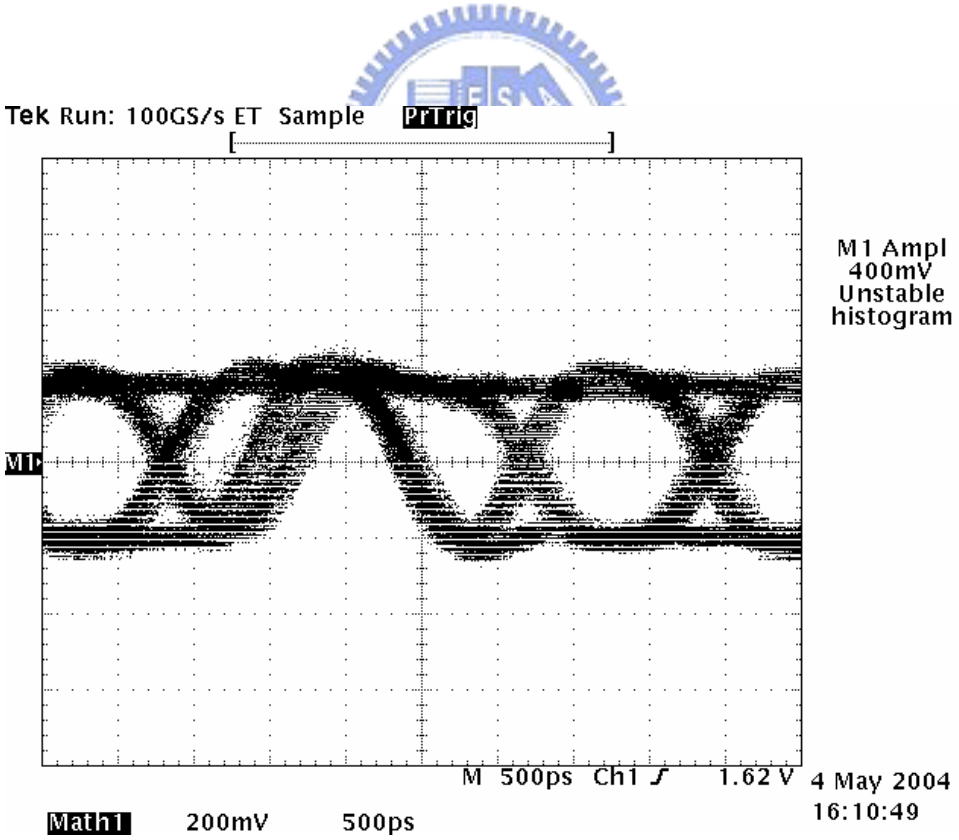


Fig.6-18 The eye diagram of the transmitter differential outputs at 1.12Gbps

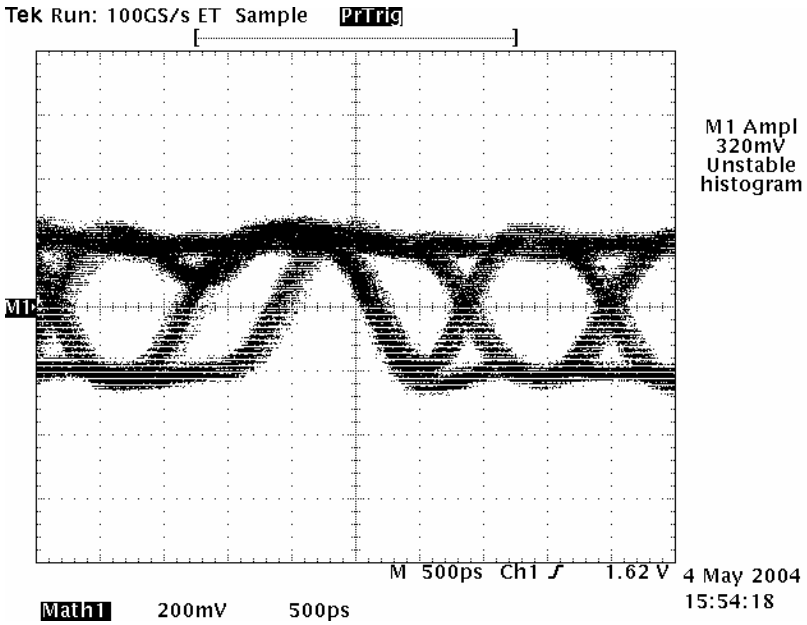


Fig.6-19 The eye diagram of the transmitter differential outputs at 1.2Gbps

Technology	**0.35um 2p4m TSMC**	**Chip Area**	**1600 x 700 um^2**
Supply Voltage	**3.3v**	**Power consumption**	**128 mW**
Input Frequency	**75MHz**	**TX Data Rate**	**1.2Gbps**

Table.6-1 The performance summary of transmitter

6.4 RX System Measurement Result

Fig.6-20(a) ~ Fig.6-20(d) show the data output waveforms of receiver, including Dout2(2), Dout3(3) and Dout4(4) from synchronizer. As shown in Fig.6-20(a), the input reference clock operates at 55MHz. As shown in Fig.6-20(b), the input reference clock operates at 75MHz. As shown in Fig.6-20(c)(d), the input reference clock operates at 65MHz. These signals are generated by PRBS in transmitter chip and fed

to receiver through the 50cm cable. According to PRBS structure, the Dout4 is always followed by the Dout3, the Dout3 is always followed by the Dout2, and so on. But there are some errors in the three data outputs caused by transmitter terrible data jitter. We use an oscilloscope (Tek TDS754D) to observe these outputs. The performance summary of receiver is listed in Table.6-2.

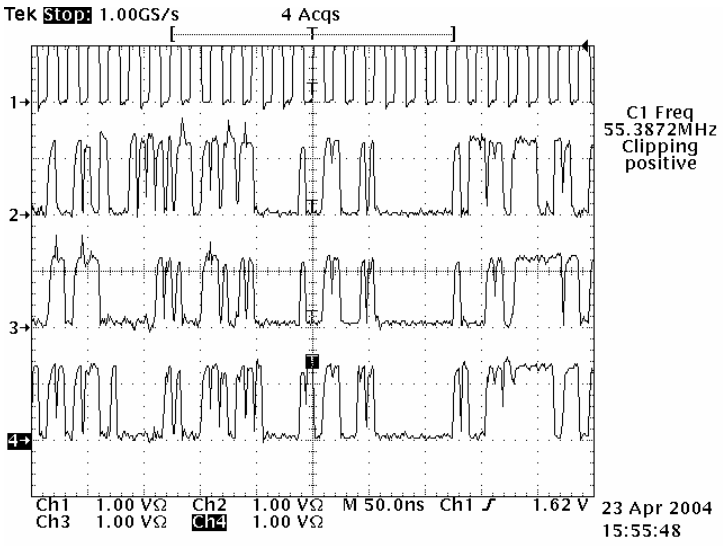


Fig.6-20(a) The data output waveforms of receiver

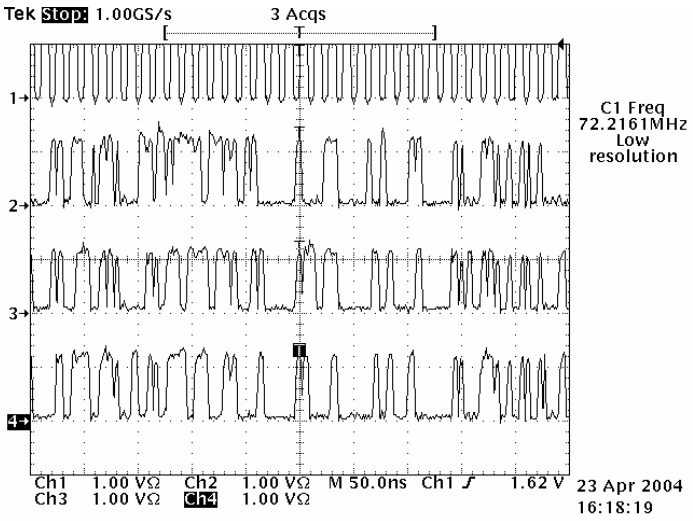


Fig.6-20(b) The data output waveforms of receiver

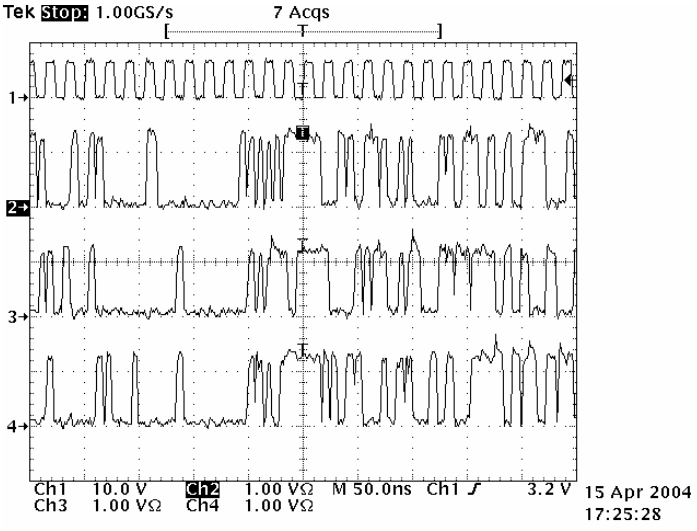


Fig.6-20(c) The data output waveforms of receiver

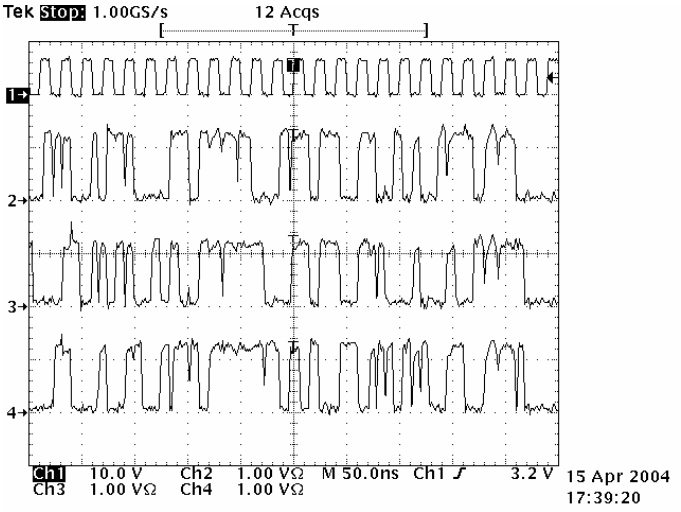


Fig.6-20(d) The data output waveforms of receiver

Technology	**0.35um 2p4m TSMC**
Supply Voltage	**3.3v**
Input Frequency	**75MHz**
Chip Area	**1800 x 1350 um^2**
Power consumption	**960 mW**
TX Data Rate	**1.2Gbps**

Table.6-2 The performance summary of receiver

Chapter 7

Conclusion and Future work

7.1 Conclusion

In this thesis, we had completed the design of the transceiver based on RSDS interface including a transmitter and a tracking data recovery receiver. It is a way to communicate data using a very low voltage swing (about 200mV) differentially over two printed circuit board (PCB) traces or a balanced cable. We have devoted to design a transceiver with the data rate at 1.2Gbps. And, the transceiver is fabricated in 0.35um 2P4M process. Transmitter is composed of PRBS, eight-phases PLL, 8-to-1 multiplexer and data driver. The input reference of eight phases PLL is 75MHz; it outputs a uniformly distributed 150MHz clock. The PLL is composed of Phase Detector, Charge Pump, Loop Filter, Voltage Control Oscillator and a divided-by-two. Eight phases PLL output a uniform distributed clock for multiplexer to convert parallel data to serial data. The transmitter drives the serial data on to the bus. Receiver is composed of a comparator with hysteresis, tracking data recovery system with three times oversampling technique. It uses the comparator to amplify incoming small signal to full swing, and tracking data recovery system to sample data correctly. Finally, the receiver converts serial data to eight parallel data channel.

7.2 Future Work

The increasing demand for data bandwidth in networking has driven the development of high-speed and low-cost serial link technology. In order to achieve higher data rate, the serial interfaces must recover clock and data reliably from a single data stream, reduce transmitter jitter and open its data eye, increase receiver jitter tolerance, reduce clock data skew. We can also use pre-emphasis which has more efficiency of swing wasting.

REFERENCES

[1]. Muneo FuKaishi, Kazuyuki Nakamura, "A 4.25-Gb/s CMOS Fiber Channel Transceiver with Asynchornous Tree-Type Demultiplexer and Frequency Conversion Architecture," *IEEE journal of solid-state circuit*, pp. 2139-2147, DECEMBER. 1998.

[2]. IEEE Standard for Low-Voltage Differential Signals for Scalable Coherent Interface (SCI), Microprocessor and Microcomputer Standards Committee of the IEEE Computer Society, *IEEE Standards Board,* IEEE std 1596.3-1996

[3]. The Low-Voltage Differential Signals Applications, http://www.national.com/appinfo/lvds

[4]. National Semiconductor Corp, "Reduced Swing Differential Signaling (RSDS^{TM}) Specification," Revision 0.95, May 2001

[5]. John Teifel and Rajit Manohar, "A High-Speed Clockless Serial Link Transceiver," *IEEE journal of solid-state circuit*, Ithaca, NY 14853, U.S.A. 2003.

[6]. Stephen H. Hall, Garrett W. Hall and James A. McCall, "High-Speed Digital System Design : A Handbook of Interconnect Theory and Design Practices," John Wiley & Sons, INC. 2000

[7]. T. Gabara, "Digital transistor sizing techniques applied to 100K ECL CMOS output buffers," *Proceedings of the Sixth Annual IEE International ASIC Conference*, pp. 456-459, Oct. 1993.

[8]. Joonsuk Lee and Beomsup Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1137-1145, Aug. 2000.

[9]. G.B Lee, P.K Chenand L. Siek, "A CMOS Phase Frequency Detector for Charge

Pump Phase-Locked Loop," *IEEE J. Solid-State Circuits*, pp. 601-604, 1999.

[10]. M. Soyuer and R.G. Meyer, "Frequency Limitation of a Conventional Phase-Frequency Detector," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1019-1022, Aug. 1990.

[11]. I. A. Young, J.K. Greason, And K.L. Wong,"A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, pp.1599-1607, Nov. 1992.

[12]. J. G. Maneatis, "Precise Delay Generation Using Coupled Oscillator," *IEEE J.Solid-State Circuits*, vol. 28, no. 12, pp. 1273-1282, Dec. 1993.

[13]. J. G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, Nov. 1996.

[14]. I. Young et al., "A PLL clock generator with 5 to 110MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599-1607, Nov. 1992.

[15]. Jiren Yuan, and Christer Svensson, "High-Speed CMOS Circuit Technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62-70, Feb. 1989.

[16]. Behzad Razavi, *RF Microelectronics*, Prentice Hall, Inc. 1998.

[17]. Frank Herzel and Behzad Razavi, "A Study of Oscillator Jitter Due to Supply and Substrate Noise," *IEEE Trans. on Circuits and Systems*, vol. 46, no. 1, pp. 56-62, Jan. 1999.

[18]. Thomas H. Lee and Ali Hajimiri, "Oscillator Phase Noise: A Tutorial," *IEEE Trans. on Circuits and Systems*, vol. 35, no. 3, pp. 326-336, Mar. 2000.

[19]. J. P. Hein, and J. W. Scott, "z-Domain Model for Discrete-Time PLL's," *IEEE Trans. on Circuits and Systems*, vol. 35, no. 11, pp. 1393-1400, Nov. 1988.

[20]. Ming-Ju Edward Lee, William J. Dally and Partick Chiagn, "Low-Power Area

Efficient High-Speed I/O Circuit Techniques," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1591-1599, Nov. 2000.

[21]. Ming-Ju Edward Lee, William Dally and Patrick Chiang, "A 90mW 4Gb/s Equalized I/O Circuit with Input Offset Cancellation," in *IEEE ISSCC Dig. Tech. Papers*, 2000, pp. 252-253.

[22]. H.W. Johnson and M. Graham, High-Speed Digital Design, A Handbook of Block Magic. Englewood Cliffs, NJ : Prentice Hall, 1993.

[23]. Andrea Boni, Andrea Pierazzi, and Davide Vecchi, "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-um CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 706-711, APRIL. 2001.

[24]. C. K. K. Yang and M. A. Horowitz, "A 0.8-um CMOS 2.5Gb/s oversampling receiver and transmitter for serial links", *IEEE Journal of Solid-State Circuits*, vol.31, pp.2015-2023, December 1996.

[25]. C. K. K. Yang and R Farjad-Rad, " A 0.5-um CMOS 4.0-Gbit/s serial link 77 transceiver with data recovery using oversampling", *IEEE Journal of Solid-State Circuits*, vlo.33, pp.713-722, May 1998.

[26]. A. Boni and A. Pierazzi, "LVDS I/O Interface for Gb/s-per-pin operation in 0.35-um CMOS," *IEEE Journal of Solid-State Circuits*, vol.36, pp.706-711, April 2001.

[27]. J. Montanaro et. al. "A 160-MHz, 32-b, 0.5W CMOS RISC Microprocessor," *IEEE Journal of Solid State Circuits,* vol. 31, no. 11, pp. 1703-1714, Nov. 1996.

[28]. K. Lee and Y. Shin, "1.04 Gbd low EMI digital video interface system using small swing serial link technique", *IEEE Journal of Solid-State Circuits*, vol.33, pp.816-823, May 1998.

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