2.4/5.8-GHz 雙頻帶正交相位壓控振盪器之製作

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摘要

在本論文中，我們分別針對於注入鎖定式振盪器及正交相位振盪器的基本操作原理提出說明，並且透過電路的實作及量測的結果來展示。

注入鎖定式振盪器的部份，我們製作一個 11-GHz 低消耗功率除數為二的注入鎖定式除頻器(ILFD)。這個除頻器藉由並連電感來提升電路節點的阻抗以提升可除頻率範圍。根據量測的結果，這個電路操作在 1.2 V 的供應電壓時，會消耗 1.2 mA。當注入訊號的功率是-10dBm，則可以除 2 的頻率範圍是 9.2-9.7 GHz (即 500 MHz 操作頻率範圍)。不使用並聯電感的技巧時，我們量到的操作頻率範圍是 200 MHz，相較之下，並聯電感的技巧對於操作頻率範圍有 50%以上的提升。

正交振盪器的部分，我們藉由正交相位振盪器本身所具備的頻率調變特性製造一個 5.2/5.8 GHz 雙模態的正交相位壓控振盪器。經由實際的量測得到的振盪頻率範圍是 5.9-6.5 GHz，而頻率調變增益(KVCO)大約是 180MHz/V。這個電路操作於 1.5V 供應電壓源，所須的最大操作電流是 23mA。此正交振盪器輸出

的相位誤差為 34°，而距離載波訊號 1MHz 處的相位雜訊為-109dBc/Hz。

透過正交相位振盪器以及除頻器的整合，進一步實現 2.4/5.8 GHz 雙頻段的正交振盪訊號源。QVCO 的直流偏壓為 1.8V，消耗電流 23mA，而除頻器的直流偏壓為 1.2V，消耗電流 4mA。振盪頻率的量測結果，在 QVCO 端為 4.1-5.2 GHz 其相位雜訊為-113 dBc/Hz @1MHz offse 而正交訊號的相位誤差為 47°，經過除頻器的降頻之後，由除頻器端可以再輸出 1.96-2.5 GHz 的振盪訊號，其相位雜訊為 -121 dBc/Hz @1MHz offse。

最後，我們說明如何應用 12-GHz 的正交相位壓控振盪器來實現 24-GHz 而且具有差動輸出的頻率推進式(Push-Push)壓控振盪器。該電路所須的直流偏壓為 1.8V，消耗電流 18mA。模擬結果顯示，該電路的輸出功率為-10dBm，且具有 24-25 GHz 的可調頻率範圍，相位雜訊的模擬結果為-104dBc/Hz @1MHz offset。

以上所提的四個電路都是使用 0.18mm CMOS 製程，並於聯華電子公司(UMC)製作晶片。

Implementation of 2.4/5.8-GHz Dual-Band Quadrature Voltage-Controlled Oscillator

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ABSTRACT

In this thesis, we discuss the fundamentals of injection locking oscillator (ILO) and quadrature voltage controlled oscillator (QVCO). Then circuit design is implemented and verified by measurements.

Based on the techniques of injection locking, an 11-GHz low power injection locked frequency divider (ILFD) is fabricated using inductive shunt peaking locking range enhancement. The frequency division ratio is two. Measurement results shows that this ILFD consumes 1.2mA from a 1.2V supply and the input dividable frequency range is 9.2-9.7 GHz (i.e., 500-MHz locking range) under -10dBm injection power. On the other hands, the locking range is only 200 MHz without shunt peaking. This work achieves more than 50% improvement in locking range.

On the part of quadrature oscillator, a 5.2/5.8-GHz Dual Mode Quadrature Voltage Controlled Oscillator (QVCO) with novel frequency tuning technique is implemented. Measurement results show that the QVCO consumes less than 23mA from 1.5 V supply and the output frequency is 5.9-6.5GHz. The KVCO is around 180 MHz/V facilitated by the novel frequency tuning mechanism. I/Q output phase has a 34° deviation from perfect quadrature (90°) and the phase noise at 1MHz offset from

the carrier is -103dBc/Hz.

With the dual mode QVCO being followed by frequency divider, a 2.4/5.8 GHz dual band quadrature VCO is realized and measured. The current consumption are 23 mA from 1.8 V supply for QVCO circuit and 4 mA from 1.2 V for frequency divider circuit. The output frequency of the QVCO can be tuned from 4.1 to 5.3 GHz, the phase noise of the QVCO is -113 dBc/Hz @1MHz offset, and the I/Q output phase of the QVCO deviates from perfect 90° (quadrature) by 47°. After frequency been divided by 2, the output frequency of the frequency divider is in the range of 1.96-2.5 GHz with a -121dBc/Hz of phase noise.

Finally, we discuss how to design a fully differential output 24-GHz push-push VCO from a 12-GHz QVCO. As indicated by the simulation results, the current consumption is 18 mA from 1.8 V supply, the output power at the push-push port is about -10 dBm and the phase noise is -104 dBc/Hz @1MHz offset. Output frequency can be tuned in the range of 24-25 GHz.

All these circuits are fabricated in UMC 0.18μm CMOS technology.

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CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER 1

Introduction

1.1 Wireless Communications

With the facility of wireless communication systems, such as mobile phone, Global Positioning System (GPS) and Wireless Local Area Network (WLAN), so that people catch information beyond the restriction of motion and position. A sketch of wireless communication system is made up of RF transceivers including antenna, mobile stations, base stations for the specified communication standard, as shown in Fig. 1.1, where the public switched telephone network (PSTN) and local area network (LAN) are used for the interconnection between the base stations for the cellular system and wireless LAN respectively.

Antenna, mobile stations and base stations are used for the reception and transmission of radio signals and perform signal modulation/ demodulation. In more detail, mobile stations or base stations include transmitter, receiver, and DSP circuit.

A simple Zero-IF down-conversion receiver architecture using I/Q downconversion is shown in Fig.1.2 [1.1], where a stable LO carrier signal is generated by frequency synthesizer. Fig. 1.3 shows a phase-locked loop based synthesizer whose frequency can be selected by the modulus selection signal. In this architecture of receiver, the external high Q image reject filter for heterodyne receiver will no longer be needed in zero IF (or direct conversion) and low IF receiver, so that Zero/Low IF receiver architecture improves the integratability of circuits [1.1] and

becomes popular for the sake of their high degree integratability and low cost. On the other hand, the upper and lower sideband of the received signal may be different, so that the downconversion with single sine tone will make the signal spectrum in the negative frequency part to overlap with the positive frequency part, as depicted in Fig.1.4. For this reason, I/Q downconversion needs be performed to make the RF signal be multiplied with only the positive frequency to avoid the overlapping of the signal spectrum when downconverted to baseband, as depicted in Fig.1.5.

For specific communication applications, the details of their communication feature need be defined as a communication standard, so that circuit designers follow this standard to develop the communication circuits properly. Generally speaking, a communication standard can be divided into two parts, i.e., digital part and physical layer part. In digital part, the communication protocol, modulation method, and DSP algorithms are defined. In physical (PHY) layer part, the requirements for RF front-end circuit are defined. Table.1.1 shows some key features of communication standards for WLAN and Cellular Phone [1.2-1.3].

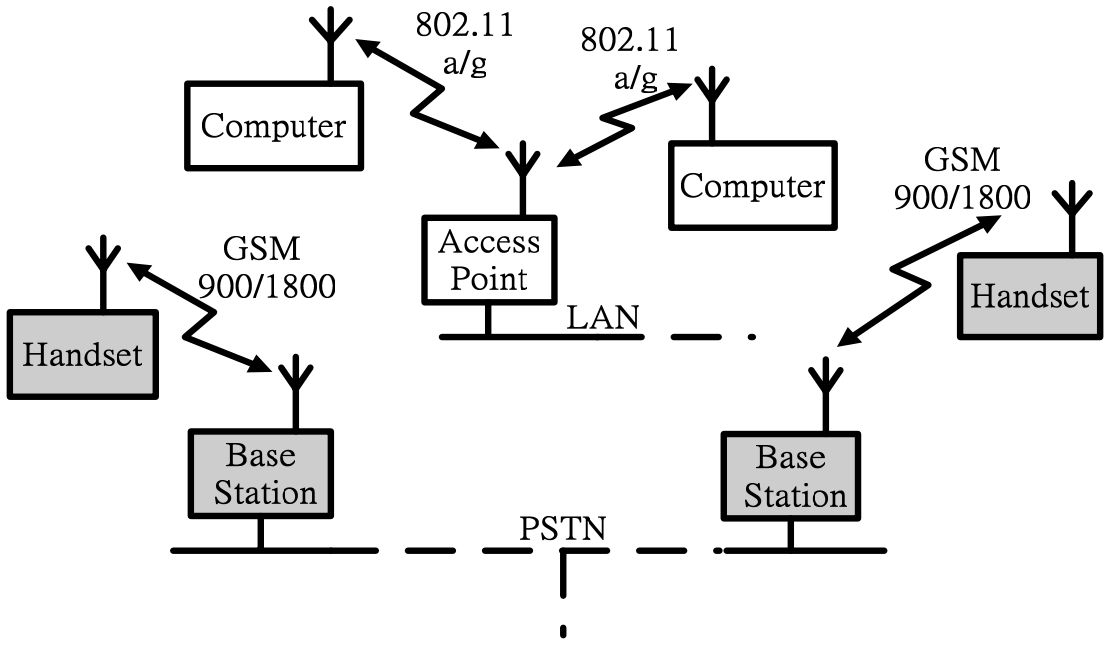


Fig. 1.1. A sketch of wireless communication systems.

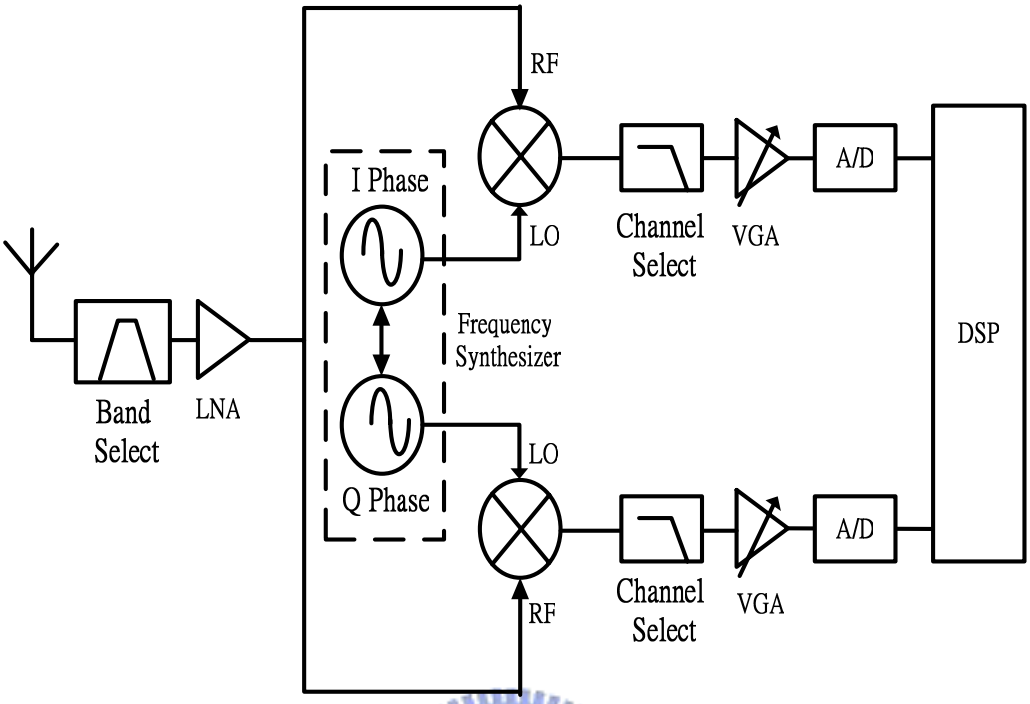


Fig. 1.2. Block diagram of a direct conversion receiver, where the LO frequency tunes to RF frequency [1.1].

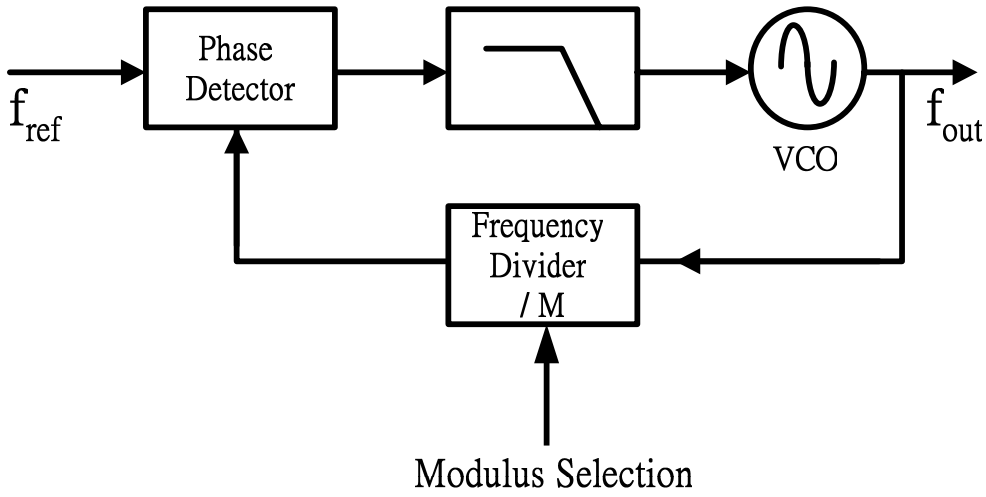


Fig. 1.3. Basic structure of synthesizer or PLL.

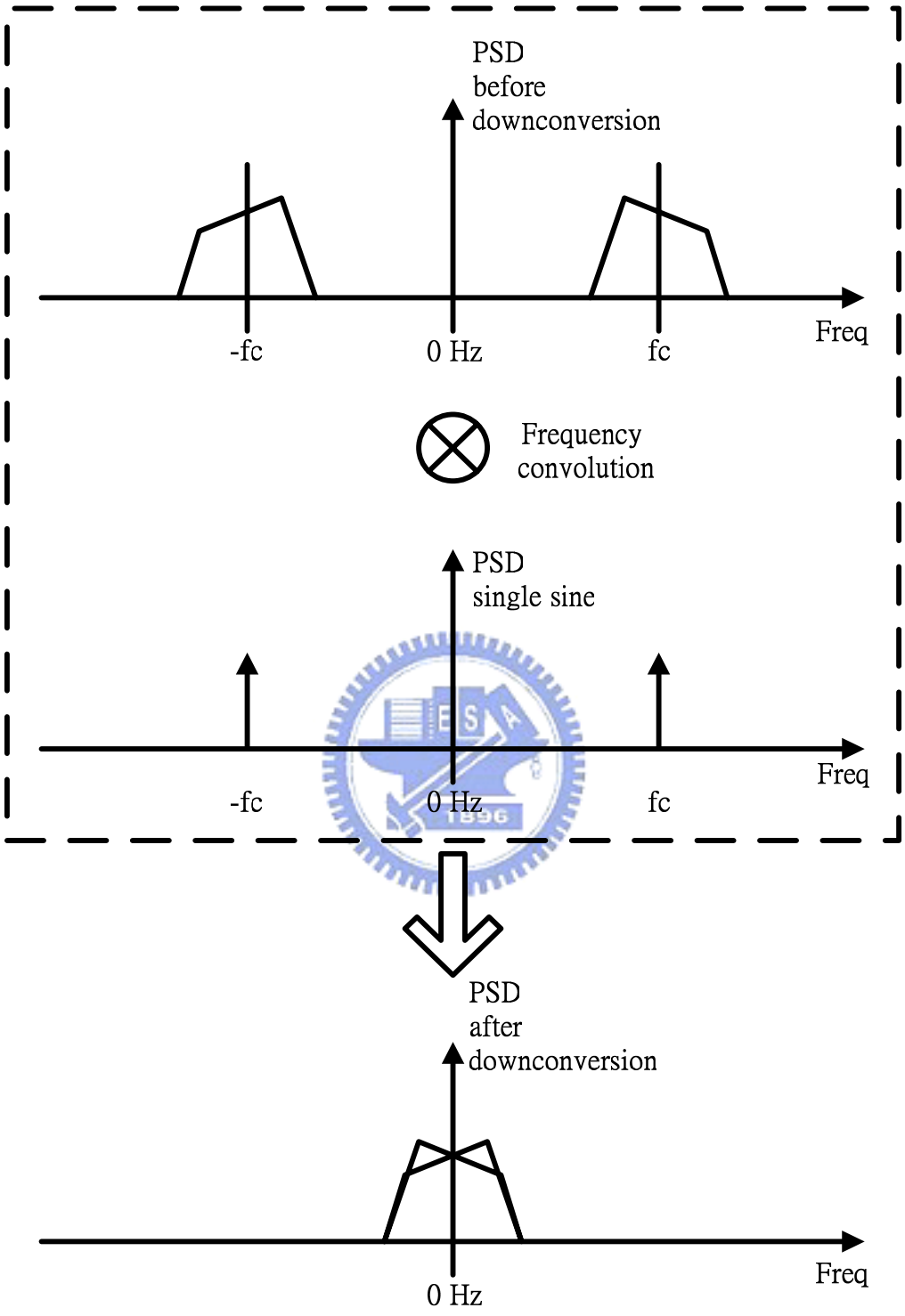


Fig. 1.4. Downconversion in a zero-IF receiver when multiplication with a single sine tone LO is used.

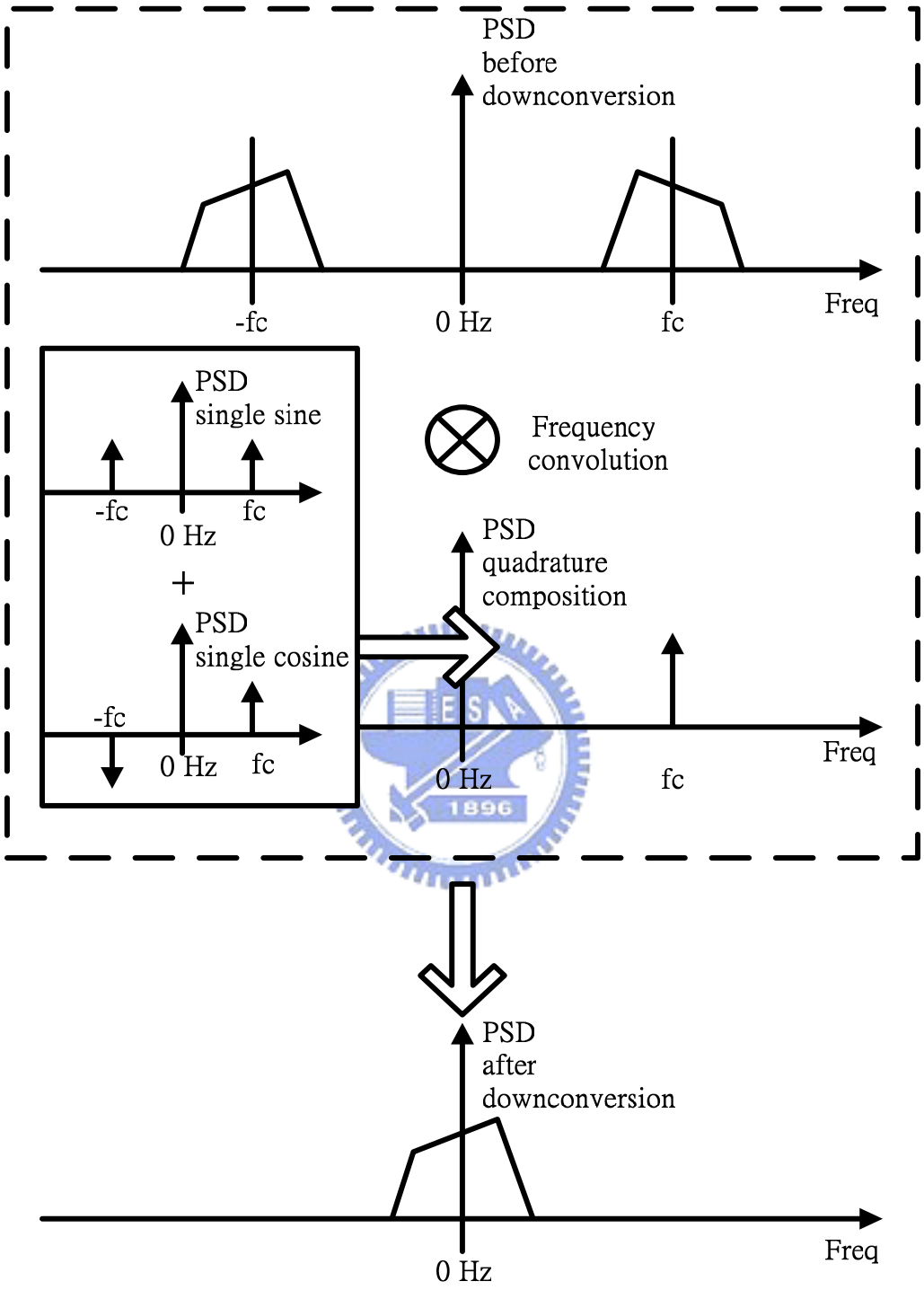


Fig. 1.5. Downconversion in a zero-IF receiver when multiplication with the positive frequency part of the LO is used.

Table.1.1 Key features of communication standard for WLAN and Mobile Phone.

		IEEE 802.11a (WLAN) [1.2]	IEEE 802.11g (WLAN) [1.2]	GSM-900 (Mobile Phone) [1.3]	GSM-1800 (Mobile Phone) [1.3]
PHY	Frequency Band (GHz)	U-NII Band: 5.15 - 5.25 5.25 - 5.35 5.75 - 5.85	ISM Band: 2.4 - 2.497	Uplink : 0.89 – 0.915 Downlink : 0.935 – 0.965	Uplink : 1.71 – 1.785 Downlink : 1.805 – 1.88
	Tolerance of Tx Center Frequency	±20 ppm	±25 ppm	N.A.	N.A.
	Channel Bandwidth	20 MHz	20 MHz	200 kHz	200 kHz
Digital Part	Modulation	BPSK QPSK 16/64 QAM OFDM FHSS/DSSS	BPSK QPSK 16/64 QAM CCK/PBCC OFDM FHSS/DSSS	GMSK (BT=0.3)	GMSK (BT=0.3)
	Multiple Access	CSMA/CA	CSMA/CA	TDMA/FDMA	TDMA/FDMA
	Duplexing	TDD	TDD	FDD	FDD
	Data Rate (Max)	< 54 Mbps	< 54 Mbps	< 270 kbps	< 270 kbps

1.2 Thesis Organization

In Chapter 2, the fundamentals of injection locking phenomenon are illustrated and 11-GHz frequency divider with locking range enhancement technique is fabricated for low power frequency synthesizer design. The measured result is also shown in this chapter.

In Chapter 3, basic analysis of quadrature output voltage controlled oscillator (QVCO) is presented, and a 5.2/5.8-GHz dual mode QVCO with novel frequency tuning technique is fabricated and measured.

In Chapter 4, two applications of frequency divider and QVCO are presented. First one is a 2.4/5.8 dual band QVCO which is configured as a QVCO followed by a frequency divider. The second is a 24-GHz fully differential push-push VCO derived from a 12-GHz QVCO.

Finally, in Chapter 5, conclusions for this thesis are given and some future work is suggested.

Appendix A is addressed for describing the properties of varactor.

Appendix B at the end of the thesis presents some techniques for quadrature phase measurement.

CHAPTER 2

Frequency Dividers

2.1 Overview

Frequency divider is an essential component in the feedback path of conventional Phase-Locked Loop (PLL). In PLL systems, the high frequency oscillation signal from the voltage-controlled oscillator (VCO) is downconverted to lower frequency by frequency dividers. After frequency division, the frequency of VCO can be compared to a clean reference source generated by crystal oscillator by using phase detector (PD). Then, according to the frequency difference between these two signals, the PD will generate control-signal to fine tune the frequency of VCO and make VCO be locked at the frequency of the reference source exactly. Besides, frequency divider has also been applied to frequency modulation receiver [2.1].

Frequency dividers can be categorized into digital frequency dividers and analog frequency dividers. Generally, digital frequency dividers are based on Data Flip-Flop (DFF) [2.2]-[2.7], while analog frequency dividers are implemented by using oscillators or mixers [2.8]-[2.16]. In spite of the implementations, the design issues for both of these two types of frequency dividers are the operating frequency range, power consumption, frequency range of operation and input sensitivity. In this chapter, the implementation of injection-locked frequency divider (ILFD) is described. On the other hand, some basic ideas of digital frequency divider will be illustrated in Chapter 3 and 4.

2.2 Injection-Locked Frequency Divider

ILFD is a kind of analog frequency divider which makes use of oscillator and takes advantage of less power consumption than its digital counter part, especially at high frequency operation. In this section, injection locking phenomenon is described first and then a superharmonic ILFD with locking range enhancement is implemented.

2.2.1 Resonator Based Oscillators

Before discussing injection-locking of oscillator, the basic idea of resonator based oscillator must be illustrated. Fig. 2.1 is a positive feedback model for oscillator analysis, this model consists of a nonlinear amplifier $f(j\omega)$, a resonator circuit $H(j\omega)$, and a positive feedback path $\beta(j\omega)$. The gain of amplifier is a nonlinear function of the oscillator's feedback voltage (V_f) and can be expressed as a polynomial series form [2.8]:

$$f(V_f) = \sum_{m=0}^{\infty} a_m \cdot V_f^{\,m} \tag{2.1}$$

where the coefficients a_m are constant. The oscillation frequency is selected by the bandpass filtering behavior of the resonator circuit whose transfer function is denoted by

$$H(j\omega) = \frac{H_0}{1 + j2Q\dfrac{\omega - \omega_r}{\omega_r}} \tag{2.2}$$

where Q and ω_r are the quality factor and resonant frequency of the resonator circuit respectively. Assuming that a sinusoidal function V_f denoted as $V_f = |V_f| \cdot \cos(\omega_o t + \phi)$, then harmonics of ω_o are generated by substitute V_f into (2.1) and can be expressed as

a Fourier series :

$$f(V_f) = \sum_{m=0}^{\infty} C_m(|\,V_f\,|)\cdot\cos(m\omega_o t + m\phi) \tag{2.3}$$

where C_m are Fourier coefficients of $f(V_f)$, which represent the nonlinearity of the amplifier, and are also functions of the amplitude $|V_f|$. The oscillation signal at the frequency ω_o travels across the closed loop and it will be sustained if it matches Barkausen criterion's gain condition and phase condition:

$$|C_1| \cdot |H(j\omega_o)| \cdot |\beta(j\omega_o)| = 1 \tag{2.4}$$

$$\angle C_1 + \angle H(j\omega_o) + \angle \beta(j\omega_o) = 2k\pi \tag{2.5}$$

where C_1 means the gain of amplifier at ω_o and $\angle C_1$ will only be 0 or π, depending on the sign of C_1. Oscillations frequency other than ω_o are prohibited by the phase shift introduced by $H(j\omega)$.

Fig. 2.2 shows two types of resonator based oscillator, where the resonator is made up of inductors (L) and capacitors (C). In Fig. 2.2(a), a common-base type colpitts oscillator is shown, where the feedback path is provided by the tapped capacitor and is positive feedback itself, while in Fig. 2.2(b), the positive feedback path is provided by the other transistor and is so called cross coupled -Gm oscillator.

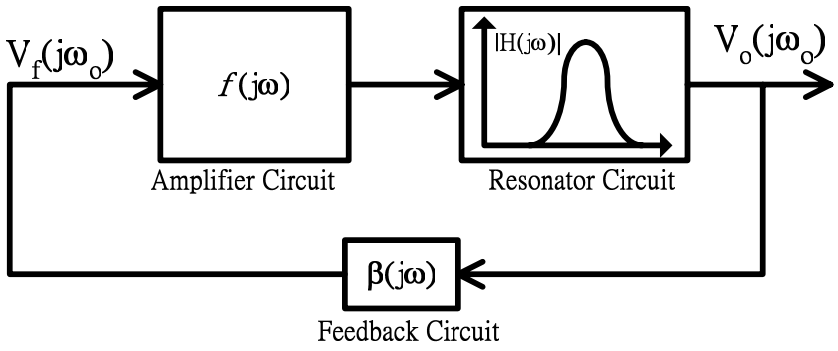


Fig. 2.1. Model for Resonator Based Oscillator.

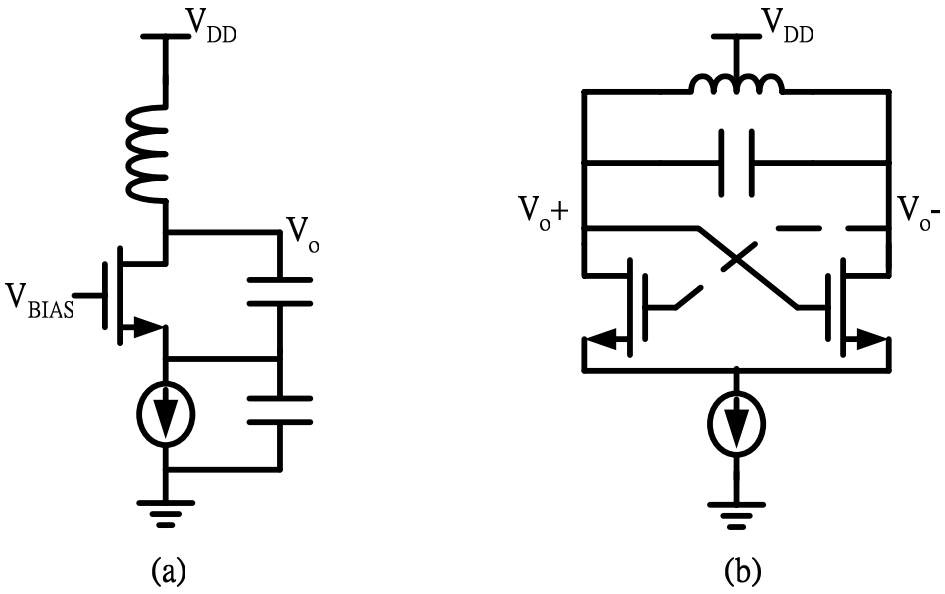


Fig. 2.2. Resonator based oscillator (a) Common Gate Colpitts Oscillator, (b) Cross Coupled -Gm Oscillator.

2.2.2 Injection-Locking Phenomenon in Oscillators

Injection-locking phenomenon can be investigated by impressing an external signal source upon an oscillator, it will be seen that both the instantaneous amplitude and instantaneous frequency of this oscillator are affected and synchronized by the impressed signal. According to the ratio of the injection signal's frequency (f_{inj}) to the output frequency of oscillator (f_o), injection locking can be classified into fundamental locking ($f_{inj} = f_o$), superharmonic locking ($f_{inj} \geqq 2 \cdot f_o$), and subharmonic locking ($f_{inj} < f_o$).

To understand the fundamental locking, the model of oscillator under injection of an external additive injection signal V_{inj} is adopted, as shown in Fig. 2.3 [2.8], and automatic volume control mechanism is provided by nonlinear element to sustain the

oscillation. When f_{inj} is made slightly deviated from the resonant frequency (f_r) of the resonator circuit, there will exist a periodic phase difference between V_{inj} and V_f[2.9]. As shown in Fig. 2.3, the summation of V_{inj} and V_f will therefore introduce a periodic variation of frequency on V_{sum}, and the instantaneous frequency f_{sum} can be represented by $\frac{1}{2\pi}(\omega_{inj} + \frac{d\alpha}{dt})$.

To derive the phase shift ϕ introduced by injection, [2.9] first assume that $|V_f| >> |V_{inj}|$ and for small ϕ we can write tan ϕ = ϕ, inspection of Fig. 2.3 yields

$$\phi = \tan \phi = \frac{|V_{inj}| \sin \alpha}{|V_f| + |V_{inj}| \cos \alpha} \approx \frac{|V_{inj}| \sin \alpha}{|V_f|} \tag{2.6}$$

On the other hand, Fig. 2.4 shows the phase of the voltage drop across a RLC resonator circuit with respect to the current flowing through it as a function of frequency. According to Fig. 2.3, current flowing through the resonator circuit must be in phase with V_{sum}, so that Fig. 2.4 can also be taken to represent the phase of V_f with respect to V_{sum} versus frequency. The phase shift (ϕ) introduced by a second-order parallel RLC tank in the vicinity of resonance frequency (ω_r) is

$$\phi = \frac{\pi}{2} - \tan^{-1}(\frac{\omega_o \cdot L}{R} \cdot \frac{\omega_r^2}{\omega_r^2 - \omega_o^2}) \tag{2.7}$$

Since $\omega_r^2 - \omega_o^2 \approx 2\omega_r(\omega_r - \omega_o)$, $\omega L / R_P = 1/Q$, *and* $\pi/2 - \tan^{-1} x = \tan^{-1}(x^{-1})$ [2.11], and for small ϕ we can write tan ϕ = ϕ, therefore

$$\phi = \tan \phi \approx \frac{2Q}{\omega_r}(\omega_r - \omega_o) \tag{2.8}$$

In Fig. 2.4, ϕ can also be written as

$$\phi = \frac{d\phi}{d\omega}\Big|_{\omega=\omega_r} \cdot (\omega_o - \omega_r) \tag{2.9}$$

Now, we derive $d\phi/d\omega = -2Q/\omega_r$ by differentiating (2.8) with respect to ω, and

substitute $d\phi/d\omega = -2Q/\omega_r$ and (2.6) into (2.9), then we get

$$\omega_o = -\frac{|V_{inj}|}{|V_f|}\cdot\frac{\omega_r}{2Q}\cdot\sin\ \alpha + \omega_r \tag{2.10}$$

(2.10) means physically that the instantaneous frequency ω is shifted from ω_r by an amount proportional to the sine of the phase angle existing at that instant between the oscillator and the injection signal, and proportional to the amplitude of injection signal. But, this frequency shift is inversely proportional to the phase versus frequency slope of the tuned circuit employed.

Furthermore, substituting $\omega_o=\omega_{inj}+d\alpha/dt$ and $\omega_r = \omega_{inj} + \Delta\omega_o$ into (2.10), we find

$$\frac{d\alpha}{dt} = -\frac{|V_{inj}|}{|V_f|}\cdot\frac{\omega_r}{2Q}\cdot\sin\ \alpha + \Delta\omega_o \tag{2.11}$$

where $\Delta\omega_o$ denotes the frequency deviation of the injected signal from the natural frequency ω_r. In the condition of injection locking, output signal frequency ω_o must be equal to ω_{inj}, that is to say $d\alpha/dt$ must be equal to 0. So that we substitute $d\alpha/dt = 0$ into (2.11) to find out the relationship for the phase angle α between oscillator signal and injection signal when injection lock happens

$$\sin\ \alpha = 2Q\cdot\frac{|V_f|}{|V_{inj}|}\cdot\frac{\Delta\omega_o}{\omega_r} \tag{2.12}$$

In (2.12), the phase angle α is stationary when the steady state is attained.

Since $\sin\alpha$ can only assume values between +1 and -1, from (2.12) we get the condition for injection locking:

$$\left|2Q\cdot\frac{|V_f|}{|V_{inj}|}\cdot\frac{\Delta\omega_o}{\omega_r}\right| < 1 \tag{2.13}$$

Rearranging (2.13), we can obtain the maximum deviation of f_{inj} from f_r, i.e., $\Delta\omega_{o,max}$

or so-called locking range, in the condition of $|V_f| >> |V_{inj}|$ as

$$\Delta\omega_{o,\max} < \frac{|V_{inj}|}{|V_f|}\cdot\frac{\omega_r}{2Q} \tag{2.14}$$

(2.14) implies that the smaller the value of quality factor and oscillation amplitude, the easier the oscillator can be injection-locked.

If injection-locking is fail, that is $d\alpha/dt \neq 0$, then output frequency beats, i.e., output frequency varies periodically, and this is called injection pulling. We solve the differential equation (2.11) to obtain the dependence of α upon time. The solution of (2.11) is [2.9][2.11]

$$\tan\frac{\alpha}{2} = \frac{\Delta\omega_{o,\max}}{\Delta\omega_o} + \frac{\omega_b}{\Delta\omega_o}\tan\frac{\omega_b\cdot t}{2} \tag{2.15}$$

where $\Delta\omega_{o,\max} < \frac{|V_{inj}|}{|V_f|}\cdot\frac{\omega_r}{2Q}$, $\Delta\omega_o = \omega_r - \omega_{inj}$, $\Delta\omega_o > \Delta\omega_{o,\max}$, and $\omega_b = \sqrt{\Delta\omega_o^2 - \Delta\omega_{o,\max}^2}$, (2.15) shows a periodic variation of α at a rate of ω_b when the frequency of injection signal falls below the locking range of oscillator, as indicated in Fig. 2.5 (a) and (b). Fig.2.5 (c) shows the periodic variation of output frequency. When the output frequency beats, the output spectrum exhibits sidebands with a frequency space of ω_b [2.11], as will be shown later.

Now, let's turn to the consideration of phase noise. Since the tank with small Q value is designed for a tolerable locking rang, the phase noise of free running oscillator will be inherently very poor. However, when the oscillator is injection locked, the phase noise in output signal can be analyzed and the noise transfer function behaves as in a first order PLL [2.8]

$$L(\Delta\omega) = L_{inj}(\Delta\omega)\cdot\frac{(\Delta\omega_{0,\max}/N)^2}{\Delta\omega^2 + \Delta\omega_{0,\max}^2} + L_{osc}(\Delta\omega)\cdot\frac{\Delta\omega^2}{\Delta\omega^2 + \Delta\omega_{0,\max}^2} \tag{2.16}$$

(2.16) shows that the phase noise of the injection locked oscillator can be either from injection signal or from the oscillator itself, and N stands for the frequency division ratio of the incident signal to the output signal. The equation shows that the noise from incident signal is shaped by the low-pass characteristic of the noise transfer function, so that the phase noise of injection locked oscillator will track the phase noise from injection signal, except the offset frequency beyond the locking range, besides, the output phase noise is reduced by N^2 due to the frequency division. On the other hand, the noise from the oscillator itself is highpass filtered and meet the phase noise in oscillator itself at the edge of the locking range. As indicated in Fig. 2.6 [2.8], the output phase noise will be dominated by the incident signal.

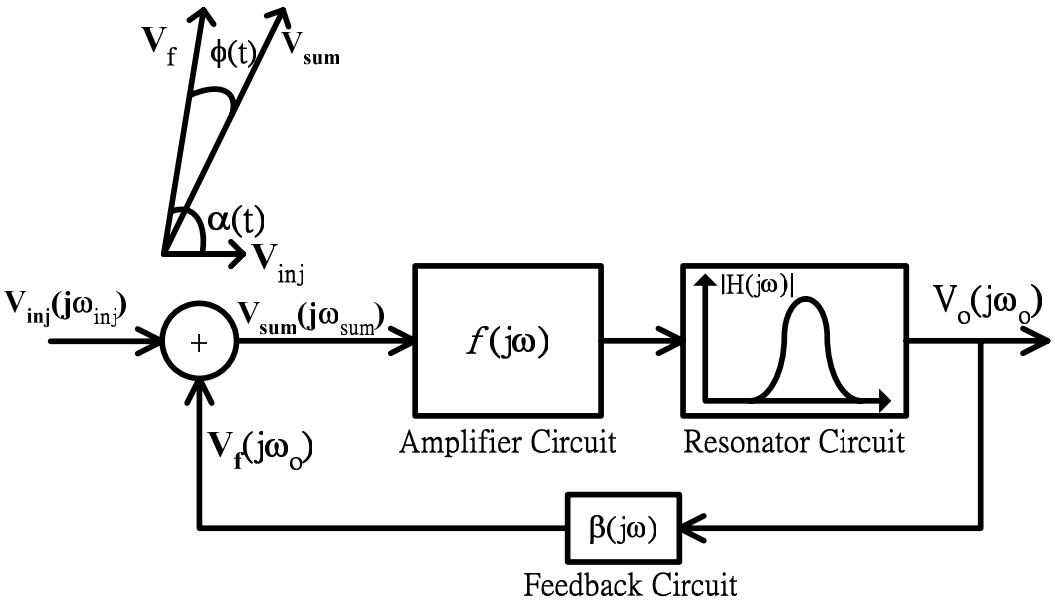


Fig. 2.3. The Model of oscillator under injection signal and the frequency of f_{inj} is made slightly different from natural frequency of resonator circuit.

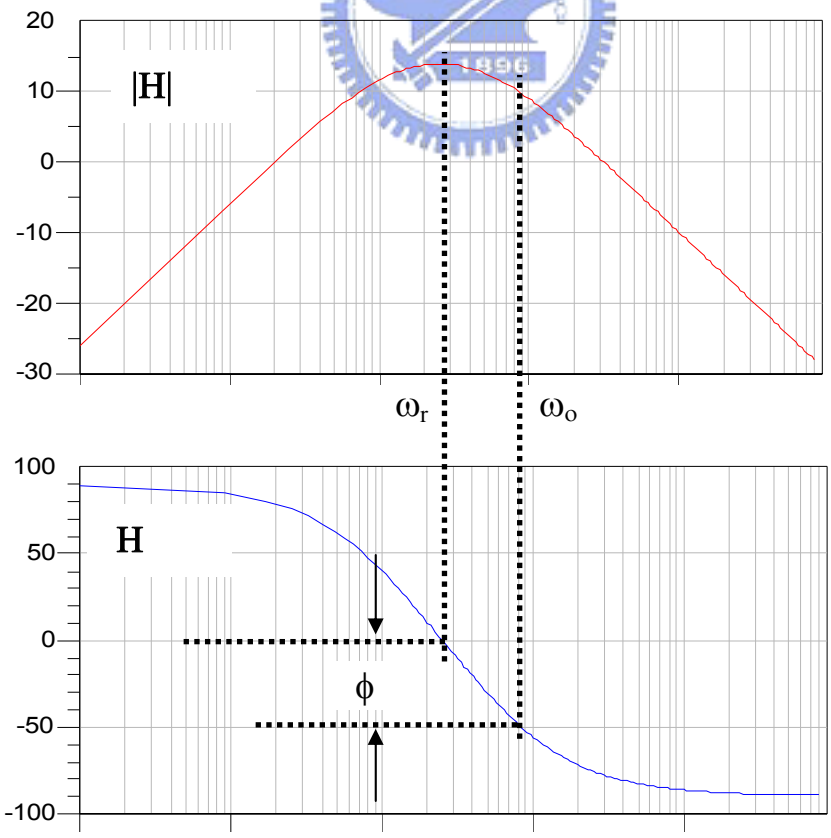
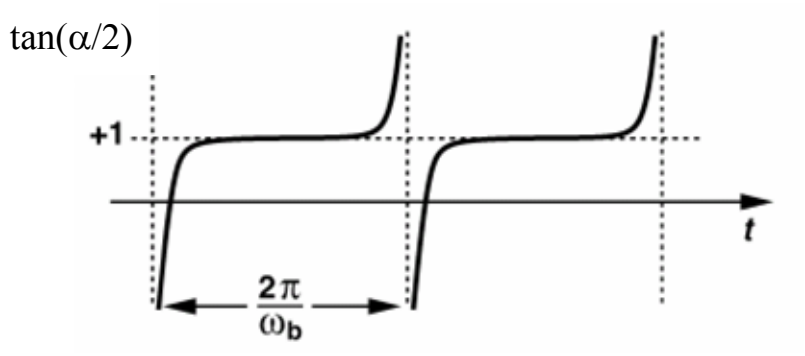
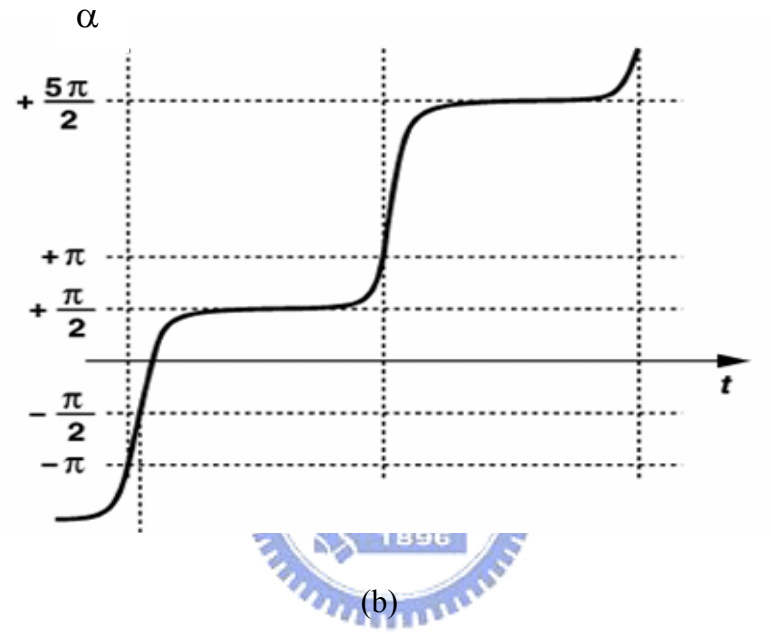


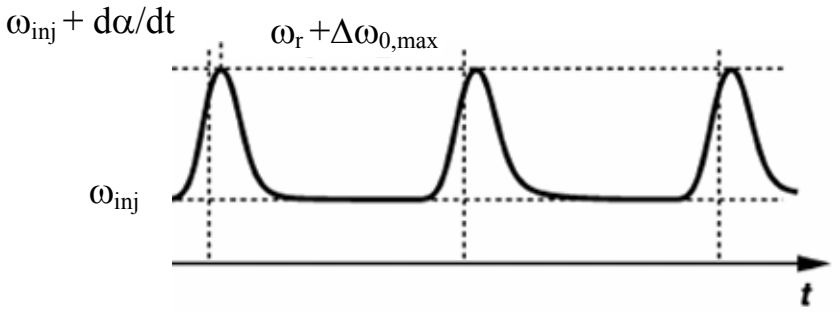
Fig. 2.4. Characteristic function of RLC tank.



(a)



(b)



(c)

Fig. 2.5. When the frequency of injection signal falls below the locking range (2.15) shows (a) Periodic variation in tan(α/2), (b) Periodic variation in α, and (c) Periodic variation in output frequency [2.11].

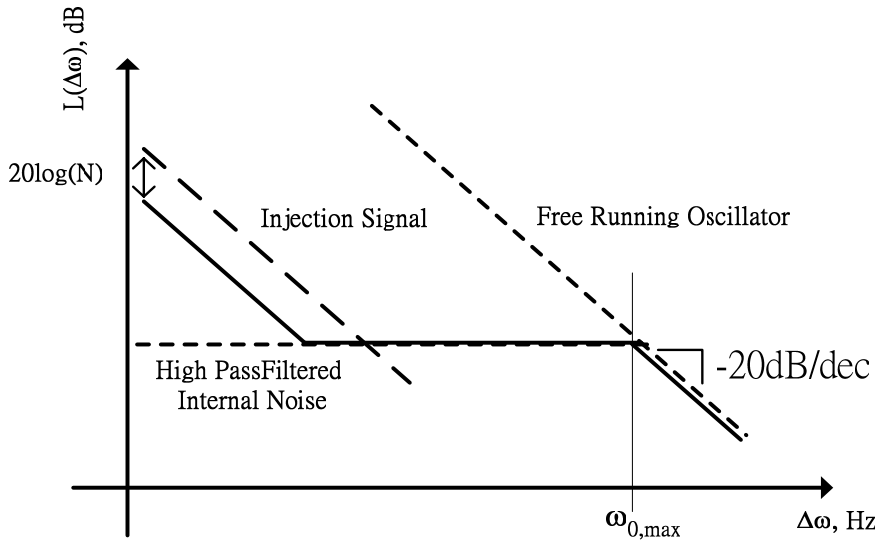


Fig. 2.6. Suppression of oscillator's phase noise due to injection locking [2.8].

2.2.3 Superharmonic Injection Locking

In addition to fundamental locking, oscillators can be superharmonic injection locked when the frequency of incident signal is around the frequency of the Nth harmonic signal in the oscillator. According to Fig. 2.3, the nonlinear amplification in oscillator first performs frequency intermodulation on the incident signal and the fundamental signal of the oscillator, and then generates a signal around the fundamental frequency of the oscillator. Analogous to fundamental locking mechanism, the new generated signal will start to synchronize the oscillator. Therefore, the superharmonic injection locked oscillator can serve frequency division by N, when the frequency of incident signal is N times the output frequency at oscillator.

Superharmonic injection could be analyzed by several nonlinear analysis

methods such as power series, harmonic balance and Volterra series. To achieve more precise prediction, power series and Harmonic balance are combined for nonlinear analysis [2.8] [2.12]. In [2.8], it assumes a third order nonlinear amplification by power series (i.e., $f(v)=a_0+a_1v+a_2v^2+a_3v^3$) to determine the operating point and then solves the 2nd order harmonic injection locking by harmonic balance analysis. The locking range and output amplitude under 2nd order harmonic injection is derived by [2.8] as

$$\left|\frac{\Delta\omega}{\omega_r}\right| < \left|\frac{H_0 a_2 V_{inj}}{2Q}\right| \tag{2.16}$$

$$V_o = \sqrt{\frac{4}{3}\frac{1}{a_3 H_0}\left[1 - H_0 \cdot \left(a_1 + \frac{3}{2}a_3 V_{inj}^2 + a_2 V_{inj}\cos\alpha\right)\right]} \tag{2.17}$$

In (2.16), $\Delta\omega = (\omega_{inj}/N)-\omega_r$ can be maximized by larger inductor (since $H_0/Q = \omega_r L$) and larger second-order distortion term a_2. In (2.17), the oscillation amplitude V_0 varies, due to $\cos(\alpha)$ being varied by the different frequency of injection signal. (2.17) also indicates that too large V_{inj} limits injection locking range when the term under the square root becomes negative.

To the consideration of phase noise, the oscillator under superharmonic injection locking has the same property as what happened in the oscillator under fundamental injection locking. However, one difference is that the noise in incident signal is 20log(N) reduced, due to the operation of the frequency division by N.

2.2.4 Operation Frequency Range Enhancement Techniques

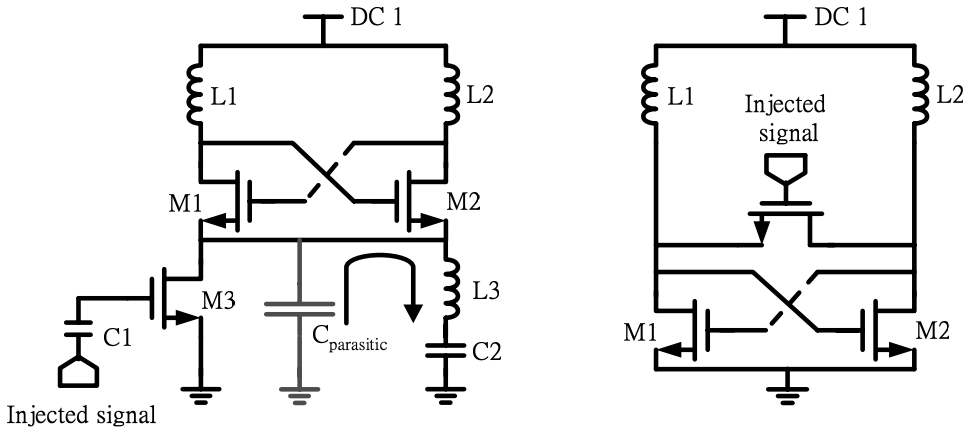
One of the methods to improve operation frequency range is achieved by enhancing $\Delta\omega_{0,max}$. According to (2.14), $\Delta\omega_{0,max}$ is proportional to the amplitude of injection signal to be summed with the feedback signal, so that has been reported the

techniques of inductive shunt peaking [2.13] and direct injection [2.14] to remedy the injection current loss into the parasitic capacitors at the signal injection node (loss of current causes the degradation in voltage amplitude).

Fig. 2.5 (a) shows the concept of inductive peaking technique, where M_{tail} is in large size to serve as a current source. Since M_{tail} will introduce a large parasitic capacitor C_{tail} at the injection node and provide a low impedance path to ground for the injection signal at high frequency, L_{shunt} is therefore placed to resonate with C_{tail} at the injection frequency, so as to provide high impedance at this node. Fig. 2.5 (b) shows the schematic of direct injection ILFD, the incident signal (IN) is injected through a MOS transistor switch over the tank. Since the size of the transistor switch can be designed much smaller than that of M_{tail} in Fig. 2.5 (a), less parasitic capacitance is introduced at the injection node.

Another way of increasing ILFD operation frequency range is to track the frequency of injection signal by making the LC tank with a tunable resonant frequency [2.14], however, this method doesn't increase $\Delta\omega_{0,max}$.

Table. 2.1 shows that shunt peaking method is a good choice for locking range enhancement at low injection power level. But [2.14] demonstrates that ILFD can do high frequency division with less power consumption. Besides, [2.13] and [2.14] reveal that injection locking efficiency depends on which node in the oscillator the injection signal being applied to.



(a) (b)

Fig. 2.7. Locking range improvement by (a) Inductive shunt peaking [2.13], (b) Direct injection [2.14].

Table. 2.1. Comparison of frequency range enhancement techniques.

	[2.13]	[2.14]	[2.15]
Technique	Shunt Peaking	Direct Injection	Tunable Tank
Technology	0.35μm CMOS	0.13μm CMOS	0.25μm CMOS
Supply Voltage	1.2V	1.5 V	2 V
Current Consumption	1.1 mA	2 mA	0.6 mA
f_{inj} (GHz)	18~19.4	40.5~42	3.9~5 [1.]
Frequency Division	2	2	2
P_{inj}	5 dBm	15 dBm	0.81 V

[1.] For a given control voltage.

2.3 An 11-GHz Injection-Locked Frequency Divider

2.3.1 Circuit Implementations

An 11-GHz differential ILFD has been designed and fabricated in UMC 0.18μm CMOS technology, Fig. 2.8 shows the schematic. As indicated by simulation result, the incident signal can be 11.4-11.8 GHz single ended at -10dBm injection power, and the output signal will be 5.7-5.9 GHz differential, i.e., a function of frequency division by 2.

The core of this ILFD is a 5.8-GHz oscillator which is constructed by a NMOS cross-coupled pair (M1-M2), inductors (L1-L2) and parasitic capacitors of M1-M2. To achieve wide locking range, according to (2.14), the Q factor of L1-L2 needs be designed as low as possible. In order to reduce the injection current loss into the parasitic capacitors at the source of M1 and M2, small size of M1, M2 and M3 is selected.

Since the Q factor of inductor is inversely proportional to the series metal resistance and proportional to the inductance. According to [2.18], we take the following equation as the guideline for choosing the size of spiral inductor

$$R_{metal} = \frac{\rho \cdot L}{w \cdot t} \tag{2.18}$$

$$L = K_1 \cdot \mu_0 \frac{n^2 \cdot d_{avg}}{1 + K_2 \cdot \varphi} \tag{2.19}$$

in (2.18), ρ is the resistivity of metal line, L is the total length of the inductor metal line, w is line width, and t is the thickness of metal line. In (2.19), K_1 and K_2 are constants for different shape of spiral inductor, e.g., for octagonal K_1 = 2.25 and K_2 =3.55, n is the number of turns, d_{avg} = $(d_{in}+d_{out})/2$ means average diameter as

indicated by Fig. 2.9, $\varphi = (d_{out}-d_{in})/(d_{out}+d_{in})$ represents how hollow the inductor is, small φ means that the inductor is hollow ($d_{out} \approx d_{in}$). In order to have a low Q and high inductance, we choose the inductor in the size of wide radius and narrow line-width. In this manner we obtain small Q while achieving a large QL product to keep the output amplitude large and save power consumption (since the impedance of tank at resonance is $H_0=\omega_r QL$) [2.8].

For further locking range enhancement, inductive shunt peaking technique is applied by placing L3 at the source of M1 and M2 and a capacitor, C2, is placed in series with L3 to serves as a DC block. To decide the inductance value, S-parameter simulation is performed at the source of M1 and M2 to tune the impedance into resistive at the interested frequency. As the circuit simulation reveals, we are aware that L3 also affects the oscillation frequency of oscillator.

For the purpose of biasing, M3-M4-R1 serves as a current mirror and the incident signal is injected into the gate of M3. The incident signal is then delivered to the common source node of M1 and M2, and is thus summed with output feedback signal across the source and gate of M1 and M2. At the gate of M4, a high resistance resistor, R_{block}, is placed to block the injected signal from leaking through the parasitic capacitor C_{gs} of M3.

Two common source output buffers, M5 and M6, are added for driving the 50Ω loading contributed by measurement instrument. And two external components - Bias Tee are needed for biasing the output buffer and coupling the output signal to measurement instrument.

Fig. 2.10 is chip's photograph, the PADs are layout for pitch 150μm on-wafer probe.

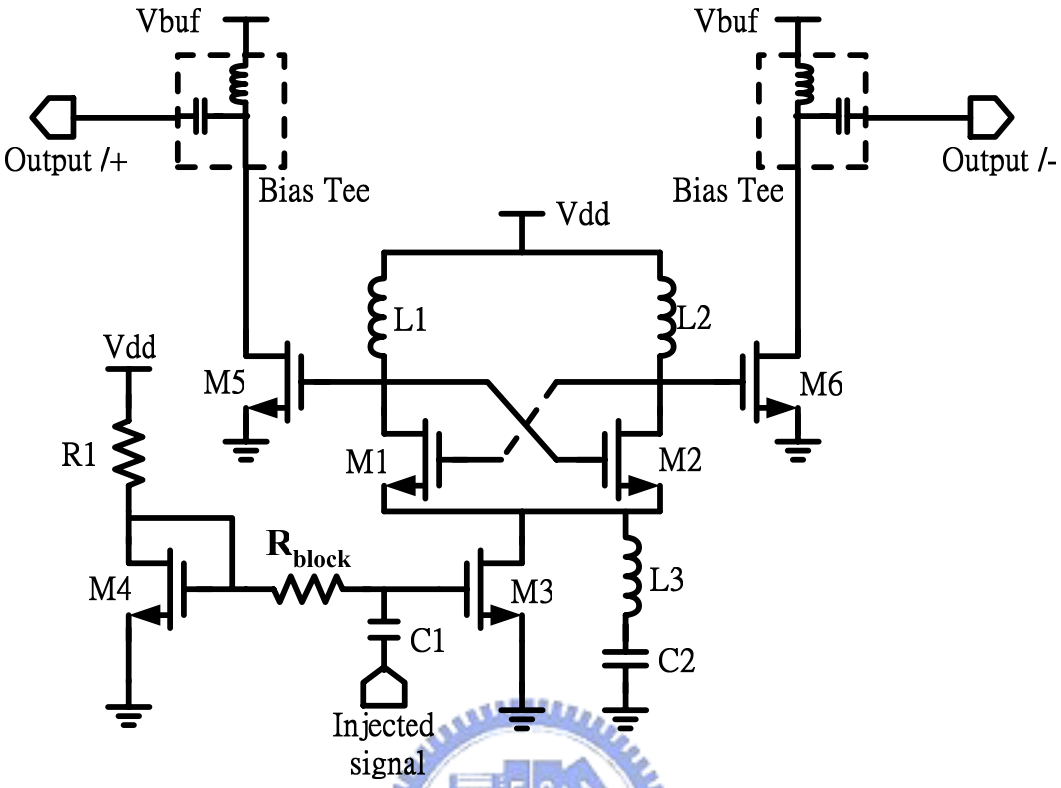


Fig. 2.8. Schematic of ILFD with shunt-peaking inductor [2.13].

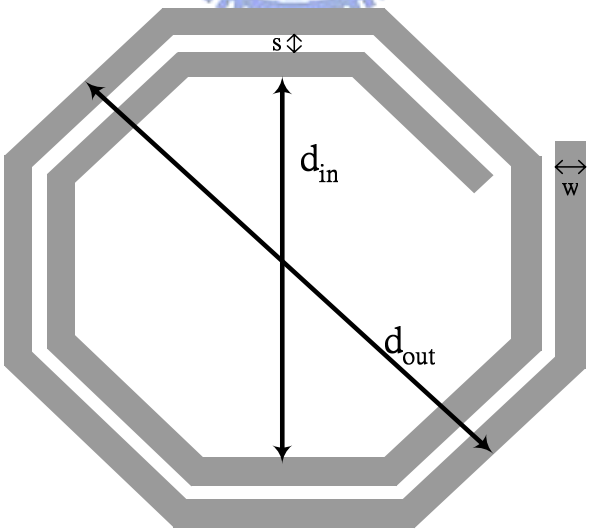


Fig. 2.9. Parameters of on-chip inductor realization [2.18].

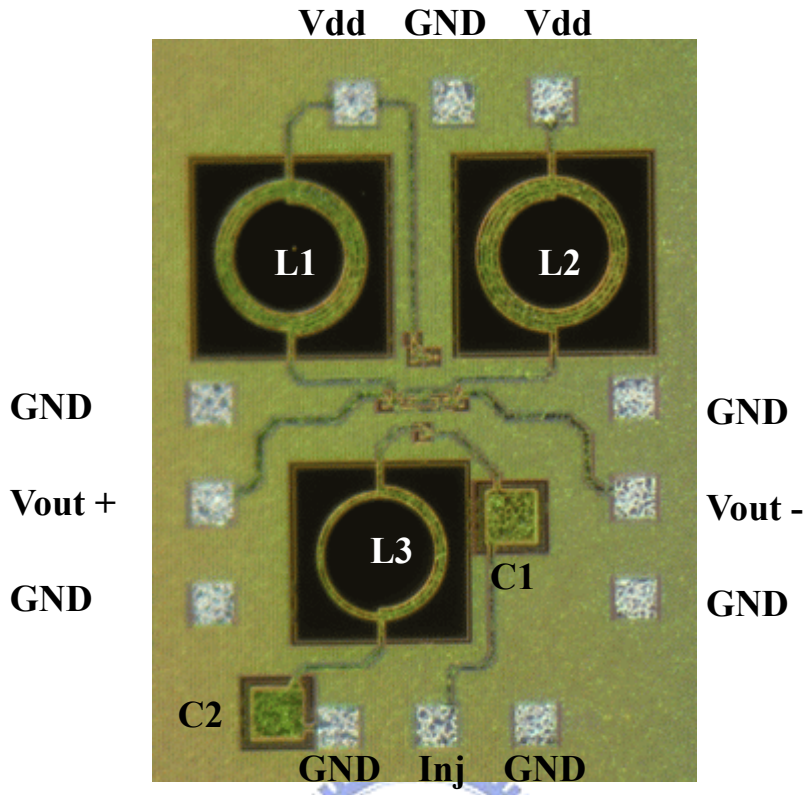


Fig. 2.10. The ILFD circuit fabricated in UMC 0.18μm CMOS technology.

2.3.2 Experimental Results

This chip is measured by on-wafer probing technique and the measurement setup is depicted in Fig. 2.11. At one of the differential output ports, spectrum analyzer is used to monitor the output spectrum, so that, for balance loading, a 50Ω resistor is terminated at the other one.

To decide the operation frequency of this ILFD, we first measure the oscillation frequency at different supply voltage with no injection signal being presented at this time. Fig. 2.12 shows that this ILFD can operate at 4.68 GHz when supplied by 1.2 V and its output power is about -4.5 dBm, as indicated in Fig.2.13. Since the measured oscillation frequency of ILFD is lower than simulated, the injection signal swept around the 2nd harmonic frequency of oscillator must now be 8.5-10.1 GHz, as the

center at 9.3 GHz.

When the oscillator is under injection, in the locking range, the output spectrum will show signal tones at the half frequency of injected signal and harmonics, looked like Fig. 2.14 Otherwise, exceeding the locking range, the frequency of output signal is pulled by the injection signal and the spectrum with beat frequency shows that most power of sidebands is confined within the locking range, looked like Fig. 2.15.

At each injection frequency, the injection power level is decreased until the ILFD fails to lock. Fig. 2.16 shows the minimum injection power for different injection frequency, at the desired injection power level of -10dBm, the input frequency range is about 500 MHz.

Besides, shunt peaking inductor is disconnected form ILFD by laser cutter and ILFD without shunt peaking is measured again, the testing result from ILFD with and without shunt peaking inductor is compared in Fig. 2.17. It shows that the input frequency range has more than 50% improvement with shunt peaking technique.

Next, phase-noise in the free running oscillator is measured, as shown in Fig. 2.18. At large offset frequency around 2~5 MHz, poor phase noise is contributed by the power supply noise. Fig. 2.19 shows that, at most offset frequency, the phase noise from injection signal is suppressed by 2^{nd} harmonic injection locking process with a 6dB reduction, as expected. However, some phase noise at 2-5 MHz offset is not suppressed by injection locking.

As a remark, fundamental injection locking of the ILFD with inductive shunt peaking is measured too and the locking range is shown in Fig. 2.20. Though fundamental locking shows smaller locking range than which of 2^{nd} harmonic locking, it is suggested to cut the shunt peaking inductor L3 to obtain fair comparison (since inductive peaking is performed at 2^{nd} harmonic frequency).

Table. 2.2 shows the performance of this circuit in comparison to other design. It shows that ILFD can operate at high frequency while consume less power than digital frequency divider.

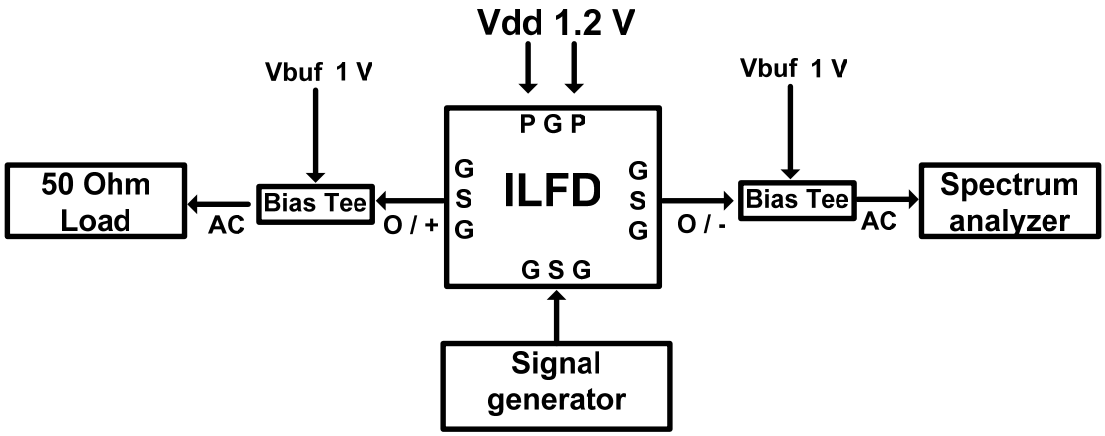


Fig. 2.11. ILFD measurement setup.

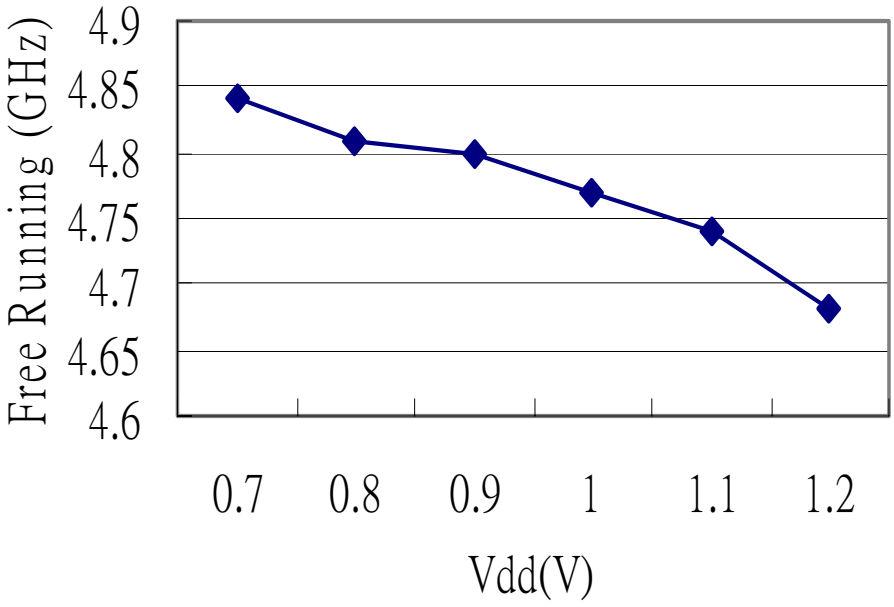


Fig. 2.12. Oscillation frequency of ILFD under no injection signal.

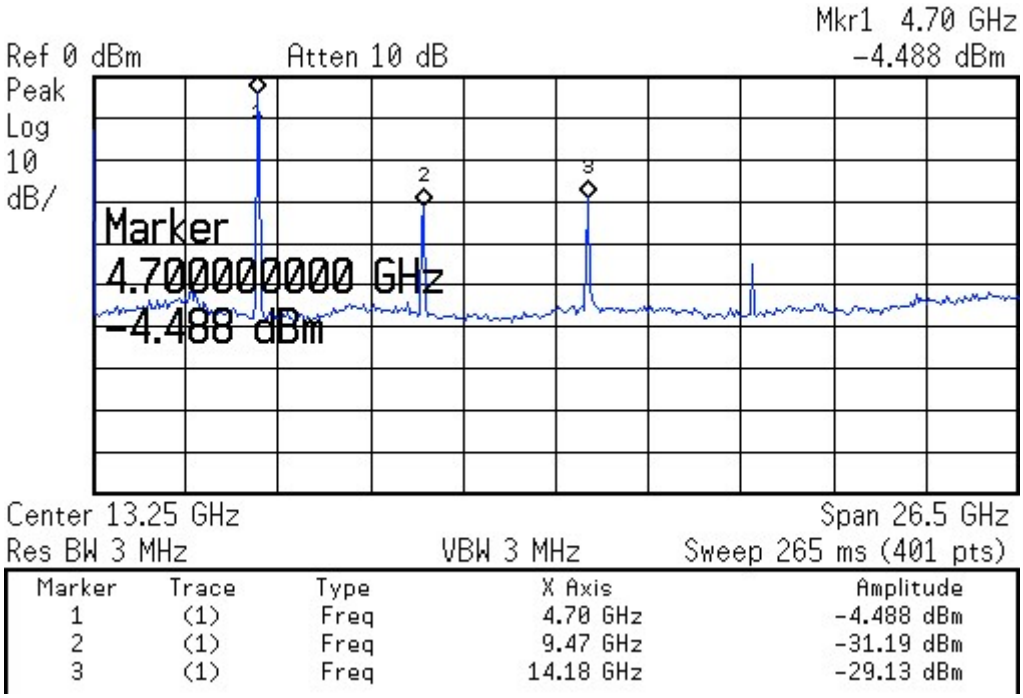


Fig. 2.13. The output spectrum of ILFD without the injection signal being applied and the supply voltage is 1.2 V.

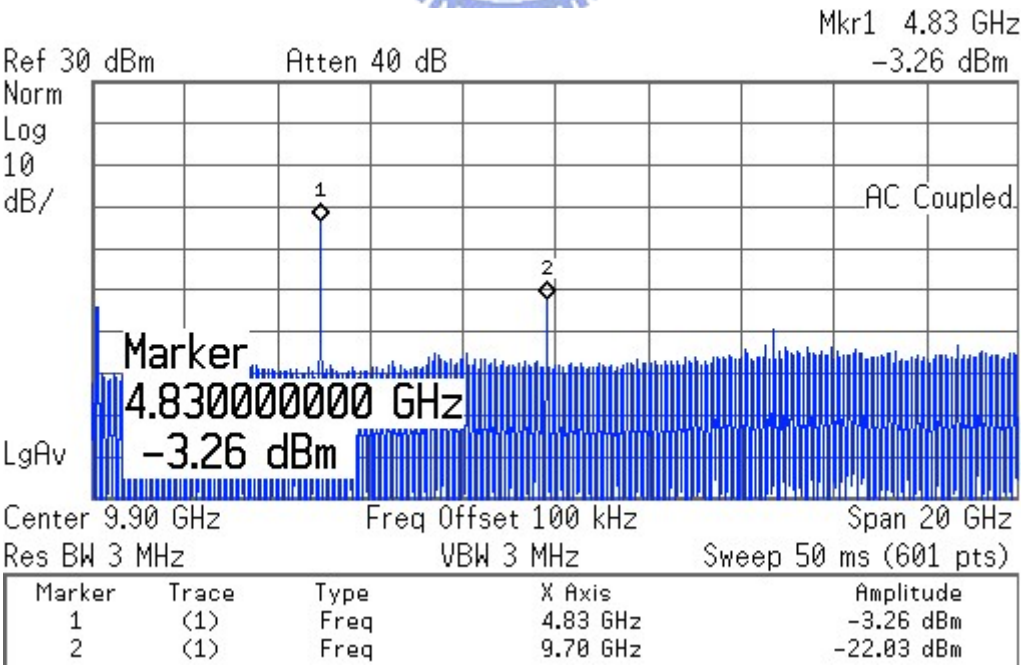


Fig. 2.14. The output spectrum of ILFD under injection locking when f_{inj}=9.7-GHz.

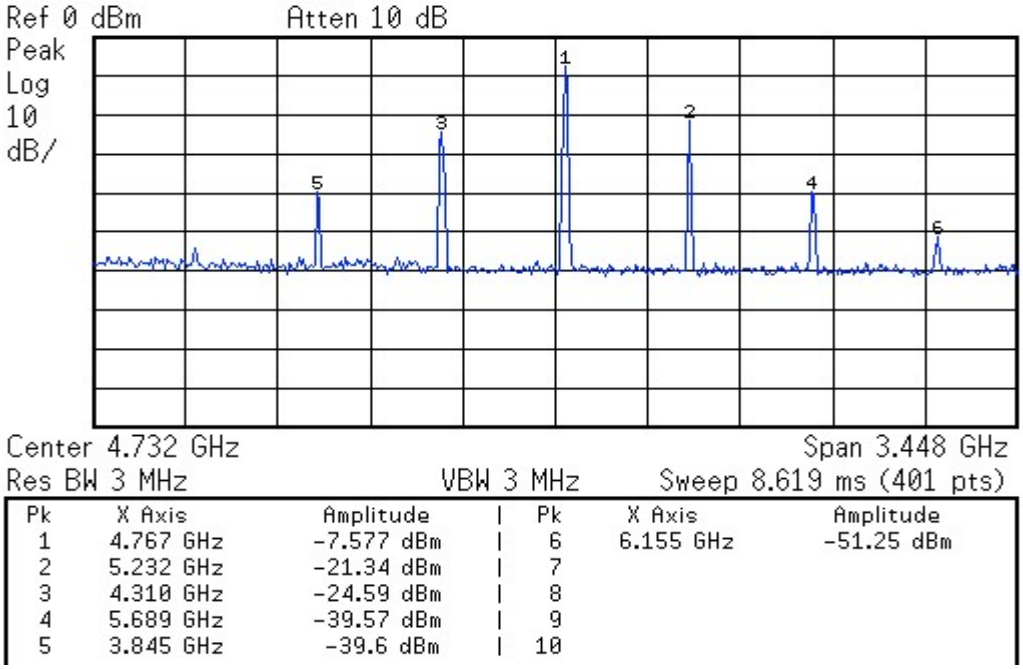


Fig. 2.15. The output spectrum of ILFD under frequency pulling when f_{inj} =10 GHz and the injection power level of -10 dBm.

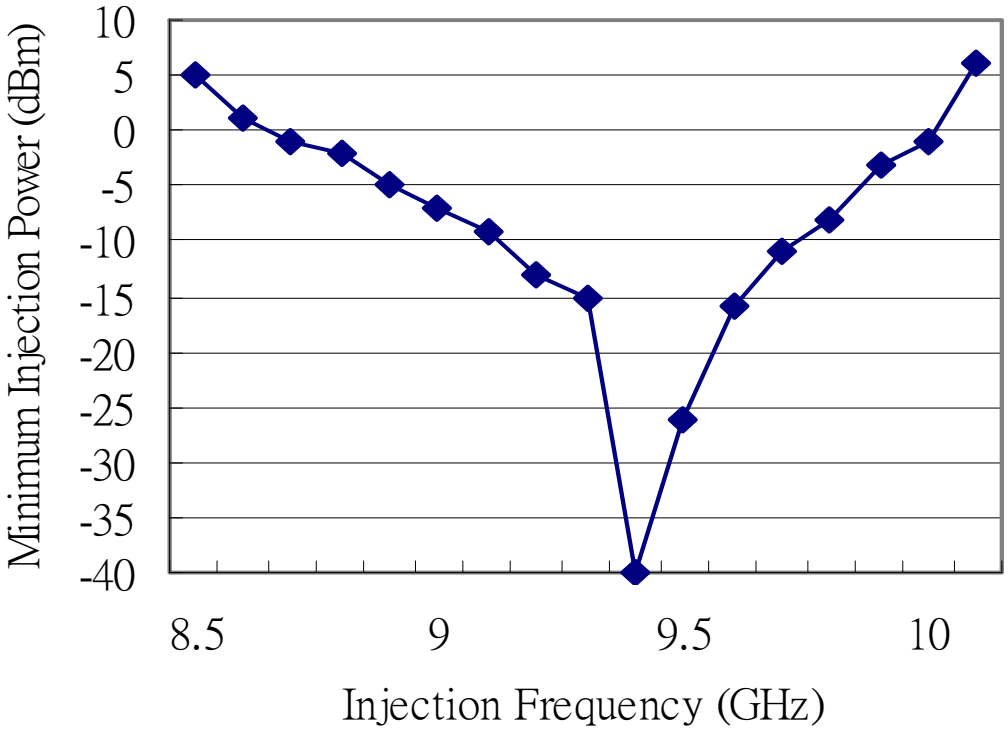


Fig. 2.16. Minimum injection power level for different f_{inj}.

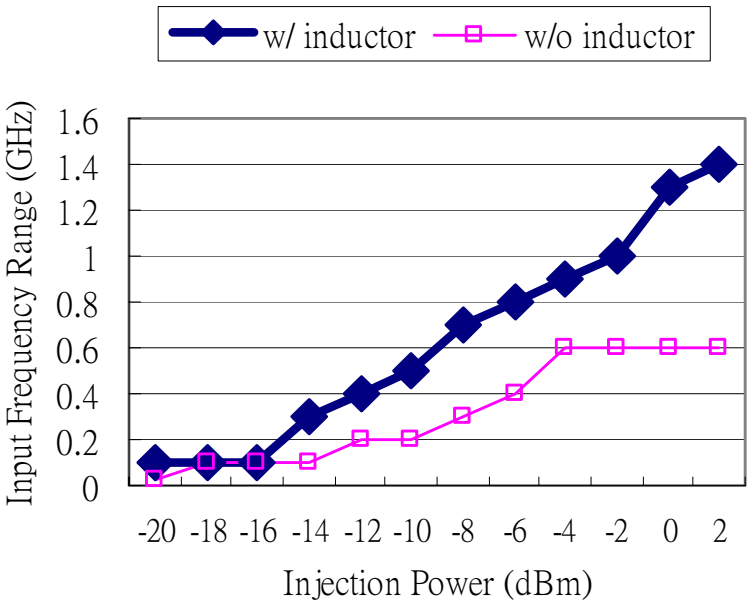


Fig. 2.17. Input frequency range of ILFD with and without shunt peaking inductor.

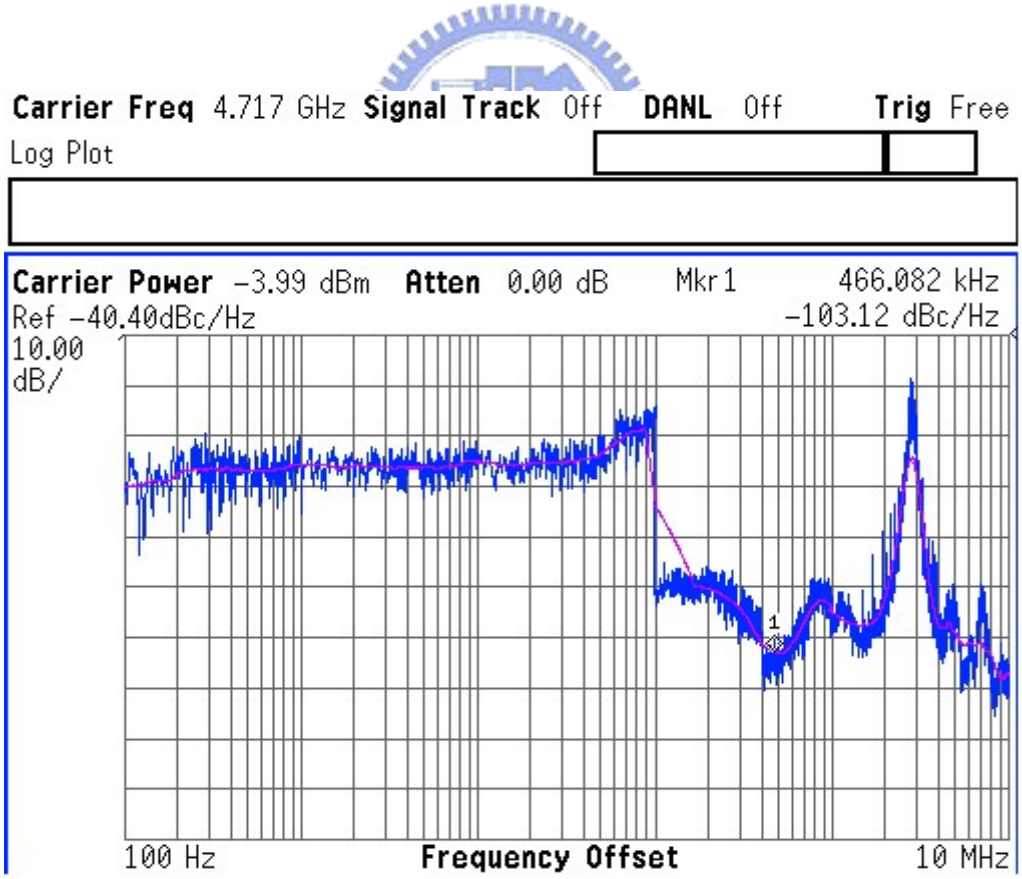


Fig. 2.18. Phase Noise of free running ILFD powered by power supply and large noise appears at the offset frequency from 2 to 5 MHz.

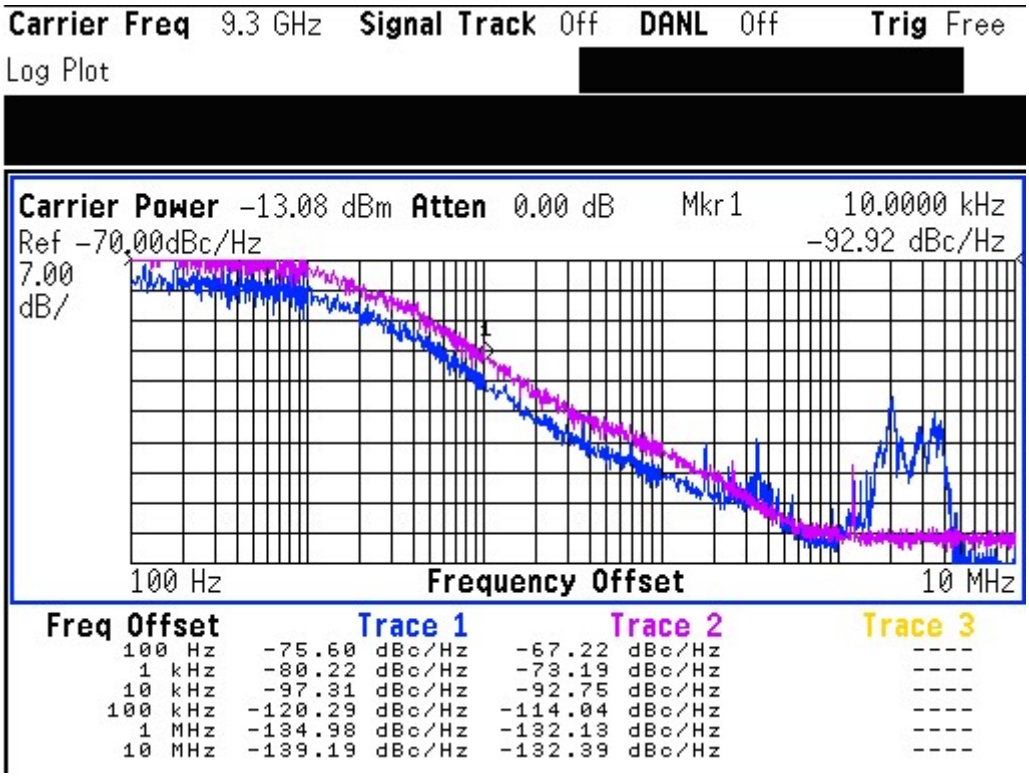


Fig. 2.19. Phase Noise difference between injection signal and output signal is 6 dB (the upper trace for injection signal and the lower trace for ILFD output), excepts at the offset frequency from 2 to 5 MHz.

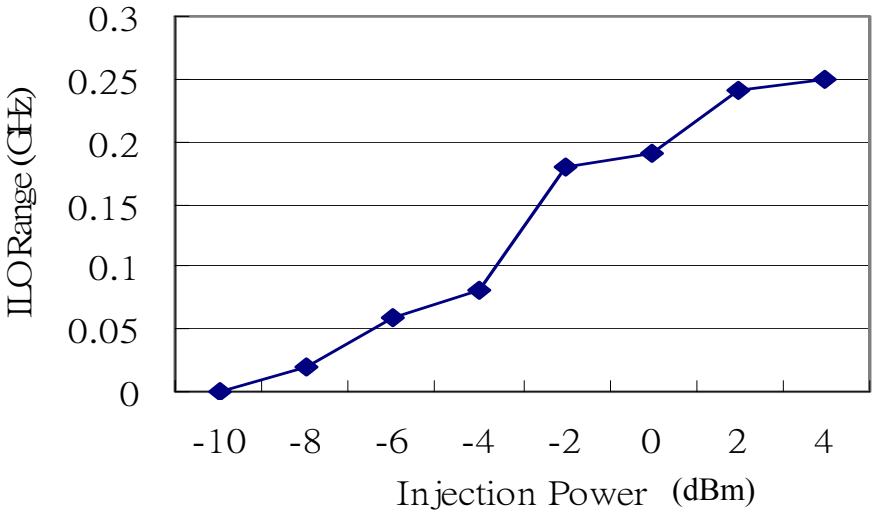


Fig. 2.20. Fundamental injection locking range of the ILFD with inductive shunt peaking at 2nd harmonic.

Table. 2.2. Performance summary of ILFD with comparison to other design.

	Simulated	Measured	[2.13]	[2.6]
Circuit Type	Analog	Analog	Analog	Digital
Technology	0.18μm CMOS	0.18μm CMOS	0.35μm CMOS	0.1μm CMOS
Supply Voltage	1.2V	1.2 V	1.2 V	2.6 V
Current Consumption	1 mA	1.26 mA	1.1 mA	10.8 mA
f_{inj} (GHz)	11.4~11.8	9.2~9.7	8.4~9.9	DC~13.4
Frequency Division	2	2	2	2
Injection Power	-10dBm	-10dBm	2dBm	Rail-to-Rail

2.3.3 Discussions

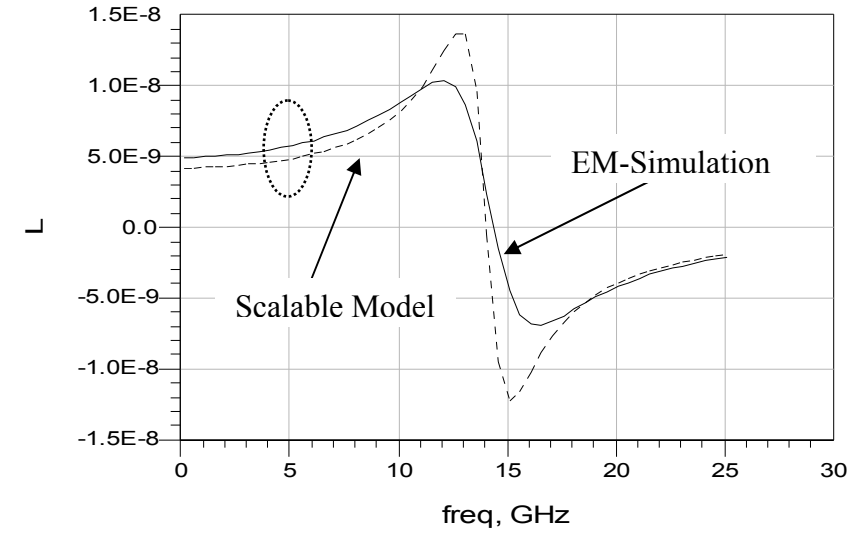
As indicated by measurement and simulation results, the measured oscillation frequency is lower than simulated, but the measured output power (-4.5dBm) of the free running oscillator is almost the same as the simulated (-4.2dBm). Starting from this observation, some discussions are made as follows.

First, we assert that the inductance value of the scalable inductor model provided by the foundry may be underestimated. So, we estimate the inductance by the EM Simulator - Ansoft Designer® and compare this result with the scalable model. In Fig. 2.21, the solid line represents the inductance and quality factor of the inductor used in this design (with ground seal ring) versus frequency by the EM-Simulation, and the dashed line represents the inductance and quality factor of the scalable model. The EM-simulation result shows that the inductance value at 5GHz is 1nH higher than the scalable model, which favors our assertion. Also, referring to Table.2.2, the biasing current is around 10% higher than the simulation result, so that we obtain a

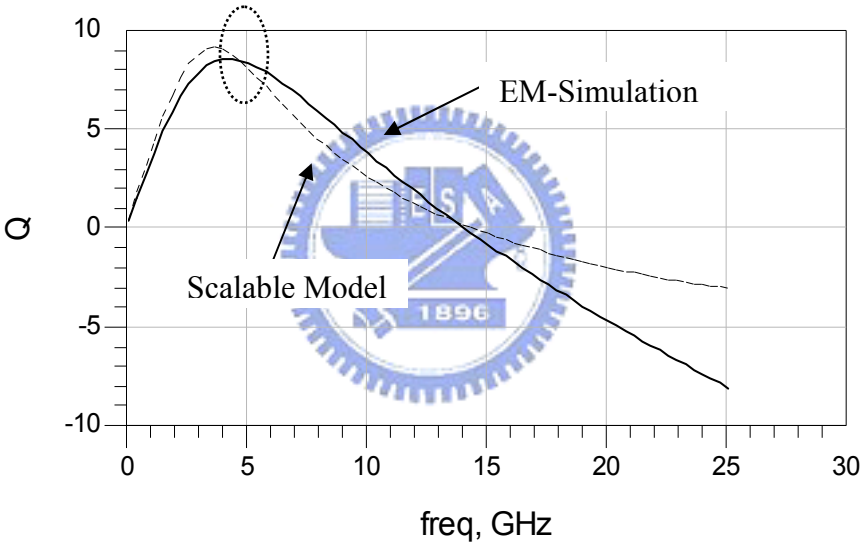
larger output power.

Since Fig. 2.19 shows that the phase noise in oscillator is suppressed by injection signal except the phase noise at the offset frequency from 2 to 5 MHz. We assert that this part of phase noise is contributed by power supply noise. So, we replace all the power supply with 1.5-V battery and obtain the output spectrum of free running oscillator. As shown in Fig. 2.22, a clear spectrum is available after the replacement and the phase noise of this free running oscillator at 1MHz offset frequency is about -80dBc/Hz. Then we observe the phase noise of the ILFD output when an injection signal of 9.3GHz being applied, as shown in Fig. 2.23.

On the other hand, we perform some circuit simulation to check the injection power efficiency of the ILFD. By the smith chart of the reflection coefficient at the injection port, as shown in Fig. 2.24, we obtain poor injection efficiency by the large magnitude of S11. In order to improve the injection efficiency, we try to make the input impedance at the injection port to get close to 50 Ohm when the signal generator with 50Ohm input impedance is applied, so we add an inductor in series with the injection port to make the reflection coefficient coincide the real axis on the smith chart at the frequency of the desired injection signal. As shown in Fig. 2.25, we obtain a smaller reflection coefficient after the improvement, and hence the injection efficiency is improved. By the improved injection efficiency, we also obtain an improved injection locking range as indicated by our circuit simulation.



(a)



(b)

Fig. 2.21. Comparison of inductor's (a) Inductance, and (b) Quality Factor by means of EM-Simulation (solid line) and Scalable Model (dashed line).

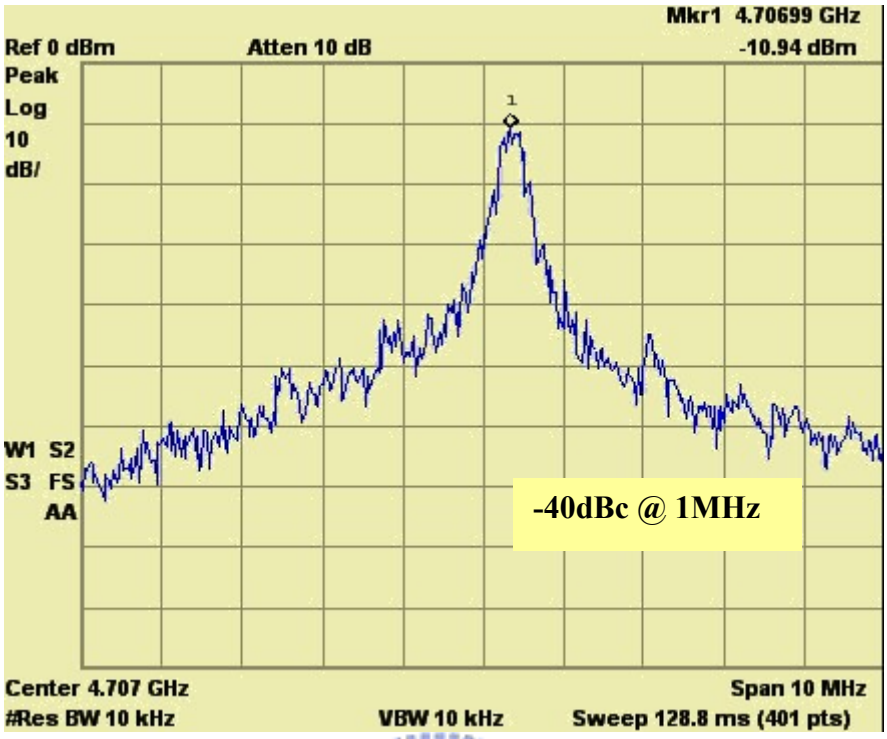


Fig. 2.22. The spectrum of the free running oscillator supplied by a 1.5V battery.

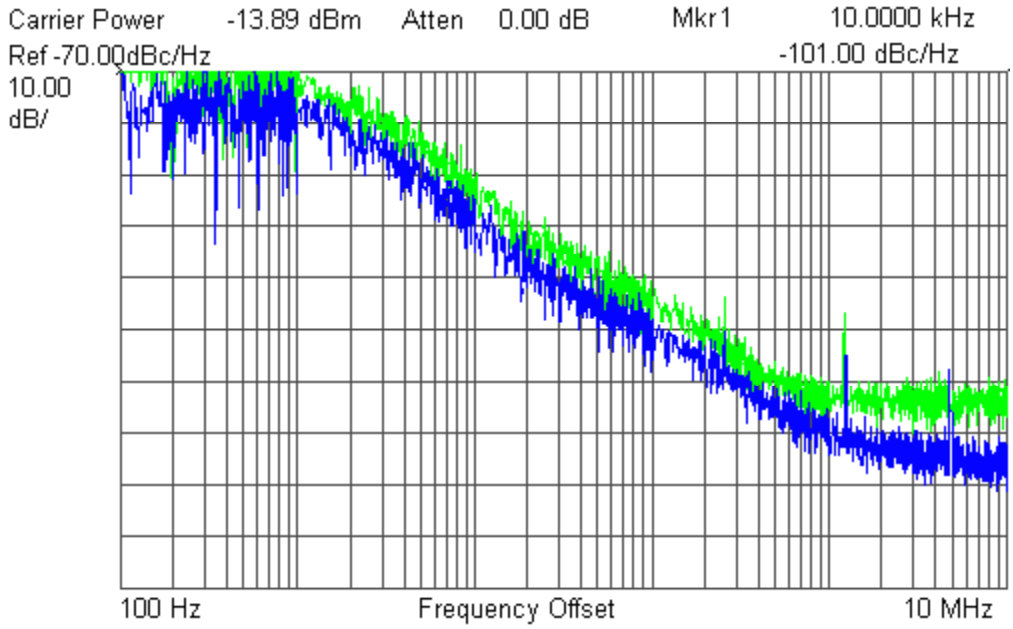
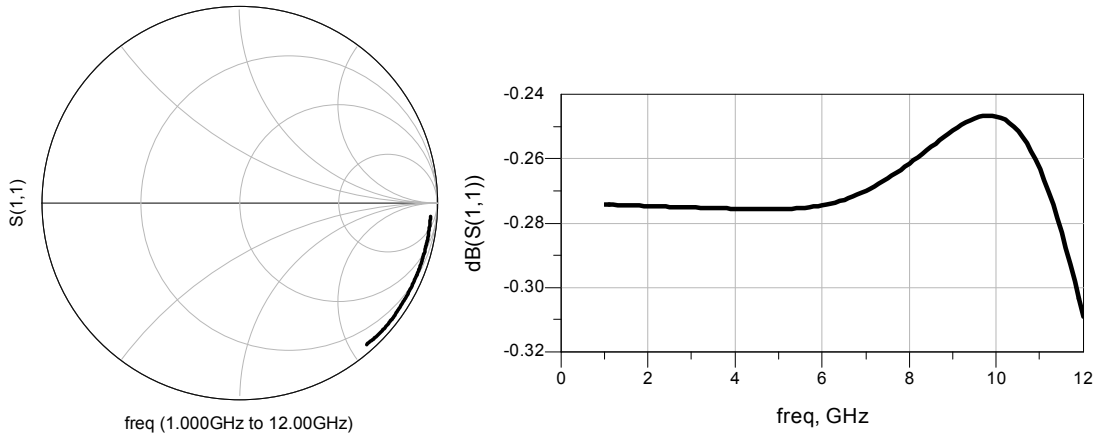
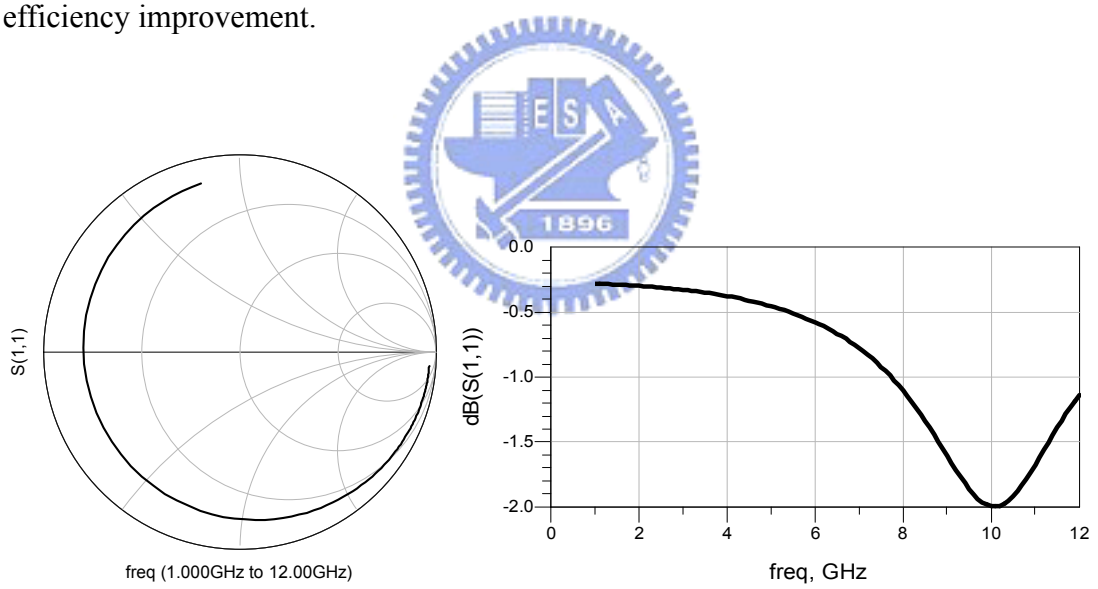


Fig. 2.23. Measured phase noise when the ILFD is supplied by battery. (The upper trace for the phase noise of the injection signal and the lower trace for ILFD output)



(a) (b)

Fig. 2.24 (a) The smith chart, and (b) the magnitude, of the reflection coefficient from the S-parameter simulation at the injection port of the ILFD circuit without injection efficiency improvement.



(a) (b)

Fig. 2.25 (a) The smith chart, and (b) the magnitude, of the reflection coefficient from the S-parameter simulation at the injection port of the ILFD circuit after injection efficiency improvement.

CHAPTER 3

Quadrature VCO

3.1 Quadrature Signal Generation Techniques

As mentioned in chapter 1, in order to avoid the destruction of information after downconverted by the Zero/Low IF receiver, both in-phase (I) and quadrature-phase (Q) frequency downconversion path need be utilized. For this reason, some techniques used to generate quadrature phase signal will be described in this section.

3.1.1 Polyphase Filter (PPF)

Conventionally, quadrature signal can be generated by converting a differential signal to quadrature, a popular way of implementation is a differential VCO followed by poly phase filters (PPF) [3.1][3.2] or LC all pass filter [3.3].

Polyphase filter is a symmetric RC network as shown in Fig. 3.1, where R's are all set identical and all C's are set identical too. To understand the operation principle of PPF, we first apply Superposition Theorem and Kirchhoff's Current Low at node V_{o2} to find the output V_{o2} when the inputs V_{i1} and V_{i2} are applied:

$$(V_{i1}\angle\theta_{i1} - V_{o2}\angle\theta_{o2}) \cdot SC = V_{o2}\angle\theta_{o2} / R \tag{3.1}$$

$$(V_{i2}\angle\theta_{i2} - V_{o2}\angle\theta_{o2}) / R = V_{o2}\angle\theta_{o2} \cdot SC \tag{3.2}$$

where S =jω, then add (3.1) and (3.2) together, we derive:

$$V_{o2}\angle\theta_{o2} = (1+\frac{1}{j\omega RC})^{-1}V_{i1}\angle\theta_{i1} + \frac{1}{1+j\omega RC}\cdot V_{i2}\angle\theta_{i2} \quad (3.3)$$

In (3.3), when the frequency (ω) of V_{i1} and V_{i2} is at the RC pole 1/(RC), then

$$V_{o2}\angle\theta_{o2} = V_{i1}\angle(\theta_{i1}+45°) + V_{i2}\angle(\theta_{i2}-45°) \quad (3.4)$$

(3.4) means that when the input frequency is 1/(2πRC), two adjacent inputs are shifted by +45° and -45 ° to the output node through the capacitor and resistor respectively, and then added together. So that, if the input signal is differential and at the RC pole frequency, the output signal of the PPF will be in quadrature, as shown in Fig. 3.2.

From the above description, the PPF can transform the differential signal into quadrature, but only at the RC pole frequency. To extent the operation bandwidth and for equiripple response, several PPFs with equally spaced pole frequency on the logarithmic frequency axis, i.e., equal ratio between adjacent pole frequencies, are cascaded together [3.2], as shown in Fig. 3.3.

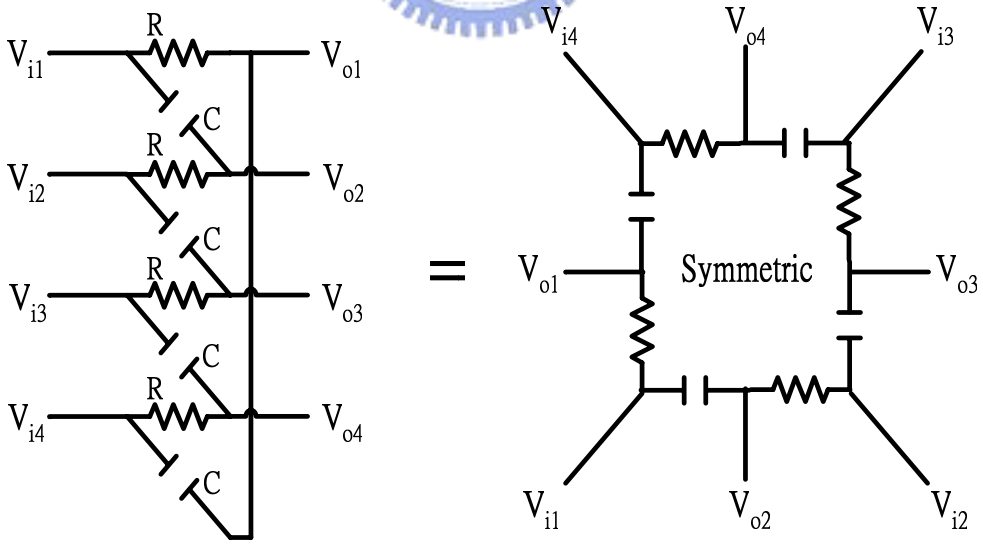


Fig. 3.1. Classic RC polyphase filter.

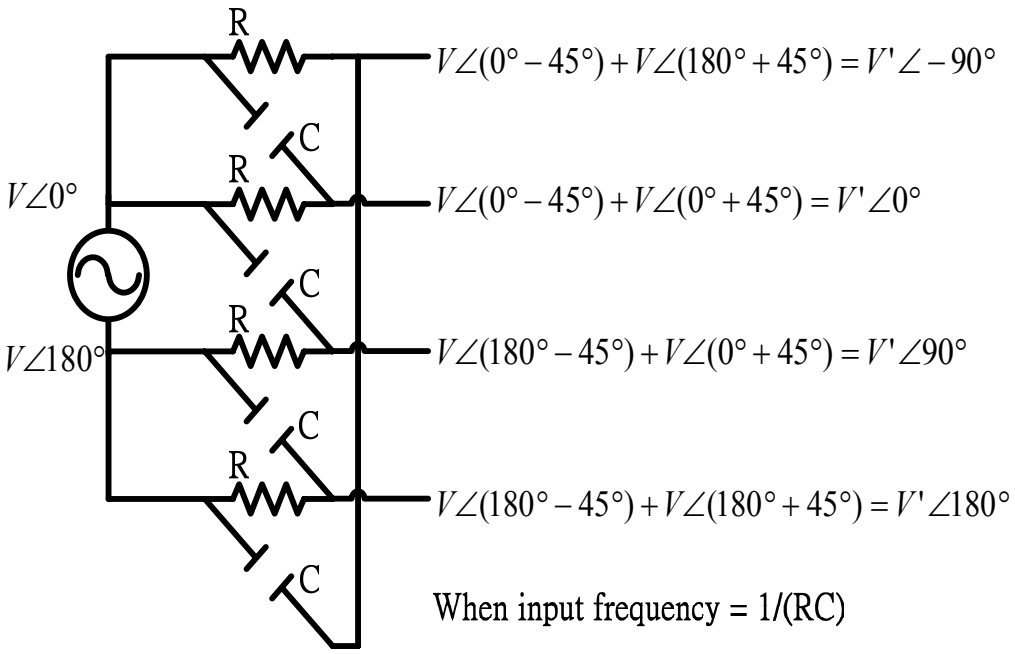


Fig. 3.2. Polyphase filter used to convert a differential signal to a differential quadrature signal.

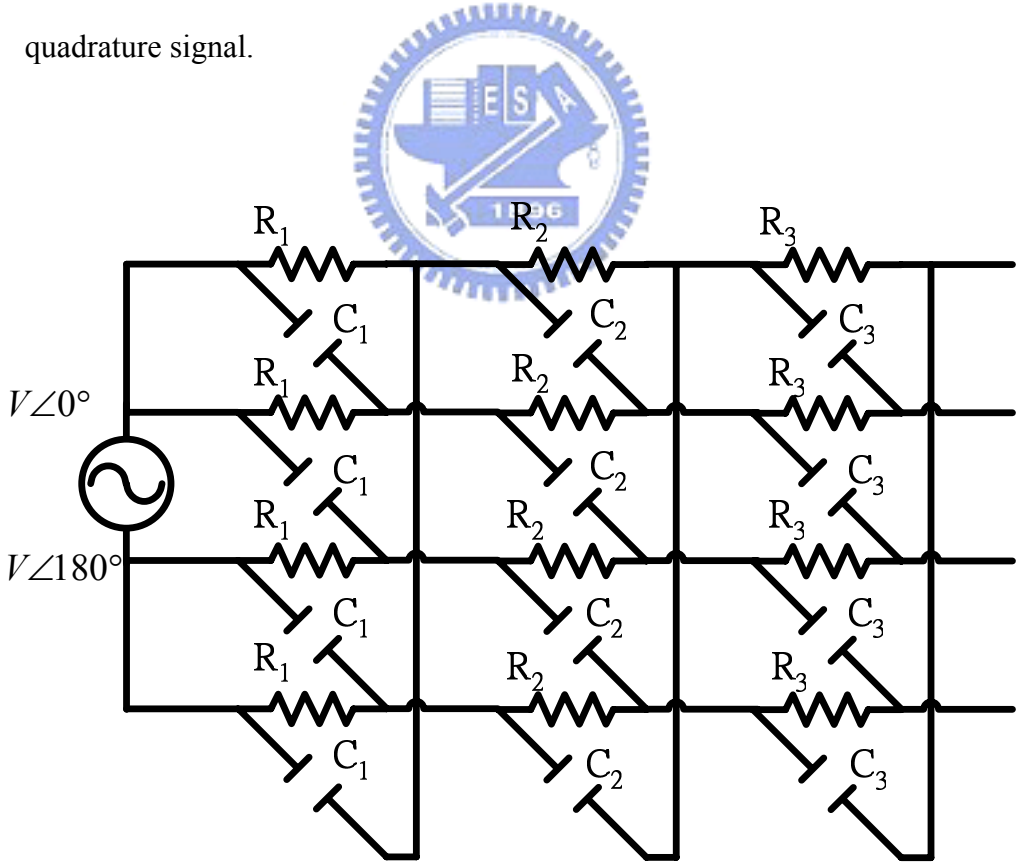


Fig. 3.3. Multistage polyphase filter with different RC pole frequency for each stage, where $(R_1C_1)/(R_2C_2)=(R_2C_2)/(R_3C_3)$.

3.1.2 Coupled Oscillator

Fig. 3.4 is the schematic of the CMOS Quadrature VCO using coupled oscillators, where the cross-coupled FETs M1-M4 and two LC tanks form two differential oscillators, and the balanced output V_B is direct coupled into oscillator (V_A) by the coupling transistor FETs M5-M6 and the balanced output V_A is cross coupled into the oscillator (V_B) by the coupling transistor FETs M7-M8. To understand how these two oscillators in Fig. 3.4 are forced into quadrature phase, we first define g_m as the differential large-signal transconductance of all the FETs, and θ as the phase difference between V_A and V_B, and then the phasor current into the two LC tank can be written as $g_m(V_A \angle 0 + V_B \angle \theta)$ and $g_m(-V_A \angle 0 + V_B \angle \theta)$ respectively. If the two oscillators in Fig. 3.4 are identical in frequency and amplitude, their phasor current will be equal in magnitude and can be written as

$$| V_A e^{j0} + V_B e^{j\theta} | = | -V_A e^{j0} + V_B e^{j\theta} | \qquad (3.5)$$

if $V_A = V_B$, it requires cosθ = 0 to satisfy (3.5), that is $\theta = \pm 90°$ [3.4]. So, V_A and V_B are in quadrature, however, V_A may either lead or lag V_B by 90°. In practice, because the tank is lossy and the frequency dependence of tank impedance is asymmetrical, the oscillation will favor the frequency which can provide largest impedance and only the V_A lead V_B by 90° sustain, the details will be described in next section.

Another type of coupled oscillator is formed by using superharmonic coupling or injection locking [3.5][3.6], as shown in Fig. 3.5. Since forcing the 2nd order harmonic to be in antiphase, the output waveform of the oscillator must be in quadrature. We are going to have the tail network in Fig. 3.5, i.e., L3-L4 and the tail capacitance, being designed to resonate at $2\omega_o$ when V_{S1} and V_{S2} are driven differentially, so as to sustain the differential 2nd-order harmonic at V_{S1} and V_{S2} and

obtain quadrature oscillator output waveform, as depicted in Fig. 3.6. In Fig. 3.5, four FETs, Mp5-Mp8, are added to set the output phase of the nodes I+, Q+, I-, and Q- in the sequence of 0°-90°-180°-270°.

There are still many coupling techniques for low phase noise and low I/Q phase error, and they are summarized in Table. 3.1. As can be seen in this table, advanced technology makes low power consumptions and series coupling technique makes good I/Q phase accuracy.

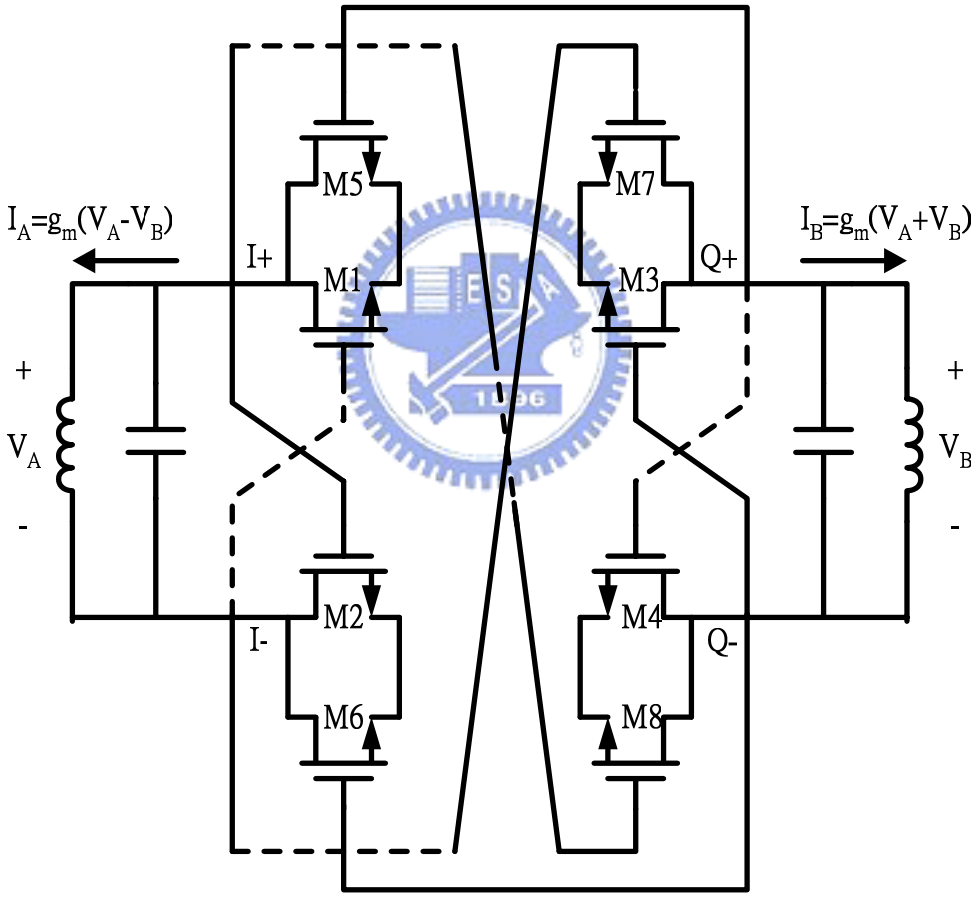


Fig. 3.4. Schematic of transistor coupling quadrature oscillator [3.4].

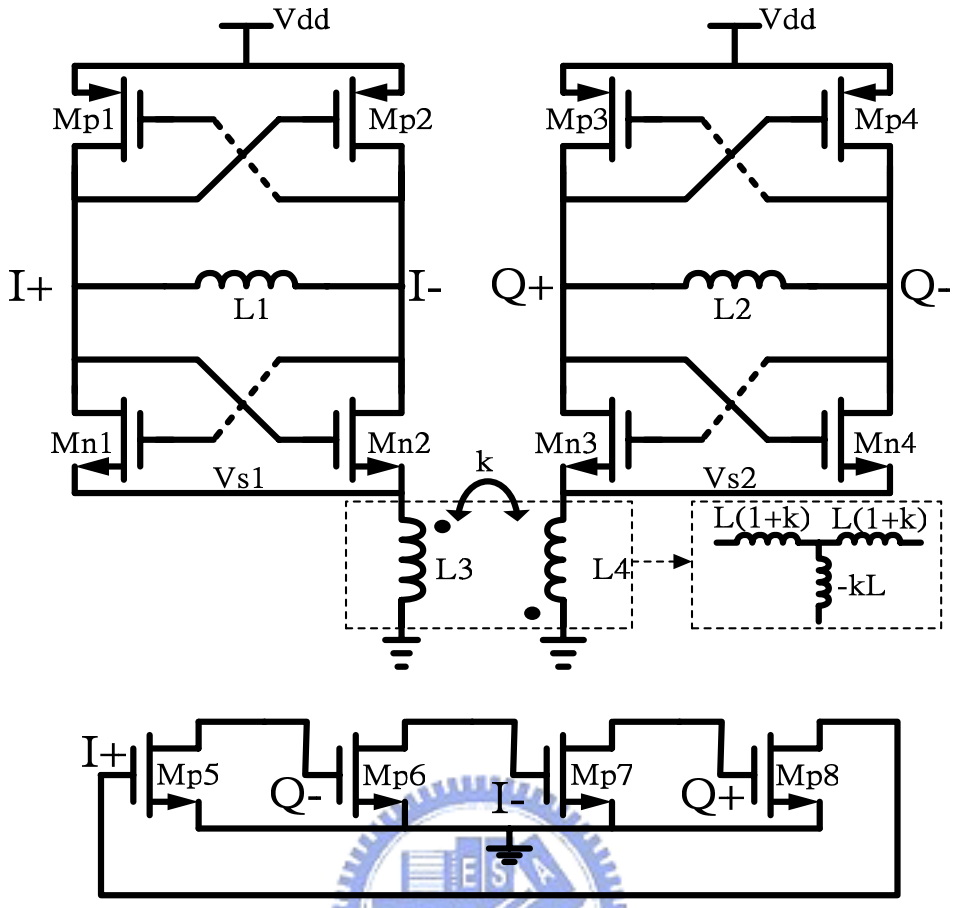


Fig. 3.5. Superharmonic coupled QVCO [3.6].

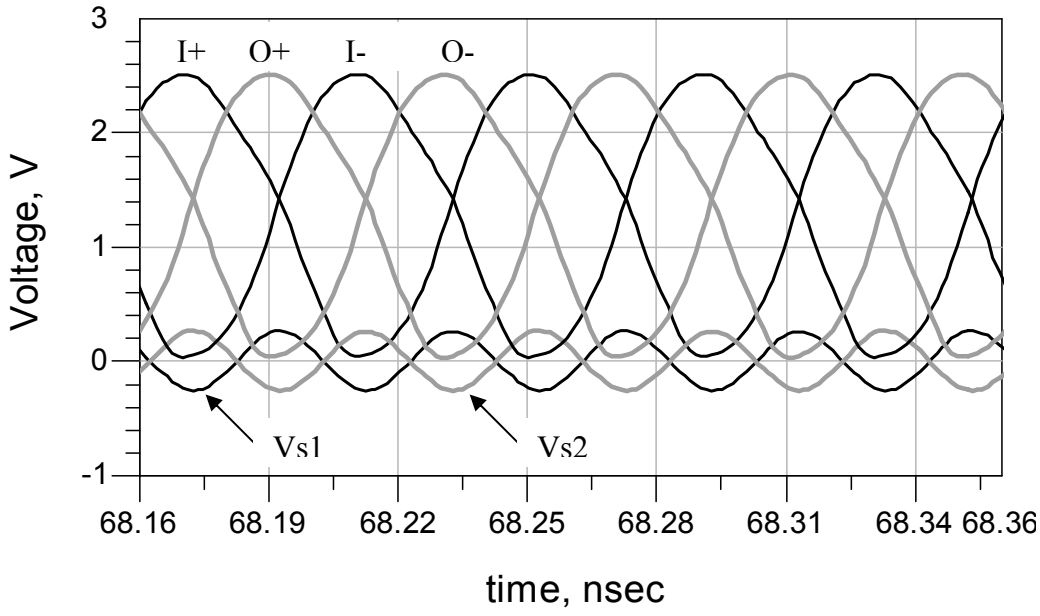


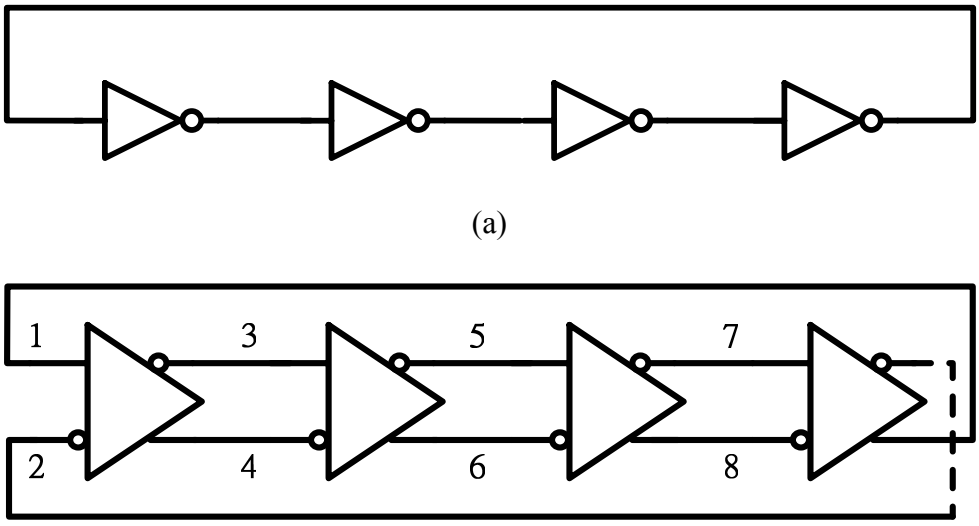
Fig. 3.6. Superharmonic coupled Oscillator's simulated voltage waveform at the output node and common source node [3.6].

Table. 3.1. Performance of different coupling techniques.

	Process	Coupling Technique	Oscillation Frequency	Phase Noise	I/Q phase Error	Power Dissipation
[3.4]	0.35um CMOS	Parallel	0.8-0.9 GHz	-85 dBc/Hz @100 KHz	< 1°	30 mW
[3.9]	0.18um CMOS	Parallel and phase shifter	2.4-2.6 GHz	-115 dBc/Hz @1 MHz	< 1.2°	7.2 mW
[3.7]	0.35um CMOS	Top Series	1.7-1.9 GHz	-132 dBc/Hz @1 MHz	< 0.25°	50 mW
[3.8]	0.35um CMOS	Bottom Series	1.7-1.9 GHz	-130 dBc/Hz @1 MHz	< 0.6°	50 mW
[3.6]	0.25um CMOS	Injection Locking	4.6-5.2 GHz	-124 dBc/Hz @1 MHz	< 3°	22 mW

3.1.3 Ring Oscillators

Because the whole phase delay in ring oscillator need be 180°, a ring structure with even number of delay cells can be used to achieve a quadrature output VCO. However, the output will be stable (or latch up) when even number stages of single-ended delay cell are used, as shown in Fig. 3.7(a). In order to make the 180° phase delay in ring oscillator, differential signaling delay cells are used, as shown in Fig. 3.7(b). In Fig. 3.7(b), the phase delay of one stage is 45°, and the phase delay between Node 3 and 7 or Node 1 and 5 is 90° [3.10].



(a)

(b)

Fig. 3.7. (a) 4- stage single-ended delay cell, (b) 4-stage differential signaling ring oscillator [3.10].

3.1.4 D-FF Frequency Divider

Conventionally, frequency division can be implemented by master-slave Data flip-flop (D-FF) configured as shown in Fig. 3.8, the slave D-FF's data output port (Q) feedback to master D-FF's data input port (D) to make the master-slave D-FFs self-oscillate.

D-FF tracks the input data signal level from port "D" when clock is "High", and next, when clock is "Low", the data from port "D" is transferred to port "Q" and latched until next clock "High" comes. Because the D-FF changes state once every clock cycle, the output frequency is half of clock frequency. Moreover, the phase of clock driving master and slave D-FF are in complement, hence, the output of slave D-FF will be half clock cycle delayed and therefore be in quadrature with the master D-FF output.

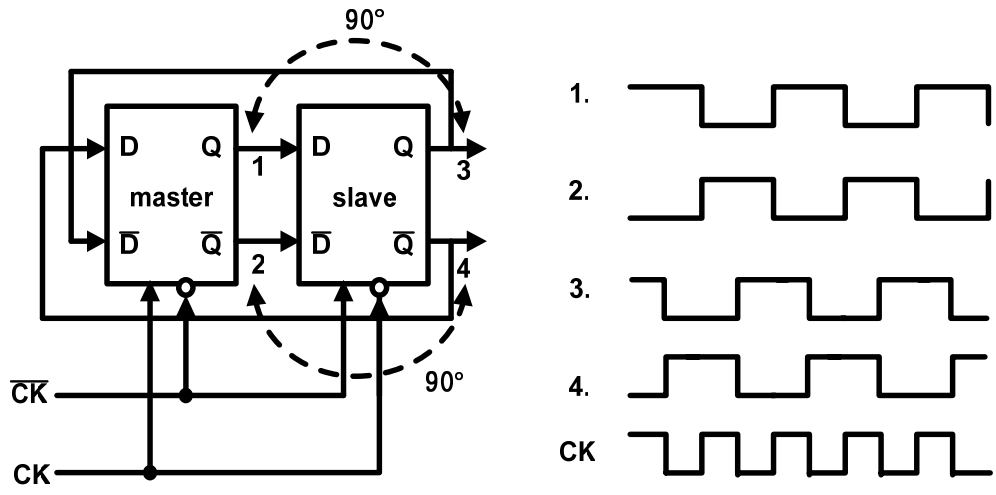


Fig. 3.8. Master-Slave D-FFs configured as a frequency and its timing diagram. 90° phase difference is available between nodes 1 and 3, and nodes 2 and 4.

3.2 Analysis of Quadrature Coupled VCO

3.2.1 Oscillation Frequency

Considering the coupled oscillator which was shown in Fig. 3.4, but redefine that the transconductance of M1-M4 and M5-M8 are g_m and g_{mc} respectively, and the impedance of tank is Z(jω). Therefore, from Fig. 3.4 the current flowing through each tank is given by

$$I_A = g_m V_A - g_{mc} V_B \tag{3.6}$$

$$I_B = g_m V_B + g_{mc} V_A \tag{3.7}$$

and the voltage V_A and V_B can be writen as

$$V_A = (g_m V_A - g_{mc} V_B) Z(j\omega) = (V_A - \frac{g_{mc}}{g_m} V_B) g_m Z(j\omega) \tag{3.8}$$

$$V_B = (g_m V_B + g_{mc} V_A) Z(j\omega) = (V_B + \frac{g_{mc}}{g_m} V_A) g_m Z(j\omega) \tag{3.9}$$

From the above, we can give a model, as Fig. 3.9 shown, to illustrate the coupled

oscillator. Then divide (3.8) by (3.9), it can be shown that $V_A^2+V_B^2=0$, and therefore $V_A = \pm jV_B$ which shows that quadrature output is obtained.

The oscillation frequency can be found by substituting $V_A = \pm jV_B$ into (3.8) or (3.9), defining the coupling coefficient: $m = \frac{g_{mc}}{g_m}$, and $G(j\omega) = g_m Z(j\omega)$

$$(1 \pm jm)G(j\omega) = 1 \tag{3.10}$$

from (3.10), since $G(j\omega) = g_m Z(j\omega)$, we derive the condition on the phase of the tank impedance for any possible quadrature oscillation to occur

$$\phi(Z(j\omega)) = \pm \tan^{-1} m \tag{3.11}$$

(3.11) show that the phase of the tank impedance for quadrature oscillation depends on the coupling coefficient m, and there may be existing ambiguous frequency.

In the following, we show that only one frequency can prevail in the circuit. In real parallel LC tank, we model the lossy inductor as an inductor in series with a resistor, like Fig. 3.10 shows, and the tank impedance Z(jω) is represented as

$$Z(j\omega) = \frac{1}{\frac{1}{j\omega L + R_S} + j\omega C} = \frac{R_S + j(\omega L - \omega^3 L^2 C - \omega {R_S}^2 C)}{(1-\omega^2 LC)^2 + (\omega R_S C)^2} \tag{3.12}$$

since resonance happens when the imaginary part of Z(jω) is zero, the resonant frequency of the lossy LC tank is

$$\omega_r = \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{C{R_S}^2}{L}} \tag{3.13}$$

from (3.13) we can see that the resonant frequency in a lossy LC tank is lower than which in an ideal tank. On the other hand, from (3.12) we can find the magnitude of the impedance Z(jω) as:

$$|Z| = \sqrt{\frac{R_S^2 + \omega^2 L^2}{(1-\omega^2 LC)^2 + (\omega R_S C)^2}} \tag{3.14}$$

, and then solve the equation: $\frac{d|Z|}{d\omega} = 0$ to find the frequency ω_m where the maximum value of |Z| happens, we can see that $\omega_m > \omega_r$:

$$\omega_m = \frac{1}{\sqrt{LC}} \sqrt{\sqrt{1 + \frac{2CR_S^2}{L}} - \frac{CR_S^2}{L}} \tag{3.15}$$

Comparing (3.13) and (3.15), it shows that the tank impedance |Z| at resonant frequency doesn't reach the maximum value, as counterintuitive to the ideal tank, and we say that the frequency dependency of impedance is asymmetrical. This asymmetric property will make oscillator select the frequency at which the tank can provide largest |Z|, or largest loop gain, when the condition (3.11) is satisfied. For this reason, although Fig. 3.11 shows that three possible oscillation frequency may happen when m=1 (i.e., $\phi(Z(j\omega)) = \pm \tan^{-1} m = \pm 45°$), the oscillation sustains only at f_3 for sufficient loop gain.

Back to (3.11), since the impedance phase is dependent on the oscillation frequency, the frequency can be tuned by tuning the coupling coefficient. A tank having small Q value helps a wider frequency tuning range, since the change of the impedance phase in the tank with small Q doesn't makes abrupt change of frequency. The oscillation frequency deviates from resonant frequency is proportional to coupling coefficient by [3.7]

$$\Delta\omega \propto \frac{m}{C} \tag{3.16}$$

where the C stands for the capacitance in the tank.

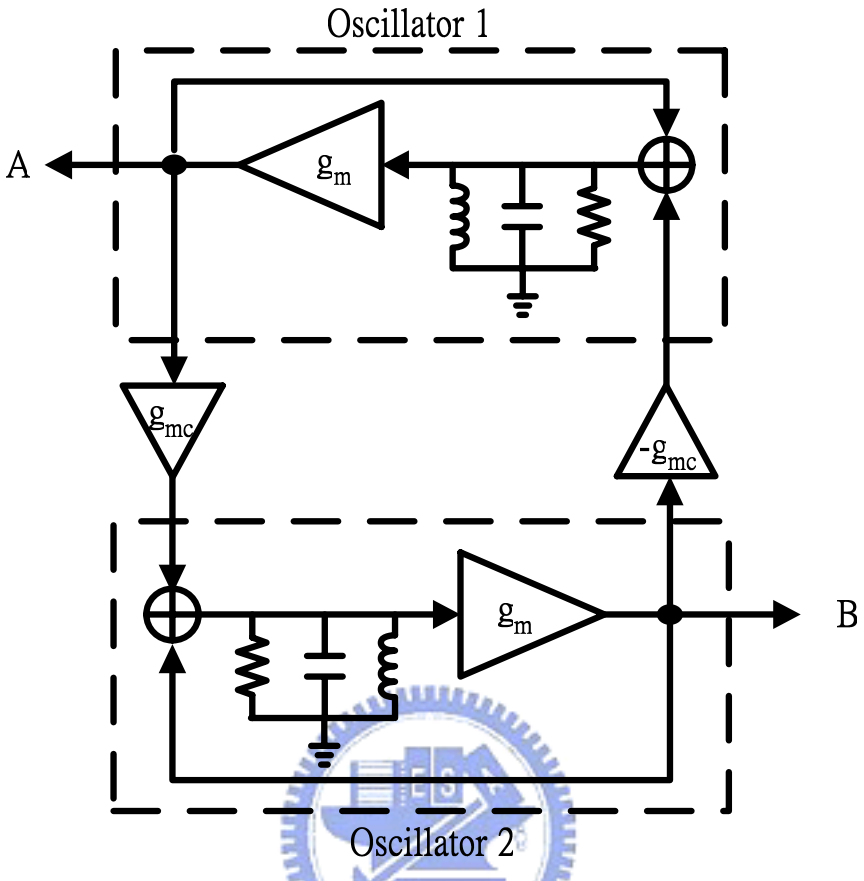


Fig. 3.9. Behavioral model of the coupled oscillator.

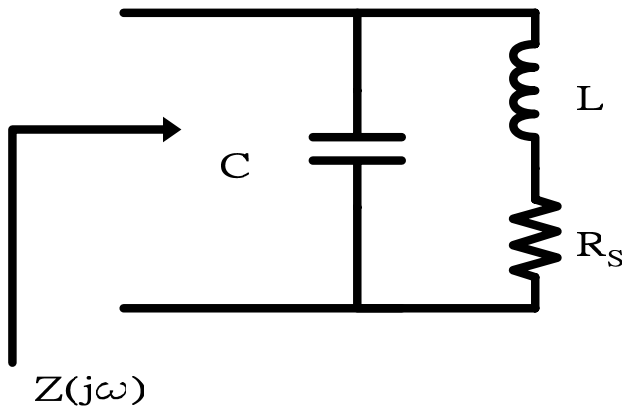


Fig. 3.10. A model of lossy LC Tank.

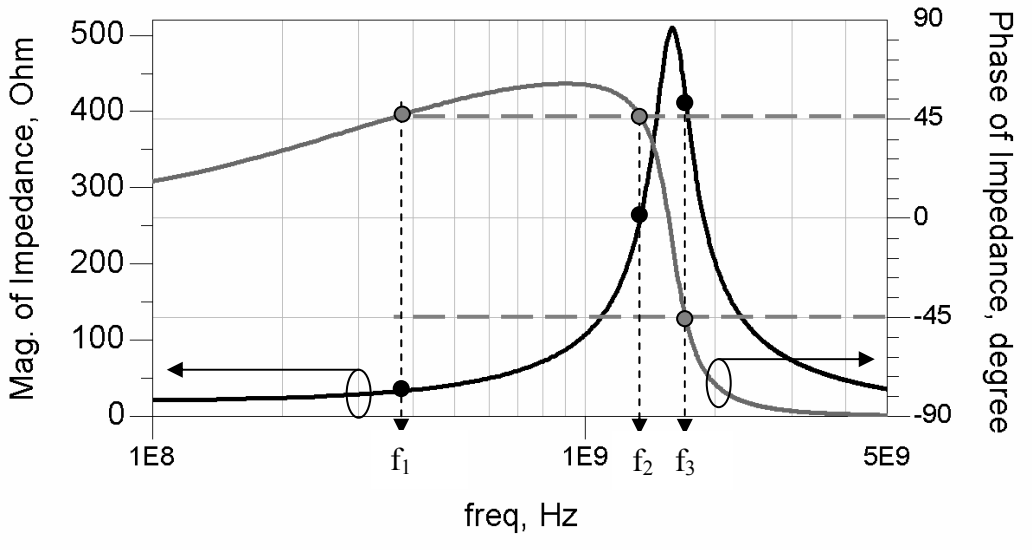


Fig. 3.11. Impedance of the resonator shown in Fig. 3.10, with L = 10 nH, C = 1pF, and Rs=20Ω.

3.2.2 Phase Accuracy

The phase accuracy of the quadrature oscillator is dependent on the mismatches between the frequencies of the differential oscillators. When a frequency mismatch $\Delta\omega$ is introduced, the phase deviation from quadrature $\Delta\phi$ is estimated by [3.11]

$$\Delta\phi = \frac{Q \cdot \Delta\omega}{m^2 \cdot \omega_r} \tag{3.17}$$

(3.17) shows that, at a given $\Delta\omega$, the phase deviation is proportional to Q but inversely proportional to the square of the coupling coefficients, also, the higher resonant frequency helps reduce this deviation.

In addition, according to the QVCO model sketched in Fig. 3.9, if the current injected into the tank from the mutual inductance effect is taken into consideration, the phase deviates from quadrature too [3.12]. Since the current I_{Q1} and I_{Q2}, generated by the coupling transistor, are injected in oscillator 1 and oscillator 2 respectively and they are both in quadrature with the corresponding tank voltage V_A and V_B. Since V_A

and V_B are in quadrature, I_{Q1} and I_{Q2} are in quadrature and they are modeled as

$$I_{Q1} = I_0 \sin \omega t \tag{3.18}$$

$$I_{Q2} = I_0 \cos \omega t \tag{3.19}$$

Ideally, without the mutual inductance, V_A and V_B can be represented as [3.12]

$$V_A = L \cdot Q \cdot \frac{dI_{Q1}}{dt} = I_0 \cdot L \cdot Q \cdot \omega \cdot \cos \omega t \tag{3.20}$$

$$V_B = L \cdot Q \cdot \frac{dI_{Q2}}{dt} = -I_0 \cdot L \cdot Q \cdot \omega \cdot \sin \omega t \tag{3.21}$$

where Q is the quality factor of the LC tank.

When the mutual inductance (M) is taken into consideration, the voltage at V_A and V_B can be represented as

$$V_A' = L \cdot Q \cdot \frac{dI_{Q1}}{dt} + M \cdot Q \cdot \frac{dI_{Q2}}{dt} = I_0 \cdot Q \cdot \sqrt{L^2 + M^2} \cdot \omega \cdot \cos(\omega t + \beta) \tag{3.22}$$

$$V_B' = L \cdot Q \cdot \frac{dI_{Q2}}{dt} + M \cdot Q \cdot \frac{dI_{Q1}}{dt} = -I_0 \cdot Q \cdot \sqrt{L^2 + M^2} \cdot \omega \cdot \sin(\omega t - \beta) \tag{3.23}$$

where $\beta = \tan^{-1}(M/L)$ (3.24)

and a phase difference 2 β is introduced between the quadrature outputs [3.12].

3.2.3 Phase Noise

For differential oscillator, the phase noise in $1/f^2$ region at an offset frequency Δω caused by an individual noise $\overline{i_n^2}/\Delta f$ is [3.13]

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\Gamma_{eff,rms}^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega} \right) \tag{3.25}$$

where $\Gamma_{eff,rms}^2$ is the square of the rms value of the effective impulse sensitivity function and stands for how much phase fluctuation results from the devices' noise

characteristics in the oscillator (Impulse sensitivity function is a function of time standing for how much phase fluctuation results from applying a unit impulse at different instant during the oscillation), $q_{\max}^2$ is the maximum charge swing at the output nodes and equals to $C_{\tan k} \cdot V_{swing}$ or $\frac{V_{swing}}{L_{\tan k} \cdot \omega_r^2}$. For uncorrelated multiple noise source, the total phase noise is obtained by summing the phase noise of the individual noise source applied

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\Gamma_{eff,rms}^2}{q_{\max}^2} \cdot \sum_m \frac{\overline{i_{n,m}^2} / \Delta f}{2 \cdot \Delta\omega} \right) \tag{3.26}$$

So that, in QVCO, since there are extra transistors added for coupling, the phase noise is degraded by the coupling ratio m [3.13].

3.3 A 5.2/5.8-GHz Dual Mode Quadrature VCO

3.3.1 Circuit Implementations

The schematic of this dual mode QVCO is shown in Fig. 3.12. This QVCO is formed by coupling two differential LC tank VCOs via the coupling transistors (Mc1-Mc4).

Each differential LC tank oscillator consists of two cross coupled pair in NMOS and PMOS used to sustain the oscillation. The size ratio of NMOS: PMOS is chosen to be 1:3, for the reason of symmetric waveform [3.14]. The NMOS transistors (Mv1-Mv4) with their source and drain connected together and their bulk connected to ground are used to serve as varactors. See Appendix A for understanding the operation of varactors. To the design of inductors, the goal is setting the Q-peak frequency of the inductors to peak at the resonant frequency of the LC tank. To obtain

the desired Q-peak frequency but keep the desired inductance, we have to adjust the line width and the outer dimension of the inductors at the same time. As a guideline, in the condition of obtaining the desired inductance, the inductor in wider line width and larger outer dimension has a lower Q-peak frequency, and vice, a higher Q-peak frequency is obtained [3.15].

In Fig. 3.12, four PMOS (Mc1-Mc4) are used for quadrature coupling with their gate being connected to the VCOs' output as indicated. To tune the frequency coarsely, the sources of the coupling transistors are separated from the sources of the cross coupled PMOS. Therefore, we further tune the frequency by varying the supply voltage Vdd2 to change the g_m of the coupling transistors. For strong coupling coefficient, the size of Mc1-Mc4 is chosen to be the same as that of the cross coupled PMOS.

Output buffers are added at the output the QVCO for driving the spectrum analyzer. Fig. 3.13 (a) shows the inverter type output buffer, and the size of the transistors are the same as which is used in the cross coupled pair of the VCO.

Furthermore, we need a single sideband mixer (SSB mixer) to evaluate the accuracy of quadrature phase at the output. Fig. 3.13 (b) shows the SSB mixer where the LO-signal is from the QVCO, and the 10 MHz IF quadrature signal is from external signal generator. See Appendix B for detail quadrature phase measurement descriptions.

The circuits described above will be integrated in single chip, as Fig. 3.14 shown, the output buffers are not only used to drive the SSB mixer directly but are also used to drive the spectrum analyzer for measuring the phase noise.

The fabricated chip is shown in Fig. 3.15, the PADs are layout for both on-wafer pitch 150μm probing and printed circuit board (PCB) measurement.

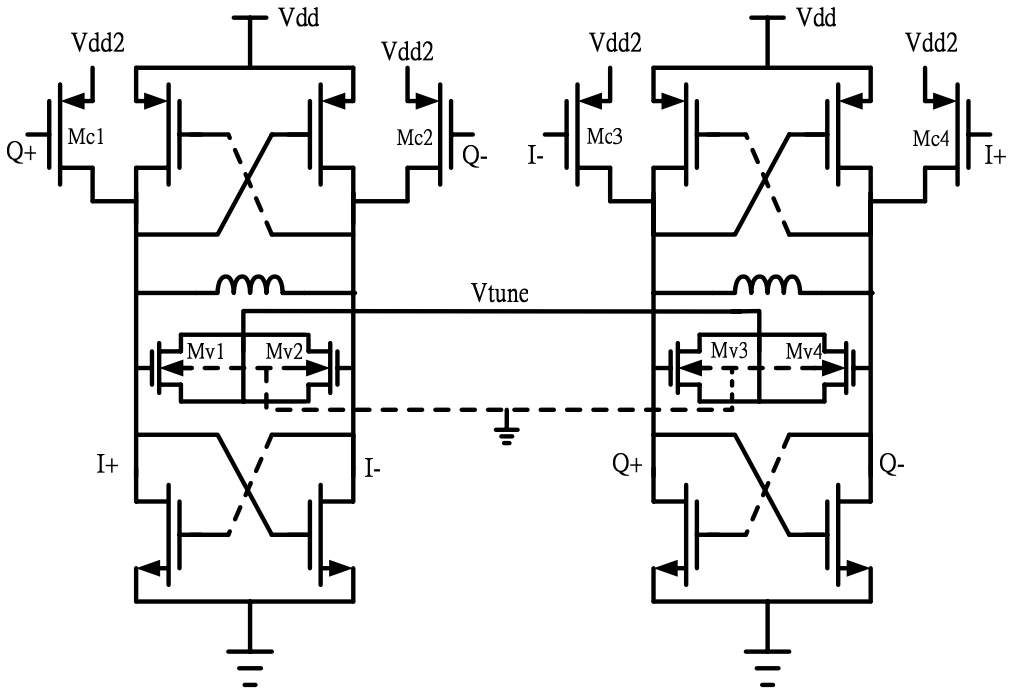
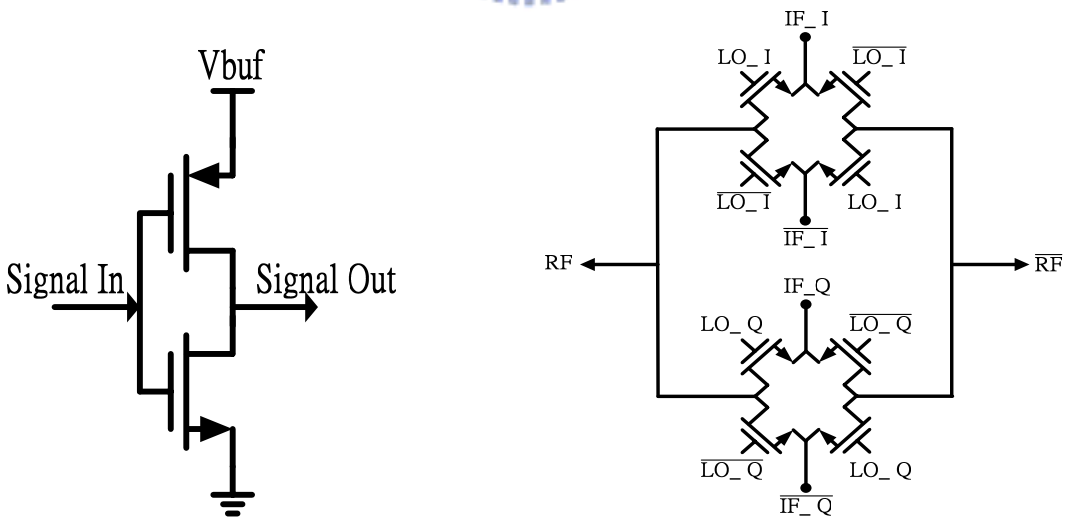


Fig. 3.12. Schematic of the QVCO in this work.



(a) (b)

Fig. 3.13. Required circuits for measurement. (a) output buffer for spectrum measurement, (b) SSB mixer for estimating quadrature output accuracy.

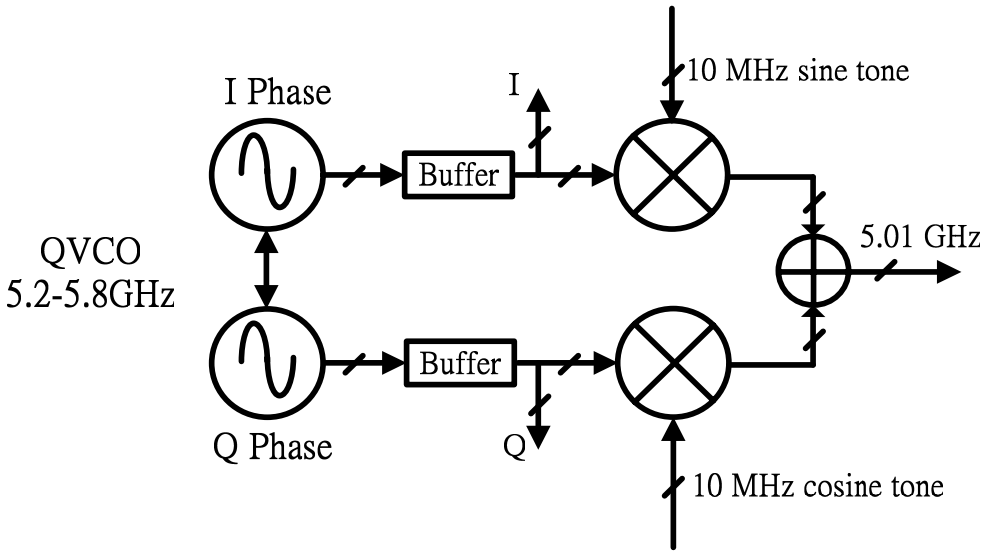


Fig. 3.14. Block diagram of the Chip architecture for measuring the phase noise and quadrature accuracy.

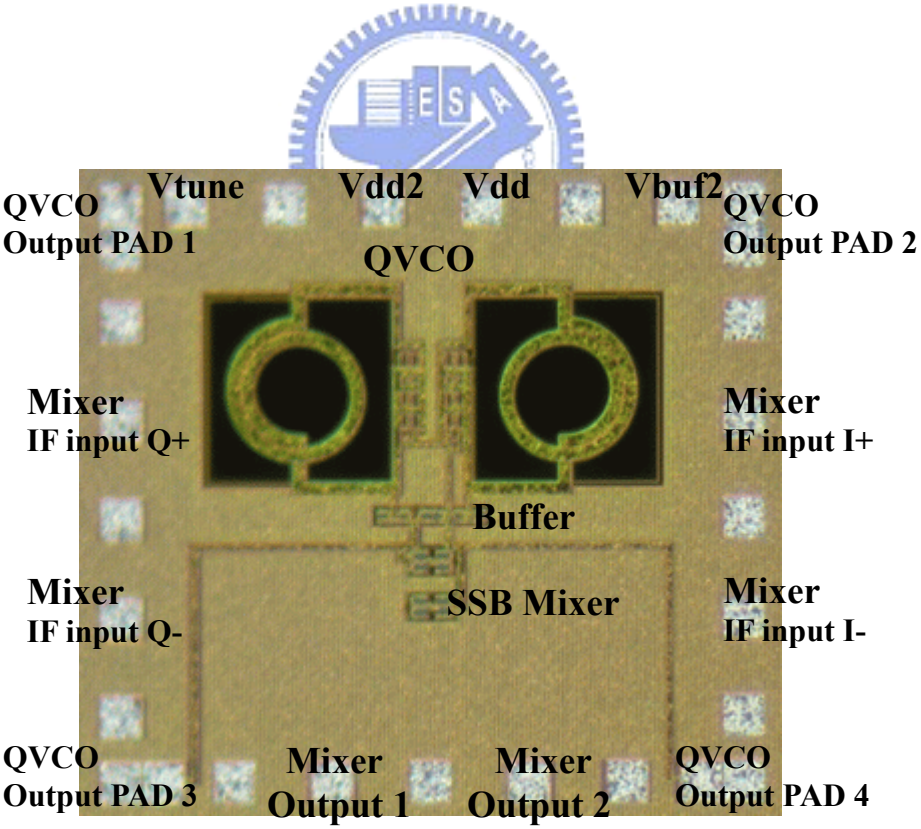


Fig. 3.15. Chip photo of the dual mode QVCO fabricated in 0.18mm CMOS technology.

3.3.2 Experimental Results

This QVCO is biased at Vdd=Vdd2=1.5V, and consume 4 and 7 mA from Vdd and Vdd2 respectively.

On chip measurement is performed for measuring the quadrature accuracy of the QVCO, and a SSB mixer is fabricated in the chip. An external signal source is used to provide a 10 MHz, 0.05-Vpp quadrature signal to the SSB mixer. Measuring the spectrum of the upconverted signal, we observe that one of the sideband is suppressed, as shown in Fig. 3.16 (the biasing condition is changed to Vdd2=1.8V but Vdd=1.5V to obtain this result), and we see that the power ratio of the unsuppressed sideband to the suppressed one (called Image Rejection Ratio - IRR) is about 10 dB. Besides, we measure the output power difference at the quadrature ports, it shows a 1.5 dB difference. According to (B.5), given the $(1+\Delta A)=1.18$ and IRR=10dB, the calculated I/Q phase error $\Delta\theta$ is around 34°.

In order to measure the output spectrum of the QVCO, the outputs of the buffers are also direct to four correspondingly bonding PADs. Therefore, we mount and wire-bonding this chip on a PCB and measure the output spectrum. The setup of PCB measurement is shown in Fig. 3.17 and Fig. 3.18, three 50Ω load is used to terminate the unused output ports. In Fig. 3.19, since a 10 kHz resolution bandwidth is set in the spectrum analyzer, we obtain that the spectrum density is -109 dBc/Hz at 1MHz offset from the carrier (a 1.5-V battery is applied at the same time to Vdd, Vdd2, V_{buf} and Vc to obtain this result).

The frequency tuning characteristics is obtained in the condition of using a fixed Vdd (=1.5-V) but different Vdd2 (i.e., Vdd2 = 1.2, 1.5, and 1.8 V, and the higher the Vdd2, the lager the coupling coefficient m), as shown in Fig. 3.20, each curve has a

K_{VCO} around 190 MHz/V. The biasing current variation in the condition of a fixed Vdd and varied Vdd2 is shown in Table. 3.3, it shows that a large current variation (or coupling coefficient) is required for the desired frequency tuning.

Table. 3.3 shows the performance summary compared to the QVCO implemented by transistor parallel coupling [3.4] and transistor serial coupling [3.7].

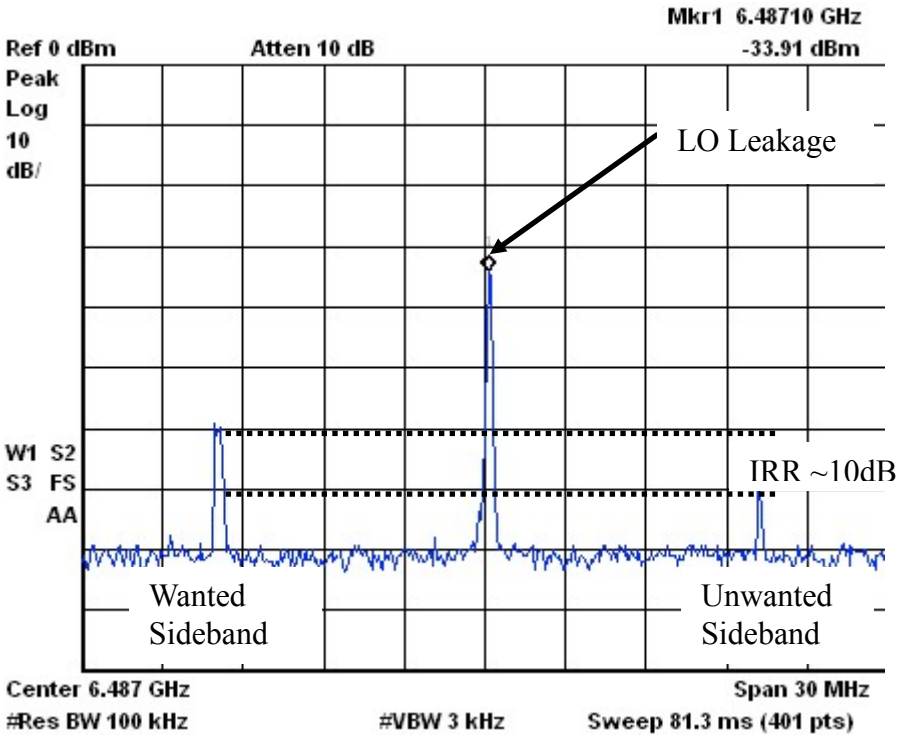


Fig. 3.16. Image rejection ratio (IRR) measurement.

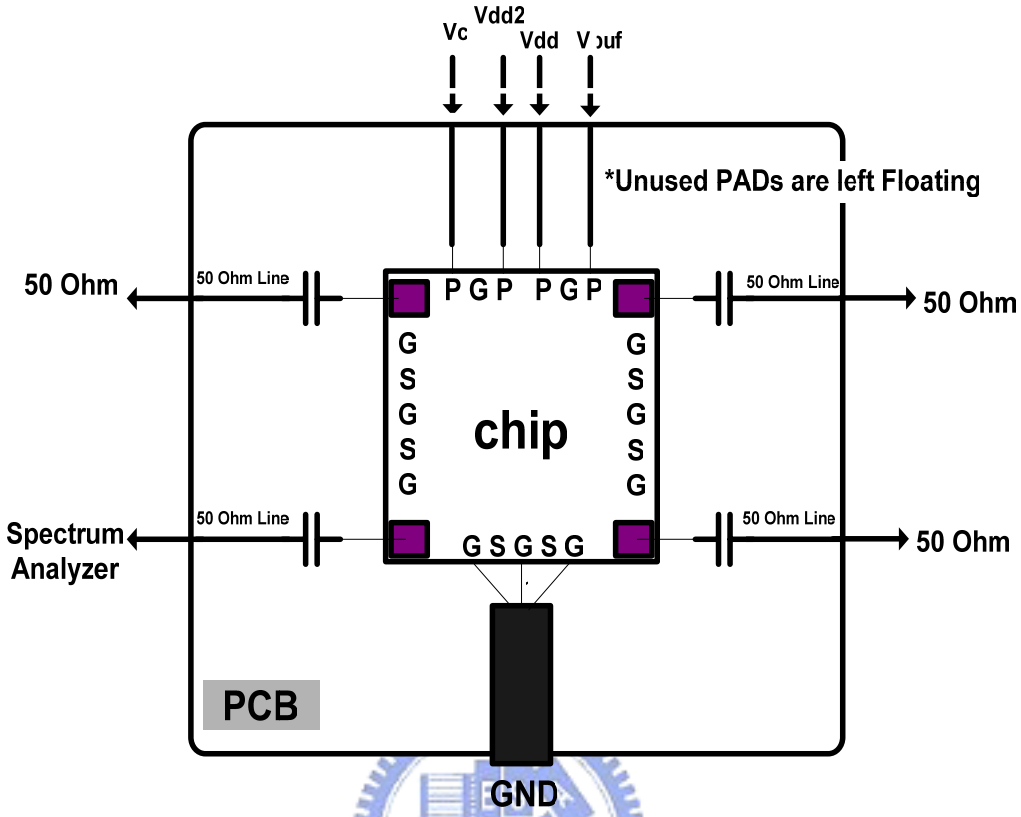


Fig. 3.17. PCB layout and measurement setup for phase noise measurement.

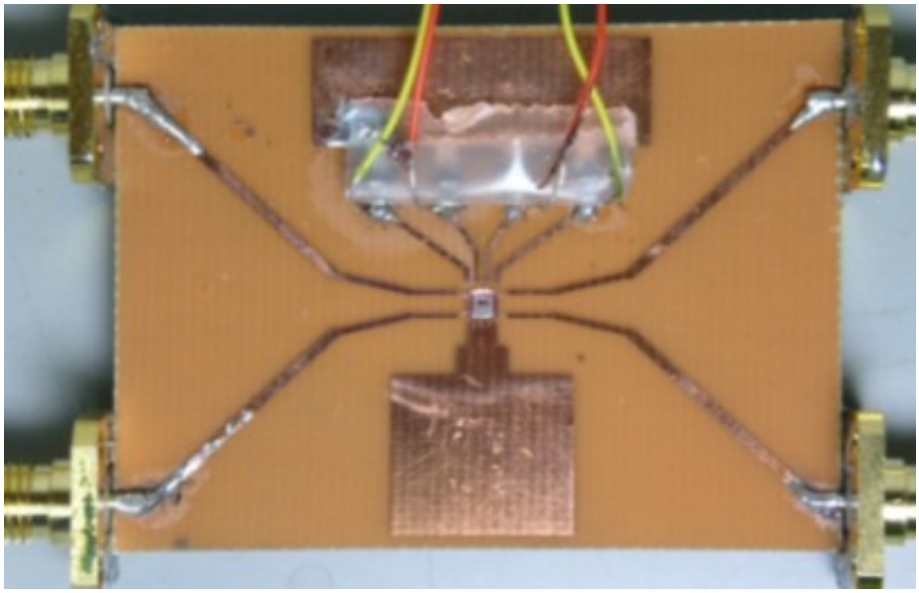


Fig. 3.18. Photo of the PCB for phase noise measurement.

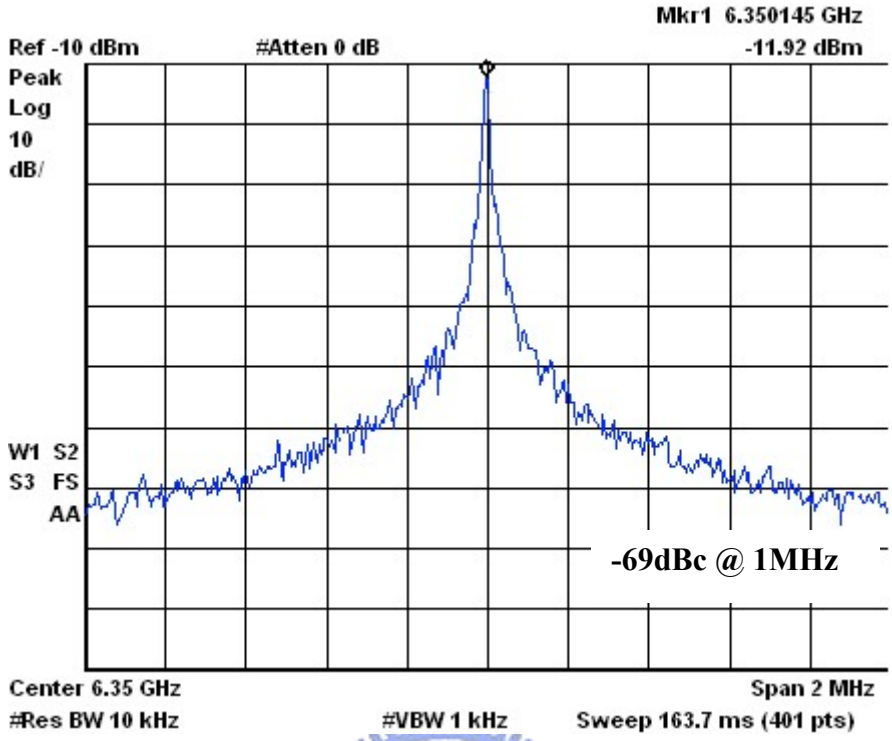


Fig. 3.19. QVCO output spectrum when 1.5-V battery is used for biasing.

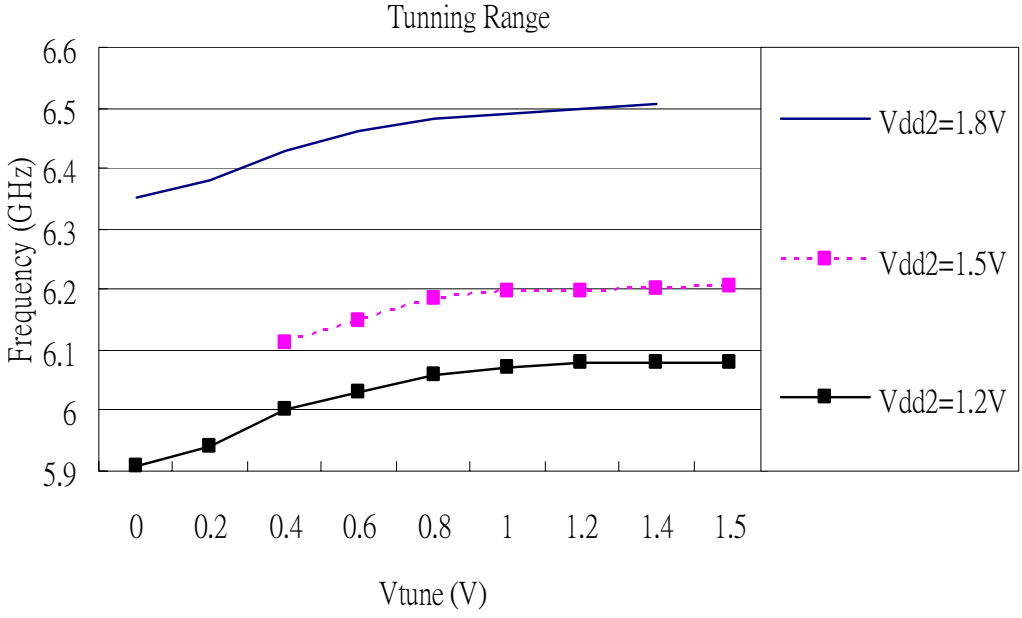


Fig. 3.20. Frequency tuning characteristics of the dual mode QVCO.

Table. 3.2. Biasing current variation at Vdd =1.5-V and varied Vdd2.

	Vdd2= 1.2V	Vdd2 = 1.5V	Vdd2=1.8V
Idd	6 mA	4 mA	1 mA
Idd2	1 mA	7 mA	15 mA

Table 3.3. Performance Summary of the dual mode QVCO.

	Simulated	Measured	[3.4]	[3.7]
Technology	0.18 μm CMOS	0.18 μm CMOS	N/A	0.35 μm CMOS
Vdd	1.5 V	1.5V	3 V	2 V
Supply Current	< 16 mA (Vdd2=1.8V)	< 16 mA (Vdd2=1.8V)	10 mA	25 mA
Frequency Tuning（GHz）	6.1 ~ 6.8 (Transient) 5.1~5.9 (Harmonic Balance)	5.9~6.5	0.8 ~ 0.9	1.64 ~ 1.96
KVCO (MHz/V)	< 250	180	200	N/A
Phase-noise (dBc/Hz)	< -107 @1MHz	-109 @1MHz	-85 @100 KHz	-140 @3MHz
Quadrature Error	N.A.	34 °	1 °	< 0.25 °

3.3.3 Discussions

Most of the measurement results are fairly identical to the circuit simulation, except the poor quadrature phase accuracy. We assert that this may be introduced by the inductor coupling effect, so we use EM simulator – Ansoft Designer to confirm this assertion. Fig. 3.23 shows the layout of the inductors in our circuit and their extended connection line to the circuit, the distance between the centers of these two inductors is around 400um and the distance between the medium of port #2 and #3 is around 30um. We first simulate the four ports S-Parameter, and then calculate Z(2,3) with port #1 and #4 grounded. We calculate the mutual inductance M by

$$M = \frac{\mathrm{Im}(Z(2,3))}{2 \cdot \pi \cdot f} \tag{3.27}$$

Fig. 3.22 shows that the inductance and mutual inductance are 1.771 nH and 0.12nH respectively, and from (3.24) we obtain a 7.72° quadrature phase error. There exists some other mechanism, such as asymmetric circuit layout, to cause the poor measured phase error. On the other hand, we separate these two inductors far away around 600um between their centers, as Fig. 3.25 indicated, a smaller M around 10% reduction with respect to simulated mutual inductance in our design is obtained. So, we may conclude that we have to reduce the mutual inductance by proper layout, such as preventing the side-by-side parallel lines and separating the inductors far apart.

Besides, as a reference, the result shown in [3.12] points out that the quadrature phase error makes by a 15% mutual inductance of the tank inductor can only achieve a 15dB image rejection ratio when this quadrature signal is applied to single side-band mixer, which also shows that the impact of the mutual inductance to the quadrature error.

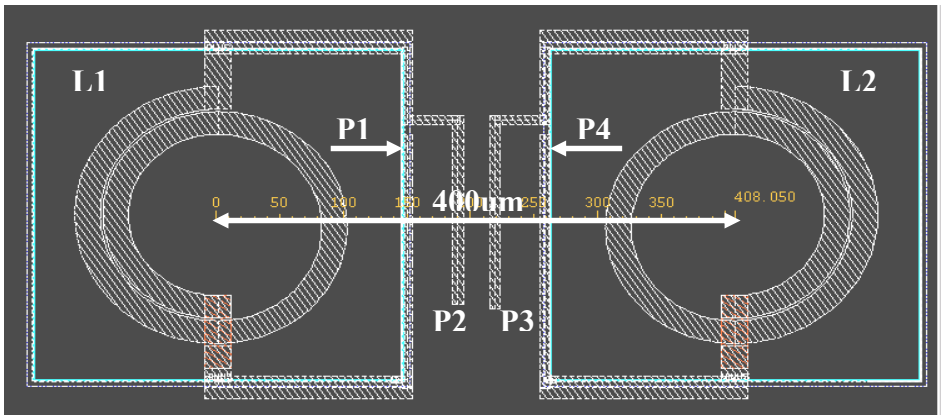


Fig. 3.21. Layout of the inductors including the connection leads in our circuit, the inductors are separated 400um center-to-center far apart.

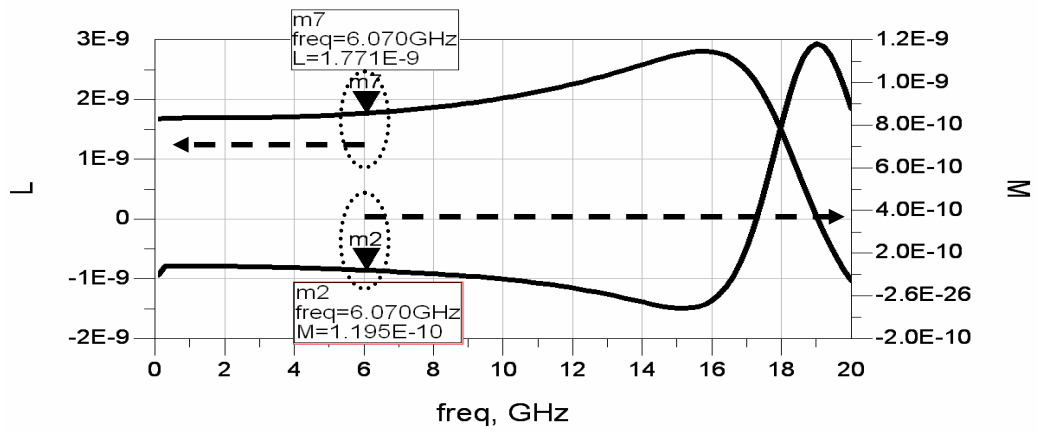


Fig. 3.22. Self and mutual inductance value of the inductors.

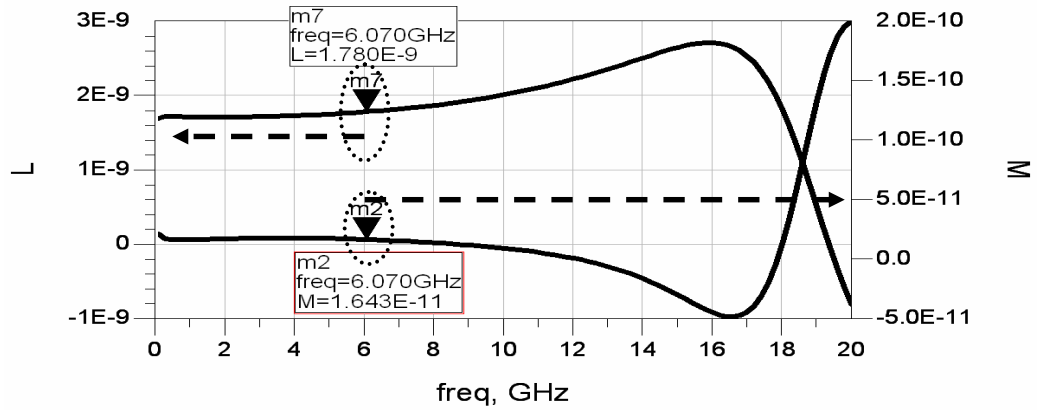


Fig. 3.23. Self and mutual inductance value of the inductors separated 600um far apart.

CHAPTER 4

Applications of Frequency Dividers and Quadrature VCOs

4.1 A 2.4/5.8-GHz Dual-Band Quadrature VCO

A conventional and straightforward way to handle different communication standards in one set is using separate circuit modules for each standard. Recently, dual-band direct conversion receiver front-end architectures capable of sharing the building blocks for different standard have been proposed [4.1], however, the following problem is the dual-band LO signal source. Several methods are proposed for generating dual-band LO signal, such as using switched-inductor to change the inductance [4.2] and analog frequency multiplication by using mixers to generate fractionally separated frequency [4.3]. However, they may have either a large "footprint" or high complexity. In this section, we use QVCO followed by frequency divider to generate dual-band quadrature signal.

4.1.1 Circuit Implementations

Fig. 4.1 shows the circuit block diagram generating dual-band quadrature signal. In this diagram, the frequency of the QVCO is 4.6-6 GHz and its in-phase output signal is used to drive the frequency divider to generate 2.3-2.5 GHz quadrature signal, as described in section 3.1.4. Buffers are added for proving the driving capability of

the oscillation signal. Fig. 4.2 shows the schematic diagram of the QVCO, supply voltage Vdd and Vdd2 are set to be 1.5-V, but Vdd2 is disconnected from Vdd for further frequency tuning. Besides, the components used in the QVCO are the same as the last design except that the varactors are replaced by accumulation mode MOS transistors for wide frequency tuning range. See Appendix B for the basic analysis on the varactors.

Fig. 4.3 shows the block diagram of the frequency divider configured by master-slave D-FFs. As mentioned before this frequency divider provides quadrature phase signal. The requirements of high frequency D-FF design is lowering the RC time constant at the output nodes of the D-FF or increasing the supply current [4.4]. The circuit schematic of D-FF is shown in Fig. 4.4, where the supply voltage is set to be 1-V.

The operation of D-FF can be separated into two phases, sensing and latching. In sensing mode, Mn5 is turned on by clock signal, and then Mn1 and Mn2 are biased in saturation region to serve as a differential amplifier sensing the voltage difference of the input signals. The size of Mn5 is chosen to be large, so as to provide large current, and the size of Mn1 and Mn2 are chosen small to reduce parasitic capacitance at output nodes. Besides, Mp1 and Mp2 operate in linear region to serve as a resistive loading and help to lower the supply voltage. We choose small Mp1 and Mp2 for small parasitic capacitance at output node and hence high speed operation. Since the biasing current is high, both Mp1 and Mp2 (in linear region) have low resistance for high speed operation.

In latching mode, Mn6 is turned on by the inversed clock signal and then the output from the differential amplifier (that is the inversed voltage difference of the input signal) is kept by the cross coupled pair, Mn3 and Mn4. The size of Mn6 is

chosen to be smaller than Mn5, so the biasing current is small in the latching time. At this time, Mp1 and Mp2 (in linear region) have high resistance and then large voltage difference can be output.

The DC voltage Vb at the gate of Mn5 and Mn6 is set to be around the threshold voltage of the transistors, so that the clock signal can switch the transistor in equal time duration. In our dual band circuit, we take in-phase output signal from QVCO to be the clock signal driving the DFF.

In Fig.4.5, we use two types of output buffer for QVCO and frequency divider respectively. In Fig. 4.5 (a), an inverter is used and the transistors size of NMOS and PMOS are set to be the same as which in the QVCO. In Fig. 4.5 (b), the common source amplifier is used for the reason of parasitic capacitance reduction, so as to achieve high speed operation of the frequency divider.

Fig. 4.6 shows the circuit fabricated in UMC 0.18um CMOS technology, the dual band signals are obtained at different PADs..

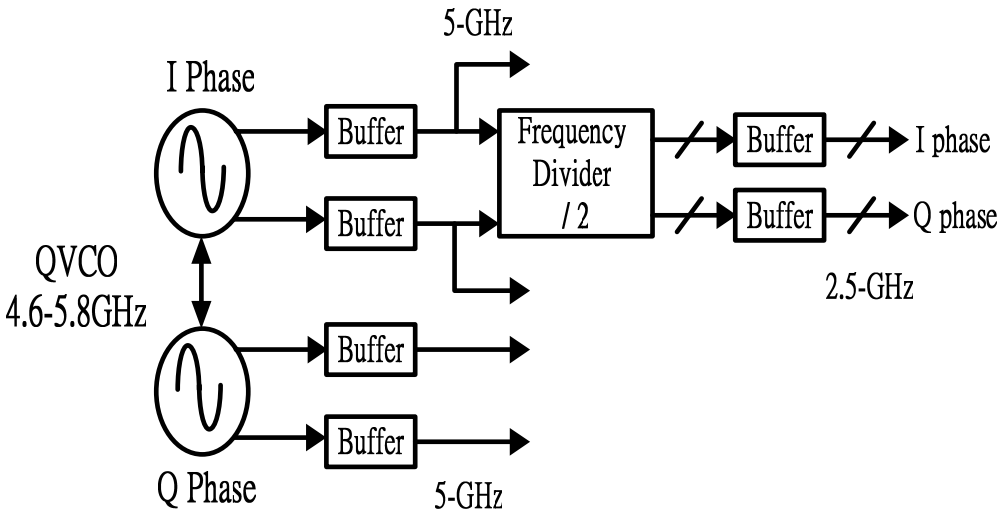


Fig. 4.1. Block diagram of Dual Band Quadrature VCO.

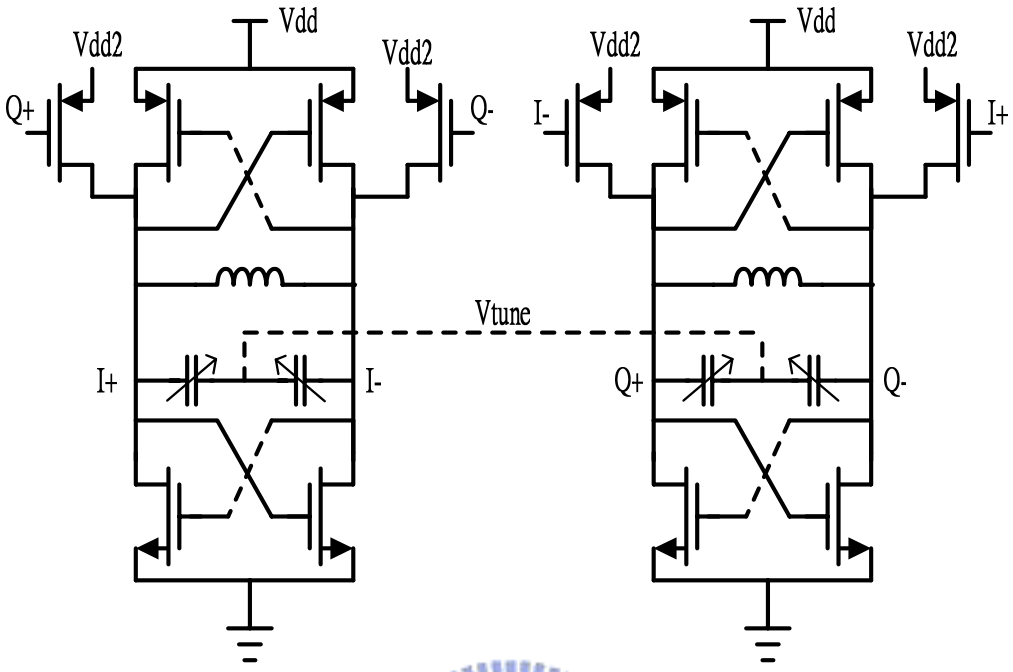


Fig. 4.2. Schematic of the QVCO using Vdd 1.5-V.

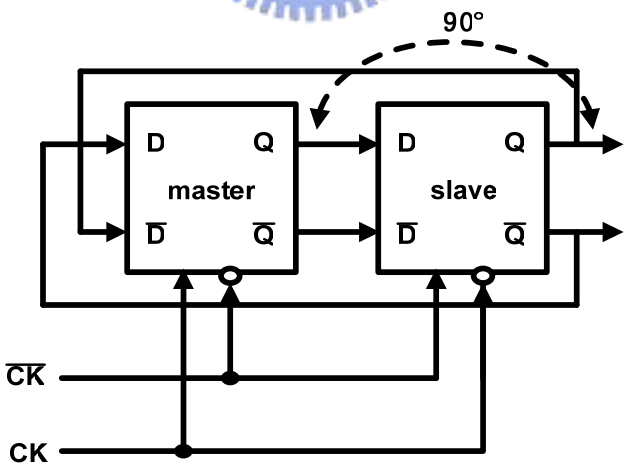


Fig. 4.3. Master-Slave DFFs as a Frequency Divider.

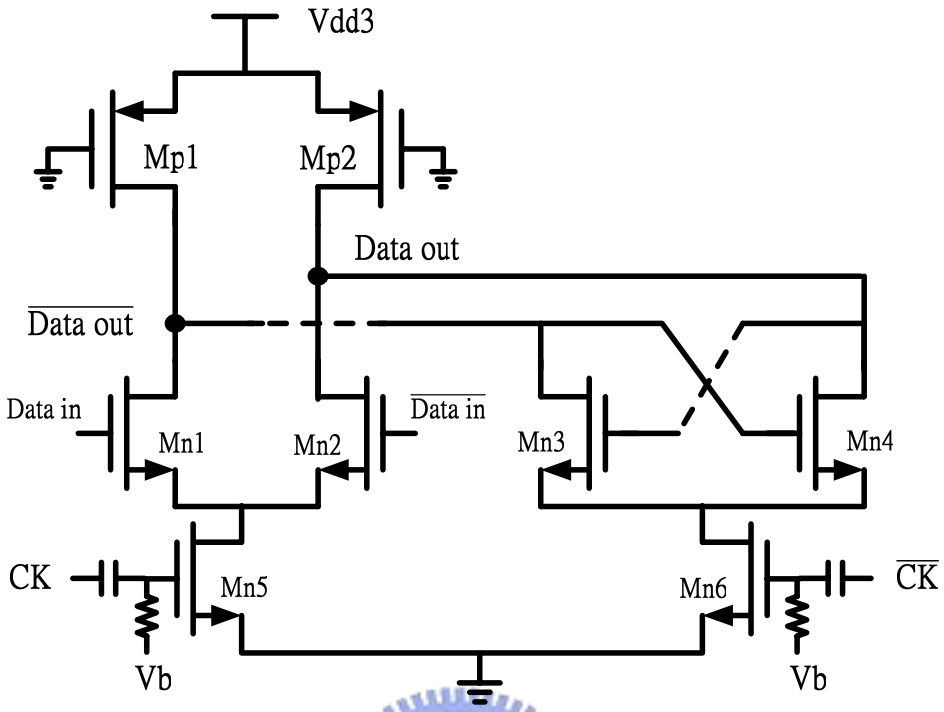


Fig. 4.4. Schematic view of the D Flip-Flop using Vdd3=1-V.

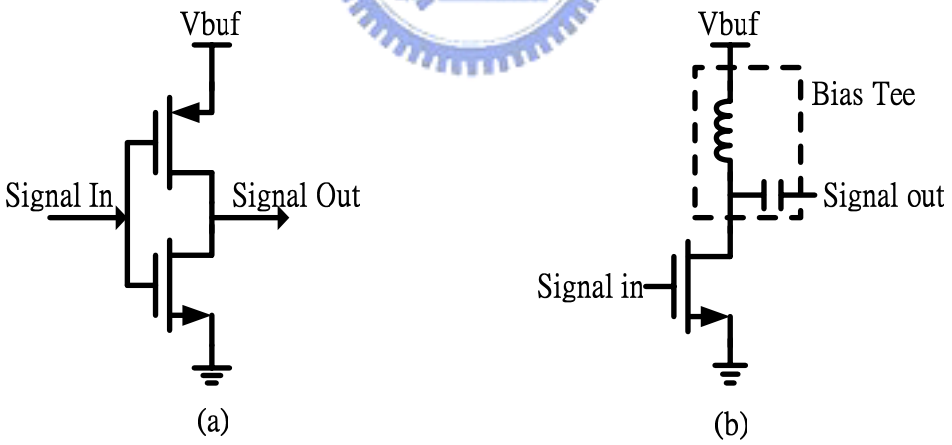


Fig. 4.5. The output buffer used (a) for QVCO, (b) for frequency divider.

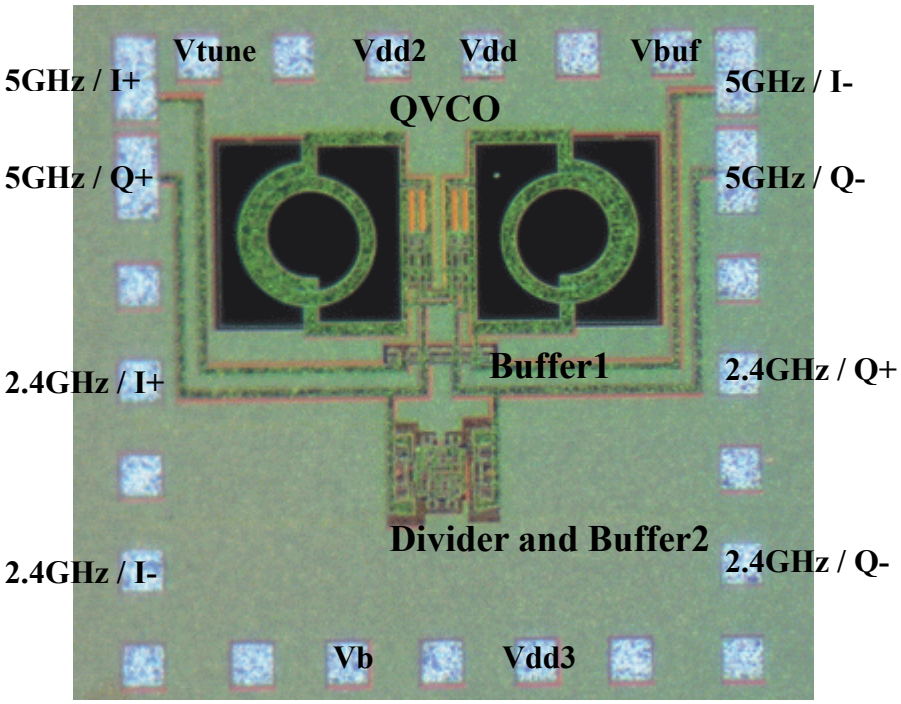


Fig. 4.6. The Dual-Band Circuit fabricated in UMC 0.18μm CMOS technology.

4.1.2 Experimental Results

In the part of the QVCO measurement, we measure it by three case of biasing condition,

Case 1: QVCO is biased at Vdd=Vdd2=1.5V, and drawing 5 mA and 4 mA from Vdd and Vdd2 respectively.

Case 2: QVCO is biased at Vdd=1.5V and Vdd2=1.8V, and drawing 2 mA and 10 mA from Vdd and Vdd2 respectively.

Case 3: QVCO is biased at Vdd=Vdd2=1.8V, and drawing 8 mA and 7 mA from Vdd and Vdd2 respectively.

We measure the output spectrum via the chip mounted on the PCB circuit, as shown in Fig. 4.7. In biasing condition case 1, the output power is around -12 dBm; in case 2,

we obtain an output power around -20 dBm, since less current flows into the cross coupled pair, and in case 3, we obtain the output power around -3 dBm, these result show us that the output power is proportional to the current flowing into the cross coupled pair, as summarized in Table 4.1. As indicated by Fig. 4.8, the frequency tuning curves of QVCO in these three cases are measured, and it shows that case 2 satisfies our frequency requirement (5.2~4.6 GHz).

For phase noise measurement, all the DC biasing voltage and control voltage are supplied by a 1.5-V battery. The output spectrum of QVCO is shown in Fig. 4.9, the power spectrum at 1MHz offset from the carrier frequency is 73 dB lower than the carrier power. Since the resolution bandwidth setting of the spectrum analyzer is 10 kHz, calculating the spectrum density, we obtain a -113 dBc/Hz phase noise @ 1MHz offset.

Instead of using the SSB mixer, this time, the quadrature phase accuracy is characterized by Vector Network Analyzer (VNA). The calibration procedure to the VNA must be very precise, since the phase measurement at high frequency is very sensitive to the misplacement of the connector. We measure the 2-ports S-parameter at the quadrature ports at the frequency from 4.5 to 5.5GHz and investigate the S11 and S21. When the oscillator is injection locked by the testing signal from VNA, we obtain a injection gain around 3dB at 5.286GHz, as shown in Fig. 4.10. Then, we obtain the phase difference at the quadrature ports by calculate $\angle$S21-$\angle$S11 at 5.286 GHz, and the result is 119°-76° = 43°, as shown in Fig.4.11. See appendix B for detail explanations to this method.

After completing the QVCO measurement, we turn to measure the frequency divider. The same PCB layout is used but we shift its signal line to an appropriate position for bonding the chip's PADs connected to the output of the divider. This

divider is biased at Vdd3=1.2V and Vb=0.65V, and it draws 4mA and 0mA from Vdd3 and Vb respectively. A function of frequency division by 2 is shown in Fig. 4.12, the output power of the carrier is 20 dB higher than the 2nd harmonic. In Fig. 4.13, when the QVCO is biased at case 3 without using battery, the measured phase noise is -121 dBc/Hz at 1MHz offset from the carrier. Tuning the frequency of QVCO when it is biased at case 3 without using battery, we obtain the frequency tuned from 1.96 to 2.5 GHz at the output of divider, as shown in Fig.4.14.

Table 4.2 and Table 4.3 show the summary of the individual circuit in dual band signal generation circuit with comparisons to other corresponding design.

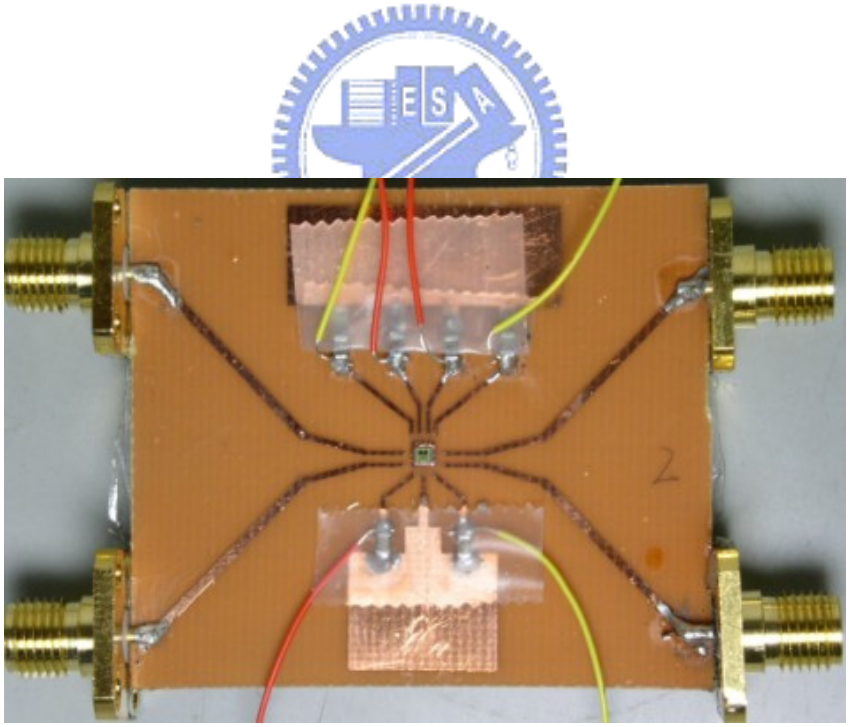


Fig. 4.7. The PCB testing board.

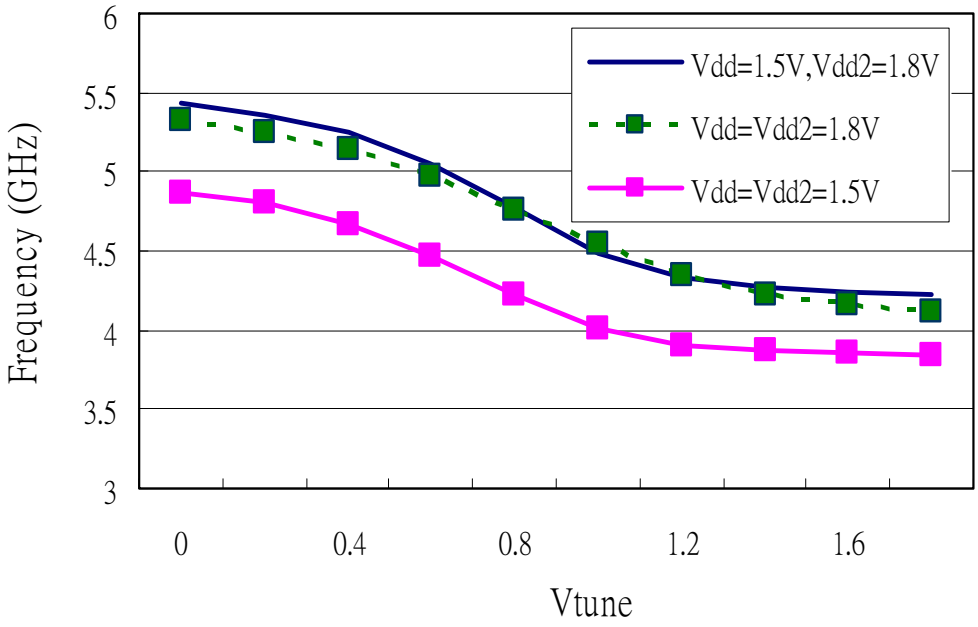


Fig. 4.8. Frequency tuning curve under different biasing conditions.

Table. 4.1. Output power of the QVCO under different biasing condition.

	Vdd=Vdd2= 1.5V	Vdd=1.5V, Vdd2 = 1.8V	Vdd=Vdd2=1.8V
Idd	5 mA	2 mA	8 mA
Idd2	4 mA	10 mA	7 mA
P_{out}	-15 dBm	-20dBm	-3 dBm

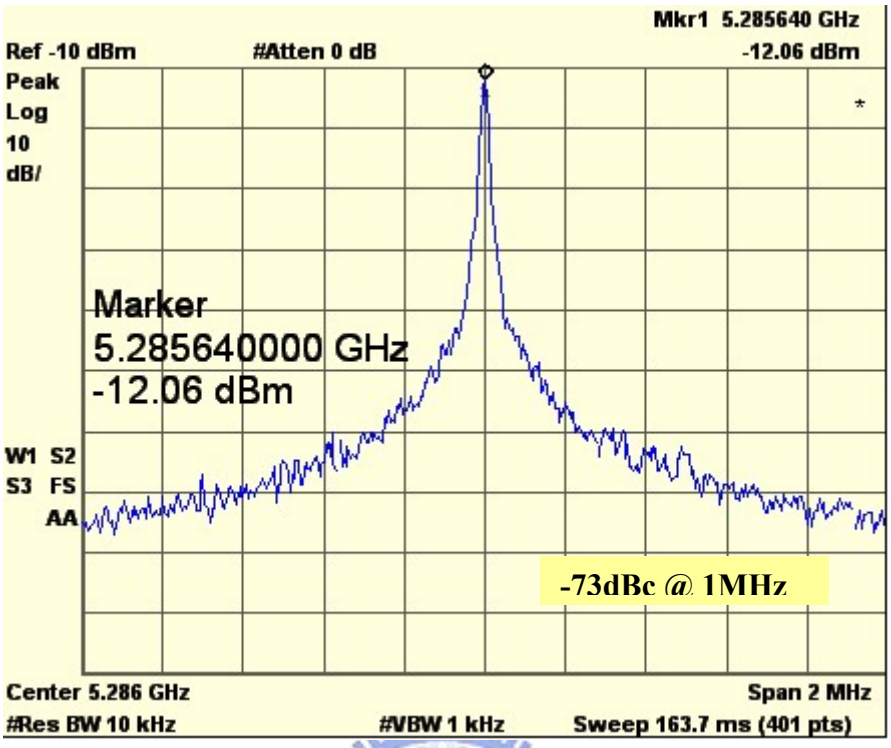


Fig. 4.9. Output spectrum of QVCO powered by a 1.5-V battery.

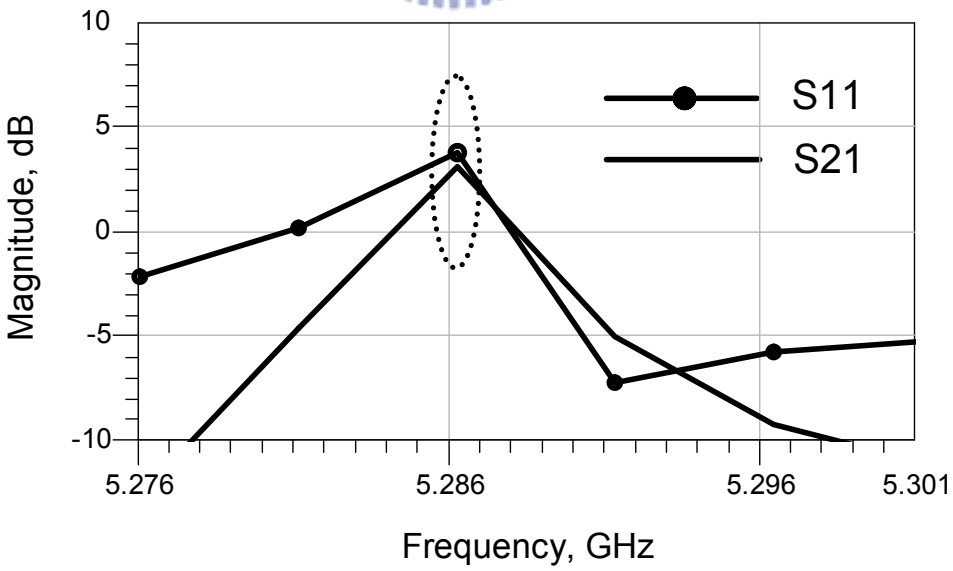


Fig. 4.10. Injection gain at the quadrature ports measured by VNA.

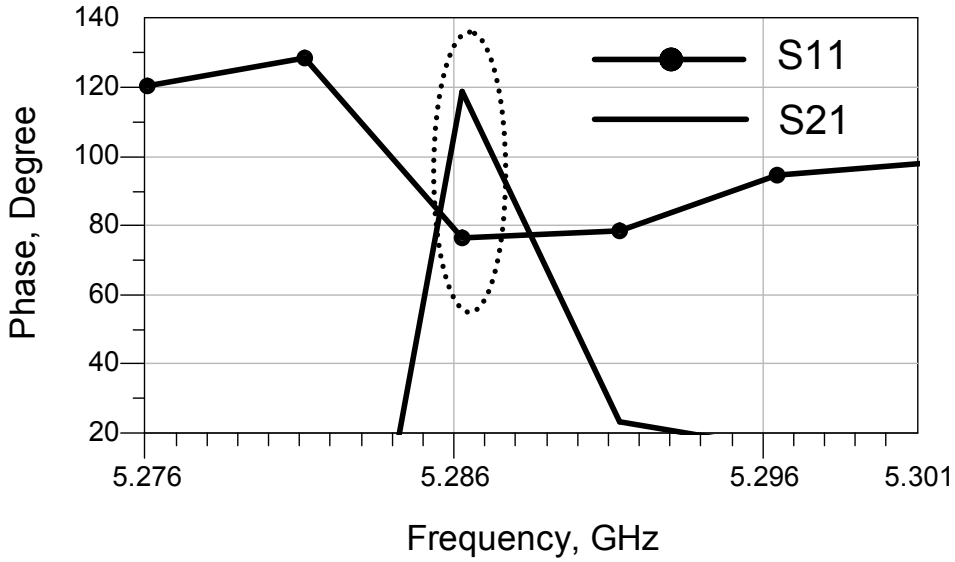


Fig. 4.11. Injection locked output phase at the quadrature ports.

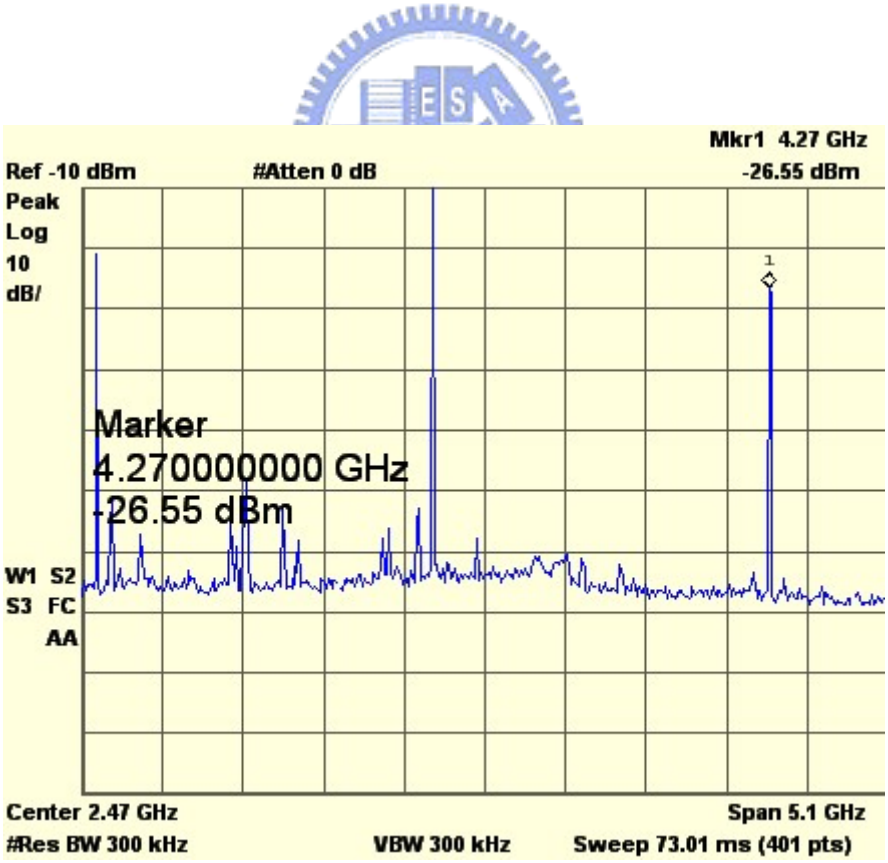


Fig. 4.12. The output spectrum of the frequency divider driven by the QVCO.

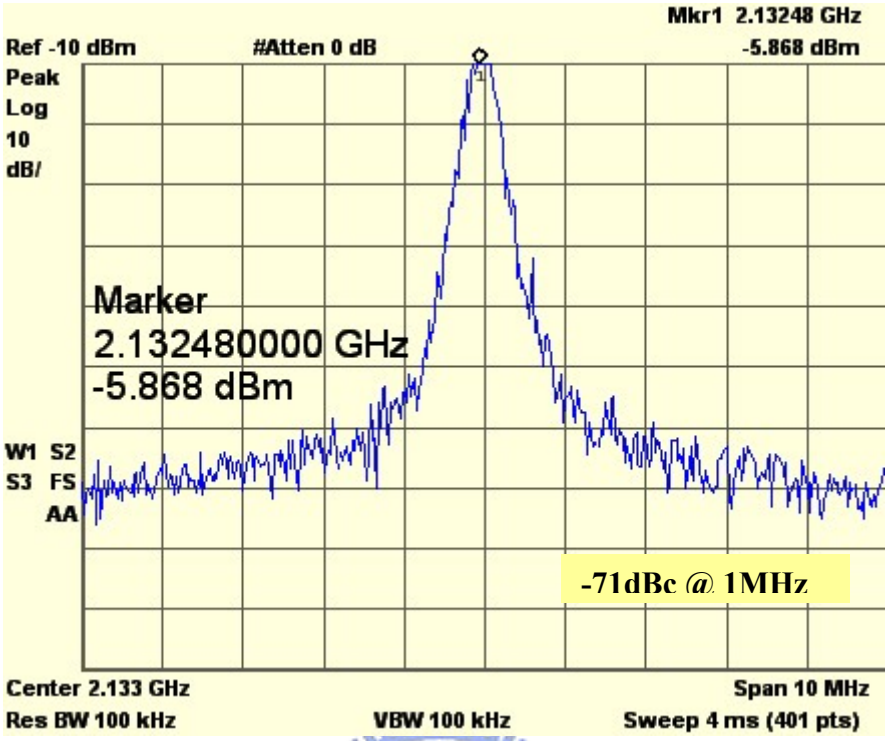


Fig. 4.13. Zoom-in view of the spectrum at the divider's output.

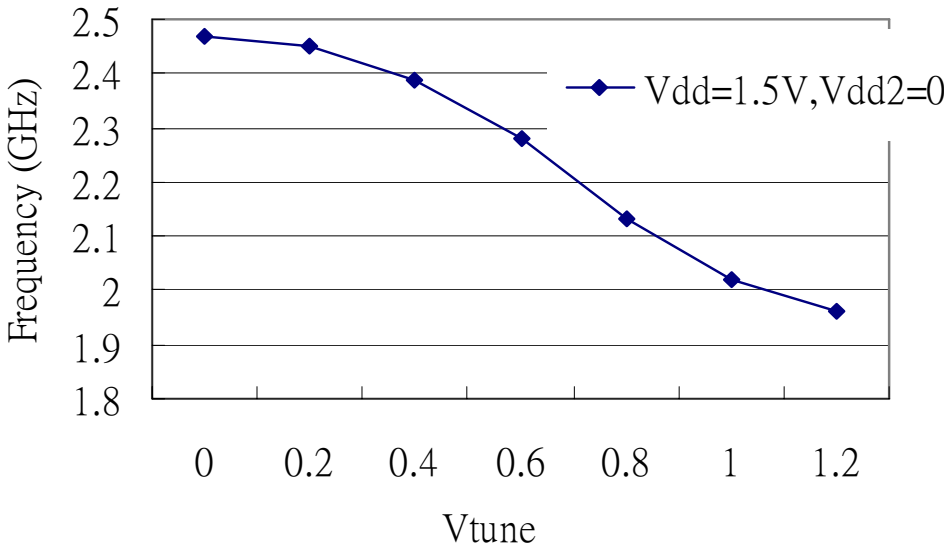


Fig. 4.14. Output frequency at divider output when the frequency of the QVCO is tuned.

Table. 4.2. Performance summary of the QVCO in the dual band signal-generation circuit.

	Simulated	Measured	[3.7]
Technology	0.18 um CMOS	0.18 um CMOS	0.35 um CMOS
Supply Voltage	1.5 V	1.8 V	2V
Current	8 mA	15 mA	25 mA
Frequency (GHz)	4.7 ~ 6	5.2~4.1	1.64~1.97
Tuning Voltage	0.4 ~ 1.8V	0.4~1.8V	N.A.
Phase Noise (dBc/Hz)	-119 @1MHz	-113@1MHz	-140 @3MHz
Quadrature Errror	N.A.	47°	0.25°

Table. 4.3. Performance summary of the frequency divider in the dual band signal-generation circuit.

	Simulated	Measured	[2.6]
Technology	0.18 um CMOS	0.18 um CMOS	0.1 um CMOS
Supply Voltage	1.0 V	1.2 V	1.2 V
Current	3.6 mA	4 mA	2.1 mA
Max. Input Frequency	5 GHz	5 GHz	5 GHz
Output Frequency	0~5 GHz	1.96~2.5 GHz	0~5 GHz
Phase Noise (dBc/Hz)	N.A.	-121[(1)]@1MHz	N.A.

[(1)] Driven by the QVCO with its phase noise = -113 dBc/Hz @1MHz.

4.1.3 Discussions

Some concerns may exist at the interface between the QVCO and frequency divider, since only two of the QVCO output are connected to frequency divider. Therefore, dummy transistors are required for the other two outputs of the QVCO.

As our experience, the frequency divider may self-oscillate when the biasing voltage Vb is high enough to make the switching transistors turn on. Therefore, the biasing condition at Vb will be critical.

The measurement result of phase relies on the calibration of the VNA, and we show our calibration strategy in Appendix B. Also, the frequency range in our measurement should be confined to the locking range for smooth read-out.

4.2 24-GHz Fully Differential Push-Push VCO

For the demand of millimeter-wave systems, push-push oscillator design has been proven to be an efficient way to extend the usable frequency range of the active devices for oscillator applications. However, the disadvantage of conventional push-push oscillators is that they only provide single-ended output. So, the push-push oscillator needs be followed by the baluns to generate differential signal. Compared to conventional design, we show a high frequency push-push VCO with differential output and less power consumption.

4.2.1 Push-Push Principle

Two oscillation signals are needed for push-push design as shown in Fig. 4.15

[4.5]. Assuming the two signals with harmonic terms and time shifting (Δt) are represented as

$$S_1(t) = a_1 e^{j\omega_0 t} + a_2 e^{j2\omega_0 t} + a_3 e^{j3\omega_0 t} + \cdots \tag{4.1}$$

$$S_2(t) = a_1 e^{j\omega_0 (t-\Delta t)} + a_2 e^{j2\omega_0 (t-\Delta t)} + a_3 e^{j3\omega_0 (t-\Delta t)} + \cdots \tag{4.2}$$

Adding the two signals in an appropriate output network (e.g., coupler.) we get

$$\begin{aligned} S_{out}(t) = S_1 + S_2 = a_1 e^{j\omega_0 t} \cdot (1 + e^{-j\omega_0 \Delta t}) + a_2 e^{j\cdot 2\omega_0 t} \cdot (1 + e^{-j\cdot 2\omega_0 \Delta t}) + \\ a_3 e^{j\cdot 3\omega_0 t} \cdot (1 + e^{-j\cdot 3\omega_0 \Delta t}) + \cdots \end{aligned} \tag{4.3}$$

If the phase difference at fundamental frequency between the two signals are enforced into differential

$$\omega_0 \cdot \Delta t = \pi \tag{4.4}$$

The output signal via the output network becomes

$$S_{out}(t) = 2 \cdot a_2 e^{j\cdot 2\omega_0 t} + 2 \cdot a_4 e^{j\cdot 4\omega_0 t} + 2 \cdot a_6 e^{j\cdot 6\omega_0 t} + \cdots \tag{4.5}$$

where all odd harmonics cancel themselves, whereas even harmonics are added constructively and 2nd harmonic dominates the output. Fig. 4.16 shows the sketch of this signal addition.

If another two differential signals, S_3 and S_4, have quadrature phase at fundamental frequency with respect to S_1 and S_2 respectively.

$$S_3(t) = a_1 e^{j\omega_0 t + \frac{\pi}{2}} + a_2 e^{j2\left(\omega_0 t + \frac{\pi}{2}\right)} + a_3 e^{j3\left(\omega_0 t + \frac{\pi}{2}\right)} + \cdots \tag{4.6}$$

$$S_4(t) = a_1 e^{j\omega_0 t + \frac{\pi}{2} + \pi} + a_2 e^{j2\left(\omega_0 t + \frac{\pi}{2} + \pi\right)} + a_3 e^{j3\left(\omega_0 t + \frac{\pi}{2} + \pi\right)} + \cdots \tag{4.7}$$

Then adding (4.6) and (4.7) together, a differential phase 2nd harmonic signal (with respect to S_{out}) is derived by

$$S_{pp,180}(t) = S_3 + S_4 = 2a_2 e^{j2\omega_0 + \pi} + 2a_4 e^{j4\omega_0} + 2a_6 e^{j6\omega_0 + \pi} + \cdots \tag{4.8}$$

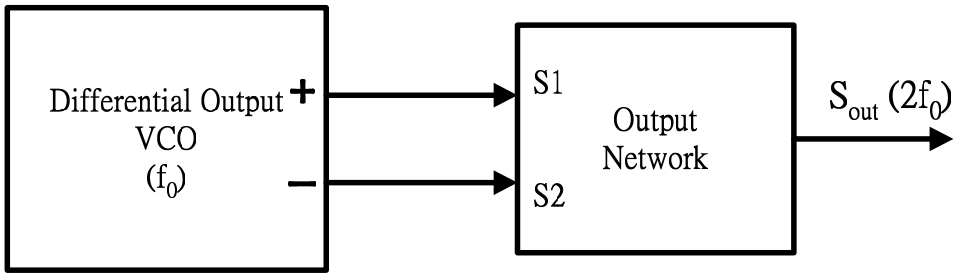


Fig. 4.15. Push-push VCO formed by a differential VCO and an output network.

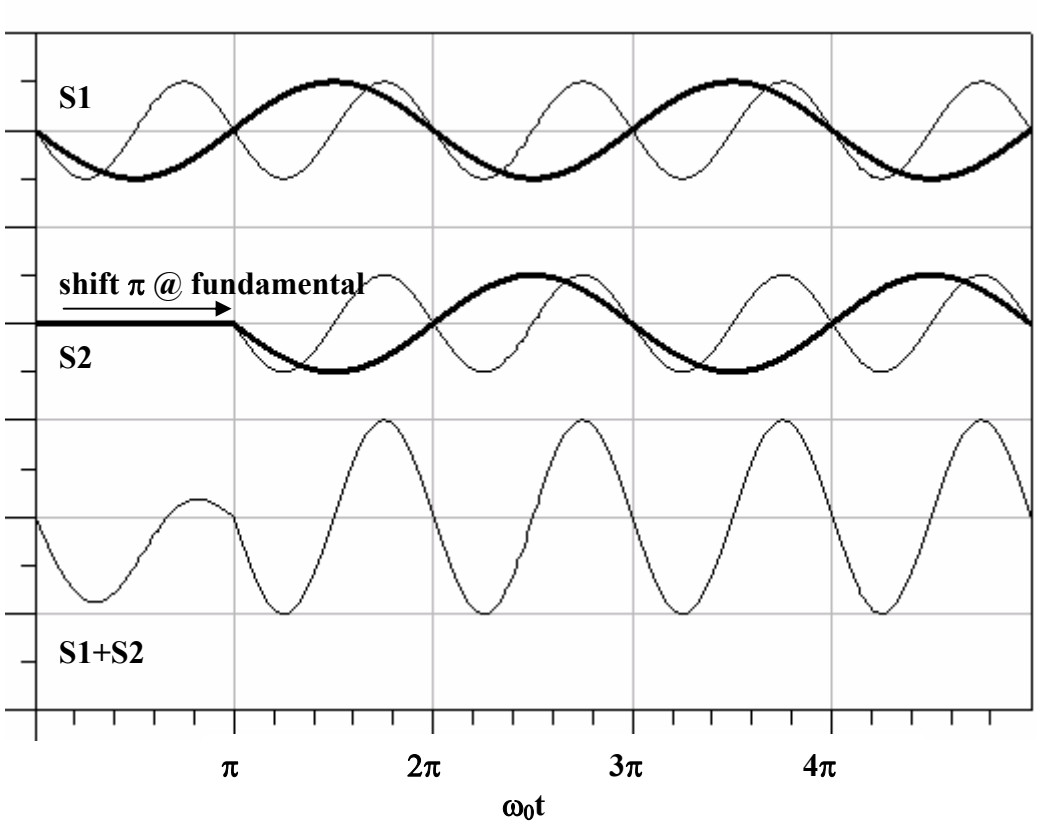


Fig. 4.16. Summation of two differential signals (S1 and S2) extracts the 2nd harmonic signal (S1+S2) [4.5].

4.2.2 Circuit Implementations

A full RFIC implementation is applied in this high frequency circuit. Fig. 4.17 shows the schematic of the 24 GHz fully differential push-push VCO. The core circuit is a 12 GHz QVCO consisting of two differential oscillators whose common mode

second order harmonics is coupled by the inductor pair L3-L4 [3.6]. The inductor pair L3-L4 is formed by a center tapped inductor with negative mutual inductance and small dimension, such that they resonate with the parasitic capacitance when driven differentially at the second order harmonic frequency in this oscillator.

The crossed coupled pairs Mn1-Mn4 and Mp1-Mp4 are used to generate negative resistance sustaining the oscillation. Low phase noise issue is treated by equal gm technique to obtain symmetric output waveform [3.9], so that the ratio of the transistor size Mn **:**Mp is set to be 1**:**2.

The four small size transistors Mp5-Mp8 (as the half size of Mp1-Mp4) are used for frequency tuning as demonstrated before. The frequency tuning is performed by varying Vdd2. We also use Mp1-Mp4 to perform quadrature coupling, but small coupling strength is provided by them.

The output network providing push-push operation path is realized by shorting the drains of the output buffer transistors Mn5-Mn6 and Mn7-Mn8 respectively. In this manner, a larger 2^{nd} harmonic is obtained while consumes small current, since the signal swing is large at the drain of output buffer transistors. To bias the output buffers, two external components Bias-Tee are needed.

Fig. 4.18 is the chip layout, where the PADs are layout for the on wafer measurement technique using pitch 150μm probes. For measurement probing, a G-S-G-S-G differential probe is needed, and a P-G-P-P-G-P 6 pins DC probe is needed. In the layout, bypass capacitors is added between the DC and GND PADs for power-supply noise eliminations.

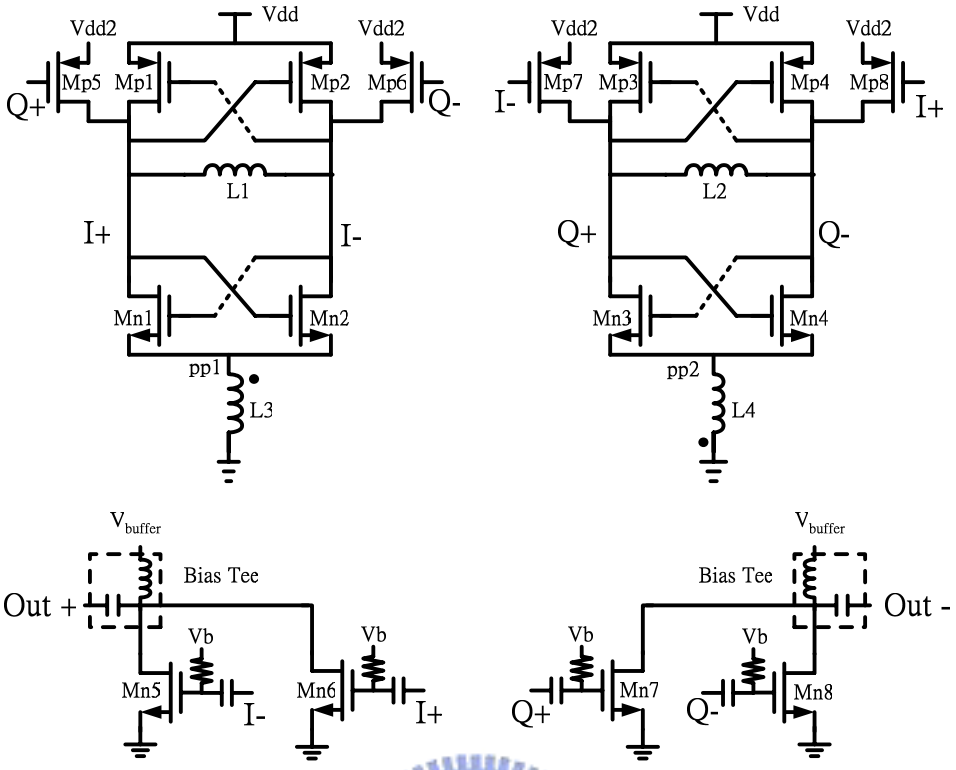


Fig. 4.17. The schematic of the fully differential push-push VCO.

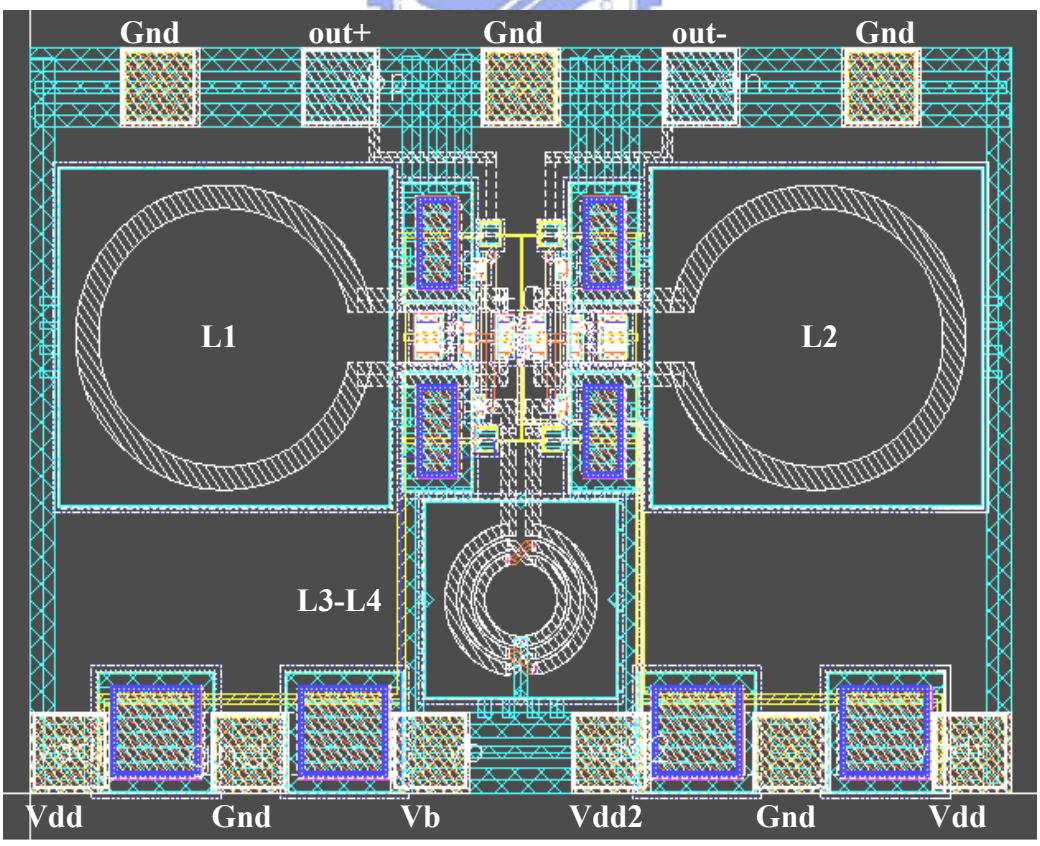


Fig. 4.18. Chip layout using UMC 0.18μm CMOS technology.

4.2.3 Simulation Results

We adopt the 0.18μm CMOS component model and process parameters provided by UMC to perform the following simulations.

First, we use the EM simulator - Ansoft Designer® to design the inductors used for LC tank oscillator and superharmonic coupling. For 12 GHz VCO design, the inductance in the LC tank we need is around 0.6 nH @12GHz, Fig. 4.19 shows the EM simulation result. For a high performance superharmonic coupling, it needs a center tapped inductor with strong mutual coupling coefficient and small inductance, Fig. 4.20 shows the simulation result of the center taped inductor we design, the inductance is around 0.44 nH each and the coupling coefficient is about 0.5 at 12GHz.

After completing the passive components design, we simulate the circuit with the long lead transmission line effect being taken into consideration. The push-push VCO draws 18mA when Vdd = 1.8V and Vdd2=1.8V. By transient analysis performed by Agilent ADS®, we obtain the output waveform of the push-push VCO, as shown in Fig.4.21. We translate the time domain waveform into frequency domain spectrum by fast fourier transformation, and we can see that the fundamental signal at the push-push port is suppressed to be 40dB lower than the 2nd harmonic, as indicated in Fig. 4.22. When Vdd2 is varied from 0.8-1.8V, the output frequency is tuned from 24 to 25GHz, as shown in Fig. 4.23. To obtain the phase noise at the push-push port, we first use Harmonic Balance analysis performed by Agilent ADS® to simulate the differential VCO and the result is -110 dBc/Hz @1MHz offset, as shown in Fig. 4.24. Since the frequency is doubled at the push-push port, so we assume the phase noise at the push-push port will be 6dB worse than the differential VCO. Table. 4.4 is the summary table of the push-push VCO.

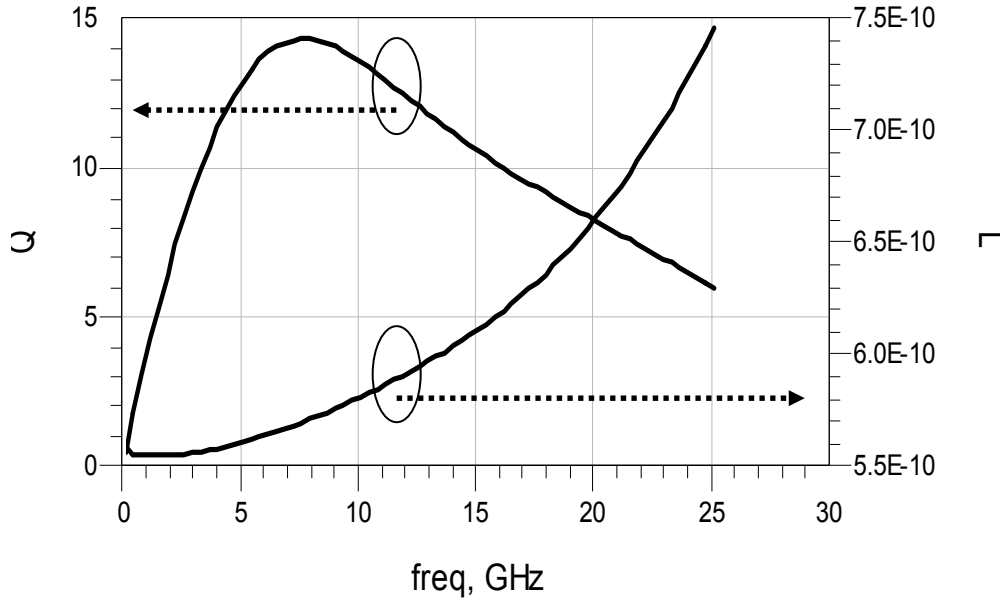


Fig. 4.19. Simulated result of Q and inductance value for 12 GHz LC tank.

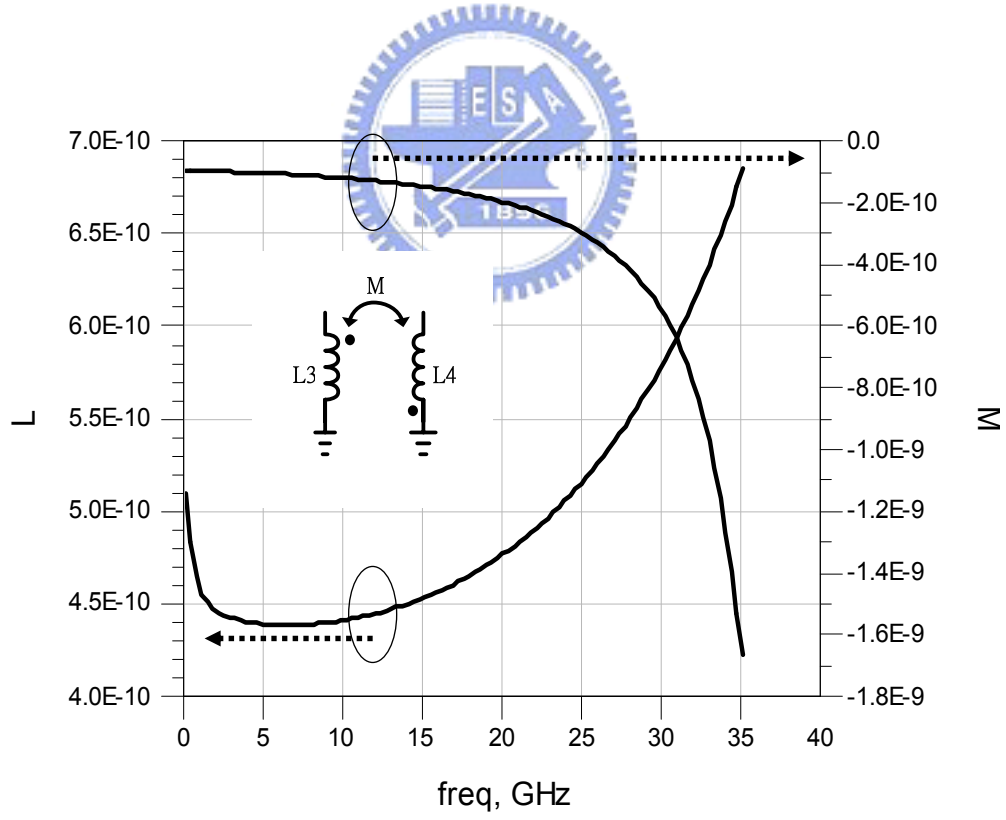


Fig. 4.20. Simulated result of inductance (L3/L4) and mutual inductance (M) of the center tapped inductor.

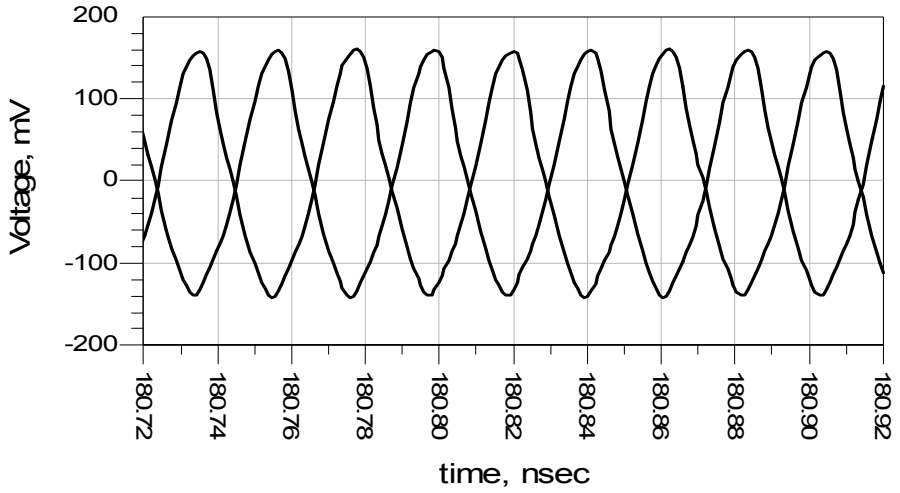


Fig. 4.21. Differential output waveform of the push-push VCO.

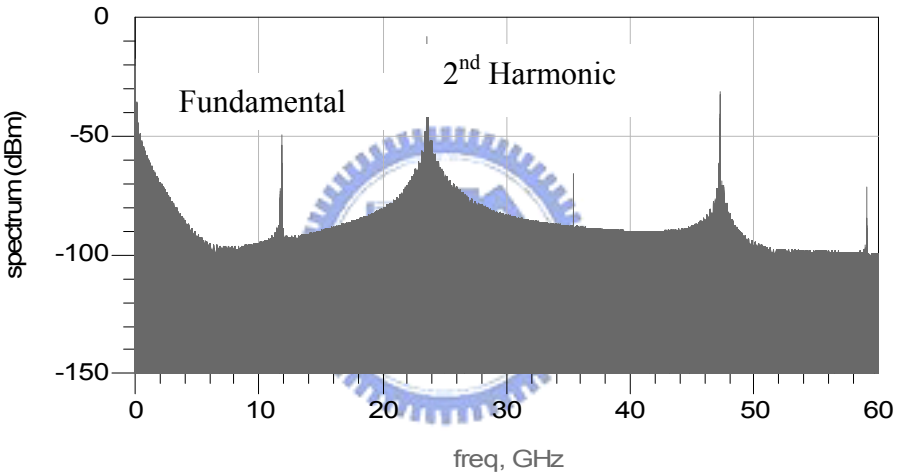


Fig. 4.22. The output spectrum at the push-push port.

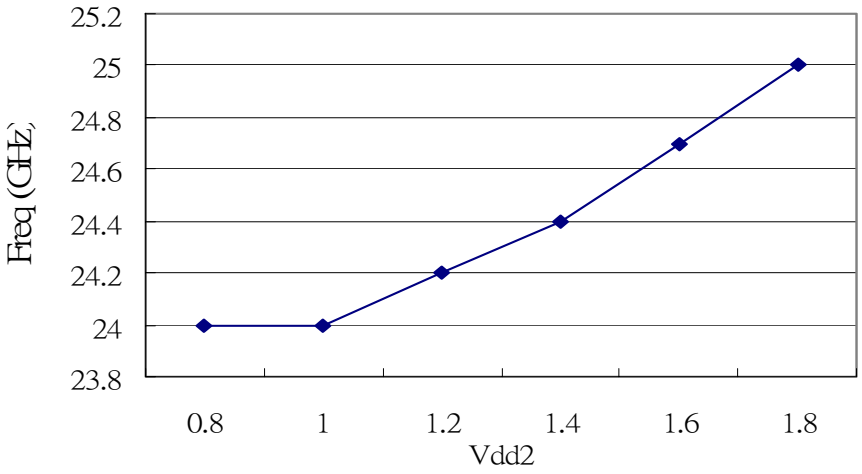


Fig. 4.23. Frequency tuning curve of the push-push VCO.

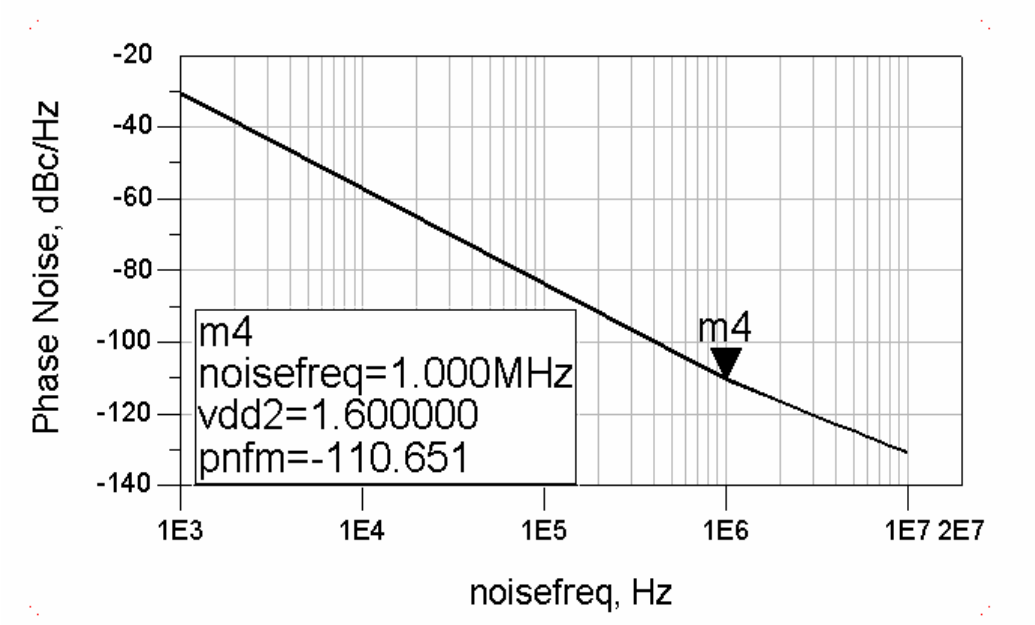


Fig. 4.24. Phase Noise of the individual differential VCO at 12.35-GHz.

Table. 4.4. Performance summary of the push-push VCO.

	This Work	[4.7]	[4.6]	[4.5]
Technology	0.18 um CMOS	0.35um CMOS	0.25 um CMOS	SiGe HBT
Supply Voltage	1.8 V	2.5 V	1.8 V	4.5 V
Current Consumption	18 mA	10.4 mA	66 mA	40 mA
Frequency Range(GHz)	24-25	4.9-5.2	62-66.5	57
Output Power	-10 dBm	-32dBm	-4dBm	+1dBm
Output Phase	Differential	Differential	Single	Single
Phase Noise (dBc/Hz)	-104 @1MHz	-104 @5MHz	-85 @1MHz	-108 @1MHz
FOM*	-175	-150	-160	-180

* FOM= $L\{\Delta f\}-20\log(\frac{f}{\Delta f})+10\log(\frac{P_{dissipation}}{1mW})$

CHAPTER 5

Conclusions and Future Work

5.1 Conclusions

In Chapter 2, the locking range of ILFD is improved by inductive shunt peaking technique and is wide enough for common wireless communication standard. As a lesson taught by the measurement result, full chip EM simulation is a good practice for precise prediction on circuit performance. We also show that the main idea of injection locking is the phase compensation mechanism introduced by the LC tank.

In Chapter 3, we show a frequency tuning mechanism by varying the transconductance of the coupling transistors, however, a large variation in biasing current is required. We also show that the poor I/Q phase error is raised from both the frequency imbalance and inductive coupling.

In Chapter 4, we try another method for quadrature phase measurement, however, we fails to measure the output phase of the digital frequency divider. On the other hand, a 24-GHz fully differential push-push VCO is implemented via a 12-GHz QVCO using the output buffers as the power combine network.

5.2 Future Work

For injection locking oscillators design, locking range may be further enhanced by replacing the current source transistor with an inductor, since the inductive shunt peaking and parasitic capacitance reduction are performed simultaneously. Besides,

high Q MEMS inductor is a good choice for inductive shunt peaking technique.

We have shown that the frequency can be tuned by varying the gm of the coupling transistors, however, the large variation in biasing current raises another problem. Therefore, gm boost technique may be a good try for alleviating this problem. Also, regulator may be needed for tuning of the bias voltage to vary the transconductance of the coupling transistors.

Push-push oscillator have a poor phase noise since the frequency doubled, for better phase noise performance, colpitts oscillator may be a good choice for push-push oscillator design. As shown in Appendix A, the varactor distorts the output waveform, it maybe manifest the push-push design too. Besides, since the output buffers in our push-push circuit need external components for biasing, it may be needed to find out another type of buffer for good integration.

Appendix A

MOS Varactors

In this appendix, we present the configurations for different types of MOS varactor and their tuning characteristics when large signal voltage swings is applied across the MOS varactors, as they are used in VCOs.

A.1 Configurations of MOS Varactor

Fig. A.1 shows the structure of a NMOS transistor, the gate capacitors is varied with different DC gate bias. The tuning curve of the gate capacitance of MOS versus dc gate bias voltage is obtained by superimposed a very small signal onto the dc bias voltage. As indicated by S-parameter simulation, gate capacitance is also dependent on the operation frequency.

Basically, a MOS transistor has five operation region, they are accumulation, depletion, weak inversion, moderate inversion and strong inversion [A.1], depending on the gate bias condition. Let's take NMOS for description.

The accumulation region is happened when $V_{Bulk}>V_{Gate}$, since the voltage at the interface between gate oxide and semiconductor is negative and low enough for holes to move freely, we have a MOS capacitor between Gate and Bulk and the capacitance value is equal to $C_{ox} = (\varepsilon_{ox}/t_{ox}) \cdot A$, where t_{ox} and A are the transistor oxide thickness and the channel area, respectively [A.1]. In strong inversion region, an inversion channel with mobile electrons is built on the surface of the P-substrate semiconductor

and this needs $V_{Gate}>V_{Bulk}+|Vt|$, where |Vt| is the threshold voltage of the transistor, so we have a MOS capacitor between Gate and Darin or between Gate and Source, and the capacitance value is also equal to $C_{ox} = (\varepsilon_{ox}/t_{ox}) \cdot A$. When V_{Gate} is much smaller than $V_{Bulk}+|Vt|$ but not negative enough for accumulation to happen, then we say that the transistor operates in depletion region and the MOS capacitor is formed between Gate and Bulk and it can be modeled as the C_{ox} in series with the depletion capacitance, which is inversely proportional to V_{GB}, so that we obtain a gate capacitance smaller than C_{ox}. With the V_{Gate} approaching to $V_{Bulk}+|Vt|$, the n-channel is going to be built up but not strong, so the MOS capacitor is formed between Gate and Drain or between Gate and Source, and the capacitance value is proportional to V_{GB} but it is smaller than C_{ox}.

Following the above descriptions, we are going to show the C-V curve for the MOS capacitance in different configurations. First, if we connect the source, drain, and bulk together to form one node of the capacitor, and the polysilicon gate forms the other node, we have a non-monotonic C-V curve, since the device can operate in these five region, Fig. A.2 (a) shows this connection and its C-V tuning curve is shown by the curve (a) in Fig. A.2 (d). Next, we connect the bulk to the lowest potential, so that, the device can't operate in the accumulation region, the curve (b) in Fig. A.2 (d) shows a monotonic but sharp C-V curve. Finally, we connect the Drain and source to the highest potential, so that, the device can't operate in inversion region, and then we obtain a smooth and monotonic C-V curve, as shown by the curve (c) in Fig. A.2 (d).

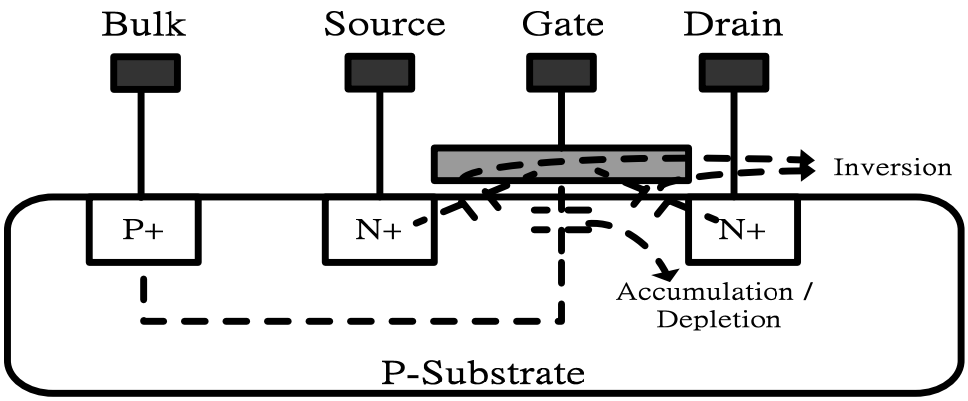


Fig. A.1. Cross section of a NMOS with the parasitic capacitor shown.

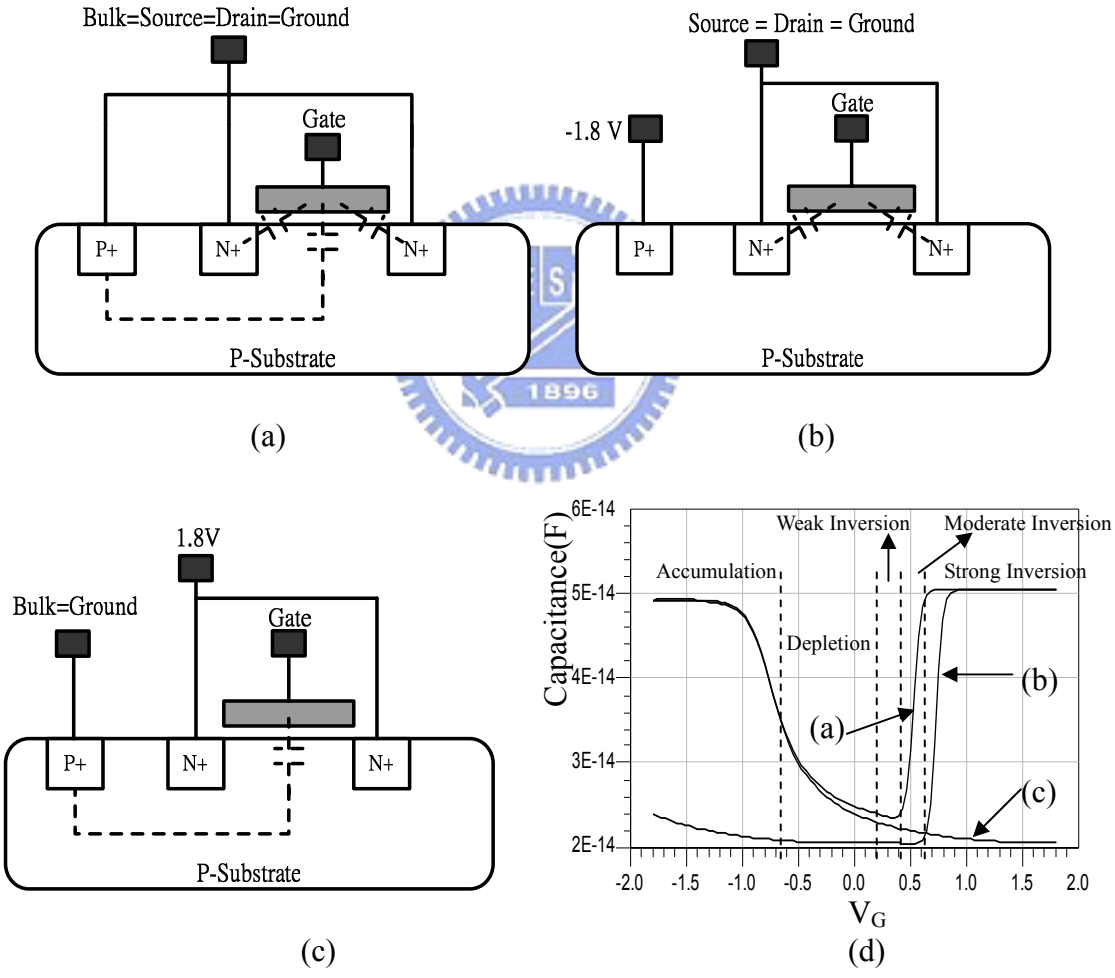


Fig. A.2 MOS varactor as a two node device in the configurations of (a) Bulk=Source = Drain, (b) Bulk connected to lowest potential (Inversion-mode), (c) Source and Drain are connected to highest potential (Accumulation-mode), and (d) C-V curves for each configuration.

A.2 MOS Varactors in Large Signal Operation

As shown in Fig. A.2 (d), the curve of the capacitance value versus bias voltage for MOS varactor is applied for small signal operation. Since the capacitance of the varactor is controlled by the voltage across the varactor, a large signal voltage swing across the varactors, e.g., applied in VCOs, will modulate the small signal capacitance of the varactors throughout the signal period. In VCOs, some counter-intuitions are raised by this modulation mechanism, such as the flatness of the small signal C-V curve [A.2], the output waveform distortion [A.3], and the flicker noise upconversion [A.3].

Let us first exam the large signal average capacitance. Assume a signal applied to the varactor is

$$v(t) = A\sin(\omega_0 t) + B \tag{A.1}$$

where A is voltage amplitude, B is the DC tuning voltage applied to the varactor. The current into the voltage-controlled capacitance is [A.2]

$$i(t) = C(v(t))\frac{dv(t)}{dt} \quad or \quad C(v(t)) = \frac{i(t)}{dv(t)/dt} \tag{A.2}$$

where C(v(t)) is the small signal C-V curve. Since v(t) is sinusoidal, we can express the time-average capacitance of C(v(t)) at some tuning voltage, B, by the root mean square value

$$C_{AVG} = \frac{rms(i(t))\big|_{\omega_0}}{rms(dv(t)/dt)} \tag{A.3}$$

where $rms(i(t))\big|_{\omega_0}$ means the rms value of the current at fundamental frequency. We find the magnitude of the current at fundamental frequency by the fourier series coefficient a_1, and divide a_1 by $\sqrt{2}$ to obtain the rms value as

$$rms(i(t)) = \frac{1}{\sqrt{2}} \cdot \frac{2}{2\pi/\omega_0} \int_0^{2\pi/\omega_0} i(t) \cdot \cos(\omega_0 t) dt \tag{A.4}$$

$$rms(d(v(t))/dt) = \frac{\omega_0 \cdot A}{\sqrt{2}} \tag{A.5}$$

Combining (A.1)-(A.5) yields

$$C_{AVG} = \frac{\omega_0}{\pi} \int_0^{2\pi/\omega_0} \left[C\left(A\sin(\omega_0 t) + B\right) \cdot \cos(\omega_0 t)\right] \cos(\omega_0 t) dt \tag{A.6}$$

Integration are taken to obtain the average capacitance for the expression C(v(t)) fitted to the C-V curve of the varactor. Fig. A.3 shows the simulated C_{AVG} of the varactor using large signal S-parameter analysis for different voltage swing amplitude A at some particular signal frequency [A.2].

Since the capacitance of varactor is varied due to the voltage swing, the output frequency changes inherently. The modulation of frequency by the varactor gives rise to a distorted output waveform of the VCO [A.3], and since the capacitance varied with the output swing, the charge conversation mechanism corresponds to an imbalance on the amplitude of the output swing, as shown in Fig. A.4.

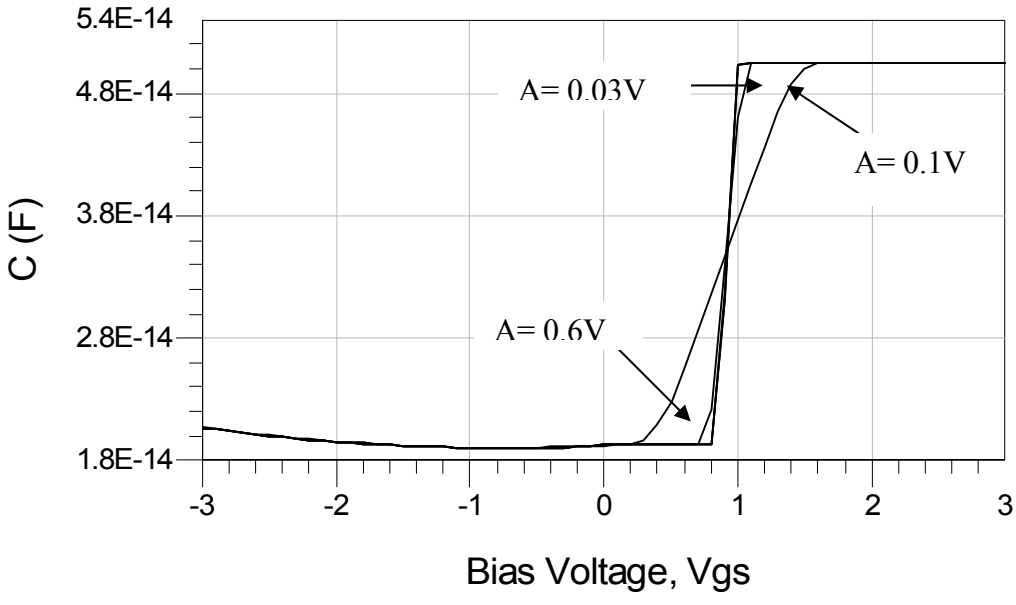


Fig. A.3. Voltage controlled capacitance for different swing amplitude A.

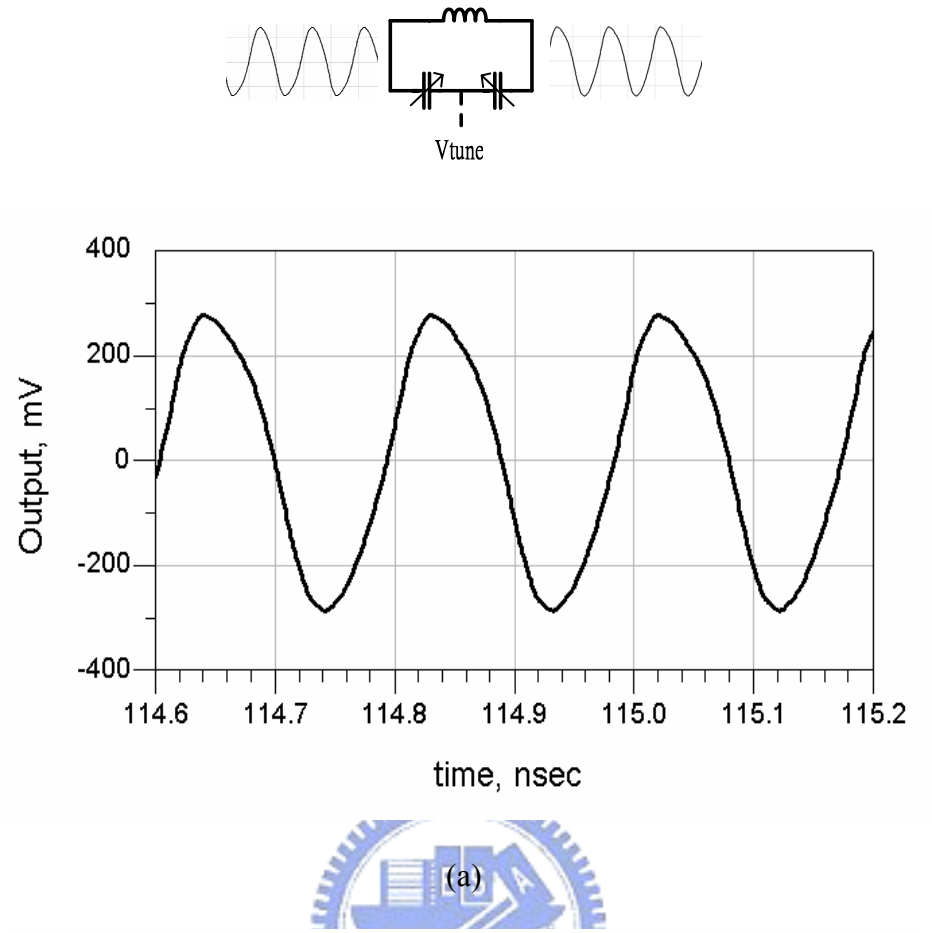


Fig. A.4. (a) Distorted output waveform due to the capacitance of the varactor varied with the output swing. (b) The output spectrum of this waveform.

Appendix B

Determination of Quadrature Accuracy

Since the quadrature phase accuracy is an important factor for high quality image rejection. So, we have to know whether the output phase is as precise as desired. This appendix is dedicated to the techniques for the measurement of quadrature phase accuracy.

B.1 Mixers for Sideband Rejection

It is known that mixers are used to shift the frequency of a signal from a lower or higher frequency to a higher or lower one. Taking the upcoversion mixer for example; a low frequency signal, say IF signal, and a single tone at high frequency, say LO signal, are multiplied together by the mixer to shift the IF frequency to a high frequency around the LO signal. After the multiplication, we obtain the RF signal

$$\begin{aligned} RF &= \cos(2\pi \cdot f_{LO} \cdot t) \cdot \cos(2\pi \cdot f_{IF} \cdot t) \\ &= \frac{1}{2}\cos\left(2\pi (f_{LO} - f_{IF}) \cdot t\right) + \frac{1}{2}\cos\left(2\pi (f_{LO} + f_{IF}) \cdot t\right) \end{aligned} \tag{B.1}$$

In (B.1), we can see that the RF signal has double sideband at a frequency offset f_{IF} with respect to the LO frequency on both sides of the LO signal, and let's call this kind of mixer as double sideband mixer.

Moreover, we can suppress one of the double sideband by using single sideband (SSB) mixer for frequency upconversion. The SSB mixer is composed of two double sideband mixers, and quadrature phase LO signals (LO_I and LO_Q) and quadrature

phase IF signals (IF_I and IF_Q) are needed for multiplication. One of the double sideband mixers multiplies LO_I with IF_I, and the other multiplies LO_Q with IF_Q, then the output of these two double sideband mixers are adding together to obtain the single sideband RF signal

$$\begin{aligned} RF &= LO_I \cdot IF_I + LO_Q \cdot IF_Q \\ &= \sin(2\pi \cdot f_{LO} \cdot t) \cdot \sin(2\pi \cdot f_{IF} \cdot t) + \cos(2\pi \cdot f_{LO} \cdot t) \cdot \cos(2\pi \cdot f_{IF} \cdot t) \\ &= \cos\left(2\pi (f_{LO} - f_{IF}) \cdot t\right) \end{aligned} \quad \text{(B.2)}$$

In (B.2), we obtain the lower sideband of the RF signal, and the upper sideband is suppressed. Or, the upper sideband can be obtained and the lower sideband be suppressed by reversing the phase ($\pm 180°$) of either the LO or IF quadrature signal [B.1]. Fig. B.1. shows the SSB mixer with each of the double sideband mixers being composed of four FET-switches in double-balanced configuration.

With an imperfect quadrature signal, such as amplitude mismatch or phase mismatch, being input to the SSB mixer, the effect of sideband rejection will be degraded. We are going to estimate the quadrature phase accuracy of the input signal to the SSB mixer by measuring how much sideband rejection is achieved. We use arbitrary waveform generator (AWG) to produce a perfect quadrature IF signal, and assume the quadrature LO signal has a phase mismatch $\Delta\theta$ and amplitude mismatch ΔA, then according to (B.2) we get

$$\begin{aligned} RF &= LO_I \cdot IF_I + LO_Q \cdot IF_Q \\ &= \sin(2\pi \cdot f_{LO} \cdot t) \cdot \sin(2\pi \cdot f_{IF} \cdot t) \\ &\quad + (1 + \Delta A) \cos(2\pi \cdot f_{LO} \cdot t + \Delta\theta) \cdot \cos(2\pi \cdot f_{IF} \cdot t) \end{aligned} \quad \text{(B.3)}$$

We replace each sine and cosine function by the exponential representation [B.2]

$$
\begin{aligned}
RF &= -\frac{1}{4}\left(e^{j\omega_{LO}t} - e^{-j\omega_{LO}t}\right)\cdot\left(e^{j\omega_{IF}t} - e^{-j\omega_{IF}t}\right) \\
&\quad + \frac{1}{4}(1+\Delta A)\cdot\left(e^{j\omega_{LO}t}e^{j\Delta\theta} + e^{-j\omega_{LO}t}e^{-j\Delta\theta}\right)\cdot\left(e^{j\omega_{IF}t} + e^{-j\omega_{IF}t}\right) \\
&= \frac{(1+\Delta A)e^{j\Delta\theta}-1}{4}\cdot e^{j(\omega_{LO}+\omega_{IF})t} + \frac{(1+\Delta A)e^{-j\Delta\theta}-1}{4}\cdot e^{-j(\omega_{LO}+\omega_{IF})t} \\
&\quad + \frac{(1+\Delta A)e^{j\Delta\theta}+1}{4}\cdot e^{j(\omega_{LO}-\omega_{IF})t} + \frac{(1+\Delta A)e^{-j\Delta\theta}+1}{4}e^{-j(\omega_{LO}-\omega_{IF})t}
\end{aligned}
\tag{B.4}
$$

By (B.4), we calculate the ratio of the unsuppressed sideband power at the positive frequency (i.e., $e^{j(\omega_{LO}-\omega_{IF})t}$) to the suppressed sideband power at positive frequency (i.e., $e^{j(\omega_{LO}+\omega_{IF})t}$), and define the ratio as the image rejection ratio (IRR)

$$
\begin{aligned}
IRR &= 10\log\frac{\left|(1+\Delta A)e^{j\Delta\theta}+1\right|^2}{\left|(1+\Delta A)e^{j\Delta\theta}-1\right|^2} = 10\log\left[\frac{\left|(1+\Delta A)\cos\Delta\theta+1+j\sin\Delta\theta\right|^2}{\left|(1+\Delta A)\cos\Delta\theta-1+j\sin\Delta\theta\right|^2}\right] \\
&= 10\log\left[\frac{\left((1+\Delta A)\cos\Delta\theta+1\right)^2+(1+\Delta A)^2\sin^2\Delta\theta}{\left((1+\Delta A)\cos\Delta\theta-1\right)^2+(1+\Delta A)^2\sin^2\Delta\theta}\right] \\
&= 10\log\left[\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos\Delta\theta}{1+(1+\Delta A)^2-2(1+\Delta A)\cos\Delta\theta}\right]
\end{aligned}
\tag{B.5}
$$

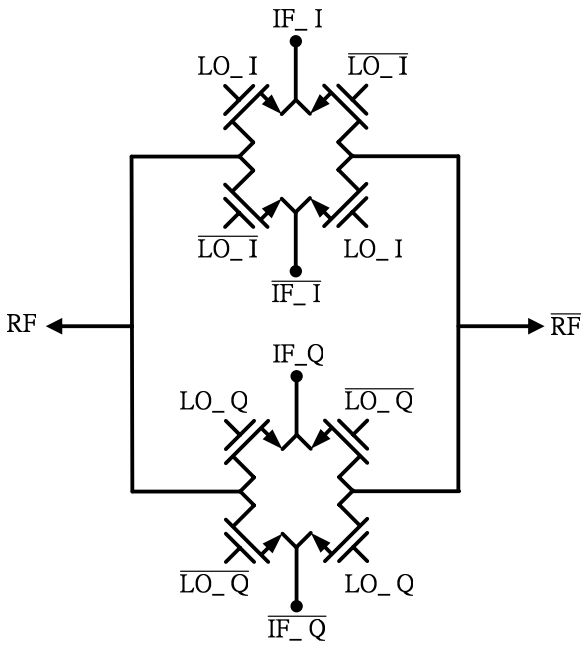


Fig. B.1. Passive single sideband mixer composed by FET-switches.

B.2 Injection Locking with Vector Network Analyzer

Basically, vector network analyzer (VNA) is a vector receiver, it stimulates the electronic networks and components at different measurement frequency by a swept or continuous wave (CW) signal and receives the reflected and transmitted signal from these circuits to obtain their magnitude and phase response.

Fig. B.2 shows the block diagram of vector network analyzer [B.3], the synthesized RF source stimulates either port 1 or port 2 (i.e., forward or reversely) of the device under test (DUT) at different measurement frequency, at the meanwhile, the other port is switched to the 50Ω load. Portion of the incident signal and the response from the DUT is directed by the signal separation components (or directional couplers) to their corresponding downconversion mixer, and these signals are downconverted to a fixed frequency for application to the synchronous detector and data processing to display the measurement result [B.4]. Since the frequency after downconversion is fixed, LO source needs be phase-locked to the RF source.

After the processing of synchronous detector, the VNA catch the response of magnitude and phase of the reflected and transmitted signal with respect to the incident signal, e.g., b_1/a_1 and b_2/a_1 for the forward path. Furthermore, calibration needs be conducted to retrieve the imperfection in the VNA system to obtain the corrected S11 and S21 from mathematical calculation performed by VNA. So, before we measure the DUT, we use VNA to measure the standard calibration kits, most often the short-open-load-through calibration kits, to obtain the system error term in both the magnitude and phase. Since we are going to apply VNA for quadrature phase measurement, the techniques for aligning the electrical reference plane during calibration will be very helpful, as indicated by Fig. B.3. More accurate reference plane alignment technique called adaptor removal is suggested by [B.4], however,

more complicated.

Since we have known that the oscillator can be locked by external injection signal, we use the testing signal from the VNA as the injection signal and inject it into one of the output ports of the oscillator, as shown in Fig. B.4. Once the oscillator is injection locked by the testing signal provided by the VNA, we can obtain injection gain, i.e., S11 and S21 > 1. Since all the other output port of the oscillator is locked consequently, we obtain constant phase difference between injection signal and oscillator output ports when injection-lock happens. We denote that the output phase at two of the quadrature output ports of the oscillator and at the RF source are θ1, θ2, and θ3 respectively. So we can obtain [B.5]

$$\theta 2-\theta 1 = (\theta 2-\theta 3)-(\theta 1-\theta 3) = \text{phase(S21)-phase(S11)} \quad \text{(B.6)}$$

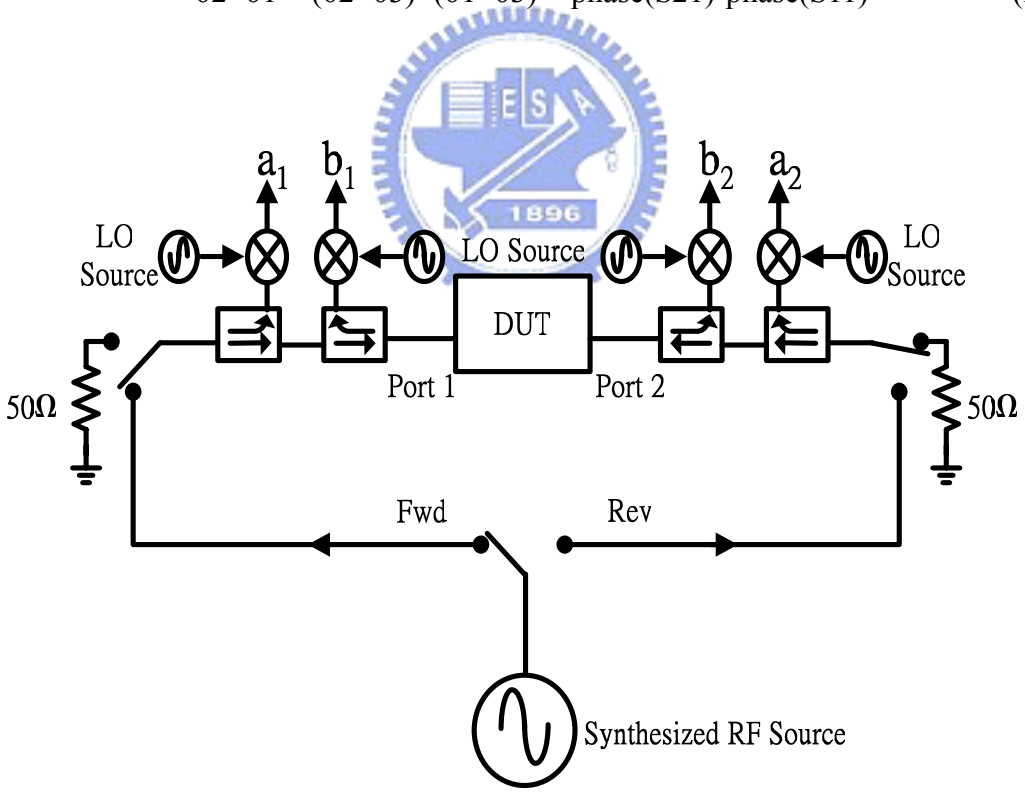


Fig. B.2. Block diagram of the vector network analyzer [B.3].

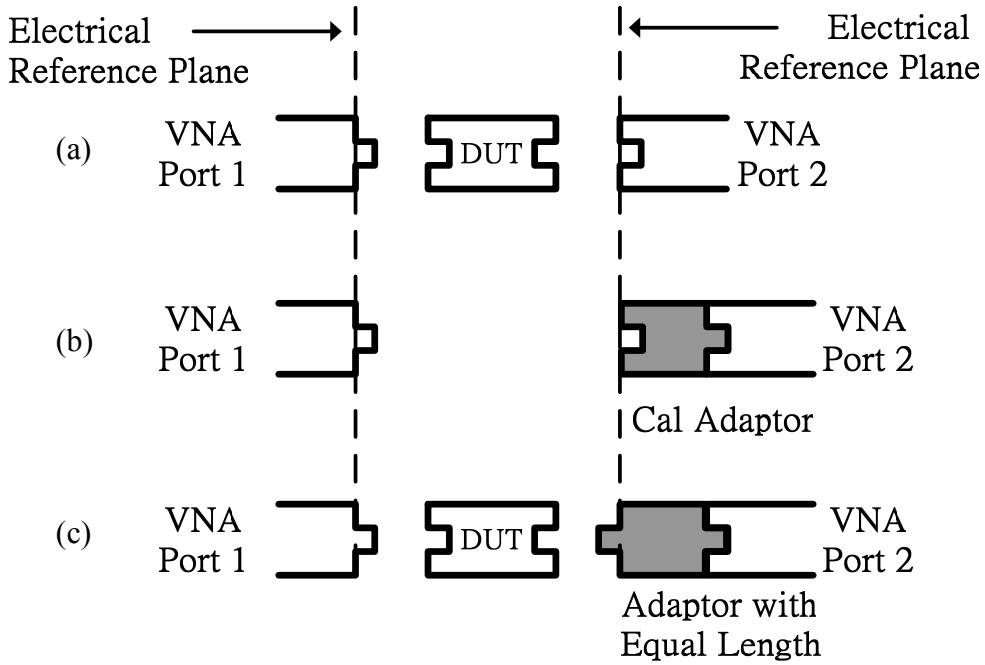


Fig. B.3. (a) A connector unmatched DUT, (b) Cal adaptor is inserted for aligning the open-short-thru-load calibration reference plane, (c) Replace the Cal-adaptor with an equal length adaptor for matched connection to DUT.

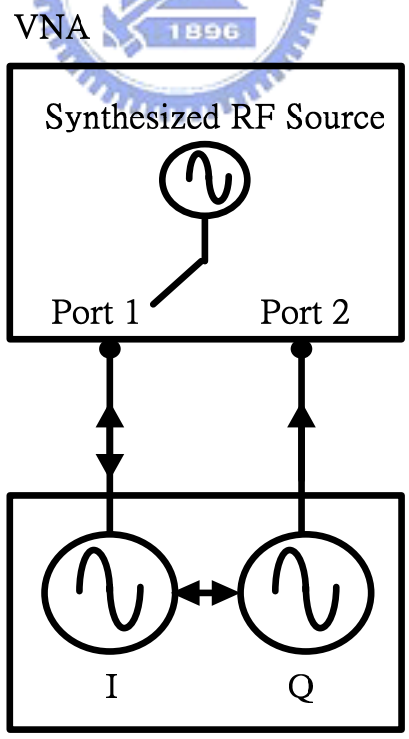


Fig. B.4. Experimental setup for phase measurement.

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