CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Wireless technology is developed to use in more and more different electronic consumer goods, for example like wireless keyboards, mouses and toys. Otherwise there are more and more wire electronic products need to add the wireless function. So, the wireless communication in today's world becomes more and more important.

In the modern communication field, phase-locked loop based frequency synthesizers have played an important role in RF front-ends. Most of the communication ICs for example used in cellular phones, WLAN and etc. are battery-powered systems, so this demands that more and more circuits able to operate in low supply voltage and low power consumption. However, while digital circuits can work without too many problems in such supply conditions, new analog circuit architecture must be developed to keep similar performance with respect to the operation at higher voltages.

There is another reason for designing a low voltage synthesizer. As the technology goes forward, the break down voltage of the MOS is lower. It means that the supply voltage must be scaled down with the process improve. For example the supply voltage of 0.18-um CMOS process is less than 1.8-V. In the future world the low voltage design in CMOS IC design can not be avoided.

1.2 REVIEWS OF CMOS FREQUENCY SYNTHESIZERS

1.2.1 2.4 GHz Frequency Synthesizer with Charge Pump

In the RF wireless systems, the frequency synthesizer plays an important role. The most popular method to realize the frequency synthesizer is the charge-pump PLL. The advantage of the charge-pump PLL is the large acquisition range, and the disadvantage of the charge-pump PLL is the mismatch current of the charge pump. This mismatch current increases the spur level.

The most popular solution of this problem is to use the current-match charge pump. Table 1.1 shows three designs of 2.4 GHz frequency synthesizer. The first one does not use the current-match charge pump. The second and third both use the current-match charge pump. From this table, we can find that the spur level can be strongly reduced by using the current-match charge pump.

We can also find that the spur level is also relating to the K_{VCO} and this can be demonstrated by the linear model of VCO.

Table 1.1 Reviews of 2.4 GHz frequency synthesizers

	[4]	[5]	[6]
Current-match CP	no	yes	yes
K_{VCO} (VCO Gain)	No mention	120 MHz/V	345 MHz/V
Spur level	-29 dBc @1MHz offset	-70.88 dBc @1MHz offset	-65.53 dBc @1MHz offset

Although the current-match charge pump can obviously reduce the spur level, it may suffer from the start-up problem when VDD like a ramp function.

1.2.2 1 V Frequency Synthesizer

Using the voltage doubler to boost up the supply voltage of prascaler is a method to make the prescaler work well in low voltage (1 V) [7].

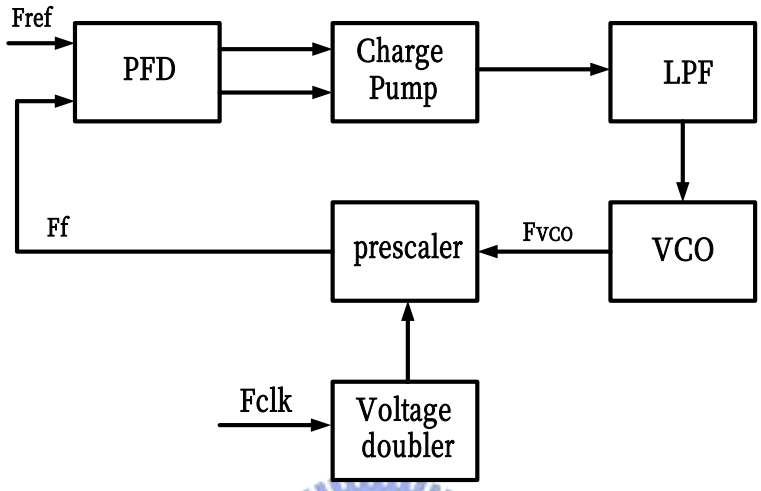


Fig 1-1 1V frequency synthesizer with voltage doubler [7]

As shown in Fig 1-2, this method may suffer from additional spurious tones at the offset frequency Fclk.

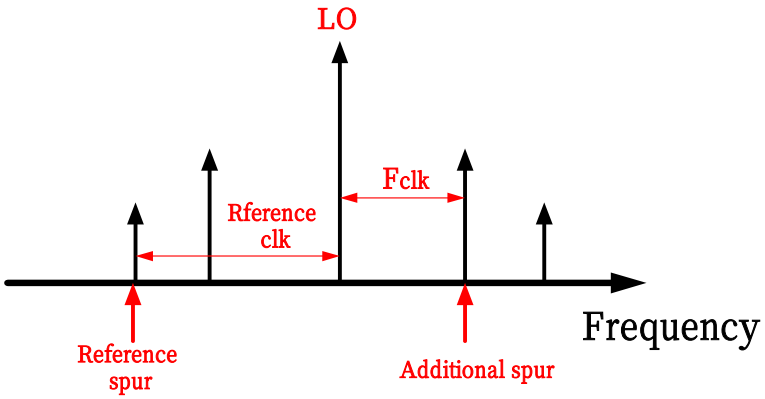


Fig 1-2 Additional spur appear when using voltage doubler.

1.3 MOTIVATION

The low voltage (1 V) and low power 2.4 GHz frequency synthesizer is desired. The low spur level is also necessary in the 2.4 GHz frequency synthesizer. In order to reduce the spur level the current-match charge pump is necessary. So, to solve the start-up problem of the current-match charge pump is also necessary in this work.

1.4 ORGANIZATION OF THIS THESIS

In order to achieve low voltage, low spur and to solve the start-up problem, a new current-match charge pump is used. In this charge pump, a bulk-driven input rail-to-rail op-amp is used in the feedback loop to work at 1 V supply voltage. In section 1.2, it is mentioned that decreasing VCO Gain (K_{VCO}) can decrease the spur level. A band-switching VCO is used to reduce the VCO Gain.

Chapter 2 is the basic theory of the PLL and frequency synthesizer and there are also some reviews of current-match charge pump. Chapter 3 shows the circuit realizations and the simulation results of this design. Chapter 4 shows the measurement results of this design. Chapter 5 talks about the conclusions and the future works.

CHAPTER 2

BASIC THEORY

2.1 TYPE I PLL

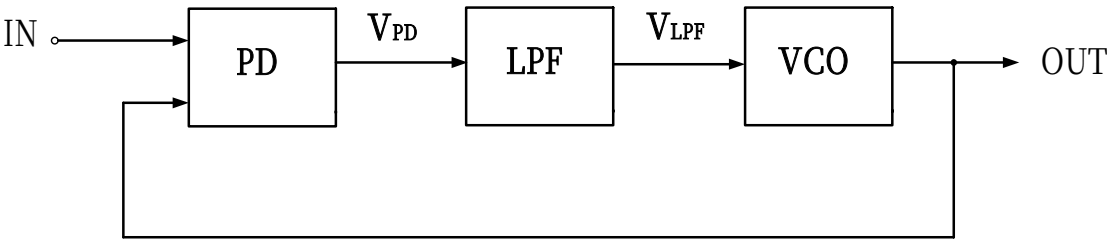


Fig 2-1 PLL block diagram .

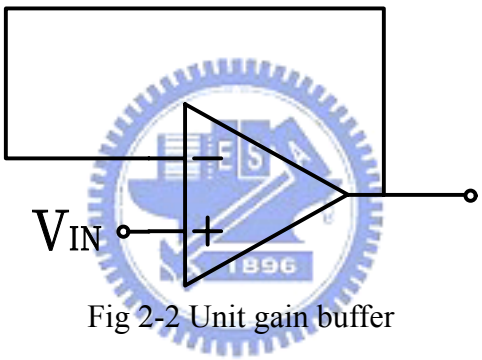


Fig 2-2 Unit gain buffer

Fig 2.1 shows the basic PLL block diagram. It contains three components, PD, LPF and VCO. The PD is a comparator which can detect the phase difference between two inputs. Usually, a XOR gate is a simplest PD (phase detector) used in PLL. The LPF (low pass filter) is used to storage the voltage which control the VCO. VCO (voltage control oscillator) is used to be an oscillator which can change frequency by different V_{LPF}.

This close loop of PLL can be seen as a unit gain buffer like Fig 2.2. The unit gain buffer has the function which can force the output voltage follow the input voltage and the different value between input and output is function of gain.

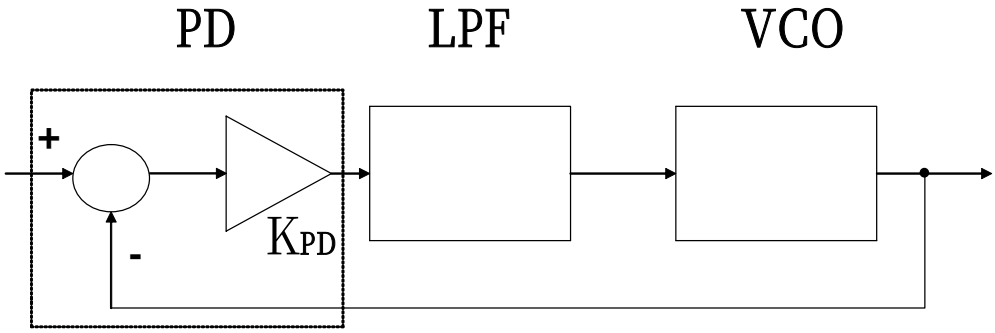


Fig 2-3 The linear model of type I PLL

The PLL loop compare the input phase and output the high or low to charge or discharge the LPF. If the phase of VCO is less than IN, the PD will increase V_{LPF} and the output frequency of VCO will increase to catch the phase of IN. After the phase is equal the PD out will stable. At this time the output phase of VCO will has a constant error with input phase. This phase error can not be a function of time, and it is defines as phase locked. When the input phase is changing, the output phase of VCO will follow it.

Fig 2.3 shows the linear model of type I PLL; assume a first-order low-pass filter for simplicity. The PD output contains a DC component equal to $K_{PD}(\phi_{out} - \phi_{in})$ and high-frequency components. Since the later is suppressed by the LPF, the PD can be simply modeled by a subtractor whose output is amplified by K_{PD}. the LPF transfer function is $1/(1+s/W_{LPF})$, where W_{LPF} denotes the -3dB bandwith, and the VCO transform function is $1/(1+s/W_{LPF})$.

The open-loop transform function is given by

$$H(s)_{open} = \frac{\phi_{out}}{\phi_{in}}(s)_{open} = K_{PD} \bullet \frac{1}{1+\frac{s}{W_{LPF}}} \bullet \frac{K_{VCO}}{s} \quad (1)$$

from (1), the close loop transform function can be written as

$$H(s)_{close} = \frac{K_{PD}K_{VCO}}{\frac{S^2}{W_{LPF}} + s + K_{PD}K_{VCO}} \tag{2}$$

This equation can be rewritten in a familiar form used in control theory.

$$H(s) = \frac{W_n{}^2}{S^2 + 2\varsigma W_n S + W_n{}^2} \tag{3}$$

where

$$Wn = \sqrt{W_{LPF}K_{PD}K_{VCO}} \tag{4}$$

$$\varsigma = \frac{1}{2}\sqrt{\frac{W_{LPF}}{K_{PD}K_{VCO}}} \tag{5}$$

The second-order transfer function of (3) suggests that the step response of the type I PLL system can be overdamped, critically damped, or underdamped.

The type I PLL has a trade-off between the settling speed and the ripple on the VCO control voltage. The lower W_{LPF}, the grater suppression of the high-frequency component produced by PD but the lower W_{LPF} cause the longer settling time constant [1].

2.2 CHARGE-PUMP PLL

2.2.1 Issue of Type I PLL

The type I PLL has been widely used. In addition to the trade-offs between ς, W_{LPF}, type I PLLs suffer from another critical drawback: limited acquisition range.

Suppose when a PLL is tuned on and the loop is not locked. The loop only locks if

the difference between W_{in} and W_{out} is less than roughly W_{LPF} [1]. The problem of lock acquisition further tightens the trade-offs in type I PLLs.

In order to remedy the acquisition problem, modern PLLs incorporate frequency detection in addition to phase detection.

2.2.2 Phase Frequency Detector

Phase frequency detector can detect both phase and frequency difference between the reference signal and the output signal of the frequency divider. As shown in Fig. 2-4, if the frequency of A is greater than the frequency of B, then Q_A is high, but Q_B is still low. Conversely, if the frequency of B is greater than the frequency of B, then Q_B is high and Q_A is low. If the frequency of A and B are equal, then the circuit will check the phase difference between the two inputs, and generates a pulse equal to the phase difference at Q_A or Q_B (depends on which input has phase leading).

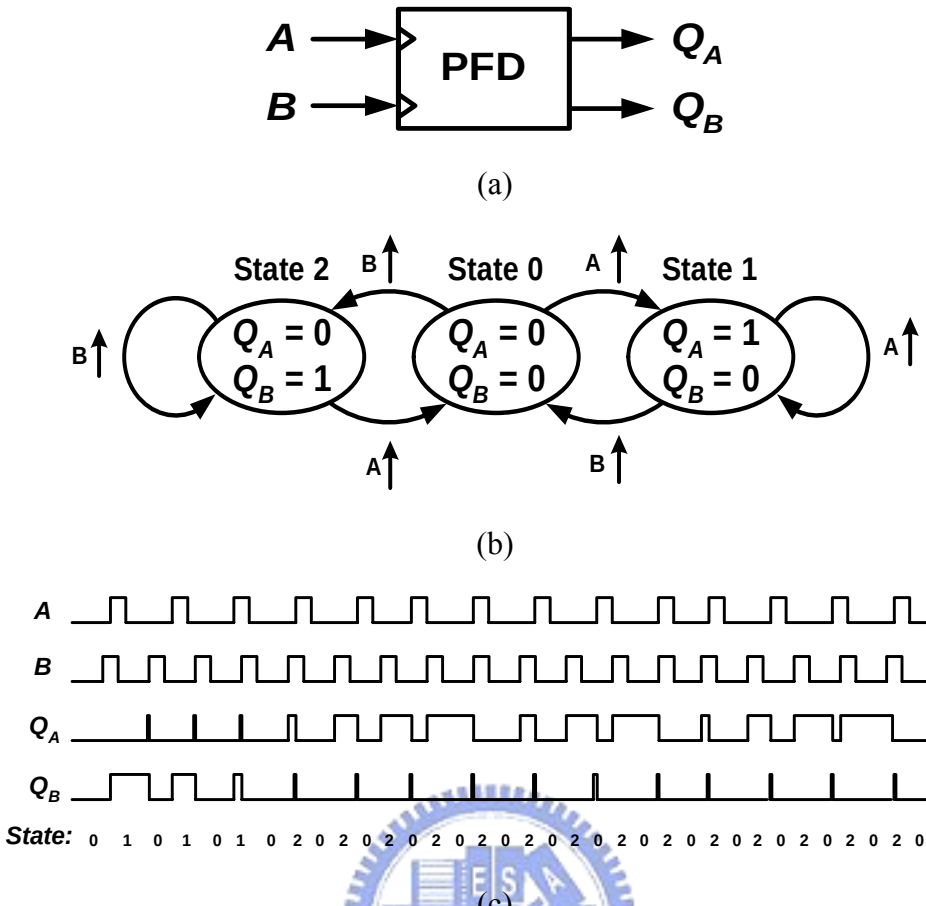
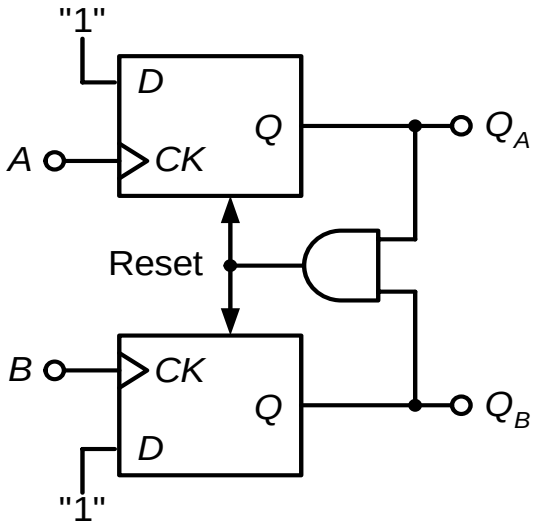


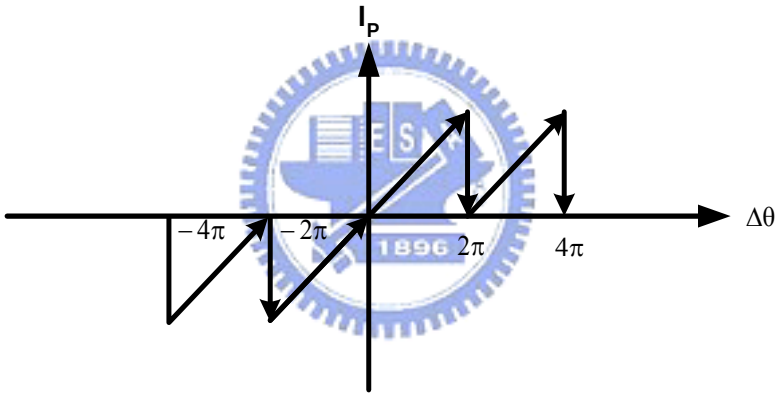
Fig 2-4 (a) PFD block diagram (b) PFD state diagram (c) PFD timing diagram

In Fig 2-5 (a), it shows a possible implementation of the above PFD. This circuit contains two resettable D-flip flops and a NAND gate. The input signals of A and B are as clock input and the input of two D-flip flops is always high. And we set the initial condition is Q_A=Q_B=0. If A is from 0 to 1, then Q_A=1, until B is from 0 to 1 and Q_B becomes high to make the two D-flip flops reset.

And Fig2-4 (b) shows the input-output characteristic of the PFD. Defining the output as the difference between the average values of Q_A and Q_B when W_A= W_B, it can be noted that the output varies symmetrically as $\Delta\theta$ begins from zero.



(a)



(b)

Fig 2-5 (a) PFD implementation (b) PFD characteristic

Since the difference between the average values of Q_A and Q_B is of interest, the two outputs can be low-pass filtered and used a op-amp to sense the difference. However, a more common approach is to interpose a charge pump (CP) between the PFD and loop filter.

2.2.3 Basic Charge-Pump PLL

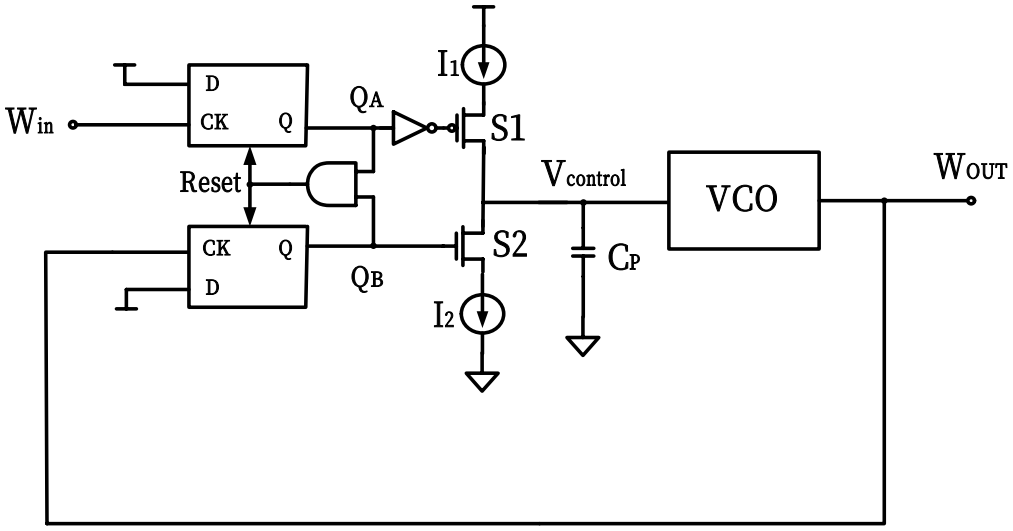


Fig 2-6 simple charge-pump PLL

Fig 2-6 shows the charge-pump PLL. A charge pump consists of two switched current source that pump charge into or out of the loop filter according to two logical inputs. The circuit has three states. If Q_A=Q_B=**0,** then S_1 and S_2 are off and V_{out} remain constant. If Q_A is high and Q_B is low, then I_1 charges C_p**.** Conversely, if Q_A is low and Q_B is high, then I_2 discharges C_p. I1 and I2 are nominally equal and called UP and DOWN currents.

When the loop is turned on, W_{out} may be far from W_{in}, and the PFD and the charge pump vary the control voltage such that W_{out} approaches W_{in}. When the input and output frequencies are sufficiently close, the PFD operate as a phase detector, performing phase lock. The loop locks when the phase difference drops to zero and the charge pump remain idle.

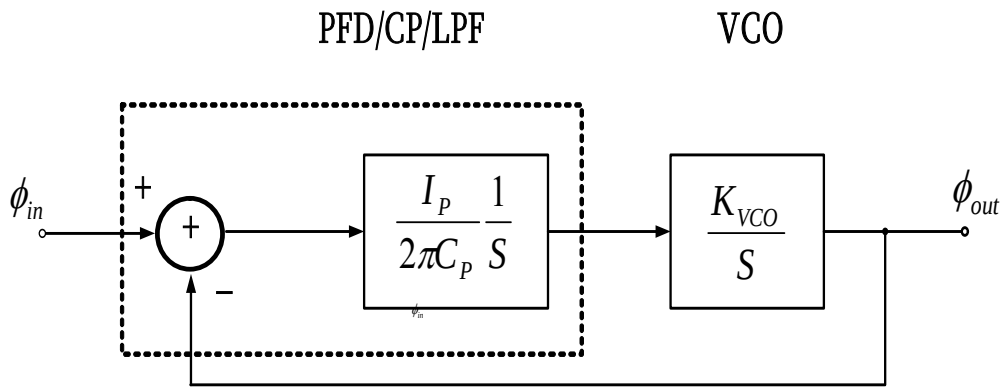


Fig 2-7 Linear model of simple charge-pump PLL

In order to quantify the behavior of charges-pump PLLs, a linear model is developed in Fig 2-7. If we consider the impedance of C_P in S domain, the impedance is $1/SC_P$. And then we think about the PFD and charge pump. When there is a phase difference between input and out put phase, this phase error will produce a peak at PFD output. If the output phase is less than input phase, the peak will appear at Q_A. On the contrary, the peak will appear at Q_B. This peak will turn on the UP or DOWN current of charge pump. And it charges or discharges the loop filter. The time width of this peak depends on the phase differential value of input and output phase. So the PFD and charge pump can be modeled as $\frac{I_P}{2\pi}$. The linear-time model in Fig 2-7 can approximate the discrete-time model.

The model in Fig 2-7 can give us an open-loop transfer function.

$$\frac{\phi_{out}}{\phi_{in}}(s)_{open} = \frac{I_P}{2\pi C_p}\frac{K_{VCO}}{S^2} \qquad (6)$$

Since the loop gain has two poles at the origin, this topology is called a type II PLL. The close-loop system is unstable because the loop gain has two poles at the origin. In order to stabilize the system, the phase characteristic must be modified such that the phase shift is less than 180^o at the gain crossover. The phase margin is compensated

by adding a resistor in serious with the loop filter capacitor C_P (Fig 2-8). So, now the PFD/CP/LPF has a transfer function

$$\frac{V_{out}}{\Delta\phi}(S) = \frac{I_P}{2\pi}(R_P + \frac{1}{SC_P}) \tag{7}$$

And the PLL open-loop transfer function is becoming to

$$\frac{\phi_{out}}{\phi_{in}}(S)_{open} = \frac{I_P}{2\pi}(R_P + \frac{1}{SC_P})\frac{K_{VCO}}{S} \tag{8}$$

Therefore the closed-loop transfer function is as follow

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P SC_P + 1)}{S^2 + \frac{I_P}{2\pi}K_{VCO}R_P S + \frac{I_P}{2\pi C_P}K_{VCO}} \tag{9}$$

$$Wn = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \tag{10}$$

$$\varsigma = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} \tag{11}$$

Where W_n is the nature frequency and ς is the damping factor.

$\varsigma < 1$: under damping

$\varsigma = 1$: critical damping

$\varsigma > 1$: over damping

Finally, the C_{P2} is added in the loop filter to reduce the ripple on the control voltage. If C_{P2} is about one fifth to one-tenth of C_P. the closed-loop time and frequency responses remain relatively unchanged and remain the same with equation (9). But C_{P2} yielding a third-order PLL and create stability difficulties.

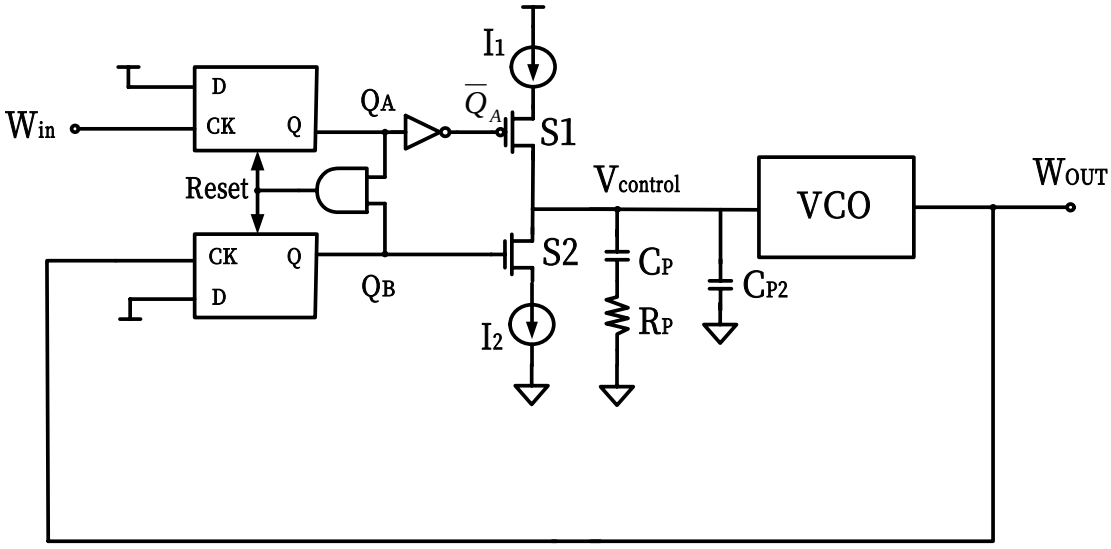


Fig 2-8 Add R_P to compensate the loop and C_2 to reduce ripple on the control voltage.

As we know the C_{P2} will make the PLL transfer function become a third-order transfer function. But (9) is still can be a good approximation, if the C_{P2} is large enough. And then let (9) become

$$H(s)=\frac{\frac{I_P K_{VCO} R_P}{2\pi}\left(S+\frac{1}{R_P C_P}\right)}{S^2+\frac{I_P K_{VCO} R_P}{2\pi}S+\frac{I_P K_{VCO} R_P}{2\pi}\frac{1}{R_P C_P}} \tag{12}$$

And let $I_P K_{VCO} R_P / 2\pi = K$, and $1/R_P C_P = W_2$. Therefore, equation (12) becomes

$$H(S)=\frac{K(S+W_2)}{S^2+KS+KW_2}\cong\frac{K(S+W_2)}{S^2+(K+W_2)S+KW_2}, (W_2 < 1/4K)$$

(13)

And then

$$H(S)=\frac{K(S+W2)}{(S+W_2)\cdot(S+K)}=\frac{K}{S+K} \tag{14}$$

So, K can be approximate the loop bandwidth of the third-order PLL. And W_2 is the zero of the PLL loop.

And the extra pole of the PLL can be calculated by anglicizing the impedance of the second-order loop filter. The extra pole is added to reduce the noise on the control voltage of VCO.

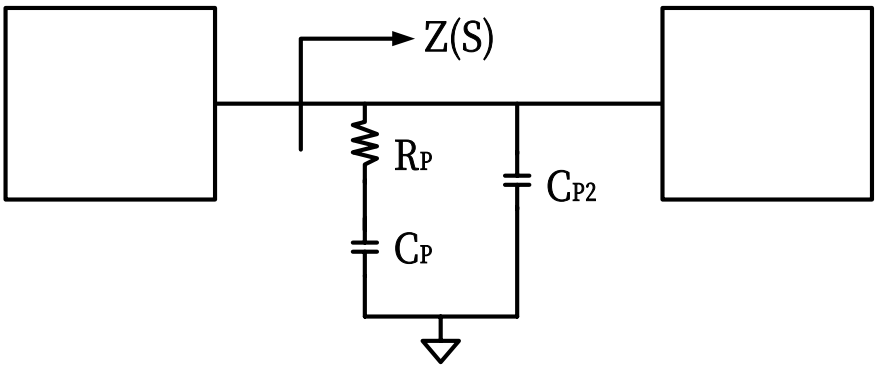


Fig 2-9 The impedance of loop filter.

As show in Fig 2-9, Z(S) is given by

$$
\begin{aligned}
z(S) &= C_{P2} //(R_P + \frac{1}{SC_P}) \\
&= \frac{1 + SC_P R_P}{S[SC_{P2}C_P + (C_{P2} + C_P)]} \\
&= \frac{C_P R_P (S + \frac{1}{R_P C_P})}{(C_P + C_{P2})S[\frac{S}{\frac{(C_P + C_{P2})}{C_P C_{P2} R_P}} + 1]} \equiv K_L \frac{S + W_2}{S(\frac{S}{W_3} + 1)}
\end{aligned}
\tag{15}
$$

where $K_L=C_PR_P/C_P+C_{P2}$, $W_2=1/C_PR_P$, $W_3=(C_P+C_{P2})/C_PC_{P2}R_P=W_2(1+(C_P/C_{P2}))$.

W_3 is the extra pole of the third-order PLL.

where

$\varsigma < 1$: under damping when $W_2<K/4$

$\varsigma = 1$: critical damping when $W_2=K/4$, persent overshot=13%

$\varsigma > 1$: over damping when $W_2>K/4$

typically, ς is selected between 0.5 and 1 to yield optimum overshot and noise performance. Therefore, a good rule of thumb is to make $W_2=K/4$ when peaking is not critical.

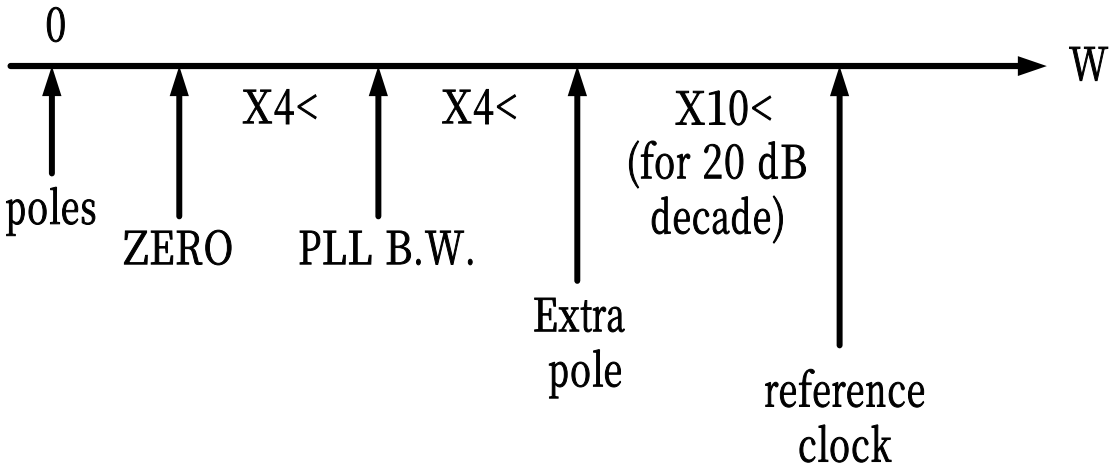


Fig 2-10 Interrelation between pole and zero in third-order PLL.

There are some frequency component should appear in type II second-order PLL as follow.

1. W_2 : zero frequency $W_2=1/R_PC_P$
2. W_3 : extra pole frequency $W_3=W_2(C_P/C_{P2}+1)$
3. W_n : nature frequency $W_n=\sqrt{I_PK_{VCO}/2\pi C_P}$ (second-order approximation)
4. K : loop bandwidth $K=K_{VCO}I_PR_P/2\pi$
5. ς : damping factor $\varsigma=(R_P/2)\cdot\sqrt{I_PC_PK_{VCO}/2\pi}$
6. W_{ref} : reference clock $W_{ref}=2\pi\cdot f_{ref}$

In order to make sure ς near 1, the W_2 is often choused as K/4. As shows in Fig 2-10, the extra pole is choused four times loop bandwidth to let the phase margin about 62^o and one-ten to reference clock to reduce the reference noise 20dB.

2.3 APPLICATION IN FREQUENCY SYNTHESIZER

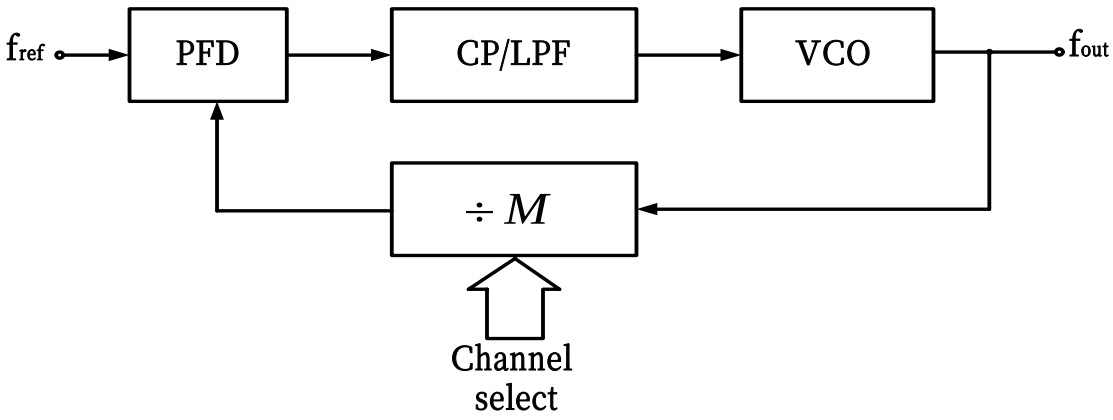


Fig 2-11 Block diagram of frequency synthesizer

Fig 2-11 shows the architecture of a PLL based frequency synthesizer. The channel select input is a digital word that varies the value of M ($f_{out}=Mf_{ref}$). As with the feedback divider in the loop alters the system characteristics. Equation (12) is rewrite as follow.

$$H(S)=\frac{\frac{I_P K_{VCO}}{2\pi C_P}(SR_P C_P+1)}{S^2+\frac{I_P}{2\pi}\frac{K_{VCO}}{M}R_P\cdot S+\frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}} \tag{16}$$

Those frequency components are rewritten as follow

The loop bandwidth is become

$$K=\frac{K_{VCO}I_P R_P}{2\pi\cdot M} \tag{17}$$

The extra poleW_3 and the zero W_2 are not changed.

$$W_n=\sqrt{\frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}}=\sqrt{K\cdot W_2} \tag{18}$$

$$\varsigma=\frac{R_P}{2}\sqrt{\frac{I_P C_P}{2\pi}\frac{K_{VCO}}{M}}=\frac{1}{2}\sqrt{\frac{K}{W_2}} \tag{19}$$

2.4 NONIDEAL EFFECTS IN PLL

Several imperfections in the PFD/CP circuit lead to high ripple on the control voltage even when the loop is locked. As it shows in Fig 2-12(a), when the reference clock and the output clock have a phase difference $\Delta\phi$, it will cause one of the PFD outputs Q_A or Q_B producing a peak. But if the $\Delta\phi$ is too short, the peak voltage of PFD output may not have enough potential to turn on the charge pump current source. This problem is often called dead zone of PFD.

In order to cancel the dead zone of PFD, the coincident pulse is generated by PFD with zero phase difference as Fig 2-13 shows.

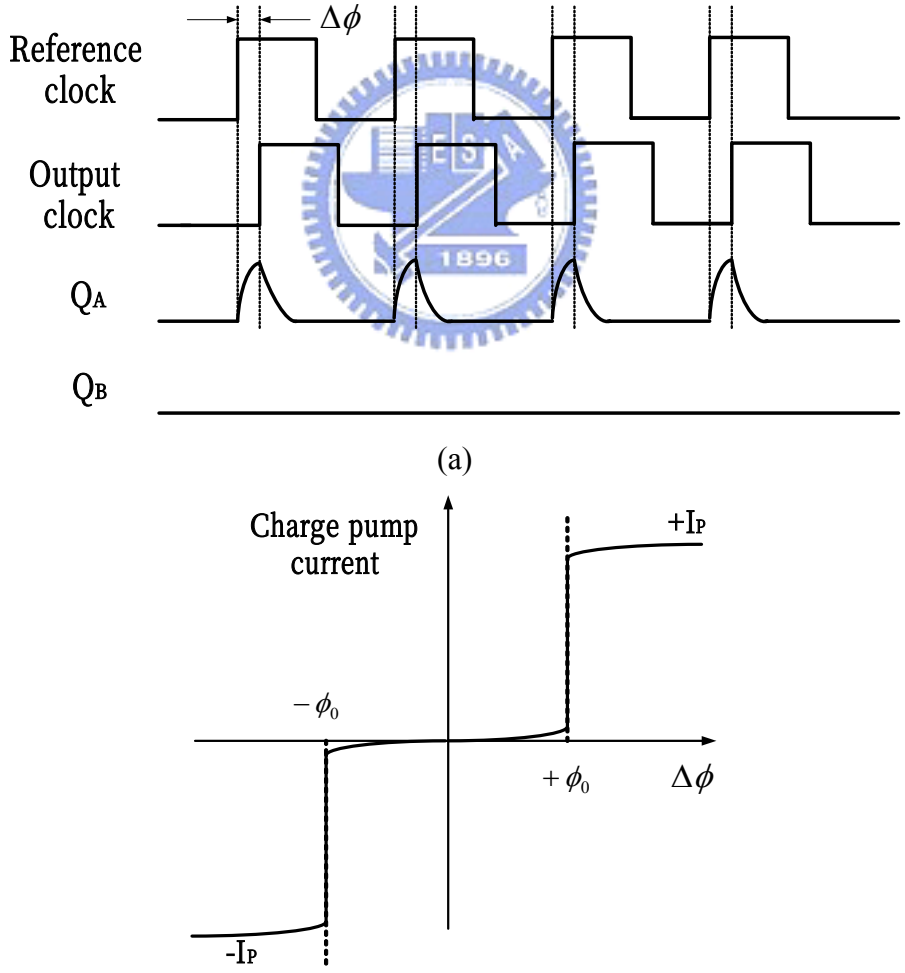


Fig 2-12 (a) A small input phase difference (b) Dead zone of charge pump current.

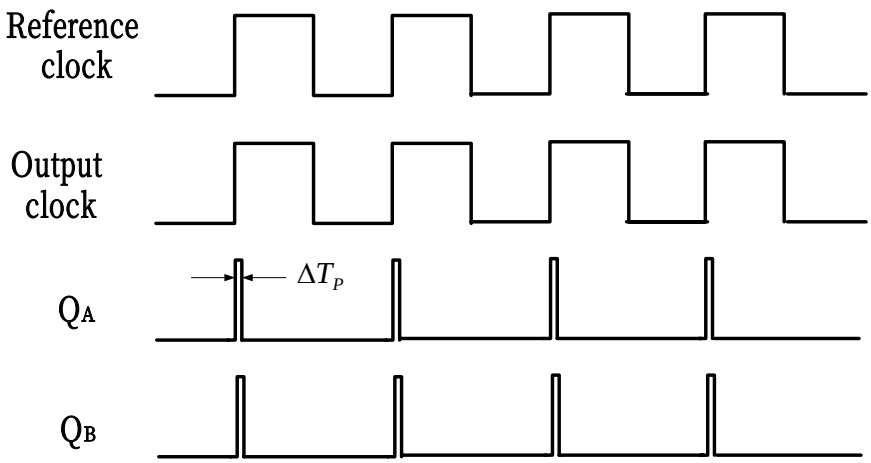


Fig 2-13 Coincident pulses generated by PFD with zero phase difference.

While eliminating the dead zone, the reset pulse on Q_A and Q_B introduce other difficulties. The first issue in the circuit of Fig 2-8 stems from the delay difference between $\overline{Q}_A$ and Q_B in turning on their respective switches. This issue can be solved by adding a transmission gate after Q_B and equalizing the delay. The second issue in the CP of Fig 2-8 related to the mismatch between the currents of I_1 and I_2. As depicted in Fig 2-14, even with perfect alignment of the UP and DOWN pulses, the mismatch current produced by the charge pump is nonzero, changing $V_{control}$ by a constant increment at each phase comparison instant.[1]

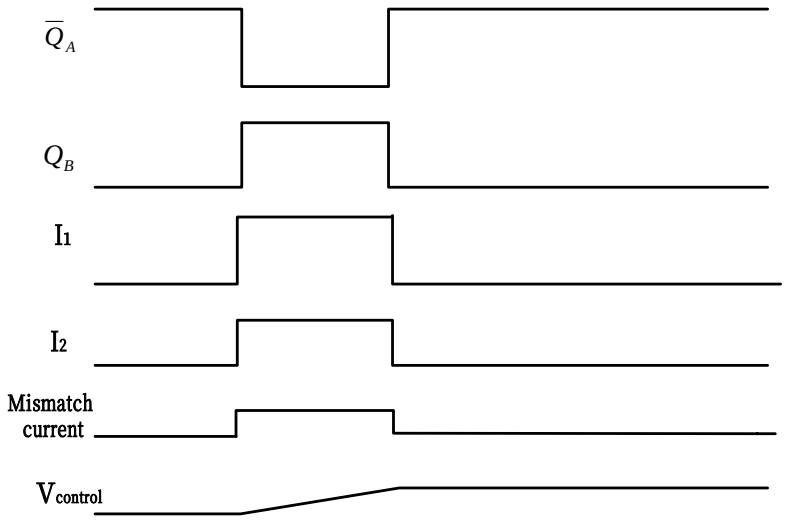
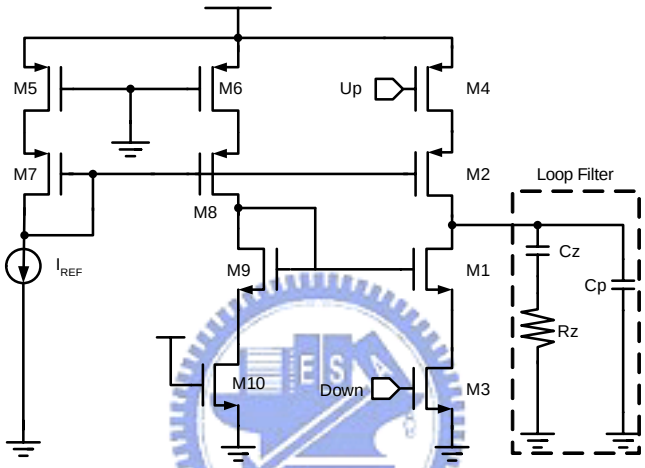


Fig 2-14 Effect of mismatch current in charge pump.

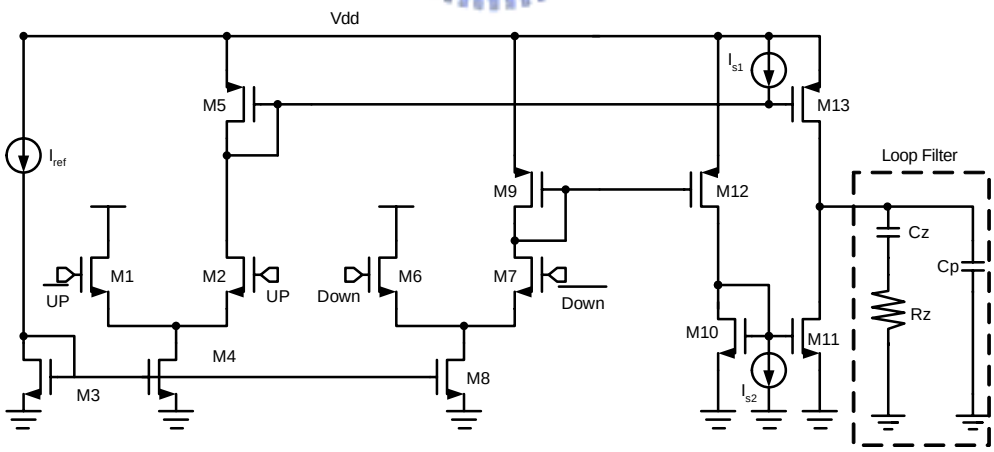
2.5 THE CURRENT-MISMATCH EFFECT OF CHARGE PUMP AND REVIEWS OF CURRENT-MATCH CHARGE PUMP

In the last of previous session, the mismatch current of charge pump is mentioned. In this section, what the real effect in our frequency synthesizer will be discussed.

We can subdivide conventional charge pump circuit into current-switching charge pump [11] and current-steering charge pump circuit [12], as shown in Fig 2-15



(a) Current-switching charge pump circuit [11].



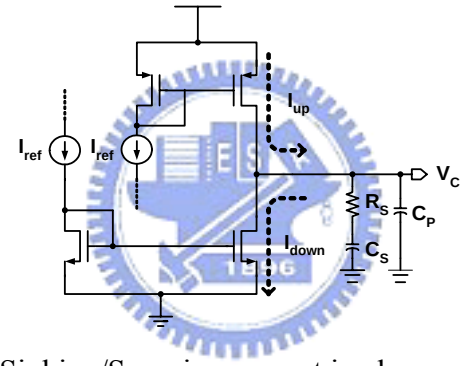
(b) Current-steering charge pump circuit [12]

Fig. 2-15 Conventional charge pump circuits

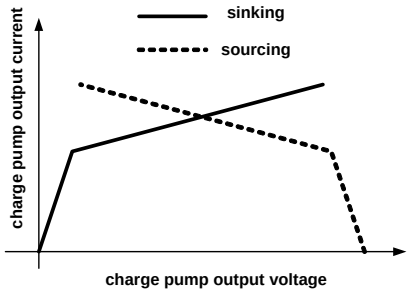
Obviously, from above schematic, the drain current of sinking and sourcing will

vary with drain voltage of M1 and M2 in Fig 2-15 (a), M11 and M13 in Fig 2-15 (b), since different channels will have different voltages on loop filter. For conventional charge pump circuit, perfect current match occurs only when the voltage of loop filter is center of the supply voltage. The sinking and sourcing current difference is relatively large when the voltage of loop filter is near supply voltage or ground.

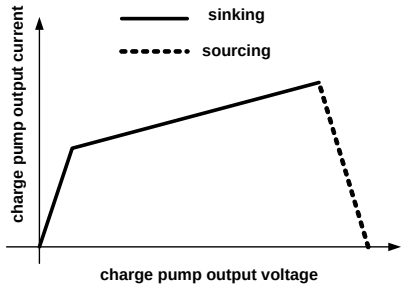
The goal of this thesis is to make the charge and discharge current equal, even those current will vary due to difference of voltage on loop filter, different temperature and process drift, as illustrated in Fig 2-16 (c) [13], therefore the difference between sinking and sourcing current will relatively small except that MOS not longer in saturation region, as shown in 2-16 (d).



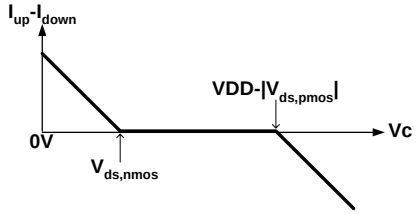
(a) Sinking/Sourcing current in charge pump



(b) Sinking/sourcing current mismatch unless charge pump output voltage is 1/2Vdd



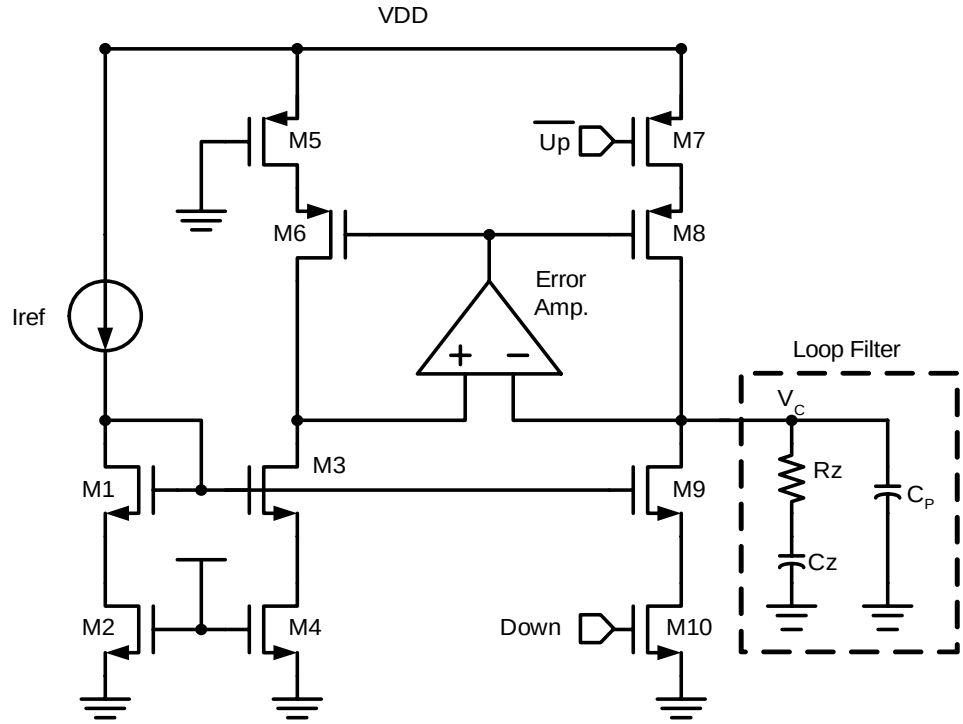
(c) Sinking and sourcing current is match, no matter what charge pump output voltage



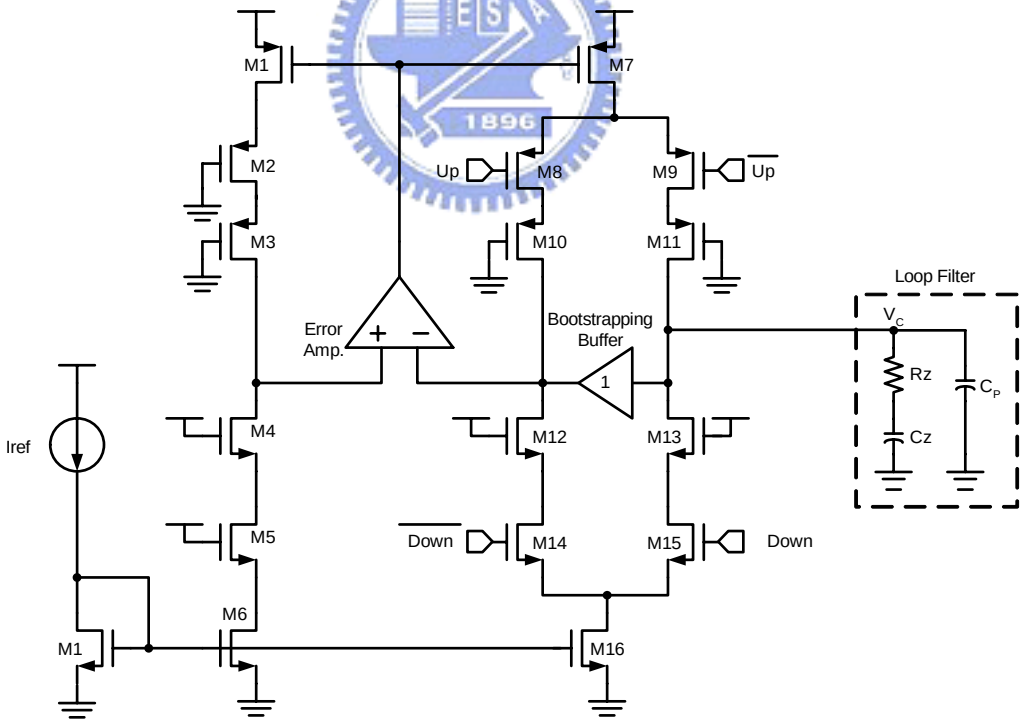
(d) No current output from charge pump circuit when sinking/sourcing current is match

Fig. 2-16 The concept of current matching characteristic

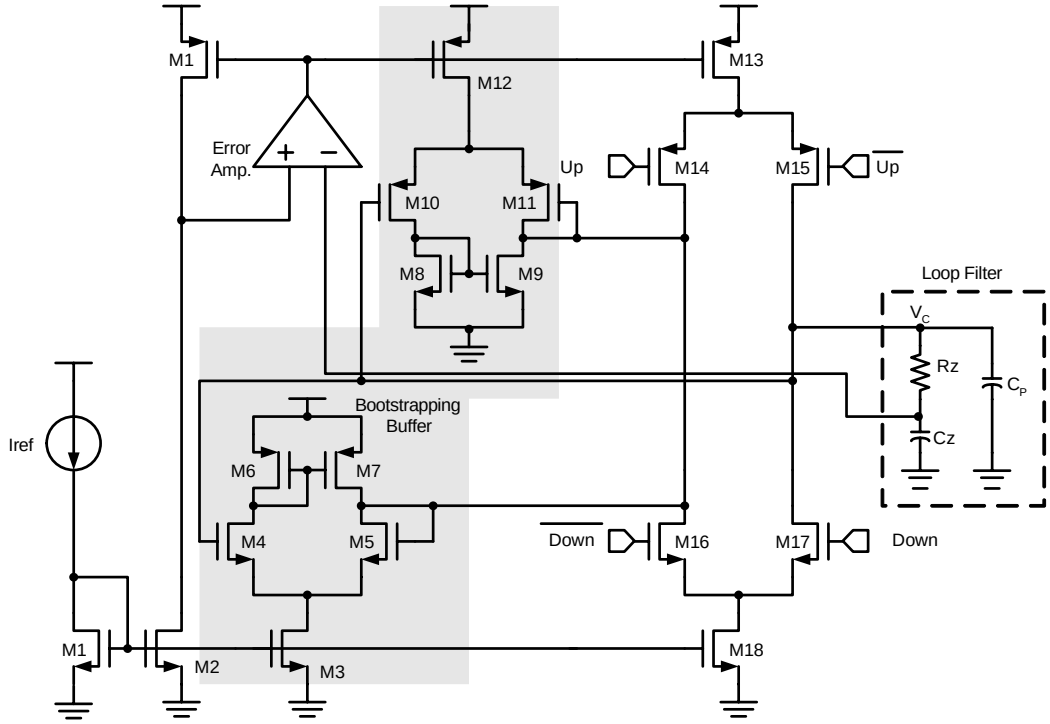
There are some conventional charge pumps circuits have been improved to perfect current match one [13] [15] [16]. In Fig 2-17 (a) [13], by using an error amplifier and reference current source, one can achieve a charge pump with good current matching characteristics. In Fig 2-17(b) [16], also provided a charge pump with good current matching characteristics, the function of feedback network is the same as the error amplifier in Fig 2-17(a), a bootstrapping buffer forces the unused output in charge pump core to the same voltage as the main output.



(a) Charge pump circuit with perfect current matching characteristic [13]



(b) Charge pump circuit with perfect current matching characteristic [16]



(c) Charge pump circuit with perfect current matching characteristic [15]

Fig. 2-17 Examples for charge pump circuit with perfect current matching characteristics

CHAPTER 3

ARCHITECTURES OF THE 1-V FREQUENCY SYNTHESIZER

3.1 DESIGN CONSIDERATION

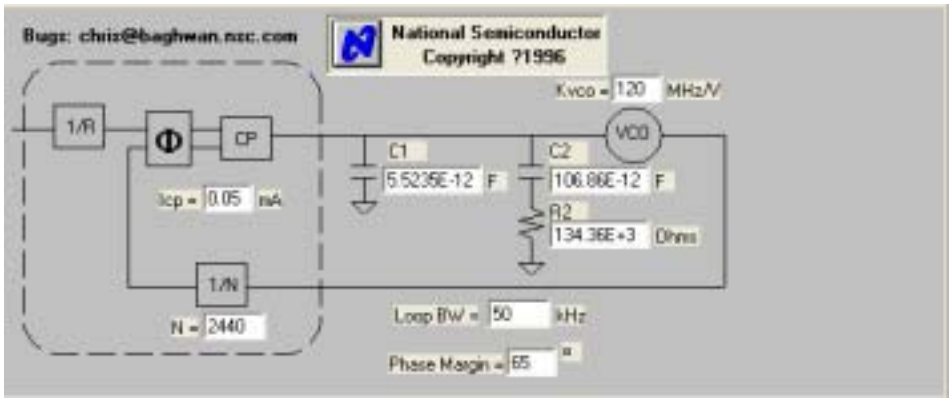
The type II PLL is choused to realize this design. At first we have to choose the loop bandwidth of PLL. According to (20) [1]

$$\pm\alpha(M+k)=\frac{k}{\sqrt{1-\varsigma^2}}\exp(-\varsigma\cdot\omega_n\cdot Ts) \tag{20}$$

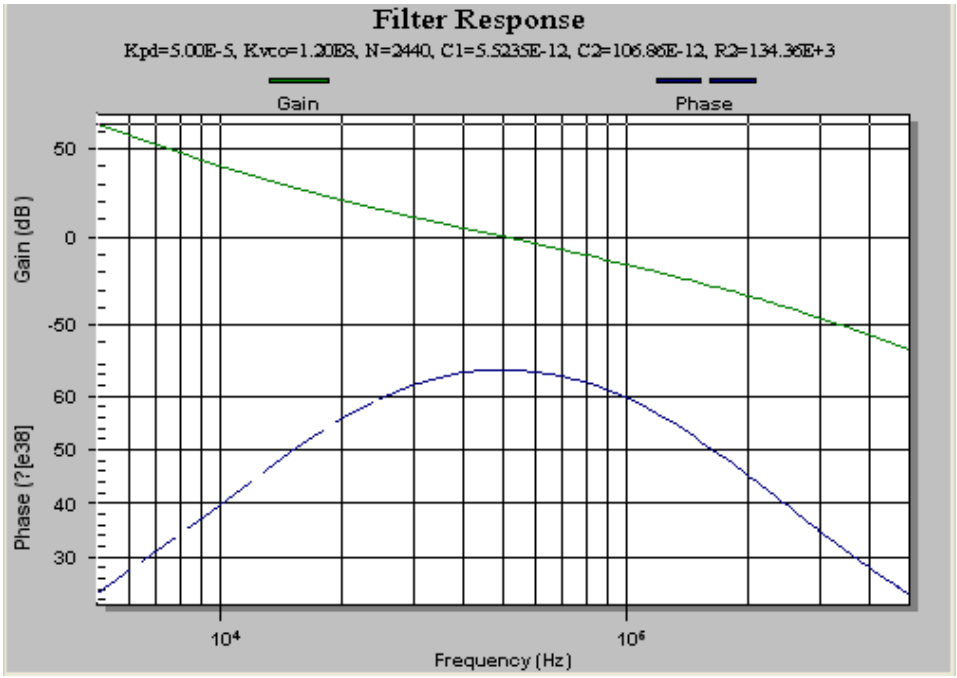
Where Ts is the locking time of the PLL, ς is the damping factor, α is the settling accuracy, M is the minimum dividing ratio of the frequency divider and (M+k) is the maximum dividing ratio of the frequency divider.

$$Ts\approx\frac{1}{\varsigma\omega_n}\ln\frac{k}{M|\alpha|\sqrt{1-\varsigma^2}} \tag{21}$$

The locking time of the Bluetooth application is 200-usec, so we have to choose a loop bandwidth to achieve this spec. First, we assume the damping factor $\varsigma=\sqrt{2}/2$. Second the channels of Bluetooth application is 2400-MHz~2480-MHz, so M=2400 and k=80. Finally assume the locking time Ts=140-usec(for a over design). The Wn is calculated about 25-kHz. According to equation (18), the Wn is equal to $\sqrt{KW_2}$. Where K is the loop bandwidth and W_2 is the zero of the PLL. If we assume $K=4W_2$ for a reasonable phase margin, the loop bandwidth is equal to 50-KHz. The loop bandwidth is got and if we assume the PM=65^{o}, the values of resister and capacitances in the loop filter of PLL can be calculated and be shown in Fig 3-1 (a).



(a)



(b)

Fig 3-1 The PLL loop filter design (a) PLL loop design software (b) Bode-plot of the loop gain and phase margin in this frequency synthesizer

As shown in Fig 3-1 the gain of VCO is 120-MHz, the charge pump current is 50-uA and the phase margin which is shown in Fig 3-1 (b) is 65^{o}.

3.2 CIRCUIT REALIZATIONS

Fig 3-2 shows the block diagram of integer-N frequency synthesizer and each block will be discussed in next section

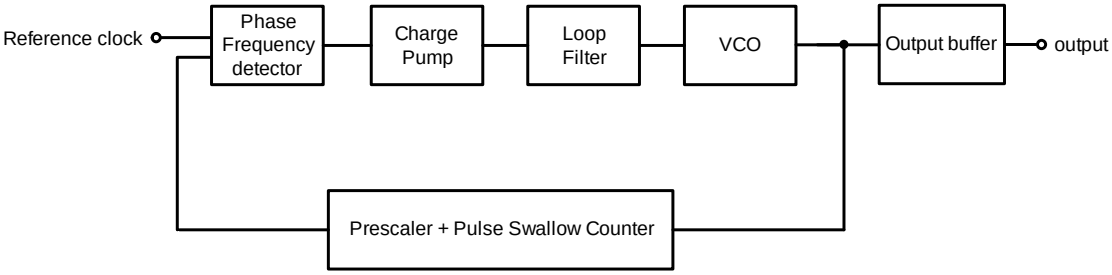


Fig 3-2 Block diagram of the integer-N frequency synthesizer used in this design.

3.2.1 1 V Charge Pump

In 1-V design, the charge pump is hard to use the cascode structure. So, in this design the current-steering charge pump is used. But the current-steering charge pump still suffers from the current mismatch issue. So, the current-match technique is used in this design.

3.2.1.1 Current-match charge pump

Because of the effect of channel length modulation, in the conventional current-steering charge pump circuit I_{up} and I_{down} can not mach at whole V_c voltage, even if M10 and M11 are sizing as the ratio of their mobility ratio and same over-drive voltage**.** At every reference clock edges, the I_{up} and I_{down} will both turn on for a very short time to cancel the dead zone effect of PFD. At this moment, if the I_{up} and I_{down} are not match each other, the mismatch current will become noise to next stage (LPF). This noise will increase the spur level of VCO output spetrum.

Fig 3-3 shows the current-match charge pump circuit. As mentioned in chapter 2, the current-match charge pump has a function which can make the up and down currents match each other. The right-part of Fig 3-3 is the current-steering charge

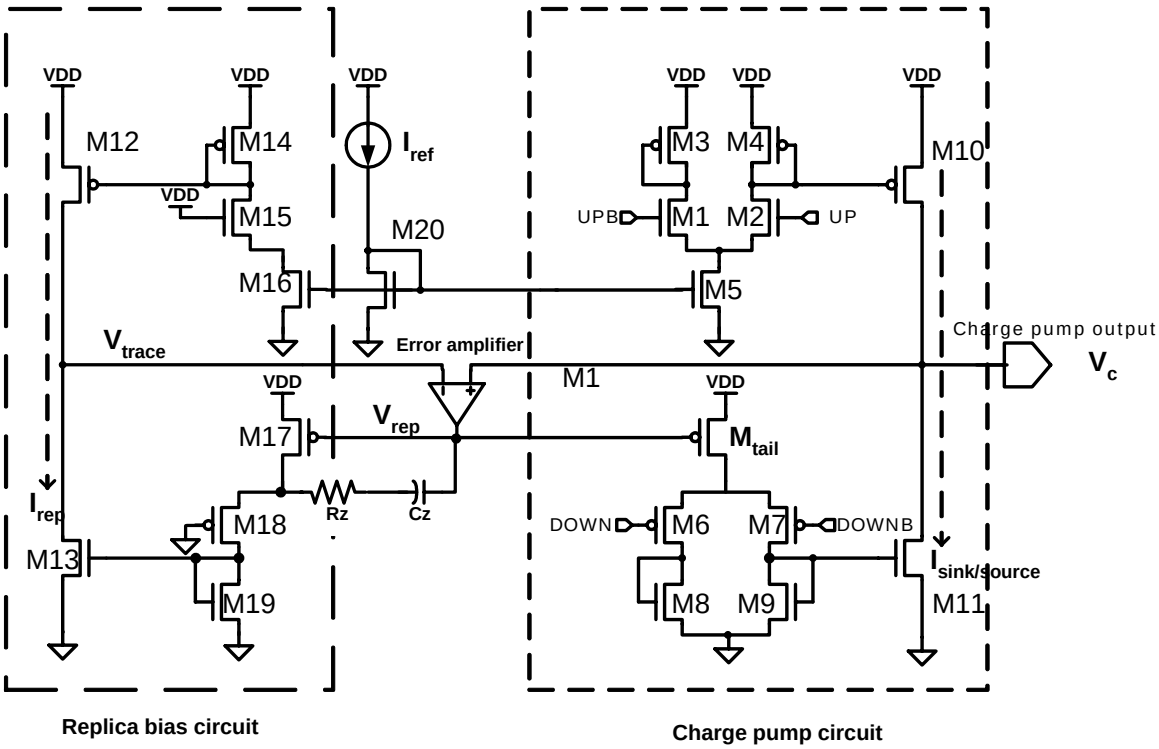
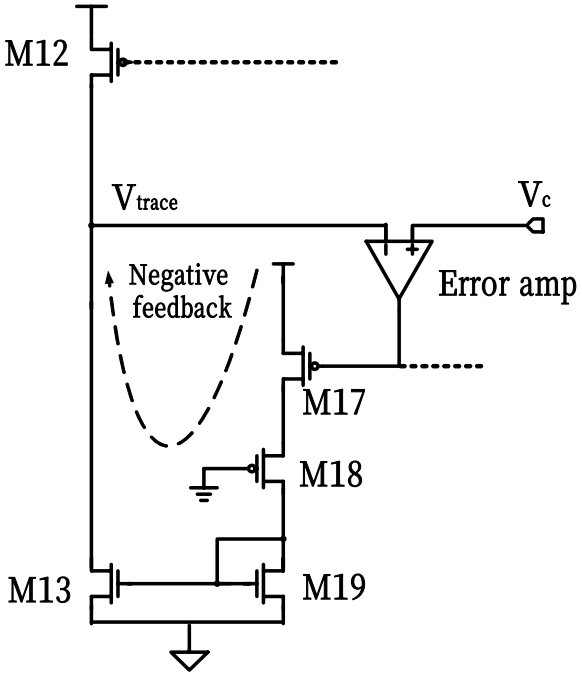


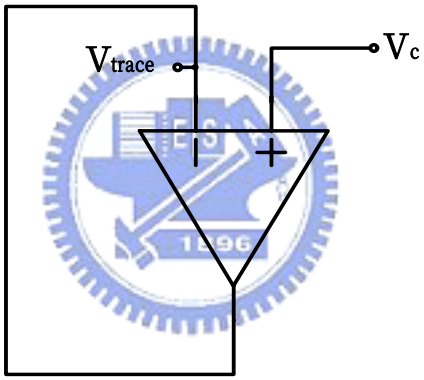
Fig 3-3 Current-match charge pump architecture used in this design [5]

pump core circuit, and the left-part is the replica bias circuit. This replica circuit is used to give the M12 and M13 the same bias as M10 and M11. The left-part is a replica bias circuit with a feedback loop, which can tune the I_{down} to match I_{up} automatically when V_C is varying.

Fig 3-4 shows the half circuit of Fig 3-3 and it can be equivalent to unit gain buffer. We can view the error-amp as the first stage, the M17 is the second stage amplify and the M18 in triode region serious with M19 in diode connecting. The third stage is common source amplify M13 with the output load $r_{O12}//r_{O13}$. Those stages amplify the difference of V_c and V_{trace}. And the negative feed back to V_{trace}. We can view these three stage as a op-amp as Fig 3-2 (b) shows. This is a voltage follow buffer and it means the V_{trace} will tracing V_c when V_c varies it value. So, we can calculate the gain of op-amp in Fig 3-2 (b) as follow.



(a)



(b)

Fig 3-4 (a)The feedback loop of the current-match charge pump shows in fig 3-1, (b)The equivalent circuit of the circuit in (a)

Assume the gain of the first stage error-amp is A_{error}. Than the next stage a PMOS common source stage, and the gain is as follow

$$A_2 = g_{m17} \cdot (R_{18} + \frac{1}{g_{m19}}) \cdot \frac{\frac{1}{g_{m19}}}{R_{18} + \frac{1}{g_{m19}}} \qquad (20)$$

$$= \frac{g_{m17}}{g_{m19}}$$

Where R_{18} is the equivalent resistor of M18 in triode region and $1/g_{m19}$ is the equivalent resistor of M19 in diode connecting.

The third stage is also a common source stage and its gain is as follow

$$A_3 = g_{m13} \cdot (r_{o12} // r_{o13}) \tag{21}$$

The overall gain of the feedback loop is

$$\begin{aligned} A_{open} &= A_{error} \cdot A_2 \cdot A_3 \\ &= A_{error} \cdot \frac{g_{m17} \cdot g_{m13}}{g_{m19}} \cdot (r_{o12} // r_{o13}) \end{aligned} \tag{22}$$

Then assume the difference between V_c and V_{trace} is V_{error}

$$V_{error} = (V_c - V_{trace}) = \frac{1}{1 + A_{open}} \cdot (V_c - \frac{V_{DD}}{2}) \tag{23}$$

And the channel-length modulation coefficient is $\lambda \cong 0.2$. So, if we assume the maximum (V_c-1/2V_{DD}) is 0.3V. According to the square law of MOS $I_D = 1/2KW/L \cdot Vov \cdot (1 + \lambda V_{DS})$, we can calculate the maximum mismatch current by follow equation

The mismatch current $\cong 2 \times \lambda \times V_{error} \times I_{up/down} = \frac{0.12}{1 + A_{open}} \cdot I_{up/down}$ (24)

So, if the A_{open} is large than 22.27 dB, the current mismatch will less than 1%.

In simulation, when Vc is equal to 0.8 V and A_{open} is 30 dB, the current mismatch is about 1.06%.

3.2.1.2 The Start-up Problem of Current-match Charge Pump

As mention in chapter 1, there is a serious problem may happen in the current-match charge pump which shown in fig 3-1. Because the op-amp's output node is a high impedance node. When the supply voltage grows up like a ramp of time, and takes about 500 us to reach VDD, the V_c may be pulled up to approach VDD. Then the V_c will be out of the input range of the error-amp, and the error-amp turn off. So, M9 turns off and the I_{down} becomes zero. At this time, the charge pump no longer works. The closed loop of the frequency synthesizer fails to have correct

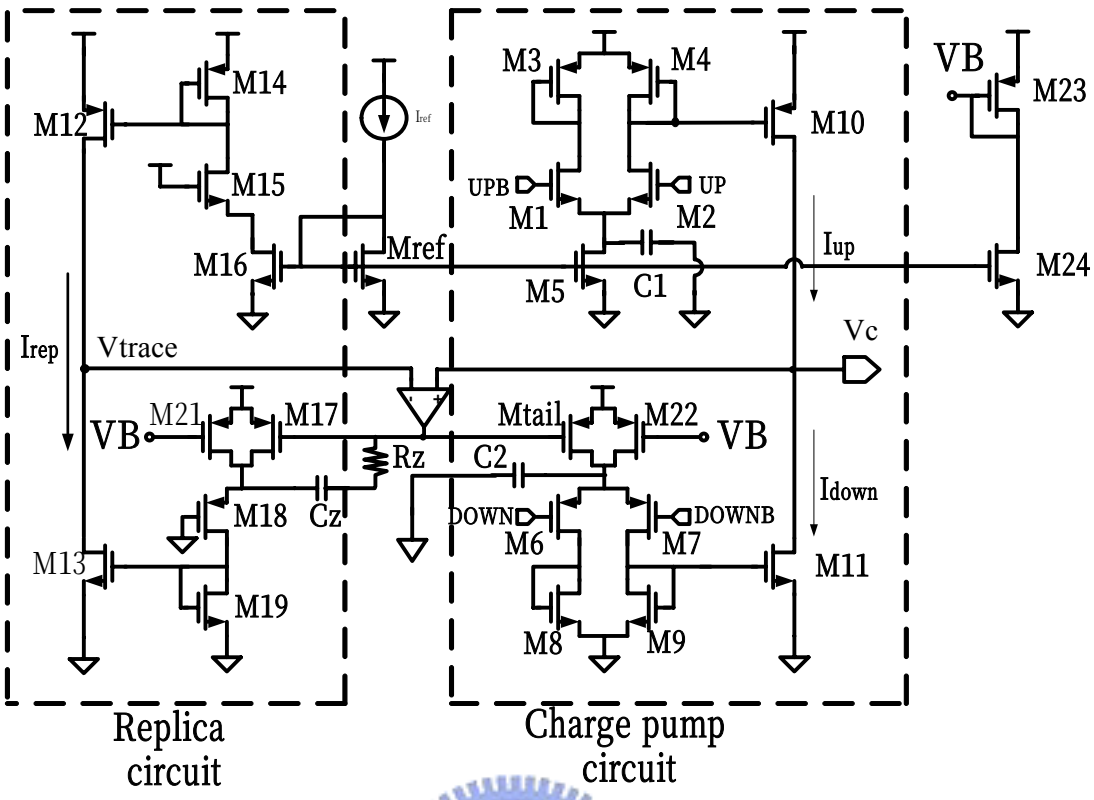


Fig 3-5 New current-match charge pump. M21 and M22 are added to solve the start-up problem. The parameter information is in Table 3-1.

function, and the output frequency of the synthesizer will always keep high.

The new current-match charge pump circuit is shown in Fig 3-5. M21 and M22 are added to give a constant bias for I_{down}, it can suppress the V_c going to near VDD. This improvement is simulated and shown in section 3.3

3.2.1.3 The Input rail-to-rail Op-amp Used in the 1-V Current-match charge pump

There is another problem of the 1 V current-match charge pump. When the supply voltage of the current-match charge pump drops to 1 V, the input rail-to-rail op is fail to work. The conventional input rail-to-rail architecture shown in Fig 3-6 can't work

in 1-V supply voltage. There is an input dead zone. The dead zone happens when VDD does not follow equation (25)

$$V_{DD} \geq V_{GS(N)} + V_{GS(P)} + 2V_{DS(SAT)} \tag{25}$$

Where VDD is the supply voltage, $V_{GS(N)}$ is the gate-to-source voltage of the N-MOS input stage $V_{GS(P)}$ is the gate-to-source voltage of the P-MOS input stage and the $V_{DS(SAT)}$ is the drain-to-source voltage of the current sources.

How the dead zone happening is shown in Fig 3-7. As shown in (a), there is two boundary and three region. As it shown in (b), the boundary of PMOS will change the value following VDD. So, if the VDD is getting lower, the boundary of the P-MOS will lower. As it shown in (c), when the VDD is low enough to make the P-MOS boundary be lower than the N-MOS boundary. There will be a region which the N-MOS and P-MOS of the input stage both tune off and this region is called dead zone of this input stage.

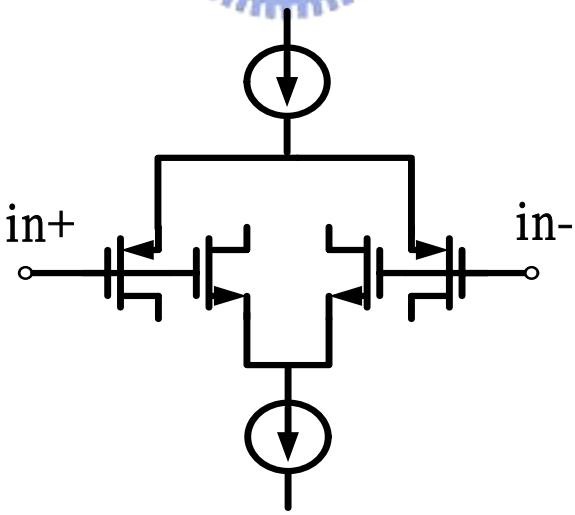
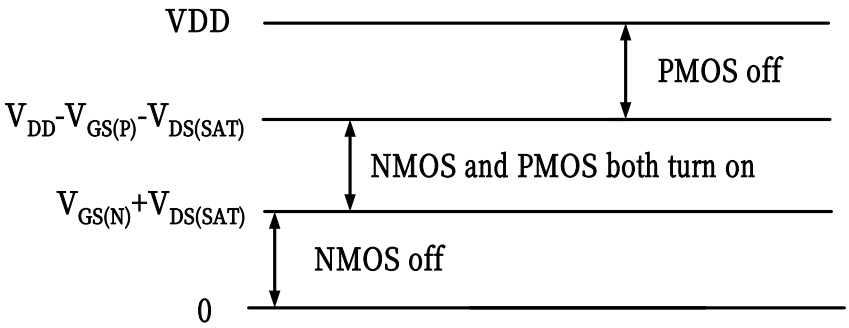
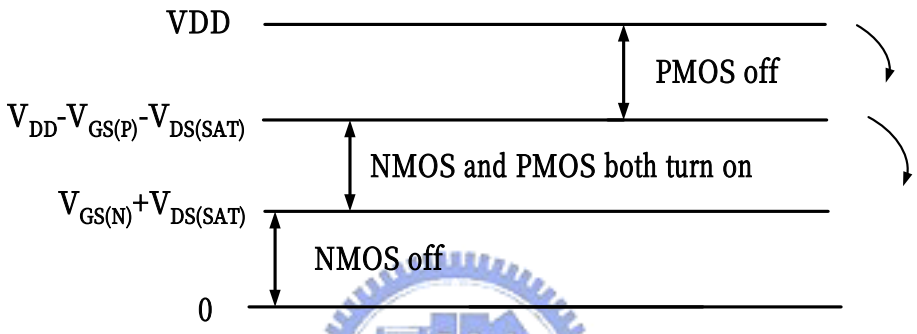


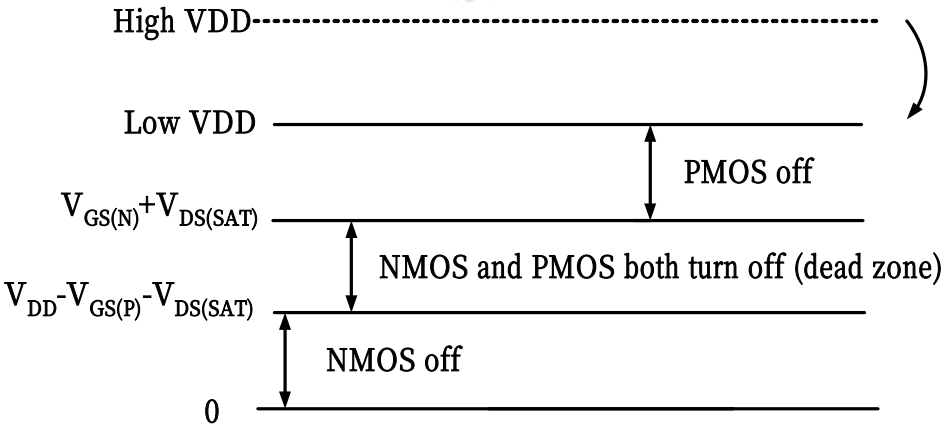
Fig 3-6 The conventional input rail-to-rail stage.



(a) There are three regions of the input rail-to-rail stage shown in Fig 3-6.



(b) When the VDD drops, the boundary of PMOS off region will also drop.



(c) If the boundary of PMOS off region drops to lower than NMOS off region, the dead zone will appear, and the input stage will not work.

Fig 3-7 The dead zone of conventional op-amp explanation.

So, the bulk-driven input stage [9] is used in this design. The 1-V input rail-to-rail op-amp is shown in Fig 3-8. As we know, because of the body effect of MOS, the body can produce a transconductance g_{mb}. Because the g_{mb} is about 1/6 of the g_m and this kind input stage may suffer from that the input capacitance varies with the difference input common-mode voltage. But in our application, the accuracy of gain and the frequency response are not so important. And as it shown in section 3.2.1.2, the overall gain of the feedback loop is produce by three stages. So, the loop gain can be compensated by next two stages and this op-amp is suitable to be used in the 1-V current-match charge pump.

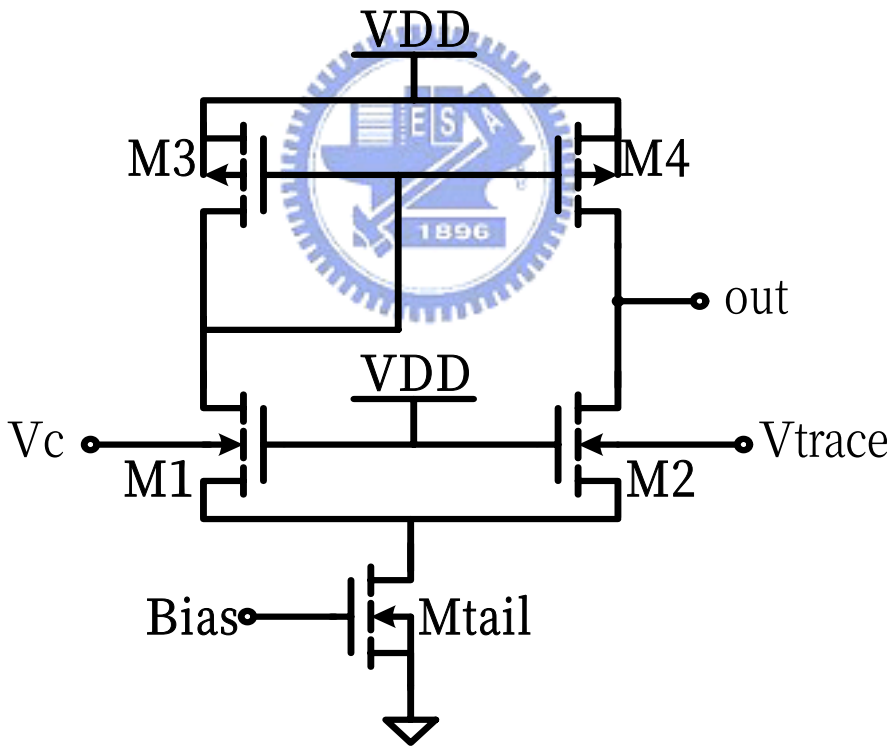


Fig 3-8 The 1-V input rail-to-rail op-amp using the bulk driven input stage. The parameter information is in Table 3-2.

3.2.2 1 V 2.4 GHz Voltage Control Oscillator

As we know, the LC VCOs usually use the cross couple pair as the negative resister. The VCOs can roughly divide into two kinds. They are N-MOS only cross-coupled VCOs and complementary cross-coupled VCOs. It has been mentioned in [2] that the complementary cross-coupled VCOs has the better phase noise than the N-MOS only cross-coupled VCOs. But in 1-V design, it is to beyond remedy to use the N-MOS VCOs in this work.

3.2.2.1 Trade-off between K_{vco} and tuning range

In 1 V design, there is another trade-off become more critical. Because the VDD becomes lower, the output voltage range of the charge pump is suppressed. So, the K_{VCO} must be increase to maintain the same tuning range. But if the K_{VCO} is larger, the VCO is more sensitive to the noise which comes from the control voltage.

An ideal VCO's mathematic expression is

$$V_{out}(t) = V_o \cos(\int \omega_{out} dt + \phi_o) \tag{26}$$

And

$$\omega_{out} = \omega_o + K_{vco} \int V_{cont} dt + \phi_o \tag{27}$$

In fact the V_{cont} is a function of time. Assume the V_{cont} has a small sinusoidal noise above its DC level.

$$V_{cont} = V_{dc} + V_m \cos \omega_m t \tag{28}$$

Put it into (28) and assume $\frac{Kvco}{\omega_m} << 1rad$, then the VCO's mathematic expression will be rewritten as follow.

$$V_{out}(t) \approx V_o \cos \omega_o t - \frac{K_{VCO} V_m V_o}{2\omega_m} [\cos(\omega_o - \omega_m)t - \cos(\omega_o + \omega_m)] \tag{29}$$

So, $V_{out}(t)$ consists of three components, those tones at $\omega_o \pm \omega_m$ are called spur.

When the spur appears in the local frequency of RF receiver, it will decade the SNR after modulation.

As it is seen in (29), the sidebands' amplitude relates to the value of K_{VCO}. So, if we can let the K_{VCO} as small as possible, the VCO output will has much smaller spur level.

3.2.2.2 Band-switching VCO

The ideal N-bits VCO output frequency v.s. the control voltage is shown in Fig 3-9. As shown in this Fig 3-9, the frequency range of VCO is split into three bands. By this way, the K_{VCO} can be lower to about 1/3 of the original K_{VCO}, and the spur level will be decade.

A 2-bits band-switching VCO [10] is shown in Fig 3-11.

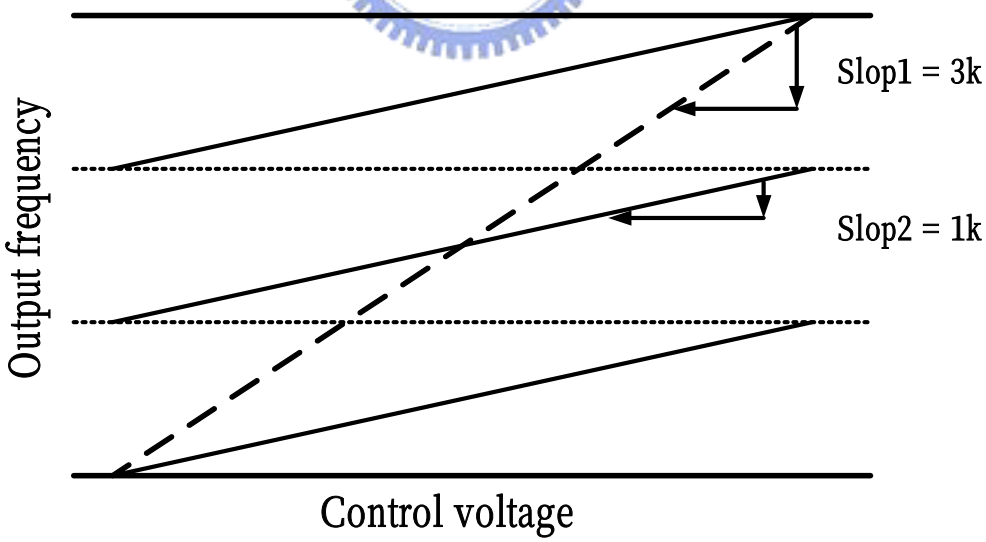


Fig 3-9 The ideal 3-bits VCO output frequency v.s. control voltage.

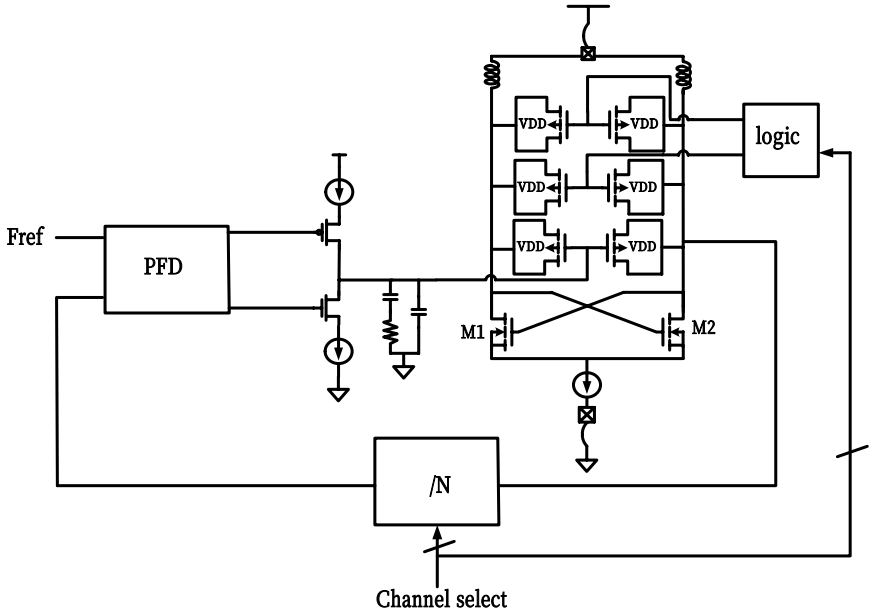


Fig 3-10 The band-switching VCO select bands from the channel selecting signal.

The PMOS varactors are used as the banks in Fig 3-10, the difference bands can be selected by connecting the source/drain of the varactors to high or low potential. Using varactors as banks help the VCO without suffering from phase noise increasing. Fig 3-11 shows the clear VCO circuit. The fourth varactor which connects to Vc3 is used to compensate the frequency.

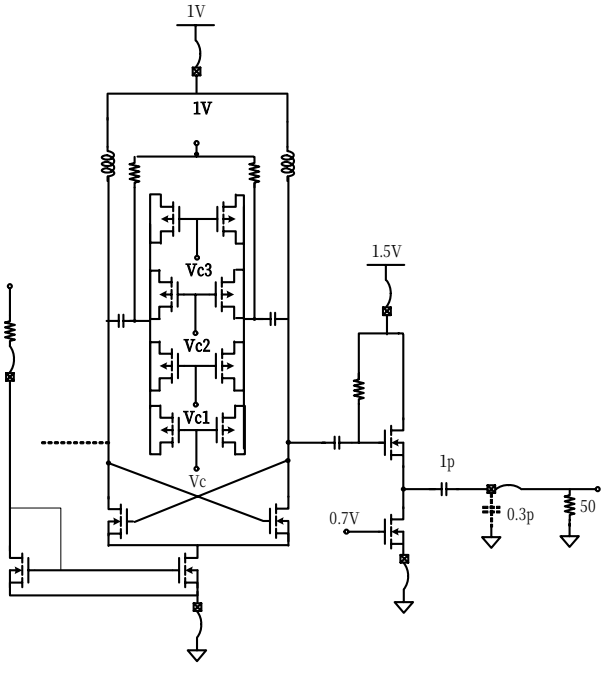


Fig 3-11 Band-switching VCO

3.2.3 1 V Frequency Divider

For integer-N frequency synthesizer, a pulse swallow counter is needed. In Fig 3-12, it shows the block diagram of frequency divider include a prescaler (/N, /N+1), a 7-bits programmable counter, and a 7-bits swallow counter. The function of pulse swallow counter is to implement the division factors. By changing the division factors, we can choose different channels. Initially, prescaler divides the input frequency by N+1. The swallow counter counts the prescaler output pulses, until number S is reached. Then the prescaler modulus control is changed, which starts dividing by N. The prescaler output pulses also counted in the programmable counter. If programmable counter has counted P pulses, it reset itself and the swallow counter. The output generates one complete cycle for $(N+1)\cdot S + N\cdot(P-S) = N\cdot P + S$ cycles at the input. The operation repeats after the swallow counter is reset. The program counter and pulse swallow counter block diagram is shown in Fig 3-13. The D-flipflop of two counters share the same D-flipflop string. The node of MC is the modulus controls which feedback to prescaler. The D-flipflop which used in pulse swallow counter is shown in Fig 3-14.

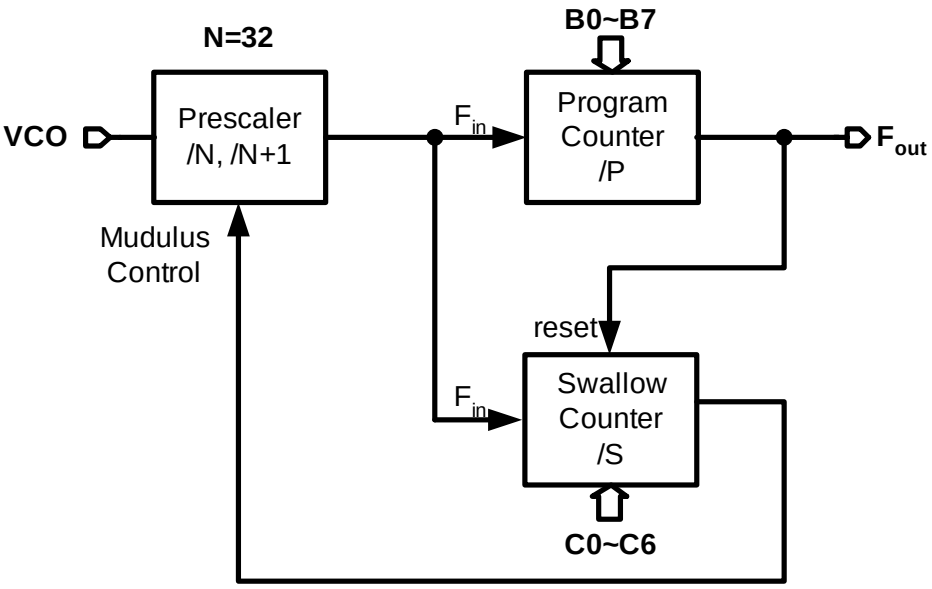


Fig 3-12 Block diagram of frequency divider.

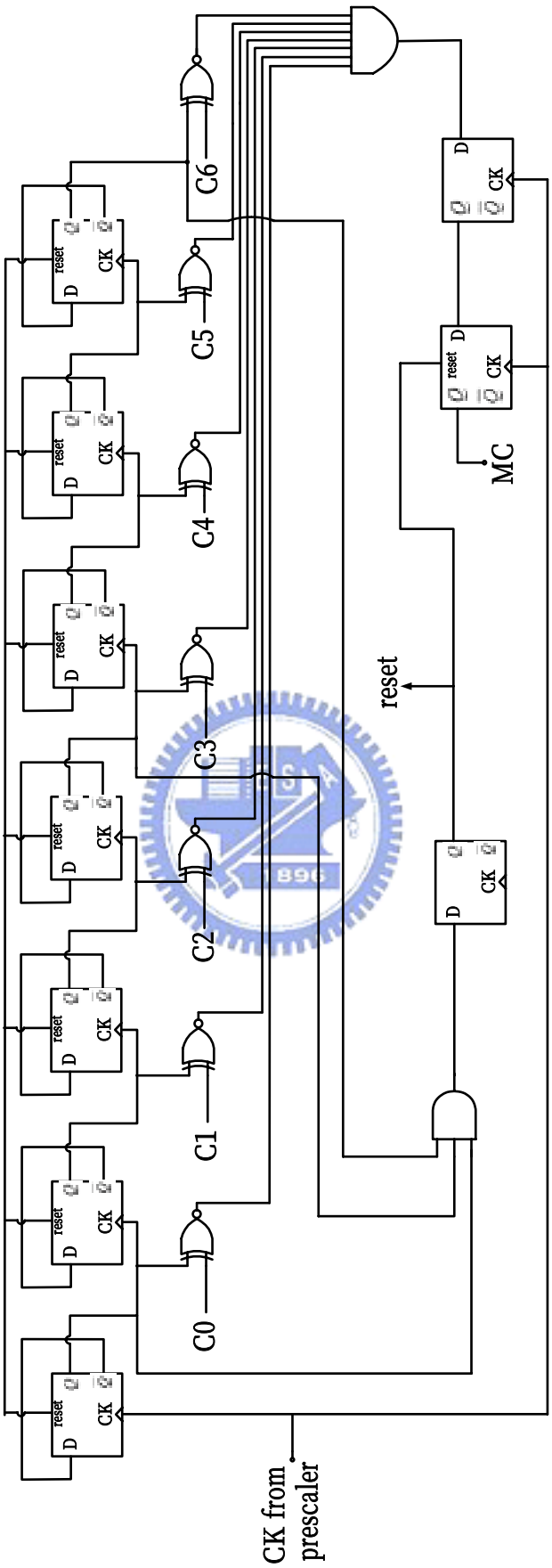


Fig 3-13 Block diagram of the program and pulse swallow counter.

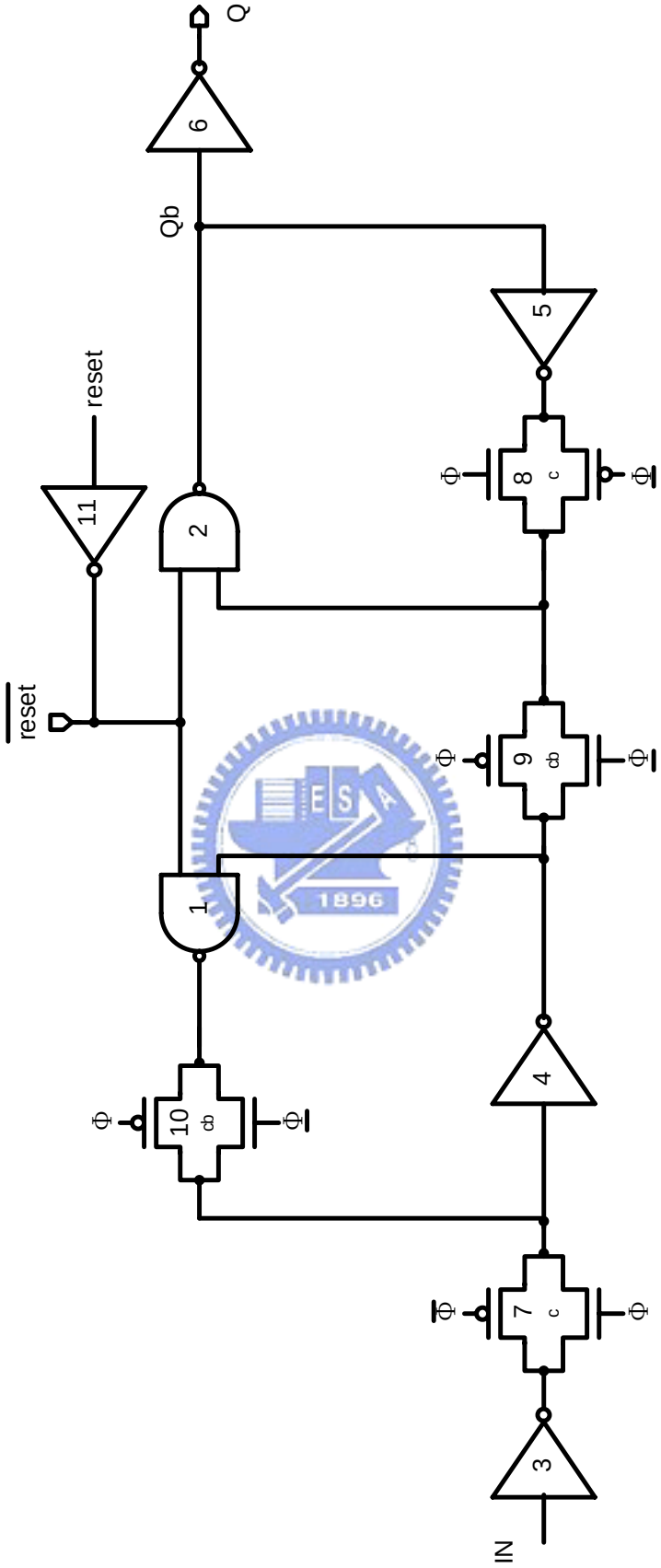


Fig 3-14 Resettable D-flipflop used in program counter and pulse swallow counter.

The prescaler consists of one dual modulus divide-by-4/5 and three divide-by-2 frequency dividers. There are several kinds of frequency divider which has been used for a long time, such as the TSPC flipflop or the SCL flipflop. In this design the TSPC flipflop and the SCL flipflop are both choused to form the prescaler, in order to save more power. Usually the TSPC flipflop can consumes less power than the SCL flipflop, but the TSPC flipflop does not work well at 2.4G-Hz in 1-V supply voltage. So, as shown in Fig 3-15, the first and second dividers use the SCL flipflop to achieve high speed operation. After the first two stages, the frequency is lower and the TSPC is suitable to be used.

The ÷4/5 frequency divider block diagram is shown in Fig 3-16. When G1 is low the it divide 4. When G1 is high, it divides 5.

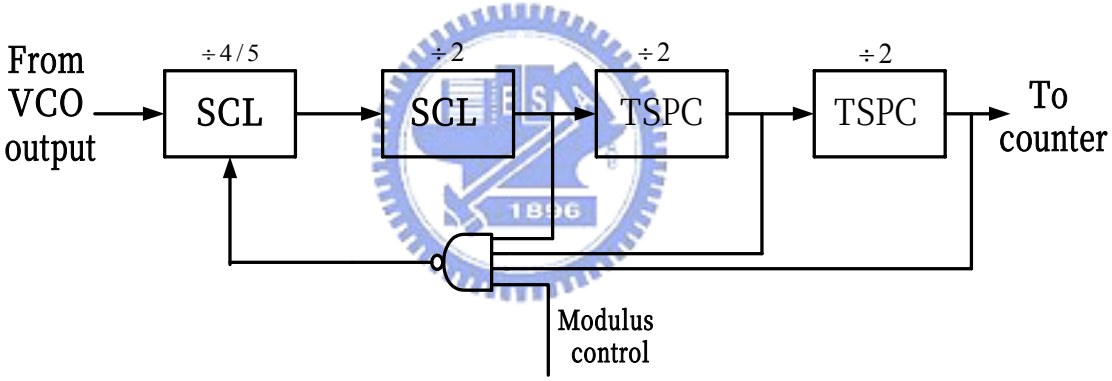


Fig 3-15 Dual modulus÷32/33 frequency divider block diagram.

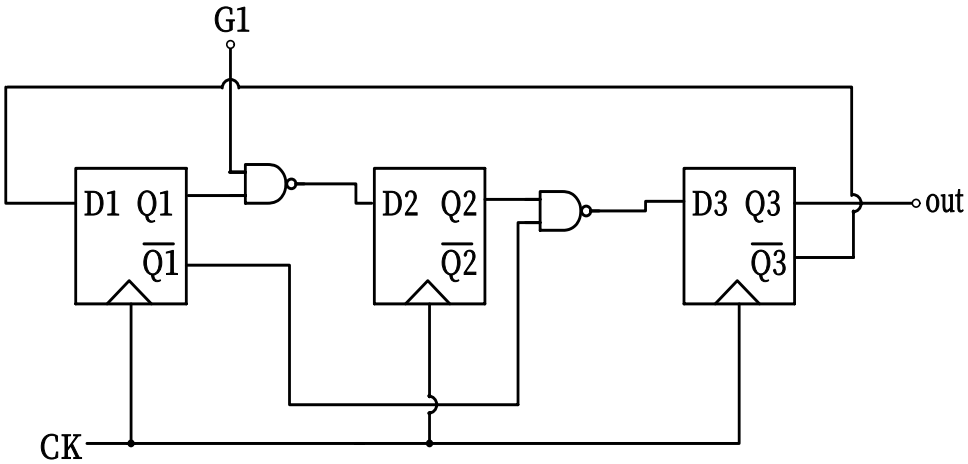
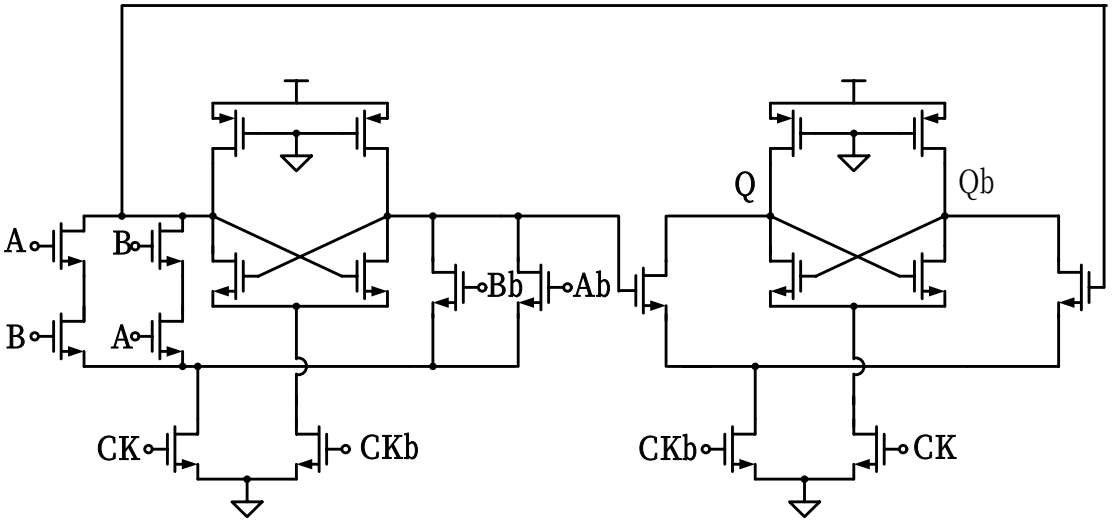
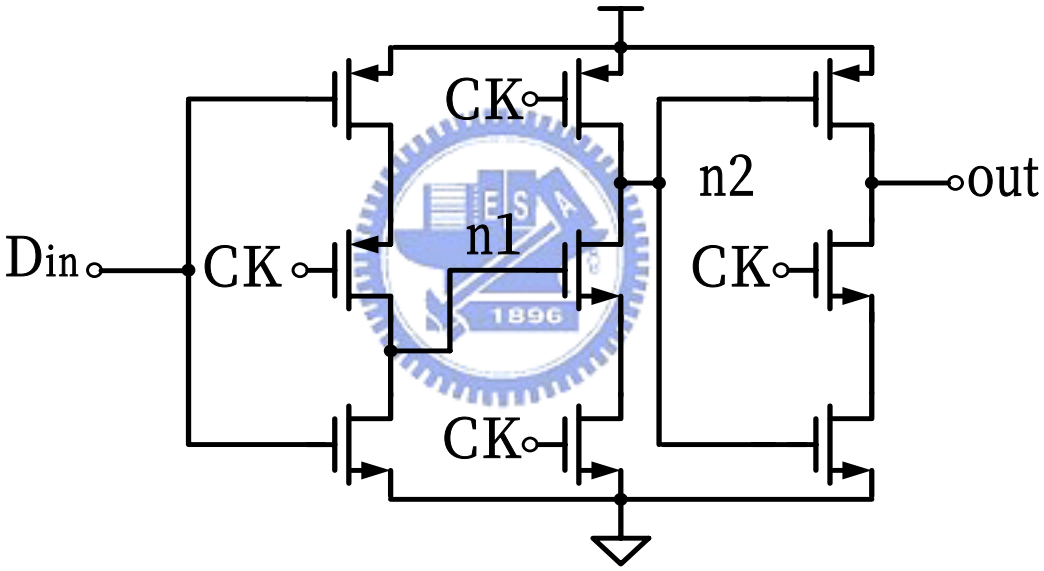


Fig 3-16 Dual modulus÷4/5 frequency divider block diagram.



(a)



(b)

Fig 3-17 (a) NAND-SCL flipflop used in the prescaler. (b) TSPC flipflop used in prescaler.

The TSPC and SCL D-flipflop circuits used in this design are shown in Fig 3-17. In order to work at 1 V supply voltage, the current source of the SCL D-flipflop is replaced. And the NAND gate uses the differential pair to form a stronger push-pull structure. By this structure, the input signals after pre-amp become larger. It makes the

cross-couple pair regeneration faster. The TSPC D-flipflops use 9 MOSFETs with pre-charge/pre-discharge topology to achieve high frequency operation and use only one phase clock. In these 9 MOSFETs, first column works as the master latch and the second and the third columns work as the slave latch.

When CK low, Din is stored at n1 and n2 is pre-charging. When CK high, n1 makes n2 to be n1_ and makes output=n2_. At this time CK will prevent Din to change n2 because:

If n2 is high, n1 will be low. If Din change from high to low, n1 still keep low with parasitic capacitance because CK is high.

If n2 is low, n1 will be high. If Din change from low to high, n1 will be discharge but n2 will not be changed but hold same state by parasitic capacitance.

This TSPC D-flipflop naturally output inverted input signal so that for a divide-2 circuit, it is simple to realize by connect out to D_{in} without an inverter. This makes critical path of this D-flipflop even shorter and can work at high frequency. But because of poor driving capability, inverter as a buffer is needed between these TSPC D-flipflop and increase delay but have no serious effects on division operation.

3.2.4 Phase and Frequency Detector

The block diagram of PFD which is used in this design is already shown in Fig 2-5 (a), and the clear circuit is shown in Fig 3-18. The logic gates G1, G2, G3 and G4 form a flip-flop as shown in Fig 2-5 (a), and G5, G6, G7, G8 form another flip-flop of the block diagram shown in Fig 2-5 (a). The transmission gates are used to balance the phase of the differential output. And the delay chain is used to reduce the dead zone of the PFD.

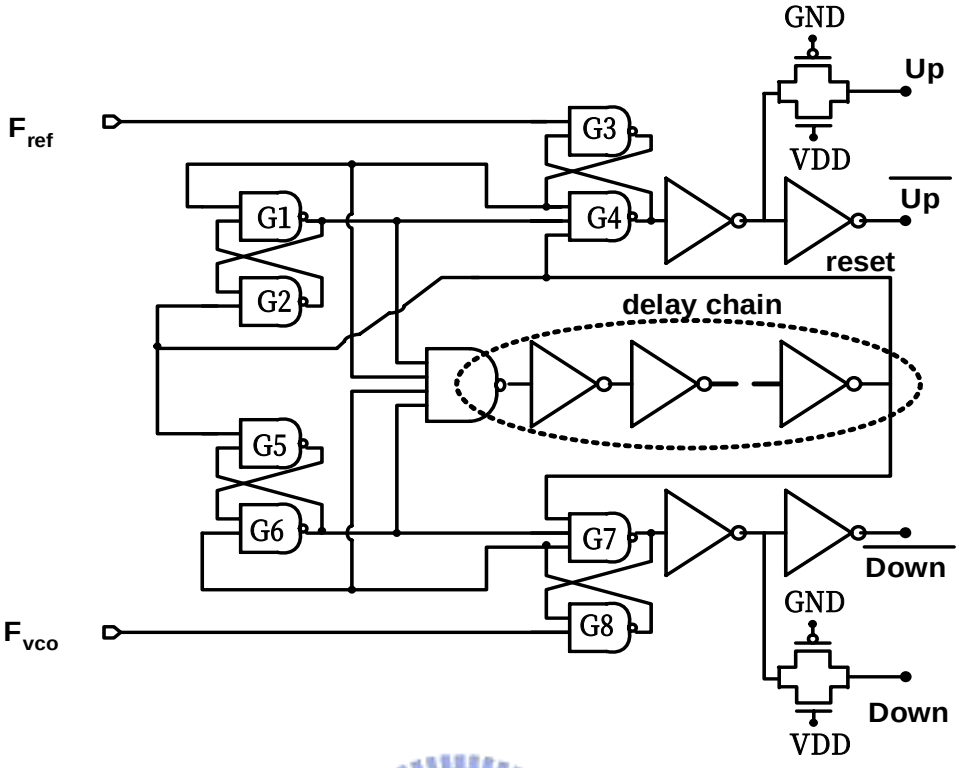


Fig 3-18 The circuit realization of the PFD.

Table 3-1 Parameter information of Fig 3-5

M8,M9,M11,M13,M19	20um/0.5um	M5,M16	20um/0.5um
M3,M4,M10,M12,M14	20um/0.4um	Mtail,M17	30um/0.5um
M1,M2,M15	5um/0.34um	M21,M22,M23	20um/0.5um
M6,M7,M18	5um/0.34um	Mref	10um/0.5um
M24	20um/0.5um	C1,C2,Cz,Rz	0.5p,0.5p,5p,7k

Table 3-2 Parameter information of Fig 3-8

M1,M2	40um/0.5um	Mtail	20um/0.5um
M3,M4	30um/0.5um		

3.3 Simulation Results

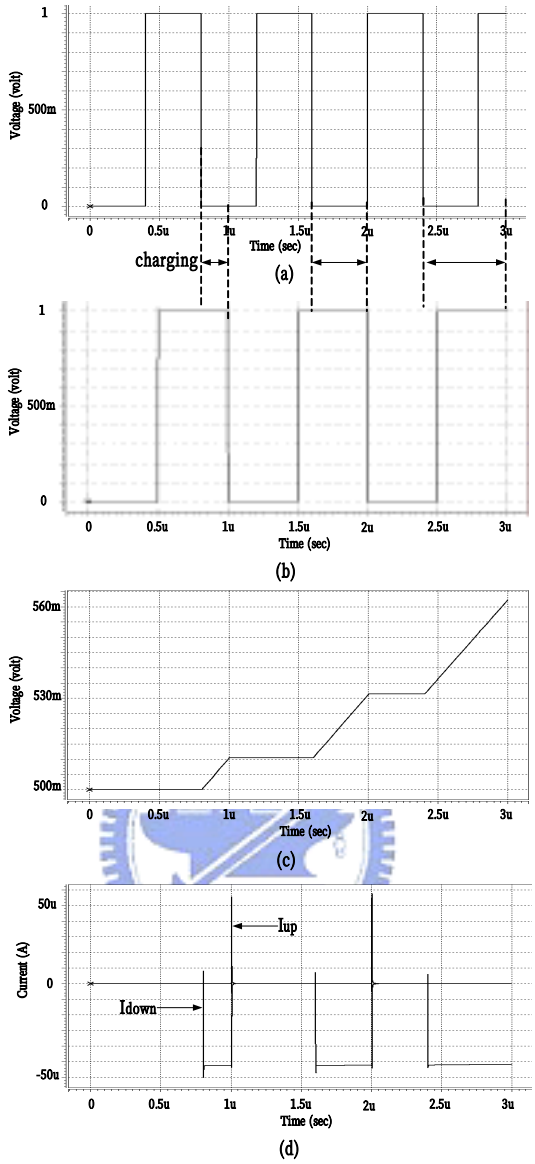


Fig 3-19 Charging simulation of charge pump (a) reference clock. (b) counter output. (c) the control voltage of VCO. (d) I_{up} and I_{down} of the charge pump.

In the Fig 3-19, the charge pump is in charging mode. In Fig 3-19 (a) and (b), we can find that the phase of the reference clock goes beyond the counter output and the frequency is higher than the counter output. So, the charge pump charges between the clock falling edges of the reference clock and output of counter. So, the control voltage is getting higher.

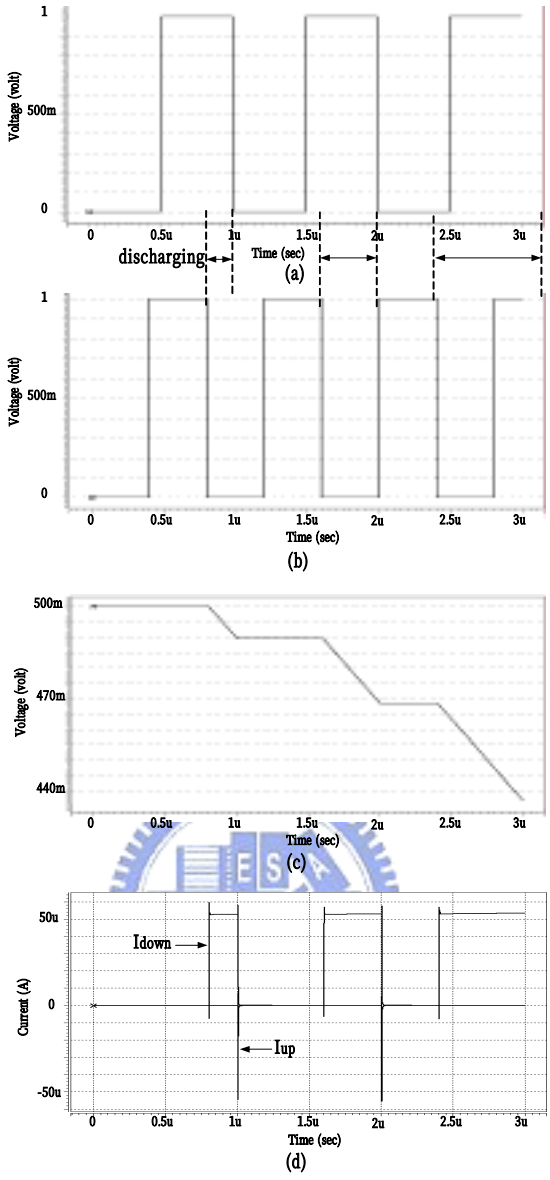


Fig 3-20 Discharging simulation of charge pump (a) reference clock. (b) counter output. (c) the control voltage of VCO. (d) I_{up} and I_{down} of charge pump

In the Fig 3-20, the charge pump is in discharging mode. In Fig 3-20 (a) and (b), we can find that the phase of the reference clock goes behind the counter output and the frequency is lower than the counter output. So, the charge pump discharges between the clock falling edges of the reference clock and counter output. So, the control voltage is getting lower.

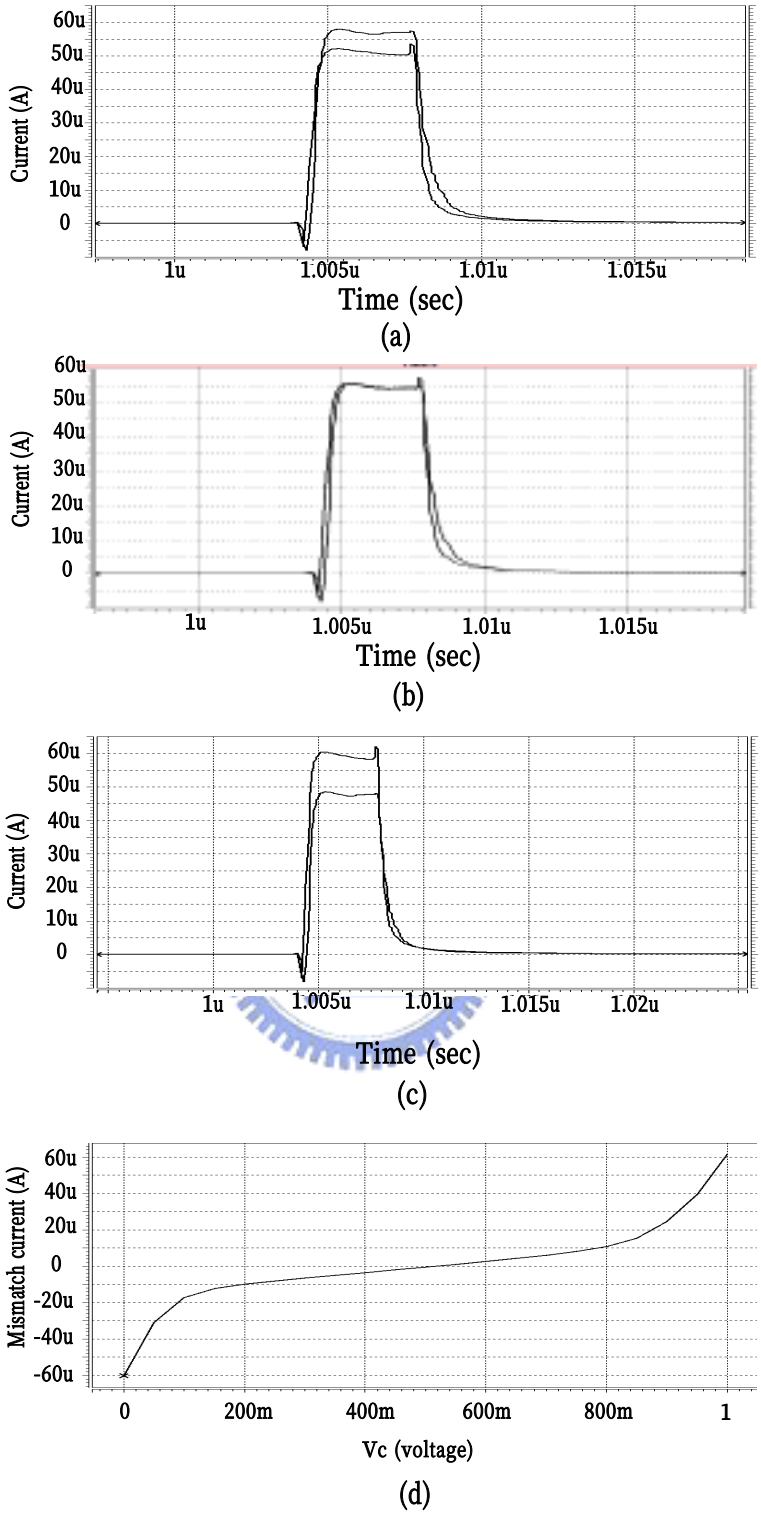


Fig 3-21 Simulation results of the current-steering charge pump without current-match structure (a) The I_{up} and I_{down} at V_c=0.3V (b) The I_{up} and I_{down} at V_c=0.5V (c) The I_{up} and I_{down} at V_c=0.8V (d) The mismatch current v.s. $V_{control}$

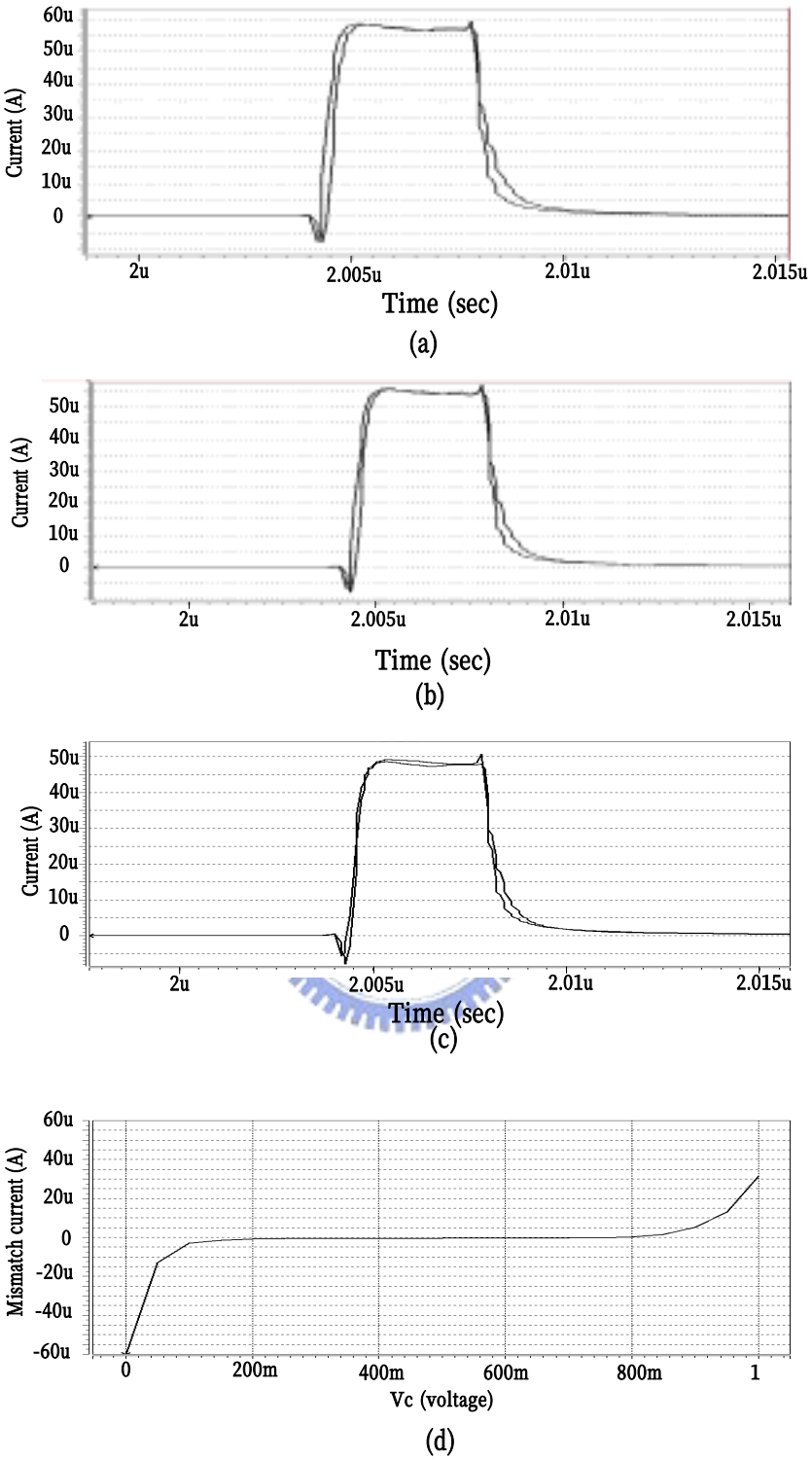


Fig 3-22 Simulation results of the new current-match charge pump (a) The I_{up} and I_{down} at V_c=0.3V (b) The I_{up} and I_{down} at V_c=0.5V (c) The I_{up} and I_{down} at V_c=0.8V (d) The mismatch current v.s. $V_{control}$.

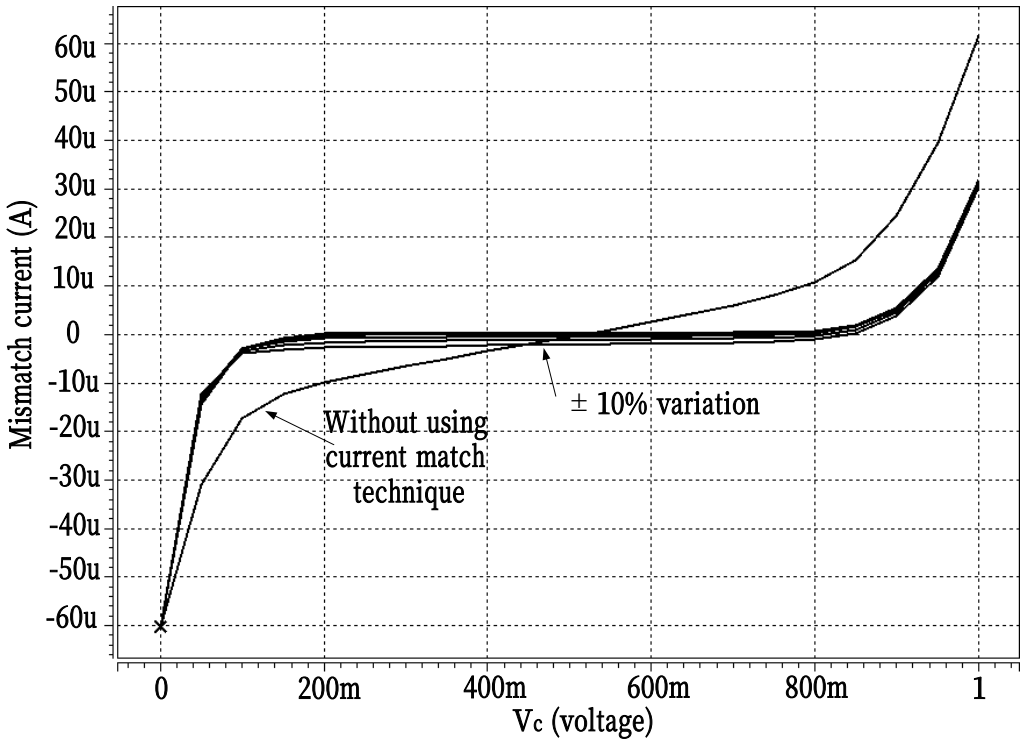
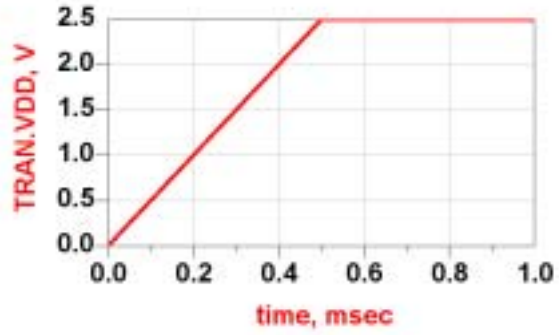


Fig 3-23 The mismatch current simulations of charge pump with process variation, and compare the results with the charge pump without feedback loop.

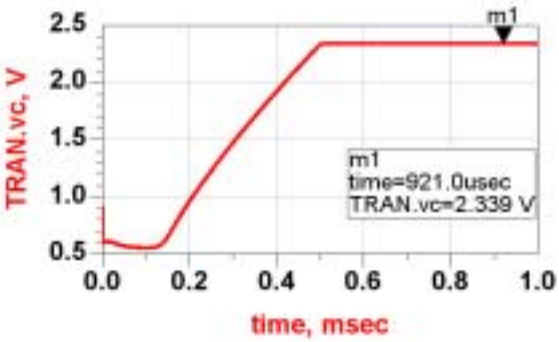
The current-steering charge pump without feedback loop is simulated in Fig 3-21. (a) to (c) shows I_{up} and I_{down} at different V_c and we can find that the I_{up} and I_{down} just match at V_c=0.5V. (d) shows the mismatch current at different V_c. The maxim difference between I_{up} and I_{down} is about 20% of the charge pump current.

The current-match charge pump which used in this design is simulated in Fig 3-22. (a) to (c) shows I_{up} and I_{down} at different V_c and we can find that when the Vc varies, I_{up} and I_{down} still match to each other. (d) shows the mismatch current at different V_c and the maxim difference between I_{up} and I_{down} is about 1.5% of the charge pump current.

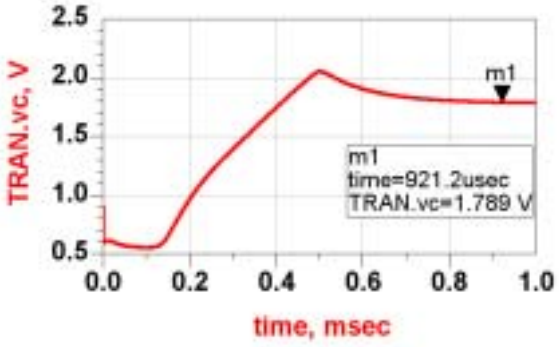
Fig 3-23 shows the process variation impact of the current-match charge pump. We can find that even if the variation up to 10%, the mismatch current is smaller than witch without feed back loop.



(a)



(b)



(c)

Fig 3-24 The start-up simulation results of the current-match charge pump at 2.5-V power supply (a) The VDD grows up with 0.5-msec (b) The V_c with the circuit in Fig 3-1 is pulled up to near the VDD (c) the V_c with the modified structure in Fig 3-3 does not be pulled up.

The start-up simulation is shown in Fig 3-24. In this figure we can find that the circuit which shown in Fig 3-3 is successfully solve the start-up problem. It is proofed in 2.5 V power supply and it also be solved in 1 V power supply.

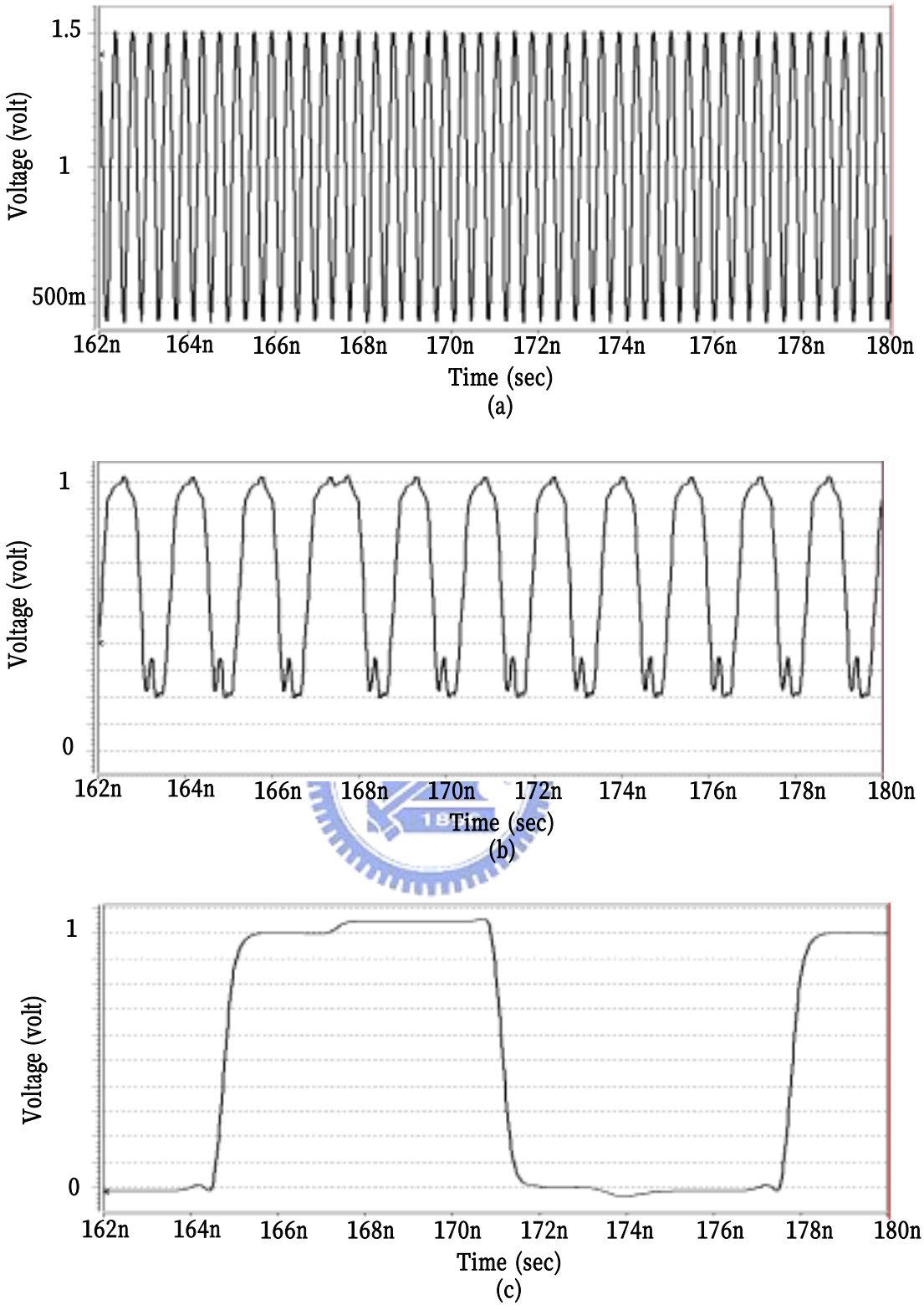


Fig 3-25 Simulation results of the VCO and the ÷32/33 prescaler (a) the output waveform of VCO (b) the output waveform of the ÷4/5 dual modulus frequency divider (c) the output waveform of the ÷32/33 prescaler

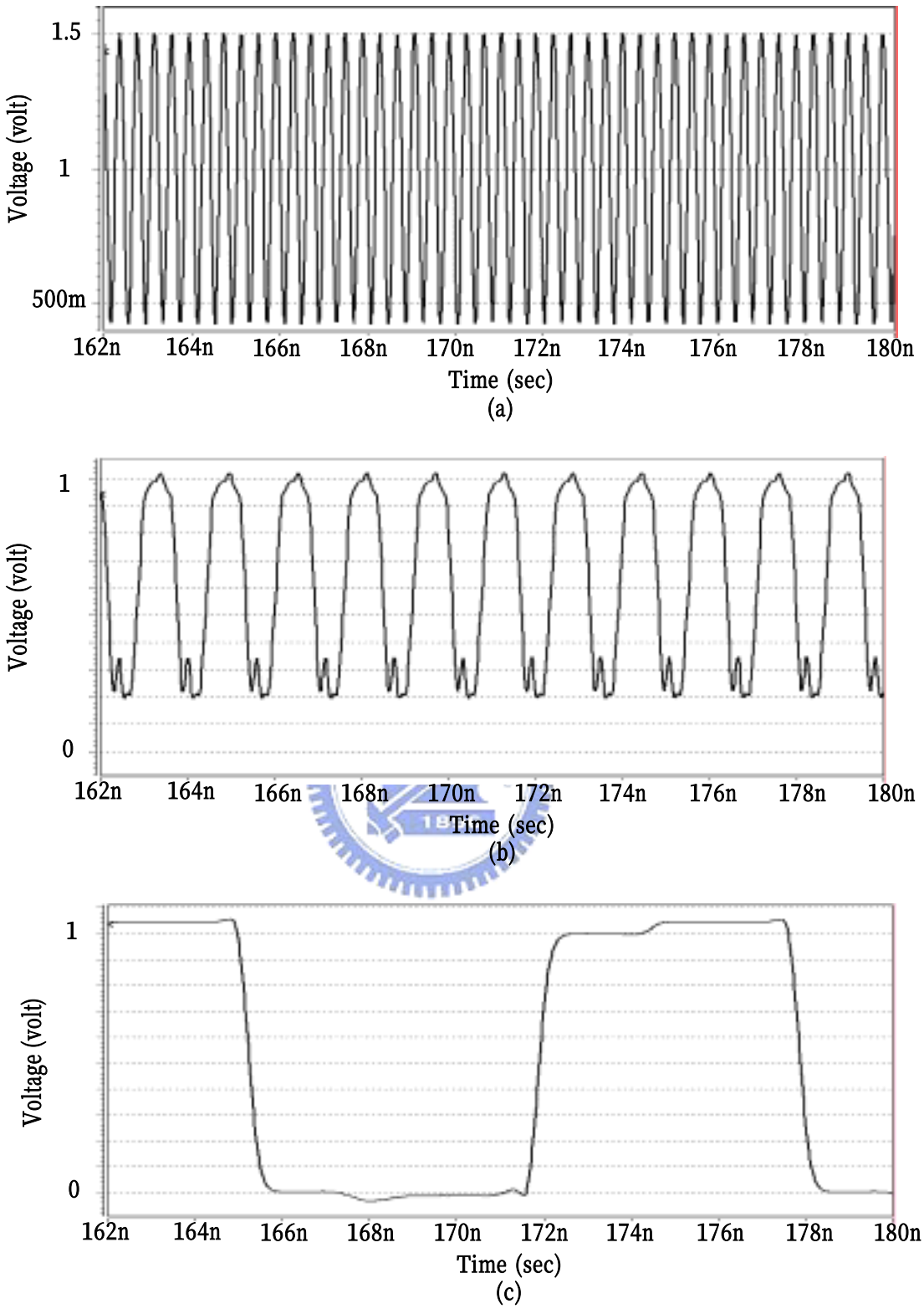


Fig 3-26 Simulation results of the VCO and the ÷32/33 prescaler (a) the output waveform of VCO (b) the output waveform of the ÷4/5 dual modulus frequency divider (c) the output waveform of the ÷32/33 prescaler

The simulation results of prescaler are shown in Fig 3-25 and Fig 3-26. In Fig 3-25 the prescaler is dividing 33. So, we can find that the $\div 4/5$ dual modulus frequency divider changes the modulus from 4 to 5 every eight clocks again. By this way, it provides the output of the prescaler has a period of 33 times of the VCO output. In the Fig 3-26, the prescaler is dividing 32. In this modulus the $\div 4/5$ dual modulus frequency divider is always dividing 4. So, the output waveform of the prescaler has a period 32 times of the VCO output.

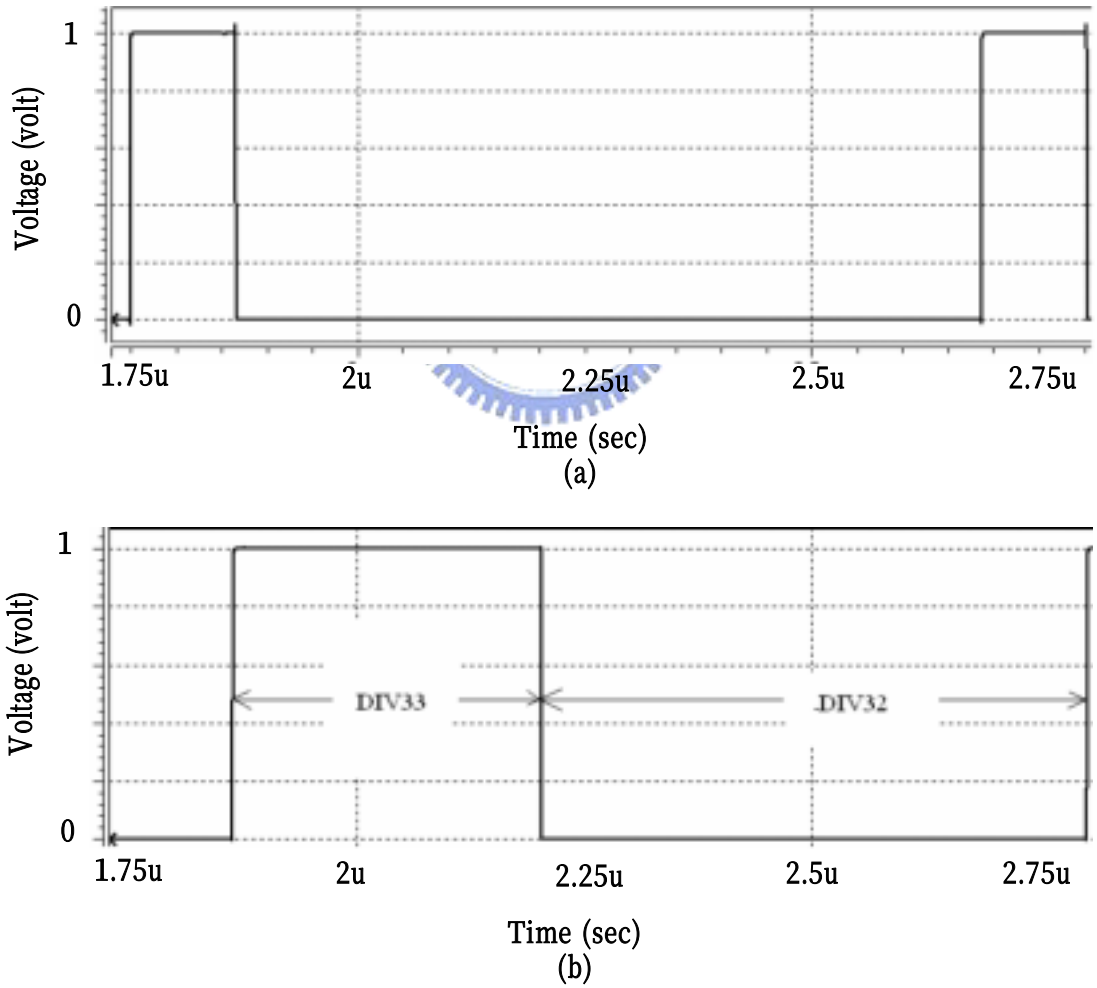
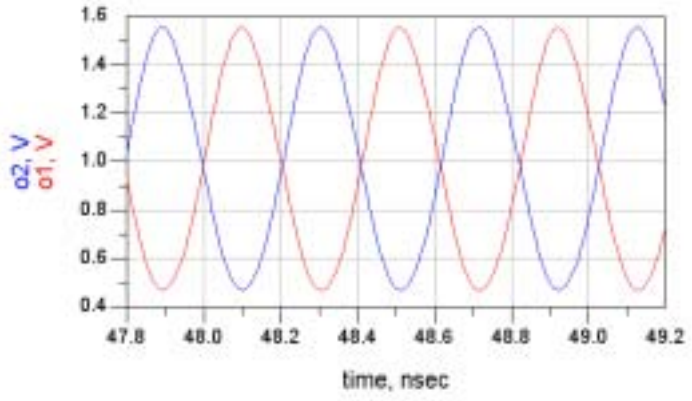


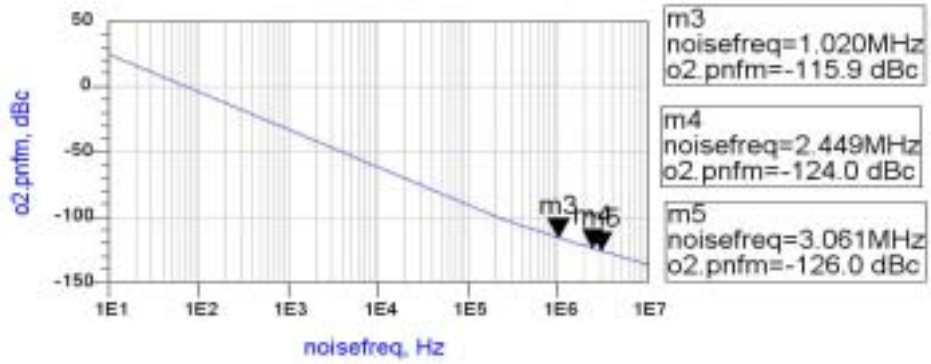
Fig 3-27 The simulation results of pulse swallow counter (a) The output waveform of the programmable counter (b) The output waveform of the swallow counter.

The simulation results of programmable counter and swallow counter are shown in Fig 3-27. As shown in (b) the swallow counter initially output high and controls the prescaler dividing 33. When the swallow counter is overflow, the output of swallow counter changes to low and it control the prescaler dividing 32.

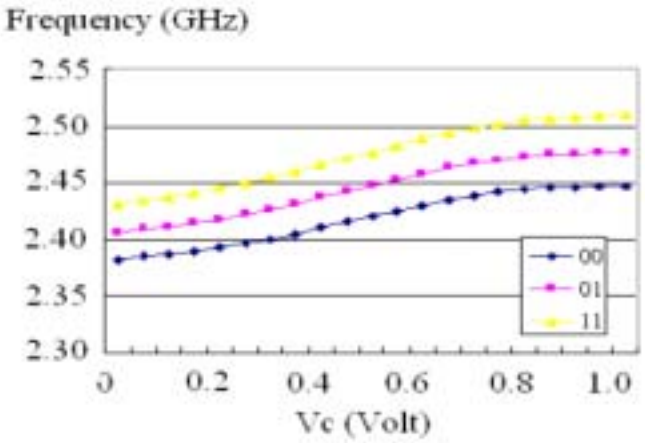
The simulation results of the VCO are shown in Fig 3-28. The differential output waveforms of VCO are shown in (a) and the peak-to-peak amplitude is 1-V. The phase noise of VCO is simulated by ADS and is shown in (b). In (b) we can find that the phase noise at offsets frequencies 1-MHz, 2.5-MHz and 3-MHz are -115.9-dBc, -124-dBc and -126-dBc. This performance is suitable for Bluetooth application. The tuning range of the 2-bits VCO is shown in (c). As mentioned in 3.2.2.2, the 2-bits band-switching VCO uses varactor as the bank and split the tuning range into three bands as show in (c). When the control word of bank is 00, the bank has the maximum capacitance. So, the VCO has the minimum frequency band. On the contrary, when the control word is 11, the VCO changes the frequency band to the maximum frequency band. Beside, when the control word changes to 10 or 01, the frequency band of VCO changes to the middle band.



(a)



(b)



(c)

Fig 3-28 The simulation results of the band-switching VCO (a) The output waveform of the VCO (b) The phase noise simulation results by ADS (c) The tuning ranges of the three bands simulation.

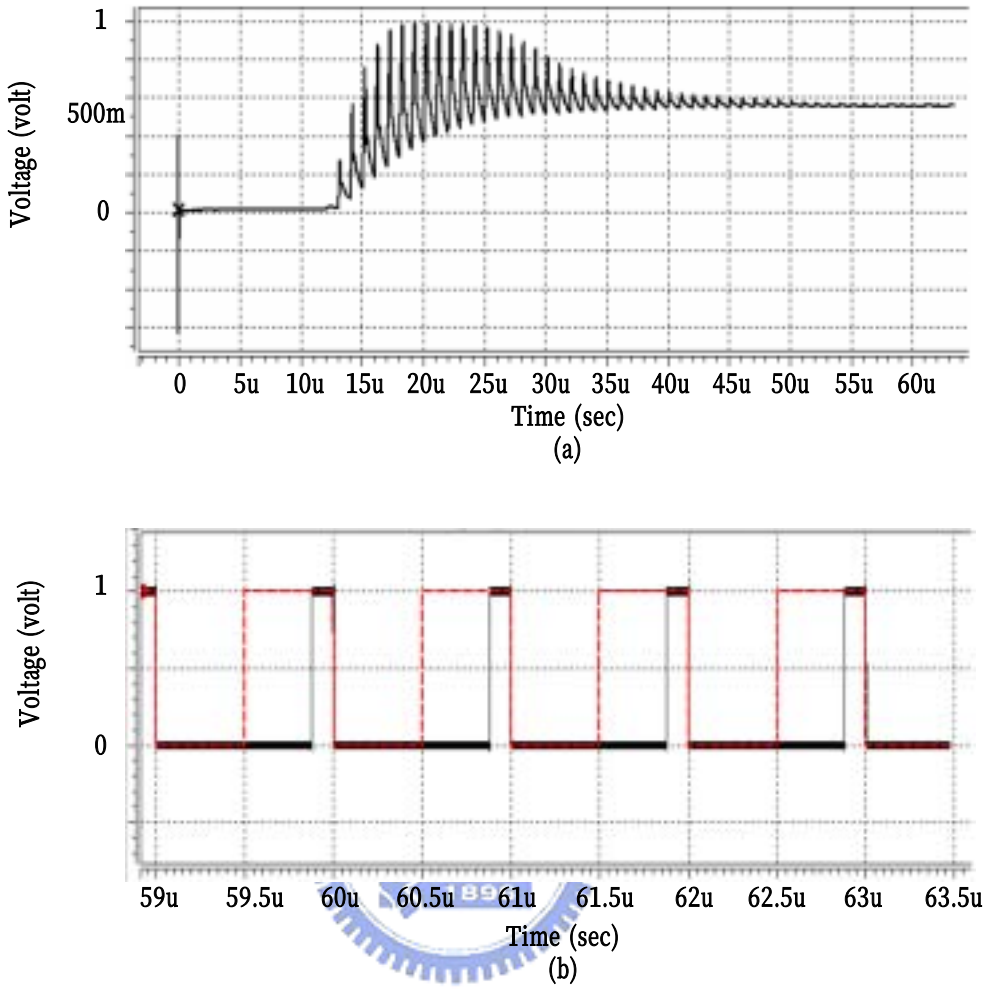


Fig 3-29 The close loop simulation of the PLL (a) The control voltage of VCO (b) The reference clock and the output waveform of counter

The close loop simulation of the frequency is shown in Fig 3-29. The V_c which controls VCO is shown in (a) and we can find that it is locked within 60 usec. Fig 28 (b) shows the reference clock and the output waveform of counter. We can find that the edges of reference clock and output of counter match to each other. This means that the frequency synthesizer is locked.

Table 3-3 Simulation summary

	Post-sim
Supply voltage	1 V
Frequency range	2.4~2.48 GHz
Reference clock	1 MHz
Power consuming	13 mW
K_{VCO} (VCO Gain)	100~120MHz/V
Phase noise (using ADS)	-115.9 dBc/Hz @1MHz offset -115.9 dBc/Hz @1MHz offset -115.9 dBc/Hz @1MHz offset
Charge pump current mismatch (I_D=50uA)	Maximum 1.5% when Vc from 0.2 V~0.8 V
Loop bandwith	50 kHz
Close loop PM	65°
settling time	60 us

CHAPTER 4

MEASUREMENT RESULTS

This section, the measurement results are presented. The spurious tones -64.97 dBc @ 1 MHz offset is achieved. The tuning range of VCO decreases about 20% which be compared with simulation and the Kvco is about half of the simulation. The phase noise is -111.14 dBc/Hz @ 1MHz offset is achieved. The power consumption is 23 mW.

This work is fabricated using 0.25 um 1-poly 5-metal standard CMOS process. Fig 4-1 shows the die micrograph of the complete frequency synthesizer.

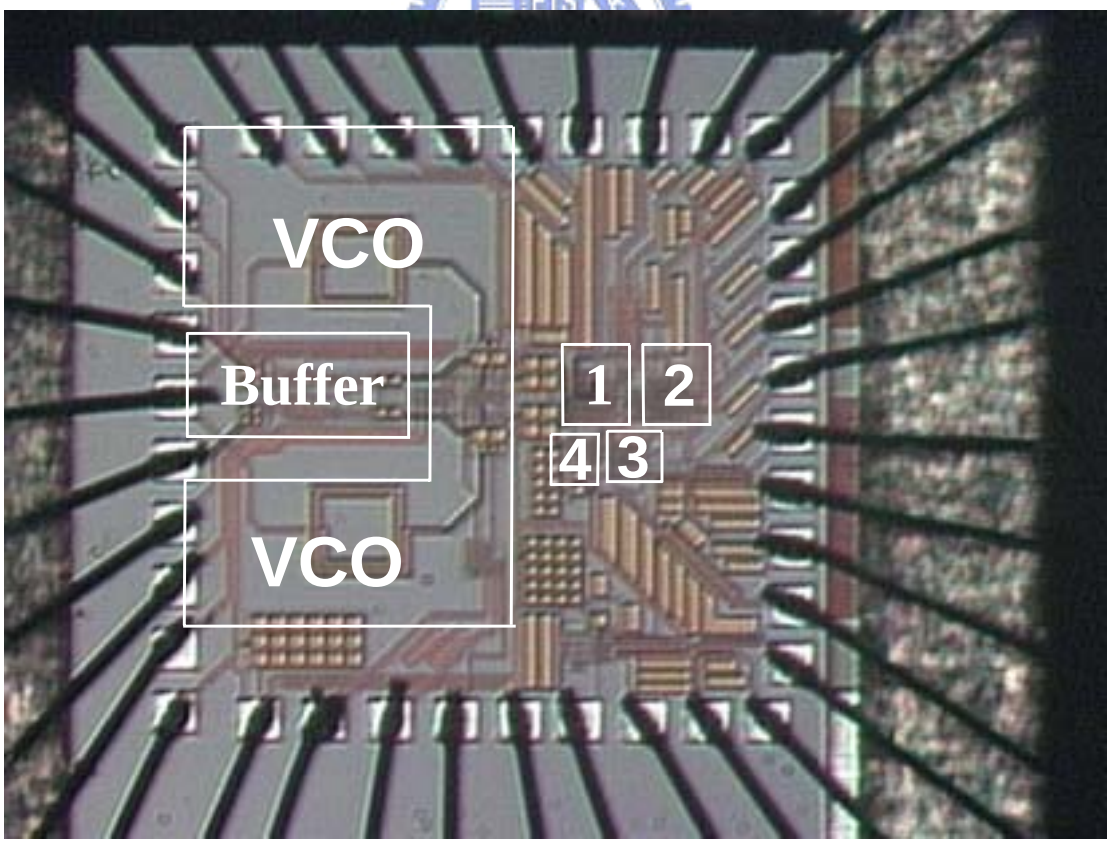


Fig 4-1 Chip micrograph of the complete frequency synthesizer; 1 is the prescaler, 2 is counter 3, is PFD and 4 is charge pump

4.1 MEASUREMENT RESULTS OF THE BAND-SWITCHING VCO

The measurement results of the band -switching VCO are shown in Fig 4-2. The measurement results shows that the frequency range shift up about 65 MHz and the tuning range is smaller than simulation.

After adjusting V_{C3} and $V_{varactor}$ (Fig3-11), the tuning ranges are shown in Fig 4-3. The K_{VCO} is calculated for every 0.1 V step of the control voltage and the K_{VCO} of the tuning range is from 40 MHz/V to 50 MHz/V.

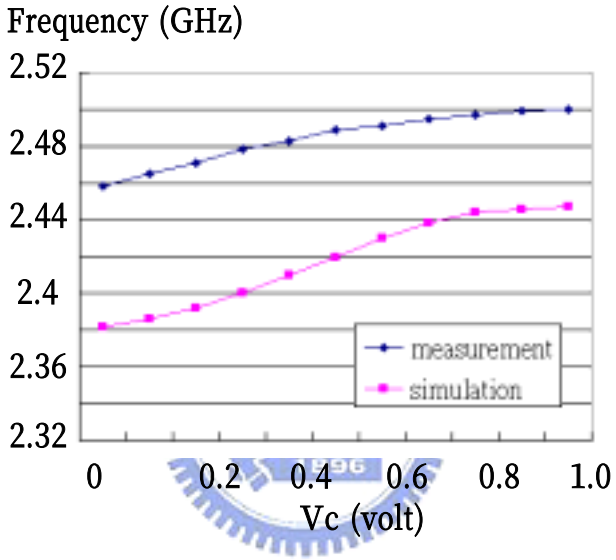


Fig 4-2 Comparison of measurement result and simulation result. The tuning range is for Vc1Vc2=00.

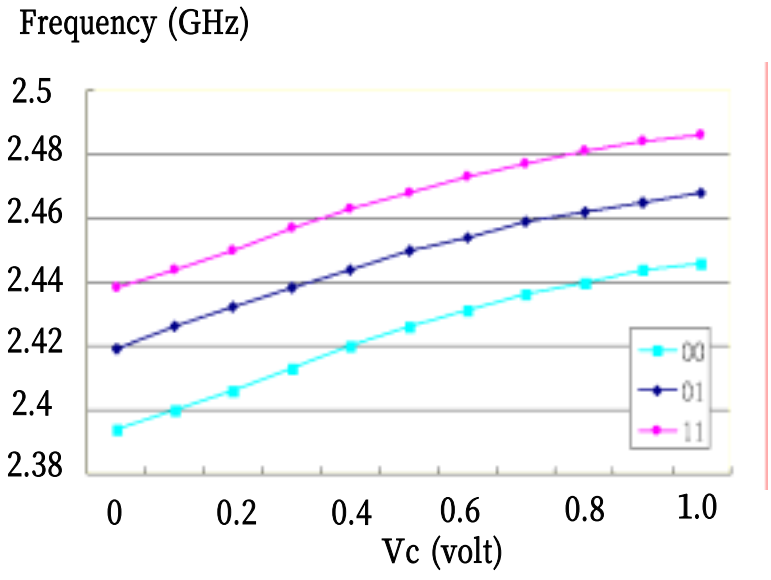


Fig 4-3 Tuning ranges of the band-witching VCO after adjust the bias nodes.

4.2 MEASUREMENT RESULTS OF THE 2.4 GHZ FREQUENCY SYNTHESIZER

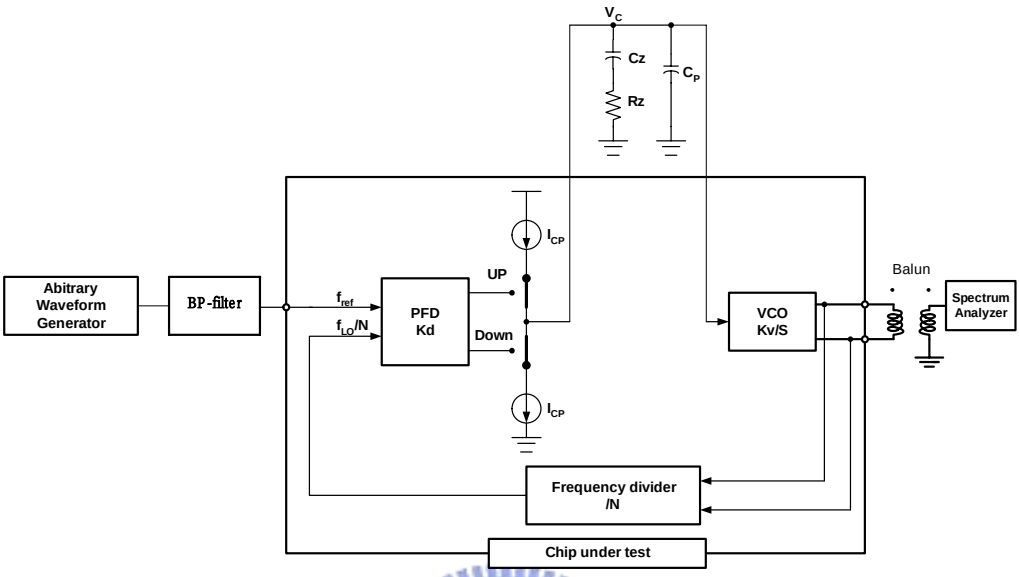


Fig 4-4 Measurement setup of the frequency synthesizer. Additional loop filter, clock generator and band-pass filter are used. Reference clock is 1 MHz.

The measurement setup of the 2.4 GHz frequency synthesizer is shown in Fig 4-4. The external loop filter and reference clock are used. The reference clock is generated by an AWG (arbitrary waveform generator) and a band-pass filter (center 1 MHz).

The measurement setup of VCO is shown in Fig 4-5. When the frequency is shift, Vc3 can be used to compensate. $V_{varactor}$ is used to make the linear range in the voltage range of charge pump output. Unfortunately, those two nodes strongly increase spur level. As shown in Fig 4-6, without by-pass capacitors in Fig 4-5 the spur level is -29dBc @ 1MHz offset. As shown in Fig 4-7, by using by-pass capacitors the spur level is decreased to -48dBc @ 1MHz offset. Finally, using the batteries as the power supply and bias for analog circuits makes the spur level be decreased to -64.97dBc @ 1MHz offset. As shown in Fig 4-8, the spur level is decreased to -64.97dBc @ 1MHz offset.

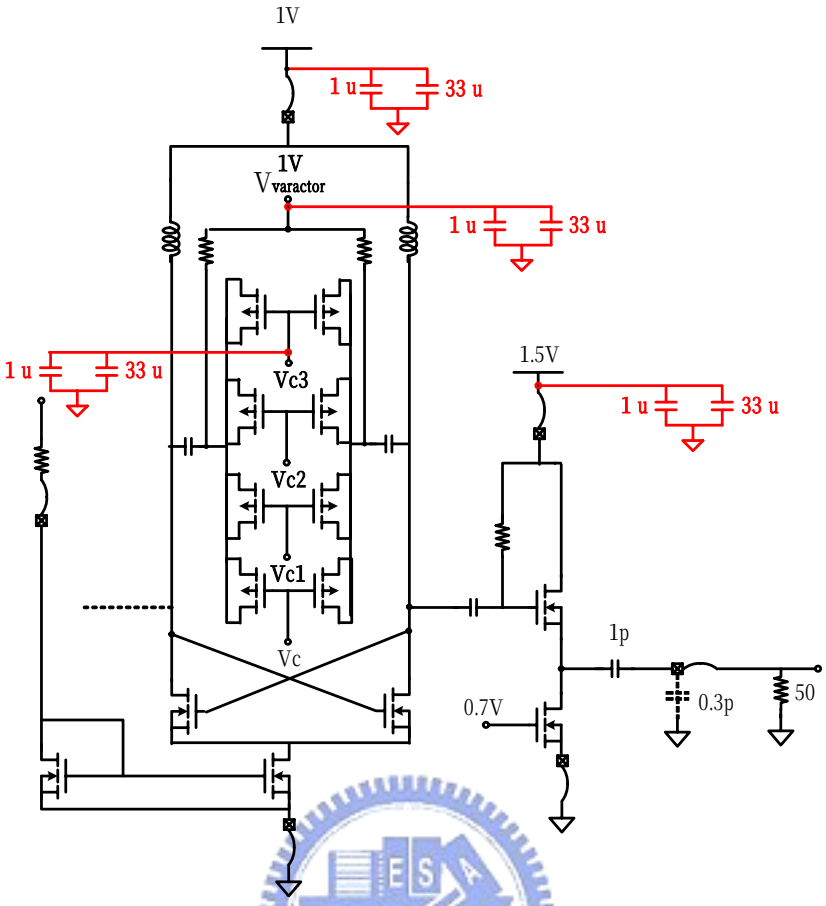


Fig 4-5 Measurement setup. Adding by-pass capacitors to reduce the spur level.

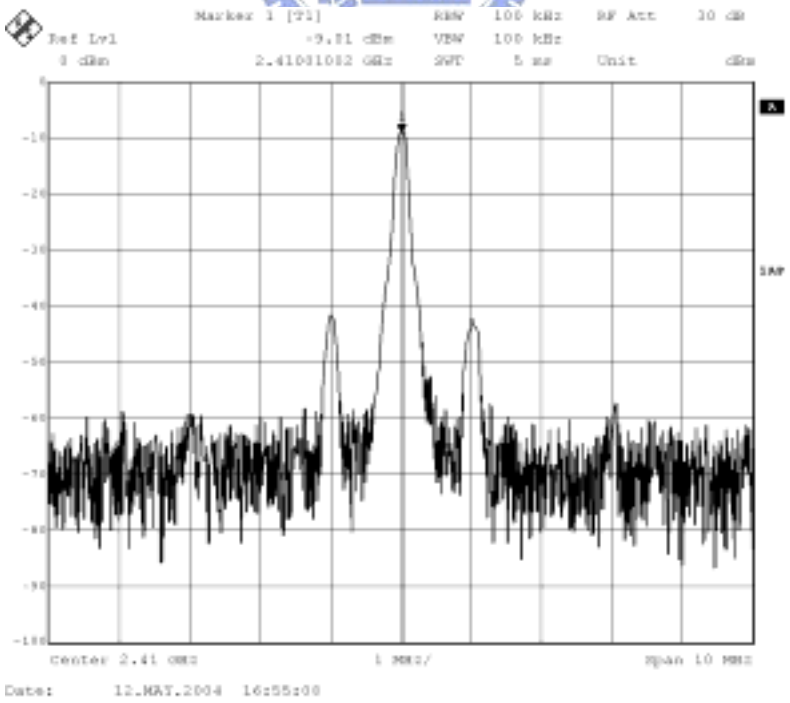


Fig 4-6 Without using by-pass capacitors the spur level is -29dBc @ 1MHz offset.

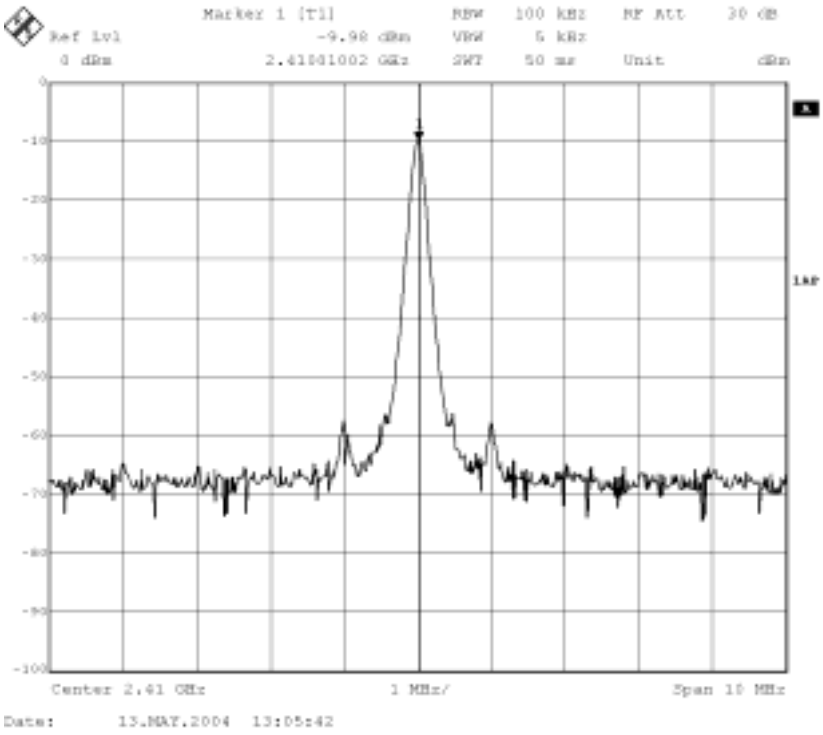


Fig 4-7 By using by-pass capacitors helps the spur level decreased to -48dBc @ 1MHz offset.

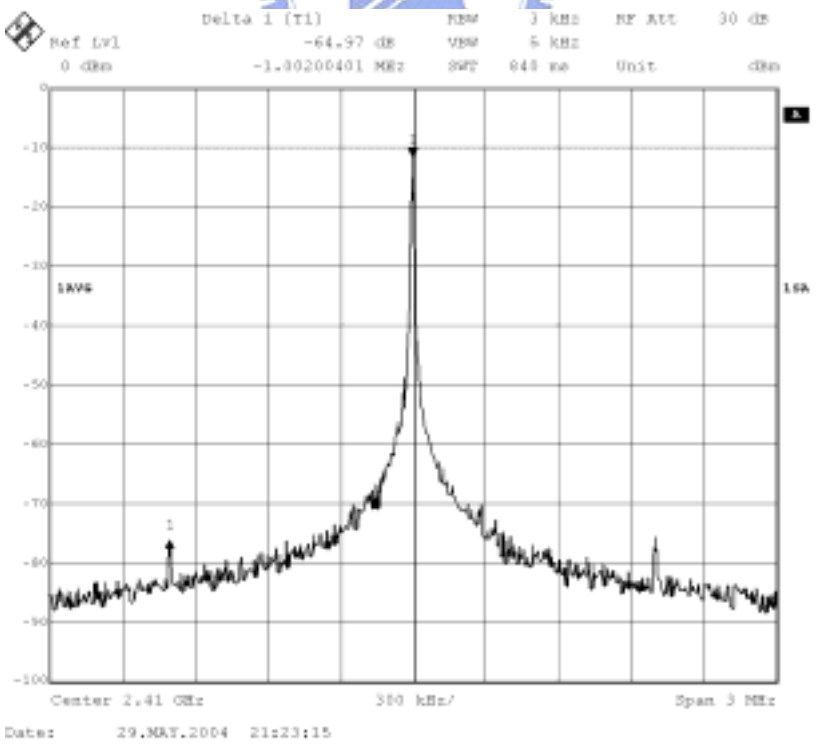


Fig 4-8 Using by-pass capacitors to filter the noise and using battery to get more clear bias and supply voltage, the spur level is decreased to -64.97dBc @ 1MHz offset.

Fig 4-9 and Fig 4-10 show the testing modules of the 2.4 GHz frequency synthesizer. In this work, we use chip on board testing. Fig 4-9 shows the signal board and Fig 4-10 shows the DC board. In Fig 4-9, we can see the by-pass capacitors used to filter the noise and in Fig 4-10, we can see the battery boxes used to provide clear bias and power supply for analog circuits.

Fig 4-9 The testing signal board.

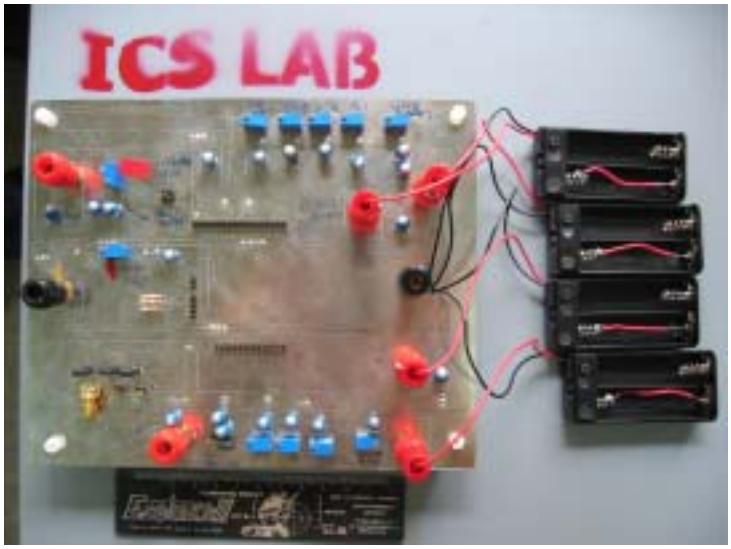


Fig 4-10 The testing DC board

The phase noise measurement result is shown in Fig 4-11. We can find that the phase noise at 1MHz offset is -111.14dBc/Hz. Fig 4-12 shows the prescaler output waveform measurement result through a tapping buffer. Fig 4-13 shows the settling measurement results, the settling time is about 70 us (using the Tek P6139A active voltage probe, 500 MHz, 8 pF, 10 MΩ). Because of the small load of the probe, the settling time is a little large than simulation result.

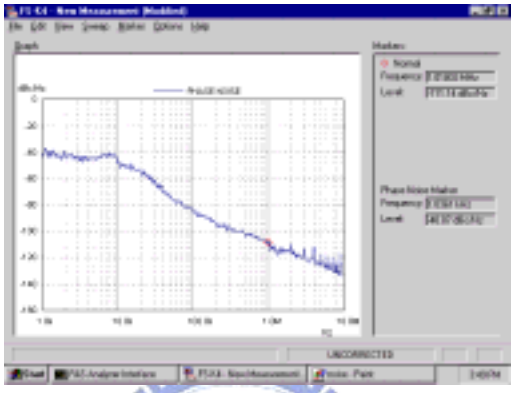


Fig 4-11 Phase noise measurement result, -111.14 dBc/Hz at 1MHz offset

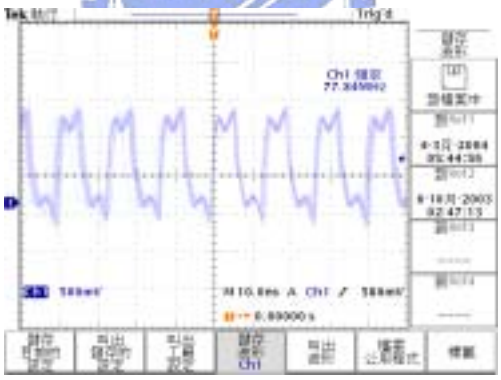


Fig 4-12 The presacler measurement through tapping buffer.

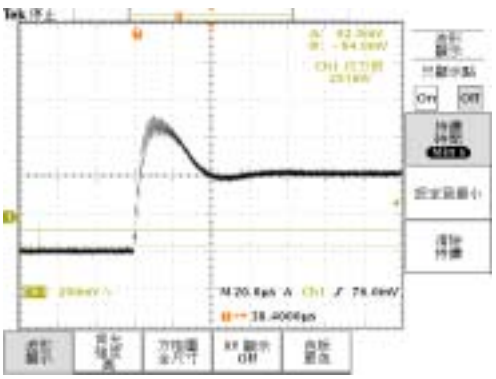


Fig 4-13 Settling time testing, the srttling is about 70 us.

Table 4-1 Measurement summary

		Post-sim	Measurement
VDD	VCO	1 V	1.3 V
	Digital	1 V	1.2 V
	Charge pump	1 V	1 V
current	VCO	3 mA	10 mA
	Digital	9.5 mA	8 mA
	Charge pump	0.4 mA	0.7mA
Total power		13 mW	23.2 mW
Spur level @ 1MHz offset		N.A	-64.97 dBc
Phase noise		-115 dBc/Hz @1MHz offset	-111.14 dBc/Hz @ 1MHz offset
$V_{varactor}$		1 V	1.2 V
V_{c3}		0.5 V	0.7 V
K_{VCO}		100~120MHz	40~50 MHz
Loop bandwidth		50 kHz	35 kHz
I_D(charge pump current)		50 uA	80 uA
Settling time		60 us	70 us
Loop filter	R_p	134 k	150 k
	C_p	107 p	100 p
	C_2	5.5 p	10 p

4.3 COMPARISON

Table 4-2 Comparison

	This work	[5]	[6]
Technology	0.25 um	0.25 um	0.25 um
Kvco(VCO Gain)	50 MHz	120 MHz	345 MHz
Loop bandwidth	35 kHz	50 kHz	60 kHz
Spur level	-64.97dBc @ 1MHz offset	-70.88dBc @ 1MHz offset	-65.88dBc @ 1MHz offset
VDD	1.3 V	2.2 V	2.5 V
Total power	23 mW	34 mW	33 mW

4.4 DISCUSSION

4.4.1 Discussion 1

In measurement when the VCO uses the same bias setup as simulation, the prescaler does not wok well. The dividing modulus is not correct. After we increase the VDD and tail current of VCO and the prescaler VDD (shown in table 4-1), the prescaler correctly work.

According to this result, we re-simulate the VCO with the parasitic resister as shown in Fig 4-14. Those values of resisters are calculated by using technology documents. The amplitude drops from 1 V to 0.415 V as shown in Fig 4-15 (a). At this situation the prescaler can not work well. In Fig 4-15 (b), the VCO is re-designed by increasing 1.4 times size parameter of the cross couple pair and increase the tail current to 6.2 mA. With those changes the amplitude of the VCO with the parasitic resistor is increased to 1.08 V.

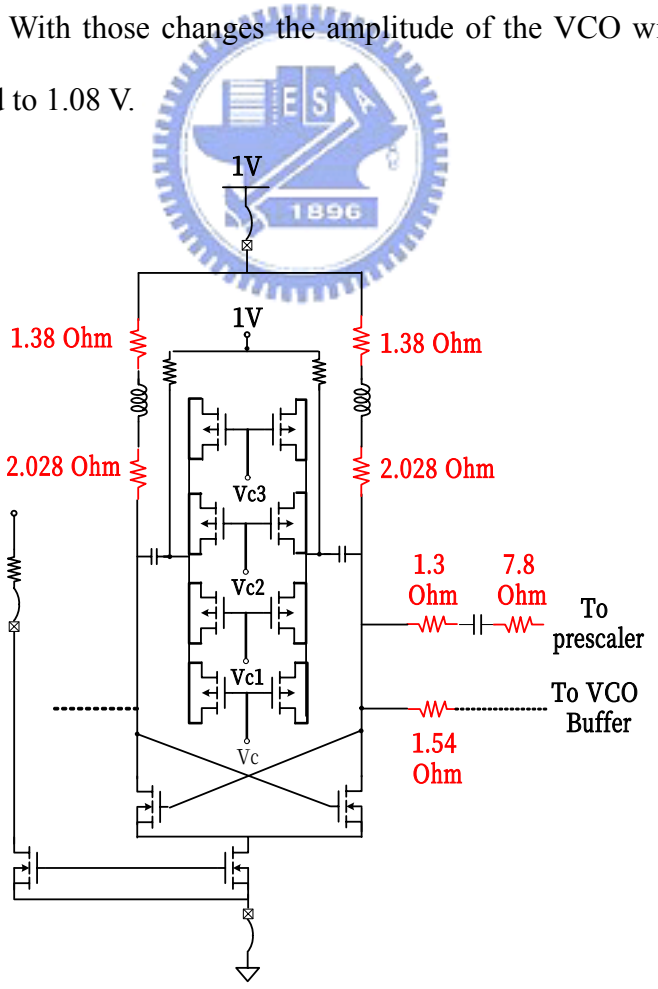
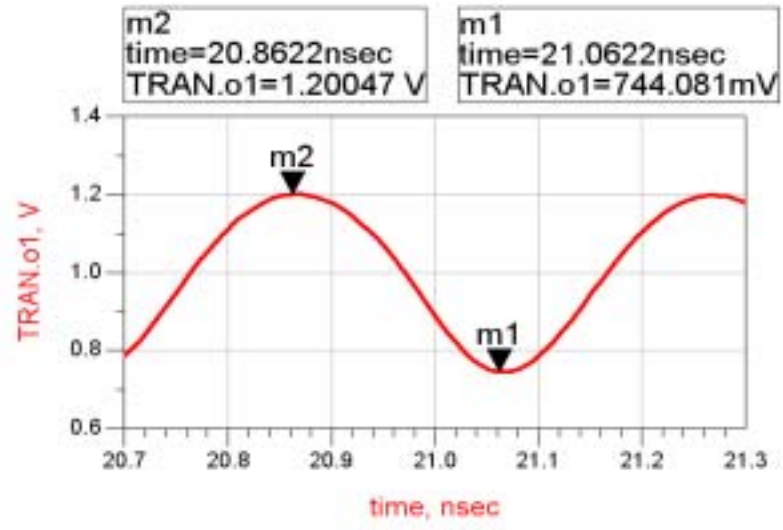
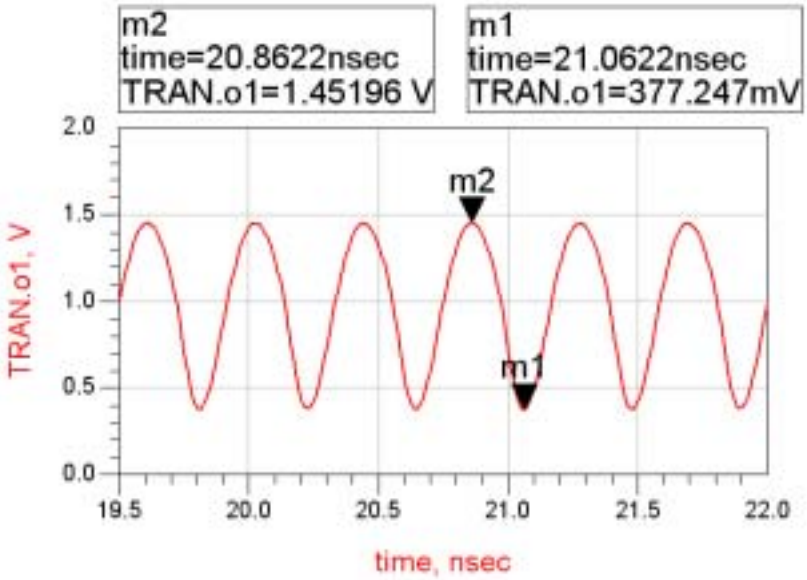


Fig 4-14 The parasitic resisters of metal line in layout.



(a) VCO simulation with parasitic resistor, the amplitude is decreased to 0.415 V.



(b) Re-design the VCO to increase the amplitude to 1.018 V.

Fig 4-15 VCO re-simulation and re-design with parasitic resistor.

Table 4-3 Comparison of re-simulation and re-design with parasitic resistors

	Re-simulation	Re-design
$V_{peak\text{-}to\text{-}peak}$	0.415 V	1018 V
Tail current	3 mA	6.02 mA
Cross couple pair size	1	1.4

4.4.2 Discussion 2

The supply voltage of the prescaler must be increase to 1.2 V in measurement. A reasonable reason is found. It is because the large current of prescaler and the long power lines of VDD and ground of prescaler. As shown in Fig 4-16, there are a 7 ohm parasitic resistor from real VDD to the prescaler VDD and an 8 ohm resistor from real ground to prescaler ground. The voltage drop on those resistors is 120 mV and this is a reason why the VDD must be increase in measurement.

Increasing the power line width of prescaler to five-times and using metal-5 as the power line can reduce the parasitic resister to 1/10. In re-simulation, if the parasitic resister is 1/10 of original, the prescaler can operate in 1 V supply voltage.

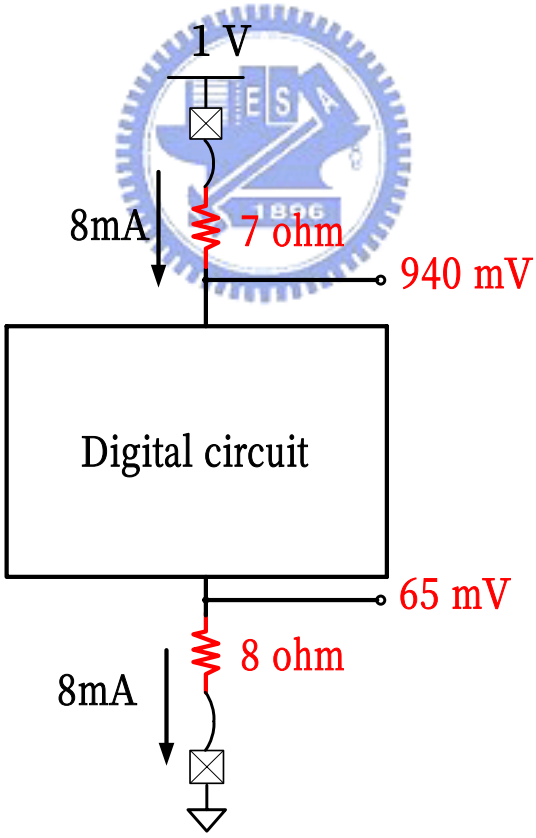
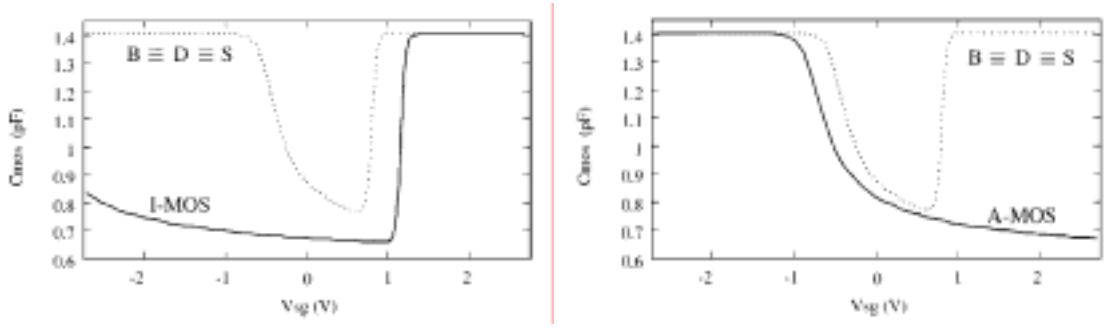


Fig 4-16 Parasic resistors of prescaler VDD and ground

4.4.3 Discussion 3



(a) (b)

Fig 4-17 (a)Capacitance of MOS in inversion mode (b) Capacitance of MOS in accumulation mode [20]

The PMOS varactors used in Fig 3-11 are in the accumulation mode, not in the inversion mode. It is because the generation of an inversion layer must be prevented, since minority carriers are only generated by generation/recombination, which seriously degrades the quality. Another reason to use the accumulation mode varactor is shown in Fig 4-17. In Fig 4-17 (a), the MOS varactor operates in accumulation mode, and we can find that the V_{sg} (source-to-gate voltage) must large than 1 V and then the capacitance change the value. This V_{sg} is large than the power supply voltage in this design, so the MOS varactors operate in accumulation mode in this design.

4.4.4 Discussion 4

In 1 V design, the prescaler is not avoided to consume more current than it operates in high supply voltage. Fig 4-18 shows the E-TSPC ÷2/3 dual-modulus frequency divider used in [21] and shows the size parameters. We use those size parameters to simulate the maximum operating frequency of the divider v.s. supply voltage. The simulation results are shown in Fig 4-19. In Fig 4-19 we can find that the maximum frequency strongly relates to supply voltage. In 2.5 V supply voltage this divider can

operate in 3.8 GHz input frequency, but it can operate in 800 MHz in 1 V supply voltage. That is why the TSPC does not be used in the first stage of prescaler in this design.

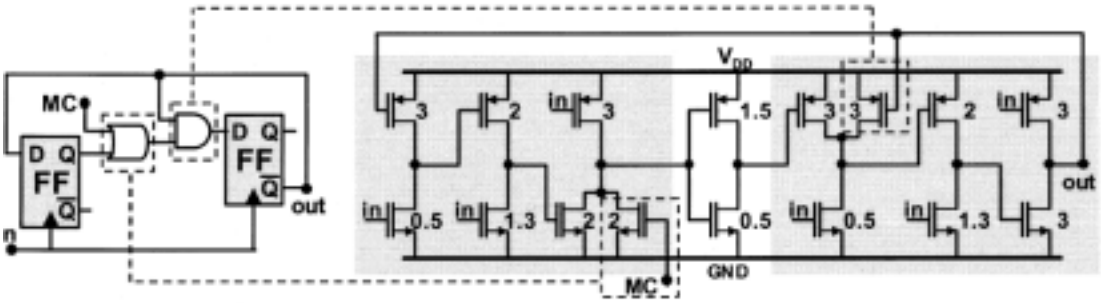


Fig 4-18 E-TSPC ÷2/3 dual-modulus frequency divider used in [21]

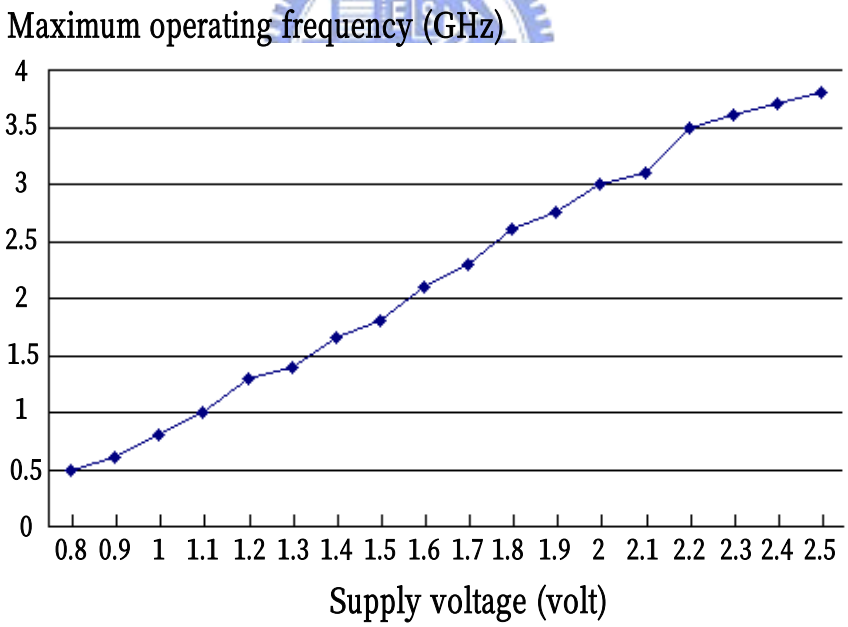


Fig 4-19 Simulation results of the maximum operating frequency V.S. supply voltage (using Fig 4-18 circuits)

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUSIONS

An improved current-match charge pump is proposed in this work. This new current-match charge pump solves the start-up problem, and it can still have good performance in current matching. So, the spur level is low.

A band-switching VCO is used in this design. By this structure, the K_{VCO} is reduced and hence that the spur level can be more reduced.

The power supply voltage is scaled to 1 V in simulation. In the charge pump, a bulk-driven OP is used to work at 1-V supply voltage. And the overall power consumption is reduced.

This work is measured and has the following performances. The spur level of this 2.4 GHz frequency synthesizer is -64.97dBc @1MHz offset. The phase noise is -111.14dBc/Hz @1MHz offset. The total power consumption is 23mW (simulation is 13 mW). The power consumption mostly increases in VCO to compensate the loss of the parasitic resisters.

5.2 FUTURE WORKS

The re-designed IC will be tabout and operate in 1 V supply voltage. The frequency divider which consume lower power in 1 V supply voltage must be developed to save more power.

In the future RF systems, the power consumption must be as small as possible. So, in the future, using the 0.13-um or 0.09-um technologies to create 0.6-V power supply systems is possible and necessary.

REFERENCES

[1] Behzad Razavi .Design of Analog CMOS IC. McGraw-Hill higher Education,2001

[2] Ali Hajimiri and Thomas H. Lee "Design Issues in CMOS Differential LC Oscillators" *IEEE J. Solid-State Circuits*, vol. 34, pp. 717-724, MAY 1999

[3] Christopher Lam and Behzad Razavi*,* "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-m CMOS Technology," *IEEE J. Solid-State Circuits*, Vol. 35, pp. 788-794, May 2000.

[4] Domine M. W. Leenaerts*,* Cicero S. Vaucher, Henk Jan Bergveld, Michael Thompson, and Kevin Moore, "A 15-mW Fully Integrated I=Q Synthesizer for Bluetooth in 0.18-_m CMOS," *IEEE J. Solid-State Circuits*, Vol. 38, pp. 1155-1162, July 2003.

[5] Chung-Chih Su. "Design of a Low-Spurious-Tones CMOS Frequency Synthesizer for 2.4GHz Transceiver." NCTU Master Thesis, 2002.

[6] Yen-Po Lee. "A CMOS 2.4GHz Low Spuriousand Quadrature output frequency synthesizer," NCTU Master Thesis, 2003.

[7] Guang-Kaai Dehng, Ching-Yuan Yang, June-Ming Hsu, and Shen-Iuan Liu, "A 900-MHz 1-V CMOS Frequency Synthesizer," *IEEE J. Solid-State Circuits*, Vol. 35, pp. 1211-1214, August 2000.

[8] J. H. Lou and J. B. Kuo, " A 1.5-V Full-swing Bootstrapped CMOS Large Capacitive –Load Driver Circuit Suitable for Low-Voltage CMOS VLSI," *IEEE J. Solid-State Circuits*, Vol. 32, pp. 119-121, January 1997.

[9] Troy Stockstad*, Member, IEEE,* and Hirokazu Yoshizawa, "A 0.9-V 0.5-uA Rail-to-Rail CMOS Operational Amplifier," *IEEE J. Solid-State Circuits*, Vol. 37, pp. 286-292, March 2002.

[10] Neric H. W. Fong, Jean-Olivier Plouchart, Duixian Liu, Lawrence F. Wagner, Calvin Plett, and N. Garry Tarr," Design of Wide-Band CMOS VCO for Multiband Wireless LAN Applications" *IEEE J. Solid-State Circuits*, VOL. 38, pp. 1333-1342, August 2003.

[11] Christopher Lam and Behzad Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-m CMOS Technology," *IEEE J. Solid-State Circuits*, Vol. 35, pp. 788-794, May 2000.

[12] Joonsuk Lee and Beomsup Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," *IEEE J. Solid-State Circuits*, Vol. 35, pp. 1137-1145, Aug 2000.

[13] Jae-Shin Lee, Min-Sun Keel, Shin-II Lim and Suki Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," *ELECTRONICS LETTERS*, 9th, Vol.36, pp. 1907-1908, No.23 Nov 2000.

[14] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1V op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 769–780, July 1998.

[15] Lizhong Sun, Dale Nelson, "A 1.0V GHz Range 0.13μm CMOS Frequency Synthesizer," *IEEE 2001 Custom Integrated Circuits Conference*, pp.327-330

[16] Thomas H. Lee, *Member, IEEE*, Hirad Samavati, and Hamid R. Rategh, "5-GHz CMOS Wireless LANs," *IEEE Transactions on Microwave Theory and Techniques,* Vol. 50, pp. 268-280, NO. 1, Jan 2002.

[17] Behzad Razavi, Member, *IEEE*, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, Vol. 31, pp. 331-343, March 1996.

[18] Hamid R. Rategh, Hirad Samavati and Thomas H Lee, "A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5-GHz Wireless LAN Receiver" *IEEE J. Solid-State Circuits*, Vol. 35, pp. 780-787, May 2000.

[19] Ali Hajimiri and Thomas H. Lee, “A General Theory of Phase Noise in Electrical Oscillators,” *IEEE J. Solid-State Circuits*, Vol. 33, pp. 179-194, Feb 1998.

[20] Pietro Andreani and Sven Mattisson “On the Use of MOS Varactors in RF VCO’s” *IEEE J. Solid-State Circuits*, Vol. 35, pp. 905-910, June 2000.

[21] S. Pellerano, S. Levantin, C. Samori, and A. L. Lacaita,“A 13.5-mW 5-GHz Frequency Synthesizer With Dynamic-Logic Frequency Divider” *IEEE J. Solid-State Circuits*, Vol. 33, pp. 378-383, Feb 2004.