2.45/5.2 GHz 雙頻帶低功率直接降頻諧波混波器之設計

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摘要

本篇論文主旨在於利用標準 0.18um CMOS 製程設計適用於無線區域網路 802.11a/b 接收器之 2.45/5.2 GHz 雙頻帶低功率直接降頻諧波混波器。此外，一個適用於 802.11a 之窄頻 5.2GHz 階段增益諧波混波器也將在本論文被設 計與分析。此兩個諧波混波器已經由晶片製作驗證。

第一顆晶片在設計與分析一個適用於 5.2GHz 頻帶無線區域網路之階段增益諧波混波器。此諧波混波器利用連接差動對的汲級消除奇次諧波及電感性帶有增益之三階濾波器加大二階諧波振幅，達到在有限電流下增益及雜訊指數最佳效能。藉由並聯開關控制，模擬結果諧波混波器有 18dB 及 8.7dB 兩種增益模式，在高增益模式下其雜訊指數在 1MHz 基頻頻率爲 16dB，輸入三階交叉點(IIP3)爲-3.1dBm。在低增益模式下其雜訊指數在 1MHz 基頻頻率爲 25.7dB，輸入三階交叉點(IIP3)爲-5.6dBm。以-10dBm 的差動 LO 訊號注入。在 1.8V 供壓，其消耗功率約爲 4.6mW。

在第二顆晶片中，一個適用於無線網路 802.11a 及 802.11b 接收器之 2.45/5.2 GHz 雙頻帶低功率直接降頻諧波混波器將被設計與驗證 。利用開關控制可變突

起頻率之三階濾波器選擇工作頻率，使諧波混波器可工作在 2.45GHz 或 5.2GHz 兩個頻率。模擬結果在 2.45GHz 之工作頻率下，其輸入返回損耗(S11)爲-11dB，轉換增益爲 16.7dB，雜訊指數爲 15.5dB，三階交叉點(IIP3)爲-6dBm。在 5.2GHz 之工作頻率下，其輸入返回損耗(S11)爲-12dB，轉換增益爲 18.9dB，雜訊指數爲 13.5dB，三階交叉點(IIP3)爲-1dBm。在 1.8V 供壓及-10dBm 差動 LO 訊號，其功率消耗約爲 2.3mW。

Design of 2.45/5.2 GHz Dual-band Low-power Direct-conversion Harmonic Mixer

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ABSTRACT

The aim in this thesis is mainly based on the design of 2.45/5.2 GHz dual-band low-power direct-conversion harmonic mixer in the receiver front-end of 802.11a/b wireless local area network (WLAN) system using standard 0.18um CMOS process. Also, a narrow band 5.2GHz step-gain direct-conversion harmonic mixer is designed and analysis for 802.11a WLAN system. The two harmonic mixers were verified through individual chips.

In the first chip, a 5.2GHz step-gain direct-conversion harmonic mixer for 802.11a WLAN system is designed and analyzed. The harmonic mixer cancels the odd harmonic of LO signal by connecting the drains of the differential pair. It adopts a third-order low-pass filter with inductive peaking increasing the second harmonic level. This optimizes conversion gain and noise performance with a restricted bias current. Controlled by a switch, the simulation result shows that the mixer offers two gain levels of 18dB and 8.7dB. At high-gain mode, it achieves noise figure of 16dB at 1MHz frequency, and third-order input intercept point of -3.1dBm. At low-gain mode, it achieve noise figure of 25.7dB at 1MHz, and third-order input intercept point of

-5.6dBm. Differential LO power level is chosen as -10dBm. With a supply voltage of 1.8V, the total power consumption is about 4.6mW.

In the second chip, a 2.45/5.2 GHz dual-band low-power direct-conversion harmonic mixer for 802.11a/b WLAN system is introduced. By tuning the peaking frequency of third-order low-pass filter, it can choose the operation frequency either in 2.45GHz or in 5.2GHz band. Simulation result shows that in 2.45GHz operation frequency, it achieves S11 of -11dB, conversion gain of 16.7dB, noise figure of 15.5dB, and third-order input intercept point of -6dBm. In 5.2GHz operation frequency, it achieves S11 of -12dB, conversion gain of 18.9dB, noise figure of 13.5dB, and third-order input intercept point of -1dBm. With1.8V power supply and -10dBm differential LO signal, the power consumption is about 2.3mW。

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劉上逸

九十三年十月

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Chapter 1

Introduction

1.1 Motivation

Wireless communications at multi-gigahertz frequencies has made much progress since the first radio frequency (RF) transceiver was published. All CMOS RF transceivers and systems-on-chip (SoC) solutions are rapidly making inroads into a WLAN market that was dominated by bipolar and BiCMOS solutions for years [1].

The typical RF receivers were assembled by such as low-noise amplifier (LNA), mixer and voltage control oscillator (VCO). The first stage of a receiver is a LNA, whose main function is to provide enough gain to suppress the noise of subsequent stages as well as adding as little noise as possible in itself. The VCO generates precise LO signal for down-conversion. The mixer connects the LNA and VCO which mixes the RF signal with the LO signal and generates intermediate frequency (IF) or base-band (BB) signal.

In heterodyne receiver architecture, there are more than two mixers and VCO(s) which convert RF signal to base-band access more than one IF. In direct-conversion architecture, there is only one mixer and VCO. Because the direct-conversion receiver

(DCR) architecture is consisted of fewer components than heterodyne one, in recent years, the DCR architecture has gained much attention as a promising solution for a single-chip RF receiver because of its low-power, low-complexity, image-rejection-free and easy-to-integrate properties.

However, design of direct-conversion receivers is required to resolve many issues such as self-mixing induced DC-offset, flicker noise, even-order distortion, I/Q mismatch, and so on. DC-offset is one of the most important issues and it can saturate the following stage in mixer output. To avoid DC-offset, harmonic mixer structure for DRC is published. In this thesis, two harmonic mixers for the receiver of 5.2GHz narrow band and 2.45/5.2GHz dual band is designed and analyzed.

The first chip for narrow band application, inductive peaking principle is applied in inter-stage of harmonic mixer for peaking of the second harmonic of LO. With a parallel switch that eliminates inductive peaking, the mixer has two gain modes. It ensures the system operating in larger input dynamic range.

The second chip for 2.45/5.2 GHz dual band system, the switchable peaking frequency third-order low-pass filter chooses the operation frequency. The dual-band input matching makes the two bands coexisted and the peaking inductor chooses the operation frequency either in 2.45GHz or in 5.2GHz. The power consumption is half of the first one, while the performance does not degrade too much.

1.2 Thesis Organization

In the Chapter 2 of the thesis, the DC-offset issue in different receiver architecture is introduced. Although in direct-conversion receiver, this issue is the most important problem to overcome. Two harmonic mixers are introduced. Based on the first harmonic mixer, two harmonic mixers in this these is designed and measured in following chapter.

In Chapter 3, a narrow band harmonic mixer using inductance peaking topology intended for application of the 5.2GHz wireless direct-conversion receiver is introduced. The detailed circuit analysis and design equation is presented. The odd-harmonic cancellation scheme and the second harmonic enhancement by inductance peaking are also discussed. Finally, measurement result of the mixer fabricated by TSMC 0.18um CMOS technology is discussed.

In Chapter 4, a 2.45/5.2-GHz dual-band low-power harmonic mixer intended for 802.11a/b system is proposed. The switchable inductance peaking scheme is adopted for switching frequency. Based on chapter 3, the harmonic mixer is designed in lower power and two bands input matching. Finally, measurement result of the mixer fabricated by TSMC 0.18um CMOS technology is discussed.

In the last chapter, all the work is summarized and concluded.

Chapter 2

DC-Offset Issue in RF Receiver

In this Chapter, the DC-offset issue is analyzed in different situations. DC-offset issues in direct-conversion receivers are analyzed in section 2.1. In this section, the DC-offset issue would be discussed about how the DC-offset influence the direct-conversion receiver and how to avoid or release it. It also shows the DC-offset-free characteristic of the harmonic mixer. DC-offset issue would be discussed in low-IF receiver and in heterodyne receiver in section 2.2 and section 2.3. In these sections, they show the DC-offset issue is migrated cleverly by the architecture design but these architectures induce other issues at the same time.

2.1 Direct-conversion Receiver

The direct-conversion receiver (DCR) [Fig. 2.1] is also called “homodyne” or “zero-IF” architecture because that the RF signal transfers to output and is down-converted to zero-frequency. Shown in Fig. 2.2 is a simple frequency conversion of DCR, where the local oscillator (LO) frequency is equal to the input radio frequency (RF) carrier and the channel selection requires only a low-pass filter with relatively sharp cutoff characteristics [2]. This architecture was invented many decades ago, and was improved greatly in recent years. The reasons that this architecture has recently become the topic of active research, perhaps to a much greater extent than before are accounted for this renaissance:

(1). Direct-conversion architecture which eliminates of SAW filter and all of

subsequent down-conversion stages are replaced with low-pass filters, in principle, lends itself to monolithic integration much more easily than heterodyne receivers;

(2). The problem of image is circumvented because of $\omega_{IF} = 0$. As a result, no image filter is required, and the LNA need not drive a 50-Ω load for off-chip SAW filters;

(3). Direct-conversion architecture's past failures arose primarily from effects that could not be removed in discrete implementations, but may be controlled and suppressed in integrated circuits.

In other words, direct-conversion architecture is one of few reception techniques whose drawbacks can be remedied through the use of only more transistors [3].

Nevertheless, the DRC direct translation of the spectrum to zero frequency entail a number of issues that do not exist or are not as serious in a heterodyne receiver. One of the most serious issues is the DC-offset issue.

2.1.1 DC-Offset Issue in Direct-Conversion Receiver

Since in the direct-conversion topology, the down-converted band extends to zero frequency, extraneous offset voltage can corrupt the signal and, more importantly, saturate the following stages. To understand the origin and impact of DC-offsets, consider the receiver shown in Fig. 2.3, where the LPF is followed by an amplifier and an A/D converter. The LPF would not decrease the DC-offset value, and it can easy saturate the following stage. The DC-offset is caused by three sources mainly.

(1). Self-mixing due to LO Leakage [Fig. 2.3(a)]:

The isolation between the LO port and the input of the mixer and the LNA is finite. This effect arise from capacitive feed-through and substrate coupling and, if the

LO signal is provided externally, bond wire coupling. The LO signal leaks into point A or point B, and is reflected at the output port of RF amplifier and at the antenna connector. The reflected LO signal is self-mixed at the mixer and results in DC-offset [4]. In most receiver architectures, the LO signal power level is much greater than RF signal power level. That means, in designing of DCR, it always considers the restriction of the mixer LO-to-RF input isolation and the low-noise amplifier (LNA) reverse isolation to avoid the base-band output with large DC-offset which will saturate the following stage. This is the main DC-offset generator in DRC architecture.

(2). Self-mixing due to large interferer in RF port [Fig. 2.3(b)]:

This is similar to former because that isolation between the LO port and the input of the mixer and the LNA is finite. The effect occurs if a large interferer leaks from the LNA and mixer LO input, point C, and is multiplied by itself to result in DC-offset.

(3). Mismatch of component:

The mismatch of differential pair also cause DC-offset in output. This can be solved by mismatch compensation circuit design.

For example: the total gain from the antenna to point X is typically around 80 to 100 dB so as to amplify the microvolt input signal to a level that can be digitized by a low-cost, low power analog-to-digital converter (ADC). Of this gain, typically 25 to 30 dB is contributed by the LNA/mixer combination.

With the above observations, we can obtain a rough estimated of the offset resulting from self-mixing to appreciate the problem. Suppose in Fig. 2.3 (a) the LO signal has a peak-to-peak swing of 0.63V (0 dBm in a 50Ω system) and experiences an attenuation of 60 dB as it couples to point A. If the gain of the mixer is on the order

of 10mV, we also note that the desired signal level at this point can be as low as approximately 30 μV_{rms}. Thus, if directly amplified by the remaining gain of 50 to 70 dB, the offset voltage saturates the following circuits, there by prohibiting the amplification of the desired signal [2].

2.1.2 Quantification of Self-Mixing DC-Offset

Fig. 2.4 shows the self-mixing mechanism. The LO frequency is set at the same frequency as the received signal frequency, and the received signal is down-converted to base-band directly. The LO signal leaks to the RF signal input port of the mixer and is reflected at the output port of the low noise amplifier (LNA) and at the antenna. The reflected LO signal is down-converted at the mixer and results in a DC-offset.

The offset voltage at the mixer output due to self-mixing V_{self} is described by

$$V_{self} = V_{leak} R_{amp} G_{LO-BB} \tag{2.1}$$

where V_{leak} is the leaked LO signal voltage, R_{amp} is the reflection factor at the RF amplifier output port, and G_{LO-BB} is the conversion gain of the mixer from LO signal frequency to base-band. The RF amplifier gain is often switched depending on received signal strength. Therefore, the self-mixing output is not a stable DC-offset.

The equation (2.1) suggests three ways to reduce the offset V_{self}. The first is reducing LO signal leakage V_{leak}. The second is reducing R_{amp}. Note that the R_{amp} is varied depending on the electromagnetic environment of the antenna and the reverse and/or forward gains of the RF amplifier, and it is difficult to realize extremely small R_{amp} practice. The last is reducing the conversion gain G_{LO-BB}. In the usual direct-conversion case, reducing conversion gain does not improve desire-

signal to undesired-signal ratio, therefore a raw output offset voltage cannot be a measure for self-mixing. In reference paper [4] [5], it uses the equivalent RF amplitude V_{eq} at mixer input while assuming the worst case of $R_{amp}=1$ as the measure of self-mixing:

$$V_{eq}=V_{leak}\frac{G_{LO-BB}}{G_{RF-BB}} \tag{2.2}$$

where G_{RF-BB} is the conversion gain from received signal frequency to baseband. The way to reduce V_{eq} are (1) to reduce V_{leak}, and (2) to reduce $\frac{G_{LO-BB}}{G_{RF-BB}}$. This will describe the efficient realization of these conditions by this thesis.

For example, in a typical direct-conversion receiver, assuming the LO signal is -10dBm, -50dBm V_{leak} from the RF input port (i.e. 40dB isolation), and the -14dB reflection factor at the RF amplifier output ($VSWR\approx 1.5$), reflected LO signal is -64dBm ($140\,\mu V_{rms}$) at mixer input. This is 57dB higher than thermal noise in 200kHz bandwidth from $50\,\Omega$ resistor.

2.1.3 To Avoid DC-Offset: Harmonic Mixer

Fig.2.5 (a) shows that the LO self-mixing problem in a DCR arises due to the situation that LO signal resides at the same frequency as the RF signal. As DC-offset can't be easily filtered out without removing any base-band signal because most modulation schemes contain significant DC and low frequency components. Because DC-offset is caused by self-mixing of LO signal mainly, one should apparently

separate the RF and LO frequencies in order to avoid the problem.

That means: if LO frequency is separated far away from RF frequency, there is no DC-offset problem. For the harmonic mixer shown in Fig.2.5 (b), it is the second harmonic of the LO signal that takes part in the mixing process. In equation (2.2), the V_{eq} is zero because the LO leakage in receiving frequency in RF input is zero. As a result, the LO leakage generates no DC component but an output the LO frequency and can be easily filtered out with a low-pass filter (LPF).

Fig.2.6 shows the typical working principal of a direct-conversion harmonic mixer. The LO frequency is just in the 1/n of RF frequency. It not only simplifies the oscillator design consideration but solves the DC-offset issue of DCR. The CMOS balance harmonic mixer proposed by Zhang [6] generates the second harmonic of LO frequency by odd harmonic cancellation and mixes it with RF signal in the NMOS pair which is operating in sub-threshold region. It adopts current injection to decrease transistor's current and lower flicker noise. The harmonic mixer proposed by Fang [7] receives quadrature LO signal with two cascaded transistors and operation as a switch at twice frequency of LO signal. These works, however, suffer from the low third-order input intercept point (IIP3) problem and fixed conversion gain.

2.1.4 Others Way to Avoid DC-Offset

This section shows some DC-offset cancellation scheme. DC free coding and DC-offset compensation will be introduced in following paragraph.

2.1.4.1 DC-Free Coding with High Pass Filter

The base-band signal in the transmitter can be encoded such that, after modulating and down-conversing to base-band, it contains little energy near DC. With accessing a high pass filter, the DC-offset problem can be solved by wasting few of signals. Called “DC-free coding,” this is particularly suited to wideband channel, for example, in DECT, where a few kilohertz of the channel can be wasted with no significant drop in the data rate.

2.1.4.2 DC-Offset compensation

This technique exploits the idle time intervals in digital wireless standards to carry out offset cancellation. Shown in Fig.2.7 is an example, where a capacitor C1 stores the offset between consecutive TDMA bursts, while introducing a virtually zero corner frequency during the reception of data. For a typical TDMA frame of a few milliseconds, offset cancellation is performed with sufficient frequency to take into account variations due to moving objects.

2.2 Heterodyne Receiver

Fig.2.8 shows the heterodyne receiver architecture with one intermediate frequency (IF) before the RF signal down-converts to base-band. The "Heterodyne" means that there is one or more IF before base-band signal. This is the most mature receiver design scheme today because each performance would trade of properly in each stage. The heterodyne architecture has some issues compare to homodyne architecture, such as image problem. The image reject filters require high Q and need off-chip SAW components usually. For this reason, the heterodyne receiver is hardly to cost down and applies to system-on-chip (SoC) designs.

2.2.1 Frequency planning

How to choose the LO frequency and the IF frequency? The principal consideration here is the "image problem." To understand the issue, note that a simple analog multiplier does not preserve the polarity of the difference between its two input frequencies, i.e., for $x_1(t) = A_1 \cos \omega_1 t$ and $x_2(t) = A_2 \cos \omega_2 t$, the mixer output products of $x_1(t)$ and $x_2(t)$ is the from $\cos(\omega_1 - \omega_2)t$, no different from $\cos(\omega_2 - \omega_1)t$. Thus, in a heterodyne architecture, the bands symmetrically located above and below the LO frequency are down-converted to the same center frequency [Fig.2.9] if the received band of interest is centered around $\omega_1 \quad (= \omega_{LO} - \omega_{IF})$, then the image is around $2\omega_{LO} - \omega_1 (= \omega_{LO} + \omega_{IF})$ and vice versa.

2.2.2 DC-offset Issue

The DC-offset issue in heterodyne receiver is so slight that most papers have not make mention of it. Chapter 2.1.1 describes that DC-offset is caused by (1) Self-mixing due to LO Leakage [Fig. 2.3(a)] (2) Self-mixing due to large interferer in RF port [Fig. 2.3(b)] (3) Mismatch of components. The DC-offset which is caused by mismatch could compensation by negative feedback or digital signal process and fully calibrated. The DC-offset which is caused by self-mixing of leakage is due to the coupling effect or substrate loss between LO and RF input. The coupling effect is proportion of operation frequency. In other words, the heterodyne architecture has slight DC-offset due to coupling effect because of the lower LO frequency. Fig.2.10 is the basic substrate model. The substrate behaves as a resistor. The metal line and substrate have parasitic capacitance effect which the resistance is the function of frequency. The resistance between LO and RF input is

$$R_{eq} = l \times R_{sub} + \frac{1}{j2\pi f C_{RF}} + \frac{1}{j2\pi f C_{LO}} \tag{2.3}$$

where l is the distance between RF and LO input, R_{sub} is the substrate resistance per unit, C_{RF} and C_{LO} is the capacitance of both port to substrate. Equation (2.3) show the substrate loss between these ports is influenced by layout scheme and the frequency. In heterodyne receiver, the frequency of the final mixing stage is less than the homodyne one's. In most of the heterodyne architecture, the final mixing stage LO frequency has less than the one-fifth of the received signal. The DC-offset which is caused by self-mixing is direct proportion of $V_{leakage}^2$, and with this reason, the DC-offset in heterodyne receiver could be ignored.

2.3 Low IF Receiver

In the heterodyne architecture of Fig.2.8, low frequency operations such as the second set of mixing and filtering can be performed more efficiently in the digital domain. Shown in Fig.2.11 is an example where the first IF signal is digitized, "mixed" with the quadrature phases of a digital sinusoid, and low-pass filtered to yield the quadrature base-band signal. This approach is sometimes called a "digital-IF architecture."

This principal issue in this approach is the performance required of the analog-to-digital converter (ADC). Since the signal level at AMP output in Fig.2.11 is typically no higher than a few hundred micro-volts, the quantization and thermal noise of the ADC must not exceed a few tens of micro-volts. Furthermore, if the first IF band-pass filter cannot adequately suppress adjacent interferes, the nonlinearity of the ADC must be sufficiently small to minimize corruption of the signal by inter-modulation. Also, the ADC dynamic range must be wide enough to accommodate variations in the signal level due to path loss and multi-path fading. Additionally, the ADC must achieve an input bandwidth commensurate with the value of IF while consuming a reasonable amount of power.

2.3.1 DC-offset Issue

In low IF structure, the DC-offset issue is migrated cleverly because that the frequency of DC-offset is different to IF signal. As shown in Fig.2.12 (b). In Fig.2.12 (a), the self-mixing introducing DC-offset is in the zero frequency, while the conventional direct-conversion mixer suffers this issue because of the signal is

down-converted to zero frequency and overlaps the DC-offset in frequency. As DC-offset can't be easily filtered out without removing any base-band signal because most modulation schemes contain significant DC and low frequency components. Low IF architecture becomes a possible solution to DC-offset, but it suffers from the complex digital process and high speed ADC to convert base-band signal from IF signal. The low IF structure also suffers from the image problem as heterodyne receiver.

2.4 Some Reference Harmonic Mixers

In this section, some harmonic mixer is introduced. All of these are designed in the cause of DC-offset-free. Some of these is done in symmetrical, and they could increase the second-order input intercept point (IIP2).

2.4.1 900MHz Balanced Harmonic Mixer

The "A 900MHz CMOS Balanced Harmonic Mixer for Direct Conversion Receiver" is published in *Proc. IEEE RAWCON2000* [6]. It's fabricated in a 0.35um standard digital CMOS process. In Fig. 2.13, the second harmonic is easily obtained because of the inherent square-law operation of the CMOS transistor. The LO stage is actually a squaring cell with converts the differential LO voltage to the time-varying current which contains the second harmonic. In principle, the fundamental and all odd harmonics of the LO will be cancelled out at the connected drain terminals and the DC offset problem will be mitigated.

Flicker noise is an issue in direct conversion receivers. When the transistor size is increased, however, it is found that the optimal point moves towards the weak

inversion region. To reduce the flicker noise, the RF part can be biased near this region. At a biasing current, a larger W/L ratio drives the device toward the moderate or weak inversion region.

The objective of the injected current source is to reduce the current in the two upper transistors driven by the RF signal. This helps to reduce the 1/f noise of the upper transistor pair. The injected current itself will not introduced noise in this balanced structure. Unlike the normal Gilbert-type mixer, the two RF transistors change their currents simultaneously and any noise at their common source node will be completely cancelled out at the differential output

2.4.2 2GHz Even Harmonic Mixer

Fig. 2.14 show a double-balanced version of the CMOS even-harmonic mixer; it provides down conversion mixing of the differential RF input signal with even harmonics of the LO differential signal while suppressing RF mixing with the LO fundamental and odd harmonics. This circuit is reference from *ISCAS 2002* [7], and it's fabricated in a 0.25um standard digital CMOS process. As shown, suppression of odd harmonic mixing is accomplished by summing differential signal at the drains of M5 and M6 (BB+), and M7 and M8 (BB-). In order to quickly switch ON and OFF the MOSFETs and obtain adequate amplitudes of the even harmonics, a non-50% duty cycle square-wave LO signal is required. As shown in Fig. 2.14, by cascading 90° (LO_{90}) and 270° LO (LO_{270}) switches with 0° (LO_0) and 180° LO (LO_{180}) switches, respectively, the input RF signal behaves as if it is mixed with an LO signal with a non-50% duty cycle. Hence, this topology generates the even harmonics required for the mixing operation and enables the use of square-wave LO signals for

good noise performance.

2.5 Summary

DC-offset issue is the most serious issue in direct-conversion receiver. Due to the frequency planning, this issue is slightly in heterodyne receiver and low-IF receiver. From Fig. 2.5, the harmonic mixer which is free from DC-offset issue seems to be one of solution for direct-conversion to overcome DC-offset. With this faith, the research will focus on direct-conversion harmonic mixer.

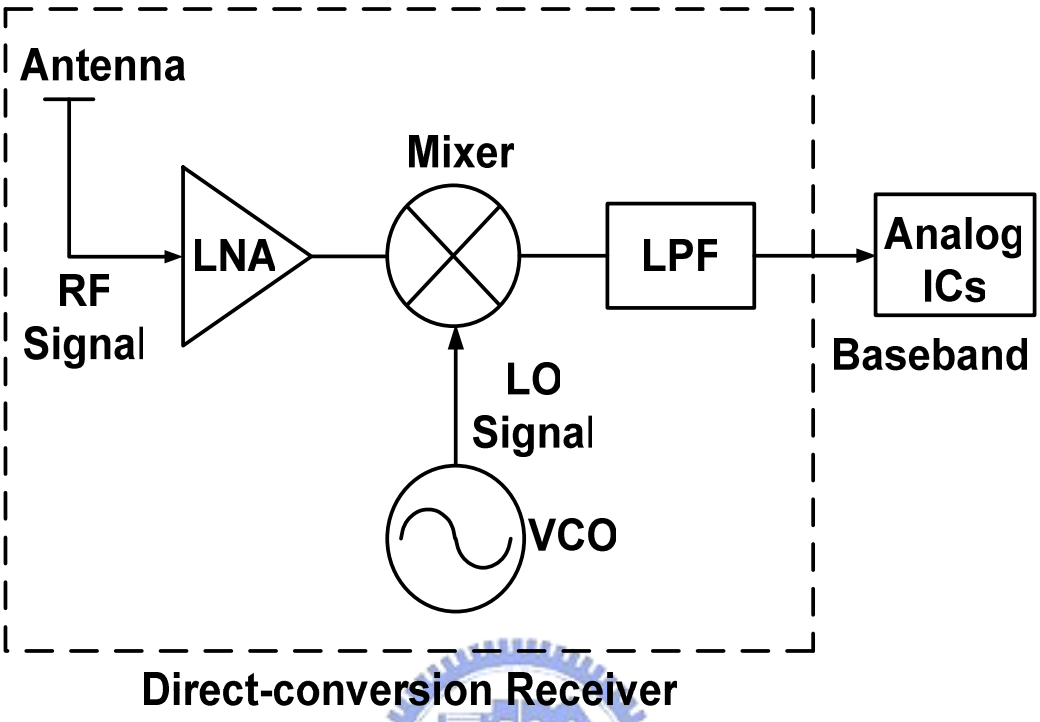


Fig. 2.1 Direct conversion receiver architecture

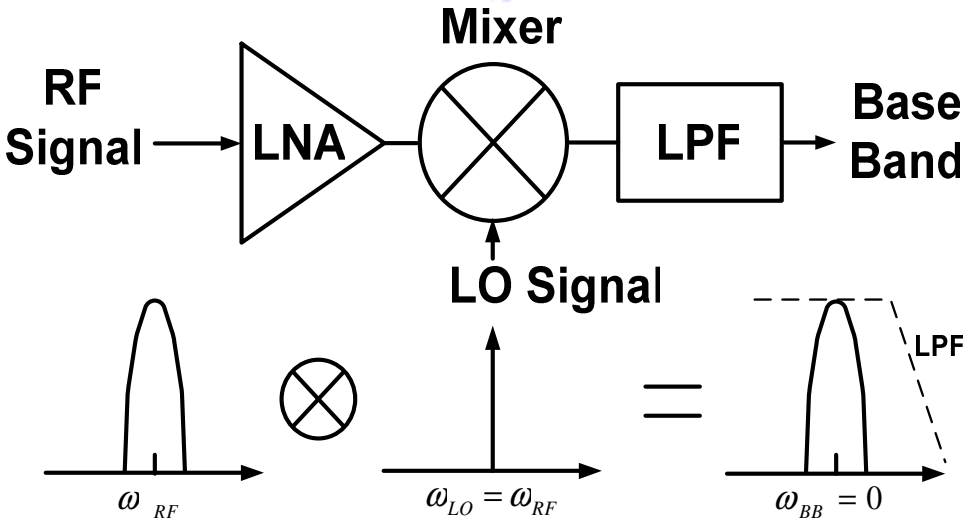


Fig. 2.2 Frequency conversion of direct conversion receiver

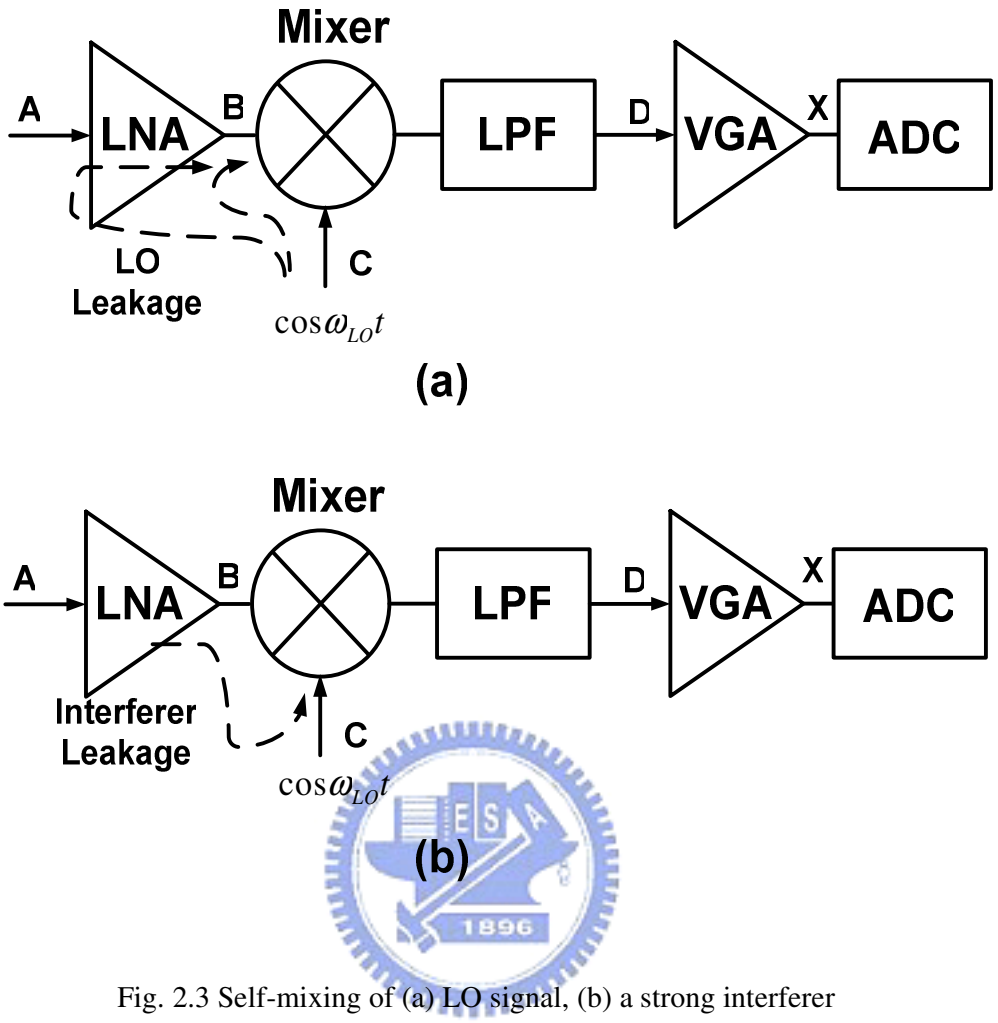


Fig. 2.3 Self-mixing of (a) LO signal, (b) a strong interferer

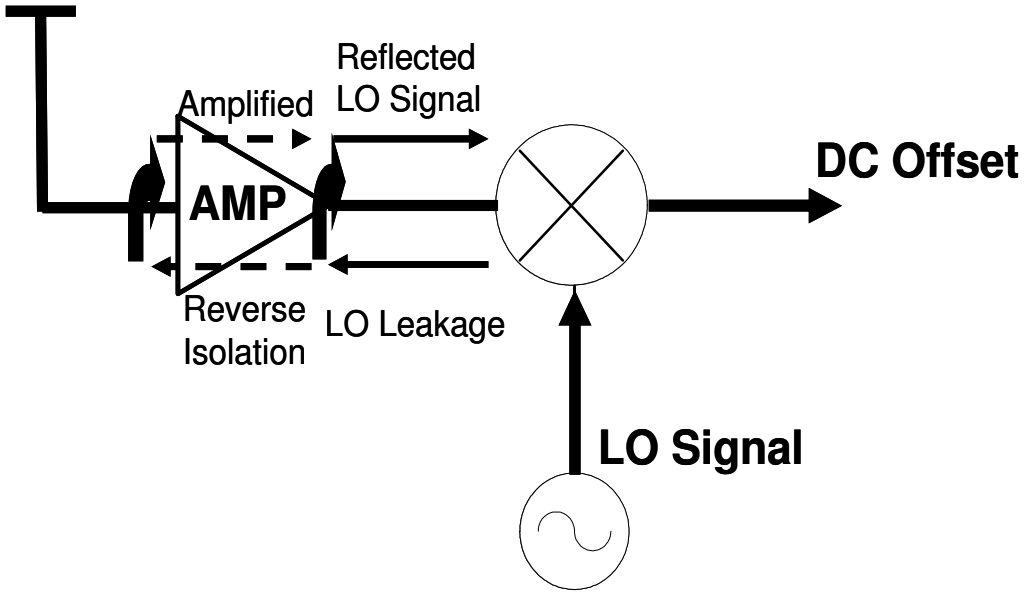


Fig. 2.4 Self-mixing due to LO leakage

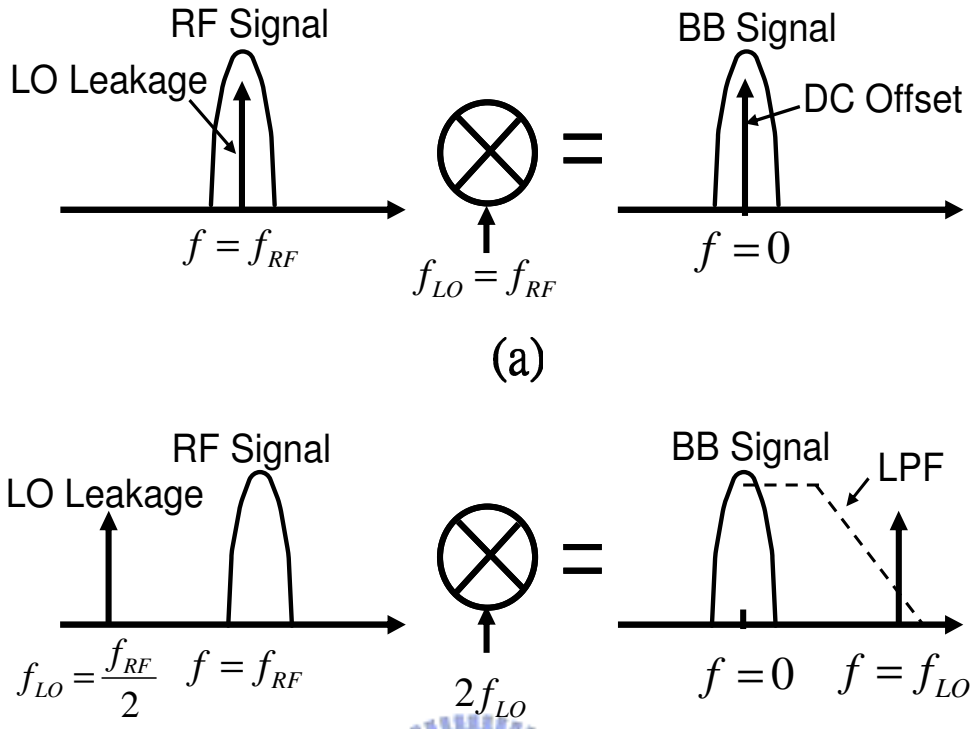


Fig. 2.5 DC-Offset issue of (a) the conventional mixer (b) the second harmonic mixer

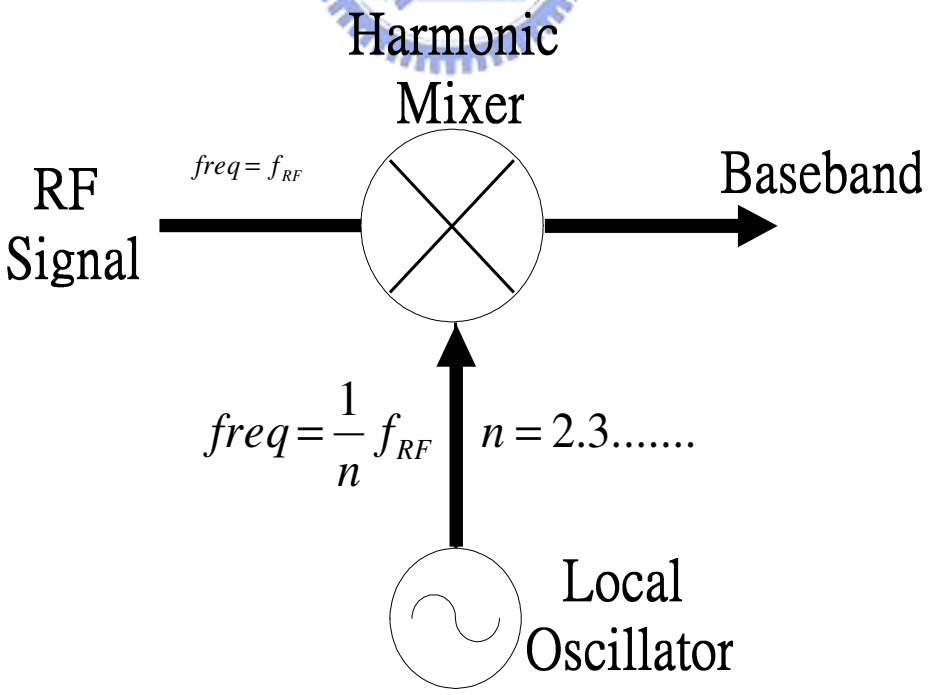


Fig. 2.6 Work principle of harmonic mixer

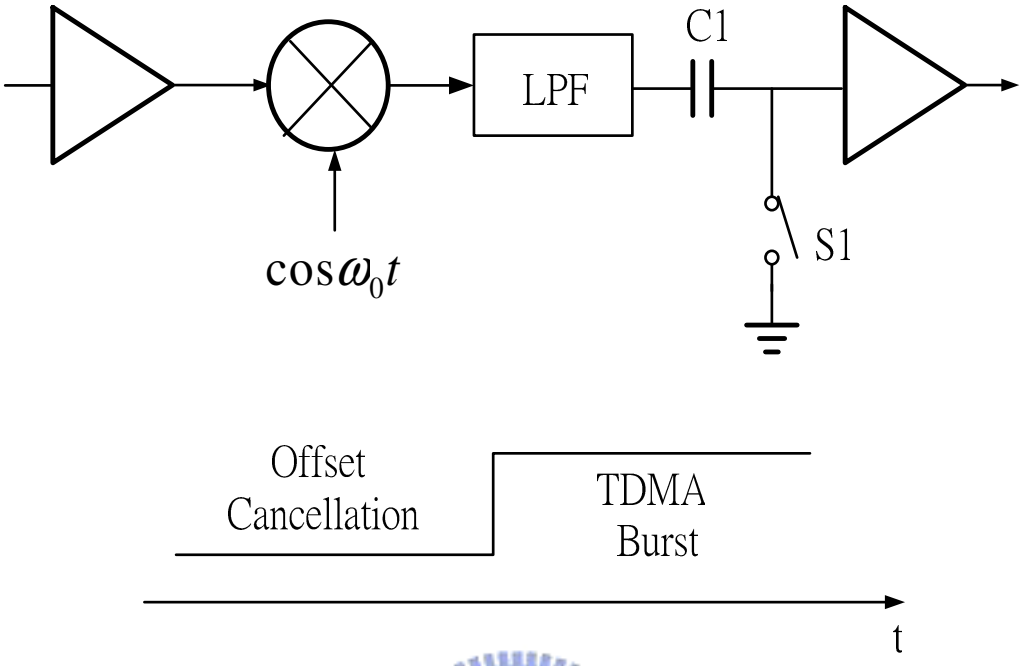


Fig. 2.7 DC-Offset compensation

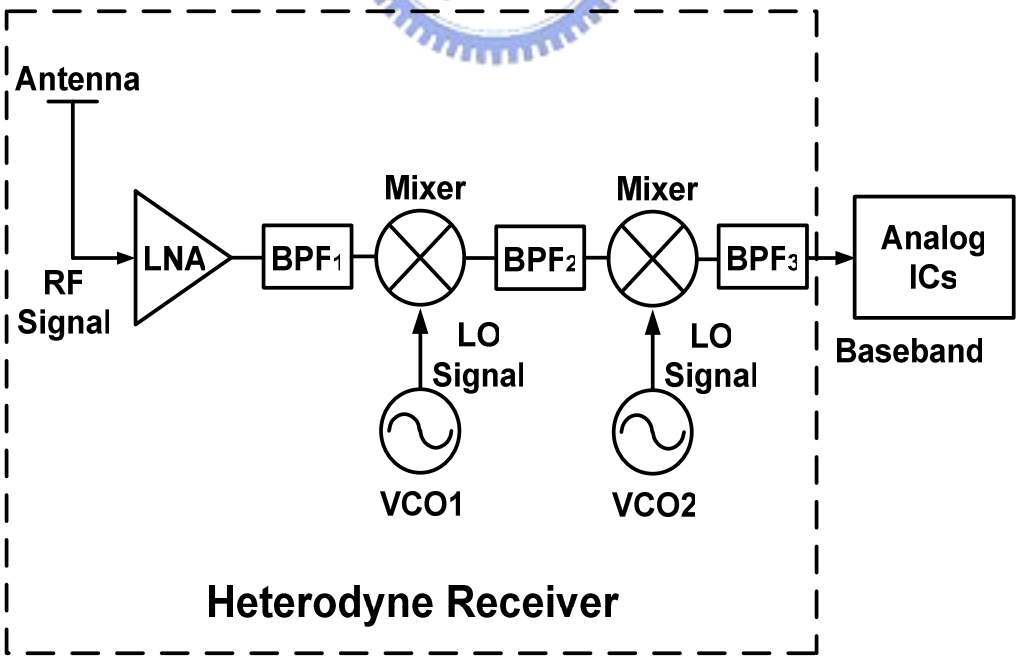


Fig. 2.8 Heterodyne receiver

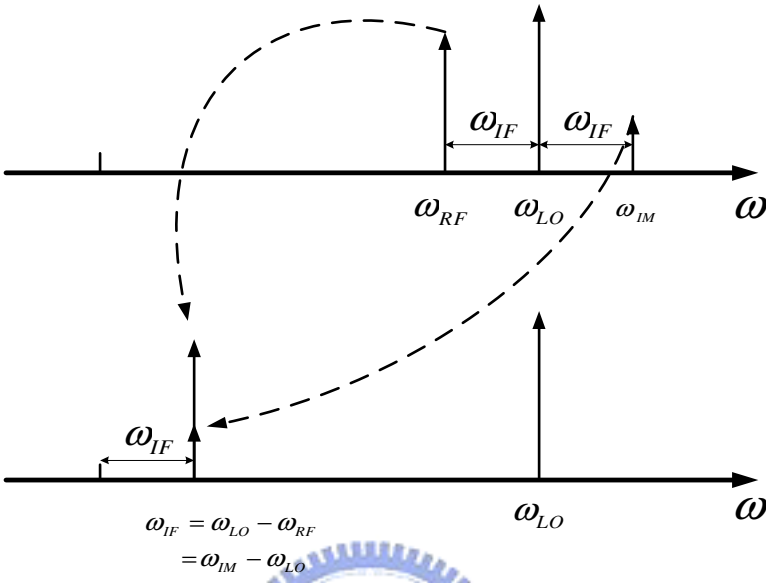


Fig. 2.9 Frequency planning

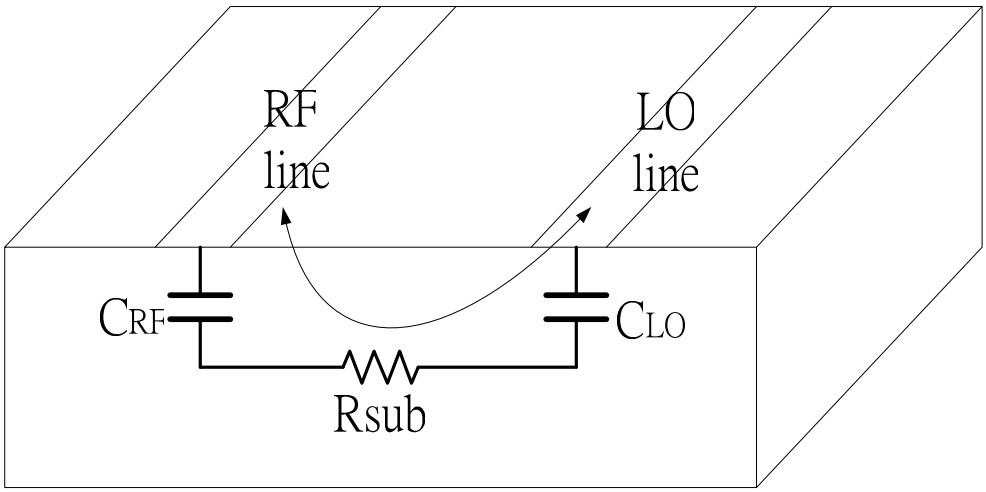


Fig. 2.10 Feedthrough caused by substrate loss

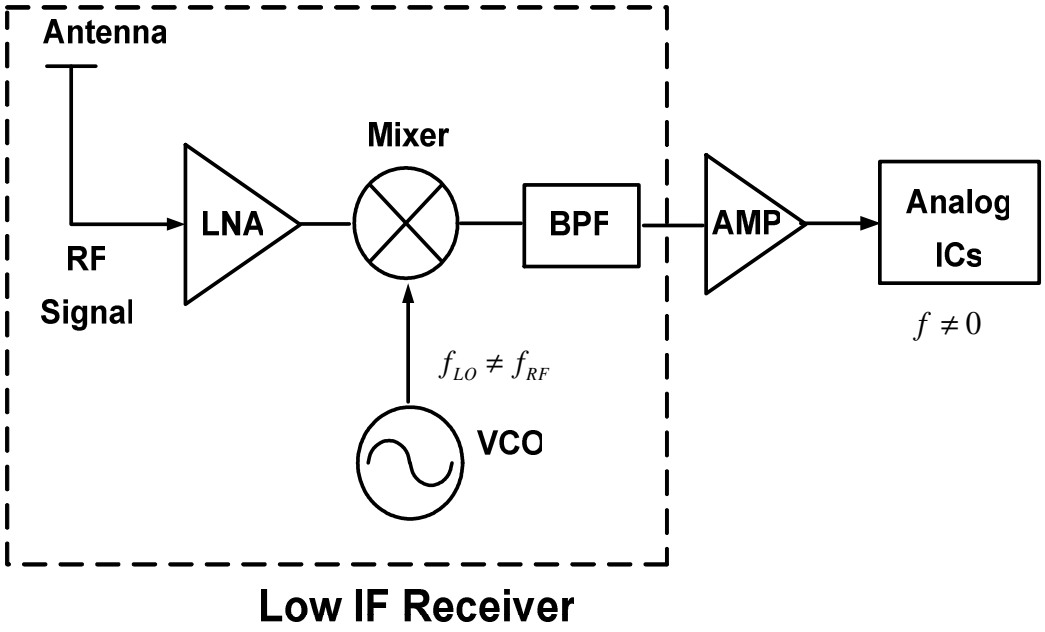


Fig. 2.11 Low IF receiver

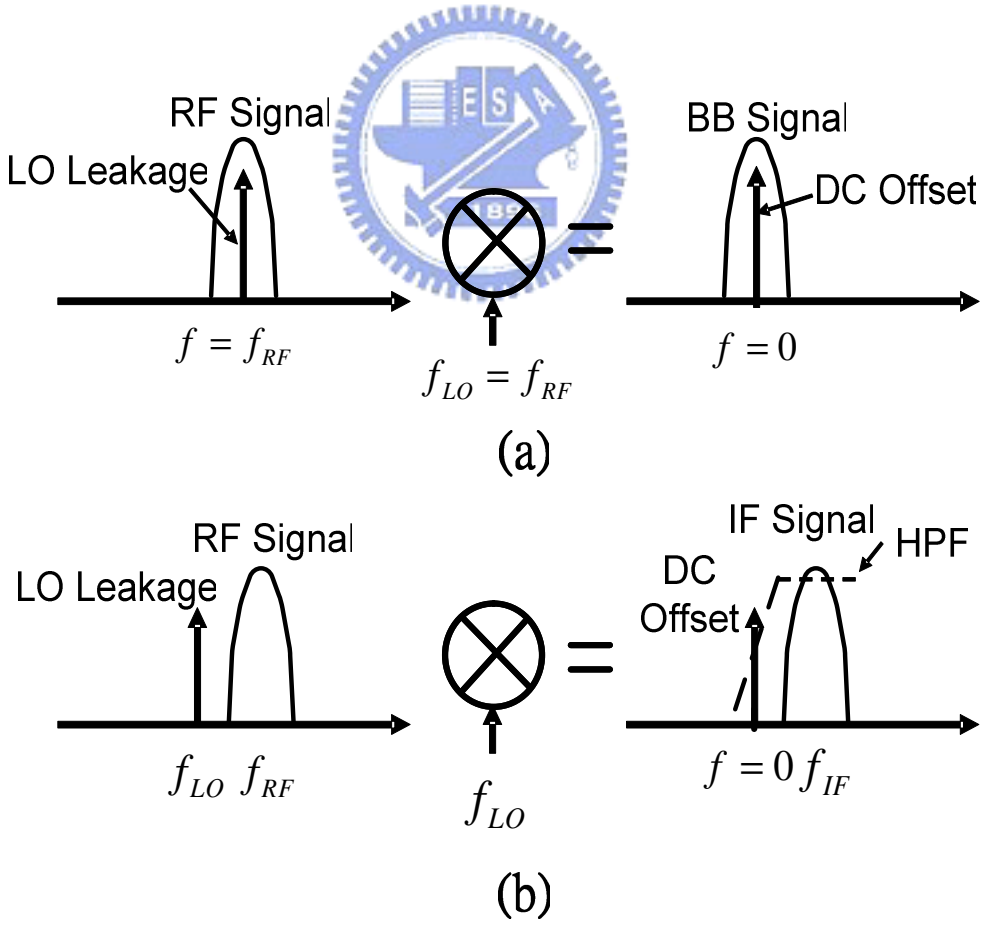


Fig. 2.12 DC-offset issue of (a) direct conversion receiver (b) low IF receiver

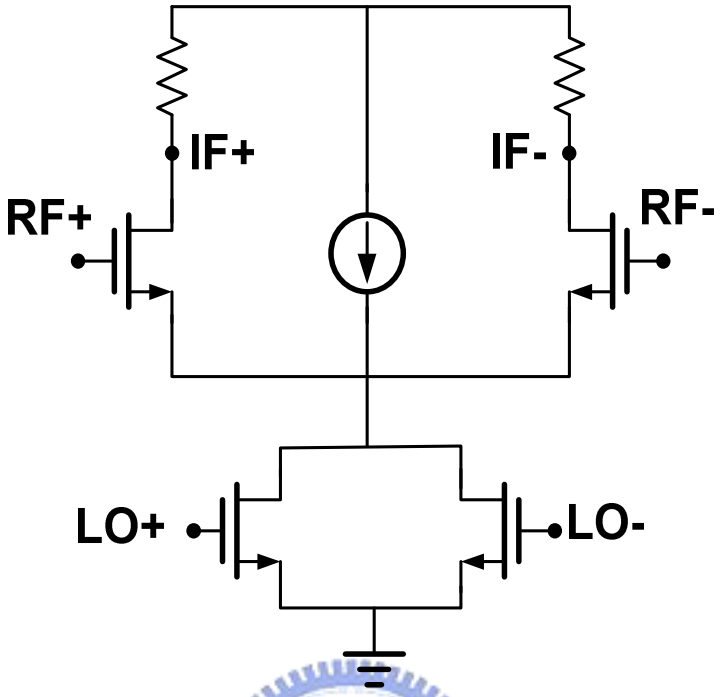


Fig. 2.13 A 900MHz balanced harmonic mixer

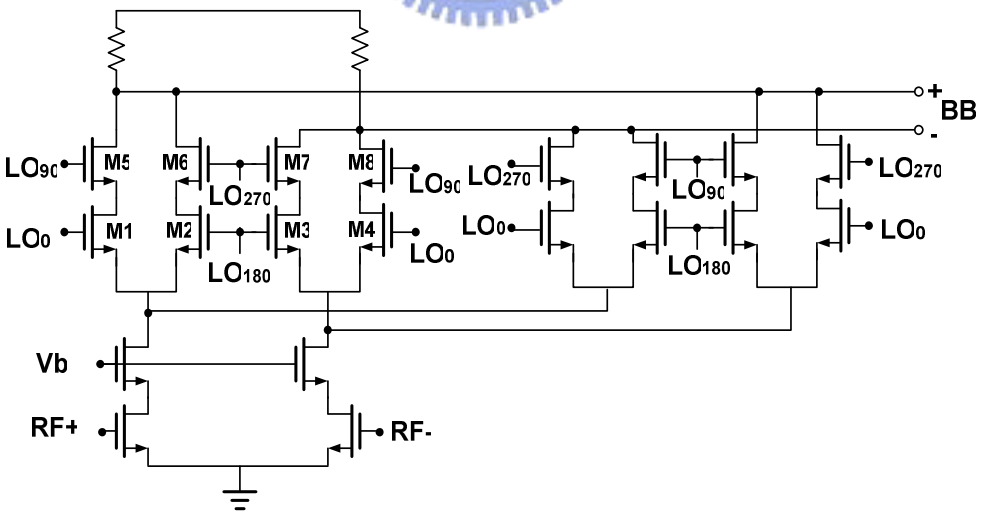


Fig. 2.14 A 2GHz even harmonic mixer

Chapter 3

A 5.2GHz Direct-Conversion Step-Gain Harmonic Mixer

3.1 Motivation

We have introduced the DC-offset issue in direct-conversion receiver in section 2.1.1. From section 2.1.3 and Fig. 2.5, they show that the LO self-mixing problem in the direct-conversion receiver arises due to the situation that the LO signal resides at the same frequency as the RF signal. As DC-offset can't be easily filtered out without removing any base-band signal because most modulation schemes contain significant DC and low frequency components. In section 2.1.3, it also shows that the harmonic mixer architecture resolves the DC-offset issue which the LO frequency is just at the half of RF frequency. This architecture is the most suitable solution of DC-offset issue because of needing no compensation circuits. In this chap, a harmonic mixer with step-gain function is introduced and implemented in 0.18 μm CMOS process.

3.2 Analysis of the Step-Gain Harmonic Mixer

The CMOS step-gain harmonic mixer is shown in Fig. 3.1 This harmonic mixer is composed of three parts: (1). harmonic generation stage; (2). mixing stage and injection current source, and (3). gain tuning stage.

3.2.1 Harmonic Generation Stage

The harmonic generation stage consists of transistors M_{LO+} and M_{LO-}. The second harmonic is obtained by the inherent square-law operation of the transistor. Each NMOS I/V curve can be shown as power series:

$$I\_LO+ = a_0 + a_1\frac{V_{in}}{2} + a_2\frac{V_{in}^2}{4} + a_3\frac{V_{in}^3}{8} + a_4\frac{V_{in}^4}{16} \tag{3.1}$$

$$I\_LO- = a_0 - a_1\frac{V_{in}}{2} + a_2\frac{V_{in}^2}{4} - a_3\frac{V_{in}^3}{8} + a_4\frac{V_{in}^4}{16} \tag{3.2}$$

$$I\_har = (I\_LO+) + (I\_LO-) = 2a_0 + a_2\frac{V_{in}^2}{2} + a_4\frac{V_{in}^4}{8} \tag{3.3}$$

$$= (2a_0 + \frac{1}{2}a_2 + \frac{3}{4}a_4) + (a_2 + a_4)\cos 2\omega t + a_4\cos 4\omega t \tag{3.4}$$

Where $V_{in} = \cos\omega t$.

Equation (3.4) shows that in drain combined point of transistors M_{LO+} and M_{LO-}. The odd harmonic of both transistors is canceling because of the differential signal input. In reference paper [6], both transistors are operating in saturation region. Equation (3.4) can be rearranged to be a square-law equation:

$$I\_har = (I\_LO+) + (I\_LO-)$$

$$= \frac{1}{2}K\left[(V_g + \frac{V_{in}}{2}\cos\omega t - V_t)^2 + (V_g - \frac{V_{in}}{2}\cos\omega t - V_t)^2\right]$$

$$= K\left[(V_g - V_t)^2 + \frac{V_{in}^2}{8}\right] + \frac{KV_{in}^2}{4}\cos 2\omega t \tag{3.5}$$

where $K = \mu_n C_{OX} \frac{W}{L}$.

As Vg is the gate bias of both transistor, V_t is the threshold voltage, μ_n is the mobility of NMOS, C_{OX} is the gate capacitance and W/L is the width/length ratio of the transistor.

In short channel devices, square-law operation is weakened due to velocity saturation phenomenon.

In long channel devices (without velocity saturation):

$$I_D \approx \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_t)^2 \tag{3.6}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_n C_{OX} W}{L} (V_{GS} - V_t) \tag{3.7}$$

$$g_m' = \frac{\mu_n C_{OX} W}{L} \tag{3.8}$$

In short channel devices (with velocity saturation):

$$I_D \approx \frac{\mu_n C_{OX}}{2\left(1 + \frac{V_{GS} - V_t}{\varepsilon_C L}\right)} \frac{W}{L} (V_{GS} - V_t)^2 \tag{3.9}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_n C_{OX} W}{2\varepsilon_c L} \left[\frac{(V_{GS} - V_t)^2}{(1 + \frac{V_{GS} - V_t}{\varepsilon_c L})^2} + 2K \frac{1}{(1 + \frac{V_{GS} - V_t}{\varepsilon_c L})} \right] \tag{3.10}$$

$$g_m' = \frac{\mu_n C_{OX} W}{2\varepsilon_c L} \left[\frac{2}{\varepsilon_c L} \frac{(V_{GS} - V_t)^2}{(1 + \frac{V_{GS} - V_t}{\varepsilon_c L})^3} + 2(1 + \frac{1}{\varepsilon_c L}) \frac{V_{GS} - V_t}{(1 + \frac{V_{GS} - V_t}{\varepsilon_c L})^2} + 2 \frac{1}{(1 + \frac{V_{GS} - V_t}{\varepsilon_c L})} \right]$$

(3.11)

As equation (3.8), the g_m' is equal to a_2 in power series. In long channel device, the square characteristic lets the a_2 as a constant. In short channel device, assume the velocity saturation is large, the $\frac{V_{GS}-V_t}{\varepsilon_c L}$ term is large. Let $\frac{V_{GS}-V_t}{\varepsilon_c L}$ term >>0, then the g_m' in equation (3.11) is zero. That means the I/V curve is linear, and the second harmonic is unapparent.

To generate higher second harmonic component level, a current source and a capacitor are connected to both M_{LO+} and M_{LO-} transistor's source terminals. Both transistors operate as switches and capacitor bypass the even order harmonics. In this operation point, the second harmonic level would be enhanced greatly.

Fig. 3.2 shows the 2nd harmonic/DC ratio curve of MOS. The dot line is the MOS which is working in saturation region and solid line is the proposed swich-like CMOS pair. The dot line in Fig. 3.2 shows that 2nd harmonic is degraded with Vgs and the proposed harmonic generation generates larger 2nd harmonic than former. It also shows that the 2nd harmonic is large in low Vgs voltage. To consider the biasing condition of Fig. 3.3 (a), if the Vgs is biased in low voltage such as 0.6V in 0.18um process, with the injection of large LO power, the Vgs is swing with LO voltage. The 2nd harmonic is not a constant, and is low when effective Vgs is large. This is because

that the source of MOS pair is connected to ground and Vgs is decided by gate voltage of MOS. To solve this issue, a proposed solution is brought out as Fig 3.3 (b). A current source is connected between common source point and ground. With floating Vs, the overdrive of Vgs is a constant and Vs is swing with Vg. By adjust current source, a proper Vgs is chosen for high 2^{nd} harmonic/DC ratio. In consideration of odd harmonics of LO, the common source point is virtual ground. In consideration of even harmonics, the common source is high resistance. This will degrade the 2^{nd} harmonic as source degeneration. By connected a bypass capacitance, the source degeneration is cancelled and the 2^{nd} harmonic will be enhanced.

Above all, the harmonic generation stage is actually a squaring cell which converts the differential LO voltage to the time-varying current which contains the second harmonic. The fundamental and all odd harmonics of the M_{LO+} and M_{LO-} drain current are cancelled at the connected drain terminal. Fig. 3.4 shows both M_{LO+} and M_{LO-} transistor's drain current and the total current Ihar at the connected point.

3.2.1.1 Define Harmonic/DC Ratio

For quantifying the second harmonic enhancement, we define a harmonic/DC ratio R.

$$R = \frac{I_{2thHarmonic}}{I_{DC}} \tag{3.12}$$

In the same biasing current, operating both M_{LO+} and M_{LO-} in saturation region the harmonic/DC ratio is about 10%. In this work, operating both M_{LO+} and M_{LO-} in switch-like operation point, the harmonic/DC ratio is 34%. It is three times more than former one. The conversion gain will increase greatly with this scheme.

3.2.2 Mixing Stage

In the mixing stage, the differential radio frequency (RF) signal from gate of M_{RF+} and M_{RF-} and the second harmonic from both sources are mixed and the RF signal is down-converted to base-band. In noise analysis, the flicker noise of M_{RF+} and M_{RF-} dominate the output noise power level. From flicker noise equation

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \tag{3.13}$$

$$\approx \frac{K}{f} \cdot \omega_t^2 \cdot A \cdot \Delta f \tag{3.14}$$

From equation (3.13):

$$\overline{i_n^2} = \frac{2KI}{L^2 C_{ox}^2} \cdot \frac{\Delta f}{f} \tag{3.15}$$

Where K is a device-specific constant, f is the frequency, g_m is the trans-conductance of transistor, W/L is transistor's width/length, C_{OX} is the gate capacitance, ω_t is the cut-off frequency, A is the gate area of transistor and I is the DC current of the transistor.

In equation (3.15), it shows that the flicker noise current of transistor is direct proportion to DC current and the inverse of the square of length. Increasing the transistor length and decreasing the bias current of transistor decreases flicker noise. Because that noise figure inverses to conversion gain, the transistor length must be optimized for noise performance. In this work, the length is increase to 0.35 μm for decreasing flicker noise.

The purpose of the injected current is to reduce the biasing current of M_{RF+} and M_{RF-}. In equation (3.15), it reduces the flicker noise of the transistor pair M_{RF+} and M_{RF-}, which is the main noise contributor. The injected current itself will not introduce noise in this balanced structure. Unlike the Gilbert-Cell mixer, the two RF transistors change their current simultaneously and any noise at their common source node will be completely cancelled out at the differential output.

At the same time, the R_L can be increased to raise the mixer conversion gain but not influences output third order inter-modulation interrupt point (OIP_3) too much. Adjust R_L could tune the conversion gain to our prefer value.

3.2.3 Gain Tuning Stage

In the gain tuning stage, the second harmonic current flows through the peaking inductor and the parallel NMOS switch M_{SW}. Reference papers [8] [9] introduce the inductive peaking LNA architecture with high gain benefit.

In this stage, inductive peaking architecture is adopted for higher second harmonic level, and with a parallel switch for gain tuning. As NMOS switch turn off (V_{SW} is connected to ground), the peaking inductor and loading from the other two stages form a third-order filter with peaking effect as shown in Fig. 3.5 (a):

$$V_{peak} = I_{har} \times \frac{1}{s^2 C_R C_P (sL_{peak} \| R_{SW}) + sC_L (sL_{peak} \| R_{SW}) G + s(C_P + C_L) + G} \tag{3.16}$$

if $R_{SW} >> sL_{peak}$ *then*

$$V_{peak} = I_{har} \times \frac{1}{s^3 C_R C_P L_{peak} + s^2 C_L L_{peak} G + s(C_P + C_L) + G} \tag{3.17}$$

Where C_L is the effective load capacitance looking into the harmonic stage, and C_P /G are the effective load capacitance/ admittance looking into the mixing stage. Fig. 3.6 shows the current flowing to mixing stage is amplified by inductive peaking. The peaking frequency is in 5.2GHz and it means the second harmonic signal at 5.2GHz is peaked up maximum when it flows across this stage. In this condition, it's called that

mixer is operating in the high-gain mode. In the high-gain mode, the third-order filter peaking at 5.2GHz makes the frequency response sharper and filters out the higher order harmonics which degrade the output spectra.

As NMOS switch is turn on, the peaking inductor parallel with a small turn-on resistance as showed in Fig. 3.5 (b).

$$V_{peak} = I_{har} \times \frac{1}{s^2 C_R C_P (sL_{peak} \| R_{SW}) + sC_L (sL_{peak} \| R_{SW}) G + s(C_P + C_L) + G} \quad (3.18)$$

$$if \quad R_{SW} \approx 0 \quad then$$

$$V_{peak} = I_{har} \times \frac{1}{s(C_P + C_L) + G} \quad (3.19)$$

When turn-on resistance R_{SW} is small, the term $(sL_{peak} \| R_{sw})$ is nearly zero. The third-order filter turns into a first-order low pass filter (LPF) with a pole at frequency $freq = \frac{G}{2\pi(C_P + C_P)}$, and suppress the second harmonic. It seems that the inductance peaking effect is eliminated by the small resistance. The simulation result of turn-on M_{SW} is showed in Fig. 3.6. The second harmonic will not be peaked across this stage. In this operating condition, the harmonic mixer is working in the low-gain mode.

With the inductance peaking scheme and a parallel switch, the gain tuning stage provides two gain modes in this work. This will ensure the mixer to operate in larger input dynamic range.

3.2.3.1 Quantify the Step Gain

In chapter 3.2.1.2, we define the harmonic/DC ratio. As equation (3.12), this ratio is direct proportion to conversion gain. In gain tuning stage, the gain step is associated with the ratio. With MOS switch turn-on, the second harmonic is suppressed by low-pass filter and the ratio is around 34%. In the other condition, pass though the third order low-pass filter with peaking, the second harmonic is amplified and the ratio is around 96%. This is nearly 2.8 times than former. Assume the impedance looking into mixing stage is constant, the voltage sweep ratio is equal to current sweep ratio. Then the gain step is:

$$Gain \quad step = 20\log\frac{R_2}{R_1} = 20\log 2.8 = 8.9(dB) \tag{3.20}$$

In simulation result, the gain step is 9.3dB. This approaches to the calculation result (3.20).

3.3 Discussion on Simulation and Measurement Result

This section lists the simulation and measure result of the step-gain harmonic mixer. The simulation is done by Agilent advanced Design System (ADS) and post simulation by ADS Momentum.

3.3.1 Measurement Consideration

The measurement of this chip is a question. With the restriction of measurement instruments, some of the data of measure results must be got indirectly. The first is consideration is that while RF signal transfers to base-band, the down-conversion mixer is high impedance in base-band output. Because the base-band circuit such as analog-to-digital converter (ADC) or variable gain amplifier (VGA) is high input impedance, the output of mixer could be design in high impedance for larger conversion gain.

There is a question: the input impedance of the measure instruments is 50Ω. Is it influences the measure results of device-under-test (DUT)? In AC consideration, the large output resistance is parallel with 50Ω, and the effective loading is dominates by instrument loading. It influences the DUT performance greatly.

For measuring the DUT without degrading it, output buffer is added between DUT and instrument. One way is added buffer circuit such as common drain transistor and implements on-chip. Shown in Fig. 3.7, the buffer circuit consuming large current and the input capacitor degrade the DUT input matching greatly by miller-effect. The following question is how to de-embed the testing circuit without adding another buffer circuit?

The measurement way of this chip is added a unit-gain buffer amplifier between DUT and instrument, shown in Fig. 3.8. Because that the DUT output is differential end, a differential-to-single end unit-gain buffer is adopted. Trading off between influence to DUT and thermal noise of resistor, the 8.2KΩ resistor for differential amplifier is adopted. The output of amplifier is series with 49.9Ω for matching with instrument. As shown in Fig. 3.8, the point A is the real output voltage

of the DUT and the measurement result is the point B. The power difference of point A and B is 6dB and we could get the real output results by measurement results.

3.3.2 Chip Implementation

Fig. 3.9 shows the microphotograph of the step-gain harmonic mixer circuit. The circuit is fabricated in the TSMC 0.18um CMOS technology. The die area including bonding pads is 0.906 mm by 0.508 mm. Careful layout is observed in order to maximize performance. The layout is done in a uni-directional fashion, i.e. no signal returns close to it origins, to avoid coupling back to the input. For the layout consideration, the RF-LO ports isolation is the first consideration and places these ports opposite of the chip to improve port-to-port isolation and enhance DC-offset cancellation scheme. The RF port, which the signal level is less than LO port, crosses the IF port vertically and decreases the overlap area to minimize the couple of both ports. The layout is placed symmetrically to minimize the mismatch of the differential signal. In order to minimize the effect of substrate noise on the system, a solid ground plane, constructed using a low resistive metal-1 material, is placed between the signal pads (metal-6 and metal-5) and the substrate.

3.3.3 Simulation and Measurement Result

The simulation and measure result is listed in TABLE I. Though the DC current is 2.2mA, similar to simulation, the conversion gain is -5dB in high gain mode (HGM) and -6.5dB in low gain mode (LGM) which is 23dB and 15dB lower than simulation result in HGM and LGM. The conversion gain and IIP3 are shown in Fig. 3.10 and Fig.3.11. Because of the conversion gain is lower than expect, the IIP3 is large than simulation. The input matching is measured and showed in Fig. 3.12. The solid line is the measured data and dot line is the simulation result. The trouble shooting is described following.

First, the second harmonic of a single LO MOS is lower than simulation as shown in Fig. 3.13(a) and Fig. 3.13(b) as the circuit is connected as Fig. 3.14. Though the parallel 50Ω resistor will degrade the mixer gain performance, we can check the second harmonic of LO in IF port and compare to simulation and find out the reason why conversion second harmonic gain degrades so much. In Fig. 3.13 (b), the second harmonic tone will be set in -27dBm in simulation which is 7dB higher than testing result as the same schematic. That means the second harmonic may be lower than simulation.

TABLE I Simulation and measure result of the first chip

	Simulation Result		Measure Result	
	High Gain Mode	Low Gain Mode	High Gain Mode	Low Gain Mode
Process	0.18u			
S11	< -20 dB		< -15 dB	
DC current	2.6mA		2.2mA	
Conversion Gain	18.0 dB	8.7 dB	-5 dB	-6.5 dB
Noise Figure	16.0 dB	25.7 dB		
IIP3	-3.1 dBm	-5.6 dBm	8 dBm	9 dBm

Focusing on harmonic generation stage, it is combined by current source and switch-like differential pair. Fig. 3.15 shows the in bias point of 0.7V, the biasing MOS is working in saturation region as simulation. As Vbias adding over 0.75V, the biasing MOS will operation in triode region because of the drain voltage is restricted by VLO. From Fig. 3.15, the assumption that the biasing MOS is working in right operation region is well.

The measurement and simulation result of inductive peaking is shown in Fig. 3.16. The testing circuit is connected the same as measurement of conversion gain, and the buffer amplifier is connected. As RF frequency and LO frequency is change the same time. The down conversion IF frequency is located at the same frequency (3MHz). The measure result and simulation in the same frequency band are shown in Fig. 3.16 (a). It shows that the inductive is shift to lower frequency in simulation result, but the discrepancy in 3.9GHz to 6GHz is small. The measurement result seems to be influenced by RF and LO input matching. Fig. 3.16 (b) is the simulation in wider frequency range, and the inductive peaking is clear. It shifts to lower frequency slightly, and don't degrade performance greatly.

To make a conclusion, the inductive peaking is moving to lower frequency because of the board. The switch-like harmonic generation scheme may not take effect as simulation and the second harmonic is much lower than simulation result. This is the reason why conversion gain is much lower than we except.

3.4 Conclusion

It seems that inductive peaking for gain tuning takes effect well. As the second harmonic is less than expected. The conversion gain is lower than simulation result. It

looks like that the differential pair working between cut-off and triode region may generate lower second harmonic than expected. The phase and amplitude of differential LO input degrade the odd harmonic cancellation largely.

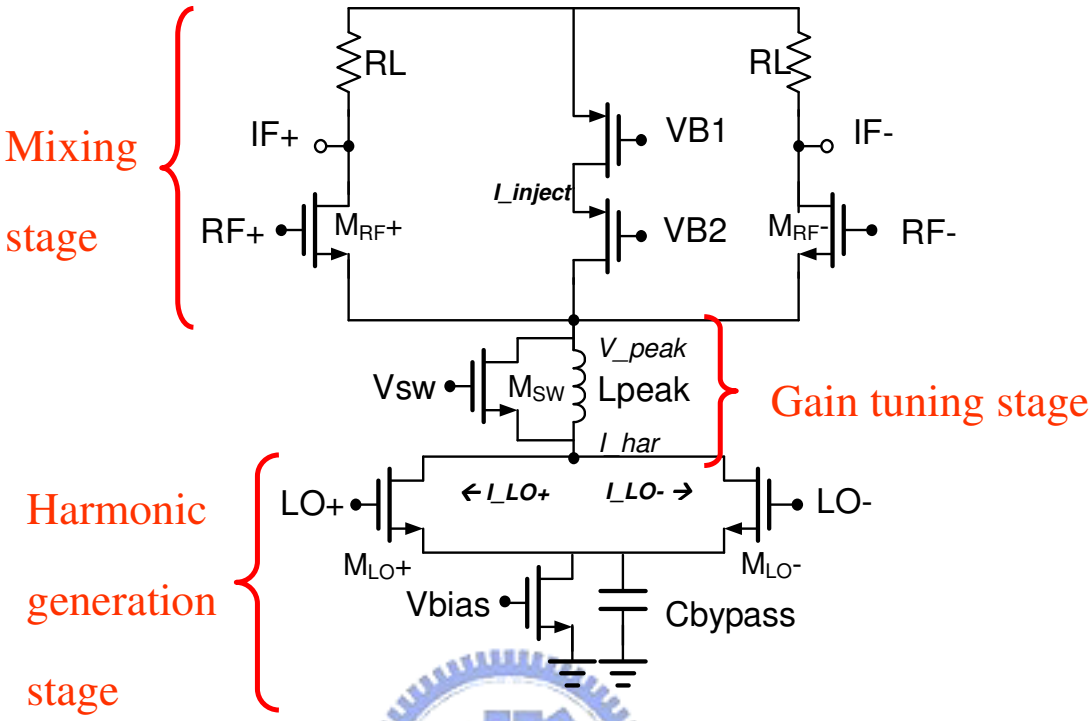


Figure 3.1 CMOS harmonic mixer with current injection

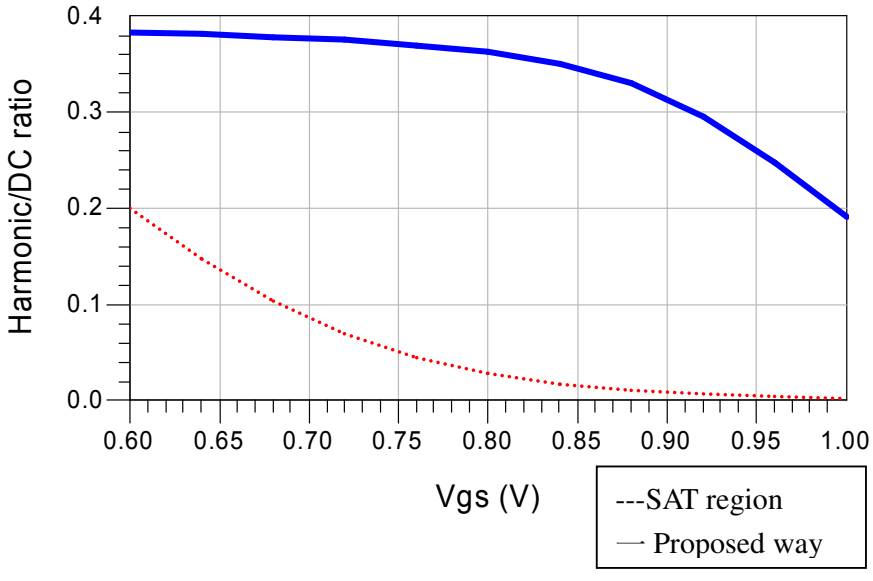


Figure 3.2 The 2nd harmonic/DC ratio of a single MOS with Vds=1V

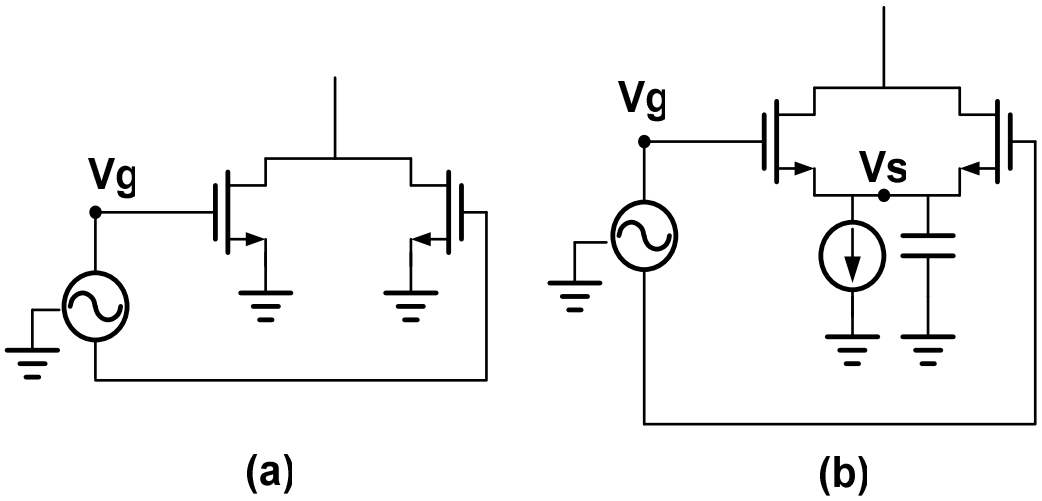


Figure 3.3 Harmonic generation stage (a) without current source (b) with current source

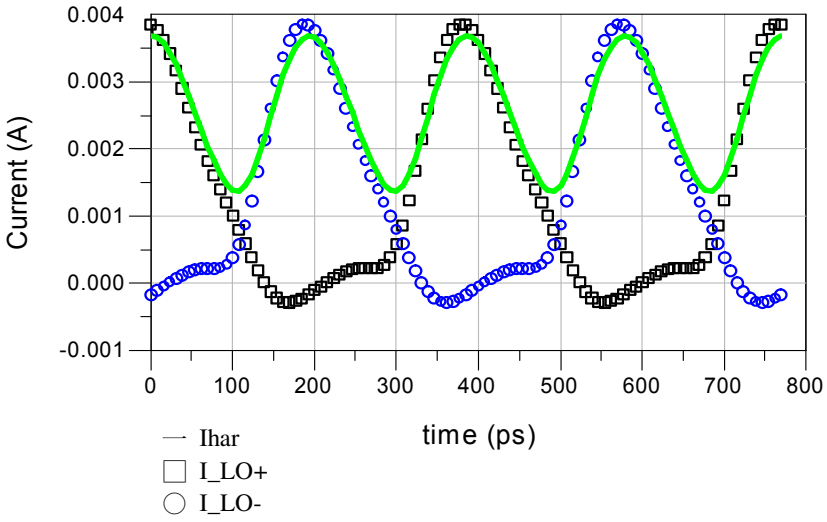


Figure 3.4 Harmonic generation stage current

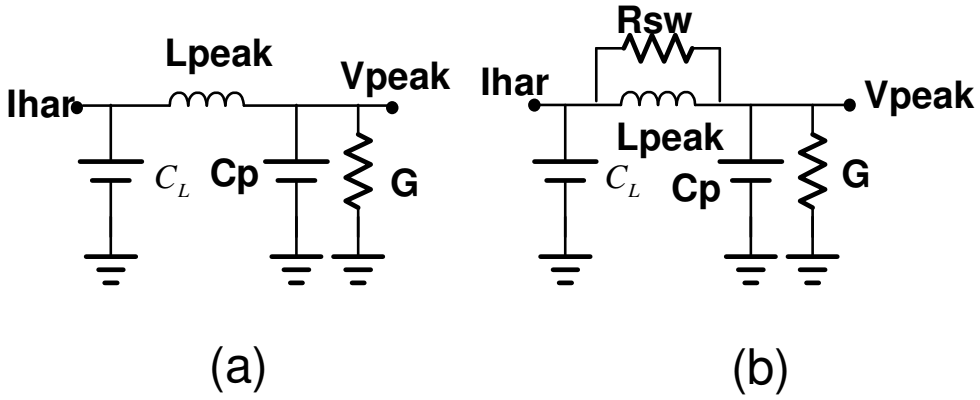


Figure 3.5 Small signal model of peaking inductor and parallel NMOS switch
(a) switch off (b) switch on

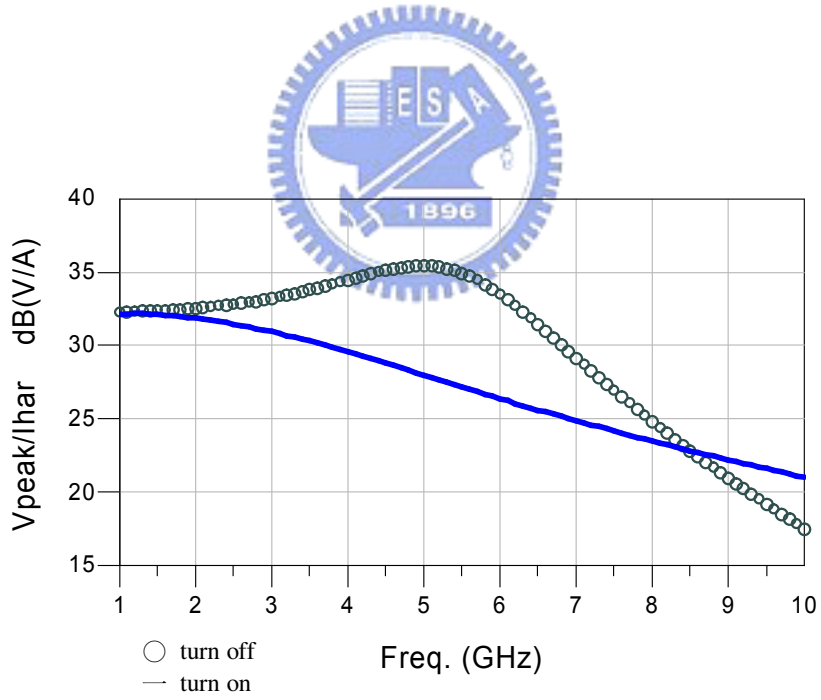


Figure 3.6 Inductance peaking effect (V_{peak}/I_{har})

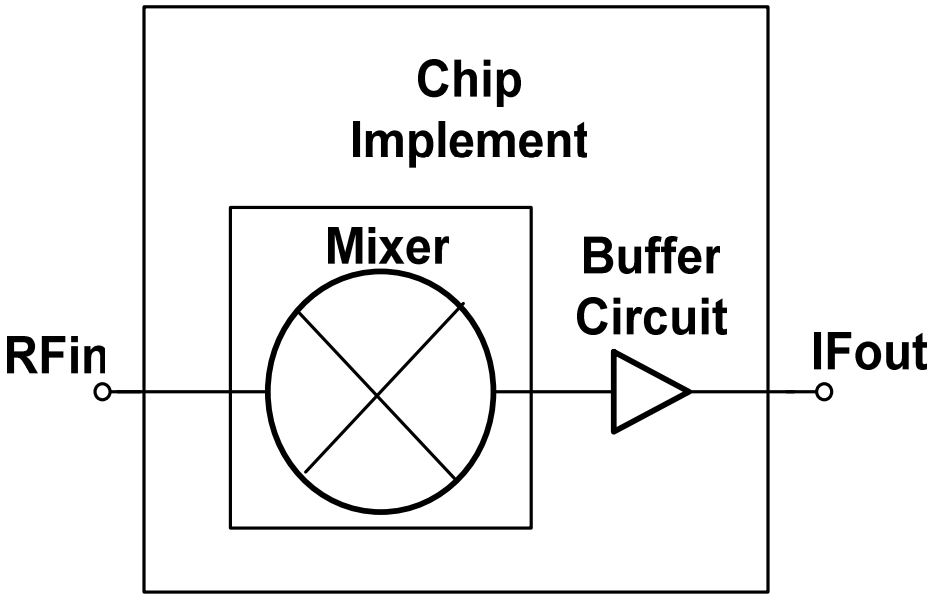


Figure 3.7 Implement buffer in chip

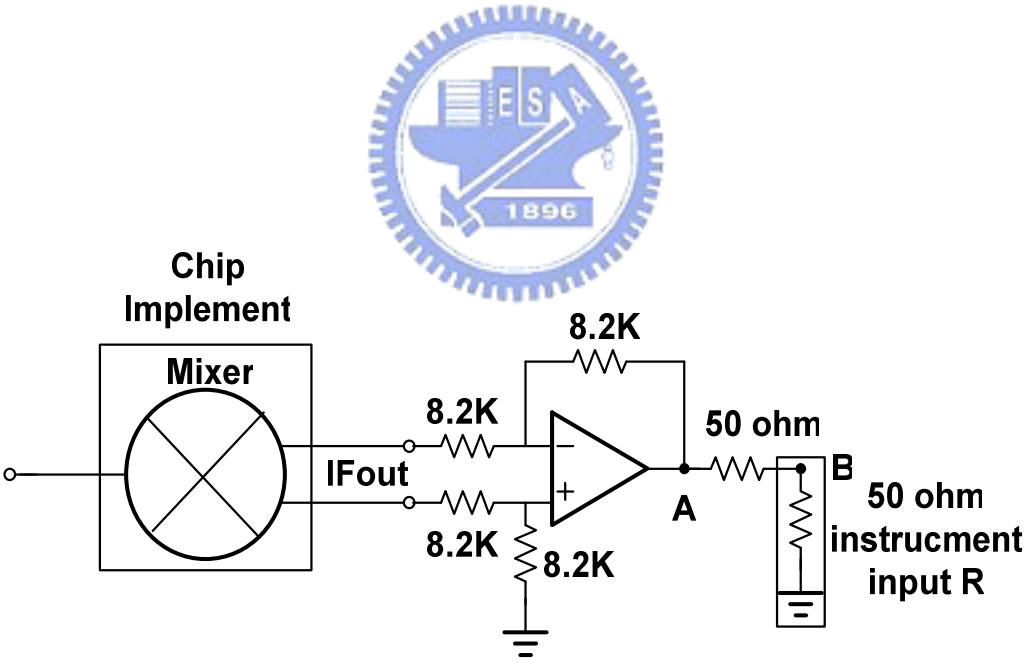


Figure 3.8 testing circuit

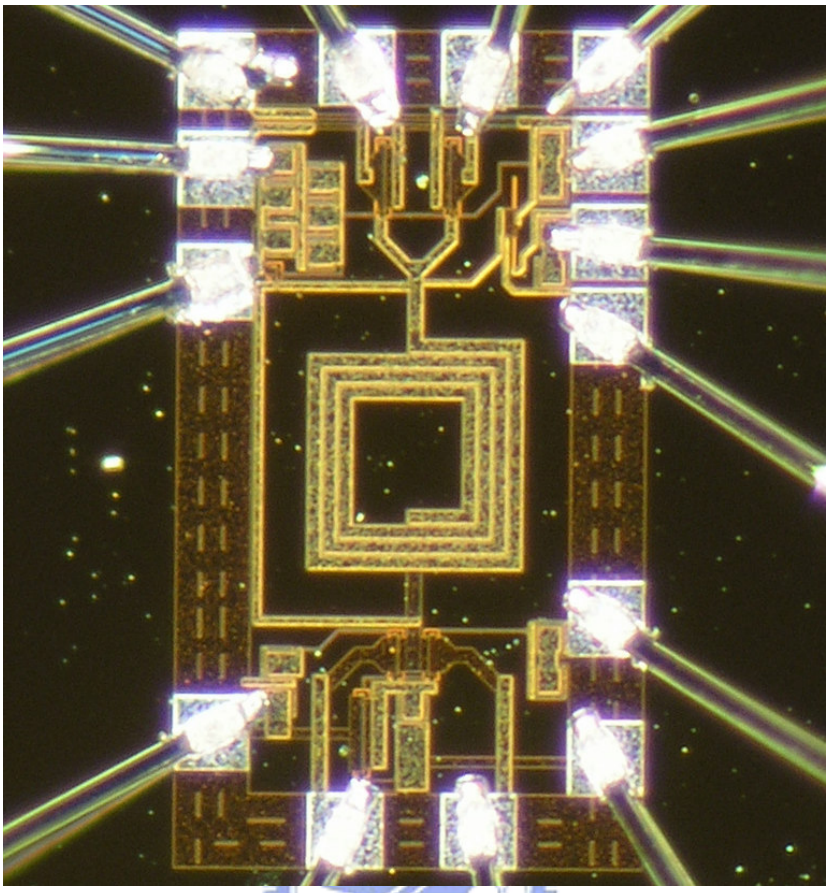


Figure 3.9 Microphoto of chip on board

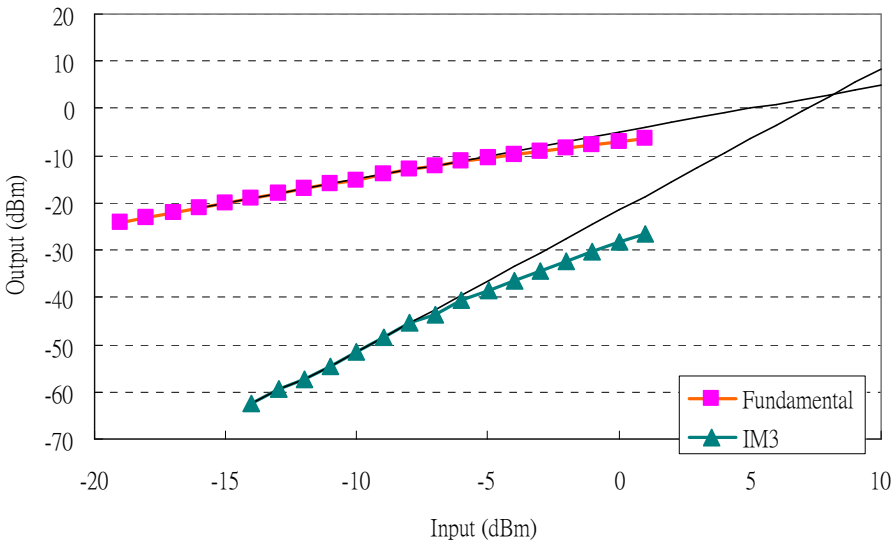


Figure 3.10 Conversion gain and IIP3 in HGM

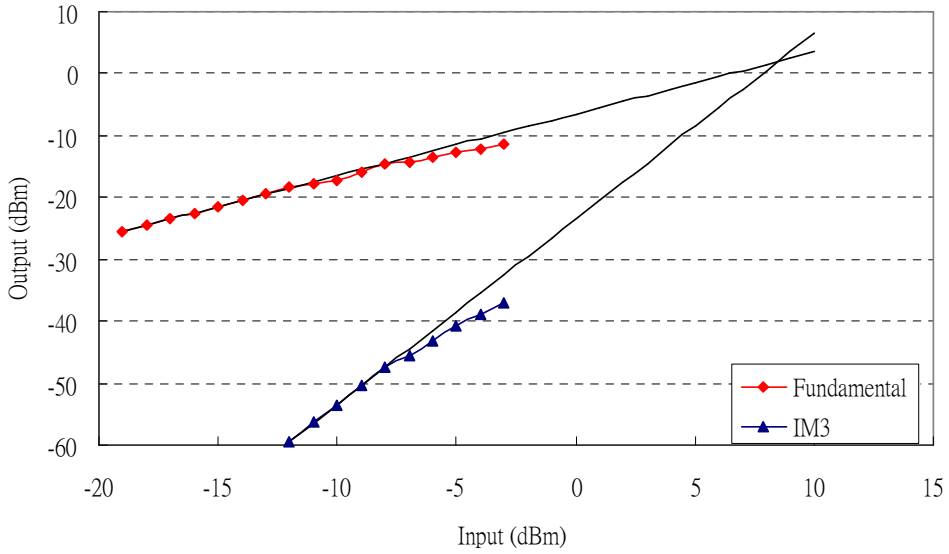


Figure 3.11 Conversion gain and IIP3 in LGM

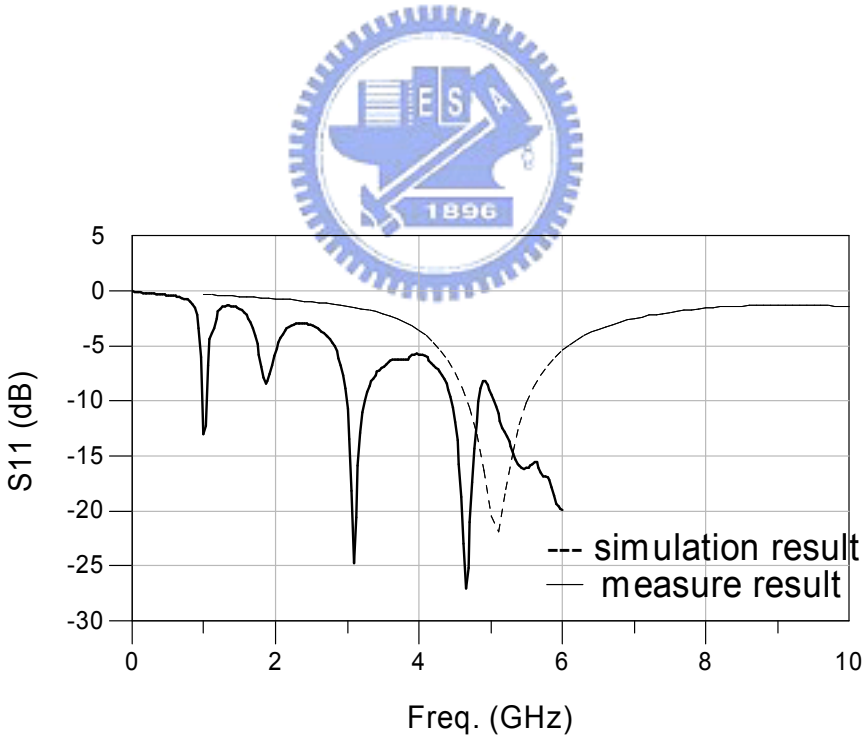


Figure 3.12 Simulation and measure result of S11

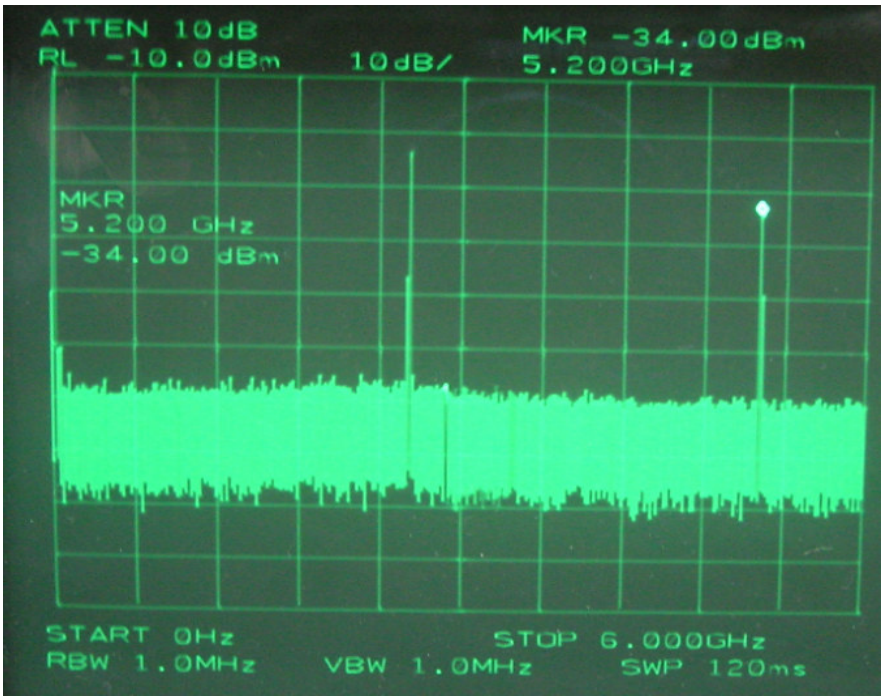


Figure 3.13 (a) Spectra in IF+

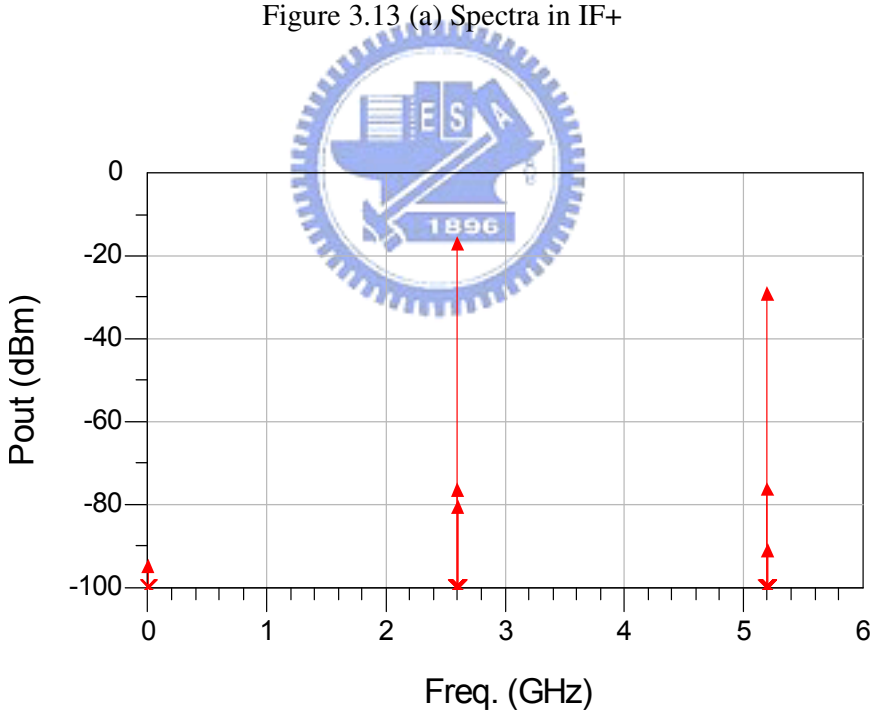


Figure 3.13 (b) Simulation Result in IF+

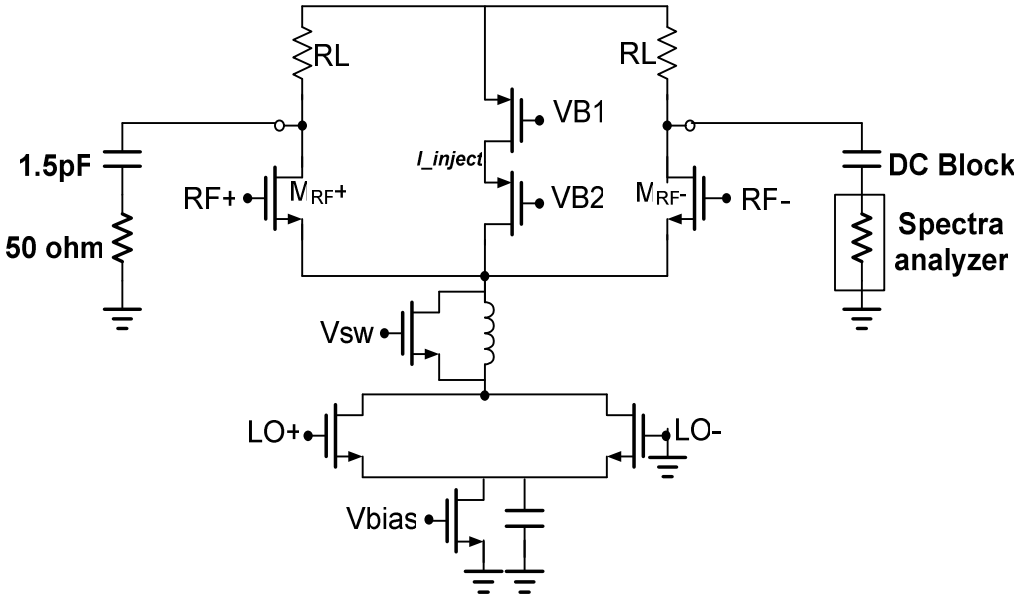


Figure 3.14 Harmonic testing of IF port

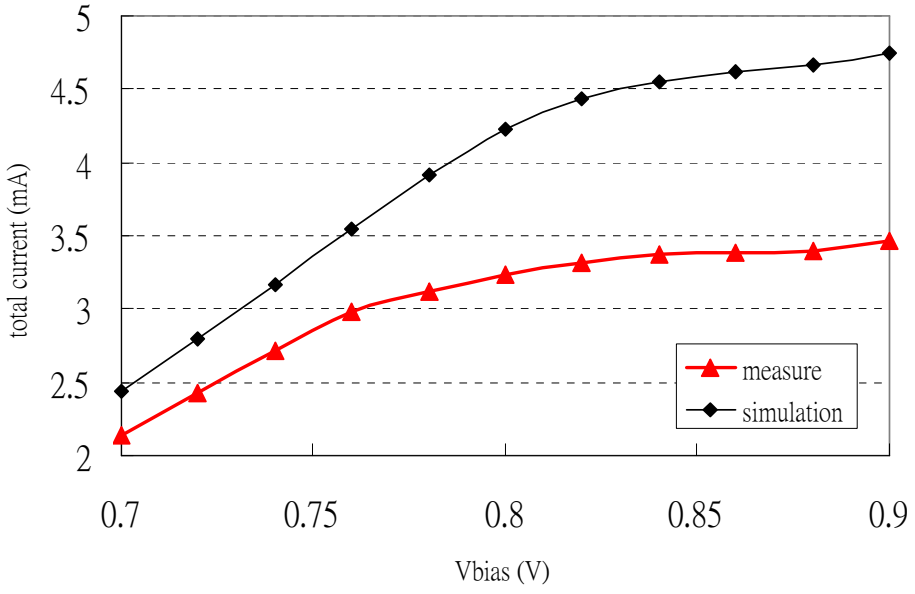


Figure 3.15 The bias current v.s bias voltage

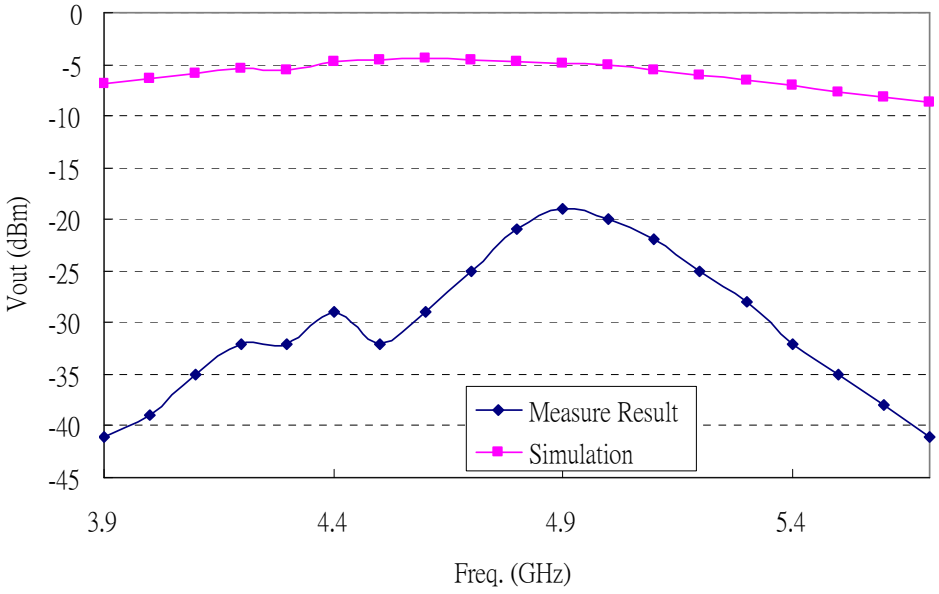


Figure 3.16 (a) Measurement of inductive peaking

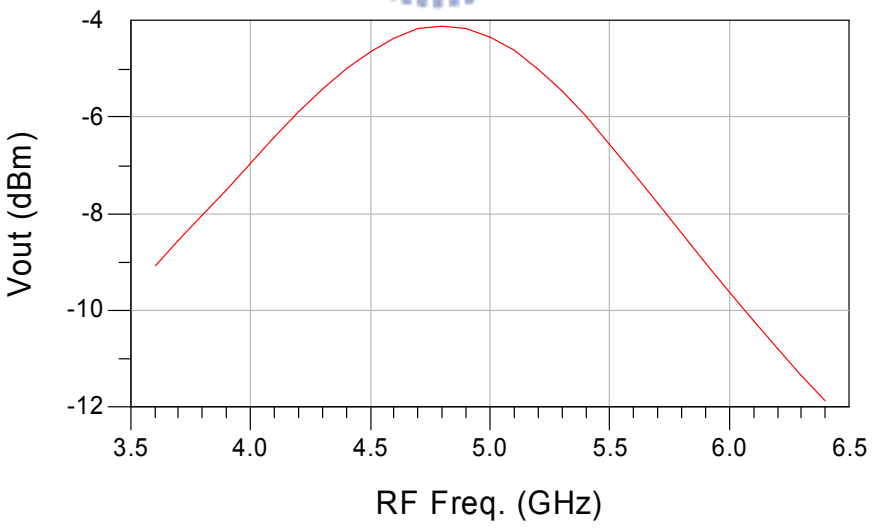


Figure 3.16 (b) Simulation of inductive peaking

Chapter 4

A 2.45/5.2GHz Dual-Band Low-Power Direct-Conversion Harmonic Mixer

4.1 Motivation

Multi-standard radio-frequency (RF) receivers are predicted to play a critical role in wireless communications in the 900-5200MHz range. With cellular and cordless phone standards operating in the 900MHz and 1.8GHz band, the Global Positioning System (GPS) in the 1.5GHz band, and wireless local area networks (WLAN) 802.11b in the 2.4GHz band and 802.11a in 5.2GHz band, it is desirable to combine two or more standards in one mobile unit [10].

The wireless communication specifications 802.11a and 802.11 utilizing different frequency could be merged in single front-end and share a single digital signal processor. In this chapter, a 2.45GHz/5.2GHz dual-band, low-power direct-conversion harmonic mixer is designed and manufactured in tsmc 0.18 μm CMOS process.

4.2 Design Consideration

Fig. 4.1 shows the conceptual example of a dual-band receiver. The receiver contains two antennas, two LNAs and two mixers. Thought the radio-frequency (RF) front-end contains two independent paths, the analog circuit and digital signal processor (DSP) could be combined and decreases the power consumption and cost. In recently research, the dual-band RF front-end is implemented in a single path (Fig. 4.2). The dual-band LNA is designed for both bands and amplifies both signals concurrent. In most operation condition, only one of the bands receives RF signal and the other signal path is unused. That means the mixer must design with concurrent input matching and only one of the bands will be transferred to output. With this conception, this mixer is designed in concurrent dual-band input matching and down-converting one of the receiving band to base-band which system needs. The conception of Fig. 4.2 will be implemented with this mixer, and the RF front-end circuit could be designed in a single path.

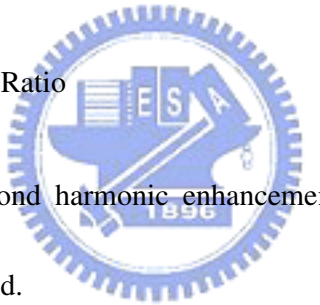
4.3 Analysis of the Dual-Band Low-Power Harmonic Mixer

The CMOS dual-band harmonic mixer is shown in Fig. 4.3 This harmonic mixer is composed of three parts: (1) harmonic generation stage; (2) mixing stage, and (3)

frequency tuning stage.

4.3.1 Harmonic Generation Stage

The harmonic generation stage is following section 3.2.1. For low power design, the biasing current is set as half of former design. By a current source, the Vgs of LO MOS is restricted in lower voltage for higher second harmonic.



4.3.1.1 Define Harmonic/DC Ratio

For quantifying the second harmonic enhancement, the harmonic/DC ratio R (3.12) in section 3.2.1.1 is used.

In the same biasing current, operating both M_{LO+} and M_{LO-} in saturation region the harmonic/DC ratio is about 10%. In this work, operating both M_{LO+} and M_{LO-} in switch-like operation point, the harmonic/DC ratio is 35%. It is three times more than former one. The conversion gain will increase greatly with this scheme.

4.3.2 Mixing Stage

The design of this stage is following as section 3.2.2. The bias current flowing to

both RF MOS is set similar as former for linearity consideration. That means, the injection current is lower than former.

4.3.3 Frequency Tuning Stage

In the frequency tuning stage, the second harmonic current flows through the peaking inductor and the parallel NMOS switch M_{SW} . Reference papers [8] [9] introduce the inductive peaking LNA architecture with high gain benefit.

In this stage, inductive peaking architecture is adopted for higher second harmonic level, and with a parallel switch for frequency tuning. As NMOS switch turn off (V_{SW} is connected to ground), the second harmonic of LO will flow into inductor L1+L2. As shown in Fig. 4.4 (a), the inductor and loading from the other two stages form a third-order filter with peaking effect. As equation (4.2), the large inductance L1+L2 will form a third order low-pass-filter with peaking frequency in lower frequency. It means that the mixer is operating in low frequency mode. As shown in Fig. 4.5 dot line, all of the frequency except frequency near 3GHz will be filtered out by frequency selection effect, and only low-side band of RF input will down-convert to base-band.

$$V_{peak} = I_{har} \times \frac{1}{s^2 C_R C_P (sL_1 + (sL_2 \| R_{SW})) + sC_L (sL_1 + (sL_2 \| R_{SW}))G + s(C_P + C_L) + G} \tag{4.1}$$

if $R_{SW} >> sL_2$ *then*

$$V_{peak} = I_{har} \times \frac{1}{s^3 C_R C_P (L_1 + L_2) + s^2 C_L (L_1 + L_2)G + s(C_P + C_L) + G} \tag{4.2}$$

Where C_L is the effective load capacitance looking into the harmonic stage, and C_P/G are the effective load capacitance/admittance looking into the mixing stage.

As NMOS switch turns on, the peaking inductor L2 parallel with a small turn-on resistance as shown in Fig. 4.4 (b). The small signal equation will be:

$$V_{peak} = I_{har} \times \frac{1}{s^2 C_R C_P (sL_1 + (sL_2 \| R_{SW})) + sC_L (sL_1 + (sL_2 \| R_{SW}))G + s(C_P + C_L) + G} \tag{4.3}$$

if $R_{SW} \approx 0$ *then*

$$V_{peak} = I_{har} \times \frac{1}{s^3 C_R C_P L_1 + s^2 C_L L_1 G + s(C_P + C_L) + G} \tag{4.4}$$

When turn-on resistance R_{SW} is small, the term $(sL_2 \| R_{sw})$ is nearly zero. The third-order filter will be peaked by inductor L1 and the peaking frequency will be in higher frequency than that in switch off. As shown in Fig 4.5 solid line, the band-pass -filter will filter out all frequency except frequency near 5.2GHz, and only up-side band of RF input will down-convert to base-band. In this operation mode, the mixer is

working in high frequency mode.

With the inductance peaking scheme and a parallel switch, the frequency tuning stage provides two frequency modes in this work. By frequency selection of the inductive peaking effect, the mixer decides one of the RF input band will be transferred to base-band. By this mixer, the conception of Fig. 4.2 will be implemented.

4.3.3.1 Quantitate the Gain Enhancement

In chapter 3.2.1.2, we define the harmonic/DC ratio. As equation (3.12), this ratio is direct proportion to conversion gain. In gain tuning stage, the gain step is associated with the ratio. With MOS switch turn-on, the third-order low-pass filter will be peaked in 2.45GHz, the second harmonic of 1.225GHz LO frequency. The second harmonic of 1.225GHz is peaked by low-pass filter and the ratio is around 89%. This is nearly 2.5 times than former without inductive peaking. In the other condition, pass though the third order low-pass filter which is peaked in 5.2GHz, the second harmonic of 2.6GHz LO frequency is amplified and the ratio is around 96%. This is nearly 2.7 times than that without inductive peaking.

4.4 Simulation and Measure Result

This section describes the simulation and measure result of the step-gain harmonic mixer. The pre-simulation is done by Agilent advanced Design System (ADS) and post EM-simulation is done by ADS Momentum.

4.4.1 Chip Implementation

Fig. 4.6 shows the microphotograph of the dual-band harmonic mixer circuit. The circuit is fabricated in the TSMC 0.18um CMOS technology. The die area including bonding pads is 0.795mm * 0.683mm. Careful layout is observed in order to maximize performance. The layout is done in a uni-directional fashion, i.e. no signal returns close to it origins, to avoid coupling back to the input. For the layout consideration, the RF-LO ports isolation is the first consideration and places these ports opposite of the chip to improve port-to-port isolation and enhance DC-offset cancellation scheme. The RF port, which the signal level is less than LO port, crosses the IF port vertically and decreases the overlap area to minimize the couple of both ports. The layout is placed symmetrically to minimize the mismatch of the differential signal. In order to minimize the effect of substrate noise on the system, a solid ground plane, constructed using a low resistive metal-1 material, is placed between the signal pads (metal-6 and metal-5) and the substrate.

4.4.2 Simulation and Measurement Result

The simulation and measure result is listed in TABLE II. Because the 1.225GHz balun is unavailable, we can not measure the 2.45GHz band now. Though the DC current is similar to simulation, the conversion gain is 39dB lower than simulation result. The conversion gain and IIP3 plot is showed in Fig. 4.7. Because most of IM3 is under noise floor, the IIP3 is gained by equation (4.5).

$$IIP3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm} \tag{4.5}$$

Because that the harmonic generation stage is the same with former, the lower second harmonic is poor to driver RF MOS. With injection current nearly to zero, the conversion gain is negative. The 5.2GHz input matching is measured and showed in Fig. 4.8. Because that the input balun is narrow band, the input matching is measured separately. The solid line is the measured data and dot line is the simulation result.

TABLE II Simulation result and measure result of the second chip

	Simulation Result		Measure Result	
Band	2.45GHz	5.2GHz	2.7 GHz	5.2GHz
DC current	1.28 mA		1.15 mA	
S11	< -11 dB	< -12 dB	-12 dB	-13 dB
Conversion Gain	16.7 dB	18.9 dB		-21 dB
Noise Figure	15.5 dB	13.5 dB		
IIP3	-6.0 dBm	-1 dBm		18 dBm

The measurement result of inductive peaking is shown in Fig.4.9. The testing circuit is connected the same as measurement of conversion gain, and the buffer amplifier is connected. As RF frequency and LO frequency is change the same time. The down conversion IF frequency is located at the same frequency (3MHz). The

peaking frequency shifts to lower frequency as plot.

4.5 Conclusion

As showed in chapter 3, the differential pair working between cut-off and triode region may generate lower second harmonic than expected. In this work, the lower injection current for current reusable let the harmonic/DC ratio too low to drive the RF MOS and the inductive peaking is moving to low frequency. It makes the conversion gain is degraded substantially.

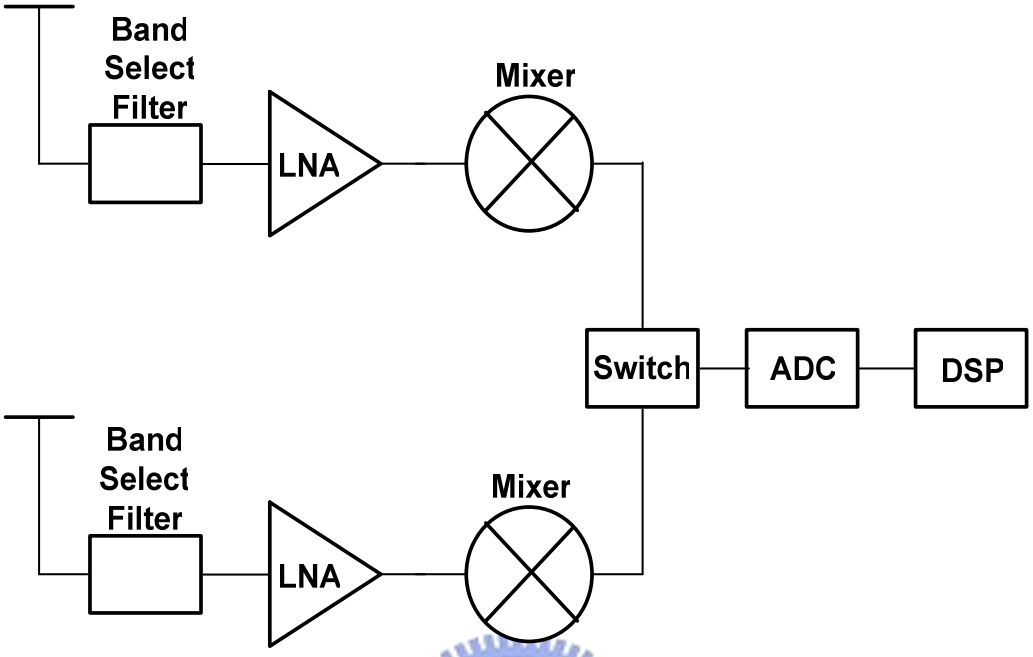


Figure 4.1 Conceptual example of a dual-band receiver

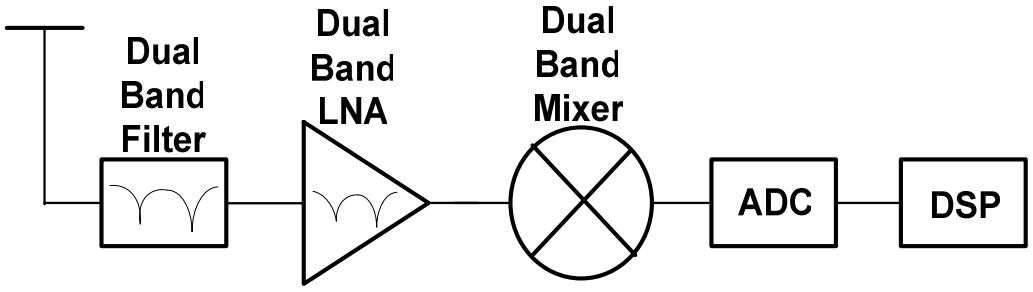


Figure 4.2 Conceptual example of a concurrent dual-band receiver

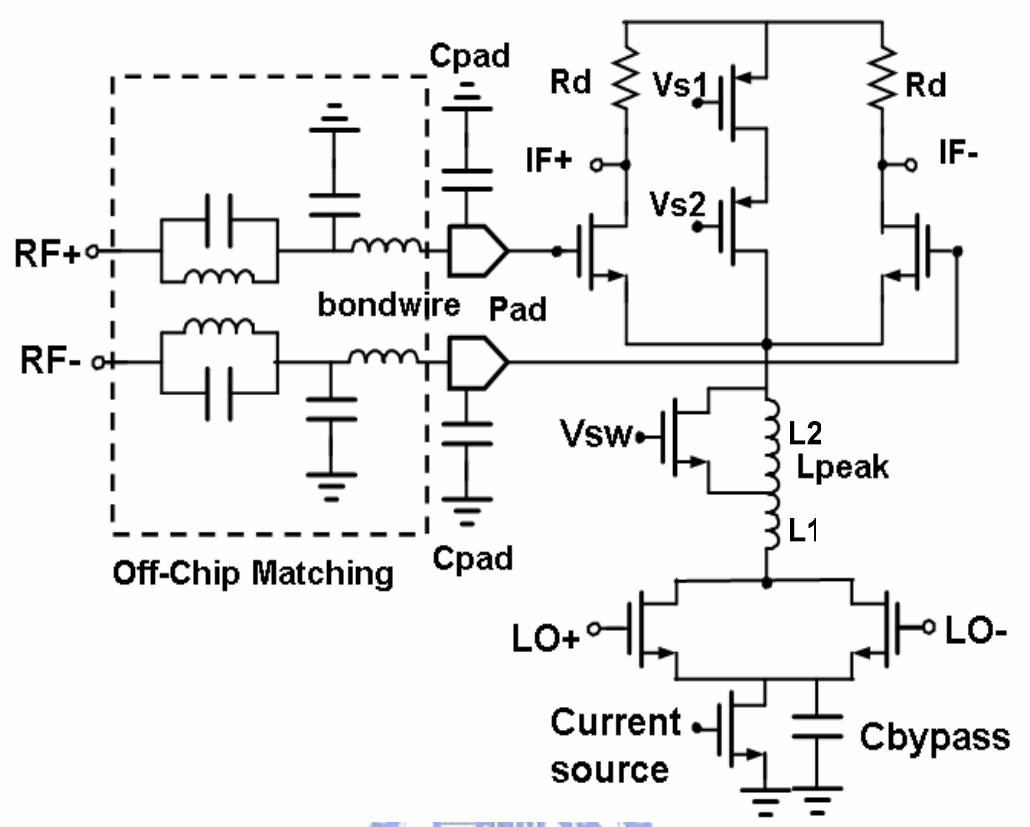


Figure 4.3 Dual-band low-power harmonic mixer

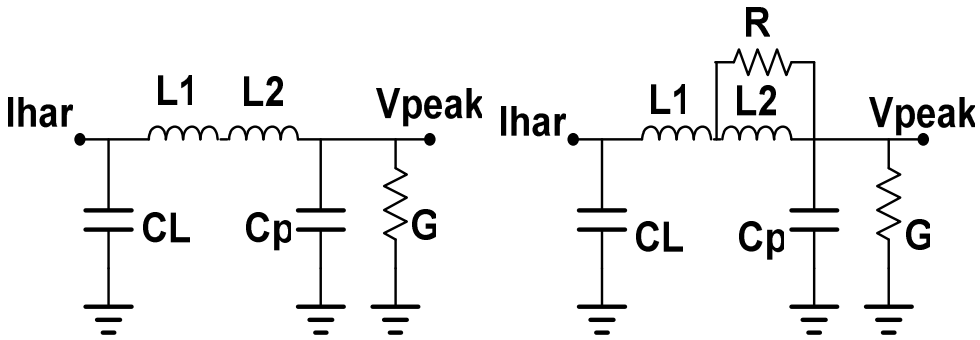


Figure 4.4 Small signal model of peaking inductor and parallel NMOS switch

(a) switch off (b) switch on

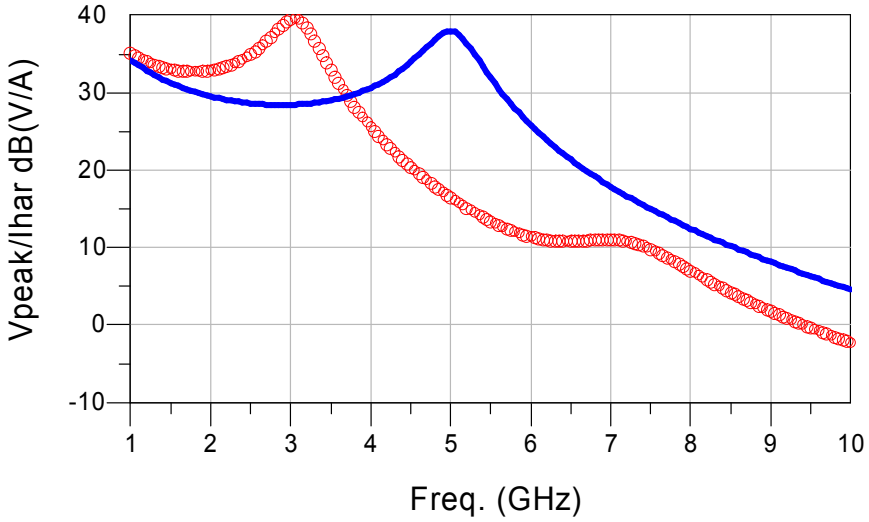


Figure 4.5 Inductance peaking effect (V_{peak}/I_{har})

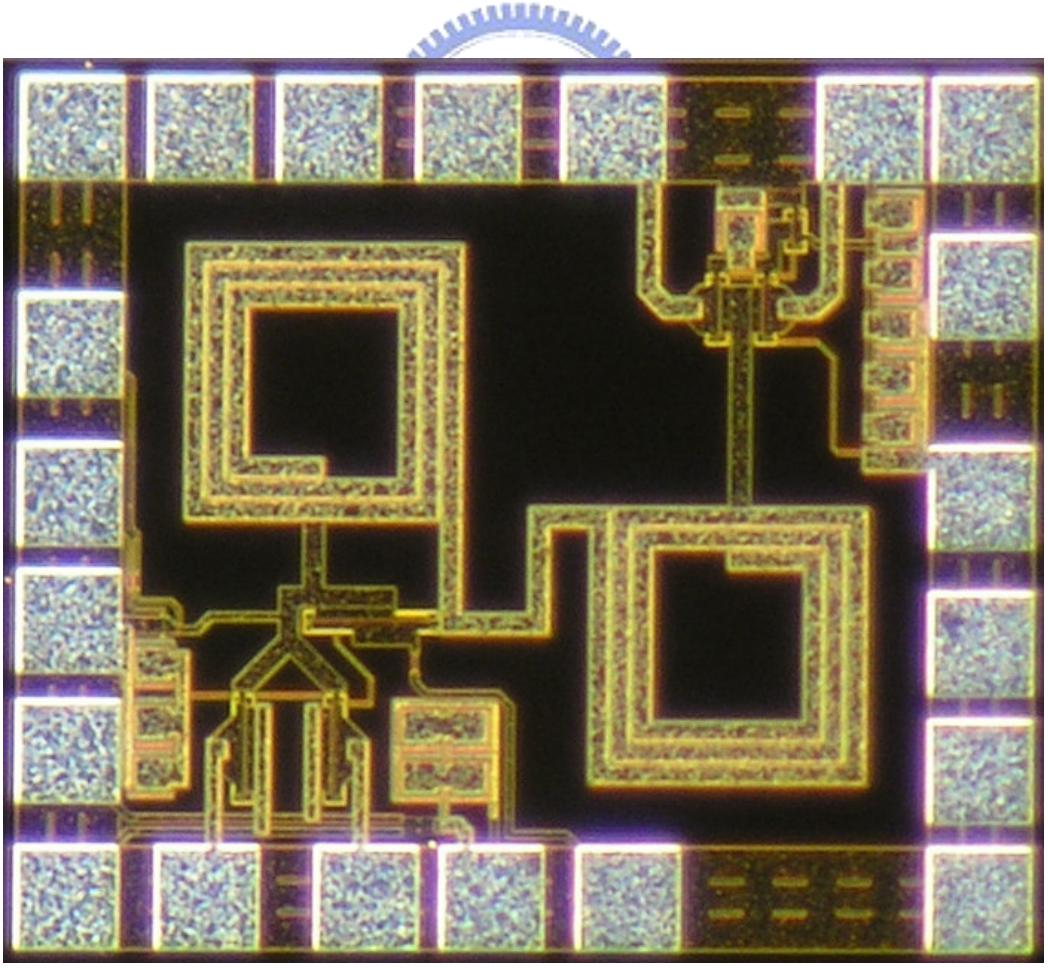


Figure 4.6 Chip implement

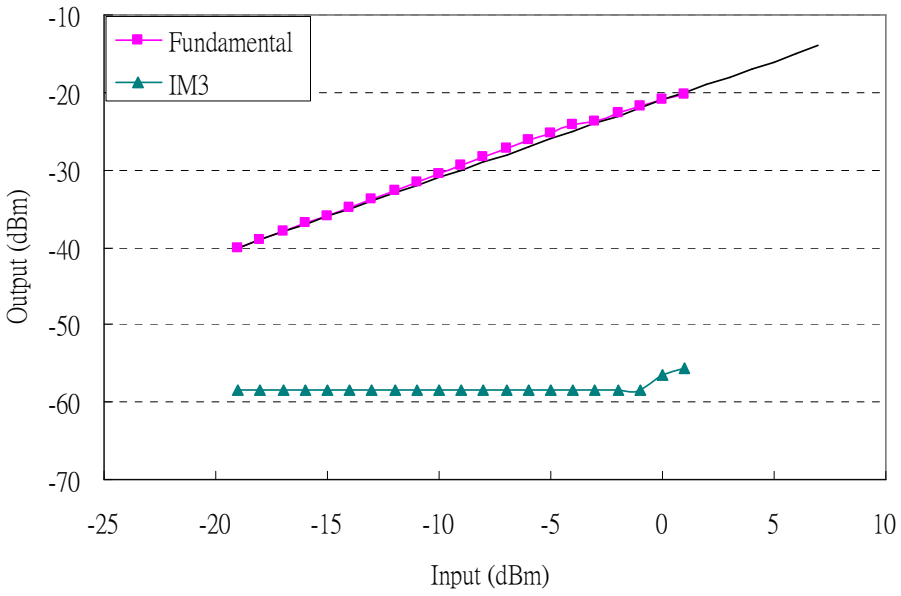


Fig 4.7 Conversion Gain and IIP3

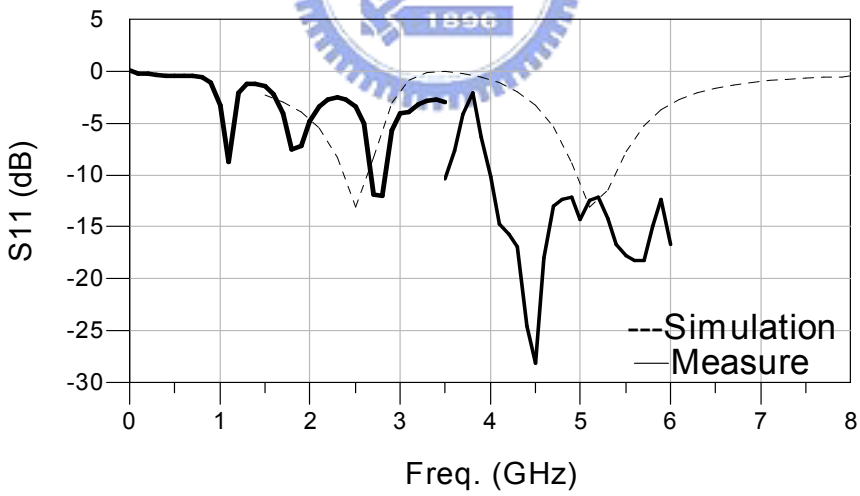


Figure 4.8 Input matching in 5.2GHz band

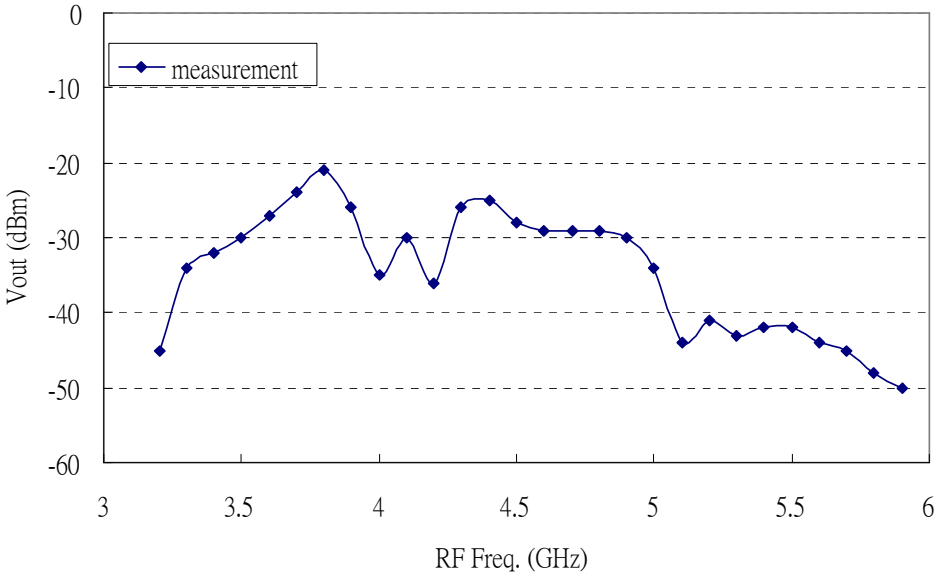


Figure 4.9 Measurement result inductive peaking in 5.2GHz band

Chapter 5

Summary and Future Works

5.1 Summary

In the chapter 2, the DC-offset of direct-conversion, heterodyne and low IF receivers are presented. The DC-offset issue is an intrinsic problem of direct-conversion receiver because of frequency planning. In the last of chapter 2, the harmonic mixer is mentioned and it seems a way to solve this issue. Besides the DC-offset consideration, two harmonic mixers are introduced. The RF signal is mixing with the second harmonic of LO signal. Both of they are influenced by low linearity.

In the chapter 3, a step-gain harmonic mixer using inductive peaking scheme and switch-like harmonic generation stage is analyzed and implemented in a standard 0.18um CMOS process. Although, measured result show that the conversion gain is lower than simulation, the switch-able inductance peaking scheme for step-gain takes effect as simulation. The trouble shooting is showed in last of chapter 3. Measured data still show that the mixer achieves -15 dB input return loss (S11), while consuming 2.2mA DC current.

In the chapter 4, a dual-band low-power harmonic mixer, intended for use in the receiver path of 802.11a/b system is designed in a standard 0.18um CMOS process. With the same harmonic generation stage as former, the conversion gain is less than simulation result.

5.2 Future Works

Although some measure results are showed in this thesis, the measurement and trouble shooting of these chips still continues. The drilled PCB board introduces some problem such as leakage and signal loss. Since the bias voltage is fed by a large resistance as RF choke, any leakage will degrade the bias voltage. It should be considered to seek a proper PCB board for testing.

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