國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

應用於六百億赫茲通訊系統的毫米波互補式金氧半電路分析與設計

The Analysis and Design of Millimeter-Wave CMOS Circuits for 60-GHz Communication Systems

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中華民國九十七年十月

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摘 要

本篇論文主要闡述了適用於60GHz低功率通訊系統的毫米波互補式金氧半電路其設計方法及製作技術。論文中包含下列三個部分：(1)次諧波注入鎖住式三倍頻器的分析、模型建立與設計方法；(2)整合注入鎖住式頻率倍乘器的60GHz鎖相迴路電路分析及設計；(3)整合注入鎖住式三倍頻器的60GHz直接降頻接收機的設計。

首先，本論文提出以及分析一個具有差動輸出的互補式金氧半次諧波注入鎖住式三倍頻器，並且設計使其適用於*K*頻段和*V*頻段。根據所提出的次諧波注入鎖住式三倍頻器的架構，發展出鎖頻範圍及輸出相位雜訊的模型。*K*頻段的注入鎖住式三倍頻器採用了0.18微米互補式金氧半製程設計與製作。由量測結果可知：當功率消耗為0.45毫瓦特和輸入功率為4dBm時，鎖頻範圍為1092MHz；輸出的三階諧波對於一階、二階、四階及五階的諧波抑制比分別為22.65、30.58、29.29及40.35分貝；當使用可變電容及增加功率消耗到2.95毫瓦特時，*K*頻段的注入鎖住式三倍頻器鎖頻範圍可達到3915MHz。另外設計了採用0.13微米互補式金氧半製程的*V*頻段的注入鎖住式三倍頻器。量測結果顯示：當功率消耗為1.86毫瓦特和輸入功率為6dBm時，鎖頻範圍為1422MHz。可以發現到此次所提出的注入鎖住式三倍頻器，其鎖頻範圍與傳統利用可變電容來調整輸出頻率的壓控振盪器是相似的。

其次，本論文提出了一個能夠產生60GHz輸出的整合注入鎖住式頻率倍乘器之鎖相迴路。此60GHz鎖相迴路整合了壓控振盪器、注入鎖住式頻率倍乘器、除32的頻率除法器、相位頻率偵測器、電荷幫浦和迴路濾波器。因為所提出的注入鎖住式頻率倍乘器能夠產生壓控振盪器的五階諧波訊號，所以壓控振盪器僅需工作在所需要頻率的五分之一。此鎖相迴路採用了0.18微米互補式金氧半製程設計與製造。由量測結果可得：鎖相迴路輸出頻率為53.04到58.0GHz及輸出功率為–37.85dBm，相位雜訊在1MHz及10MHz偏移量下每赫茲分別較主訊號低85.2及90.9分貝，參考突波訊號較主訊號低65分貝。在1.8伏特的電壓工作下，其電路功率消耗為35.7毫瓦特。整個鎖相迴路的晶片面積為0.96×0.84平方毫米。

最後，本論文提出一個應用於60-GHz頻段且整合次諧波注入鎖住式三倍頻器的直接降頻接收機。本論文提出的直接降頻接收機包含了低雜訊放大器、四相位降頻混頻器、一個20-GHz的四相位壓控振盪器、兩個次諧波注入鎖住式三倍頻器、兩個中頻放大器以及兩個輸出緩衝級。在這個接收機中，本地振盪器的訊號是經由一個操作在三分之一載波的四相位壓控振盪器串接兩個次諧波注入鎖住式三倍頻器來提供。由於四相位壓控振盪器的頻率偏移，所以產生的本地振盪器訊號最高頻率只有55.03GHz。在以射頻訊號55.03GHz以及中頻訊號100MHz時的量測結果可知：接收機的增益為18.2分貝、雜訊指數16.96分貝、增益1分貝壓縮點在輸入端為–17.0dBm、三階互調失真點為–7.6dBm。本論文提出的接收機是使用0.13微米的互補式金氧半製程所製作。在供應電壓1.2伏特時的總功率消耗為31.0毫瓦特，整個直接降頻接收機的晶片面積為1.21×1.03平方毫米。

經由模擬以及量測結果可以證實，本論文所提出的注入鎖住式三倍頻器可適用於低功率高性能工作在毫米波頻段的收發機。在未來中，更進階的研究將可以整合低功率的單一晶片收發機以及頻率合成器。

The Analysis and Design of Millimeter-Wave CMOS Circuits for 60-GHz Communication Systems

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ABSTRACT

In this thesis, the design methodologies and implementations of millimeter-wave CMOS circuit for 60-GHz low-power communication system are presented. There are three parts: (1) the analysis, modeling, and design of the subharmonic injection-locked frequency tripler (ILFT); (2) the analysis and design of 60-GHz phase-locked loop (PLL) integrated with injection-locked frequency multiplier (ILFM); and (3) the design of 60-GHz direct-conversion receiver integrated with ILFT.

At first, *K*-band and *V*-band CMOS differential subharmonic ILFTs are proposed, analyzed, and designed. Based on the proposed ILFT structure, models for the locking range and the output phase noise are developed. A *K*-band ILFT is designed and fabricated using 0.18-μm CMOS technology. The measured locking range is 1092 MHz with a dc power consumption of 0.45 mW and an input power of 4 dBm. The harmonic rejection-ratios are 22.65, 30.58, 29.29, 40.35 dBc for the first, second, fourth, and fifth harmonics, respectively. The total locking range of the *K*-band ILFT can achieve 3915 MHz when the varactors are used and the dc power consumption is increased to 2.95

mW. A *V*-band ILFT is also designed and fabricated using 0.13-μm CMOS technology. The measured locking range is 1422 MHz with 1.86-mW dc power consumption and 6-dBm input power. It can be seen that the locking range of the proposed ILFT is similar to the tuning range of a conventional varactor-tuned bulk-CMOS voltage-controlled oscillator (VCO).

Secondly, a novel CMOS PLL integrated with ILFM that generates the 60-GHz output signal is proposed. The proposed 60-GHz PLL is composed of VCO, ILFM, 1/32 frequency divider, phase/frequency detector, charge pump, and loop filter. Because the proposed ILFM can generate the fifth-order harmonic frequency of VCO output, the operational frequency of the VCO can be reduced to only one-fifth of the desired frequency. The PLL is designed and fabricated in 0.18-μm CMOS technology. The output frequency range of the proposed PLL is from 53.04 GHz to 58.0 GHz with output power of –37.85 dBm. The measured phase noises at 1 MHz and 10 MHz offset from the carrier are –85.2 and –90.9 dBc/Hz, respectively. The reference spur level of –40.16 dBc is measured. The dc power dissipation of the fabricated PLL is 35.7 mW under a 1.8-V supply. The chip area including pads is 0.96 mm × 0.84 mm.

Finally, a 60-GHz direct-conversion receiver integrated with ILFT is proposed. The proposed direct-conversion receiver front-end is composed of a low-noise amplifier (LNA), I/Q quadrature down-conversion mixers, a 20-GHz QVCO, two ILFTs, two IF amplifiers, and two output buffers. In the proposed receiver, the local oscillator (LO) signals are generated by QVCO operated at only one-third of carrier frequency cascade with the two ILFTs. Due to the frequency shift of QVCO, the maximum RF frequency is only 55.03 GHz. The measured results show a receiver gain of 18.2 dB, a noise figure of 16.96 dB with RF frequency of 55.03 GHz and IF frequency of 100 MHz, channel bandwidth of 2 GHz with LO frequency of 55.02 GHz, an input-referred 1-dB compression point (P1dB) of –17.0 dBm, and input third-order inter-modulation intercept point (IIP3) of –7.6 dBm. The proposed receiver is implemented using

0.13-μm CMOS technology and draws 25.84 mA from a 1.2-V supply. The total chip area, including testing pads, is only 1.21 mm × 1.03 mm.

It is believed that the proposed ILFT can be used in low-power high-performance transceiver design in the millimeter-wave band. Further research for low-power single chip transceiver and frequency synthesizer can be integrated in the future.

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陳 旻 玟
誌于風城交大
戊子 秋

CONTENTS

Table Captions

Figure Captions

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Wireless communication system has been under significant development over the past few decades and it is closer to our daily life than ever before. Wireless communication products such as cellular phones, Personal Digital Assistants (PDAs), and Global Positioning System (GPS) greatly facilitate and enrich our life. Nowadays, the wireless system is continuing to surge under increasing demands of high data rate and lower power consumption. The early developed standards such as Bluetooth and IEEE 802.11 family fail to come to this end due to their maximum data rate merely up to 54 Mega-bit-per-second (Mbps).

Ultra-Wideband (UWB) is a new rapidly advancing technology targeting at this goal and specified in IEEE 802.15.3a. The IEEE 802.15 TG3a specifies the unlicensed 3.1–10.6 GHz UWB band for short-range and high data-rate wireless communications. The UWB system provides Wireless Person Area Networks (WPANs) with data communication capabilities up to 480 Mbps.

The 7-GHz unlicensed band around 60 GHz for short-range and high-speed communication is developed for new consumer applications such as wireless High-Definition Multimedia Interface (HDMI) for high-definition television (HDTV) video stream and wireless data bus for cable replacement in recent years. Presently available unlicensed frequency bands are 59.0–66.0 GHz in Japan, 57.05–64.0 GHz in USA and Canada, 57.0–64.0 GHz in Korea, 57.0–66.0 GHz in Europe, and 59.4–62.0

GHz in Australia.

The landscape of wireless communication systems is shown in Fig. 1.1. Obviously, multi-gigabit-per-second (Gbps) data transmission becomes a challenge for future wireless communication systems.

Although the 60-GHz band offers the same amount of spectrum as UWB system at 3 to 10 GHz, few interferences and up to 40 dBm of transmit power envision a link to support multi-Gbps communication. According to the recently convention record in November 2007, the possible carrier frequencies are 58.32, 60.48, 62.64, and 64.8 GHz. The channel plan for full-rate (2 GHz) and half-rate (1 GHz) are shown in Figs. 1.2(a) and (b), respectively. The detail frequency plan is listed in Table 1.1. The target data rate for single carrier is 50.2 and 1506.6 Mbps with common rate (CR) and mandatory low rate (MLR), respectively. The propositional modulation schemes are $\pi/2$ binary phase shift keying (BPSK) and Gaussian minimum shifting keying (GMSK).

Historically, the implementation of 60-GHz integrated circuits are designed and fabricated by using Gallium Arsenide (GaAs) or advanced Silicon Germanium (SiGe) [1]–[3]. However, a low cost solution is necessary for consumer applications. Due to the continual scaling down of the CMOS technology, the transition frequency (f_T) of the nanometer CMOS technology up to 400 GHz has been reported in [4]. The CMOS technology can become the potential choice for the implementation of the 60-GHz wireless transceiver. Moreover, advanced CMOS technology has the advantages of low cost and of high-level integration with digital VLSI section. Therefore, CMOS technology can be a viable option to address the millimeter-wave market [5].

It is a tough task to grasp the analog and high-frequency character in monolithic

microwave integrated circuit (MMIC) design especially by using low-cost CMOS technology. There are still many problems and issues that we are facing and even have experienced. Researchers are supposed to invest much time and efforts to make great advancement. Making a more comfortable and convenient world is our destination as well as the motivation of our endeavors.

1.2 REVIEWS ON CMOS CIRCUITS FOR 60-GHZ APPLICATIONS

1.2.1 Frequency multiplier

There are two methods to generate local oscillator (LO) signals. In the first method, LO signals are generated directly by using fundamental frequency oscillators [6]–[10]. In the second one, they are generated by using lower frequency oscillators cascaded with frequency multipliers to obtain signals at the desired frequencies [11]–[19]. Because of the limited performance of active and passive devices at high frequency, it is easier to design high-performance voltage-controlled oscillators (VCOs) at low frequency rather than at high frequency. Moreover, high frequency dividers operated at the carrier frequency with a significant amount of power dissipation are not needed when using a low frequency VCO. Therefore, the second method is advantageous in low-power CMOS circuit implementation in the millimeter-wave band.

In general, a frequency multiplier can be divided into two stages: the harmonic generation stage and the LO amplification stage. The harmonic generation stage is designed to generate the signal at the desired harmonic and the LO amplification stage

is designed to amplify the output amplitude at the desired frequency. Because large output amplitude is provided by the LO amplification stage, a large power consumption is required for driving output swing. Thus, a frequency multiplier with a significant amount of power dissipation is the main drawback [11]–[18]. It can be seen from Fig. 1.3, the power consumption of frequency multiplier is increased as the increase of output frequency of frequency multiplier. As a result, the key design requirement of the second method is to increase the frequency conversion gain of the frequency multipliers. In order to achieve this requirement, low input power and low dc power consumption are necessary to obtain the desired output power level.

Frequency multipliers integrated with injection-locked oscillators (ILOs) [20]–[25] can efficiently increase the conversion gain because ILOs have the superior properties of frequency stabilization and high conversion gain with a narrow bandwidth [26]. Such a frequency multiplier with ILO is called the subharmonic injection-locked frequency multiplier (ILFM). It offers great potential use with millimeter-wave frequency synthesizers because of its low input power and low dc power consumption. Even with low input power, the subharmonic ILFM [20]–[25] can provide the same performance as a conventional frequency multiplier [27].

1.2.2 Phase-locked Loop and Frequency Synthesizer

Frequency synthesizer (FS) is a key building block of the radio-frequency integrated circuits (RFICs), which generates the carrier signal to convert transmission data up to the desired frequency band. The transmission and reception qualities in the wireless communication system are determined by the performance of LO that is generated by the FS.

In the conventional FS [28]–[31], VCO is always operated at the highest

frequency to generate the LO signal as shown in Fig. 1.4. The output frequency f_{out} of VCO is M-times of input reference frequency f_{ref} under locked condition. Owing to the limited performance of the active and passive devices, the performance of the VCO is mainly determined by the device technology.

The implementation of the high-frequency divider is another important design issue in the conventional FS structure. The injection-locked frequency dividers (ILFDs) [32]–[39] or Miller divider [40]–[42] are the popular options for the high-frequency divider design. It can be seen from Fig. 1.5 that ILFDs can be operated under small power consumption but they are of narrow band characteristics. Any frequency shift in these dividers can cause the failure of the whole FS. Another high-speed frequency divider is current-mode logic (CML) divider [43]–[52]. The CMOS CML divider has been demonstrated to have high-speed operation with low power dissipation because the full swing for internal operation is not required. As can be seen from Fig. 1.6, the operational frequency of recently published CMOS CML divider without inductor is still lower than 60 GHz. Therefore, ILFD is the only one solution for 60-GHz frequency divider. Overdesign for locking range to avoid frequency shift is required. As a result, the output frequency range of conventional FS operated around 60 GHz can not be too large.

The other FS structure is composed of a low-frequency FS cascaded with a frequency multiplier to generate the desired output frequency as shown in Fig. 1.7. So far, there is no prior design with this FS structure in CMOS technology. In this FS structure, the low-frequency FS is operated at the subharmonic of the desired frequency and the target frequency is generated by the frequency multiplier after the low-frequency FS [53]–[55]. Obviously, it has the advantages of smaller division ratio and low power dissipation from the frequency divider. Therefore, the second FS

structure can be attractive for CMOS design in the millimeter-wave band if the high-frequency and low-power CMOS frequency multiplier can be developed.

The comparison of FS architectures is listed in Table 1.2. A high-performance and wide tuning range VCO can be designed in the subharmonic FS integrated with frequency multiplier due to lower operational frequency. Moreover, the division ratio of frequency divider can be lower than that of fundamental FS to reduce the power consumption. However, large power consumption is required as the operational frequency of frequency multiplier is high such as millimeter-wave band. Finally, because the last stage of the subharmonic FS structure is frequency multiplier, the output signal is usually mixed with the total harmonics of VCO output frequency. Hence, extra effort to suppress undesired harmonics is required.

As described in Section 1.2.1, the large power consumption from frequency multiplier can be reduced significantly by using ILO. ILO chain can become a possible solution to millimeter-wave MMIC synthesizers [53].

1.2.3 Receiver

So far, some 60-GHz receivers have been demonstrated in CMOS technology [18]–[19], [56]–[64]. The homodyne receiver architecture is firstly implemented in the millimeter-wave receivers [56]–[59] because of its advantages of high integration and low system complication. The block diagram of the homodyne receiver is shown in Fig. 1.8. The radio-frequency (RF) signal is directly mixed with the local oscillator (LO) at the carrier frequency. Since the intermediate frequency (IF) is zero, the homodyne receiver is also called as zero-IF receiver or direct-conversion receiver.

Because the frequency of LO signal must be the same as the received frequency, the dc offset effect from the LO leakage by capacitive and substrate coupling [65] is

serious. Two main sources of dc offsets are shown in Figs. 1.9 (a) and (b). The first source is the LO leaking to the low-noise amplifier (LNA) input and mixing with itself at the $MIXER_{RF}$. The second source is the large nearby interferers leaking into VCO and then self-mixing.

Recently, a novel dc offset cancellation circuit has been proposed with simple Miller capacitor filter [66]. However, high-frequency synthesizer and high-frequency dividers with large power consumption are required. Due to large power consumption, the homodyne receiver structure is not suitable for consumer mobile applications.

The heterodyne receiver architecture is the one solution for the high-frequency synthesizer because the frequency of LO signals can be lower than received frequency as shown in Fig. 1.10 [60]–[64]. However, twice frequency translations make that the architecture of the receiver more complicated and image signal rejection is required for better signal-to-noise ratio (*SNR*). As compared with Fig. 1.8, the extra filters for frequency selection, BPF_{RF} and BPF_{IF}, are required. Therefore, the system complication is increased. Moreover, more inductors are required for system integration. Hence, total chip area is increased as compared with direct-conversion receiver.

Another solution for the high-frequency synthesizer is the frequency multiplier as shown in Fig. 1.11 [18]–[19]. The new CMOS frequency doubler [18] and frequency tripler [19] for the LO generation is proposed. Because of the even order frequency multiplier, the differential output can not be provided for the mixer operation. Thus, the extra effort is required for single to differential converter [18]. The first millimeter-wave CMOS frequency tripler is introduced in [19]. Due to its fully differential structure of frequency tripler, it is suitable for complex modulation schemes.

The comparison of receiver architectures is listed in Table 1.3. The homodyne receiver can achieve high-integration and low-power consumption, but the operational frequency of frequency synthesizer is the highest. The heterodyne receiver can be operated with lower operational frequency synthesizer but its system is too complex for millimeter-wave circuits. Finally, the homodyne receiver integrated with frequency multiplier is the best choice for high-frequency receiver design it has the advantages of homodyne receiver and the lower operational frequency of frequency synthesizer.

1.3 MOTIVATION AND MAIN RESULTS

The performance of VCO in the millimeter-wave band strongly depends on the characteristics of active and passive devices. To design the high-performance of low-frequency VCO cascaded with frequency multiplier is a solution to generate the high-performance LO signals. However, the power consumption of frequency multiplier is large when the operational frequency is high. The design of CMOS subharmonic ILFMs becomes the new interesting research topic in the millimeter-wave band because of their low power consumption. In this dissertation, the novel CMOS subharmonic injection-locked frequency tripler (ILFT) is developed for millimeter-wave band applications. The proposed ILFT can provide the similar output power as a VCO with small power consumption. Moreover, the locking range of the proposed ILFT can be similar to the tuning range of a VCO. As a result, the proposed ILFT can offer great potential application in LO signal generators for frequency synthesizers in the millimeter-wave band.

The proposed CMOS subharmonic ILFMs are further verified by the integration

with phase-locked loop (PLL) and receiver. In the PLL design, the new CMOS PLL structure that is formed by a low-frequency PLL cascaded with subharmonice ILFM is designed to avoid the use of the conventional ILFDs and Miller dividers with narrow-band characteristics. In addition, the maximum operational frequency of frequency divider can be reduced. The low-power PLL without ILFDs or Miller dividers for 60-GHz applications is designed in CMOS technology. Finally, the direct-conversion receiver is also integrated with subharmonic ILFT.

The aim of this dissertation is to develop low-power 60-GHz CMOS millimeter-wave circuits including millimeter-wave CMOS ILFTs, a 60-GHz PLL and a 60-GHz direct-conversion receiver.

Firstly, a *K*-band ILFT is designed and fabricated using 0.18-μm CMOS technology. The total locking range of the *K*-band ILFT can achieve 3915 MHz with 4-dBm input power when the varactors are used and the dc power consumption is 2.95 mW. A *V*-band ILFT is also designed and fabricated using 0.13-μm CMOS technology. The measured injection-locking range is 1422 MHz with 1.86-mW dc power consumption and 6-dBm input power. The locking range of the proposed ILFT is similar to the tuning range of a conventional varactor-tuned bulk-CMOS VCO. Moreover, the output power of the proposed ILFT is also similar to that of a VCO.

Secondly, a novel CMOS PLL integrated with ILFM that generates the 60-GHz output signal is proposed and designed in 0.18-μm CMOS technology. The output frequency range of the proposed PLL is from 53.04 GHz to 58.0 GHz. The measured phase noises at 1 MHz and 10 MHz offset from the carrier are –85.2 and –90.9 dBc/Hz, respectively. The reference spur level of –40.16 dBc is measured. The dc power dissipation of the fabricated PLL is 35.7 mW under a 1.8-V supply. It can be seen that the performance of the proposed PLL is similar to previous woks and the

power dissipation of the proposed PLL is only two-third of previous works [28]–[31]. Therefore, the proposed PLL structure is suitable for low power and high performance millimeter-wave PLL in 60-GHz applications.

Finally, a novel 60-GHz CMOS direct-conversion receiver front-end integrated with ILFTs is described. In the proposed receiver, the LO signals are generated by the QVCO operated at only one-third of carrier frequency cascade with the two ILFTs. Because of the QVCO frequency shift, the maximum RF frequency is 55.03 GHz. The measured results show a receiver gain of 18.2 dB, a noise figure of 16.96 dB, and an input-referred 1-dB compression point of –17.0 dBm. The proposed receiver is implemented using 0.13-μm CMOS technology and draws 25.84 mA from a 1.2-V supply. The total chip area is 1.21 mm × 1.03 mm. From the measurement results, the proposed receiver architecture provides a potential choice for high-integration and low-power in 60-GHz transceiver design.

1.4 ORGANIZATION OF THIS DISSERTATION

In Chapter 2, a novel CMOS ILFT is proposed and designed. The new concept for frequency tripler integrated with injection-locked oscillator (ILO) is introduced. In addition, the model and design methodology for the proposed ILFT are analyzed and developed. Finally, the performances of the proposed ILFTs are verified by experimental results at *K*-band and *V*-band. The experimental results show that the proposed ILFTs can provide large output power with low dc power dissipation.

In Chapter 3, a 60-GHz CMOS PLL used for IEEE 802.15.3c applications is proposed and designed using 0.18-μm CMOS technology. The extension model from ILFT for fifth-order harmonic of ILFM is presented. The proposed ILFM worked

beyond device transition frequency (f_T) is designed to generate the 60-GHz output signal. Because this design takes the advantage of low division ratio of frequency and low power consumption by using ILFM, the total power dissipation of the proposed PLL is significantly reduced as compared with published CMOS PLLs.

A 60-GHz CMOS direct-conversion receiver integrated with ILFT is described in Chapter 4. The proposed receiver is the first CMOS receiver design that integrates with ILFT. In addition, the maximum operation frequency of the frequency divider in a frequency synthesizer can be reduced to one-third by using the ILFT. Since it is feasible to design a high-performance VCO at low frequency and to save the large power consumption from full-speed frequency dividers, the proposed receiver can provide a solution to the wireless transceiver in the millimeter-wave band. Finally, conclusions and future work are given in Chapter 5.

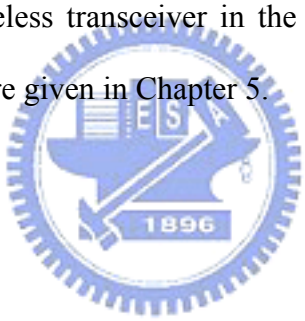


Table 1.1

Frequency plan for 60-GHz applications.

Channel Plan : Full-Rate (2 GHz)				
Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)
A1	57.24	58.32	59.40	1728
A2	59.40	60.48	61.56	1728
A3	61.56	62.64	63.72	1728
A4	63.72	64.80	65.88	1728
Channel Plan : Half-Rate (1 GHz)				
Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (MHz)
B1	57.78	58.32	58.86	864
B2	59.94	60.48	61.02	864
B3	62.10	62.64	63.18	864
B4	64.26	64.80	65.34	864

Table 1.2

Comparison of the FS architectures.

Structure	Fundamental FS (Direct Generation)	Subharmonic FS with Frequency Multiplier
Output purity	Pure	Mixed
VCO performance	Poor	Good
Frequency divider division ratio	High	Low
Frequency divider power consumption	High	Low
Frequency divider bandwidth	Narrow (ILFD or Miller divider)	Wide (if CML frequency divider can be used)
Frequency multiplier	Not Required	Yes
Frequency multiplier power dissipation	None	Large

Table 1.3

Comparison of the receiver architectures.

Structure	Homodyne Receiver	Heterodyne Receiver	Homodyne Receiver with Frequency Multiplier
Integration ability	Good	Poor	Good
Image rejection	Not required	Required	Not required
dc-offset	Yes	No	Yes
1/f noise	Yes	No	Yes
Operational frequency of FS	High (Large power consumption)	Mediate	Low (Small power consumption)
Frequency multiplier	Not required	Not required	Required

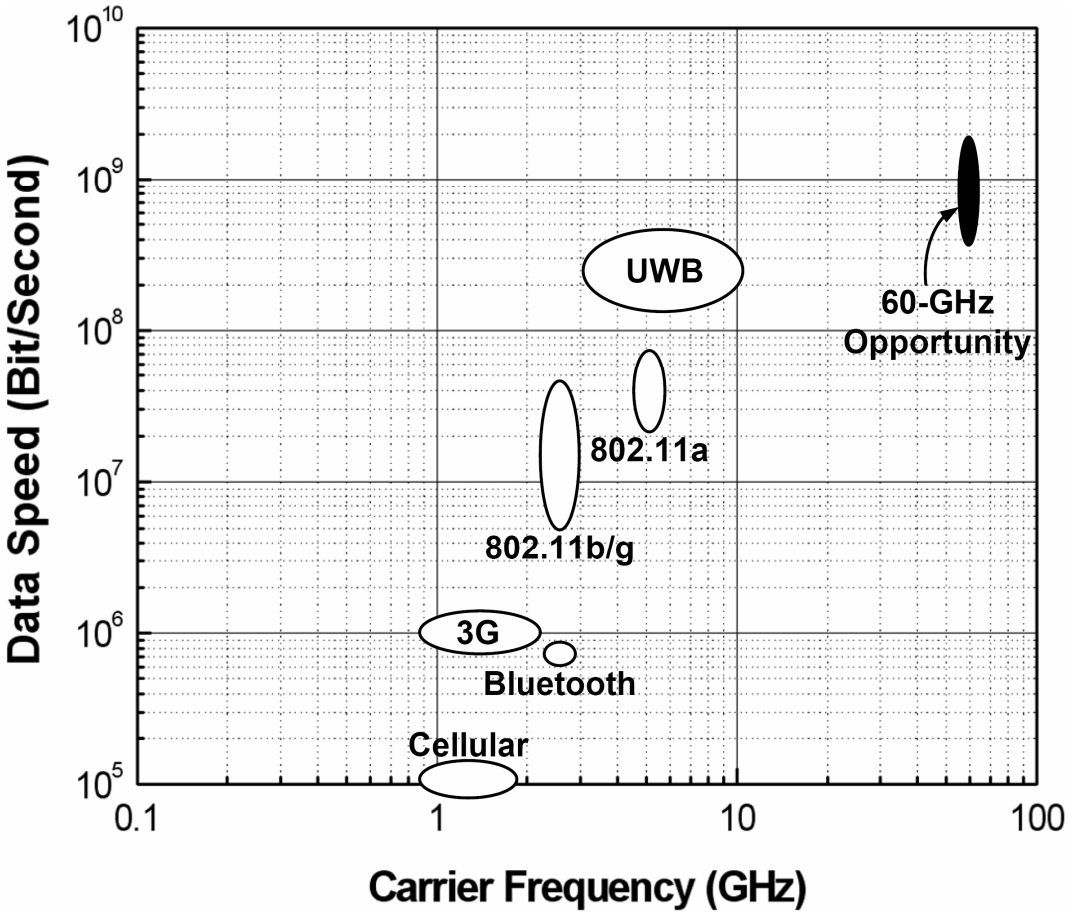
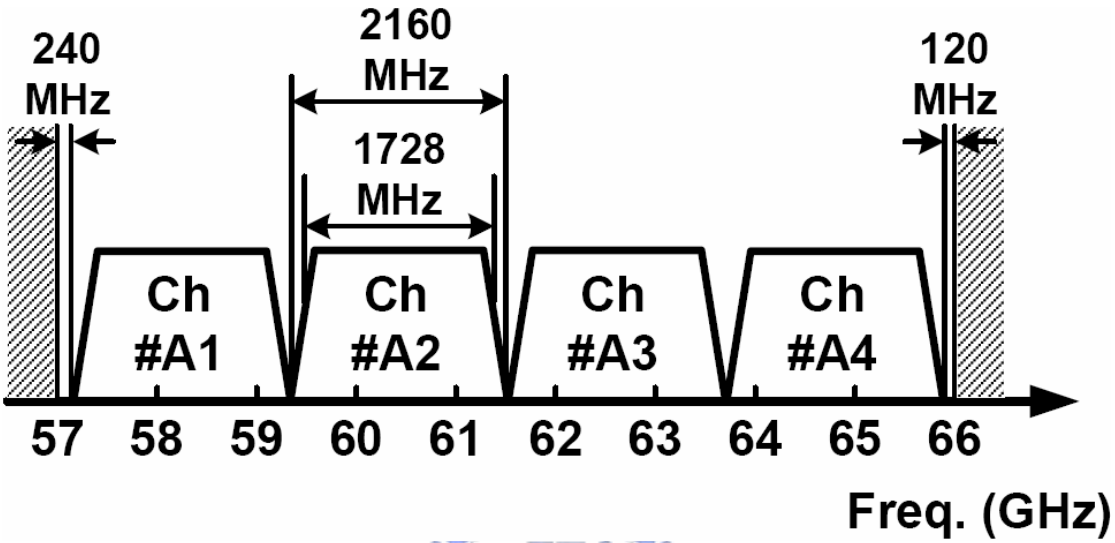
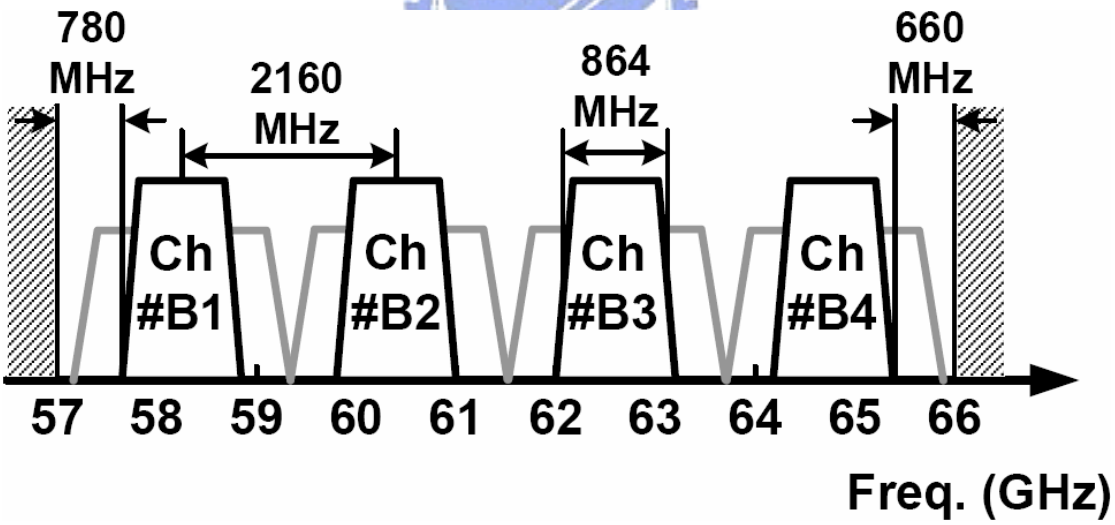


Fig. 1.1 The landscape of wireless communication systems.

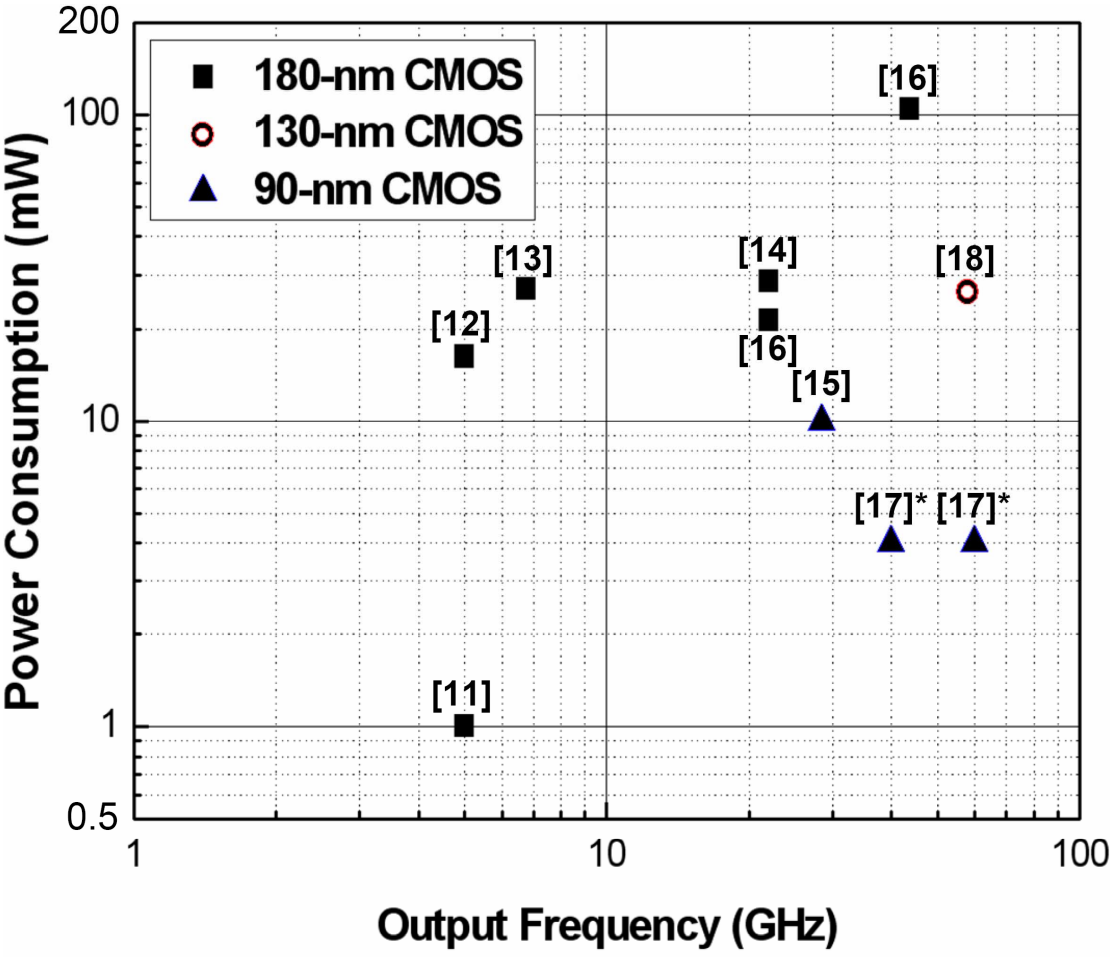


(a)



(b)

Fig. 1.2 Frequency plan for (a) full-rate and (b) half-rate in 60-GHz applications.



*** These values exclude the amplification stage with small output power for a fair comparsion.**

Fig. 1.3 Recently published CMOS frequency multipliers.

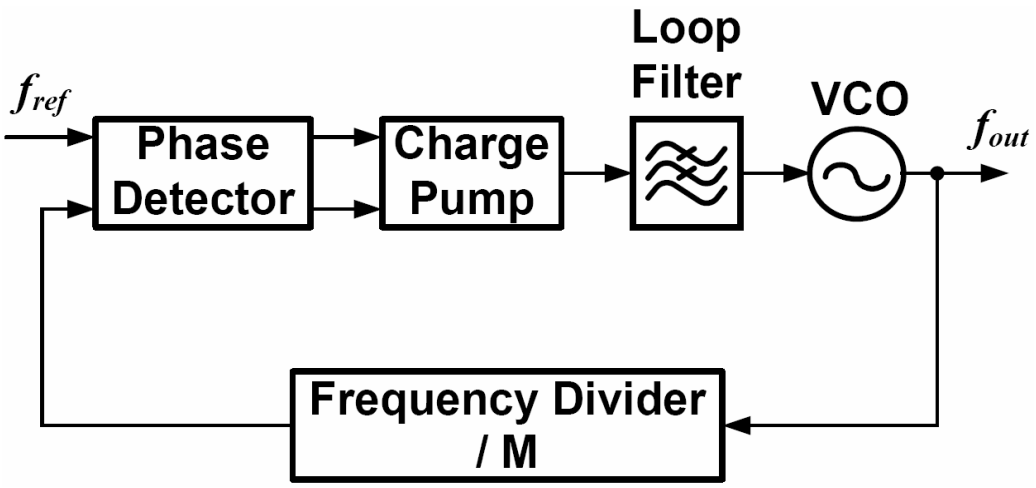
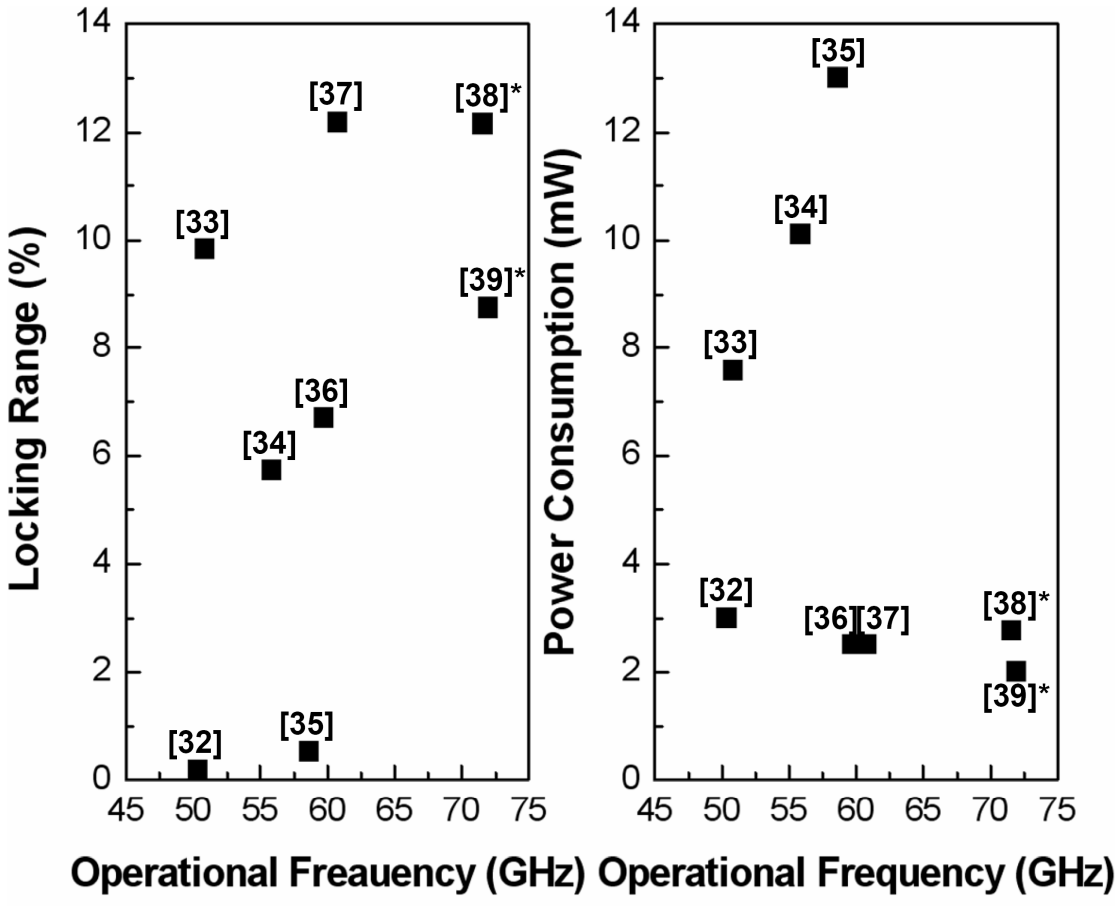


Fig. 1.4 Block diagram of the conventional frequency synthesizer.



*** Tuning Varactors are used for increasing locking range.**

Fig. 1.5 Recently published CMOS injection-locked frequency dividers.

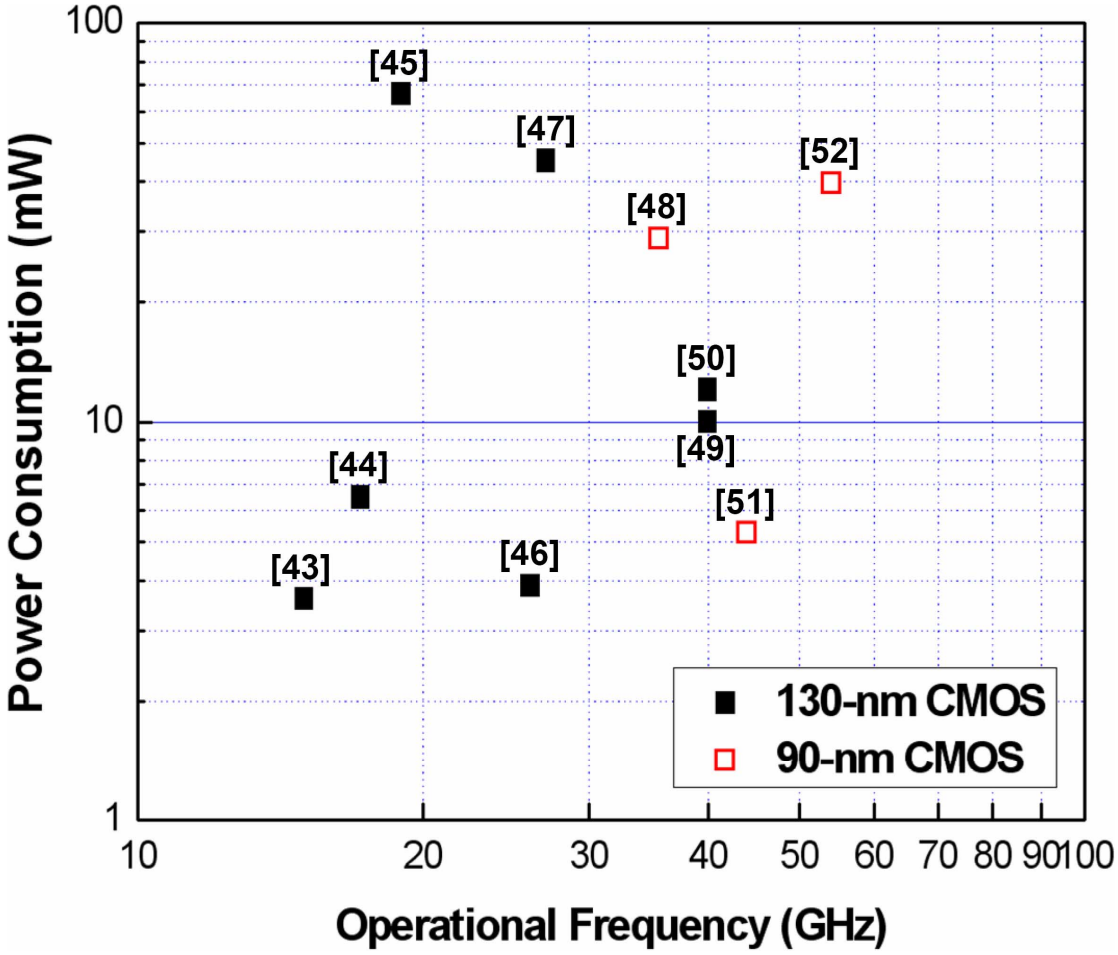


Fig. 1.6 Recently published CMOS CML frequency dividers without inductor peaking.

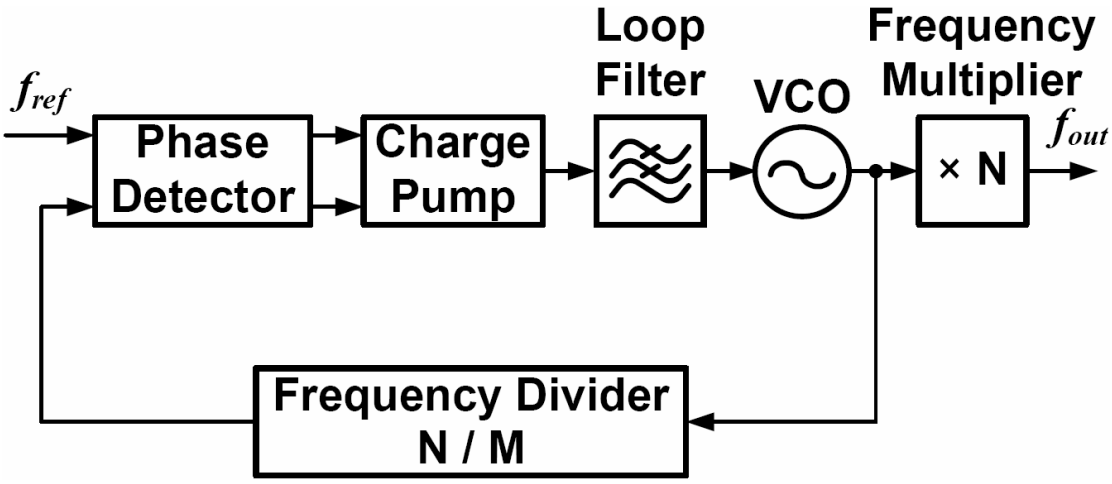


Fig. 1.7 Block diagram of frequency synthesizer with frequency multiplier.

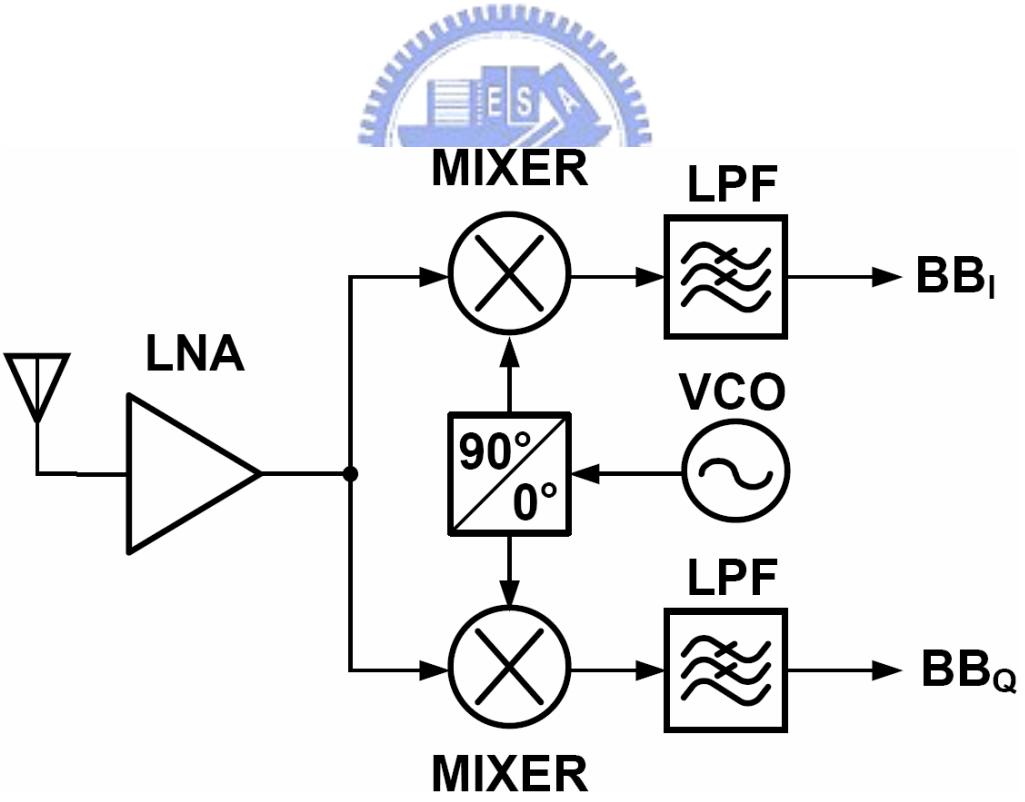
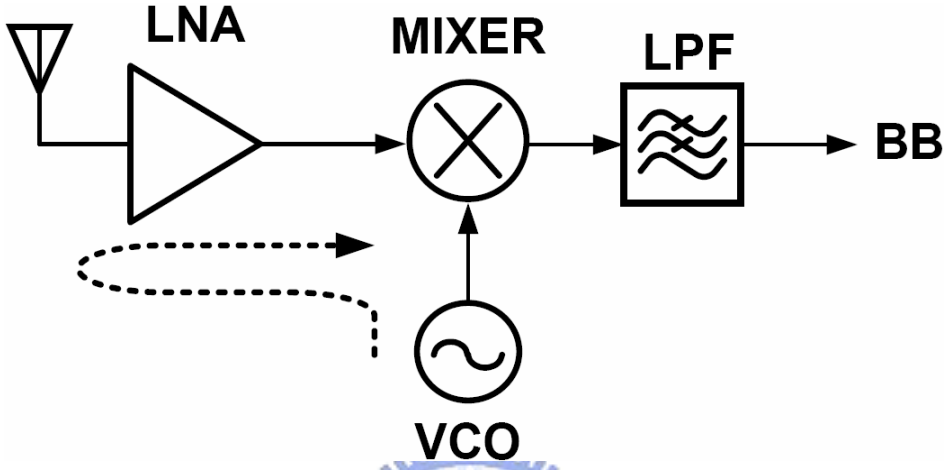
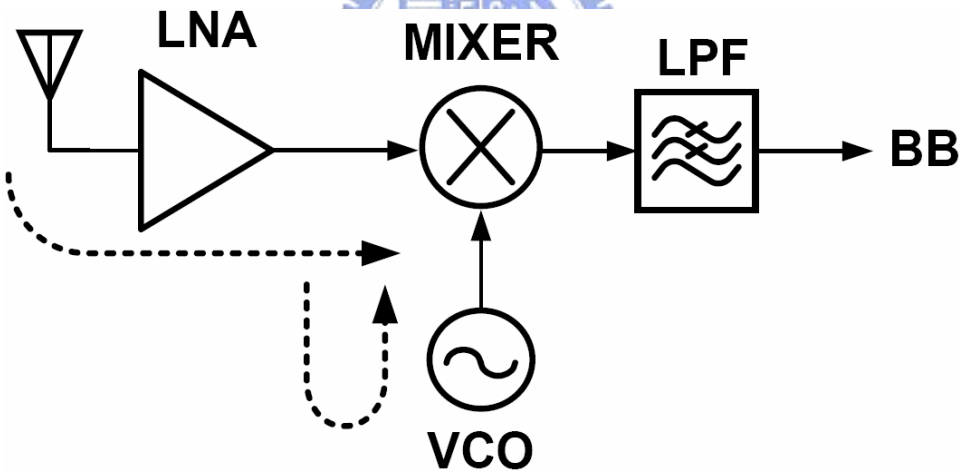


Fig. 1.8 Block diagram of the homodyne receiver.



(a)



(b)

Fig. 1.9 The sources of dc offsets from (a) LO leaking to LNA input and (b) large interferers leaking to VCO.

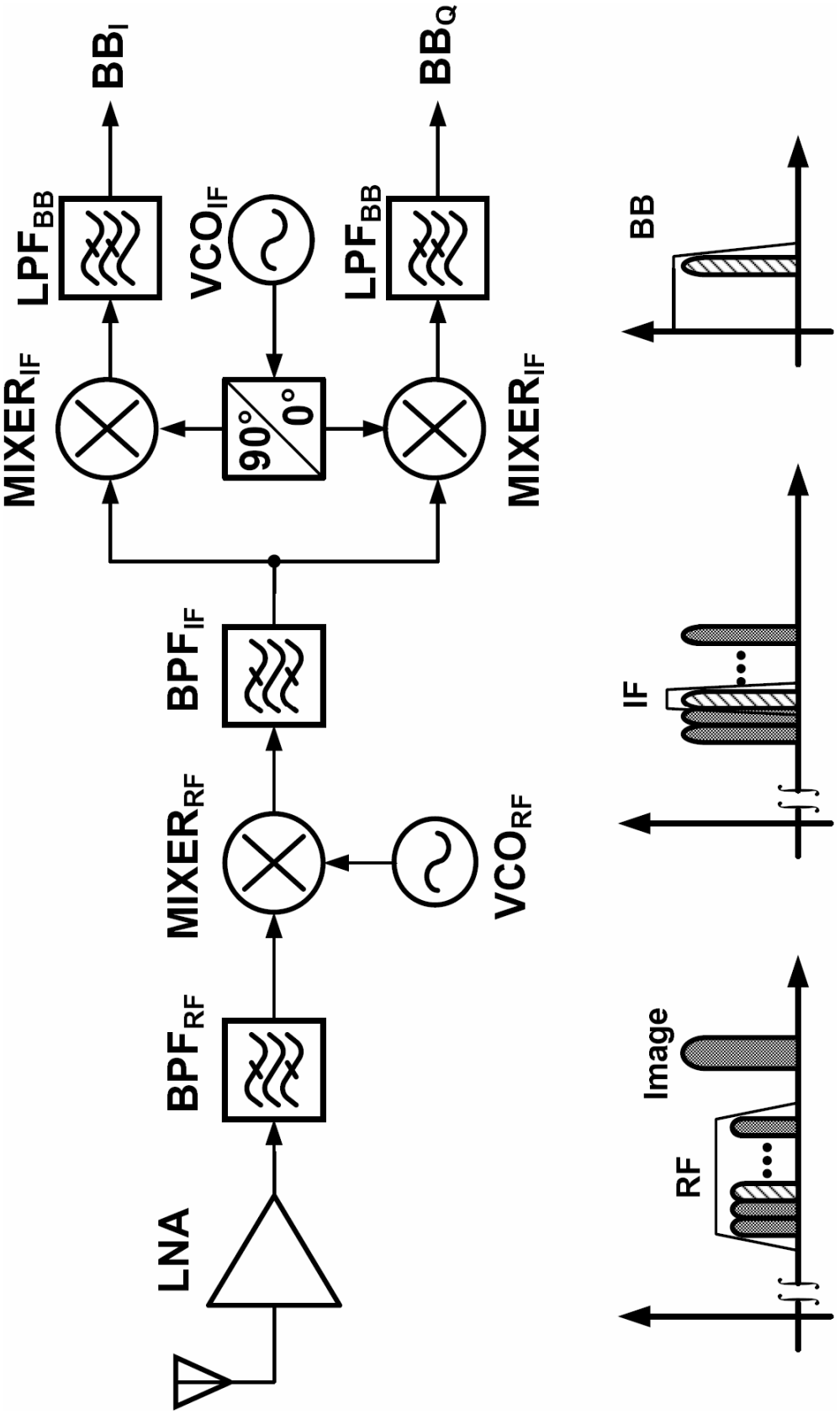


Fig. 1.10 Block diagram and frequency translation of the heterodyne receiver.

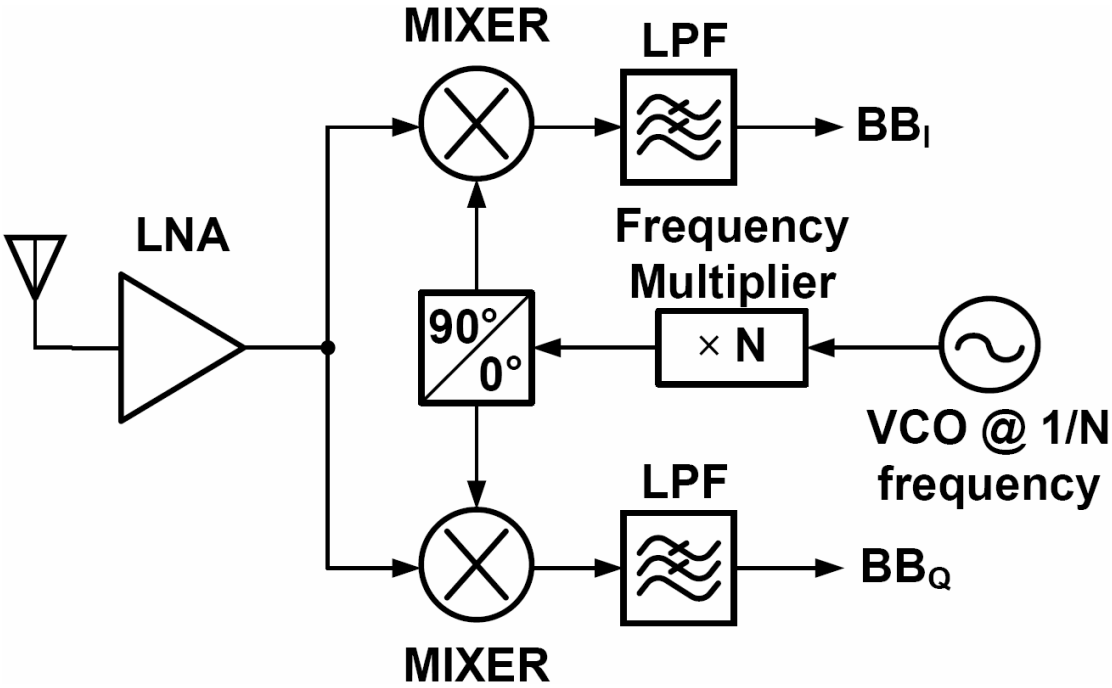


Fig. 1.11 Block diagram of the homodyne receiver with frequency multiplier.

CHAPTER 2

CMOS SUBHARMONIC INJECTION-LOCKED FREQUENCY TRIPLERS

In this chapter, a new CMOS fully differential subharmonic injection-locked frequency tripler (ILFT) is proposed and analyzed. It is suitable for complex modulation schemes because of its fully differential structure. The locking range of the proposed ILFT is improved by inserting the frequency pre-generator circuit before the ILO. The main advantage of a frequency pre-generator is that the locking range can be maximized with little degradation of ILO output performance. An analytical model is developed to characterize both the locking range and the output phase noise of the proposed ILFT. The proposed *K*-band ILFT is fabricated using 0.18-μm CMOS technology. According to the measured results, it has an locking range of 1092-MHz wide with an input power of only 4-dBm and a dc power consumption of 0.45 mW. Moreover, the output power can achieve –9.4-dBm with 10.5-dB phase noise higher than that of the input signal. This chapter shows that the key design requirement can be achieved in the proposed ILFT. Finally, the theoretical results are verified by the experimental results.

In Section 2.1, the model for the proposed ILFT is derived. The CMOS circuit implementation is described in Section 2.2. The experimental results are presented in Section 2.3. Finally, the conclusion and summary are given in Section 2.4.

2.1 THEORETICAL MODEL FOR INJECTION-LOCKED FREQUENCY TRIPLER

Based upon the locking mechanism for a small injection signal [26] and the simple ILO model [67], a physical representation of the proposed ILFT with a frequency pre-generator to generate the third-order harmonic signal connected to an ILO is shown in Fig. 2.1. In the ILO model, $H(j\omega)$ is the transfer function of the band pass *LC*-tank filter used to eliminate undesired frequencies generated by the frequency pre-generator. The active devices of the ILO are modeled as the linear constant transconductance stage G_m. The frequency pre-generator is modeled as the nonlinear characteristic function $f(v_I)$. Both the G_m and $H(j\omega)$ with a feedback path form the ILO. Without any input signal, the ILO has a steady output signal if the Barkhausen criterion is satisfied in the close-loop structure. An incident signal $v_I(t)$ with input frequency ω_I is injected into the oscillator via a frequency pre-generator. The output frequency ω_O is the function of input frequency ω_I while the oscillator is under the locked situation.

If the ILFT is under the locked condition, the following apply:

$$v_I(t) = V_i \cos(\omega_I t + \theta) \tag{2.1}$$

$$v_O(t) = V_o \cos(\omega_O t) \tag{2.2}$$

$$v_{I,ILO}(t) = f(v_I(t)) = f(V_i \cos(\omega_I t + \theta)) \tag{2.3}$$

where $v_I(t)$ is the incident signal with input frequency ω_I, amplitude V_i, and phase θ; $v_O(t)$ is the output signal with frequency $\omega_O = 3\omega_I$ and amplitude V_o; and $v_{I,ILO}(t)$ is the output signal of the frequency pre-generator.

From [68], $v_{I,ILO}(t)$ can be expressed as a polynomial series:

$$v_{I.ILO}(t) = f(v_I(t)) = \sum_{n=0}^{\infty} a_n (v_I(t))^n$$

$$= a_0 + a_1 v_I(t) + a_2 (v_I(t))^2 + a_3 (v_I(t))^3 + O((v_I(t))^4) \quad (2.4)$$

where a_n is the coefficient of polynomial f, and $O((v_I(t))^4)$ is the terms of order higher than three. The coefficient a_3 is proportional to the conversion gain of the third-order harmonic frequency generator. The output current of the transconductance stage G_m can been written as

$$i_{OUT} = G_m[f(v_I(t)) + v_O(t)]$$

$$= G_m[v_{I,ILO}(t) + v_O(t)]. \quad (2.5)$$

By substituting (1)–(3) into (5),

$$i_{OUT} = G_m[v_{I,ILO}(t) + v_O(t)]$$

$$= G_m[f(V_i \cos(\omega_I t + \theta)) + V_o \cos(\omega_o t)]. \quad (2.6)$$

By neglecting the $O((v_I(t))^4)$ term in (2.4), by substituting other terms in (2.4) into (2.6), by assuming that any frequency not close to ω_O is filtered out by the frequency selective load $H(j\omega)$, and by rearranging the terms, (2.6) can be rewritten as

$$i_{OUT} = \mathrm{Re}\left\{ e^{j\omega_O t} \left[G_m V_o + \frac{a_3 G_m V_i^3}{4} e^{j3\theta} \right] \right\}$$

$$= |i_{OUT}| \cos(\omega_O t + g(\theta)) \quad (2.7)$$

where

$$|i_{OUT}| = \sqrt{\left[G_m V_o + \left(\frac{a_3 G_m V_i^3}{4}\right)\cos 3\theta\right]^2 + \left[\left(\frac{a_3 G_m V_i^3}{4}\right)\sin 3\theta\right]^2} \tag{2.8}$$

$$g(\theta) = \arctan\left\{\frac{a_3 G_m V_i^3 \sin 3\theta}{4G_m V_o + a_3 G_m V_i^3 \cos 3\theta}\right\} \tag{2.9}$$

and a_3 is the coefficient of cubic term in the nonlinear characteristic function of the frequency pre-generator.

The approximate transfer function of the band pass *LC*-tank filter $H(j\omega)$ can be written as

$$H(j\omega) = \frac{H_0}{1 + j2Q\left(\frac{\omega - \omega_r}{\omega_r}\right)} \tag{2.10}$$

where ω_r and Q are the resonant frequency and quality factor of the *LC*-tank, respectively. H_0 is the impedance of the *LC*-tank at resonant frequency.

If the Barkhausen criterion is satisfied in the close-loop, the phase shift of the close-loop should be zero. Thus

$$-\arctan\left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right] + g(\theta) = 0. \tag{2.11}$$

Combing (2.9) and (2.11), gives

$$\left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right] = \left\{\frac{a_3 G_m V_i^3 \sin 3\theta}{4G_m V_o + a_3 G_m V_i^3 \cos 3\theta}\right\}. \tag{2.12}$$

By rearranging (2.12) and finding the solution for θ, the following is derived

$$\sin(3\theta-\phi)=\frac{\frac{4V_o}{a_3V_i^3}\left[\frac{2Q(\omega-\omega_r)}{\omega_r}\right]}{\sqrt{1+\left[\frac{2Q(\omega-\omega_r)}{\omega_r}\right]^2}} \tag{2.13}$$

where

$$\phi=\arcsin\left\{\frac{\frac{2Q(\omega-\omega_r)}{\omega_r}}{\sqrt{1+\left[\frac{2Q(\omega-\omega_r)}{\omega_r}\right]^2}}\right\}. \tag{2.14}$$

Since $\left|\sin(3\theta-\phi)\right|\le 1$, (2.13) can be rewritten as

$$\frac{|\omega-\omega_r|}{\omega_r}\le\frac{1}{2Q}\sqrt{\frac{\left(a_3V_i^3\right)^2}{(4V_o)^2-\left(a_3V_i^3\right)^2}}\approx\frac{1}{2Q}\left|\frac{a_3V_i^3}{4V_o}\right|. \tag{2.15}$$

If $4V_o >> a_3V_i^3$, the approximation in (2.15) is valid.

The output voltage amplitude can be written as

$$V_o=\left|i_{OUT}\right\|H(j\omega)|$$

$$=G_mH_0\sqrt{\left[V_o+\left(\frac{a_3V_i^3}{4}\right)\cos 3\theta\right]^2}\ . \tag{2.16}$$

By solving (2.16) and assuming $V_o+\left(a_3V_i^3\cos 3\theta/4\right)>0$, the expression of the output amplitude can be rewritten as

$$V_o=\frac{a_3G_mH_0V_i^3\cos 3\theta}{4(1-G_mH_0)}. \tag{2.17}$$

In general, the locking range is limited by failure of either the phase condition (2.15) or the gain condition (2.16) [67]. From (2.15), it can be seen that the locking

range increases with an increase in either the conversion gain of the frequency pre-generator or the incident amplitude V_i. The degradation of the *LC*-tank quality factor Q can also improve the locking range. However, the latter causes a decrease in the impedance of the *LC*-tank H_0 and, thus, the output voltage amplitude also decreases (2.17). This result is consistent with the results in [26]. According to the proposed ILFT model, the design principle can be developed. It can be seen from (2.17) that the quality factor of the *LC*-tank can be maximized in order to obtain increased output amplitude. The resulting degradation of the locking range can be improved by increasing of the conversion gain of the frequency pre-generator (2.15).

The overall ILO output phase noise is characterized by the noise contributions of all blocks in an ILO [69]. The simplified noise source model of the proposed ILFT is shown in Fig. 2.2 where the conversion gain of the third-order harmonic signal in the frequency pre-generator is simplified to be a constant value A_{FPG} and $v_{I,ILO3\omega}$ is the signal with frequency $3\omega_I$. The noise contribution from the frequency pre-generator and the ILO are modeled as $n_{FPG}(t)$ and $n_{ILO}(t)$, respectively. The linear phase-domain model [70] is adopted to calculate the output phase noise.

The simplified noise source model of the proposed ILFT, as shown in Fig. 2.2, can be divided into two parts. One part is the noise calculation of the frequency pre-generator and the other is the noise analysis of the ILO. First, the noise characteristic between v_I and $v_{I,ILO3\omega}$ is considered. The phase noise spectral density $S_{IN,ILO}(\omega_m)$ at $v_{I,ILO3\omega}$ node can be expressed as [69]

$$S_{IN,ILO}(\omega_m) = 3^2 \cdot S_{INJ}(\omega_m) + S_{FPG}(\omega_m) \tag{2.18}$$

where $S_{INJ}(\omega_m)$ and $S_{FPG}(\omega_m)$ are phase noise spectral densities of the injection signal and frequency pre-generator, respectively. ω_m is the offset frequency from output

frequency ω_O.

The noise relation between $v_{I,ILO3\omega}$ and v_O can be written as [69]

$$S_{OUT}(\omega_m)=\frac{1}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{IN,ILO}(\omega_m)+\frac{\left(\frac{\omega_m}{\omega_p}\right)^2}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{FreeRun}(\omega_m) \tag{2.19}$$

where the corner frequency of the ILFT noise transfer function ω_p can be written as

$$\omega_p=\frac{\omega_r}{2Q}\frac{\eta}{1+\eta} \tag{2.20}$$

$$\eta=\frac{A_{FPG}V_i}{V_o}. \tag{2.21}$$

In the above equations, $S_{OUT}(\omega_m)$ and $S_{FreeRun}(\omega_m)$ are phase noise spectral densities of output and internal circuits, respectively; A_{FPG} is the conversion gain of the third-order harmonic signal in the frequency pre-generator; ω_r and Q are the resonant frequency and the quality factor of LC-tank in the band pass filter, respectively; H_0 is the impedance of the LC-tank at resonant frequency; and V_i and V_o indicate the amplitudes of input and output, respectively.

The combination of (2.18) and (2.19) results in the following:

$$S_{OUT}(\omega_m)=\frac{3^2}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{INJ}(\omega_m)+\frac{1}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{FPG}(\omega_m)+\frac{\left(\frac{\omega_m}{\omega_p}\right)^2}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{FreeRun}(\omega_m) \tag{2.22}$$

.

As may be seen from the first and the second terms in (2.22), the noise from the input signal and frequency pre-generator are passed through the low-pass filter so that their noise transfer functions have low-pass transfer characteristics. Thus, the output

phase noise is dominated by these two noise sources at small offset frequency ω_m. If the noise contribution from the frequency pre-generator is negligible, the output phase noise is 9.5 dB [=10log (3^2)] higher than that from the input signal with a small offset frequency. The noise from internal circuits as given in the third term of (2.22) has a high-pass transfer characteristic. At large offset frequency ω_m, the output phase noise is dominated by this noise and has a high-pass shape. To minimize the output phase noise, the corner frequency ω_p can be increased to filter out the internal noise. As may be seen from (2.20) and (2.21), ω_p can be increased by either degradation of the *LC*-tank quality factor Q or the high incident amplitude V_i.

A summary of the proposed ILFT can be developed from (2.6)–(2.11). The quality factor Q of the *LC*-tank is maximized for a large output voltage swing and for low-power consumption. The degradation of the locking range and the output phase noise from the increase in quality factor Q can be compensated for by increasing the conversion gain of the frequency pre-generator.

If the frequency pre-generator is removed from ILFT, the nonlinear characteristic function is performed by ILO. Thus, the locking range can be derived as

$$\frac{|\omega-\omega_r|}{\omega_r} \le \frac{1}{2Q}\sqrt{\frac{\left(a_3V_i^3\right)^2}{\left(4a_1V_o+6a_3V_i^2V_o+3a_3V_o^3\right)^2-\left(a_3V_i^3\right)^2}}$$

$$\approx \frac{1}{2Q}\left|\frac{a_3V_i^3}{4a_1V_o+6a_3V_i^2V_o+3a_3V_o^3}\right|. \qquad (2.23)$$

Whereas the output amplitude is represented as

$$V_o = G_m H_0 \sqrt{\left[a_1V_o+\left(\frac{a_3V_i^3}{4}\right)\cos 3\theta+\frac{3}{2}a_3V_i^2V_o+\frac{3}{4}a_3V_o^3\right]^2}. \qquad (2.24)$$

It can be seen from (2.23) that the locking range can be increased by increasing $|a_3|$. In general, the value of a_3 is negative, and an $|a_3|$ which is too large would degrade the output amplitude of the ILFT in (2.24) significantly. Obviously, if an ILFT works without the frequency pre-generator, the extra power consumption is required for both a large locking range and large output amplitude.

2.2 CIRCUIT REALIZATION

2.2.1 The Circuit Design of Injection-locked Frequency Triplers

Based on the model developed in Section 2.1, the *K*-band and *V*-band CMOS ILFTs are designed. The proposed CMOS ILFT circuit is shown in Fig. 2.3. The off-chip transformer T1 is designed to generate the differential input signal. The function of the frequency pre-generator is implemented by M1 and M2. The design guideline of M1 and M2 is the same as for the conventional frequency multipliers in [71]. The gate bias V_{BIAS} of M1 and M2 is fed from the input off-chip transformer T1 and the conversion gain of the frequency pre-generator can be maximized with an appropriate V_{BIAS} value. The tripled-frequency signal generated by the frequency pre-generator is injected into the ILO formed by M3, M4, C1, C2, L1, and L2. The selected values of inductors L1/L2 and varactors C1/C2 are chosen so that their resonant frequency is close to the third-order harmonic frequency of the input signal. According to the design guideline in Section 2.1, the quality factor of the *LC*-tank is maximized for a large output swing and low power consumption. V_{TUNE} is the external controlled signal used to increase the locking range. M3 and M4 are used to generate the negative resistance to compensate for the loss of the *LC*-tank. R1 is designed for the improvement of the harmonic rejection-ratios (HRRs). Finally, the

output signals are taken from the open-drain buffers for test purposes. The proposed ILFT has a current-reuse structure between the frequency pre-generator and the ILO for low power operation.

Fig. 2.4 shows the HSPICE simulated normalized third-order harmonic currents I_{d3}/I_{dmax} of the frequency pre-generator M1/M2 as a function of conduction angle (θ_{CON}) where I_{d3} is the output amplitude of the drain current at the third-order harmonic frequency, I_{dmax} is defined as the maximum peak-to-peak output drain current, and conduction angle is the device turn-on angle within one period of input signal. The simulation condition involves an 8-GHz input signal with 4-dBm input power and a MOS device with dimensions of W/L = 18 μm/0.18 μm with gate-source bias voltage changing from 0.03 V to 1.03 V. Because of the parasitic capacitance of the device, the ac current between the gate and drain is included in the output drain current I_{dmax}. Thus, the normalized harmonic current curve in Fig. 2.4 is not the same as the ideal switch condition in [71]. The maximum output third-order harmonic current occurs when the conduction angle is 100°. With this conduction angle, the devices M1/M2 must be biased at the weak-inversion region. Under this condition, the ILO circuits may not satisfy the oscillation condition with such a small dc current. In the proposed ILFT, the frequency tripled function devices (M1 and M2) are biased at a conduction angle of 250° for higher frequency conversion efficiency while maintaining oscillation. The V_{BIAS} can be calculated by a given input power, a device threshold voltage, and a suitable conduction angle [71].

Because the even harmonic signals are common-mode signals, an appropriate value for resistor R1 is set to eliminate the undesired even harmonic signals. To verify the effect of R1, Fig. 2.5 shows the HSPICE simulation results of the second-order and forth-order HRRs for various values of R1 in the *K*-band ILFT design. It can be

seen that the HRR can be improved with a small R1 value. When the R1 value is 90 ohm, the HRRs improve with only a small voltage drop for the *K*-band ILFT. However, for the *V*-band ILFT, the R1 value needs only to be 55 ohm because of the low nominal power supply voltage in 0.13-μm CMOS technology.

2.2.2 The Simulation Results of Injection-locked Frequency Triplers

2.2.2.1 *K*-band ILFT

Based on the model development in Section 2.1 and the circuit description in Section 2.2.1, the device dimension for *K*-band ILFT in 0.18-μm CMOS technology is shown in Table 2.1 (a). The locking range as a function of input bias V_{BIAS} is shown in Fig.2.6. Small dc current is allowed through M3/M4 as the input bias V_{BIAS} is decreased, the negative-resistance generated by M3/M4 becomes weaker. Therefore, the locking range is increased due to the small effective quality factor of *LC* tank. Due to a large third-order harmonic current is generated by M1/M2 at the V_{BIAS} of 0.65 V, it exists a peak locking range. As a results, the input bias value V_{BIAS} of 0.65 V is suggested in the *K*-band ILFT.

The simulated power consumption of the *K*-band ILFT is 2.95 mW at a power supply of 1.5 V. The SPECTRE RF simulated free-running *K*-band ILFT output after output buffer at time-domain and frequency-domain analysis are shown in Figs. 2.7 and 2.8, respectively. The free-running *K*-band ILFT provides the output amplitude of 250 mV as can be seen from transient simulation and output power of –2.04 dBm at 25.39 GHz as shown in the Fast-Fourier Transform (FFT) results. The simulated locked *K*-band ILFT output after output buffer with input power of 4 dBm, input frequency of 8.48 GHz, and V_{BIAS} of 0.65 at time-domain and frequency-domain are shown in Figs. 2.9 and 2.10, respectively. It can be seen from Fig. 2.9 that the fundamental signal is existed in the output waveform. The simulated output spectrum

of locked *K*-band ILFT is shown in Fig. 2.10 where the HRRs compared to the desired third-order harmonic are 24.21, 16.56, 25.49, 40.40 dBc for the first, second, forth, and fifth harmonics, respectively. Due to the parasitic capacitance of resistor R1, the HRRs can not reach to the ideal case in Fig. 2.5.

The SPECTRE RF simulated output frequency under locked condition as the varactors tuning voltage V_{TUNE} varies from 0 to 1.5 V is shown in Fig. 2.11. Because the quality factor of the varactor decreases as the tuning voltage V_{TUNE} decreases, the locking range at lower tuning voltage is larger than that at higher tuning voltage. The output frequency range of the *K*-band ILFT under free-running condition is from 22.98 GHz to 25.39 GHz. With a 4-dBm input signal, the output frequency range of the *K*-band ILFT under locked condition is from 21.54 GHz to 25.71 GHz. Therefore, the output frequency range extends from 2410 MHz to 4170 MHz. The simulated input power versus the output frequency when the input bias V_{BIAS} is set at 0.65 V is shown in Fig. 2.12. The upper and lower locking ranges are labeled as the maximum and minimum output frequencies under locked condition, respectively. The locking range is from 30 to 690 MHz while the input power varies from –7 to 4 dBm.

2.2.2.2 *V*-band ILFT

The *V*-band ILFT is also designed in 0.13-μm CMOS technology. Due to the poor performance of varactor in *V*-band frequency, the varactors C1/C2 are not included in the *V*-band ILFT. Hence, the selected value of inductors L1/L2 is chosen so that they can resonate with the total parasitic capacitances at the drain of M3/M4 at the third-order harmonic frequency of input signal. The threshold voltage V_{th} in 0.13-μm CMOS technology is smaller than that in 0.18-μm CMOS technology so the input bias V_{BIAS} for maximization of third-order harmonic current is 0.55 V. The device dimension for *V*-band ILFT is shown in Table 2.1 (b). The simulated power

consumption of the *V*-band ILFT is 2.09 mW at a power supply of 1.2 V.

The SPECTRE RF simulated free-running *V*-band ILFT output after output buffer at time-domain and frequency-domain analysis are shown in Figs. 2.13 and 2.14, respectively. The free-running *V*-band ILFT provides the output amplitude of 127 mV as shown from transient simulation and output power of –8.9 dBm at 60.10 GHz as shown from FFT results. The simulated locked *V*-band ILFT output after output buffer with input power of 6 dBm, input frequency of 20.3 GHz, and V_{BIAS} of 0.55 V at time-domain and frequency-domain are shown in Figs. 2.15 and 2.16, respectively. The simulated output spectrum of locked *V*-band ILFT is shown in Fig. 2.16 where the HRRs compared to the desired third-order harmonic are 19.08, 18.92, 29.47, 39.31 dBc for the first, second, forth, and fifth harmonics, respectively.

The SPECTRE RF simulated input power versus the output frequency with input bias V_{BIAS} of 0.55 V is shown in Fig. 2.17. The locking ranges are 870 MHz, 1200 MHz, and 1590 MHz at the input power are 4dBm, 6dBm, and 9dBm, respectively. To simulate the phase noise relation between *V*-band ILFT input and output, a low-frequency VCO operated at the one-third of the *V*-band ILFT output frequency is designed and the VCO output is directly injected into the ILFT input. The SPECTRE RF simulated phase noise of *V*-band ILFT input and output with the offset frequency from 100 kHz to 100 MHz is shown in Fig. 2.18. The phase noise difference between input and output of *V*-band ILFT are 9.55, 9.6, and 12.5 dB at the frequency offset of 1 MHz, 10 MHz, and 100 MHz, respectively. At small frequency offset, these values are close to the theoretical limit 9.54 dB (=$10\log(3^2)$) as can be seen from (2.22).

2.2.3 Layout Consideration

Layout is an important issue in the millimeter-wave circuit design. There is a

reason for explanation that the conventional layout parameter extractions (LPE) method is not suitable for such high frequency application. The interconnection inductance can not be extracted by LPE command. The interconnection inductance should be taken into consideration if the length of the metal line is longer than one-tenth of the wavelength. In the millimeter-wave frequency range, the wavelength is the order of hundreds μm. Therefore, the characteristics of those interconnection metal lines are simulated by the 3D EM CAD tool High-Frequency Simulation Software (HFSS).

2.3 EXPERIMENTAL RESULTS

Based upon the proposed ILFT circuit structure, both *K*-band and *V*-band ILFTs are designed and fabricated using 0.18-μm and 0.13-μm CMOS technologies, respectively. The chip microphotograph of the *K*-band ILFT is shown in Fig. 2.19 where the chip area is 0.66 mm × 0.69 mm. The chip photograph of the *V*-band ILFT is shown in Fig. 2.20 where the chip area is 0.59 mm × 0.66 mm. The chip areas of both the proposed ILFTs are limited by the minimum distance between the pads.

In the measurement setup, an on-wafer measurement system incorporating a probe station, ground-signal-ground (GSG) coplanar probes, and high-speed cable is used to measure chip performance as can be seen from Fig. 2.21. The input signal for the fabricated *K*-band ILFT is from an analog signal generator and is connected to a 180° hybrid coupler. The output power is measured by a spectrum analyzer. Because the maximum available frequency of 180° hybrid coupler is lower than *K*-band ILFT output frequency, the differential output cannot be measured. A waveguide harmonic mixer is used to measure the output power of the fabricated *V*-band ILFT.

Additionally, due to the higher cable loss of input signal for the *V*-band ILFT, a microwave system amplifier is used to compensate the loss.

The phase and magnitude imbalance of the input differential signals can be tested by combing the differential signals. Ideally, the summation of differential signals is zero. In other words, if the phase or magnitude is imbalance, the summation of differential signals is nonzero. The phase and magnitude imbalances can be minimized by using phase shift and power attenuator.

2.3.1 *K*-band ILFT

The fabricated *K*-band ILFT starts to oscillate at a bias current of 0.79 mA from 1.5 V. The measured output spectra of the *K*-band ILFT versus the output frequency under free-running and locked conditions with probe and cable losses and input bias V_{BIAS} of 0.56 V are shown in Figs. 2.22 and 2.23, respectively. The measured peak output power is –11.76 dBm at 26.32 GHz under free-running condition and –8.09 dBm at 26.32 GHz under locked condition with input power of 4 dBm, input bias V_{BIAS} of 0.56 V, and 4.7-dB power loss from cable and probe. Because of the contribution of input power, the locked ILFT has a higher output power than the free-running ILFT.

The simulated and measured input power versus the output frequency with the input bias V_{BIAS} of 0.56 V and external tuning voltage V_{TUNE} of 1.5 V is shown in Fig. 2.24. The upper and lower locking ranges are labeled as the maximum and minimum output frequencies under locked condition, respectively. The simulated and measured locking ranges versus input power are shown in Fig. 2.25 where the measured locking range is from 156 to 567 MHz while the input power varies from –9 to –1 dBm. At an input power greater than 0 dBm, the locking range decrease slightly, as shown in Fig. 2.25. With small input power, the measurement result is close to the simulation result.

With large input power, the measured locking range is smaller by 100 MHz. This is because the valid frequency range of the simulation model is not completely covered with the desired frequency range.

The locking range is mainly determined by two important factors. One is the nonlinear term a_3 of the frequency pre-generator whereas the other is the nonlinear characteristic of the ILO. As input power is small, the linear model of the ILO is valid. Thus, the locking range is dominated by the nonlinear term a_3 as can be seen from (2.15). As the input signal is increased, the locking range is increased due to the increase of V_i and a_3. If the input signal is increased to a moderate value which causes the conduction angle smaller than 250°, this leads to the large decrease of a_3 as can be seen from Fig. 2.4. The locking range is, therefore, almost saturated.

The simulated and measured locking range versus the input bias voltage V_{BAIS} of M1/M2 with input bias V_{BIAS} of 0.65 V and tuning voltage V_{TUNE} of 1.5 V are shown in Fig. 2.26. It can be seen from Fig. 2.26 that the locking range increases with a decrease in the input bias. This result can be explained by the fact that the lower input bias allows only a small current through M3/M4. Thus, the weaker negative-resistance generated from M3/M4 reduces the effective quality factor of *LC*-tank. Besides, the conversion gain of the frequency pre-generator is a function of input bias V_{BIAS}. Therefore, the locking range is increased at the higher third-order harmonic current region as can be seen from Fig. 2.4.

The varactors C1/C2 are designed in the *K*-band ILFT. In Fig. 2.27, the total output frequency under locked condition is 3920 MHz as the varactors tuning voltage V_{TUNE} varies from 0 to 1.5 V with a dc power consumption of 2.95 mW and an input power of 4 dBm. The output frequency range of the *K*-band ILFT under free-running condition is from 24.08 GHz to 26.27 GHz. With a 4-dBm input signal, the output

frequency range of the *K*-band ILFT under locked condition is from 22.58 GHz to 26.50 GHz. Therefore, the output frequency range extends from 2190 MHz to 3920 MHz.

The measured phase noises of the reference input, free-running output, and locked output from 1 kHz to 10 MHz is shown in Fig. 2.28. It shows that the phase noise difference between the reference input and the locked output is 10.5 dB from 1 kHz to 1 MHz offset. The slightly larger output phase noise at a signal frequency higher than 1 MHz offset is due to excess noise from the internal circuit and output buffer. The spur at around 1MHz offset is from signal generator.

The measured output phase noise as a function of input power is shown in Fig. 2.29. At large input power levels, the measured phase noise of the locked output can approach the theoretical limit of $10\log(3^2) = 9.5$ dB, as derived in Section 2.1. The phase noise degradation from the frequency pre-generator is 0.8 dB at 1-kHz offset and 1.5 dB at 100-kHz offset, respectively. In addition, the phase noise at small frequency offset can be close to the theoretical limit as compared to that at large frequency offset with the same input incident amplitude V_i due to the low pass frequency response.

The measured output spectrum is shown in Fig. 2.30 where the HRRs compared to the desired third-order harmonic are 22.65, 30.58, 29.29, 40.35 dBc for the first, second, forth, and fifth harmonics, respectively. The HRRs of even-order harmonics are 6.64-dB higher than those of odd-order harmonics because of the common-mode rejection capability of R1. In general, R1 does not affect the output performance for odd-order harmonics.

Finally, the measurement of reference input and locked output waveforms are

also tested by the oscilloscope. The measured output waveform with cables and probe losses, input bias V_{BIAS} of 0.65 V, and tuning voltage V_{TUNE} of 1.5 V is shown in Fig. 2.31. Due to the phase shift from the cables, the phase relation between input and output signal as shown from oscilloscope is not exactly the same as those of *K*-band ILFT. It can be seen from Fig. 2.30 that the locked *K*-band ILFT can provide a stable output waveform with the three time frequency of input signal.

2.3.2 *V*-band ILFT

The *V*-band ILFT starts to oscillate at a bias current of 1.55 mA from 1.2 V. The measured output spectra of the *V*-band ILFT versus the output frequency under free-running and locked conditions with probe and cable losses are shown in Figs. 2.32 and 2.33, respectively. The loss from the external waveguide subharmonic mixer is de-embedded by the spectrum analyzer. The measured peak output power is –16.14 dBm at 60.025 GHz under free-running condition and –14.81 dBm at 60.025 GHz under locked condition with 4-dBm input power, a V_{BIAS} of 0.55 V, and 9.6-dB power loss from cable and probe.

The measured input power versus the output frequency when the input bias V_{BIAS} is set at 0.55 V are shown is Fig. 2.34. It can be seen from Fig. 2.35 that the locking range achieves 1422 MHz with 6-dBm input power and 1662 MHz with 9-dBm input power. As the input power is smaller than 1 dBm, the ILO stage is linear and a_3 is nearly constant. Thus, the locking range is increased with V_i. With the input power greater than 1 dBm, the locking range is nearly saturated because of the large decrease of the nonlinear term a_3. If the input signal is increased to be larger than 2 dBm, the ILO becomes nonlinear and (2.15) is not valid. Under this condition, the extra third-order harmonic is generated by the nonlinear ILO. Therefore, the locking range is increased instead of saturated.

The measurement setup for output phase noise with external down-conversion mixer is shown in Fig. 2.36. A power splitter is required for the operation of instrument. The measured phase noises of the reference input, free-running output, and locked output from 1 kHz to 10 MHz is shown in Fig. 2.37. The noise contribution for external down-conversion mixer is not de-embedded. It shows that the phase noise difference between the reference input and the locked output is 10 dB from 1 kHz to 500 kHz offset. The slightly larger output phase noise at a signal frequency higher than 500 kHz offset is due to excess noise from the internal circuit. Because the phase noise measurement with ultra low noise floor and a cross-correlation method can be provided by the signal source analyzer, the measured value of the output phase noise can be lower than –155 dBc as shown in Fig. 2.37.

The measurement of reference input and locked output waveforms are tested by the high-speed wideband sampling oscilloscope. The measured output waveform with cables and probe losses is shown in Fig. 2.38. Due to the phase shift from the high-speed cables, the phase relation between input and output signal as shown from oscilloscope is not exactly the same as those of *V*-band ILFT. It can be seen from Fig. 2.38 that the output waveform is similar to the simulated result as shown in Fig. 2.15.

Due to the limitations of the instruments currently available, the HRR can not be measured. From the simulation results, the HRRs are higher than 18.9 dBc for every undesired harmonics.

In Table 2.2, the recently published CMOS subharmonic ILFMs are compared with the proposed ILFTs. It can be seen that the proposed ILFTs, in contrast to the corresponding CMOS subharmonic ILFMs, can operate with lower dc power consumption. Moreover, this design is the first CMOS ILFT operated in the millimeter-wave band.

As compared with the work in [23], the locking range is around six-times of the proposed work in this chapter. Because low quality factor of *LC*-tank is chosen and the output power in [23] is only one-third that of the proposed work, the locking range can be larger than the proposed work as shown in (2.15). In addition, the method for the generation of third-order harmonic signal is different. The characteristic of third-order harmonic generation devices can affect the output amplitude directly as shown in Fig. 2.39 where the signal v_{in} is the input signal for quadrature signal generation.

The published bulk-CMOS VCOs worked at the *K*-band and *V*-band listed in Table 2.3 are compared with the proposed ILFTs. It can be seen that the locking range of the proposed ILFT is similar to the tuning range of a bulk-CMOS VCO. The proposed ILFT can provide similar output power with lower power consumption even when the input power P_{INJ} is considered as compared with the corresponding bulk-CMOS VCOs.

The simulation and measurement results have shown that the proposed ILFTs can achieve high output power and low power consumption. However, the locking range of ILFT still can not be larger than 10-GHz even if the quality factor of *LC*-tank is decreased. The main reason is that the large parasitic capacitances between frequency pre-generator stage and ILO stage. The generated third-order harmonic signal is leaked to substrate. Thus, the locking range expressed in (2.15) should be considered the effect. To achieve larger locking range, the transformer can be designed to increase the injection current as can be seen from Fig. 2.40.

2.4 SUMMARY

A millimeter-wave CMOS subharmonic ILFT with a triple-frequency pre-generator is proposed and analyzed. A model for the proposed ILFT is developed to calculate both the locking range and the output phase noise. Based on the model, the design guideline for the maximization of the locking range and the minimization of the output phase noise is developed. The quality factor of the *LC*-tank of the ILO stage and the conversion gain of the frequency pre-generator stage are maximized to obtain a wider locking range, higher output voltage, and lower output phase noise with low dc power consumption.

According to the developed design guidelines, both the *K*-band and *V*-band CMOS ILFTs have been designed and fabricated using 0.18-μm and 0.13-μm technologies, respectively. As seen from the measurement results, the fabricated CMOS *K*-band ILFT can achieve the locking range of 4.83 % with 4-dBm input injection power and 0.45-mW dc power consumption. Moreover, the locking range of 15.06 % is performed using varactors. The fabricated *V*-band CMOS ILFT has a locking range of 2.3 % with 6-dBm input injection power and 1.86-mW dc power consumption. The measurement results have verified the performance of the proposed ILFTs.

Since it is feasible to design a high-performance VCO at low frequency without the use of full-speed frequency dividers, the proposed CMOS ILFT offers great potential application in LO signal generators for frequency synthesizers in the millimeter-wave band or even in the sub-millimeter-wave band.

Table 2.1

Dimensions of devices in (a) *K*-band ILFT and (b) *V*-band ILFT.

(a)

Device	Dimension
M1 / M2	(1.5 μm / 0.18 μm)× 24
M3 / M4	(3 μm / 0.18 μm)× 8
M5 / M6	(4 μm / 0.18 μm)× 6
C1 / C2	(3 μm / 0.18 μm)× 20
L1 / L2	Metal width = 15 μm Radius = 80 μm Turn = 1
R1	87.6 Ω

(b)

Device	Dimension
M1 / M2	(1.4 μm / 0.13 μm)× 12
M3 / M4	(1.5 μm / 0.13 μm)× 6
M5 / M6	(1.5 μm / 0.13 μm)× 8
L1 / L2	Metal width = 9 μm Radius = 33 μm Turn = 1
R1	55.7 Ω

Table 2.2

Comparison with published subharmonic ILFMs.

Ref.	Tech.	Freq. (GHz)	Type	Locking Range / Input Power (MHz / dBm)	Output Power (dBm)	Supply (Volt)	P_{DISS} (mW)
This Work	0.18-μm CMOS	26.5	× 3	1092 / 4	-8.09	1.5	0.45
This Work	0.18-μm CMOS	26.5	× 3	3915[a] / 4	-6.85	1.5	2.95
This Work	0.13-μm CMOS	60.0	× 3	1422 / 6	-14.8	1.2	1.86
[20]	0.35-μm CMOS	2.4	× 2	151 / 2	-33.91	3.3	4.95
[21]	0.18-μm CMOS	3.2	× 2	1100 / 6	-17	1.0	2.2
[21]	0.18-μm CMOS	4.8	× 3	600 / 6	-12	1.0	3.7
[22]	0.18-μm CMOS	4.8	× 3	100.8 / 6	N/A	N/A	1.47
[23]	0.09-μm CMOS	60.5	× 3	9000 / 1	-27.26	1.0	9.6
[24]	0.18-μm CMOS	61.2	× 4	3640 / 12	-34.92	2.0	9.8

a The tuning varactor is used.

Table 2.3

Comparison with published bulk-CMOS VCOs.

Ref.	Tech.	Freq. (GHz)	Tuning Range (MHz)	Locking Range (MHz)	Supply (Volt)	P_{DISS} / P_{INJ} (mW / dBm)	Output Power (dBm)
This Work	0.18-μm CMOS	26.5	-	1092	1.5	0.45 / 4	-8.09
This Work	0.18-μm CMOS	26.5	-	3915	1.5	2.95 / 4	-6.85
This Work	0.13-μm CMOS	60.0	-	1422	1.2	1.86 / 6	-14.8
[72]	0.18-μm CMOS	19.9	510	-	1.8	32.0 / -	-3.0
[73]	0.18-μm CMOS	25.1	3012[a]	-	2.2	11.0 / -	-29.77
[74]	0.10-μm CMOS	25.9	600	-	1.5	24.0 / -	-22.0
[7]	0.12-μm CMOS	51.6	700[b]	-	1.0	1.0 / -	-30.0
[8]	0.09-μm CMOS	60.0	100	-	1.0	1.9 / -	-30.5
[9]	0.13-μm CMOS	59.5	5800[c]	-	1.5	9.6 / -	-10.0

a The tuning voltage is 4 V and higher than supply voltage.

b The tuning voltage is 1.5 V and higher than supply voltage.

c Two stage output buffer is used for low output loading of VCO.

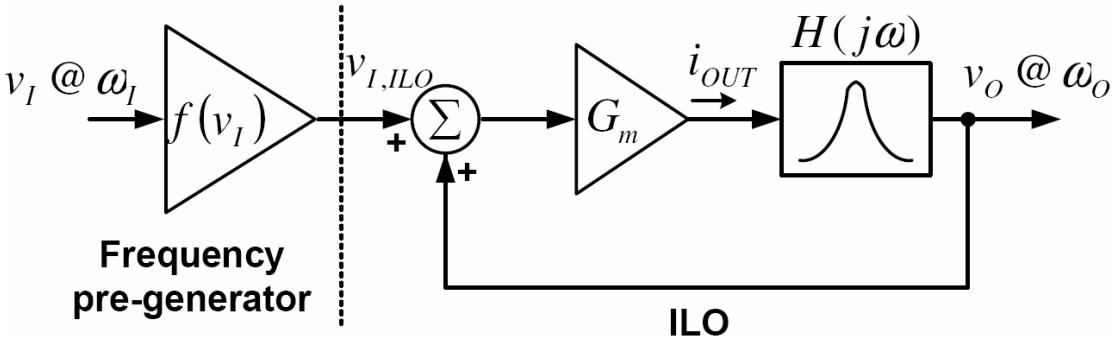


Fig. 2.1 The model of the proposed ILFT.

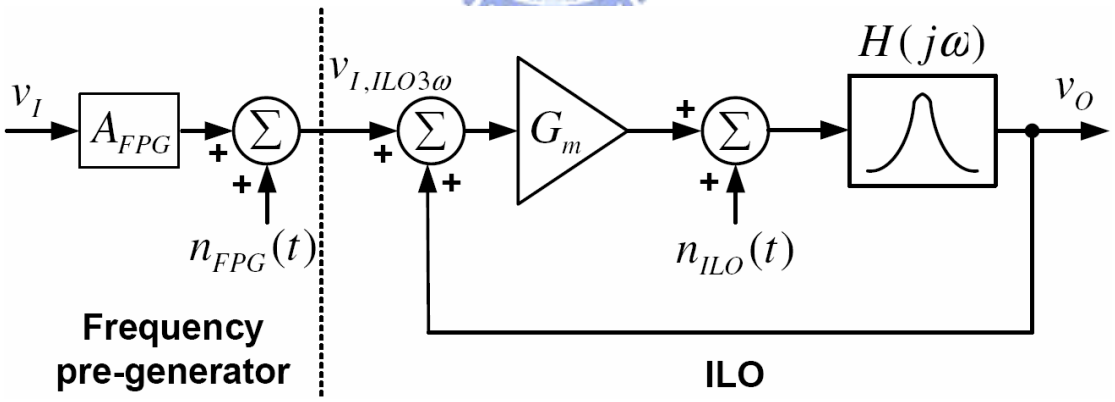


Fig. 2.2 Simplified noise source model in the proposed ILFT.

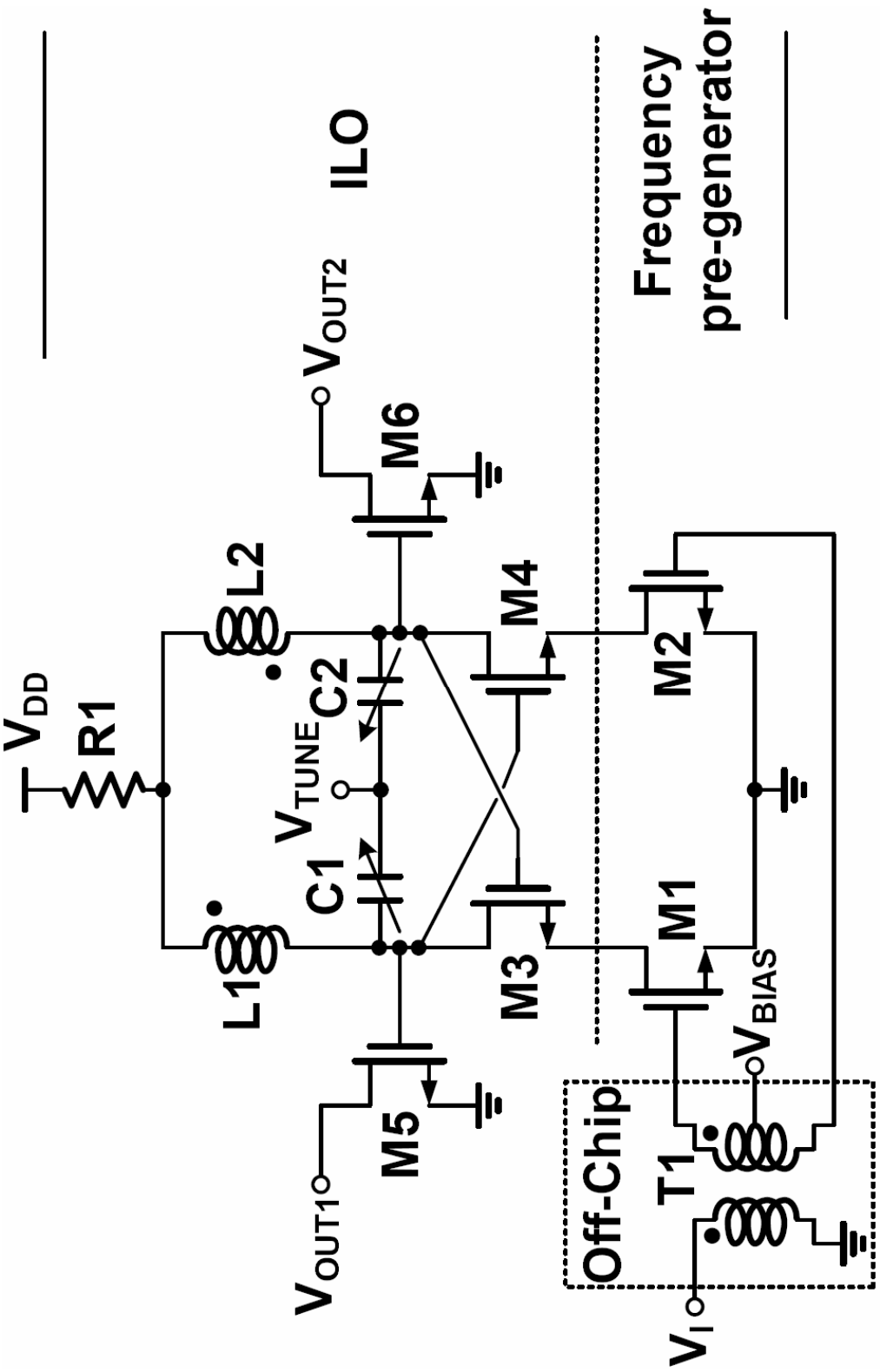


Fig. 2.3 The schematic of the proposed ILFT.

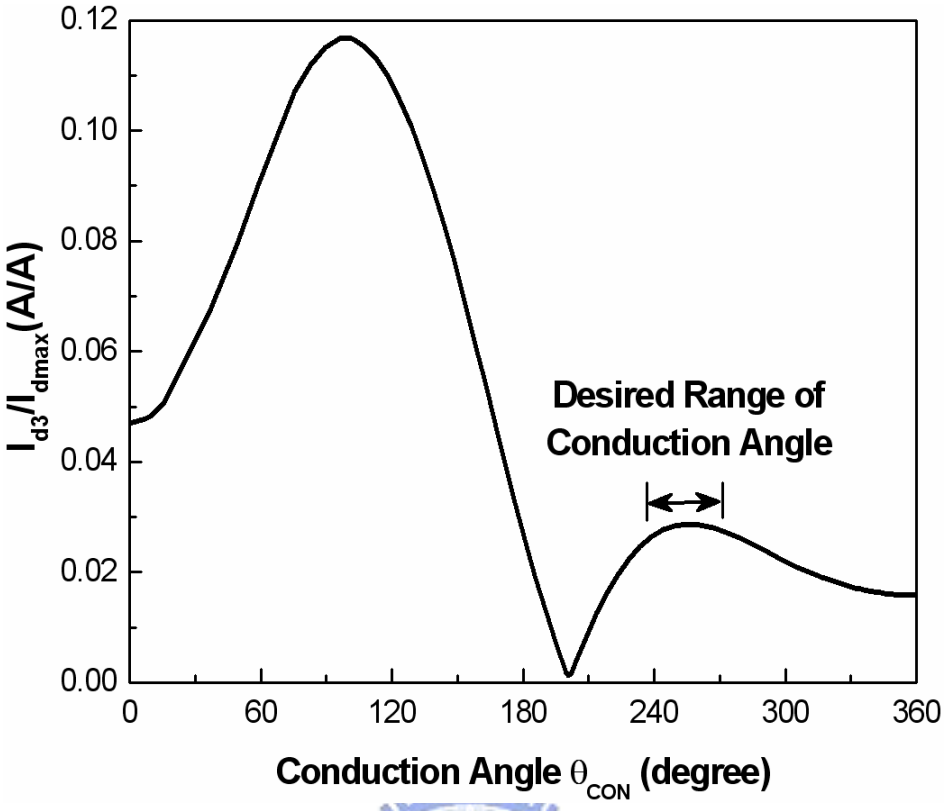


Fig. 2.4 HSPICE simulated coefficient of output harmonic current as a function of conduction angle.

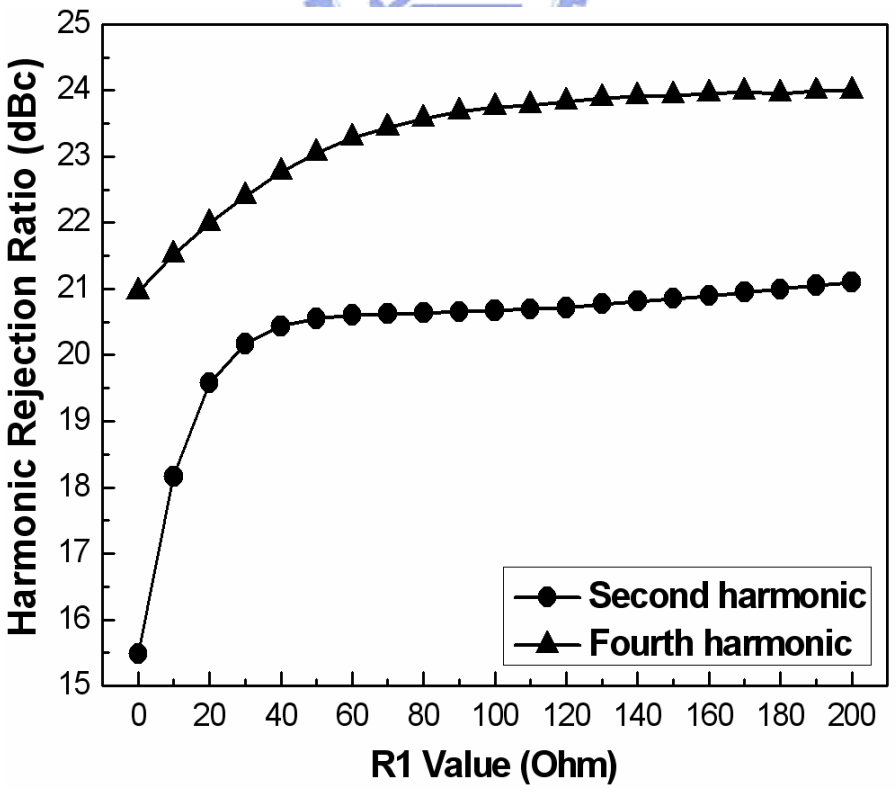


Fig. 2.5 HSPICE simulated HRRs for various value of R1 for *K*-band ILFT..

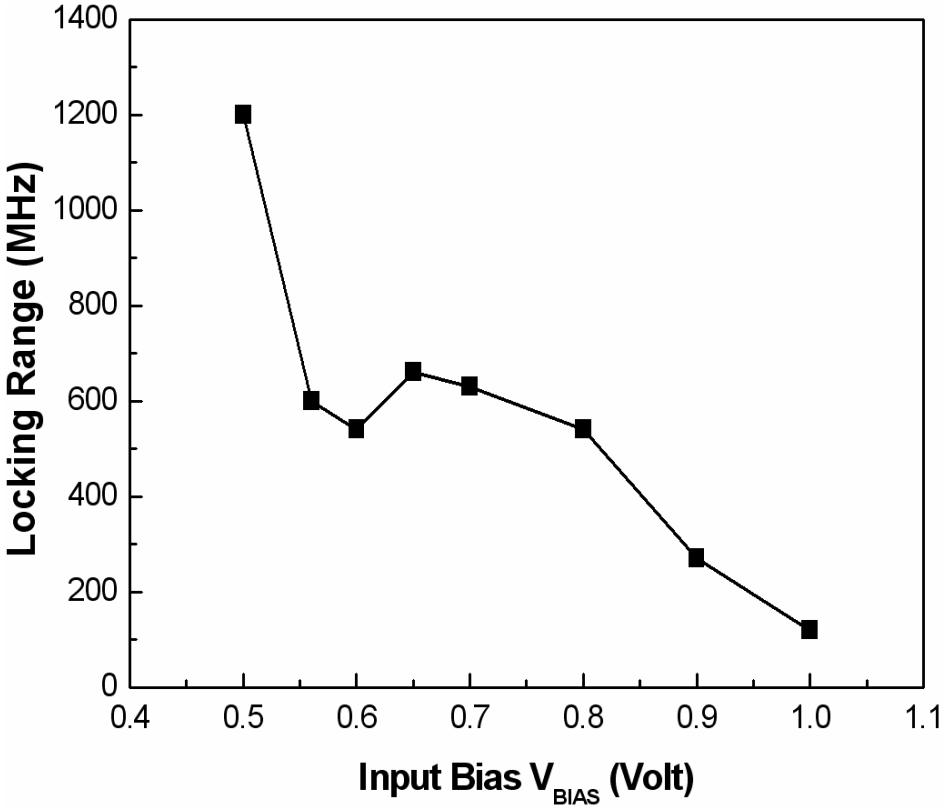


Fig. 2.6 Simulated locking range as a function of input bias V_{BIAS} for *K*-band ILFT.

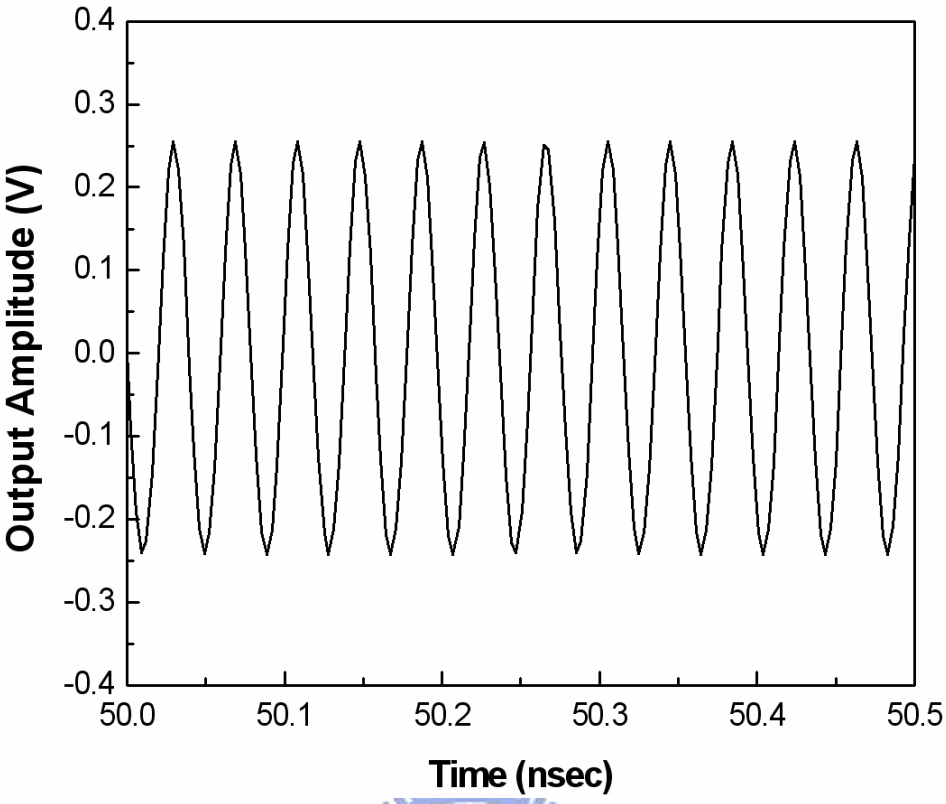


Fig. 2.7 The transient simulation of the free-running *K*-band ILFT.

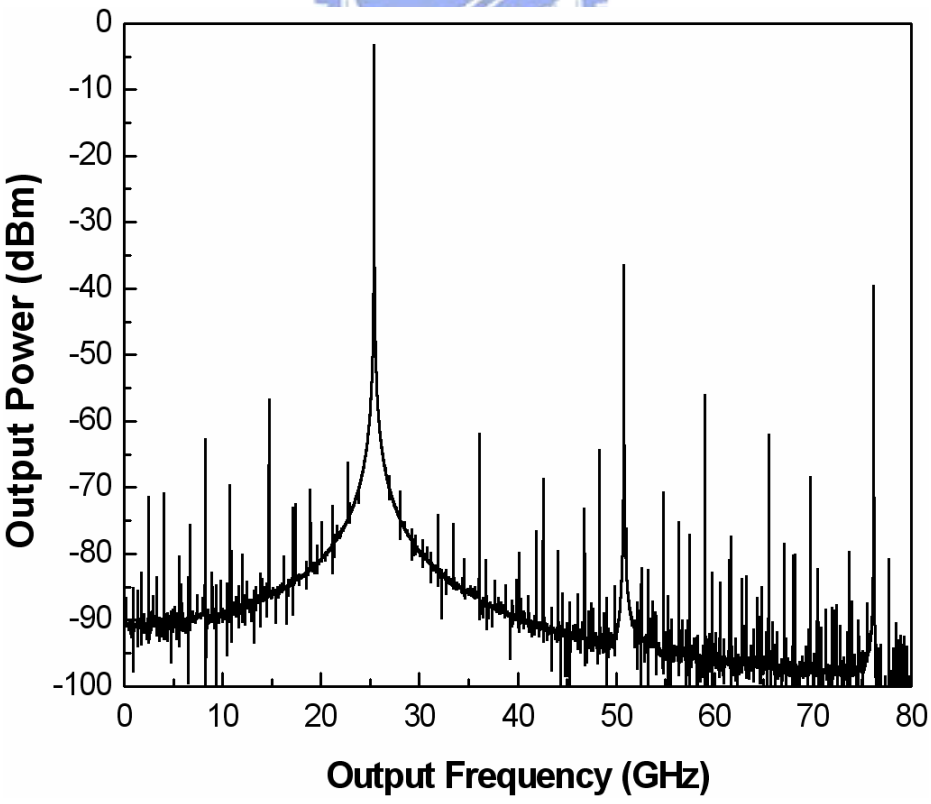


Fig. 2.8 Simulated output spectrum of the free-running *K*-band ILFT.

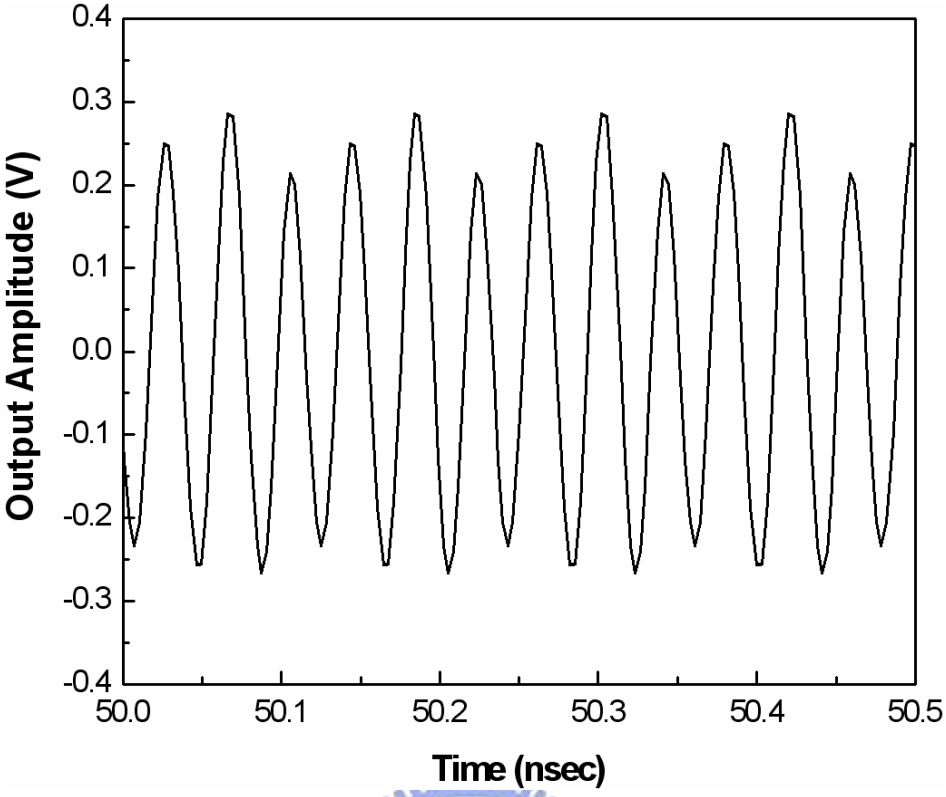


Fig 2.9 The transient simulation of the locked *K*-band ILFT with 4-dBm input power, 0.65-V V_{BIAS}, and 8.48-GHz input frequency.

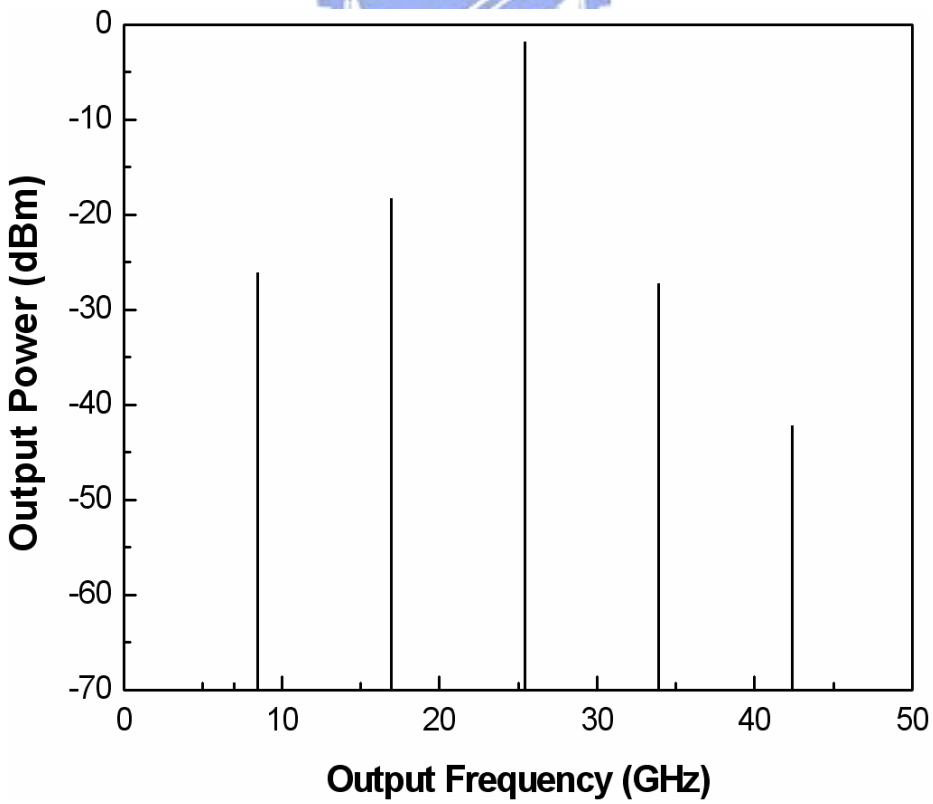


Fig. 2.10 Simulated output spectrum of the locked *K*-band ILFT with 4-dBm input power, 0.65-V V_{BIAS}, and 8.48-GHz input frequency.

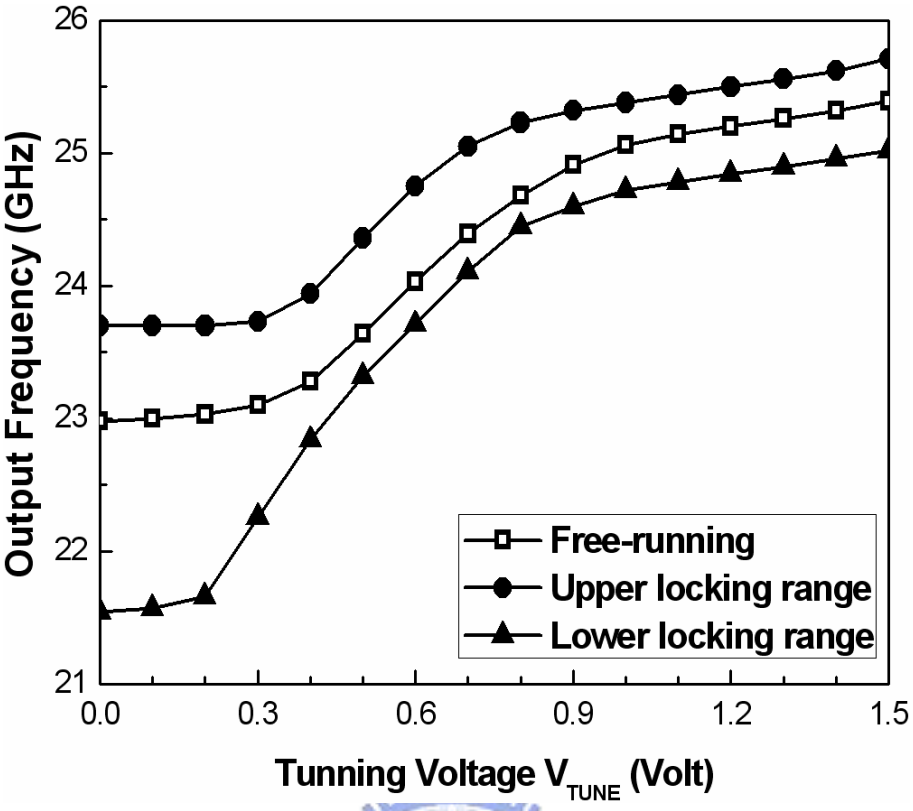


Fig. 2.11 Simulated tuning voltage V_{TUNE} versus output frequency with 0.65-V V_{BIAS} and 4-dBm input power for *K*-band ILFT.

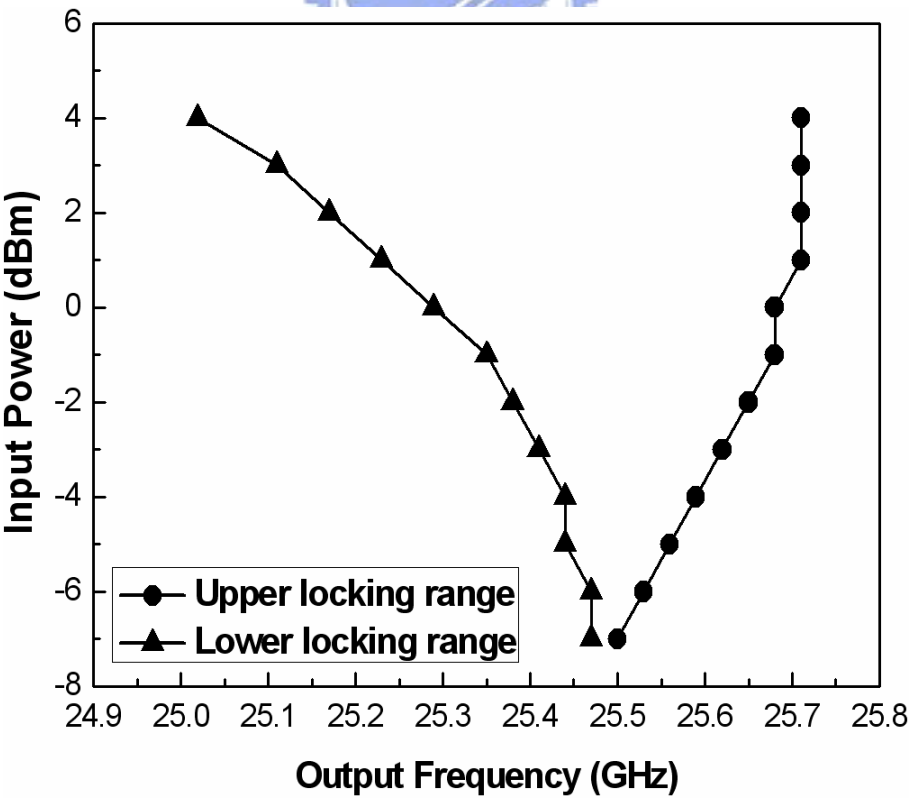


Fig. 2.12 Simulated input power versus output frequency with 1.5-V V_{TUNE} and 0.65-V V_{BIAS} for *K*-band ILFT.

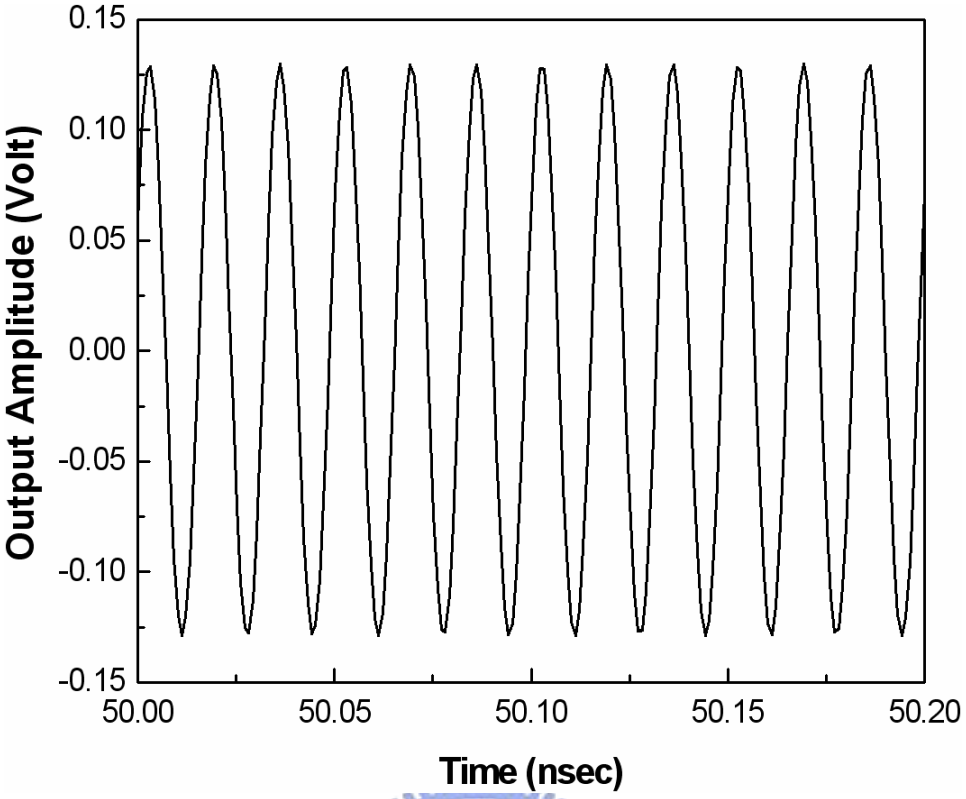


Fig. 2.13 The transient simulation of the free-running *V*-band ILFT.

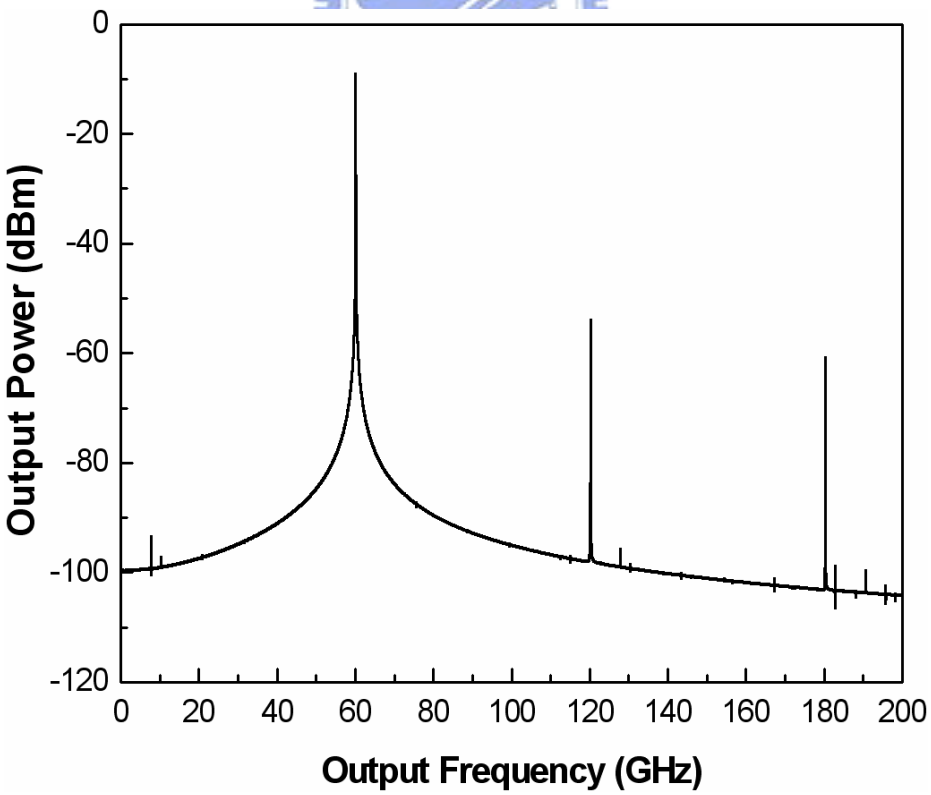


Fig. 2.14 Simulated output spectrum of the free-running *V*-band ILFT.

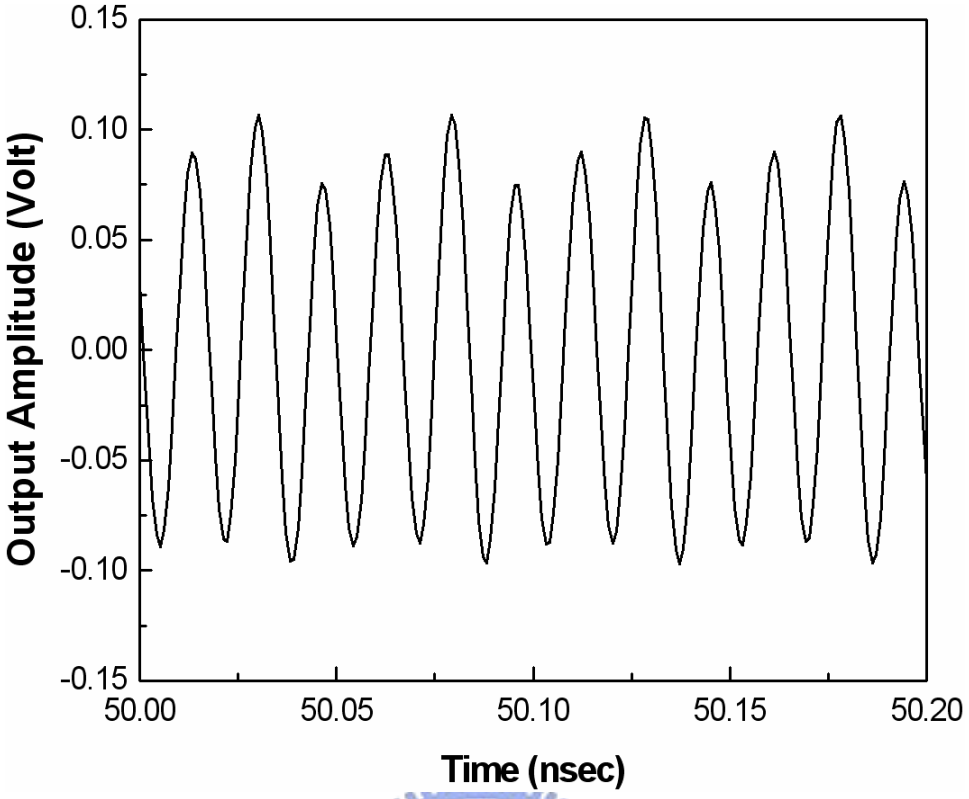


Fig. 2.15 The transient simulation of the locked *V*-band ILFT with 6-dBm input power, 0.55-V V_{BIAS}, and 20.3GHz input frequency.

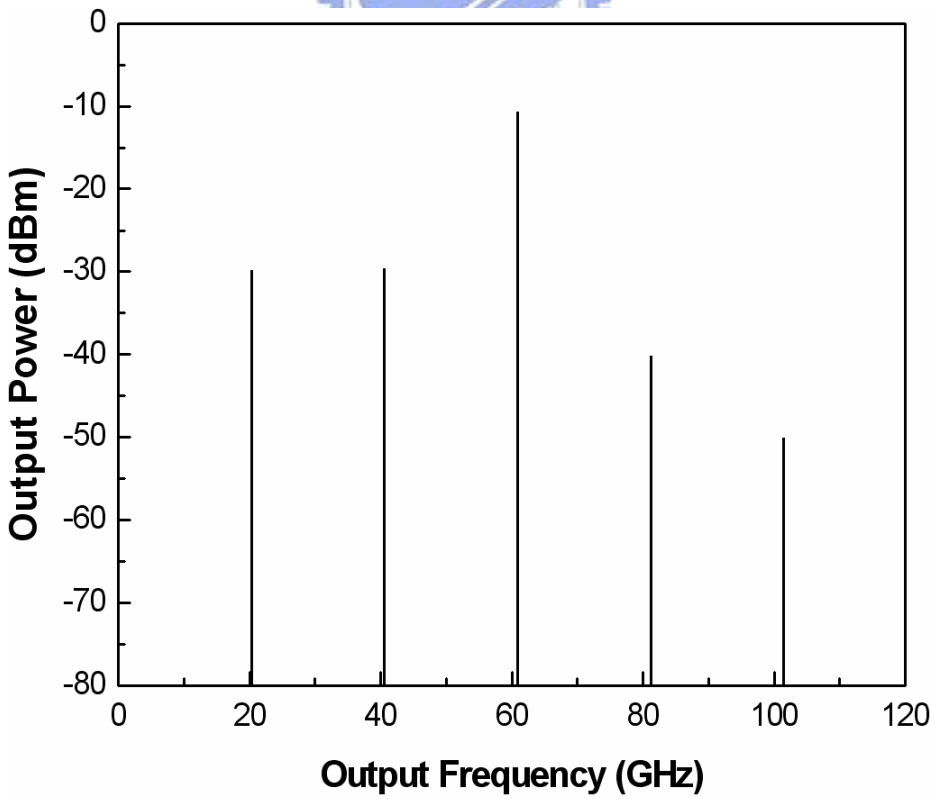


Fig. 2.16 Simulated output spectrum of the locked *V*-band ILFT with 6-dBm input power, 0.55-V V_{BIAS}, and 20.3-GHz input frequency.

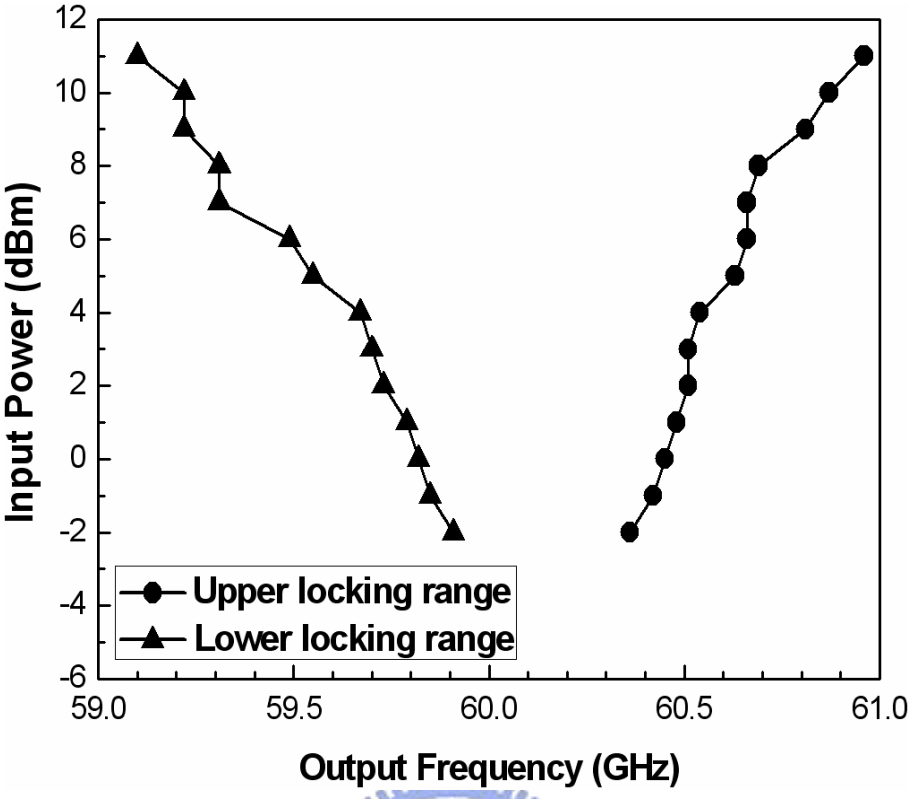


Fig. 2.17 Simulated input power versus output frequency with 0.55-V V_{BIAS} for *V*-band ILFT.

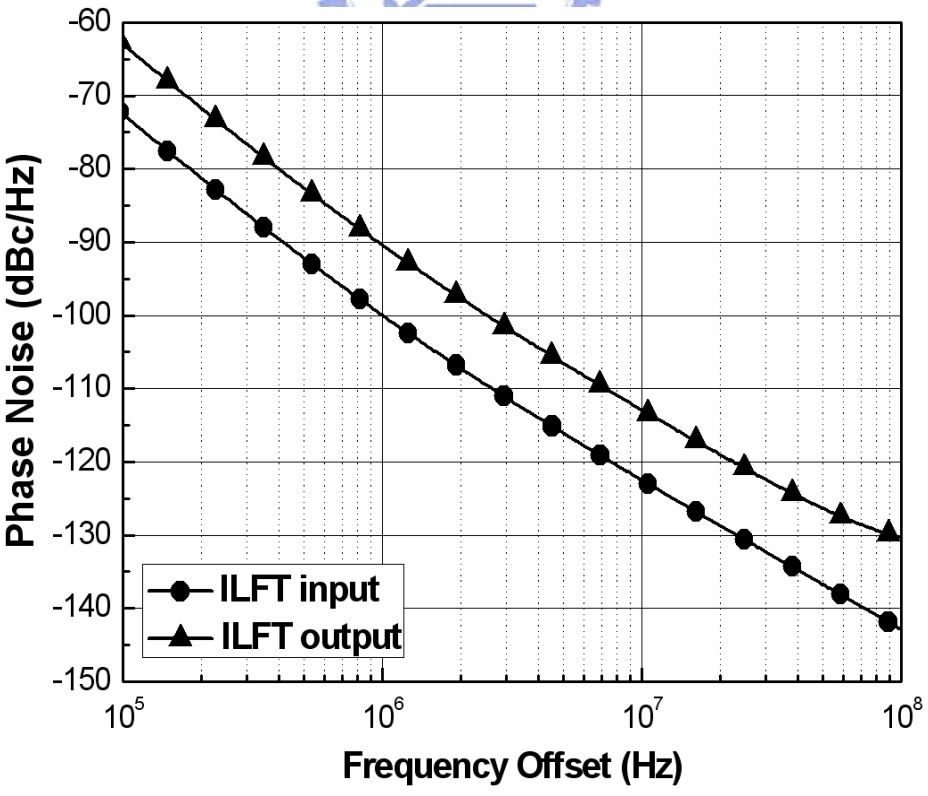


Fig. 2.18 Simulated the phase noise of ILFT input and output for *V*-band ILFT.

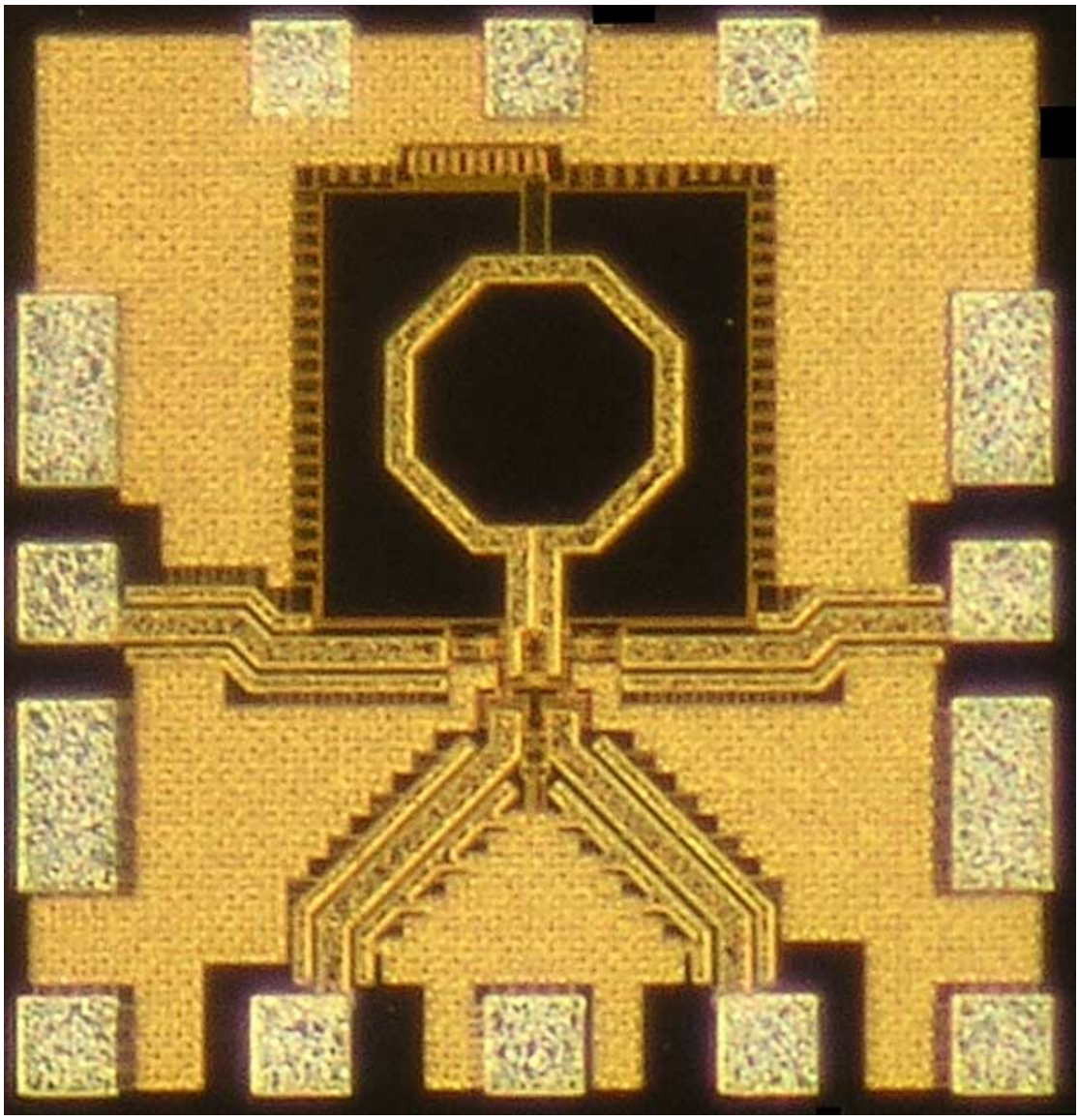


Fig. 2.19 Chip microphotograph of *K*-band ILFT (0.66 mm × 0.69 mm).

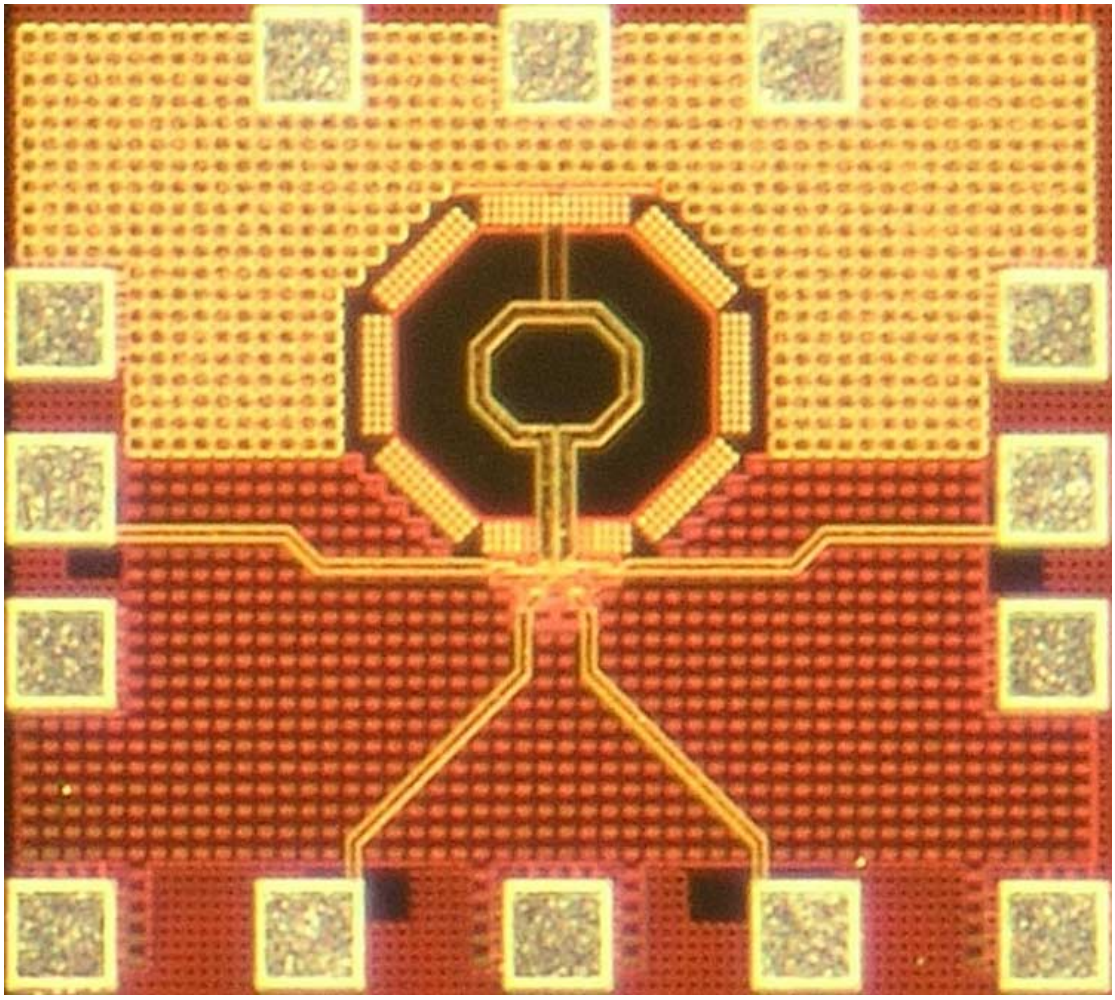


Fig. 2.20 Chip microphotograph of *V*-band ILFT (0.59 mm × 0.66 mm).

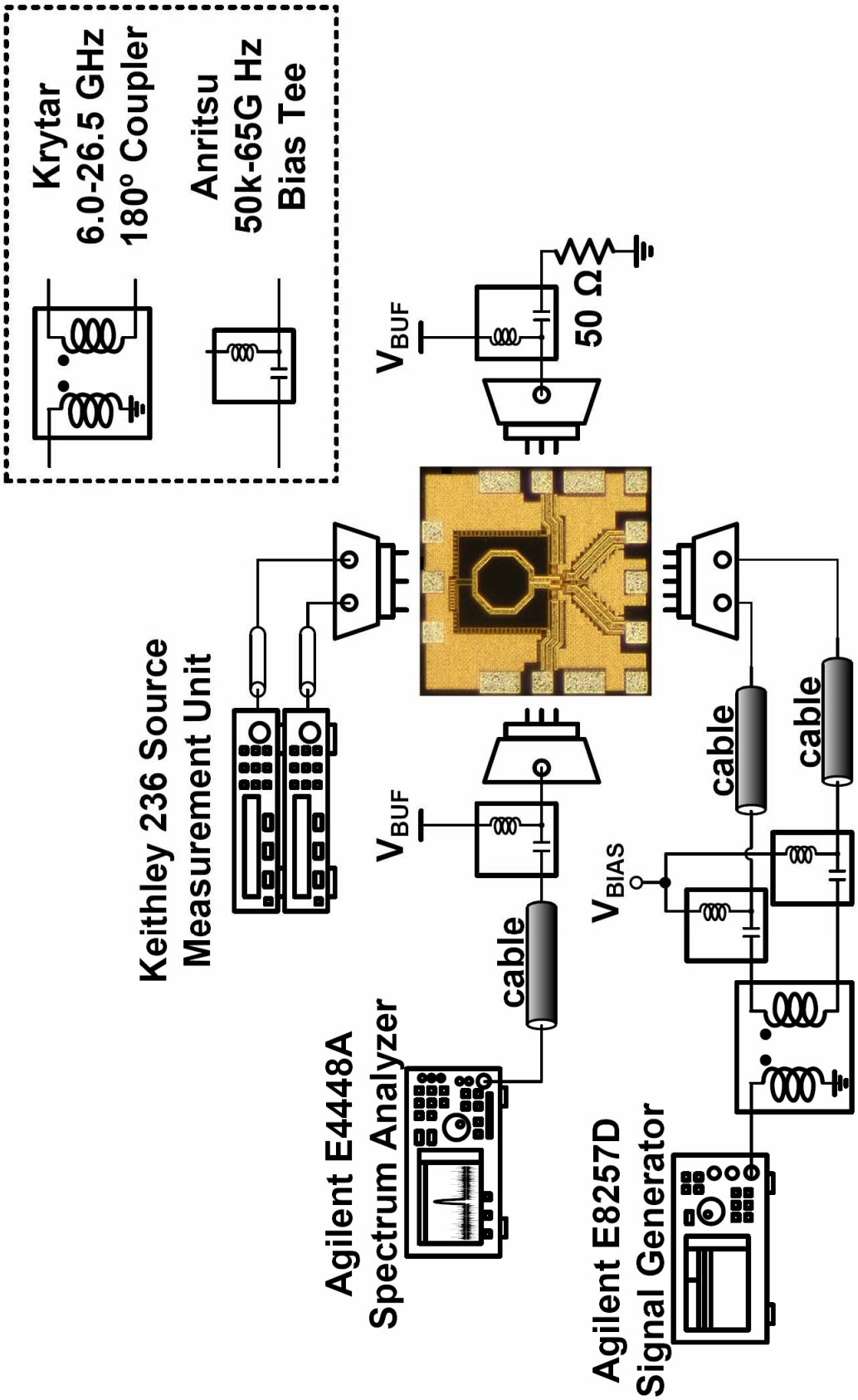


Fig. 2.21 Measurement setup for subharmonic ILFT testing.

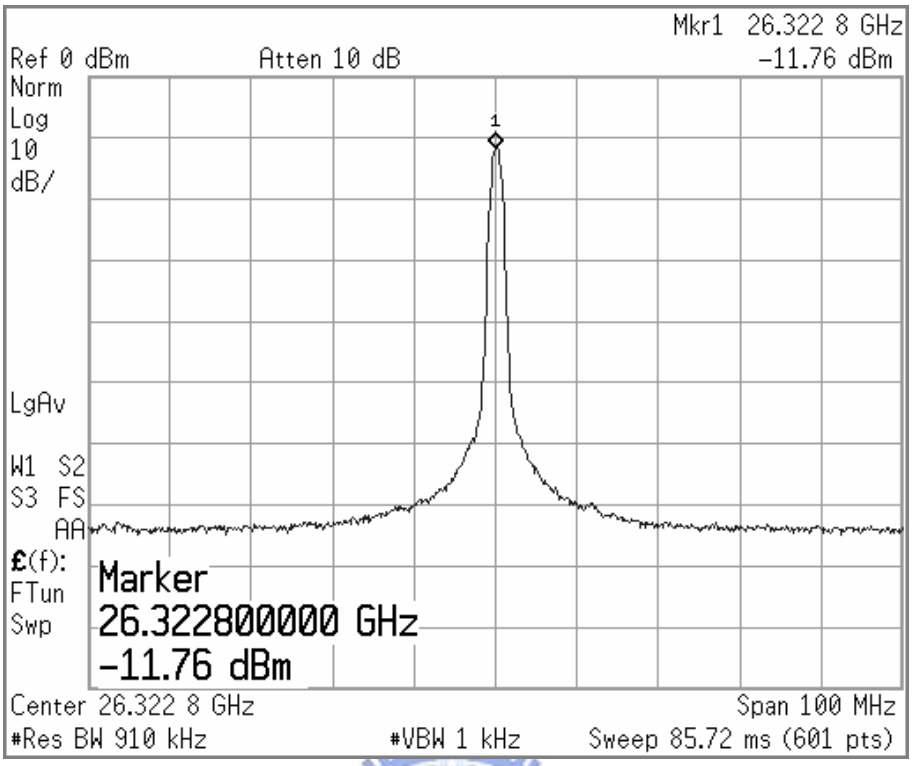


Fig. 2.22 Measured output spectrum of the fabricated *K*-band ILFT under free-running condition with probe and cable losses and V_{BIAS} of 0.56 V.

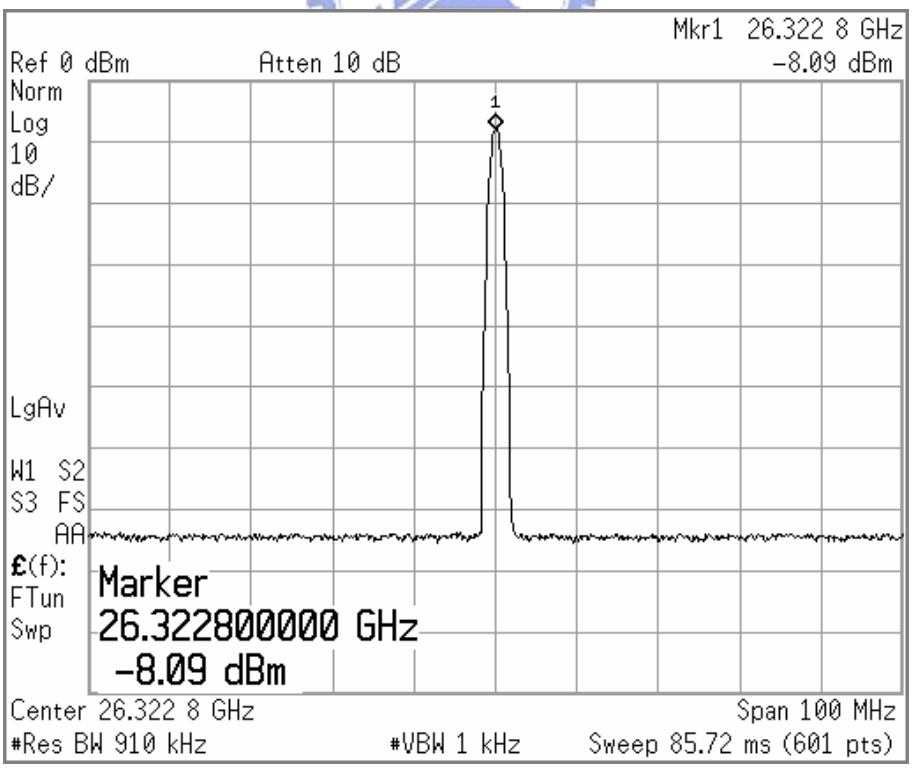


Fig. 2.23 Measured output spectrum of the fabricated *K*-band ILFT under locked condition with probe and cable losses, V_{BIAS} of 0.56 V, and input power of 4 dBm.

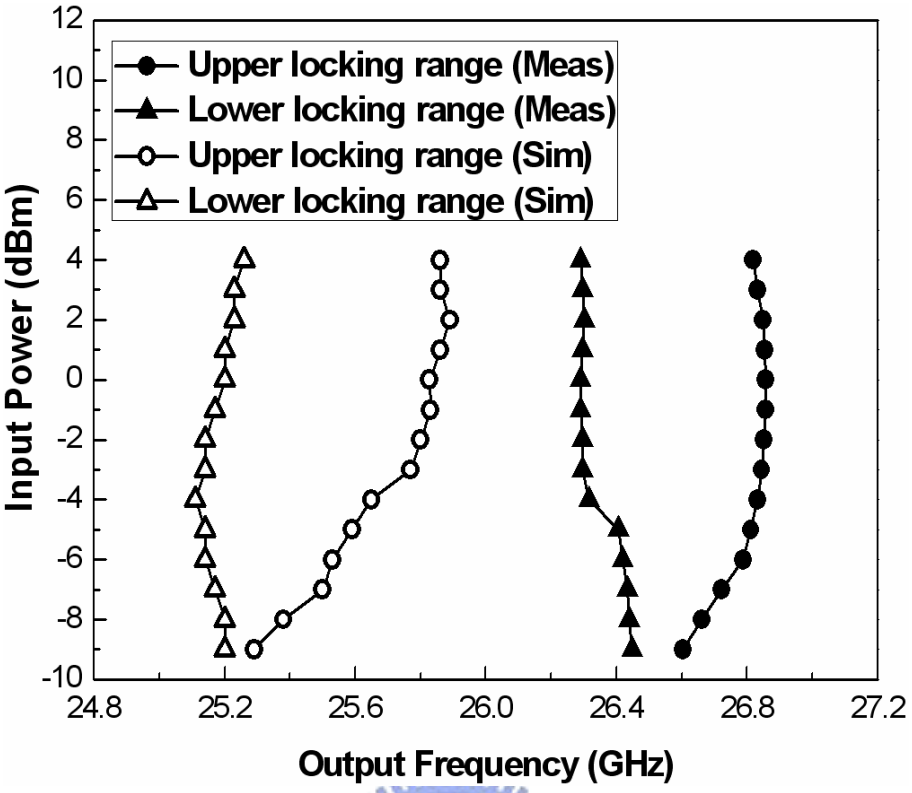


Fig. 2.24 Simulated and measured input powers versus output frequency with 1.5-V V_{TUNE} and 0.56-V V_{BIAS} for *K*-band ILFT.

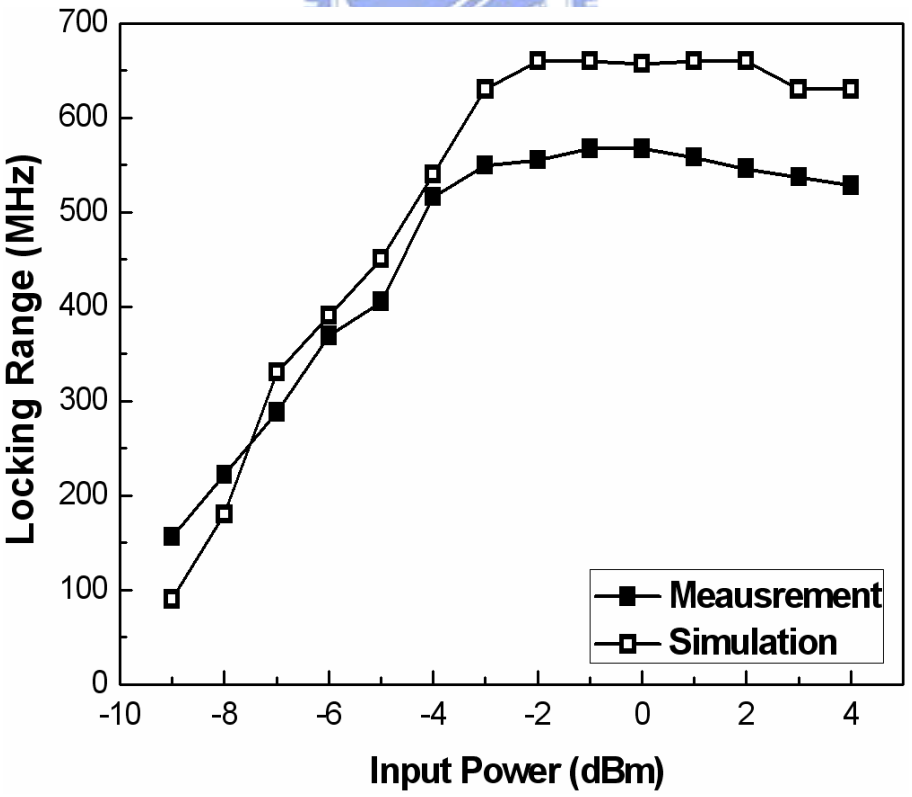


Fig. 2.25 Simulated and measured locking ranges versus input power with 1.5-V V_{TUNE} and 0.56-V V_{BIAS} for *K*-band ILFT.

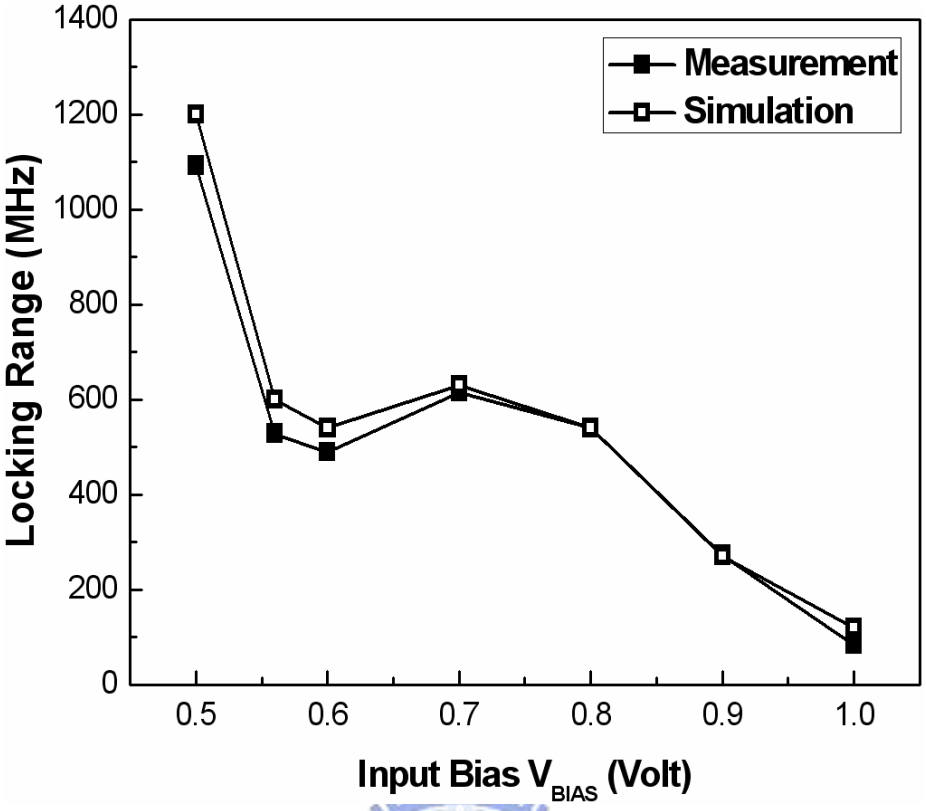


Fig. 2.26 Locking range as a function of input bias V_{BIAS} with 4-dBm input power and 1.5-V V_{TUNE} for *K*-band ILFT.

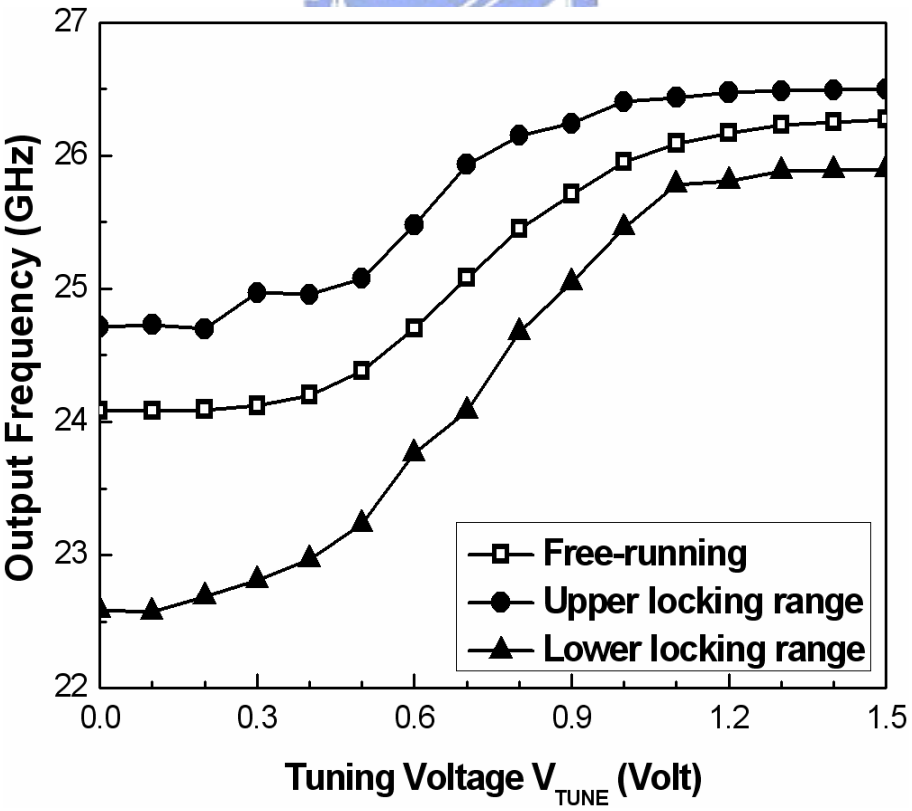


Fig. 2.27 Measured tuning voltage V_{TUNE} versus output frequency with 0.65-V V_{BIAS} and 4-dBm input power for *K*-band ILFT.

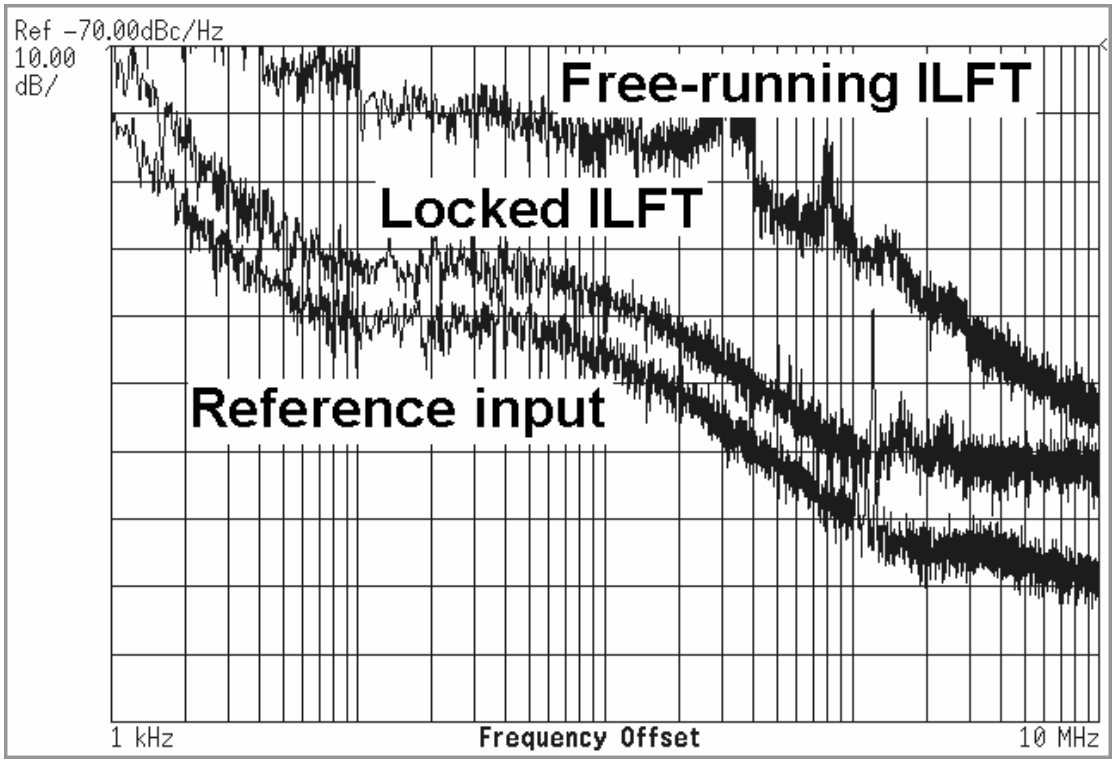


Fig. 2.28 Measured phase noise of reference input, free-running output, and locked output with 0.65-V V_{BIAS} and 4-dBm input power for *K*-band ILFT.

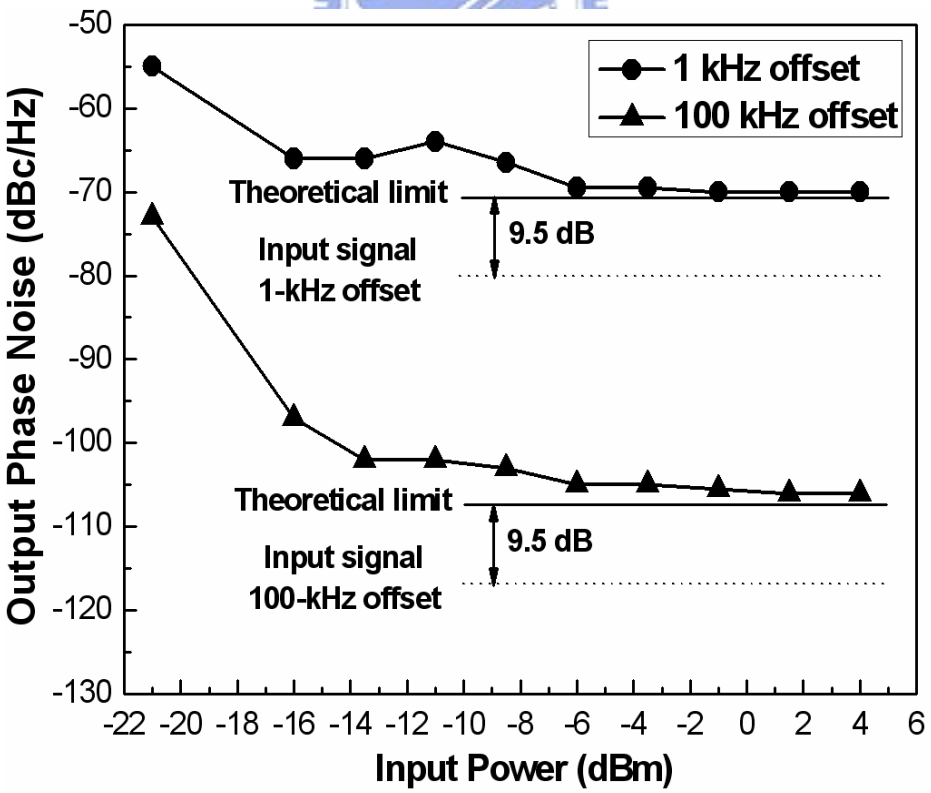


Fig.2.29 Measured phase noise characteristics of locked output as a function of input power with 0.65-V V_{BIAS} for *K*-band ILFT.

Fig 2.30 Measured output power spectra of first, second, third, fourth, and fifth harmonics with 0.65-V V_{BIAS} and 4-dBm input power for *K*-band ILFT.

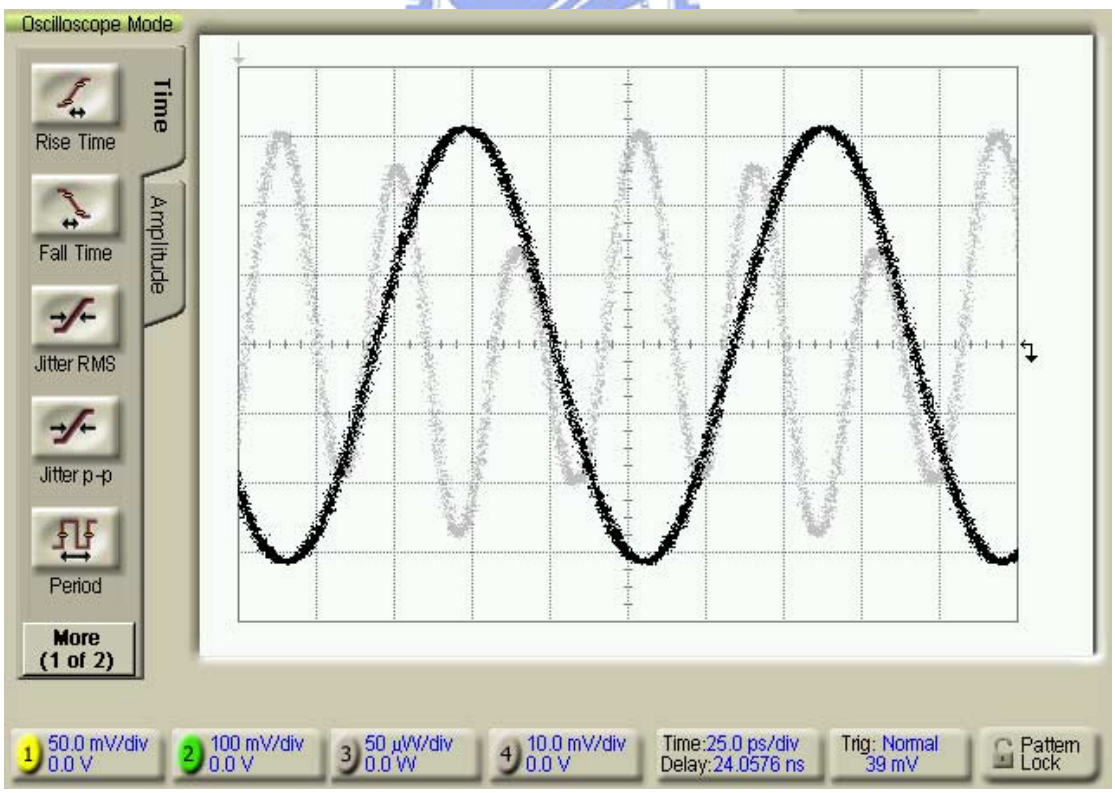


Fig 2.31 Measured input and output waveforms with cables and probe losses, 0.65-V V_{BIAS}, and 1.5-V V_{TUNE} for *K*-band ILFT.

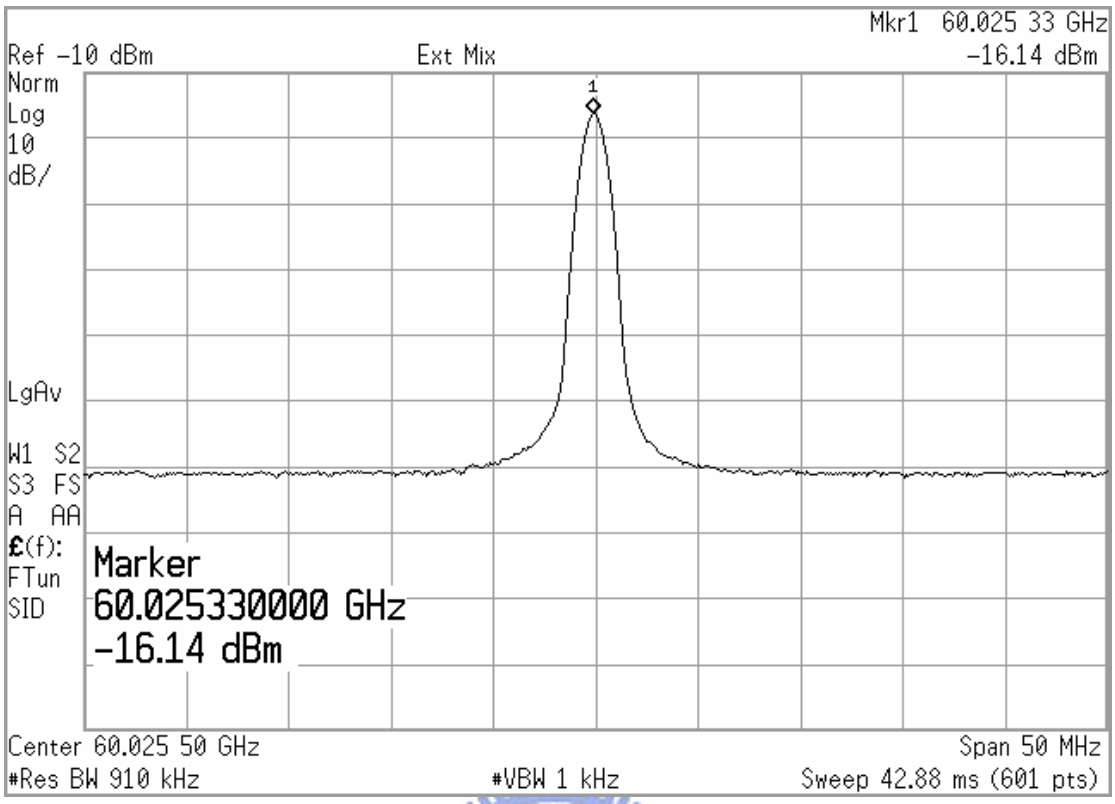


Fig 2.32 Measured output spectrum of the fabricated *V*-band ILFT under free-running condition with probe and cable losses.

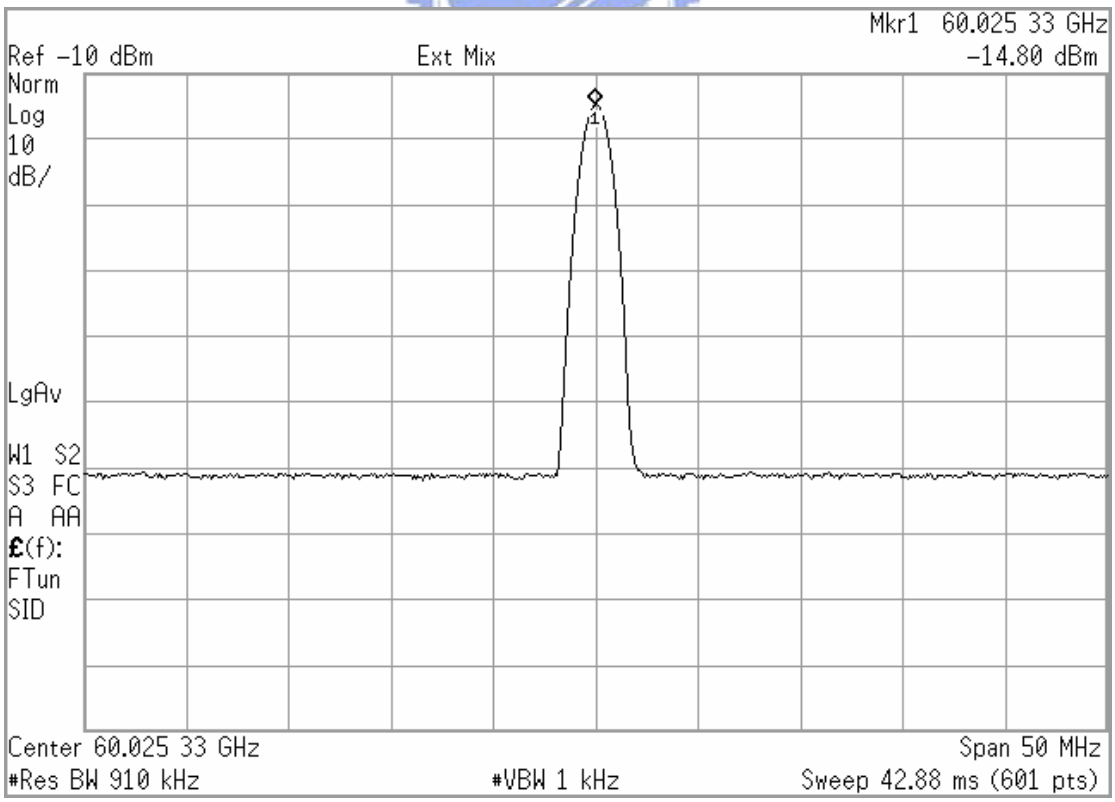


Fig. 2.33 Measured output spectrum of the fabricated *V*-band ILFT under locked condition with probe and cable losses and input power of 4 dBm.

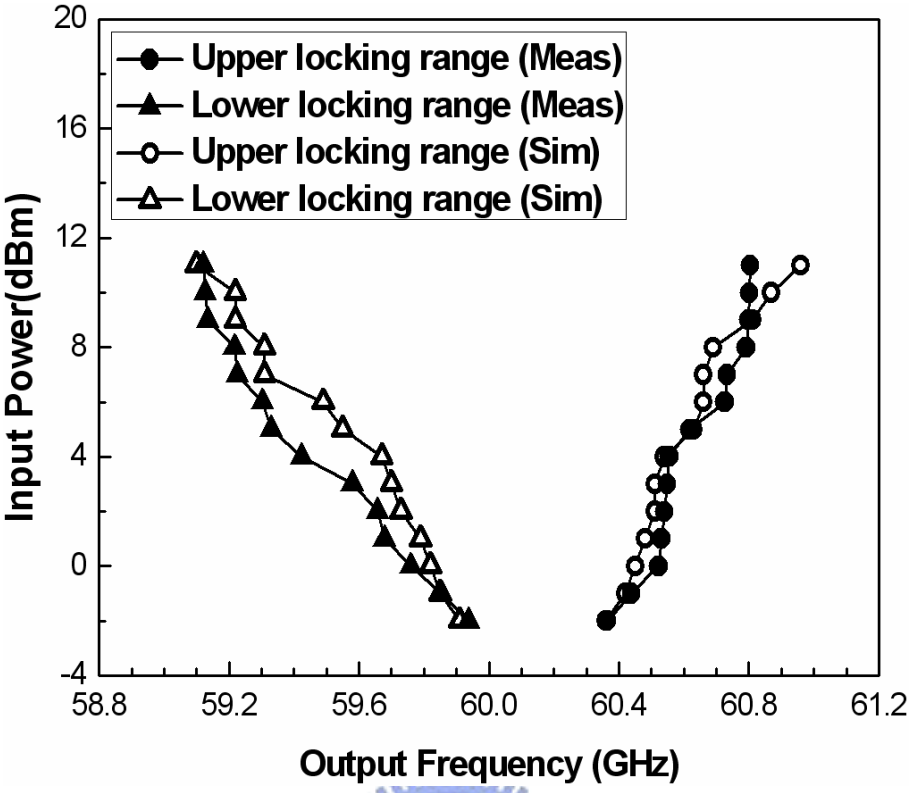


Fig. 2.34 Simulated and measured input power versus output frequency for *V*-band ILFT.

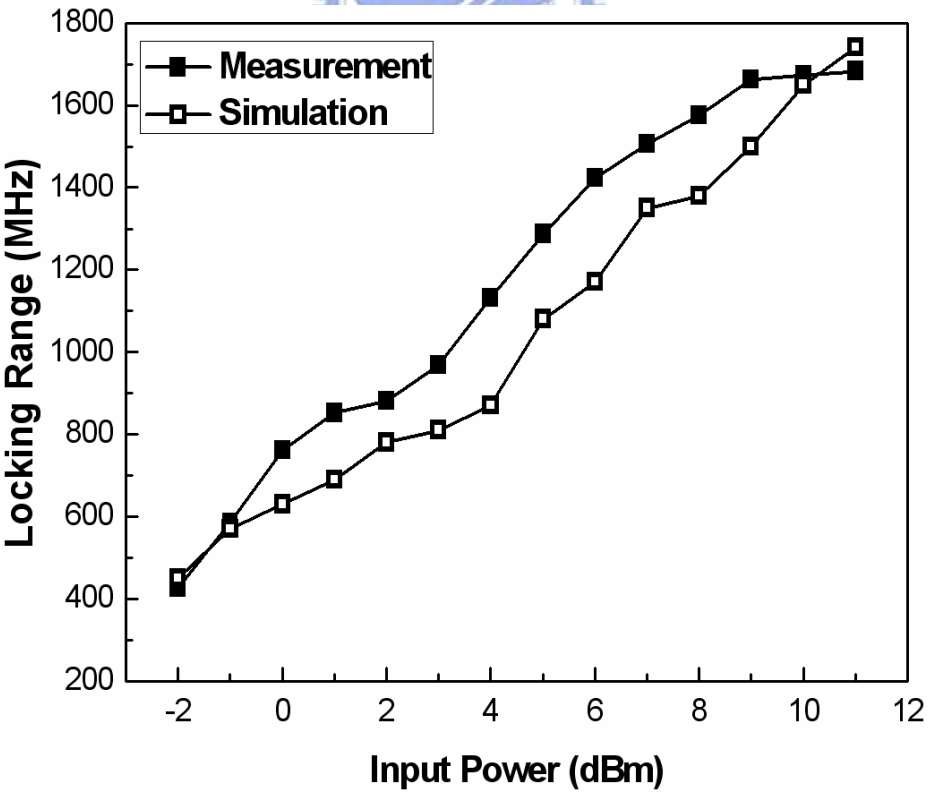


Fig. 2.35 Simulated and measured locking ranges versus input power for *V*-band ILFT.

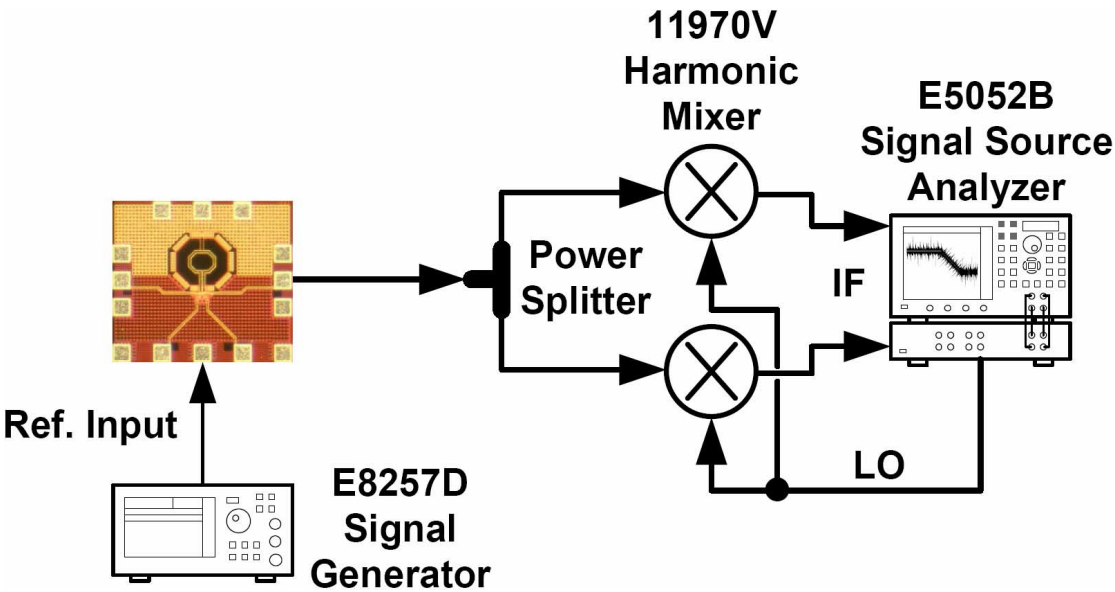


Fig2.36 Measurement setup for output phase noise with external down-conversion mixer.

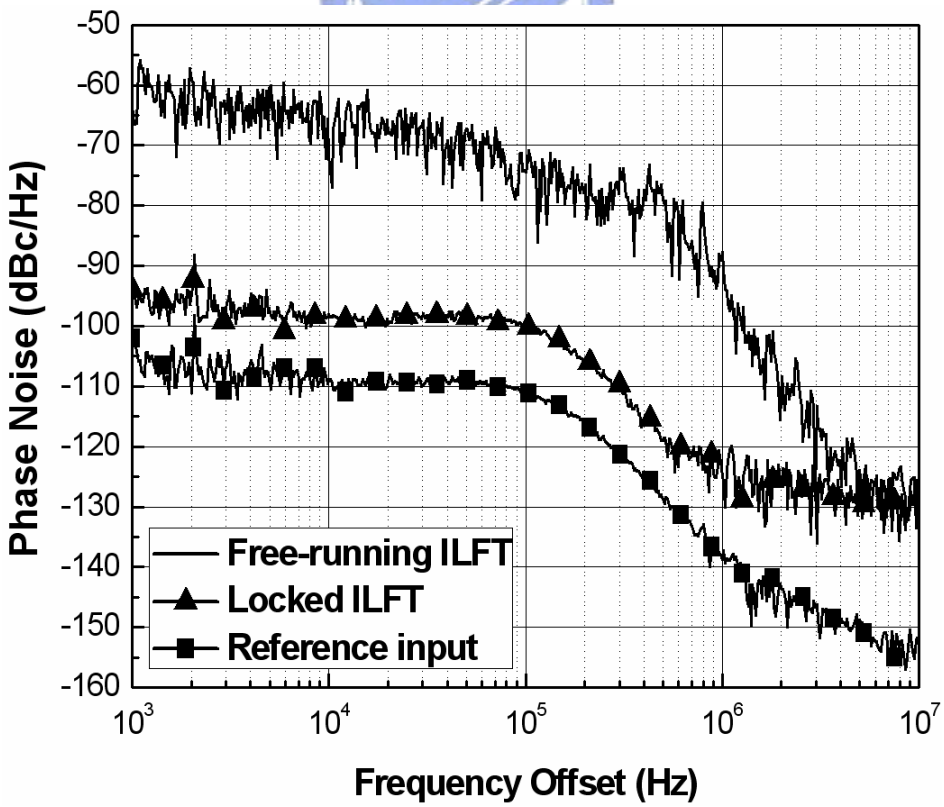


Fig. 2.37 Measured phase noise of reference input, free-running output, and locked output with 6-dBm input power for *V*-band ILFT.

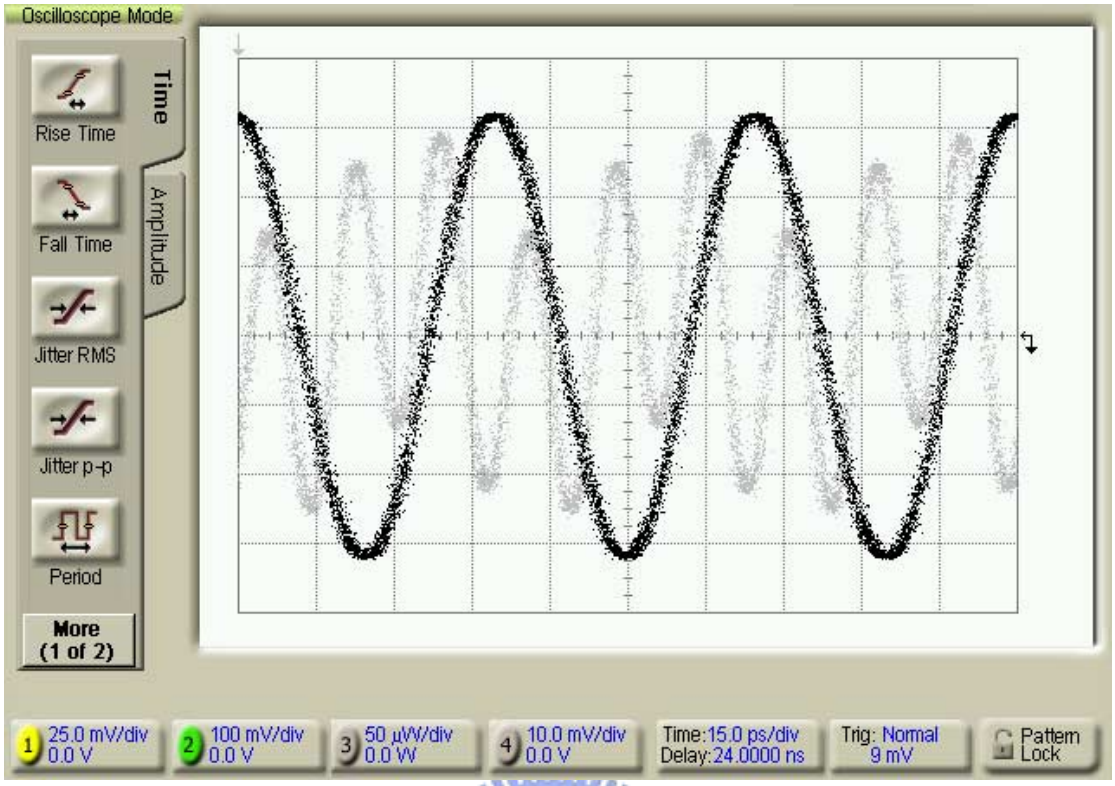


Fig. 2.38 Measured input and output waveforms with cables and probe losses for *V*-band ILFT.

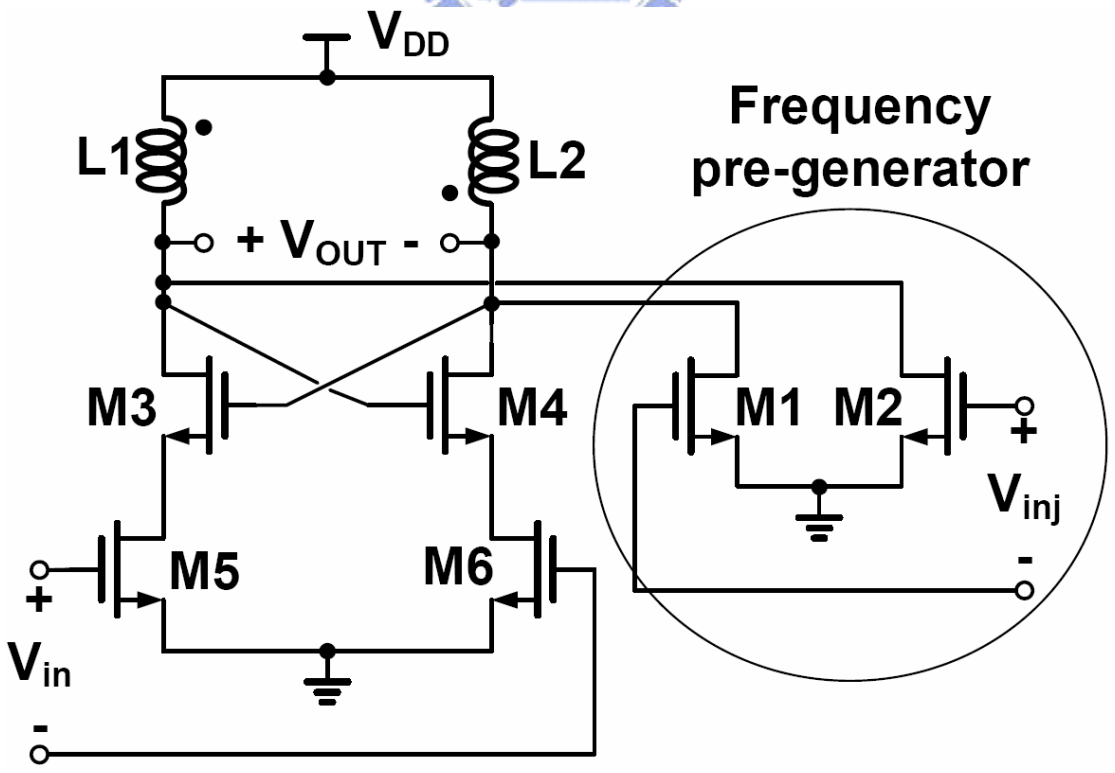


Fig. 2.39 Circuit diagram of the subharmonic ILFT in [23].

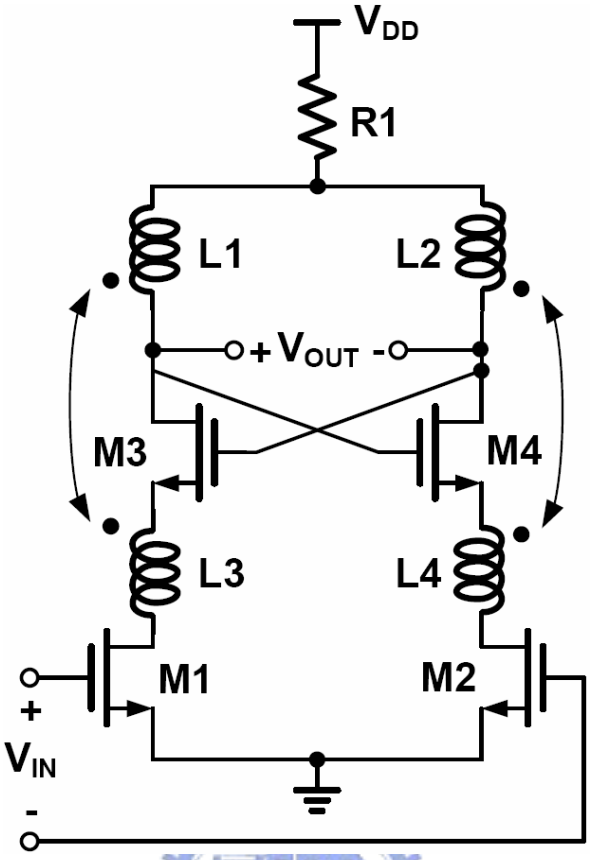


Fig. 2.40 Transformer-based ILFT.

CHAPTER 3

60-GHZ CMOS PHASE-LOCKED LOOP WITH INJECTION-LOCKED FREQUENCY MULTIPLIER

In this chapter, the design of a CMOS phase-locked loop (PLL) cascaded with the injection-locked frequency multiplier (ILFM) for 60-GHz applications is proposed and designed to verify the low-power design concept of millimeter-wave CMOS PLL. The proposed CMOS ILFM is designed to generate the fifth-order harmonic frequency of the voltage-controlled oscillator (VCO) output. The proposed PLL with ILFM is designed and fabricated using 0.18-μm bulk CMOS technology. The measured output frequency range is from 53.04 GHz to 58.0 GHz which is higher than the transition frequency (f_T ~ 55 GHz) of the device, but the highest frequency of the frequency divider in the proposed PLL structure is only 11.6 GHz. As a result, the total power dissipation can be reduced significantly as compared with pervious work [28]–[31].

In Section 3.1, the general theoretical model for odd-order ILFM is presented. The design consideration for third-order PLL is described in Section 3.2. The proposed architecture of the 60-GHz PLL and the building blocks of the proposed PLL including VCO, ILFM, frequency divider, phase-frequency detector (PFD), charge pump (CP), and loop filter are described in Section 3.3. The experimental results are shown in Section 3.4. Finally, the conclusion is given in Section 3.5.

3.1 THEORETICAL MODEL FOR INJECTION-LOCKED FREQUENCY MULTIPLIER

The model for injection-locked frequency tripler (ILFT) developed in Chapter 2 can be extended into higher-order structure for odd-order ILFM analysis. In this Section, the general expression for fifth-order ILFM is described. Based upon the model developed in [25], the extension model for fifth-order ILFM is shown in Fig. 3.1. The frequency pre-generator is modeled as the nonlinear characteristic function $f(v_I)$; the active devices of the injection-locked oscillator (ILO) stage are modeled as the linear constant transconductance stage G_m; $H(j\omega)$ is the transfer function of the band pass LC-tank filter in the output of the ILO stage; $v_I(t)$ is the incident signal with the input frequency ω_I; $v_O(t)$ is the output signal with the frequency $\omega_O = 5\omega_I$; the positive odd integer, $v_{I,ILO}(t)$ is the output signal of the frequency pre-generator; and i_{OUT} is the output current of the transconductance stage G_m.

By extending the nonlinear characteristic function $f(v_I)$ into the fifth-order polynomial,

$$v_{I,ILO}(t) = f(v_I(t)) = \sum_{n=0}^{\infty} a_n (v_I(t))^n$$

$$= a_0 + a_1 v_I(t) + a_2 (v_I(t))^2 + a_3 (v_I(t))^3 + a_4 (v_I(t))^4$$

$$+ a_5 (v_I(t))^5 + O((v_I(t))^6) \tag{3.1}$$

where a_n is the coefficient of polynomial f, and $O((v_I(t))^6)$ is the terms of order higher than five.

The output of the frequency pre-generator $v_{I,ILO}$(t) can be expressed as

$$v_{I,ILO}(t)=\left(a_1V_i+\frac{3a_3V_i^3}{4}+\frac{5a_5V_i^5}{8}\right)\cos(\omega t+\theta)$$

$$+\left(\frac{a_3V_i^3}{4}+\frac{5a_5V_i^5}{16}\right)\cos(3\omega t+3\theta)+\frac{a_5V_i^5}{16}\cos(5\omega t+5\theta). \tag{3.2}$$

where V_i and V_o are the incident and the output amplitude, respectively.

By use of the same process shown in Section 2.1, the normalized locking range of the ILFT can be rewritten as

$$\frac{|\omega-\omega_r|}{\omega_r}\le\frac{1}{2Q}\sqrt{\frac{\left(\frac{a_3V_i^3}{4}+\frac{5a_5V_i^5}{16}\right)^2}{(V_o)^2-\left(\frac{a_3V_i^3}{4}+\frac{5a_5V_i^5}{16}\right)^2}}\approx\frac{1}{2Q}\left|\frac{a_3V_i^3}{4V_o}+\frac{5a_5V_i^5}{16V_o}\right| \tag{3.3}$$

and the normalized locking range of the ILFM with fifth-order harmonic output can be expressed as

$$\frac{|\omega-\omega_r|}{\omega_r}\le\frac{1}{2Q}\sqrt{\frac{\left(a_5V_i^5\right)^2}{(16V_o)^2-\left(a_5V_i^5\right)^2}}\approx\frac{1}{2Q}\left|\frac{a_5V_i^5}{16V_o}\right| \tag{3.4}$$

where ω_r and Q are the resonant frequency and quality factor of the *LC*-tank in the output of the ILFM, respectively. The expression of the output amplitude for ILFT can be rewritten as

$$V_o=\frac{G_mH_0\left(\frac{a_3V_i^3}{4}+\frac{5a_5V_i^5}{16}\right)\cos3\theta}{(1-G_mH_0)} \tag{3.5}$$

and the expression of the output amplitude of ILFM with fifth-order harmonic output can be written as

$$V_o=\frac{a_5G_mH_0V_i^5\cos5\theta}{16(1-G_mH_0)} \tag{3.6}$$

where H_0 is the impedance of the LC-tank at their resonant frequency, and θ is the phase difference between the input signal and the output signal.

To compare with (2.15) and (3.3), the locking range of ILFT is determined by not only the third-order coefficient a_3 but also the fifth-order coefficient a_5. In general, the coefficients a_3 and a_5 are negative and positive, respectively. In other words, the locking range can be maximized by the maximization of coefficients a_3 and the minimization of coefficient a_5 of the frequency pre-generator. The derived output amplitude V_o (3.5) is also degraded by the coefficient a_5. As a result, the choice for the conduction angle θ_{CON} discussed in Section 2.2 should be considered the effect from a_5 for more detail analysis.

The design flow of the ILFM for fifth-order harmonic output can be decided from (3.4) and (3.6). The conversion gain of the frequency pre-generator and the amplitude of the incident signal from VCO are maximized for the maximization of the locking range. To further increase the locking range of ILFM, it can trade off output voltage swing for large locking range via the quality factor degradation of LC-tank.

The simplified noise model of ILFM for fifth-order harmonic output is shown in Fig. 3.2 [25] where the conversion gain of the fifth-order harmonic signal in the frequency pre-generator is simplified to be a constant value A_{FPG} and $v_{I,ILO5\omega}$ is the signal with frequency $5\omega_I$. The noise contribution from the frequency pre-generator and the ILO are modeled as $n_{FPG}(t)$ and $n_{ILO}(t)$, respectively. The linear phase-domain model [69]–[70] is adopted to calculate the output phase noise. By using the same process in Section 2.1, the derived output phase noise can be expressed as

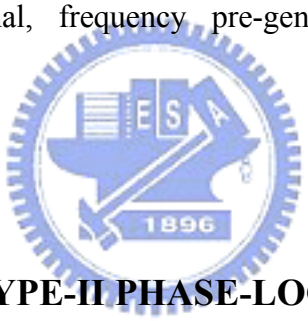
$$S_{OUT}(\omega_m)=\frac{5^2}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{INJ}(\omega_m)+\frac{1}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{FPG}(\omega_m)+\frac{\left(\frac{\omega_m}{\omega_p}\right)^2}{1+\left(\frac{\omega_m}{\omega_p}\right)^2}S_{FreeRun}(\omega_m) \quad (3.7)$$

where the corner frequency of the ILFM noise transfer function ω_p can be written as

$$\omega_p=\frac{\omega_r}{2Q}\frac{\eta}{1+\eta} \quad (3.8)$$

$$\eta=\frac{A_{FPG}V_i}{V_o}. \quad (3.9)$$

In the above equations, ω_m is the offset frequency from output frequency ω_O and $S_{OUT}(\omega_m)$, $S_{INJ}(\omega_m)$, $S_{FPG}(\omega_m)$, and $S_{FreeRun}(\omega_m)$ are the phase noise spectral densities of output, input injection signal, frequency pre-generator, and internal circuits, respectively.



3.2 THIRD ORDER TYPE-II PHASE-LOCKED LOOP DESIGN CONSIDERATION

The block diagram of a typical PLL is shown in Fig. 3.3. It is composed of PFD, low-pass filter (LPF), VCO, and divide-by-M frequency divider. The PFD is a comparator that can detect the phase/frequency difference between two inputs, f_{ref} and f_{div}. The LPF is used to storage the PFD output voltage which controls the VCO output frequency. If the phase/frequency of frequency divider f_{div} is lower than the phase/frequency of the reference frequency f_{ref}, the VCO control voltage is increased by PFD. Thus, the output frequency of VCO increases to catch the reference frequency. After their phases/frequencies are equal, the PFD output is stable. At the moment, a constant phase error between the phase of frequency divider output and the

phase of reference input is existed. If the phase error is not a function of time, it is defined as phase locked. In this PLL configuration, the output frequency of VCO f_{out} is M times the reference frequency f_{ref} under locked condition.

A charge-pump PLL can be modeled as the linear and phase domain system as shown in Fig. 3.4 if the loop bandwidth of the PLL is much less than the reference frequency [75]. In this model, VCO is modeled as an integrator with a gain of K_{VCO} in rad/sec/volt, the phase detector has a gain of $K_{PD} = I_P / 2\pi$ where I_P is the nominal charge-pump current; the transimpedance transfer function of the loop filter is $Z_{LF}(s)$; and the divider ratio of the frequency divider is M. The closed-loop transfer function $H(s) \equiv \theta_{out} / \theta_{ref}$ can be written as

$$H(s) = \frac{\theta_{out}}{\theta_{ref}} = \frac{\frac{I_{CP}}{2\pi} Z_{LF}(s) \frac{K_{VCO}}{s}}{1 + \left(\frac{I_{CP}}{2\pi} Z_{LF}(s) \frac{K_{VCO}}{s} \right) \frac{1}{M}}$$

$$= \frac{\frac{I_{CP}}{2\pi} Z_{LF}(s) K_{VCO}}{s + \left(\frac{I_{CP}}{2\pi} Z_{LF}(s) K_{VCO} \right) \frac{1}{M}}, \qquad (3.10)$$

which a low-pass transfer characteristic of $H(s)$ is shown. In a third-order type-II PLL, the transfer function of passive loop filter as shown in Fig. 3.5 can be expressed as

$$Z_{LF}(s) = \left(\frac{b}{b+1} \right) \frac{\tau s + 1}{sC1 \left(\frac{\tau s}{b+1} + 1 \right)} \qquad (3.11)$$

where

$$\tau = R1 \cdot C1 \qquad (3.12)$$

$$b = C1 / C2 . \qquad (3.13)$$

By substituting (3.11) into (3.10), the closed-loop transfer function is found to be

$$H(s)=\frac{K\left(\frac{b}{b+1}\right)\left(s+\frac{1}{\tau}\right)}{\frac{M\tau}{b+1}s^3+Ms^2+\frac{Kb}{b+1}s+\frac{Kb}{(b+1)\tau}} \tag{3.14}$$

where

$$K=\frac{I_{CP}}{2\pi}K_{VCO}R1. \tag{3.15}$$

The transfer function (3.14) has a denominator of three degree, so the system is a third-order PLL. However, a three poles system introduces a stability problem. The loop filter should be designed carefully to maintain the loop stability.

In the open-loop transfer function, the additional pole is located at $s=-(b+1)/\tau$, which is much larger than other low-frequency poles for large b. If C2 is small for large b, then only high-frequency property is affected by the additional pole. Thus, the low-frequency response is essentially the same as for the second-order loop [75]. In general, the selected value of additional pole is larger than the loop bandwidth for stability consideration. A phase margin is 62° as the additional pole is four times of the loop bandwidth.

There are several noise sources in a PLL. To simplify the noise analysis, three main noise sources in a PLL are considered. They are φ_{ref} from reference signal in rad/Hz$^{1/2}$, φ_{vco} from VCO in rad/Hz$^{1/2}$, and v_{lf} from the loop filter in volt/Hz$^{1/2}$. The linear phase-domain PLL model is shown in Fig. 3.6. The transfer functions from these noise sources to the output can be expressed as

$$\frac{\varphi_{out}(s)}{\varphi_{ref}(s)}=T_{ref}(s)=\frac{A(s)}{1+A(s)\beta} \tag{3.16}$$

$$\frac{\varphi_{out}(s)}{\varphi_{vco}(s)} = T_{vco}(s) = \frac{1}{1+A(s)\beta} \tag{3.17}$$

$$\frac{\varphi_{out}(s)}{\varphi_{lf}(s)} = T_{lf}(s) = \frac{1}{1+A(s)\beta} \cdot \frac{K_{VCO}}{s} \tag{3.18}$$

where

$$A(s) = K_p Z_{LF}(s) \frac{K_{VCO}}{s} \tag{3.19}$$

$$\beta = \frac{1}{M}. \tag{3.20}$$

Assume the cross-correlation functions of these noise sources are zero, the total noise can be calculated with an root-mean-square (RMS) sum,

$$\begin{aligned} \varphi_{out}^2 &= (\varphi_{ref} T_{ref})^2 + (\varphi_{vco} T_{vco})^2 + (\varphi_{lf} T_{lf})^2 \\ &= \left(\frac{A(s)}{1+A(s)\beta}\right)^2 (\varphi_{ref}^2) + \left(\frac{1}{1+A(s)\beta}\right)^2 (\varphi_{vco}^2) + \left(\frac{1}{1+A(s)\beta}\right)^2 (\varphi_{lf}^2)\left(\frac{K_{VCO}}{s}\right). \end{aligned} \tag{3.21}$$

As may be seen from the first term in (3.21), the noise from the reference clock is passed through the low-pass filter so that the PLL output phase noise is dominated by the noise from the reference clock at small offset frequency. In addition, the noise contribution from reference clock is increased by the feedback divider ratio *M* in side the loop bandwidth.

The noise from VCO as given in the second term of (3.21) is of high-pass transfer characteristic. Therefore, the noise from VCO is suppressed inside the loop bandwidth and dominates the PLL phase noise beyond the loop bandwidth.

The third term of (3.21) is the noise contribution from the loop filter. It can be seen that if K_{VCO} is large, the noise contribution from loop filter become serious. The only noise source in a loop filter is the thermal noise from the resistor R1 as shown in

Fig. 3.5. The noise from loop filter and the controlled node is passed through the band-pass transfer function. Thus, it is important to maintain low noise contribution from loop filter to the PLL output both at small offset frequency and at large offset frequency.

3.3 CIRCUIT REALIZATION

The proposed 60-GHz third-order type-II CMOS PLL that is composed of VCO, ILFM, 1/32 frequency divider, PFD, CP, and loop filter is shown in Fig. 3.7. The reference signal with the input power of 0 dBm and the frequency f_{ref} from 331.5 MHz to 362.5 MHz is fed from the external signal generator. The output frequency ($5f_{out}$) with the frequency range from 53.04 GHz to 58.0 GHz, which is five times the VCO output frequency (f_{out}), is generated by the ILFM.

3.3.1 VCO and Injection-locked Frequency Multiplier

The circuit diagram of both VCO and ILFM is shown in Fig. 3.8 where the dimensions of the devices are listed in Table 3.1. The VCO is made of a cross-coupled pair M_{VCO1}/M_{VCO2} to generate negative resistance for the compensation of the loss from *LC*-tank. An on-chip spiral inductor L_{VCO1} with symmetric structure and accumulation mode MOS varactors C_{VCO1}/C_{VCO2} are used in the VCO design. C_{VCO1}/C_{VCO2} has the higher quality factor compared with pn-junction varactors. The poly-resistor R_{VCO1} is designed for a proper bias condition of the cross-coupled pair. The utilization of resistor instead of PMOS current source is attributed to its free-of-flicker-noise property [76]. Hence, the output phase noise of VCO can be improved.

The schematic of the proposed ILFM can be divided into two stages [25]. The first stage is the frequency pre-generator stage and the second stage is the injection-locked oscillator (ILO) stage. The input signal from VCO is injected into the frequency pre-generator stage. The function of the frequency pre-generator stage that generates the fifth-order harmonic of the input injection signal is implemented by M_{ILFM1}/M_{ILFM2}. The conversion gain of the frequency pre-generator can be maximized by selection of an appropriate gate bias value of M_{ILFM1}/M_{ILFM2} V_{BIAS}. In addition, the locking range of the ILFM can be increased by an increase of the conversion gain of the frequency pre-generator [25].

The signal generated by the frequency pre-generator is directly transmitted into the ILO stage formed by M_{ILFM3}/M_{ILFM4} and a symmetric spiral inductor L_{ILFM1}. The value of the inductor L_{ILFM1} is chosen so that it can resonate with the total capacitances at the drain of M_{ILFM3}/M_{ILFM4} at the fifth-order harmonic frequency of the input frequency. M_{ILFM3}/M_{ILFM4} is used to generate negative conductance to cancel the loss of the *LC*-tank for free-running oscillation of the ILO stage and to make the output signal differential. The resistor R_{ILFM1} is designed for the improvement of the harmonic rejection ratio (HRR) at every undesired even-order harmonic [25].

Because the output frequency is higher than the transition frequency f_T of the device, the open-drain output buffer is not suitable in this design owing to the poor property of the device. A source follower is chosen as the output buffer for testing purpose. The simulated voltage loss of output buffer from 50 to 66 GHz is shown in Fig. 3.9. The loss form output buffer is higher than 16 dB within the desired frequency range. The length of the interconnection metal line from the ILFM output to the testing pad is around 70 μm. To avoid the frequency shift, the characteristic of this metal line is simulated by the 3D EM CAD tool High-Frequency Simulation

Software (HFSS). Finally, M_{DUMMY} is designed to provide a balanced-load for ILFM outputs.

Fig. 3.10 shows the HSPICE simulated normalized fifth-order harmonic currents I_{d5}/I_{dmax} of the frequency pre-generator where I_{d5} is the magnitude of the output drain current at the fifth-order harmonic frequency, I_{dmax} is the magnitude of the output total drain current, and conduction angle θ_{CON} is the device turn-on angle within one period of the input signal. The simulation condition involves a 12-GHz input signal with 4-dBm input power and a NMOS with dimensions of W/L = 18 um/0.18 um. Because of the parasitic capacitances of the NMOS from gate-drain and drain-source, those undesired ac currents through gate-drain and drain-source are included in the output drain current I_{dmax} and I_{d5}. It can be seen from Fig. 3.10 that the normalized harmonic current curve is not the same as the ideal switch condition in [71]. In the proposed ILFM, the devices M3/M4 performed as the frequency pre-generator function are biased at a conduction angle θ_{CON} of 230˚ for higher frequency conversion efficiency while maintaining the oscillation of the ILO. Finally, the value of V_{BIAS} can be calculated by a given input power, the device threshold voltage, and a suitable conduction angle [71].

3.3.2 Frequency Dividers

The 1/32 frequency divider is composed of the four-stage CML divide-by-two dividers and one-stage digital static-flip-flop-based divide-by-two divider. The CML divider [77] is made of a master-slave D-type flip-flop (DFF) with the output terminal (Q) connected to the input terminal (D) in inverted polarities. The CMOS CML divider has been demonstrated to have high-speed operation with low power dissipation because the full swing for internal operation is not required [77]. The schematic diagram of master and slave latch is shown in Fig. 3.11(a) where the

dimensions of the devices are listed in Table 3.2. In the latch circuit, the sense stage consists of transistors M_{CML1}, M_{CML3}, and M_{CML4} whereas the latch stage comprises the transistors M_{CML2}, M_{CML5}, and M_{CML6}. In order to increase the operational frequency, the output load is chosen as the poly-resistors R_{CML1}/R_{CML2} for smaller parasitic capacitance instead of PMOS load [45]. Each CML divider stage is optimized at its operational frequency by changing the device ratios of sense stage and latch stage.

Because a full swing input for PFD is required, the last stage of the 1/32 frequency divider is designed as the digital-type frequency divider. The divide-by-two divider comprises two ring-connected D-latches. The circuit diagram of the digital static divider is shown in Fig. 3.11(b).

3.3.3 Phase Frequency Detector, Charge Pump, and Loop Filter

PFD is designed to detect both phase and frequency difference between the reference signal and the output signal of the frequency divider. The PFD state diagram is shown in Fig. 3.12(a). The operation principle of PFD is to detect the rising edge of signal A and B. If the rising edge of A is arrived before the rising edge of B, output Q_A is set to charge the VCO control voltage. In the difference scenario, if the rising edge of B is arrived before the rising edge of A, output Q_B is set to discharge the VCO control voltage. The timing diagram of PFD is shown in Fig. 3.12(b). The circuit diagram of PFD [78] is shown in Fig. 3.13. The true-single-phase-clock (TSPC) dynamic DFF is used for hundred-MHz frequency operation in the PFD circuit implementation. A slow NOR gate is used to generate the reset signal (V_{RESET}) for reducing the dead zone problem. Additionally, in order to reduce the skew between the complementary output signals, (UP/UPB) and (DN/DNB), complementary pass-transistor gates are used to match the delay of an inverter in the output of PFD.

The circuit diagram of charge pump [79] and loop filter is shown in Fig. 3.14. A simple current-switched charge pump is used. Switches M_{CP3} and M_{CP4} are turned on at every phase comparison and may create the ripple on the control voltage (V_C). M_{CP1} and M_{CP2} are used to decrease the charge injection and clock feedthrough from M_{CP3} and M_{CP4} to the output node (V_C) [80]. The small bandwidth of loop filter is designed to reduce the effect of non-ideal property of switches. Because there is no current-matched technique in the CP design, the reference spur is stronger than that with current-matched technique.

In the loop filter design, all the passive components are implemented by the on-chip elements. The vertical metal-insulator-metal capacitors (MIMCaps) are used to realize the capacitors C1 = 19.98 pF and C2 = 2.67 pF with reasonable chip area. The resistor R1 = 11.4 kΩ is made of poly-resistor.

3.3.4 Simulation Results of Phase-locked Loop

The simulated locked ILFM output waveform after output buffer is shown in Fig. 3.15(a). The simulated output power at the fifth-order harmonic is -12 dBm with frequency of 59.5 GHz as can be seen from Fig. 3.15 (b). The simulated phase noises of VCO output and ILFM output with the frequency offset from 10 kHz to 100 MHz are shown in Fig. 3.16. The phase noise differences between VCO output and ILFM output at 10 kHz, 1 MHz, and 100 MHz offset are 14.01 dB, 14.03 dB, and 16.5 dB, respectively. If the noise contribution from the frequency pre-generator is negligible, the output phase noise is 13.98 dB [=10log (5^2)] higher than that from the input signal with a small frequency offset (3.7). Therefore, the noise contributions from the frequency pre-generator to the output phase noise at 10 kHz and 1 MHz are 0.03 dB and 0.05 dB, respectively.

The tuning range of VCO is from 10.79 to 12.17 GHz with the control voltage V_C form 0 to 1.5 volt as shown Fig. 3.17. The simulated VCO output waveform and output power spectrum with control voltage of 1.3 V are shown in Figs. 3.18(a) and 3.18(b) respectively. The output amplitude of VCO is around 573 mV.

The simulated waveforms of charge pump in charging mode in shown in Fig. 3.19. It can be seen from Figs. 3.19(a) and (b) that the rising edge of the reference clock is before that of the divider output. Therefore, charge pump charges the control voltage V_C as shown in Fig. 3.19(c) for increasing the frequency of divider output until the rising edge of the divider output is the same as that of reference clock. On the other hand, the simulated waveforms of charge pump in discharging mode in shown in Fig. 3.20. Because the rising edge of the divider output is before that of the reference clock, charge pump discharges the control voltage V_C to decrease the frequency of the divider output.

The simulated timing diagrams of the VCO and four stage CML divide-by-two frequency dividers are shown in Fig. 3.21. The amplitude of each divide-by-two frequency divider is increased with the decrease of the operational frequency. The timing diagram of the digital divide-by-two frequency divider is shown in Fig. 3.22. The output amplitude is reached to full-swing for PFD operation.

Finally, the simulated settling time of the close-loop PLL with reference frequency f_{ref} of 360 MHz is shown in Fig. 3.23. The settling time is around 1.2 us for stable output control voltage V_C. The overall circuit of the proposed PLL is shown in Fig. 3.24 where the dummy MOS in CML frequency divider block is designed for balance output waveform. In Table 3.3, the summary the post-simulation of the PLL is listed.

3.4 EXPERIMENTAL RESULTS

The proposed 60-GHz PLL is designed and fabricated by using 0.18-μm Al 1P6M standard CMOS technology with ultra-thick metal of 2 μm. The chip microphotograph of the proposed PLL is shown in Fig. 3.25 where the chip area including all the test pads and dummy metal is 0.96 mm × 0.84 mm. An on-wafer measurement system incorporating a probe station, GSG coplanar probes, and high-speed cables is used to measure chip performance. Because the VCO output load including the ILFM and the frequency divider is large, the output signal from VCO is not directly connected to the testing pad. In order to check the function of the low-frequency PLL, the output signal from the first divide-by-two divider is connected to the testing pad. The measurement setup for 60-GHz PLL testing is shown in Fig. 3.26.

Due to the inaccuracy extraction of parasitic resistance and long cable line from power supply to test chip, the fabricated 60-GHz PLL can not worked under the supply voltage of 1.5 V. As the supply voltage is increased to 1.6 V, the function of the PLL is worked. Thus, the supply voltage is shift to nominal voltage 1.8 V of the 0.18-μm CMOS technology.

The total power dissipation of the fabricated 60-GHz PLL is 35.7 mW at a power supply of 1.8 V. The measured output spectrum of the locked ILFM is shown in Fig. 3.27 where all the losses from probe, cable, adaptors, and external harmonic mixer have been de-embedded. It can be seen from Fig. 3.27 that the proposed PLL structure provides the output power of –37.85 dBm with the output frequency of 58.0 GHz and 362.5-MHz reference frequency f_{ref} which is higher than the transition frequency f_T. The output phase noises marked at 1 MHz and 10 MHz are measured as shown in Fig.

3.28. The measured output phase noises at 1 MHz and 10 MHz offset from the carrier are –85.2 and –90.9 dBc/Hz, respectively.

Because of the large conversion loss from the external harmonic mixer and the small output power from the fabricated chip, the high-resolution setup for the spectrum analyzer is required in the reference spur measurement [22]. To reduce the time-cost of the high-resolution setup, a *V*-band (low-noise amplifier) LNA is added before the external harmonic mixer. The output power to the spectrum analyzer is therefore large enough to reduce the resolution requirement. The measurement setup for output reference spur testing is shown in Fig. 3.29. As can be seen from the measurement results in Fig. 3.30, the measured reference spur level is –40.16 dBc. Because of the cross-product between output frequency and reference spurs in the frequency pre-generator stage, the frequency offset between the carrier and the spur tone is therefore the same as the reference frequency.

The performance of the first divide-by-two frequency divider is also measured. The measured output power of –16.55 dBm at 5.8 GHz output frequency is shown in Fig. 3.31. The measured phase noise of the first divide-by-two frequency divider output from 100 Hz to 100 MHz is shown in Fig. 3.32. The measured output phase noises at 100 kHz, 1 MHz, and 10 MHz offset from the carrier are –102, –108, and –121 dBc/Hz, respectively. The phase noise difference between the ILFM output and the first divide-by-two frequency divider output at 1 MHz offset is 22.8 dB which is 2.8 dB higher than the theoretical limit 20 dB [=10log(10^2)] as can be seen from Fig. 3.28 and Fig. 3.32. The output waveform of the divider is tested by the high-speed oscillator. It can be seen from Fig. 3.33 that the output amplitude is around 50 mV with cable and adaptor losses.

Because the measured output power is much lower than that in the simulation

result and the output frequency range is larger then that in the simulation result, the measurement for only ILFM is executed. To further discuss the performance of the ILFM, a laser cut is executed to turn off VCO shown in Fig. 3.34. Without the input signal from VCO, the performance of the free-running ILFM can be measured. It can be seen from Fig. 3.35 that there is no free-running output signal of ILFM. Therefore, the performance of ILFM is like the conventional frequency multiplier with high quality factor *LC*-tank as a load. Because the operational frequency of ILFM is higher than device transition frequency and the valid frequency of device model is not covered the entire frequency of interest, the models for active devices are not accurate.

In Table 3.4, the recently-published CMOS FS's and PLLs worked at the *V*-band are compared with the proposed PLL. It can also be seen that the proposed PLL can operate with lower dc power consumption and better phase noise. Because the CP is not current-match structure and larger VCO gain in this work, the reference spur is not as good as in the pervious work. In addition, due to the operational frequency is higher than the device transition frequency of 180-nm device in the output buffer, the output power level is only –37.85 dBm. Finally, this design is the first CMOS PLL integrated with the ILFM in the millimeter-wave band.

3.5 SUMMARY

The proposed PLL integrated with the novel CMOS ILFM for 60-GHz applications is designed and fabricated using 180-nm standard CMOS technology. The proposed ILFM circuit is introduced to multiply the frequency by five times and successfully co-designed with a low-frequency PLL. As can be seen from the

measurement results, the ILFM has a great potential in the applications of LO signal generators for high-frequency PLL design. In addition, the maximum operational frequency of the frequency divider in a PLL can be reduced to only one-fifth by use of the proposed ILFM.

The recently published CMOS FS's and PLLs [81]–[91] are shown in Fig. 3.36. The total power consumption is increased as the operational frequency is increased. The proposed PLL can be operated with lower power consumption and higher operational frequency. The output powers for recently published CMOS FS's and PLLs are shown in Fig. 3.37. Due to the poor device performance and without free-running output, the proposed PLL provides smaller output power as compared to the expected output power. Finally, since it is feasible to design a high-performance VCO at low frequency and to save the large power consumption from full-speed frequency dividers, the proposed PLL structure provides a solution to the low-power and high-performance PLL for 60-GHz applications.

Table 3.1
Dimensions of devices in VCO and ILFM.

Device	Dimension
M_{VCO1} / M_{VCO2}	(1.5 μm / 0.18 μm)× 8
M_{ILFM1} / M_{ILFM2}	(1.5 μm / 0.18 μm)× 20
M_{ILFM3} / M_{ILFM4}	(1.5 μm / 0.18 μm)× 10
M_{BUF}	(1.5 μm / 0.18 μm)× 4
C_{VCO1} / C_{VCO2}	(2.5 μm / 0.5 μm)× 10
L_{VCO1}	Metal width = 9 μm Radius = 36 μm Turn = 3
L_{ILFM1}	Metal width = 9 μm Radius = 30 μm Turn = 1
R_{VCO1}	259.3 Ω
R_{ILFM1}	68.8 Ω

Table 3.2

Dimensions of devices in four stage CML divide-by-two frequency dividers.

1st stage divide-by-two divider		2nd stage divide-by-two divider	
Device	Dimension	Device	Dimension
M_{CML1}	(1.5 μm / 0.18 μm)× 12	M_{CML1}	(1.5 μm / 0.18 μm)× 10
M_{CML2}	(1.5 μm / 0.18 μm)× 4	M_{CML2}	(1.5 μm / 0.18 μm)× 5
M_{CML3} / M_{CML4}	(1.5 μm / 0.18 μm)× 12	M_{CML3} / M_{CML4}	(1.5 μm / 0.18 μm)× 10
M_{CML5} / M_{CML6}	(1.5 μm / 0.18 μm)× 4	M_{CML5} / M_{CML6}	(1.5 μm / 0.18 μm)× 5
R_{CML1} / R_{CML2}	716 Ω	R_{CML1} / R_{CML2}	876.6 Ω
3rd stage divide-by-two divider		4th stage divide-by-two divider	
Device	Dimension	Device	Dimension
M_{CML1}	(1.5 μm / 0.18 μm)× 3	M_{CML1}	(1.5 μm / 0.18 μm)× 2
M_{CML2}	(1.5 μm / 0.18 μm)× 5	M_{CML2}	(1.5 μm / 0.18 μm)× 5
M_{CML3} / M_{CML4}	(1.5 μm / 0.18 μm)× 3	M_{CML3} / M_{CML4}	(1.5 μm / 0.18 μm)× 2
M_{CML5} / M_{CML6}	(1.5 μm / 0.18 μm)× 5	M_{CML5} / M_{CML6}	(1.5 μm / 0.18 μm)× 5
R_{CML1} / R_{CML2}	1385 Ω	R_{CML1} / R_{CML2}	1385 Ω

Table 3.3

Summary of the post-simulation results.

	Post-Simulation	
Frequency Range (GHz)	59.0 – 60.5	
Reference Frequency (MHz)	369 – 378	
VCO Gain (MHz/Volt)	~ 1000	
Phase Noise @ 1 MHz (dBc/Hz)	ILFM : –94.77 VCO : –108.08	
Loop Bandwidth (MHz)	~ 5	
Settling Time (nsec)	< 1500	
Power Consumption (mW)	ILFM	5.2
	VCO	3.8
	Dividers	9.2
	PFD & CP	0.9
	Total	19.1

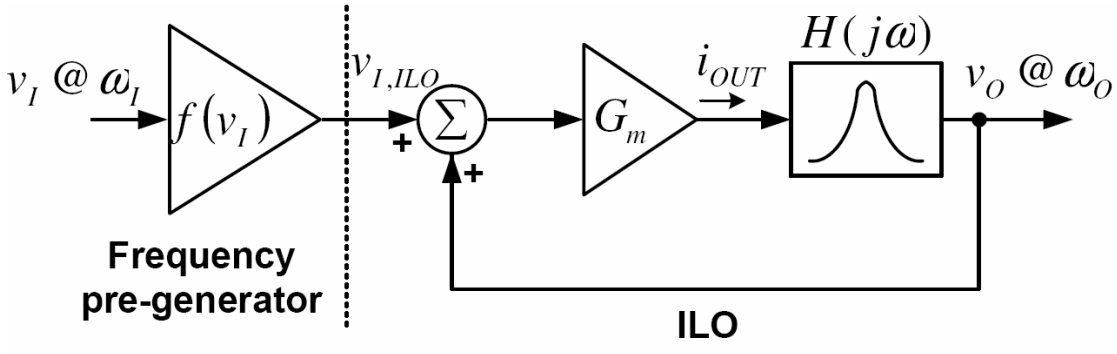
Table 3.4

Comparison with recently published *V*-band CMOS FS's and PLLs.

Ref.	This Work	[28]	[29][a]	[30]	[31]
Technology	180-nm CMOS	130-nm CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS
Frequency (GHz)	53.0 ~ 58.0	49.5 ~ 50.5	58.0 ~ 60.4	61.1 ~ 63.1	73.5 ± 0.32
Reference Freq. (MHz)	350	50	234	60	2340
Phase Noise (dBc/Hz)	− 85.2 @ 1 MHz	− 72.0 @ 1 MHz	− 85.1 @ 1 MHz	− 80.1 @ 1 MHz	− 88.0[b] @ 100 kHz
Reference Spur (dBc)	− 40.2	− 27 ~ − 40	− 50.5	− 49.0	− 72.0
Output Power (dBm)	− 37.85	− 13.86	− 22.0	− 7.0	− 27.06
Supply Voltage (Volt)	1.8	1.5	1.2	1.2	1.45
Power (mW)	35.7	57	80	78	88
Chip Area (mm × mm)	0.96 × 0.84	1.16 × 0.75	1.00 × 0.95	1.20 × 0.70	1.00 × 0.80

a This work is a frequency synthesizer for a fair comparison.

b This value is estimated from divider output.



$$\begin{cases} f(v_I) = a_0 + a_1 v_I + a_2 v_I^2 + a_3 v_I^3 + a_4 v_I^4 + a_5 v_I^5 + O((v_I)^6) \\ \omega_O = 5\omega_I \end{cases}$$

Fig. 3.1 The general model of ILFM.

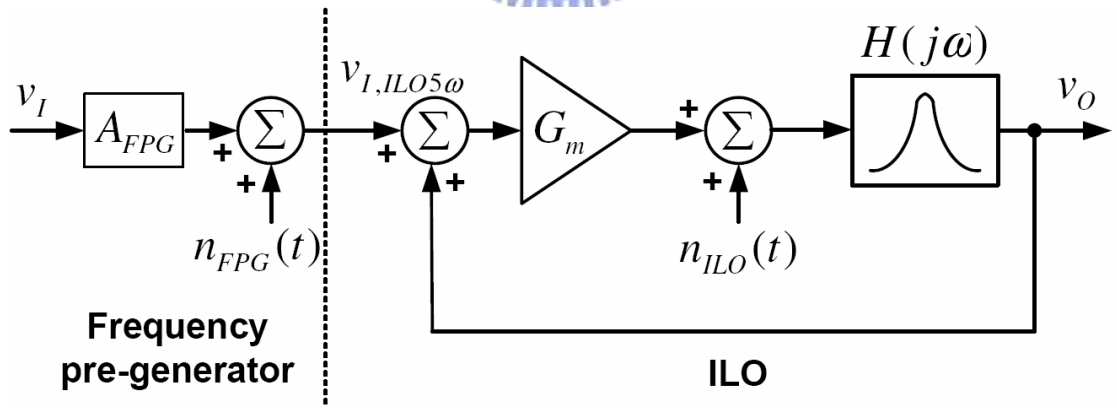


Fig. 3.2 Simplified noise source model for ILFM.

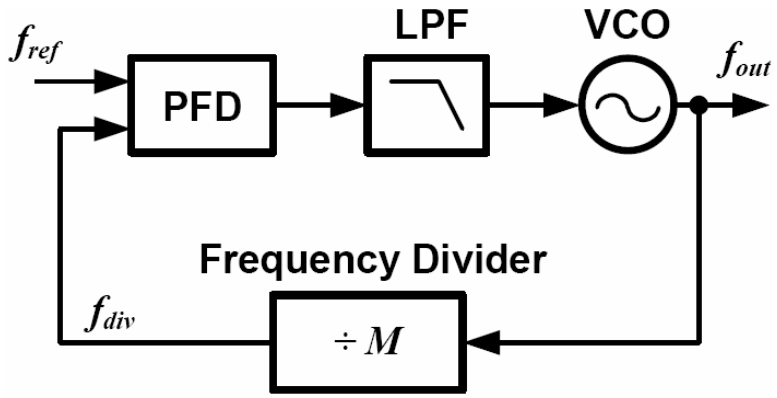


Fig. 3.3 Block diagram of a typical PLL.

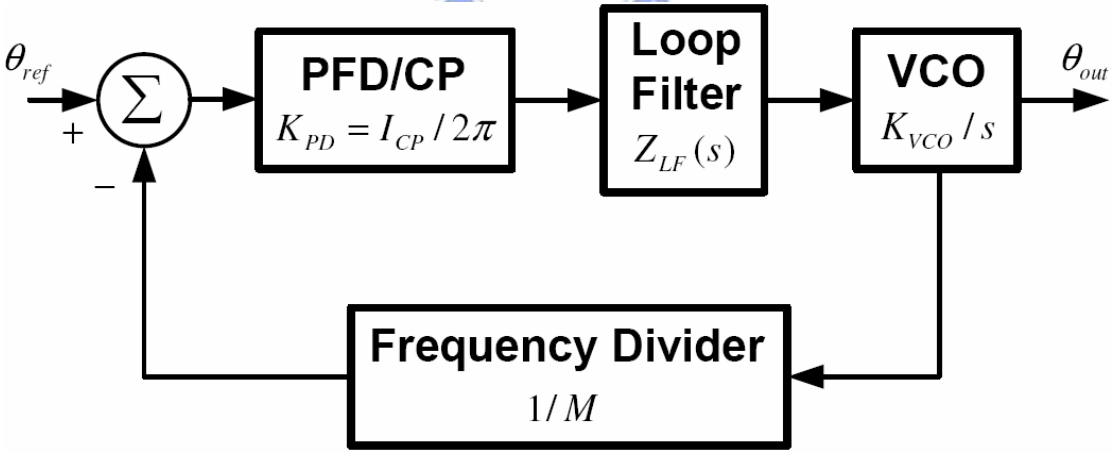


Fig. 3.4 The linear phase-domain PLL model.

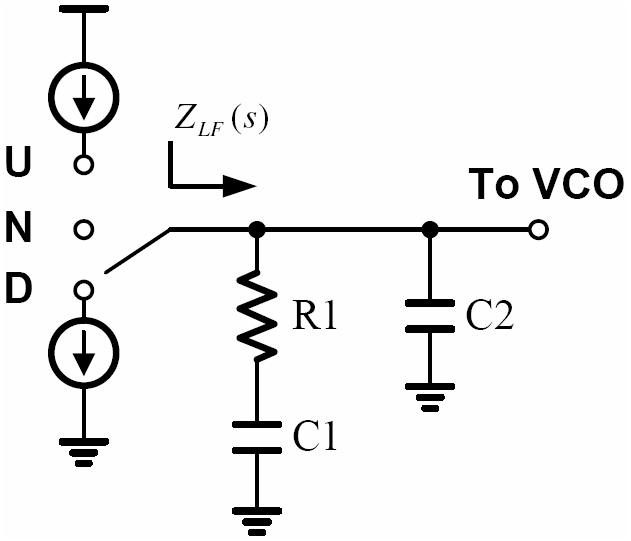


Fig. 3.5 Loop filter in a third-order PLL.

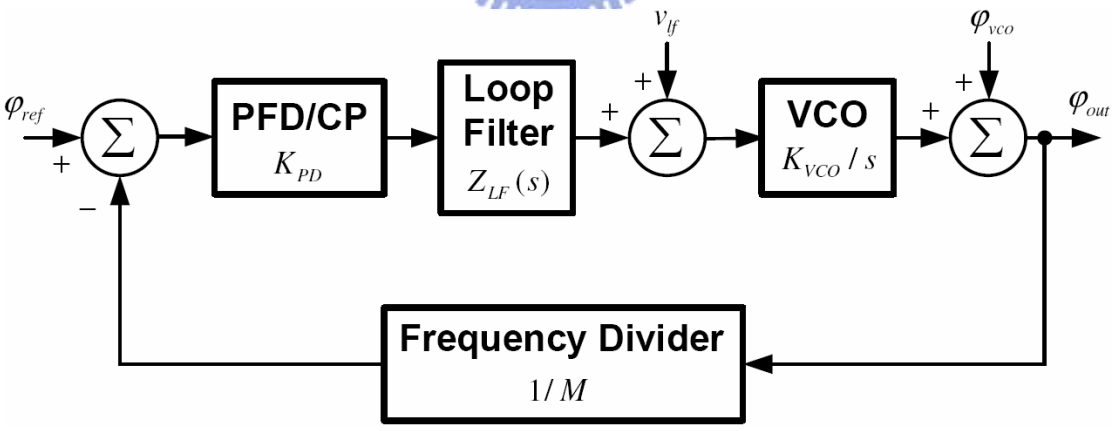


Fig. 3.6 PLL noise model.

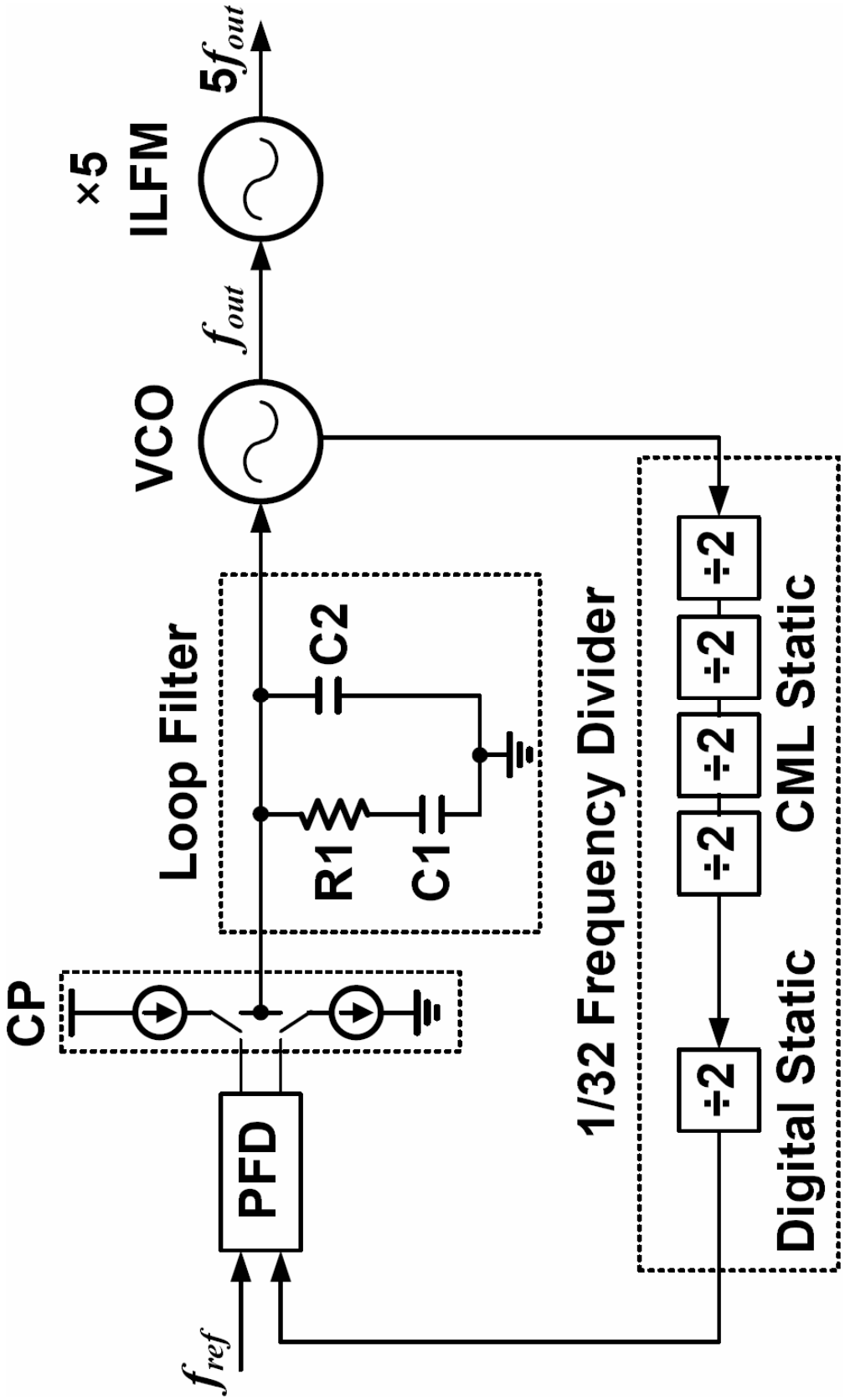


Fig. 3.7 Block diagram of the proposed 60-GHz PLL.

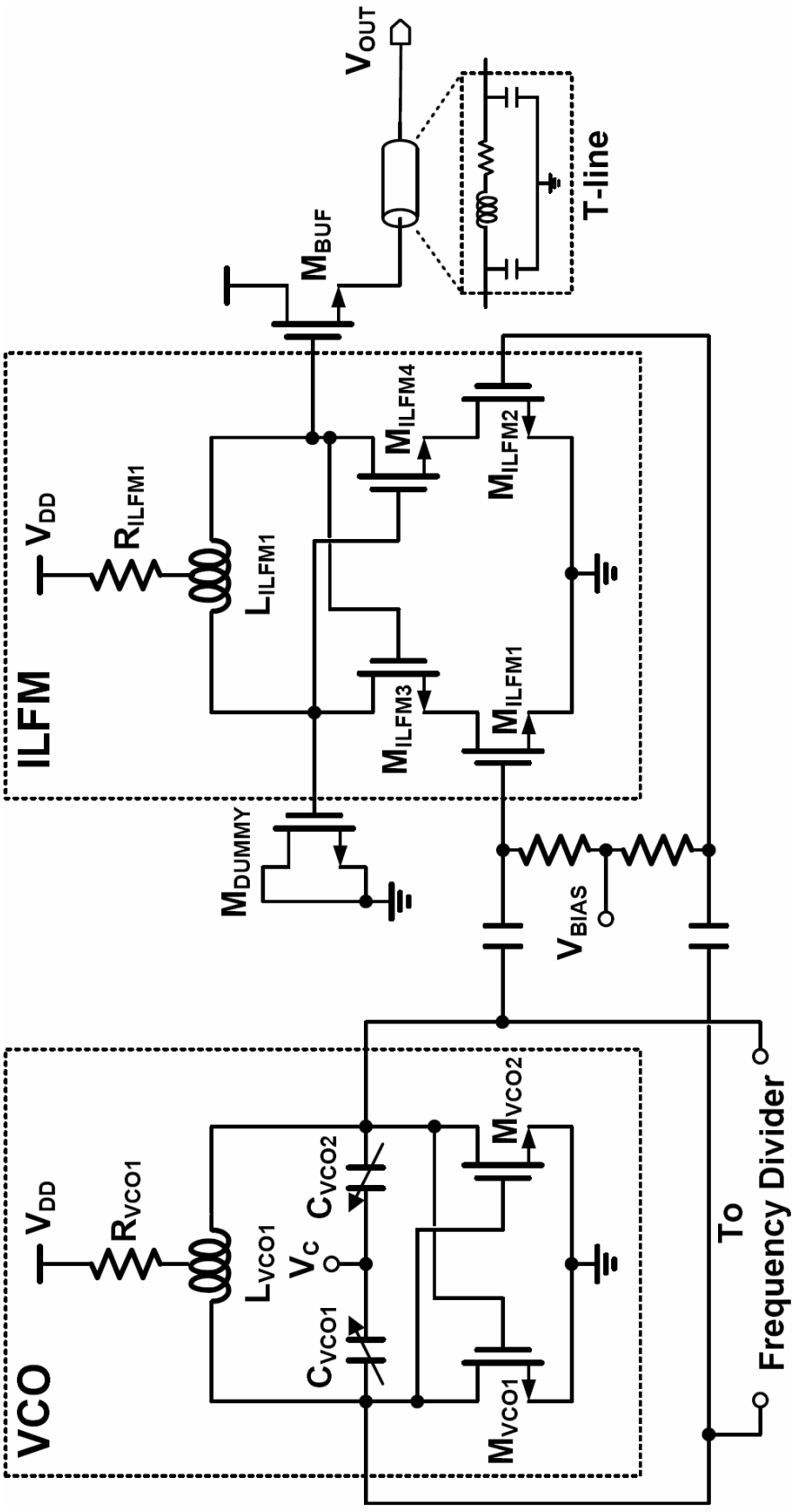


Fig. 3.8 Circuit diagram of both VCO and ILFM.

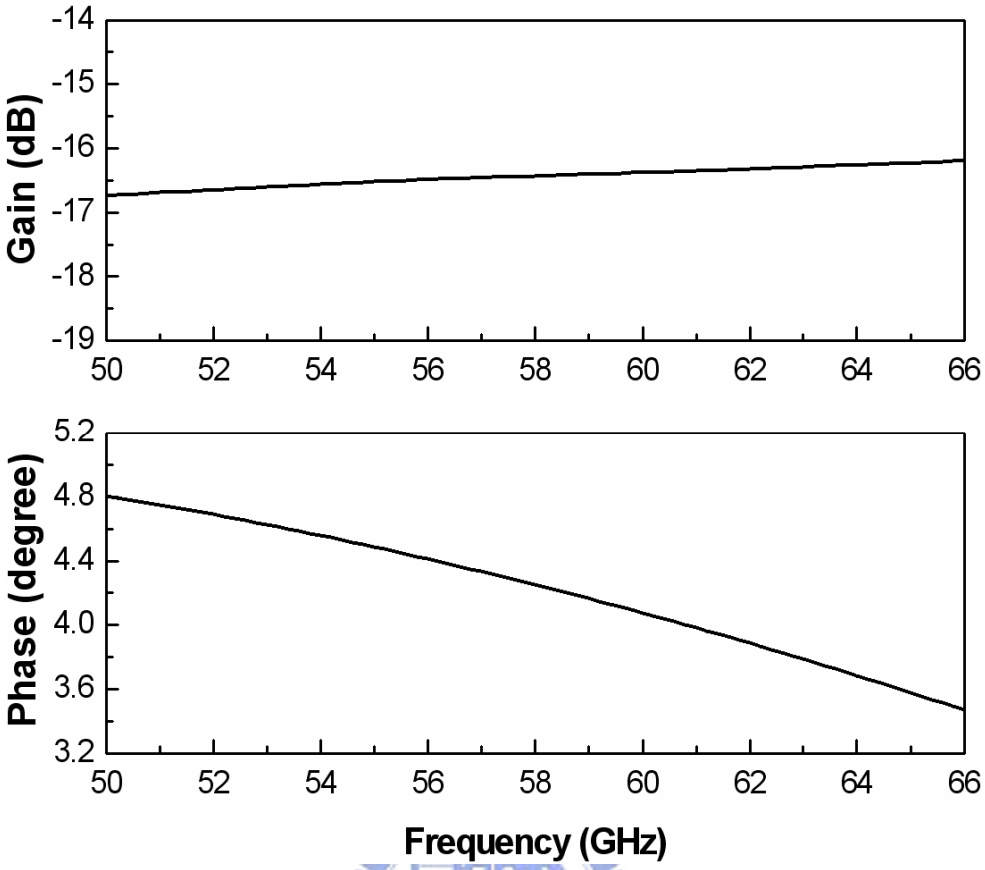


Fig. 3.9 Simulated output buffer loss.

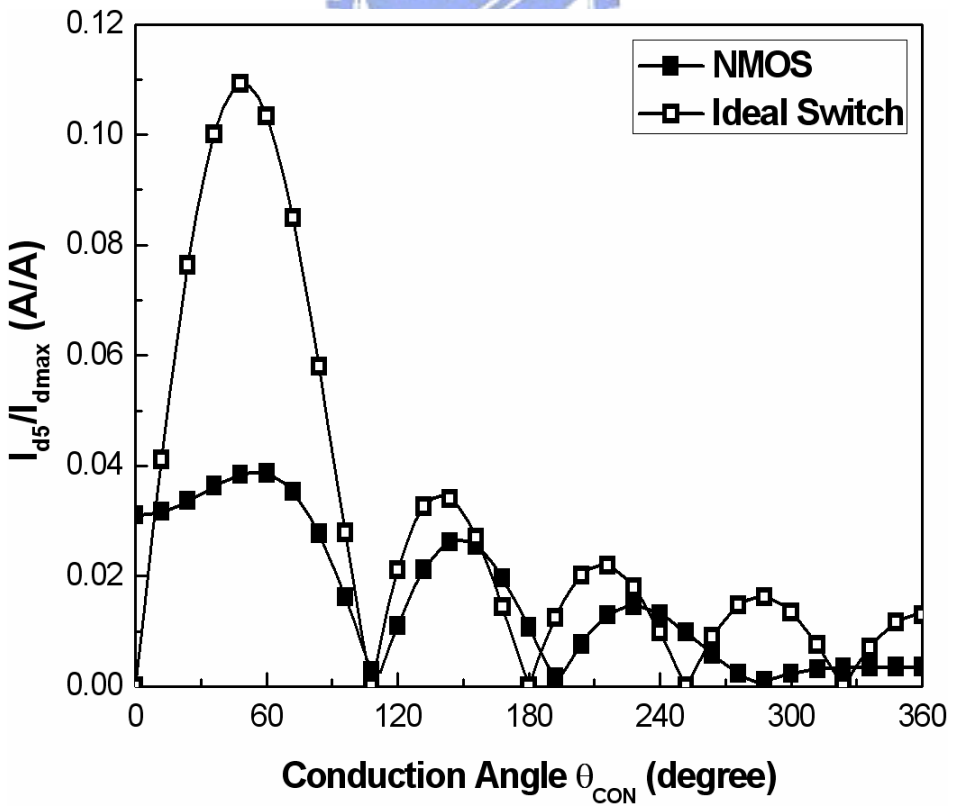
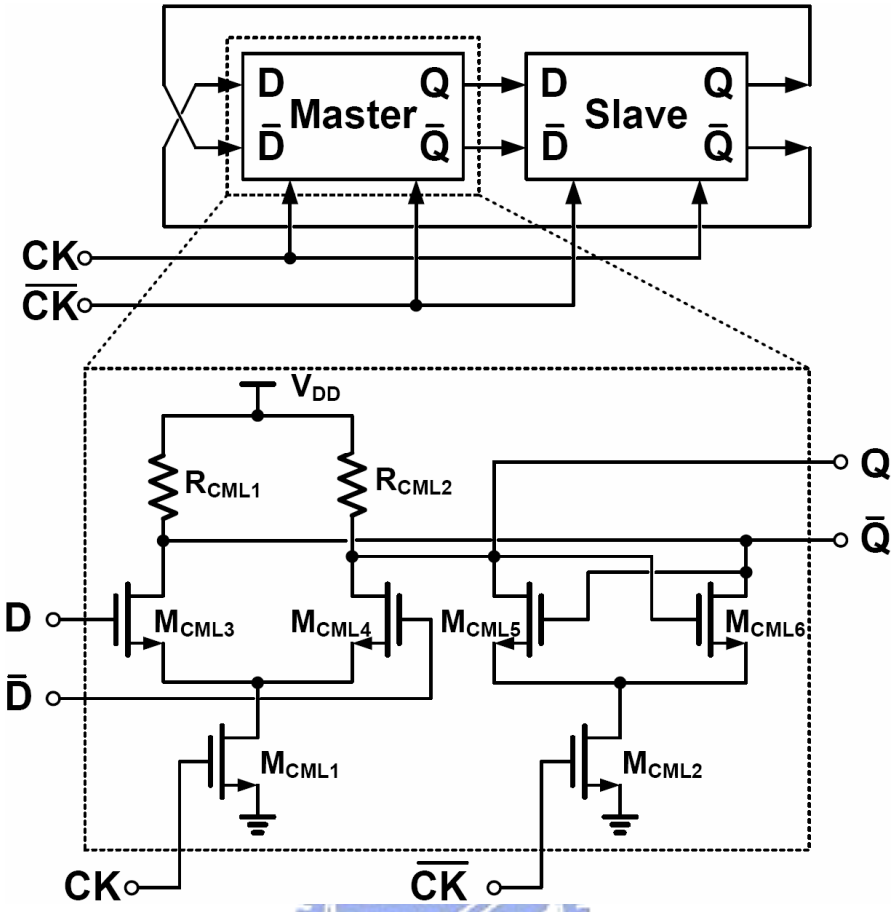
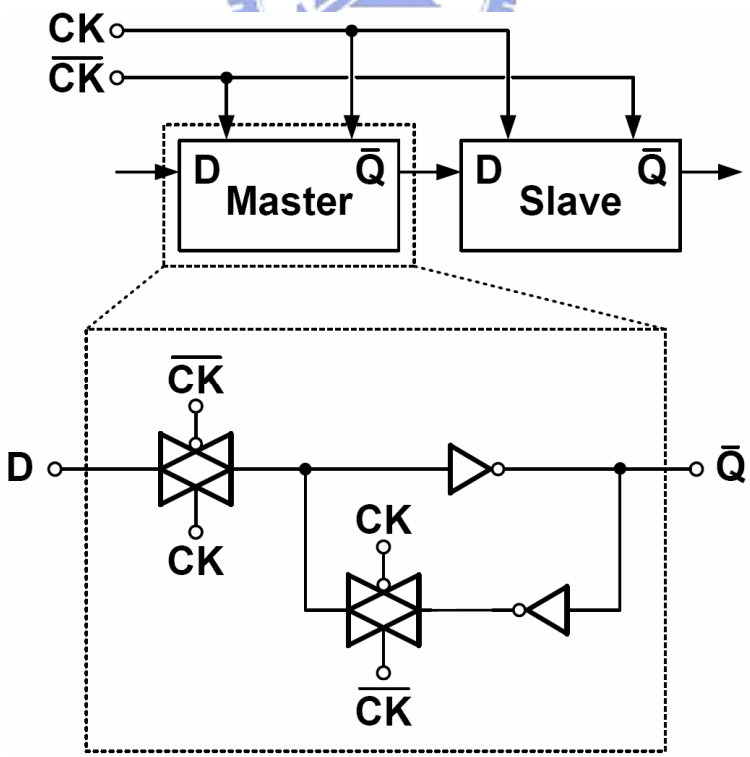


Fig. 3.10 HSPICE simulated coefficient of output harmonic current as a function of conduction angle.

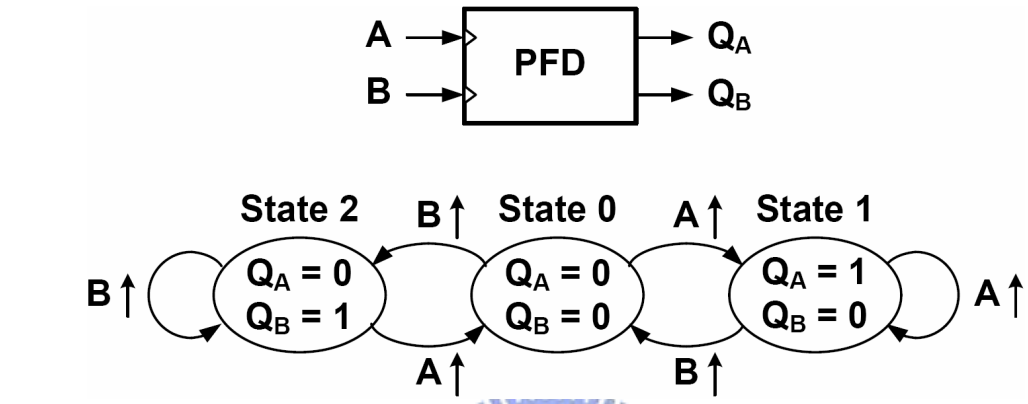


(a)

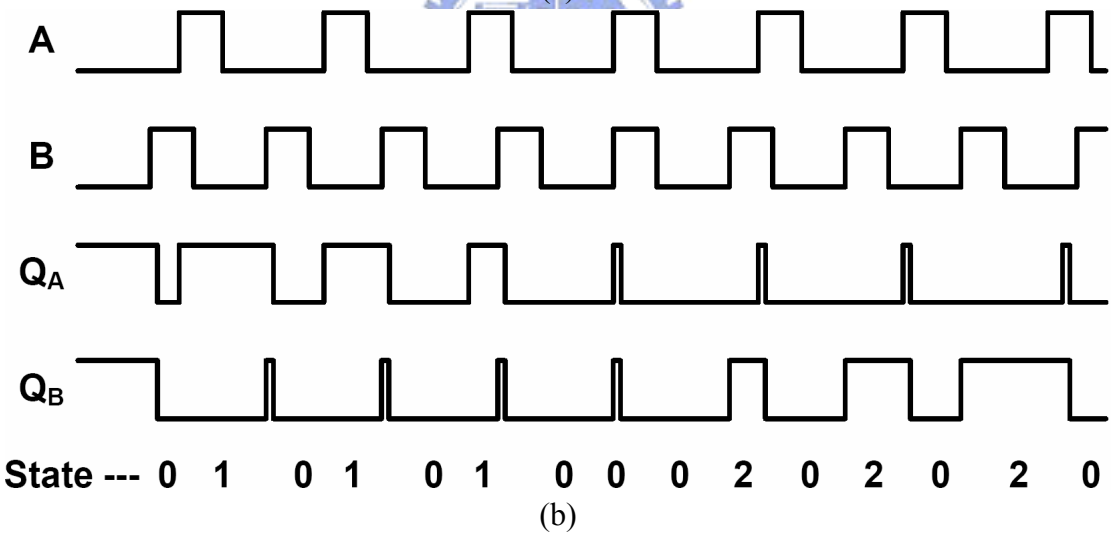


(b)

Fig. 3.11 Simplified schematic of (a) CML static divider and (b) digital static divider.



(a)



(b)

Fig. 3.12 PFD (a) state diagram and (b) timing diagram.

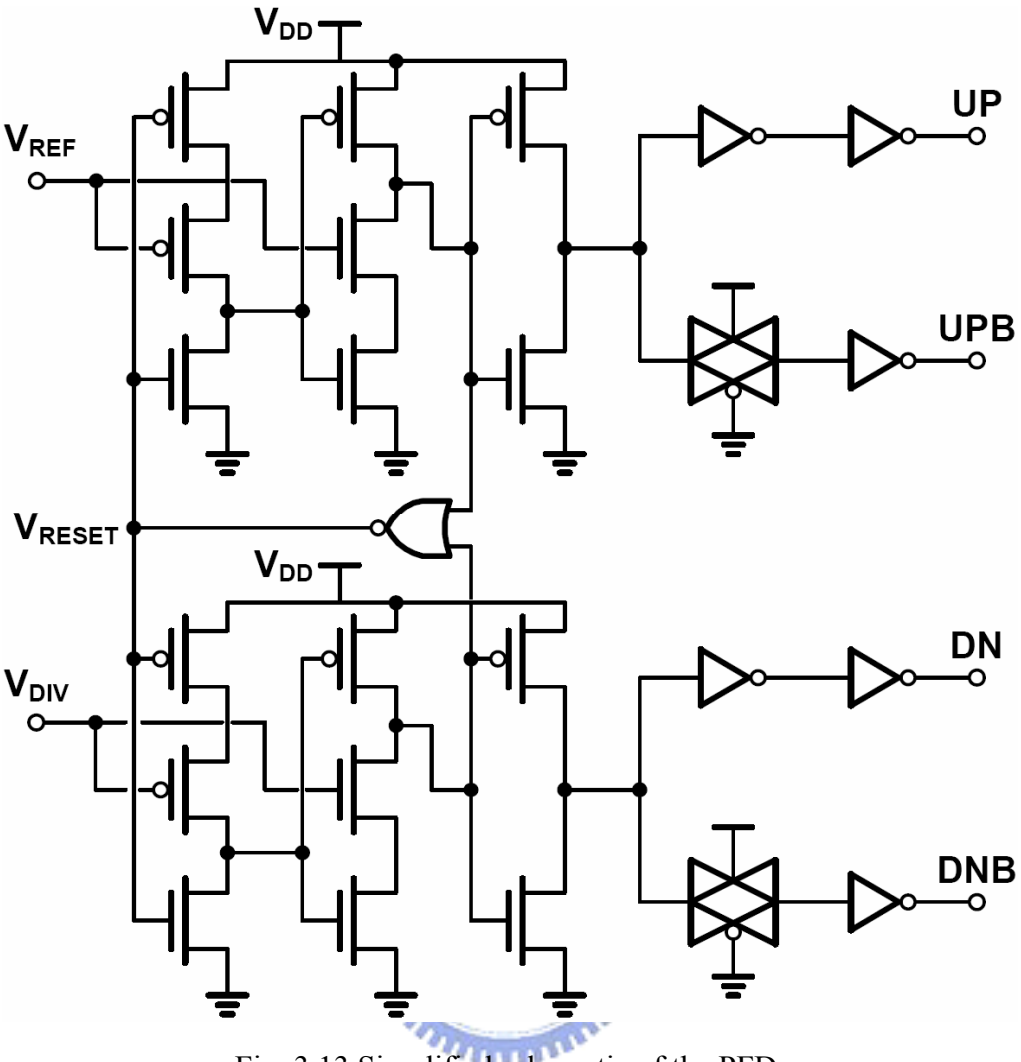


Fig. 3.13 Simplified schematic of the PFD.

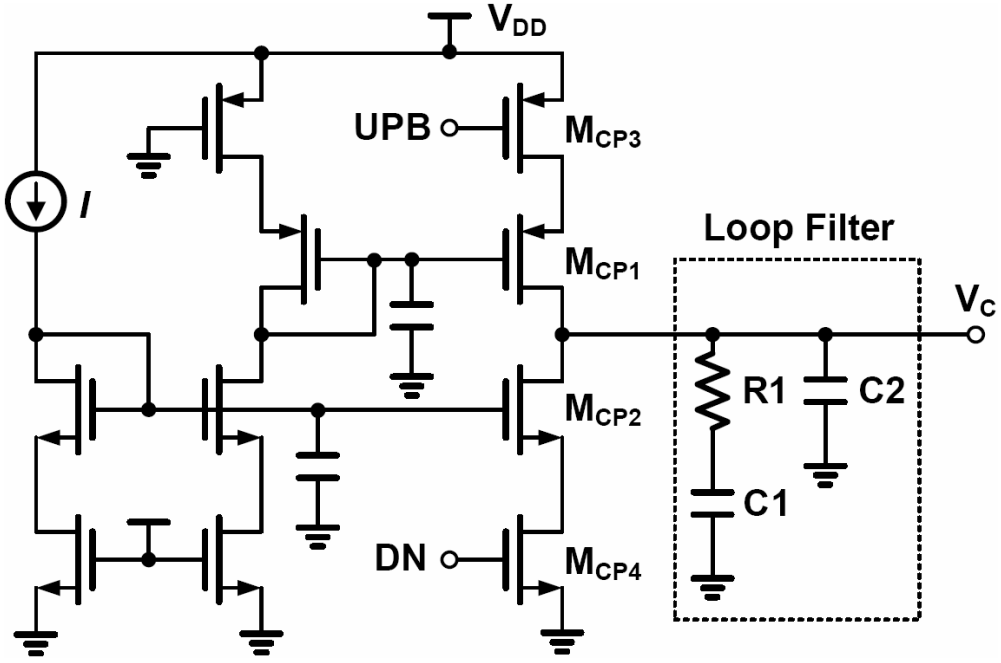
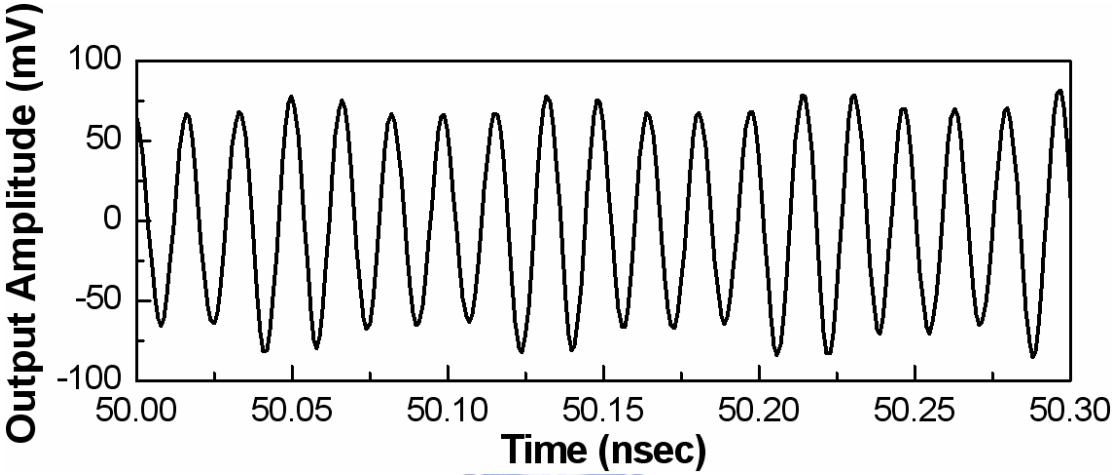
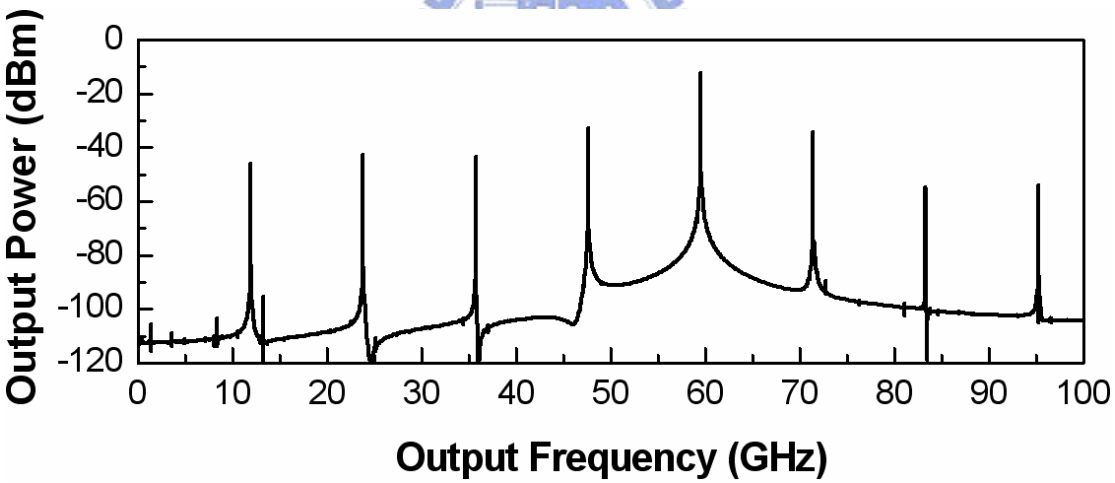


Fig. 3.14 Circuit diagram of the charge pump and loop filter.



(a)



(b)

Fig. 3.15 Simulated ILFM output (a) waveform and (b) power spectrum.

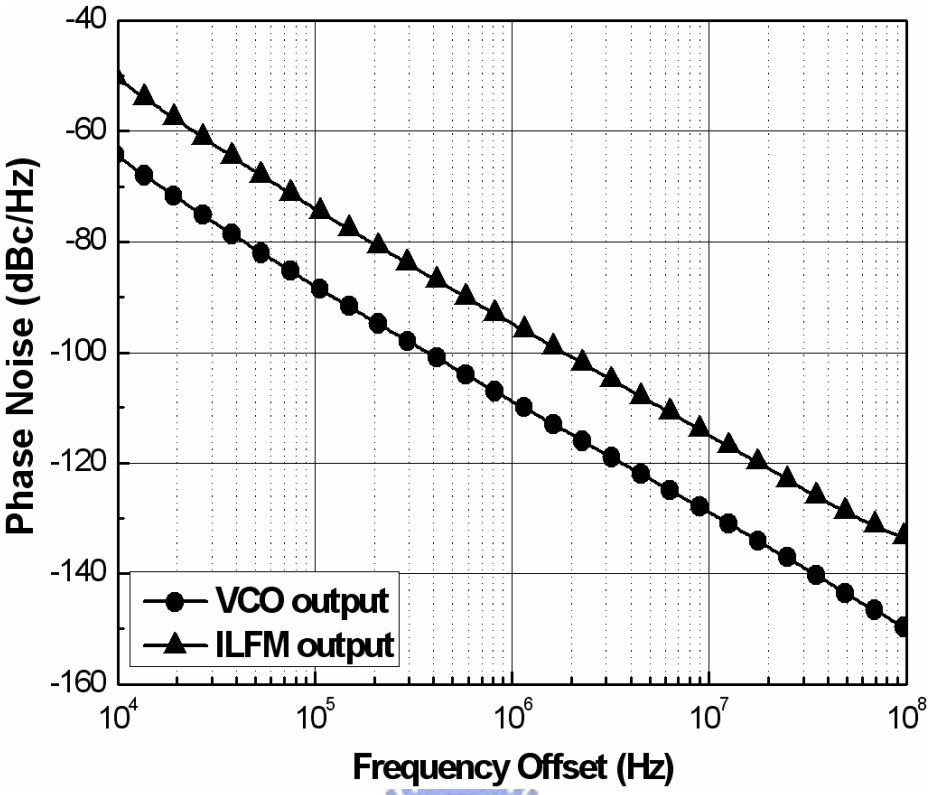


Fig. 3.16 Simulated output phase of VCO and ILFM.

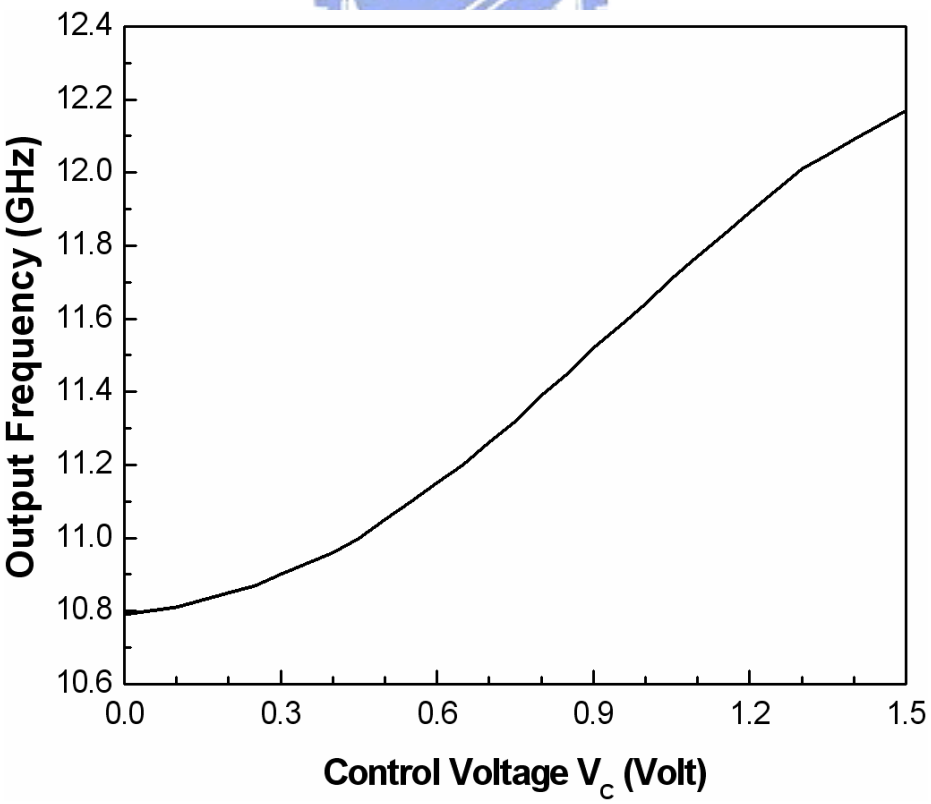
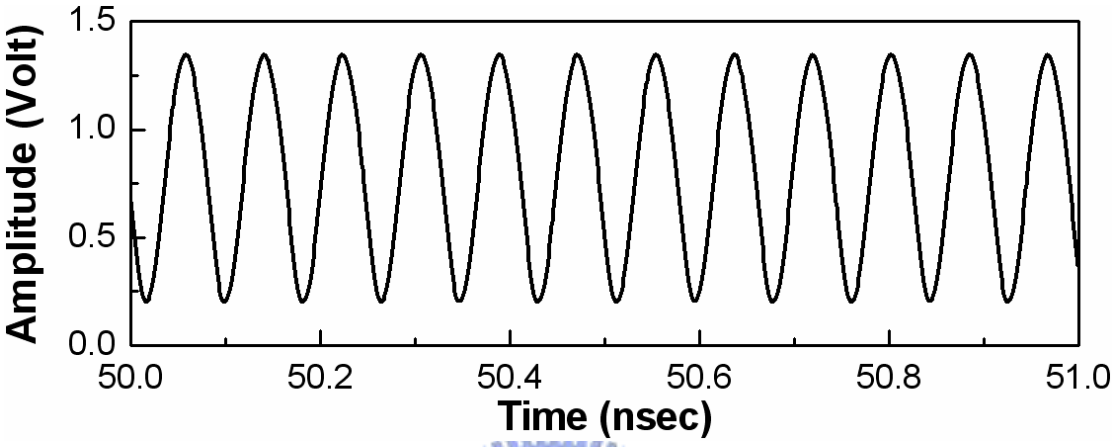
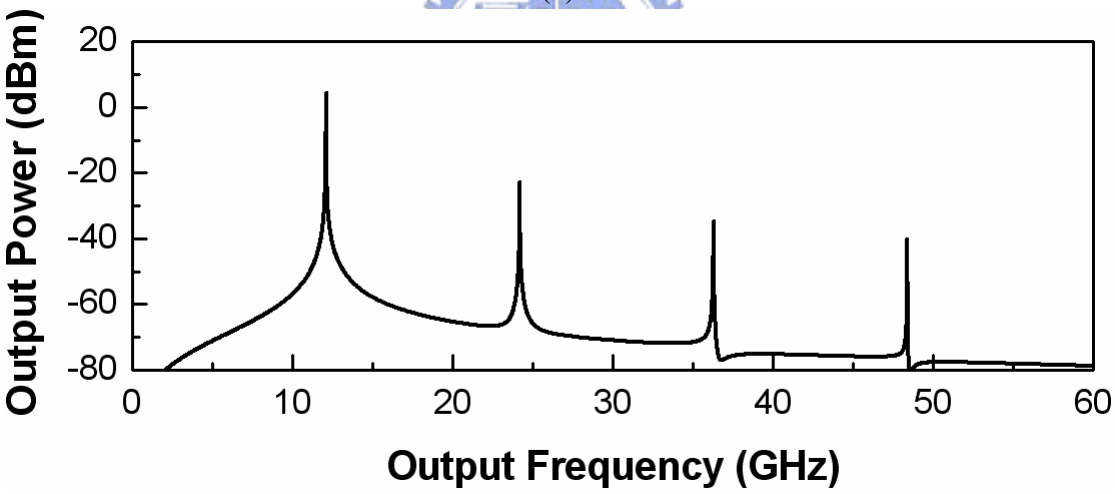


Fig. 3.17 Simulated VCO control voltage V_C versus output frequency.

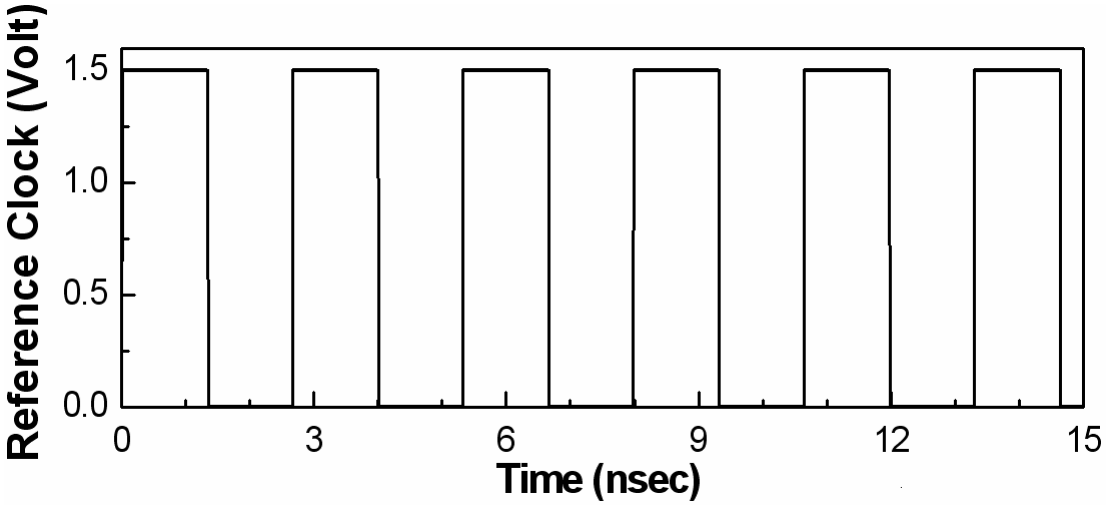


(a)

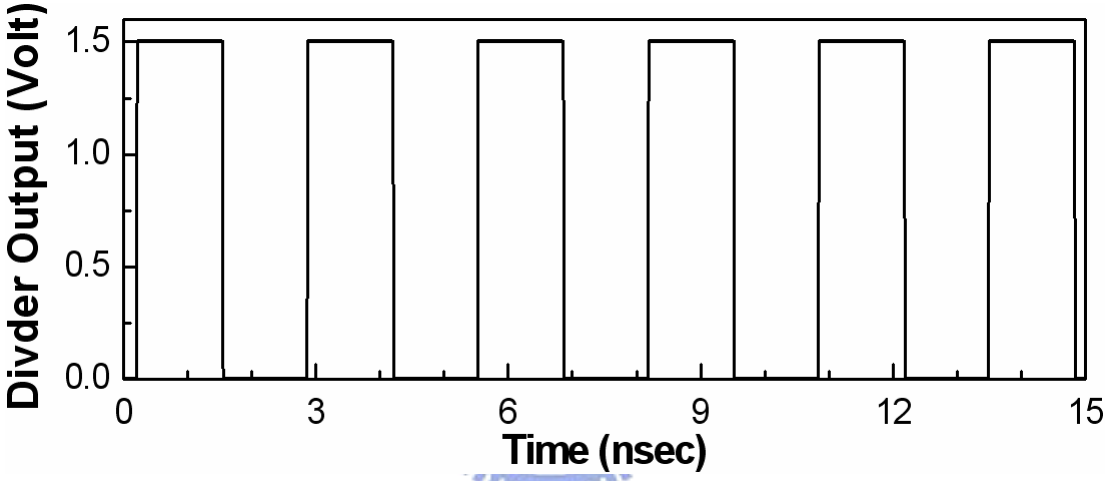


(b)

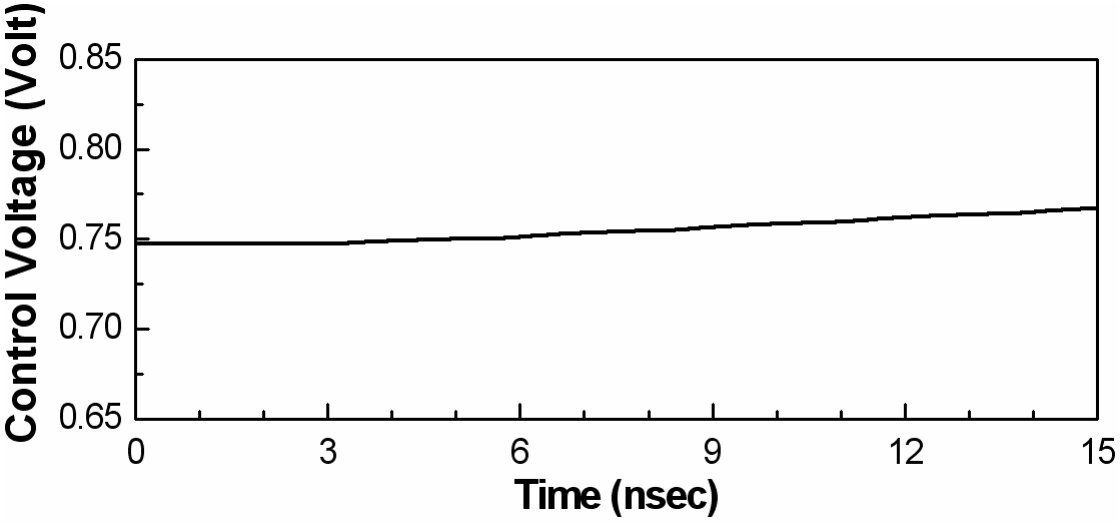
Fig. 3.18 Simulated VCO output (a) waveform and (b) power spectrum.



(a)

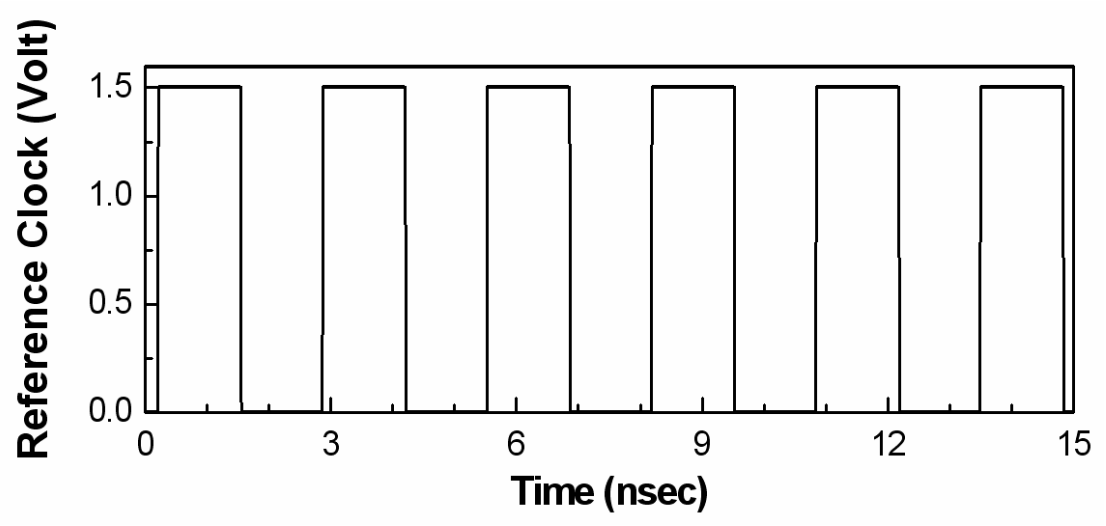


(b)

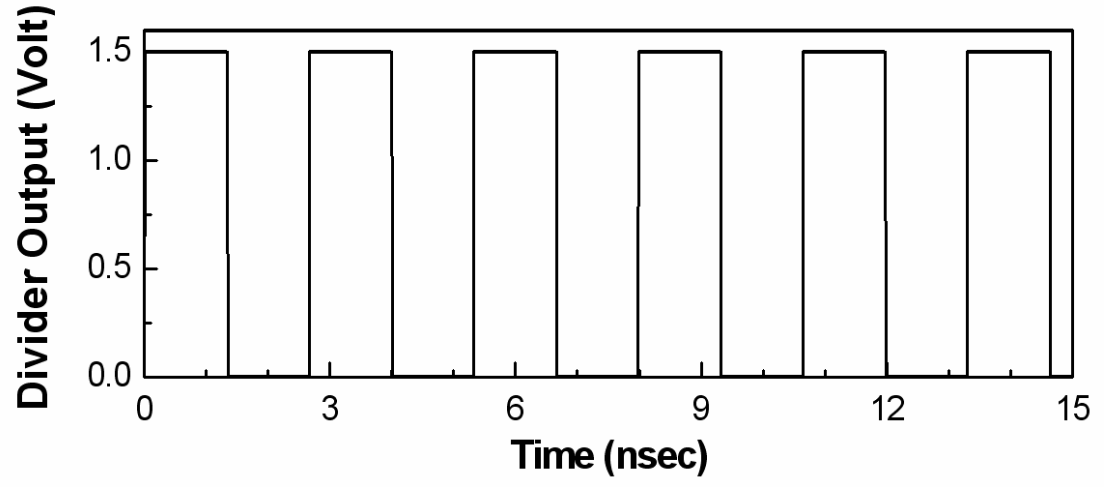


(c)

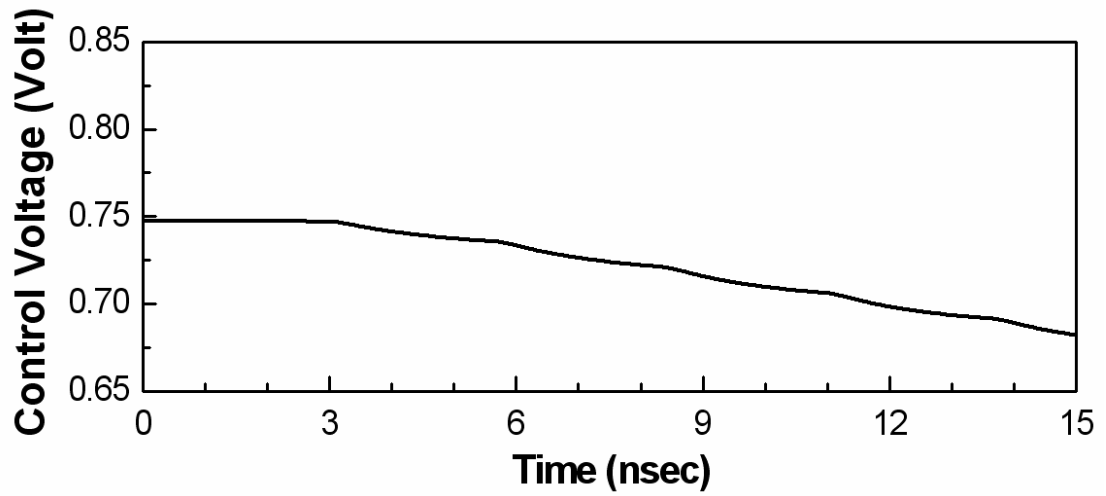
Fig. 3.19 Simulated waveforms of (a) reference clock, (b) divider output, and (c) control voltage of VCO with charging mode of charge pump.



(a)



(b)



(c)

Fig. 3.20 Simulated waveforms of (a) reference clock, (b) divider output, and (c) control voltage of VCO with discharging mode of charge pump.

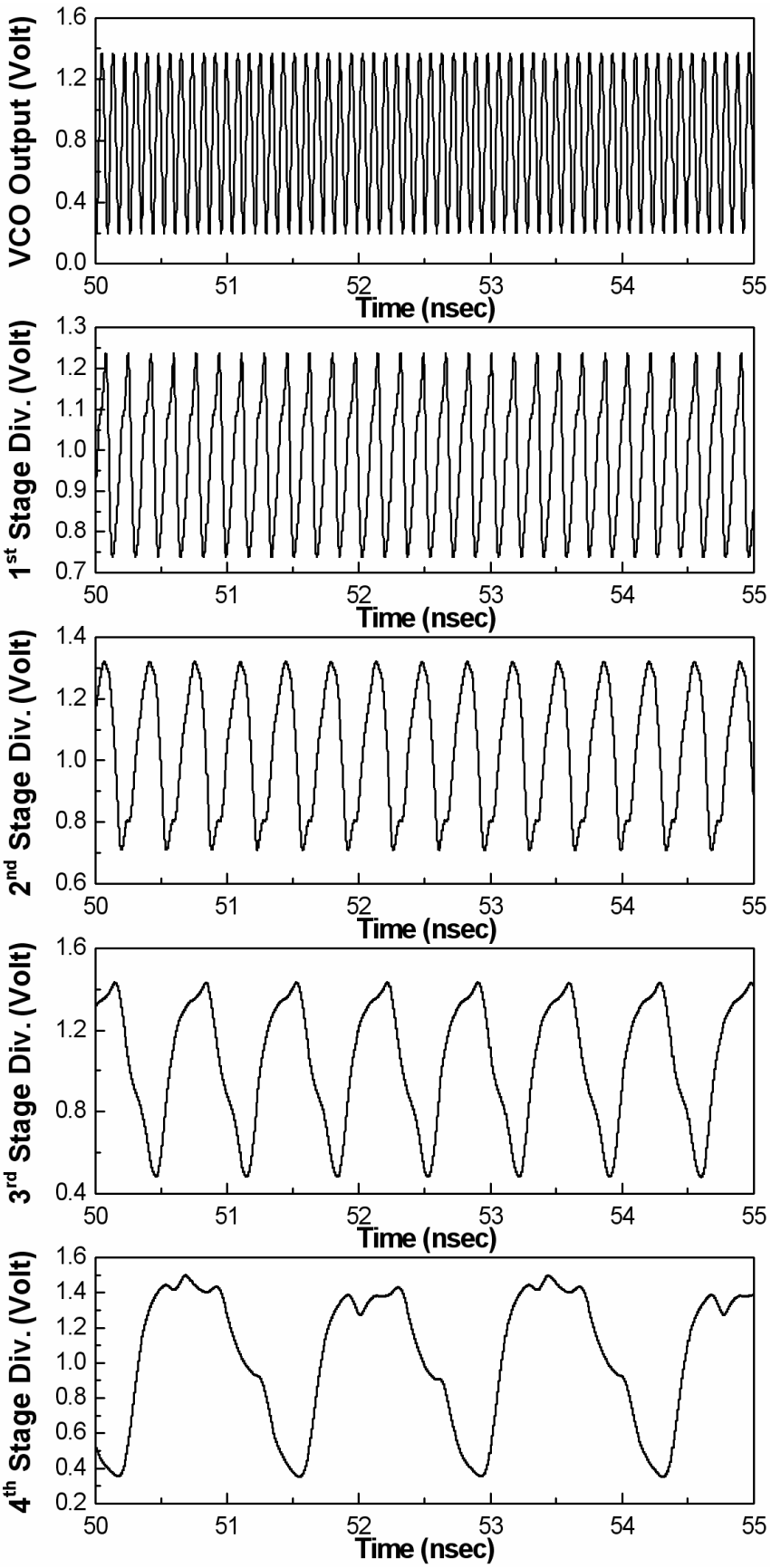


Fig. 3.21 Timing diagrams of VCO, first stage divider, second stage divider, third stage divider, and fourth stage divider.

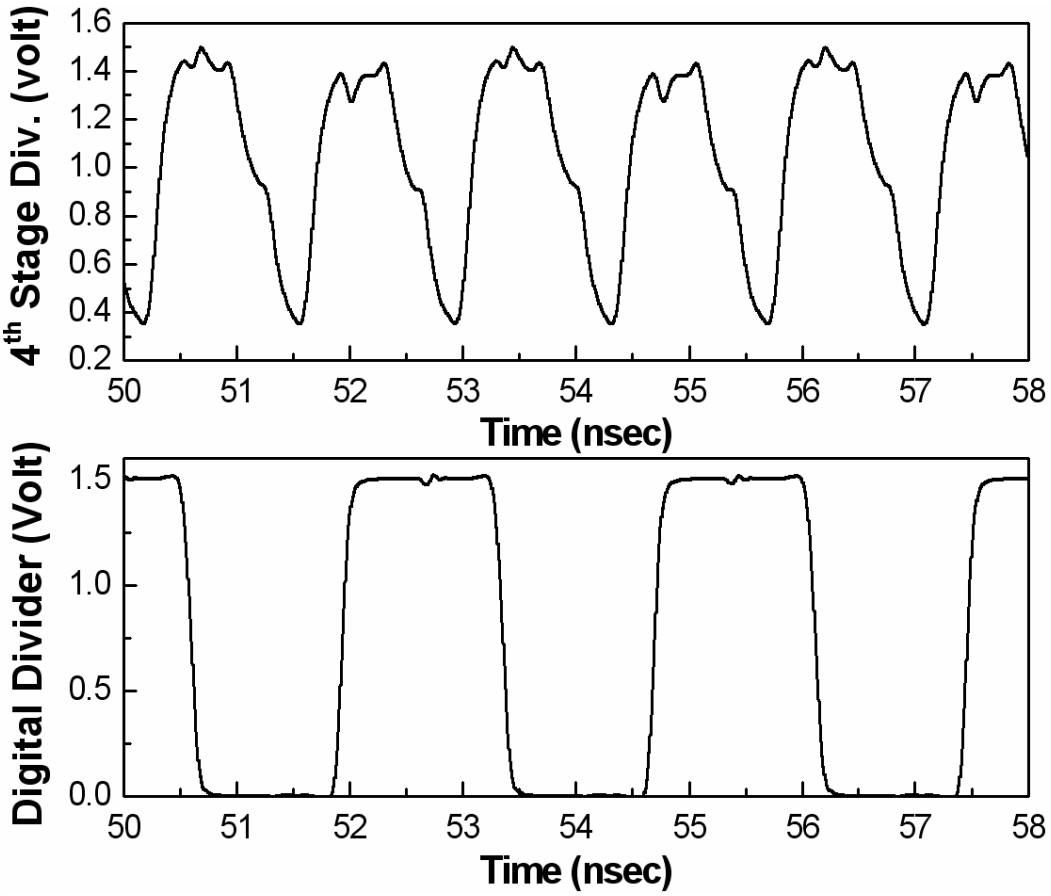


Fig. 3.22 Timing diagrams of the last digital frequency divider output waveform.

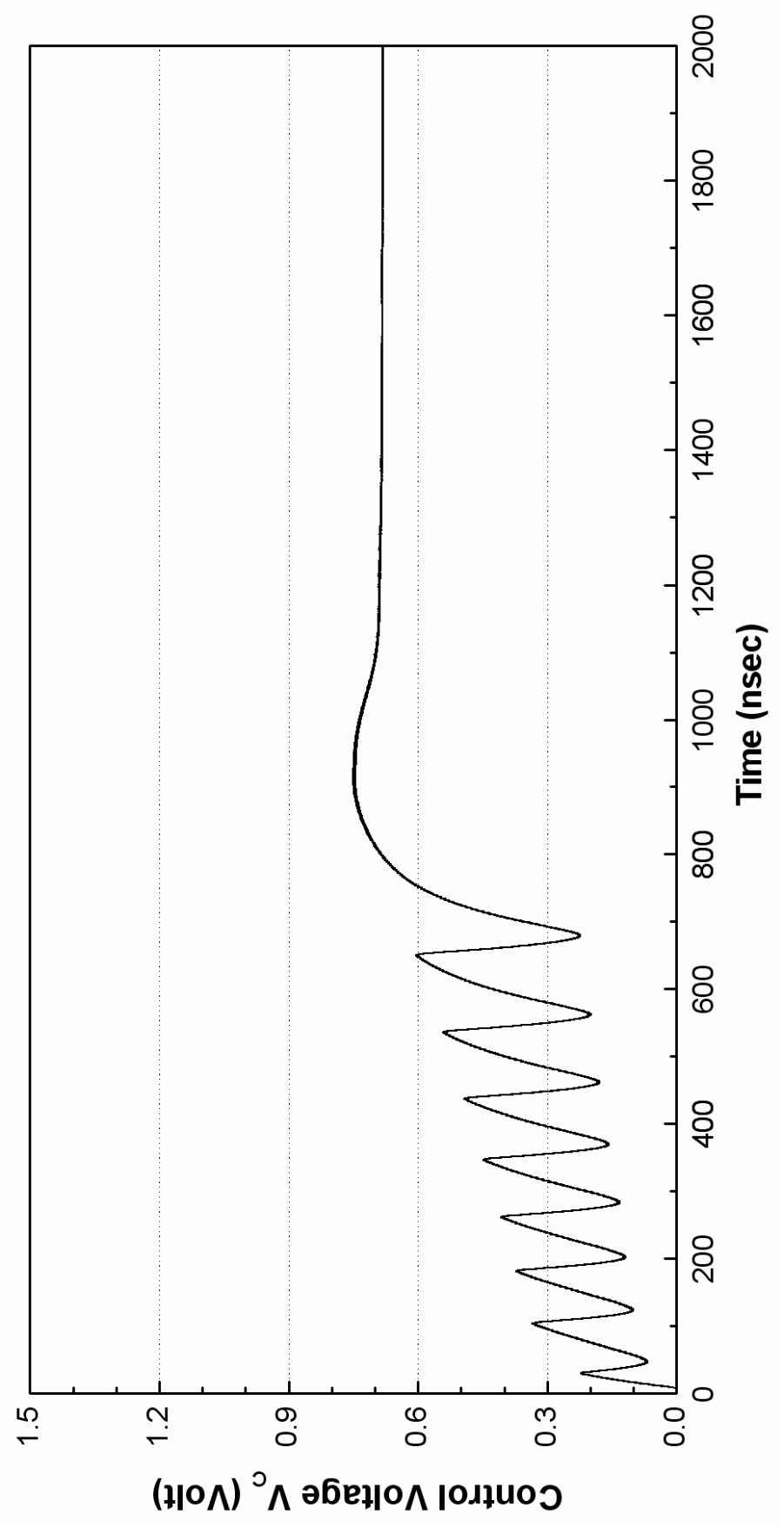


Fig. 3.23 Simulated waveform of control voltage V_C in close-loop simulation.

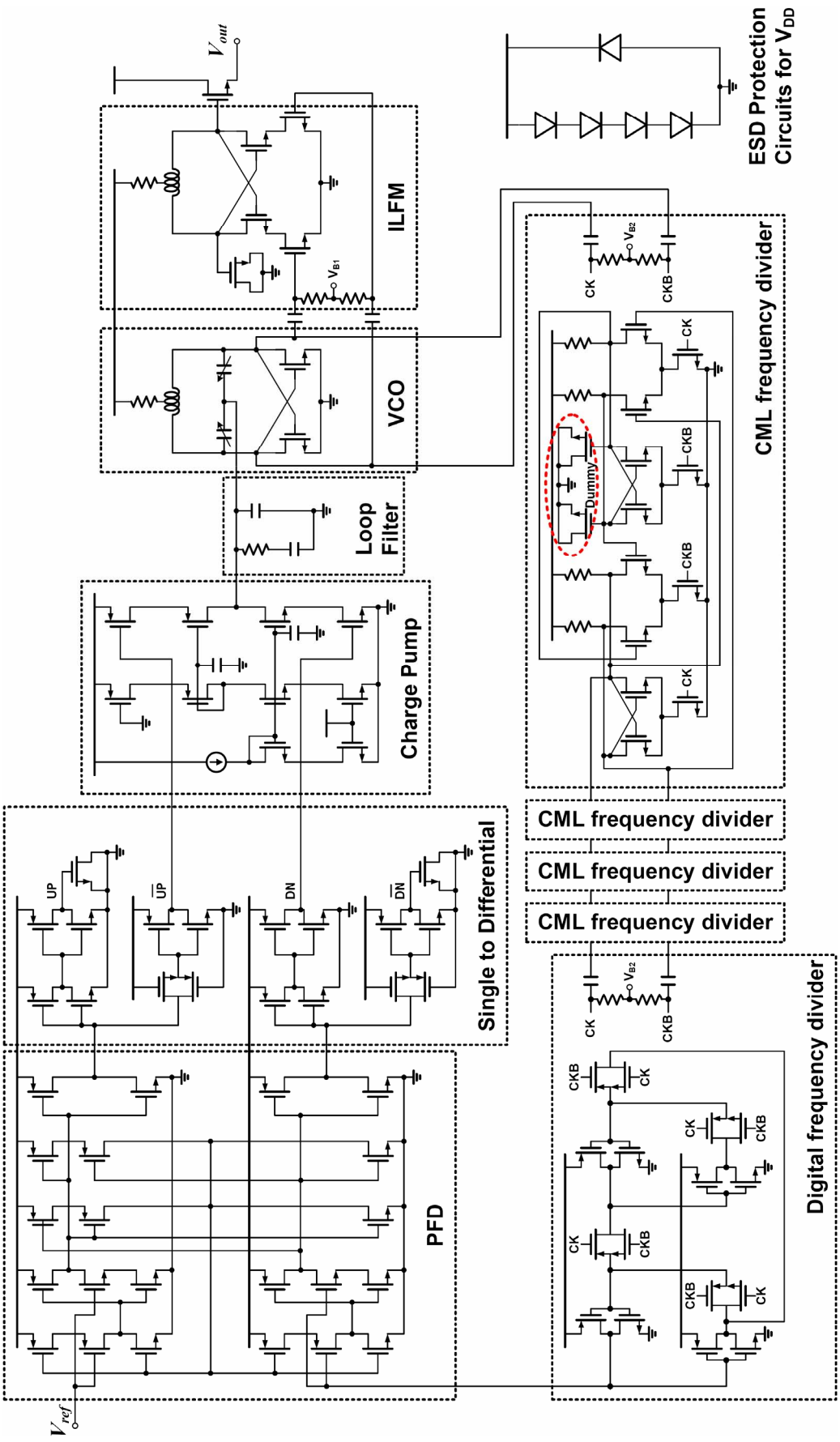


Fig. 3.24 Circuit diagram of the overall PLL.

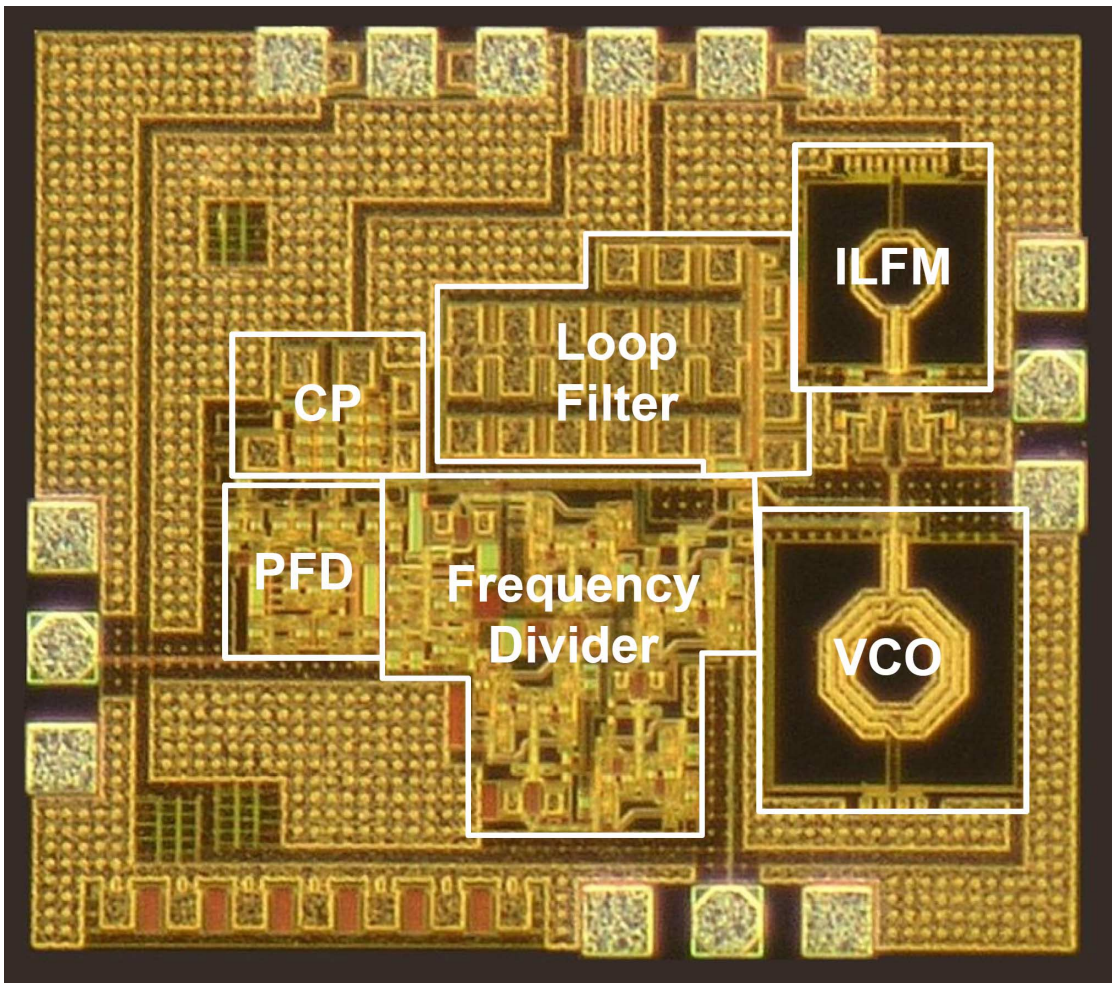


Fig. 3.25 Chip microphotograph of the proposed 60-GHz PLL (0.96 mm × 0.84 mm).

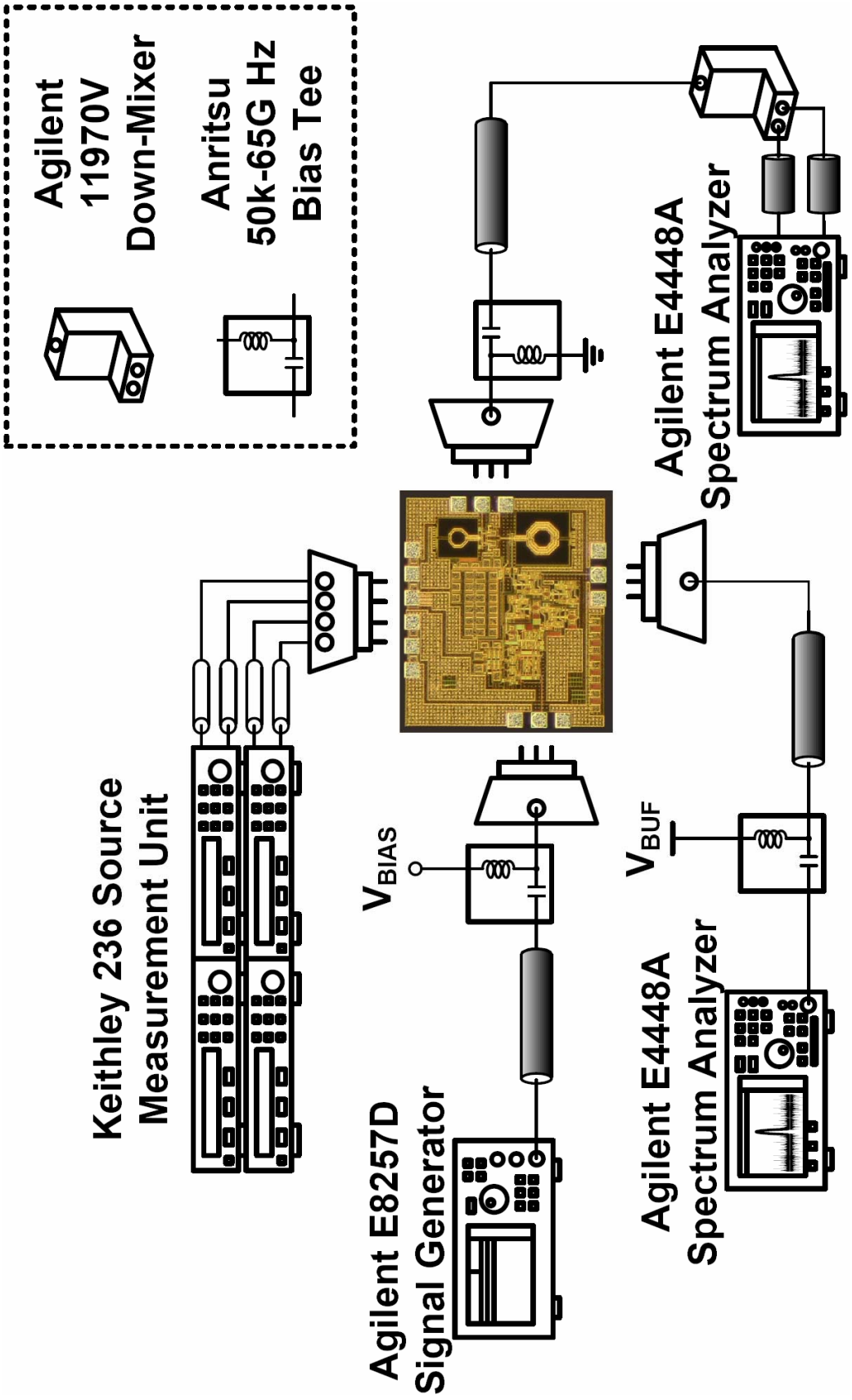


Fig. 3.26 Measurement setup for 60-GHz PLL testing.

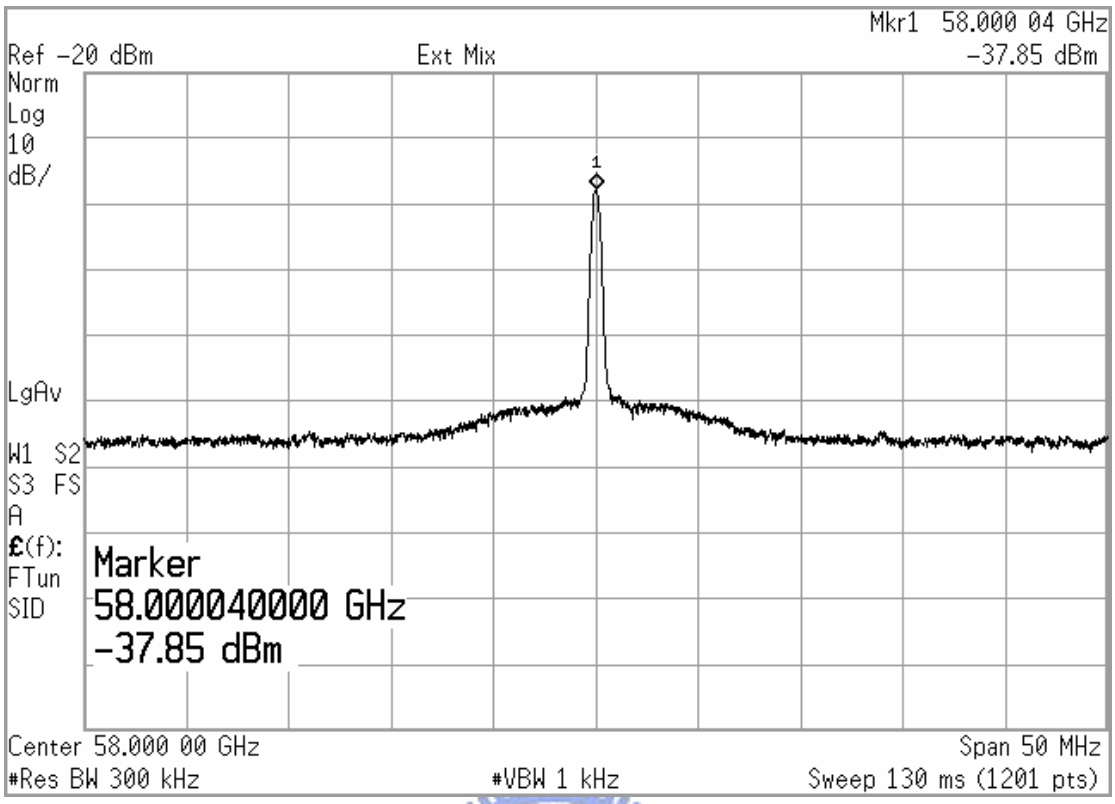


Fig. 3.27 Measured Output spectrum of the 60-GHz PLL with 362.5-MHz reference frequency f_{ref}.

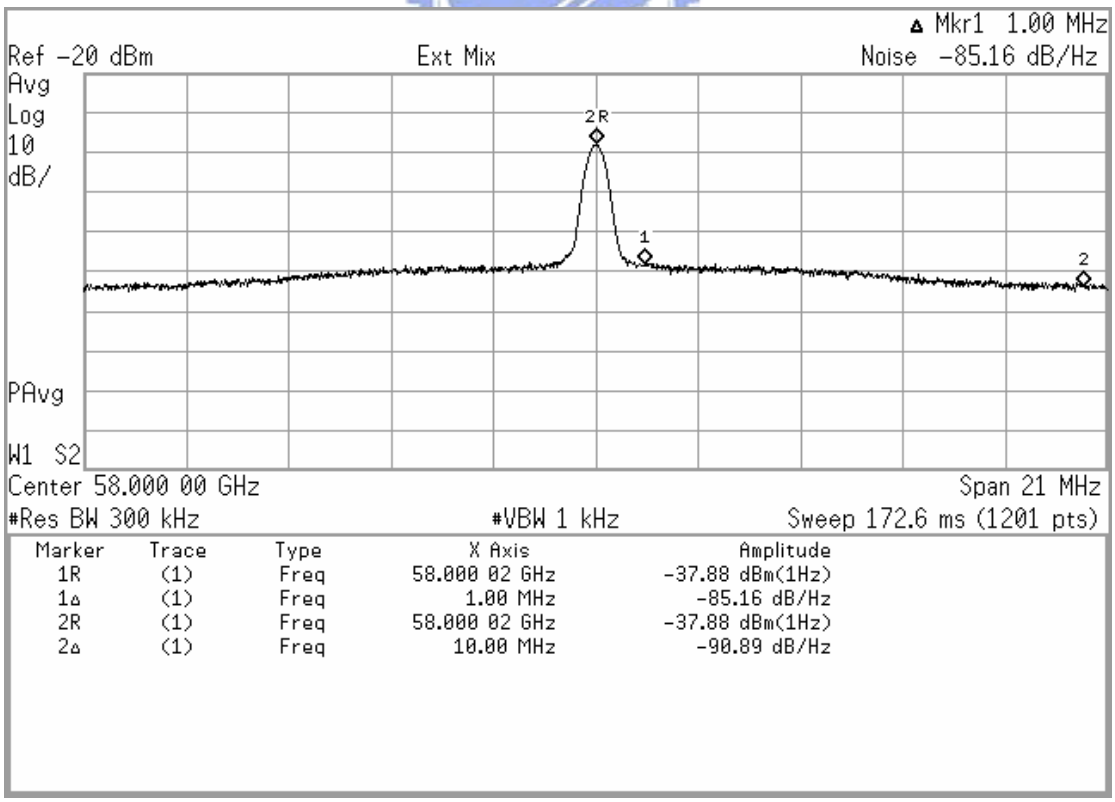


Fig. 3.28 Measured output phase noise marked at the offset frequency of 1MHz and 10 MHz.

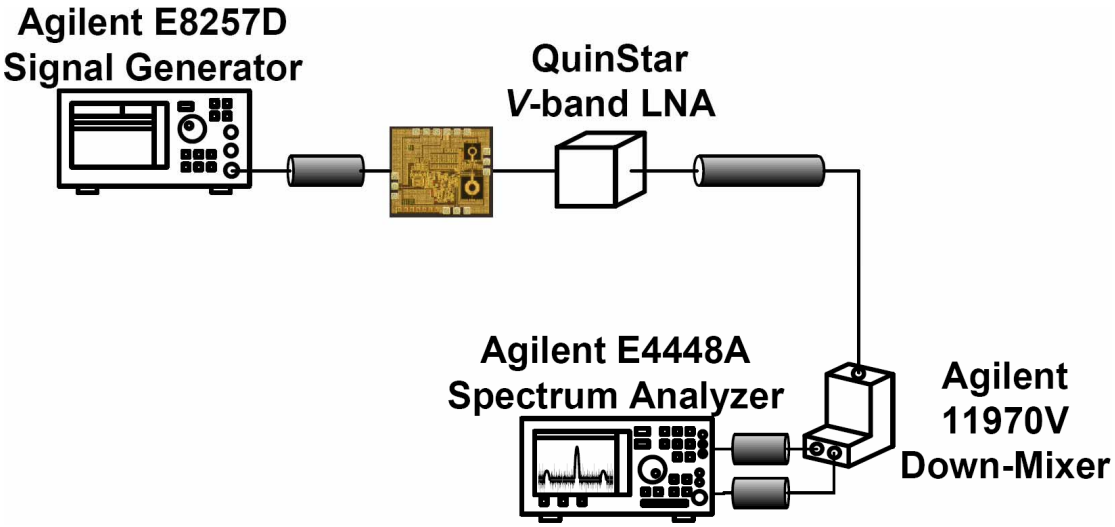


Fig. 3.29 Measurement setup for the reference spurs testing.

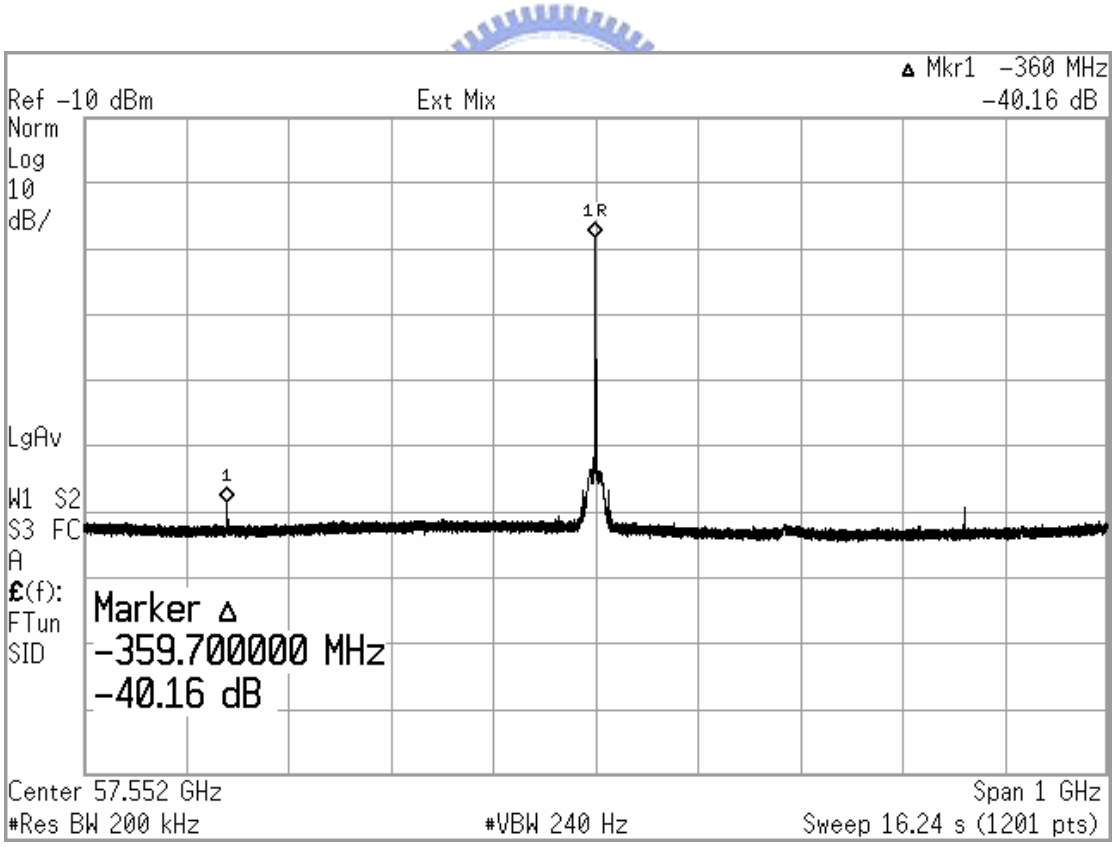


Fig. 3.30 Measured reference spurs as the reference frequency of 359.7 MHz.

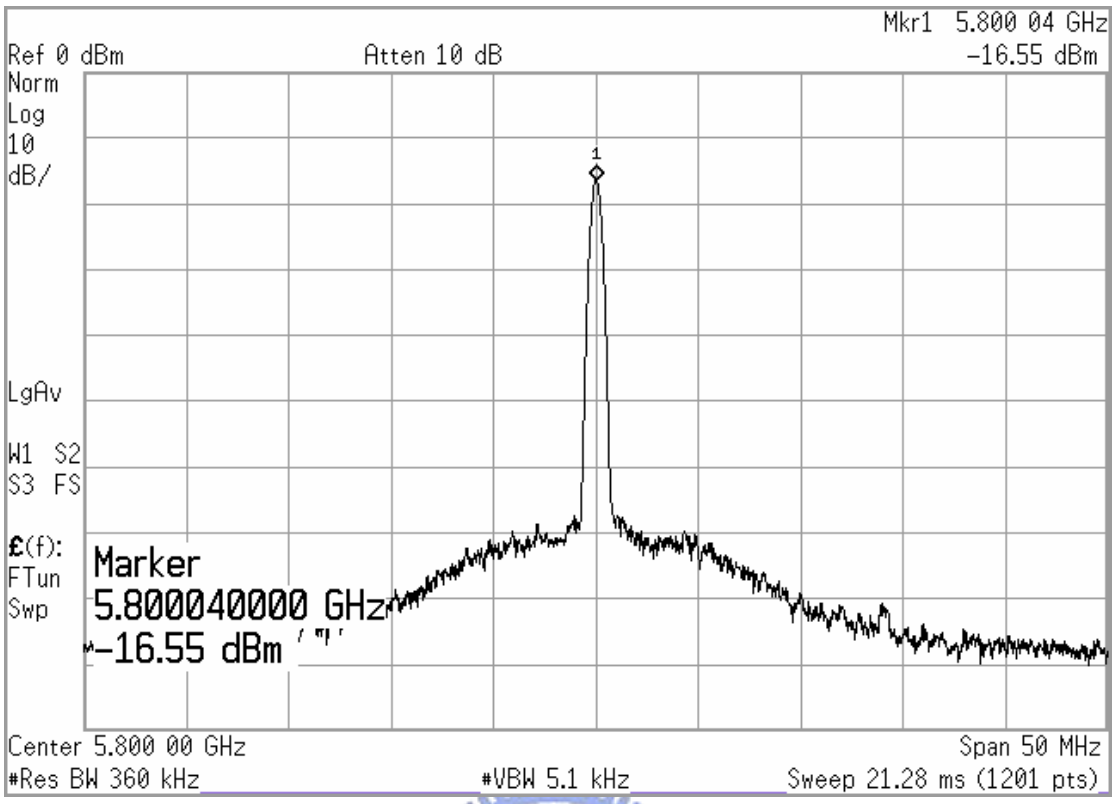


Fig. 3.31 Measured output spectrum of the first divide-by-two frequency divider.

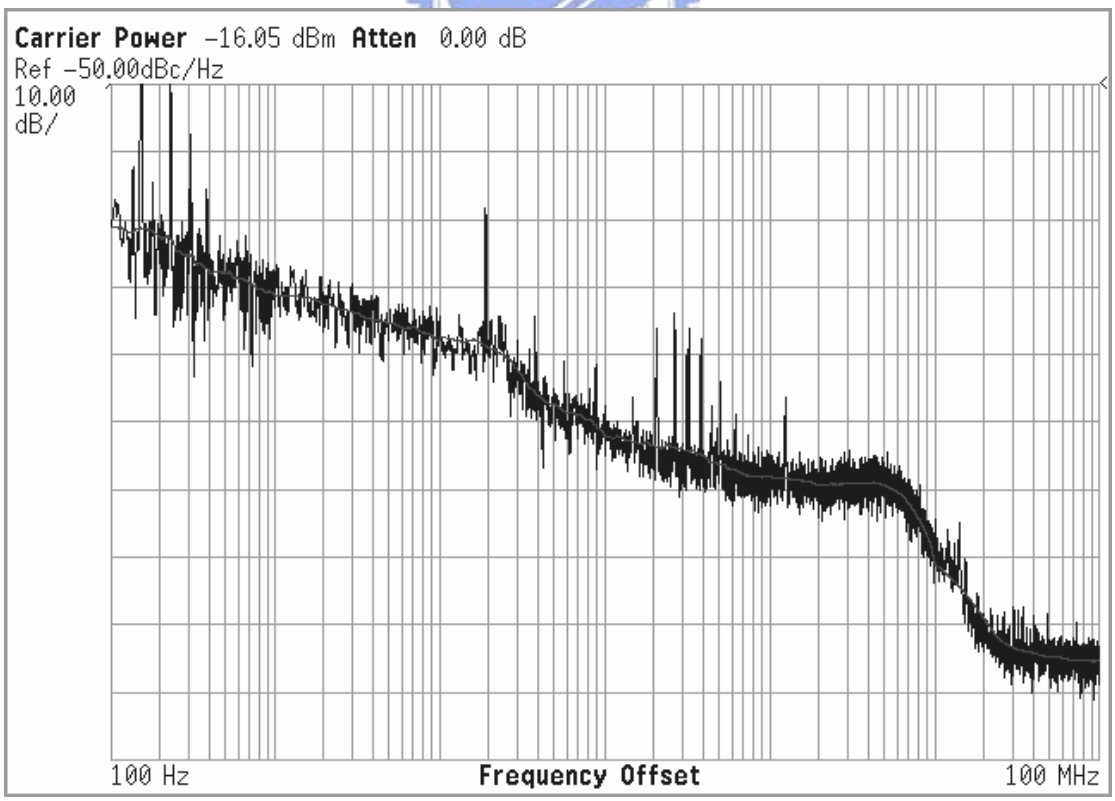


Fig. 3.32 Measured phase noise of the first divide-by-two frequency divider.

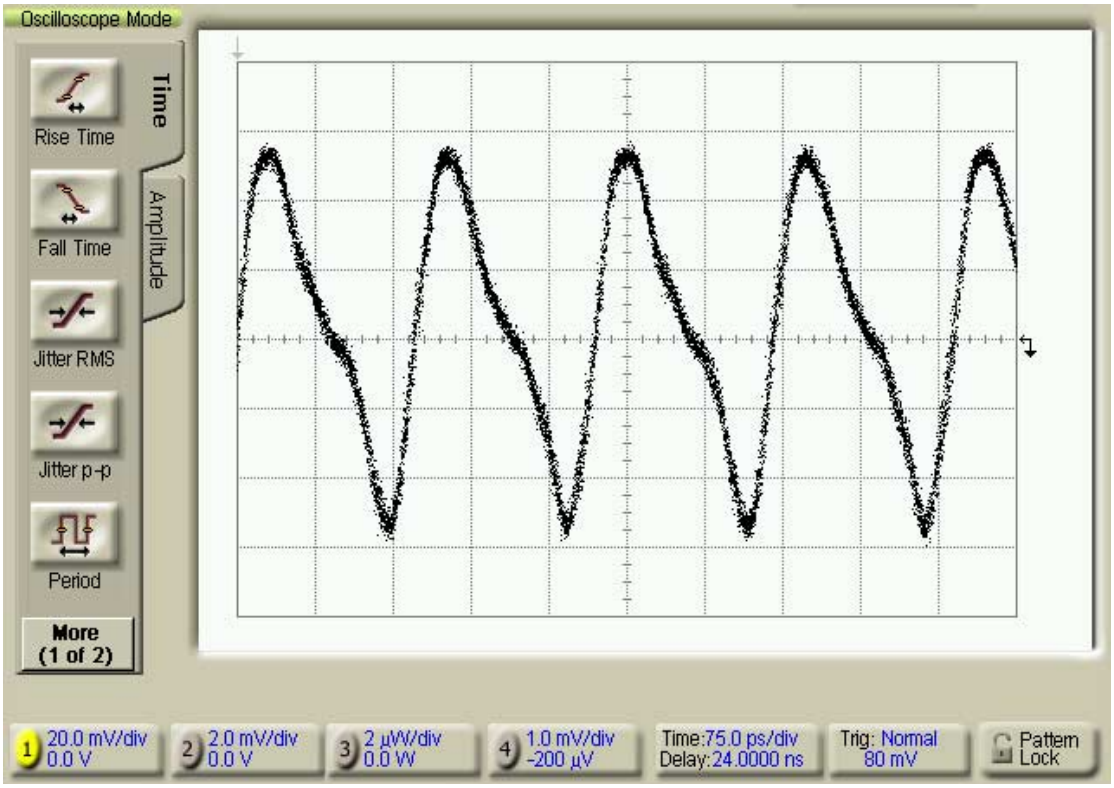


Fig. 3.33 Measured output waveform of the first divide-by-two frequency divider.

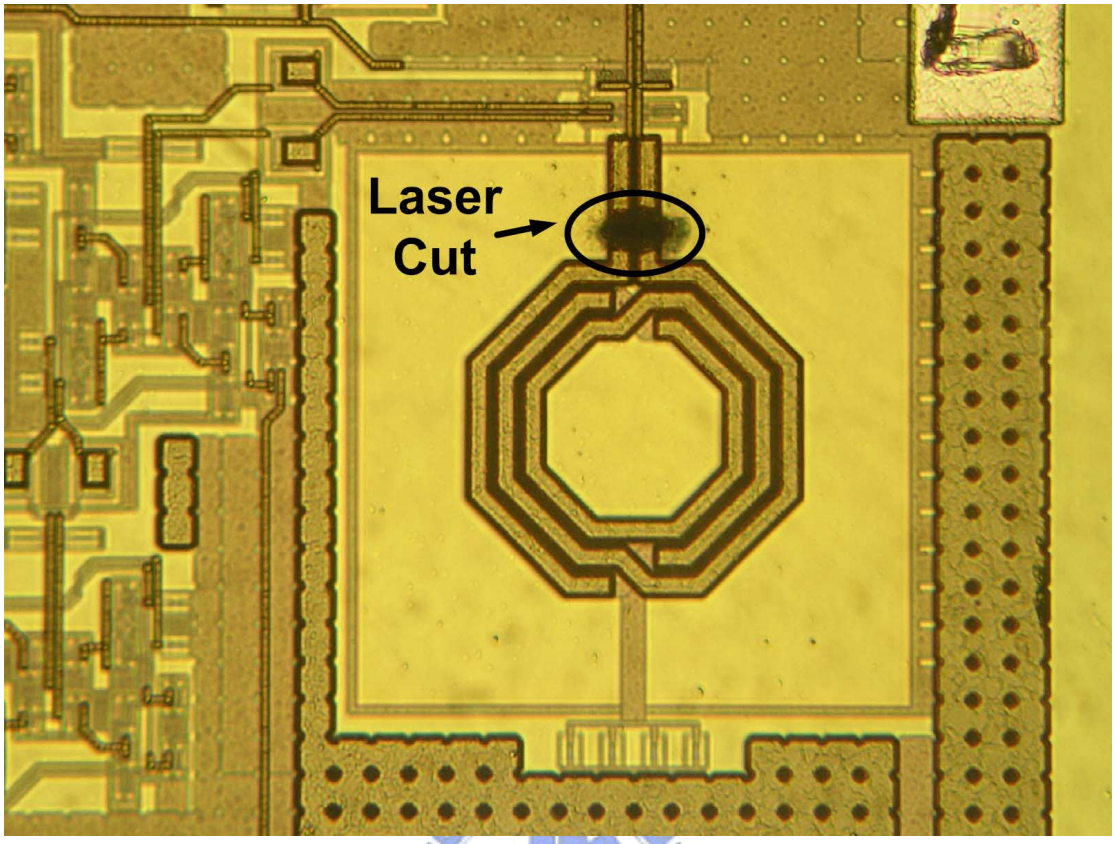


Fig. 3.34 The microphotograph of the laser cut position.

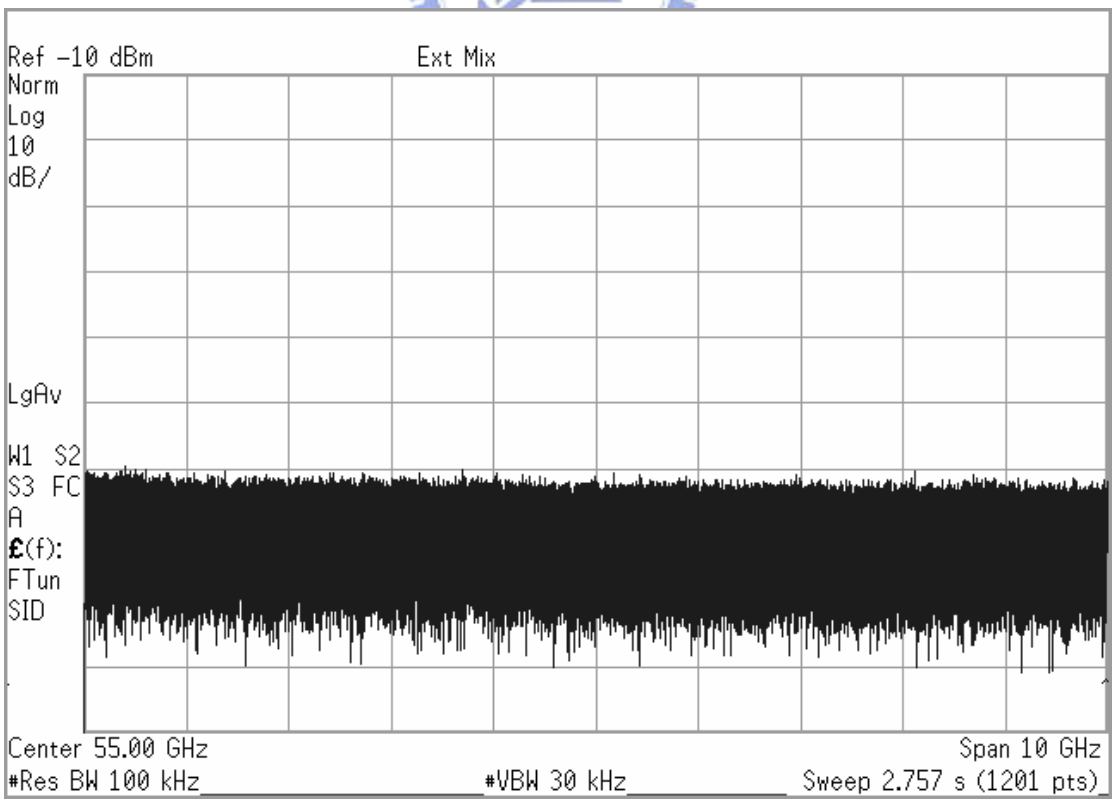
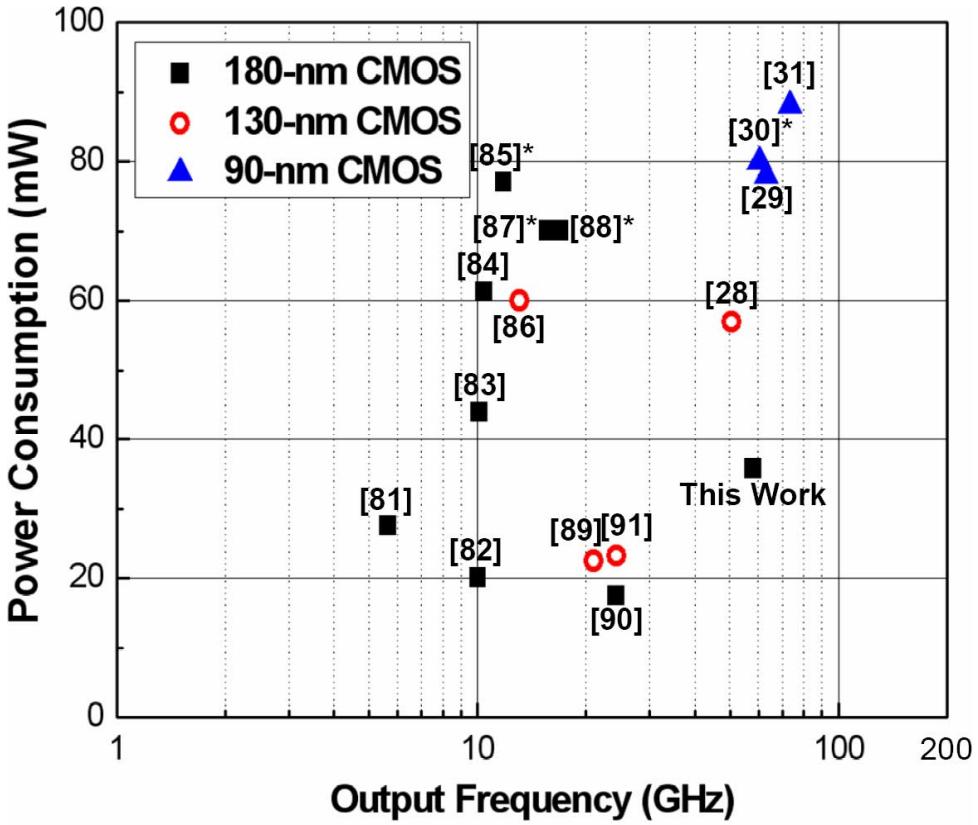


Fig. 3.35 Measured the output spectrum of the free-running ILFM.



* These designs are frequency synthesizers.

Fig. 3.36 Power consumption as a function of output frequency.

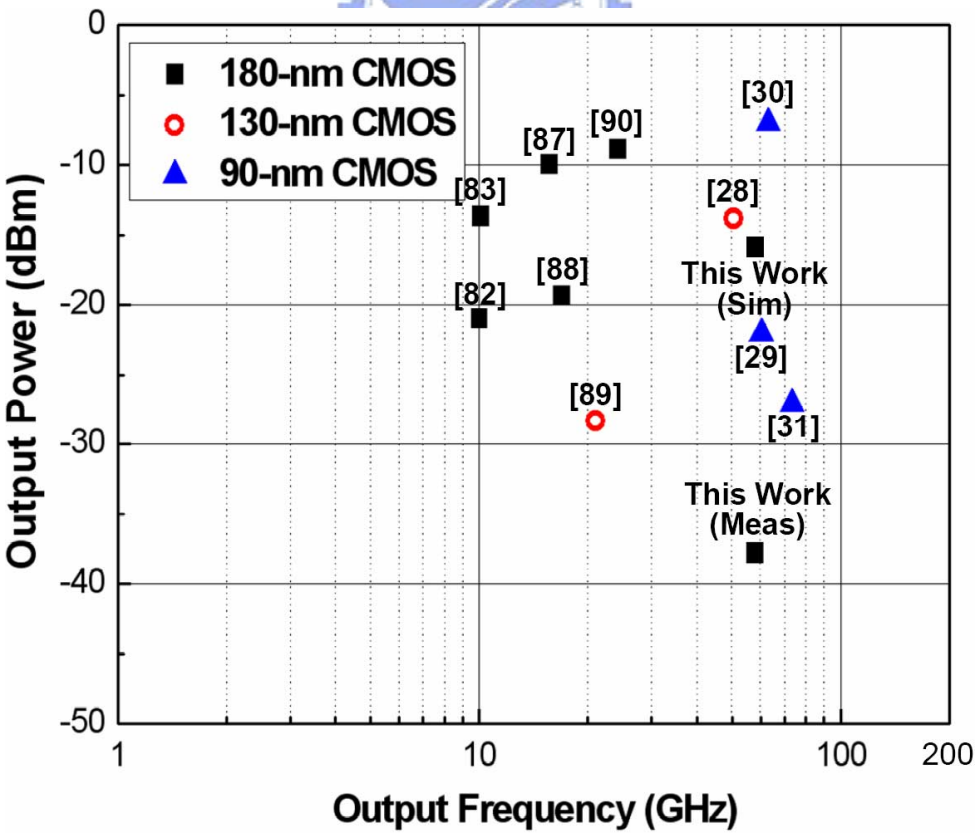


Fig. 3.37 Output power as a function of output frequency.

CHAPTER 4

60-GHZ CMOS DIRECT-CONVERSION RECEIVER FRONT-END WITH INJECTION-LOCKED FREQUENCY TRIPLERS

In this chapter, the design of low-power 60-GHz CMOS direct-conversion receiver front-end is described. The proposed direct-conversion receiver can be operated with 20-GHz frequency synthesizer because injection-locked frequency triplers (ILFTs) [25] are used for 60-GHz local oscillator (LO) signals generation. Injection-locked oscillators (ILOs) have the superior properties of frequency stabilization and high gain amplification with a narrow bandwidth [26]. Therefore, frequency multiplier integrated with ILO can be the solution to the large power consumption of conventional frequency multiplier in [18]–[19] because it can be operated for signal amplification with small power consumption. Finally, the proposed direct-conversion receiver provides the advantages of high integration, low power consumption, and small chip area.

In Section 4.1, the receiver system design considerations are described. The proposed architecture of direct-conversion receiver front-end that takes advantage of ILFT to reduce the overall power consumption is given in Section 4.2. Section 4.3 is presented the building blocks of the proposed receiver including low-noise amplifier (LNA), down-conversion mixer, quadrature voltage-controlled oscillator (QVCO), ILFT, intermediate-frequency amplifier (IFA), and output buffer. The experimental results are shown in Section 4.4. Finally, the conclusion and summary are given in Section 4.5.

4.1 SYSTEM DESIGN CONSIDERATIONS

Due to the required system specifications and the trend of advanced CMOS technology, some system design parameters become the important challenges for millimeter-wave CMOS receiver front-end design.

4.1.1 Noise Figure

The noise performance of the receiver front-end defines the sensitivity of the receiver front-end by limiting the lowest input RF power that can be detected with a reasonable data error rate by the receiver. The noise factor (F) is defined as

$$F \equiv \frac{\left(\frac{S}{N}\right)_{input}}{\left(\frac{S}{N}\right)_{output}} = \frac{N_{output}}{G_a N_{input}} \tag{4.1}$$

where $(S/N)_{input}$ and $(S/N)_{output}$ are the signal-to-noise ratio (SNR) at a system of input and output, respectively; G_v is the available power gain; and N_{input} and N_{output} are the total noise at the input and output of a system, respectively.

In general, N_{output} can be expressed as

$$N_{output} = G_a N_{input} + N_{system} \tag{4.2}$$

where N_{system} is the total noise contribution from the system. It can be seen from (4.1) and (4.2) that F can be decreased by increasing the available power gain of the system G_a and decrease the noise contribution from the system.

The performance of a cascade system with total stage of M as shown in Fig. 4.1 can be calculated by the Frii's formula. The total available power gain (G_{total}) and total noise factor (F_{total}) are expressed as

$$G_{total} = G_1 \times G_2 \times G_3 \times \Lambda \times G_M \tag{4.3}$$

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \Lambda + \frac{F_M - 1}{G_1 G_2 G_3 \Lambda \; G_{M-1}} \tag{4.4}$$

where G_n and F_n are the available power gain and F of the n-th stage, respectively.

It can be seen from (4.4) that the F_{total} can be minimized by either the increase of the available power gain G_1 or the decrease of the F_1. Therefore, the first stage of the receiver front-end is designed with minimum F and reasonable gain for lower system F and higher system sensitivity. For this reason, it is important to have a low noise amplifier as close to the antenna as possible.

Noise figure (NF) in dB can be expressed as

$$NF = 10\log(F) \tag{4.5}$$

The minimum input signal strength needed to produce a good quality output signal is referred to as the receiver sensitivity. The sensitivity of the receiver can be written as [92]

$$P_{sen} = -174 \text{ dBm/Hz} + 10\log(BW) + NF_{RX} + SNR_{\min} \tag{4.6}$$

where BW is the channel bandwidth in hertz, NF_{RX} is the NF of receiver front-end in dB, and SNR_{min} is the minimum SNR for digital section.

The possible channel for 60-GHz application is 1728 MHz as shown in Chapter 1. By substituting 1728 MHz to (4.6), we have

$$P_{sen} = -81.6 \text{ dBm/Hz} + NF_{RX} + SNR_{\min} \tag{4.7}$$

It can be seen from (4.7) that the sensitivity for wide channel bandwidth can not be too low due to large channel bandwidth.

A simple for 60-GHz system is given as followed. By assuming that the modulation is QPSK with bit-error rate of 10^{-6} with additive white Gaussian noise (AWGN) channel and the *NF* from receiver is 15 dB, it has the sensitivity of –55.6 dBm [= –81.6 + 15 +11].

4.1.2 P1dB and IIP3

Linearity is the criterion that defines the upper limit for detectable RF input power level of the receiver. The linearity performance of a RF system is usually determined by 1dB compression point (P1dB) and input-referred third-order intercept point (IIP3).

The P1dB value is defined as the input power level at which the power gain is decreased 1dB. The IIP3 is defined as the input power where the output powers of the fundamental and the third-order intermodulation are equal. In many circuits the IIP3 is beyond the allowed input range, thus the practical method to obtain the IIP3 is linear extrapolation on measured behavior for small input amplitude as shown in Fig. 4.2. In general, the IIP3 value is about 10 dB larger than the P1dB value for one stage circuit.

The IIP3 of a cascade system can expressed as [92]

$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \Lambda \tag{4.8}$$

where $IIP3_n$ and G_n are the IIP3 and power gain of the nth-stage, respectively.
For gains greater than one, the total receiver linearity is dominated by the linearity of latter stages. Thus, the linearity of the latter stages should be as large as possible to maximize the gain of the whole system.

As compared with (4.4) and (4.8), the power gain of first stage is increased to

reduce the *NF* of the total system. However, the linearity of the system is decreased due to the large gain of first stage. As a result, an adjustable or switched gain of first stage is designed to meet the *NF* and linearity.

The advanced CMOS technology is required for 60-GHz transceiver design. However, the power supply voltage is decreased as the minimum channel length of CMOS technology decreases. In other words, the system linearity becomes worse while using advanced CMOS technology.

4.1.3 Link Budget Analysis

Link budget analysis is an important design issue for wireless communication system [93]. A link budget is the accounting of all of the gains and losses from the transmitter, communication medium in a telecommunication system.

The free-space path loss (L_P) can be expressed as

$$L_P = 20\log\left(\frac{4\pi d}{\lambda}\right) \tag{4.9}$$

where d is the distance between transmitter and receiver and λ is the wave length of the carrier frequency.

It can be seen from (4.9) that the path loss is increased as the increase of carrier frequency. For 60-GHz wireless communication system, the path losses are 68 and 88 dB for the distance of 1 and 10 m, respectively.

The power level at the receiver input can be written as

$$P_r = P_t + G_t + G_r - L_P \tag{4.10}$$

where P_r is the power at the receiver input in dBm, P_t is the delivered power by the transmitter, and G_t and G_r are power gain of the transmitter and receiver antenna,

respectively.

Assume that the maximum transmit power at the transmitter output is 10 dBm, the antenna gain in the transmitter part is 9 dB, the shadowing loss is 10 dB, the receiver antenna gain is 9 dB, and the distance between receiver and transmitter is 1 m, the received power level at the receiver input is –50 dBm in a 60-GHz communication system.

From (4.6), the minimum power level that is detectable is –55.6 dBm if the modulation is QPSK with bit-error rate of 10^{-6} and the *NF* from receiver is 15 dB are assumed. Detail system parameter is listed in Table 4.1. In summary, the available margin for *SNR* is only 5.6 dB. If the distance between transmitter and receiver is increased to 10 m, the signal level can not be detectable. Therefore, the secure communication in 60-GHz band is provided by large signal path loss.

4.2 ARCHITECTURE AND OPERATIONAL PRINCIPLES

The proposed CMOS direct-conversion receiver front-end consisting of LNA, I/Q quadrature down-conversion mixers, 20-GHz QVCO, two ILFTs, two IFAs, and two output buffers is shown in Fig. 4.3. Because the quadrature LO signals are generated by the 20-GHz QVCO cascade with I/Q ILFTs, the symmetric layout floor plan is required for minimization of phase and magnitude error from the quadrature LO signals. In addition, due to the limited performance of active and passive devices at 60 GHz, it is easier to design high-performance QVCO at 20 GHz rather than at 60 GHz. Consequently, this approach can provide higher purity of the LO signals.

The RF input signal V_{RF} is amplified by the LNA. The I/Q down-conversion mixers are followed by the LNA. By mixing with LO signals provided by the ILFTs

and the QVCO, the frequency at mixer output is translated to zero-IF. The extra gain is given by the IFAs, and the output buffers are designed for test purposes to drive the 50-ohm loads.

According to the system design consideration for receiver front-end, the target specifications for the proposed 60-GHz direct-conversion receiver front-end are listed in table 4.2.

4.3 CIRCUIT REALIZATION

4.3.1 Low-noise amplifier

The key performance requirements of the 60-GHz LNA are power gain, noise figure, linearity, stability, impedance matching, power dissipation and bandwidth.

The circuit diagram of LNA consisting of two stage amplifiers is shown in Fig. 4.4. The first stage is implemented by a common-source (CS) amplifier with inductive source degeneration for minimum *NF* design consideration. The elements T_{LNA1}–T_{LNA3} and M_{LNA1} form the input matching network for matching to 50 ohm impedance from the antenna and achieve the better noise matching in the meantime [94]. The ac coupling capacitor between the two stages of the LNA can exhibit the signal amplitude divider, and the caused signal amplitude division would reduce the total voltage gain of the LNA. The effect of signal amplitude division can be minimized by using a large ac coupling capacitor. However, too large vertical metal-insulator-metal capacitor (MIMCap) suffers from large bottom-layer parasitic capacitor. Hence the M_{LNA2} is designed to generate a proper gate bias value of M_{LNA3} to avoid the usage of ac coupling capacitor. The selected value of C_{LNA2} is chosen as

large as possible to filter out the noise contribution from M_{LNA2}.

The second stage of LNA constructed by M_{LNA3}/M_{LNA4}, T_{LNA4}/T_{LNA5}, and C_{LNA3} is implemented as a cascode amplifier for high isolation capability between input and output to suppress the LO leakage to the antenna. In addition, the cascode transistor M_{LNA4} is used to reduce the Miller capacitance and to improve the stability. Because the pole frequency at the drain of M_{LNA3} on the order of $f_T/2$ [8] is lower than the desired frequency, it causes that both the noise contribution from M_{LNA4} and extra signal current leakage into ground can not be negligible. Shunt peaking inductor T_{LNA4} is applied to resonate with the total capacitances at the drain of M_{LNA3} [61]. Therefore, the effects from the pole at the drain of M_{LNA3} can be minimized. In addition, the noise contribution from M_{LNA4} can be also reduced by the increase of the impedance at the drain of M_{LNA3}.

Microstrip transmission lines are extensively used in this design for impedance matching, on-chip inductor, and bias networks. All transmission lines (T-lines) are kept as short as possible to minimize the signal loss and of mender structure to reduce the chip area. The characteristics of those T-lines are simulated by the 3D EM CAD tool High-Frequency Simulation Software (HFSS).

4.3.2 Down-conversion mixer

In the direct-conversion receiver architecture, high gain in the RF section is required to minimize the effect of flicker noise contributed from the IF section. Therefore, active mixer with the positive conversion gain is a better choice rather than passive mixer even though passive mixer can provide the capability of higher linearity and operate without dc power consumption [95]–[96].

The simplified schematic of down-conversion mixer in this design is shown in

Fig. 4.5 [97]. The input transconductance stage is composed of M_{MIX1}. Capacitor C_{MIX1} is designed to make the currents of the input stage and the switching stage consisting of M_{MIX2} and M_{MIX3} can be operated separately. Hence more current can be used for driving the input stage to increase the conversion gain of the mixer. The current through the switching stage controlled by the current sink I_{BIAS1} is selected for lower flicker noise contributed from M_{MIX2} and M_{MIX3} to the mixer output [98].

Owing to large parasitic capacitance at the drain of M_{MIX1}, the transmission line type inductor T_{MIX1} is chosen to resonate with the capacitance for gain improvement. The output loads are implemented by poly resistors R_{MIX1} and R_{MIX2} to avoid flicker noise. The ac coupling capacitor between LNA and down-conversion mixer is not required because the drain voltage of M_{MIX1} is close to supply voltage.

4.3.3 Quadrature voltage-controlled oscillator and injection-locked frequency triplers

The circuit diagram of the QVCO is shown in Fig. 4.6 [99]. The 20-GHz QVCO is composed of two mutually coupled identical VCOs marked by the dashed squares. Each VCO is made of a cross-coupled pair, M_{VCO1}/M_{VCO2} and M_{VCO3}/M_{VCO4}, to generate negative resistance to compensate the losses of *LC*-tanks. On-chip spiral inductors L_{VCO1}/L_{VCO2} with symmetric structure and accumulation mode MOS varators C_{VCO1}–C_{VCO4} with higher quality factor compared with pn-junction diode varactors are used in each VCO design. Poly resistors R_{VCO1} and R_{VCO2} are designed for proper bias condition of the VCO and the utilization of resistors instead of PMOS current sources are attributed to their free of flicker noise property. In final, transistors M_{VCO5}–M_{VCO8} form the even-stage ring oscillator to generate the quadrature phase outputs.

The output phases of QVCO are strongly dependent on the device matching performance in the even-stage ring oscillator. The simulated output phase imbalance with 10-% channel width mismatch of transistor in the even-stage ring oscillator is shown in Fig. 4.7. The phase imbalance of QVCO outputs are from 1.65° to 2.47° with the control voltage V_C from 0 to 1.2 V. Therefore, careful layout plan is important to reduce the phase imbalance effect from device process variations.

The circuit diagram of the ILFT used in the proposed direct-conversion receiver is shown in Fig. 4.8. According to the analysis in [25], the schematic of the ILFT can be divided into two stages for different purposes. The first stage is the frequency pre-generator stage and the second stage is the ILO stage. The input signal (I_{VCO}) from QVCO is injected into the frequency pre-generator stage, and function of frequency pre-generator that generates third-order harmonic of input injection signal is implemented by M_{ILFT1}/M_{ILFT2}. The proper gate bias value of M_{ILFT1}/M_{ILFT2} V_{BIAS} can maximize the conversion gain of frequency pre-generator for an increase in the locking range of the ILFT.

The tripled-frequency signal generated by frequency pre-generator is transmitted to the ILO stage formed by NMOS M_{ILFT3}/M_{ILFT4} and a symmetric spiral inductor L_{ILFT1}. The selected values of inductor L_{ILFT1} is chosen so that it can resonate with the capacitances at the drain of M_{ILFT3}/M_{ILFT4} at the third harmonic frequency of input frequency, respectively. M_{ILFT3} and M_{ILFT4} are used to generate negative conductance to cancel the loss of *LC*-tank. Resistor R_{ILFT1} is designed for improvement of the rejection ratios to undesired even-order harmonics [25].

As shown in [25], the normalized locking range of the ILFT can be expressed as

$$\frac{|\omega-\omega_r|}{\omega_r} \le \frac{1}{2Q}\sqrt{\frac{\left(a_3V_i^3\right)^2}{\left(4V_o\right)^2-\left(a_3V_i^3\right)^2}} \approx \frac{1}{2Q}\left|\frac{a_3V_i^3}{4V_o}\right| \tag{4.10}$$

where ω_r and Q are the resonant frequency and quality factor of the *LC*-tank in the output of the ILFT, respectively; the coefficient a_3 is the nonlinear characteristic property of third order term from frequency pre-generator; and V_i and V_o are the incident and output amplitude, respectively.

The expression of the output amplitude can be written as

$$V_o = \frac{a_3G_mH_0V_i^3\cos 3\theta}{4\left(1-G_mH_0\right)} \tag{4.11}$$

where G_m is the transconductance stage of the ILO, H_0 is the impedance of the *LC*-tank at their resonant frequency, and θ is the phase difference between input and output.

From (4.10), it can be seen that the locking range increases with an increase in either the absolute value of the coefficient a_3 in the frequency pre-generator nonlinear characteristic function or the incident amplitude V_i from QVCO. The quality factor degradation of the *LC*-tank can also improve the total locking range but it causes a decrease in the impedance of the *LC*-tank H_0. In general, the coefficient a_3 is proportional to the conversion gain of the third-harmonic frequency pre-generator.

A summary of the design flow of the ILFT in this design can be decided. The conversion gain of the frequency pre-generator and the incident amplitude from QVCO are maximized for the maximization of the locking range. To further increase the locking range of ILFT, it can trade off output voltage swing for large locking range via the quality factor degradation of *LC*-tank resonator as can be seen from (4.11). However, the latter approach causes the decrease in the conversion gain and the increase in the noise figure in the down-conversion mixer [100].

According to the previous design in Chapter 2, the locking range of ILFT is around 1.5 GHz with reasonable input power. The frequency range is smaller than the target frequency range of 6.48 GHz. Therefore, the increase of input amplitude from QVCO and the *LC*-tank quality factor degradation are designed to increase the locking range of the ILFT. Recently, the ILFT described in Chapter 2 has been demonstrated with 9-GHz locking range by increasing the dc power consumption and *LC*-tank quality factor degradation [23].

4.3.4 IF Amplifiers and Output Buffers

The circuit diagram of IF amplifiers and output buffers for I-channel is shown in Fig. 4.9. IF amplifiers are implemented by two differential CS amplifier pairs with passive poly-resistors as the loads for smaller flicker noise. The extra gain from IF amplifiers are designed to suppress the noise contribution from output buffers. Additionally, because of the large parasitic capacitor from output buffers, IF amplifiers are designed to avoid mixer driving output buffers directly. The bandwidth in the IF section is, therefore, increased. Finally, the unity-gain open-drain buffer is used for output buffer to drive 50-ohm instrumentation.

4.3.5 Overall Circuits

The overall circuit of the proposed direct-conversion receiver is shown in Fig. 4.10 where the output buffer is not drawn. The device parameters of the whole receiver are listed in Table 4.2.

The RF input signal V_{RF} is applied to the input nodes of the LNA. The LNA amplifies the RF signal to provide reasonable gain to suppress the noise contribution from the subsequent stages. The LNA output is connected to I/Q down-conversion mixers. By mixing with LO signals (LO_I and LO_Q) provided by the ILFTs and the

QVCO, the frequency at mixer output is translated to zero-IF. The extra gain is given by the IFAs, and the output buffers are designed for test purposes to drive the 50-ohm loads.

LO signals (LO_I and LO_Q) are generated by I/Q ILFTs by taking the third-order harmonic frequency of QVCO output. The performance of ILFTs outputs are, therefore, determined by the performance of QVCO. To get the better QVCO performance, the ratio of better ratio of the cross-couple pairs (M_{VCO1}–M_{VCO4}) and ring oscillator (M_{VCO5}–M_{VCO8}) is chosen [101].

4.4 EXPERIMENTAL RESULTS

The proposed 60-GHz direct-conversion receiver front-end is designed and fabricated using 0.13-μm 1P8M Cu CMOS technology with ultra thick metal of 3.3 μm. The chip microphotograph of the proposed direct-conversion receiver is shown in Fig. 4.11; the chip area including all the test pads and dummy metals is 1.21 mm × 1.03 mm. An on-wafer measurement system incorporating a probe station, GSG coplanar probes, GSGSG differential coplanar probes, high-speed cables is used to measure chip performance. The measurement setup for 60-GHz direct-conversion chip testing is shown in Fig. 4.12.

The total power dissipation of the fabricated direct-conversion receiver is 31.0 mW under a 1.2-V supply voltage. The simulated and measured input return loss (S11) at the RF port with the frequency range from 54 to 66 GHz is shown in Fig. 4.13. It can be seen from Fig. 4.13 that the measured S11 is lower than –10 dB as RF frequency is close to 60 GHz. The measured S11 is better than –8 dB with the frequency range from 57 to 66 GHz.

The measured output frequency of QVCO versus control voltage V_C from 0 to 1.2 V is measured by the observation of the QVCO leakage from IF port. It can be seen from Fig. 4.14 that the measured QVCO output frequency is shifted to lower frequency around 2.5-GHz as compared with the simulated results. Because the model of the two-turn symmetric inductor is calculated by the interpolation from one-turn and three-turn symmetric inductors, the accuracy of the interpolation method is verified by the 3D EM CAD tool HFSS. The 3D-view of the inductors and interconnection metals are shown in Fig. 4.15. All active devices are removed and replaced as a grounded metal. The HFSS EM simulation and measurement results of QVCO output frequency versus control voltage V_C from 0 to 1.2 V are shown in Fig. 4.16. The whole EM simulation result can be closer to measurement result with frequency offset around 1 GHz. The 1-GHz frequency offset can be explained as the process variations.

The simulated and measured whole receiver power gain and single-side band (SSB) *NF* with RF frequency range of 51.5 GHz to 55.03 GHz and inter-mediate (IF) frequency of 100 MHz are shown in Fig. 4.17. Due to modeling inaccuracies of the inductor and transmission line characteristic and possibly transistor capacitances from QVCO, the measured frequency range is not the same as expected frequency range. The maximum receiver power gain is 18.2 dB and the minimum SSB *NF* is 16.96 dB at 55.03-GHz RF frequency. The measured RF frequency range is limited by the tuning range of QVCO.

The measured 3-dB channel bandwidth with fixed LO frequency of 55.02 GHz is shown in Fig. 4.18. The measured channel bandwidth of 2 GHz is achieved for high-speed data transmission. In addition, the measured bandwidth is only 160 MHz smaller than the possible specifications for full-rate data transmission shown in

Chapter 1. The asymmetric frequency response can be explained that the magnitude response of LNA is asymmetric. Thus, the power gain provided by LNA is larger at higher frequency.

The linearity performance of the proposed receiver is shown in Figs. 4.19 and 4.20. The measured input-referred 1-dB compression point (P1dB) is about –17.0 dBm with RF frequency of 55.03 GHz and IF frequency of 100 MHz. The two tone test for the input third order inter-modulation intercept point (IIP3) with the RF frequency of 55.04 and 55.03 GHz is also measured. The measured IIP3 is around –7.6 dBm as can be seen from Fig. 4.20.

The output waveforms of I- and Q- channel IF signals are measured by real-time oscilloscope. The output waveforms with IF frequencies of 500 MHz, 100 MHz, and 50 MHz are shown in Fig. 4.21, 4.22, and 4.23, respectively. The amplitude and phase imbalance between I- and Q- channels at 100-MHz IF frequency are around 1.58 dB and 17°, respectively.

The amplitude imbalance of I- and O-channel can be minimized by using an automatic gain control (AGC) circuits. However, the effect of phase imbalance can not be reduced by using extra calibration circuits. The signal constellations of QPSK with ideal I/Q phase and non-ideal I/Q phase are shown in Figs. 4.24 (a) and (b), respectively. In Fig. 4.24 (a), ideal I- and Q-channel are performed. The BER P_{E1} is calculated by using a normal distribution function. In Fig. 4.24 (b), a phase imbalance is existed and the BER P_{E2} is larger than ideal case P_{E1} in Fig. 4.24 (a). In order to maintain the required BER in digital section, the minimum required *SNR* at the baseband should be increased. Therefore, the sensitivity of whole receiver system is decreased.

To further discuss the phase mismatches of IF signals, the QVCO output phase imbalance versus control voltage V_C from –0.2 to 1.4 V is shown in Fig. 4.25 where the model for passive inductors and interconnection metals are simulated from Fig. 4.15 and the phase imbalance is defined as the phase difference between I- and Q-channel output. It can be seen from Fig. 4.25 that phase imbalance is introduced by asymmetric two-turn inductors and interconnection metals. However, the asymmetric performance of inductors can not be found from HSPICE models. The phase mismatch is from –0.57° to 3.44° with the control voltage V_C from –0.2 to 1.4 V. Therefore, the phase imbalance at the output of ILFTs is –1.71° to 10.32°. These values are close to the measurement results.

Because the control voltage V_C is not controlled by a close-loop phase-locked loop, the control voltage node is directly fed by a power supply. The measured VCO gain is very large, 5000 MHz/Volt. It is very difficult to measure the IF signal with frequency lower than 1 MHz as the dc output of a power supply is not very clear. Therefore, the performances of dc offset and flicker noise cannot be measured in the current receiver version.

Finally, the single carrier modulation scheme is specified in the 60-GHz communication system. The distance between each carrier is 2160 MHz which is larger then required IF bandwidth. Thus, second-order input intercept point (IIP2) is not measured.

In Table 4.3, the recently published CMOS receivers worked at the *V*-band are compared with the proposed receiver. It can be seen that the proposed receiver can be operated with lower dc power consumption and small chip area. In [102], QVCO and Q-path modulator are not included so its chip area and power consumption is small. Additionally, the proposed receiver can provide an IF bandwidth of 1 GHz that is

close to the specification frequency plan. The proposed receiver provides a high-integration and low power choice for 60-GHz receiver design. The NF is highest because the gain which is provided by LNA is not large enough. Probably RF frequency is not in the LNA bandwidth. In summary, the main drawback of the proposed receiver is large NF as compared with receiver integrated with conventional frequency multiplier. However, high *NF* problem can be solved by increasing the gain of LNA. This design is the first CMOS receiver integrated with the ILFTs in the millimeter-wave band.

4.5 SUMMARY

The 60-GHz direct-conversion receiver front-end integrated with ILFTs is designed, fabricated, and measured. Because the output frequency of QVCO is shift to 18.3-GHz, the maximum operational frequency of the direct-conversion receiver is only 55-GHz. The reason of frequency offset is verified by 3-D EM simulator HFSS. The modeling inaccuracies of the inductors and transmission lines characteristics are main reasons for the output frequency shift. Thus, the measured RF frequencies are not the same as expected frequency range.

In addition, the phase imbalance of I- and Q-channel outputs is discussed due to the asymmetric two-turn inductors and interconnection metals. Because I/Q ILFTs are designed after QVCO, the phase imbalance from QVCO is amplified three-times at the ILFTs outputs. Therefore, the phase mismatch is large at the IF outputs. The solution to phase mismatch is to add a ring oscillator between I/Q ILFTs [23]. The ILFTs output phases can be forced to quadrature phase by the additional ring oscillator. The phase imbalance can be also reduced by using careful layout for

QVCO.

Finally, because the rejection ability to fundamental signal is around 20 dB in the post-simulation of IFLT, the 20-GHz signal from ILFT is also injected into switching stage of mixer. Due to the nonlinear characteristic of switching stage, the RF signal is also translated to IF section by mixing with 20 GHz signal. The *NF* is increased by the undesired signal. In the post-simulation results, the 20-GHz signal at the switching stage input is very small. The nonlinear characteristic generated by the signal can be neglected. Therefore, the effects of undesired harmonics in the ILFT output are not important as a direct-conversion receiver integrated with ILFT.

Table 4.1

Link budget analysis for 60-GHz wireless communication.

	Specifications	Running Results	
TX Output Power	10 dBm	10 dBm	
TX Antenna Gain	9 dB	10 + 9 = 19 dBm	
Path Loss	-68 dB	19 - 68 = -49 dBm	1 m
Shadowing Loss	-10 dB	-49 -10 = -59 dBm	Received Power Level
RX Antenna Gain	9 dB	-59 + 9 = -50 dBm	
Background Noise	-174 dBm/Hz		
Noise BW	92.4 dB	-81.6 dBm (Noise)	1728-MHz Channel BW
Receiver NF	15 dB	-81.6 +15 = -66.6 dBm	
SNR required for Digital	11 dB	-66.6 + 11 = -55.6 dBm	QPSK and BER = 10^{-6}
System Margin		-50 - (-55.6) = 5.6 dB	

Table 4.2

Design target of receiver front-end.

Building Blocks		Target Specifications
Receiver Front-end	Freq. Range	57 – 64 GHz
	Power Gain	> 20 dB
	SSB NF	< 12 dB
	P1dB	> - 40 dBm
	IF Bandwidth	> 1080 MHz
LNA	Power Gain	12 dB
	NF	5 dB
	P1dB	> -40 dBm
Down Conversion Mixer	Power Gain	6 dB
	NF	20 dB
	P1dB	> -25 dBm
IF Amplifier	Power Gain	6 dB
	NF	< 10 dB
	P1dB	> -10 dBm

Table 4.3

Dimensions of devices in 60-GHz direct-conversion receiver.

Low-Noise Amplifier (LNA)	
Device	Dimension
M_{LNA1}	(1.2 μm / 0.13 μm)× 8
M_{LNA2}	(3.7 μm / 0.3 μm)× 5
M_{LNA3}	(1.2 μm / 0.13 μm)× 12
M_{LNA4}	(1.2 μm / 0.13 μm)× 14
C_{LNA1}	211.0 fF
C_{LNA2}	125.3 pF
C_{LNA3}	50.1 pF
T_{LNA1}	172.5 pH
T_{LNA2}	98.0 pH
T_{LNA3}	138.7 pH
T_{LNA4}	198.3 pH
T_{LNA5}	120.4 pH

I/Q Mixers	
Device	Dimension
M_{MIX1}	(1.2 μm / 0.13 μm)× 6
M_{MIX2} / M_{MIX3}	(1.5 μm / 0.13 μm)× 8
M_{MIX4}	(1.2 μm / 0.13 μm)× 6
M_{MIX5} / M_{MIX6}	(1.5 μm / 0.18 μm)× 8
C_{MIX1} / C_{MIX2}	47.9 fF
T_{MIX1} / T_{MIX2}	198.3 pH
R_{MIX1} – R_{MIX4}	1857.8 Ω

Quadrature Voltage-Controlled Oscillator (QVCO)	
Device	Dimension
M_{VCO1} - M_{VCO4}	(1.2 μm / 0.13 μm)× 6
M_{VCO5} - M_{VCO8}	(1.5 μm / 0.13 μm)× 2
C_{VCO1} – C_{VCO4}	(0.75 μm / 0.4 μm)× 26
L_{VCO1} / L_{VCO2}	Metal width = 9 μm Radius = 39 μm Turn = 2
R_{VCO1} / R_{VCO2}	224.4 Ω

I/Q Injection-Locked Frequency Triplers (I/Q ILFTs)	
Device	Dimension
M_{ILFT1} / M_{ILFT2}	(1.5 μm / 0.13 μm)× 12
M_{ILFT3} / M_{ILFT4}	(1.5 μm / 0.13 μm)× 6
M_{ILFT5} / M_{ILFT6}	(1.5 μm / 0.13 μm)× 12
M_{ILFT7} / M_{ILFT8}	(1.5 μm / 0.13 μm)× 6
L_{ILFT1} / L_{ILFT2}	Metal width = 9 μm Radius = 37.5 μm Turn = 1
R_{ILFT1} / R_{ILFT2}	46.1 Ω

IF Amplifier (IFA)	
Device	Dimension
M_{IFA1} - M_{IFA4}	(1.2 μm / 0.13 μm)× 4
R_{IFA1} - R_{IFA4}	796.2 Ω

Table 4.4

Comparison with Recently published *V*-band CMOS receivers.

	This Work	[18]	[102]	Target Spec.
Receiver Structure	Homodyne Receiver with ILFTs and I/Q modulators	Heterodyne Receiver with Freq. doubler	Homodyne Receiver with Freq. tripler and external LO	
Frequency (GHz)	55	57 – 63	53 – 60	57 – 64
Technology	130-nm CMOS	130-nm CMOS	130-nm CMOS	
Receiver Gain (dB)	18.2	11.8	16.4 – 19.4	> 20
NF (dB)	16.96	10.4	10.2 – 13.0	< 15
P1dB (dBm)	-17.0	-15.8	-20.0	> -40
IIP3 (dBm)	-7.6	N/A	-8.5	
IF BW (MHz)	1000	N/A	650	> 1080
Power Consumption (mW)	31.0	76.8	18.96	
Supply Voltage (Volt)	1.2	1.2	1.2	
Chip Area (mm^2)	1.25	3.8	0.63	

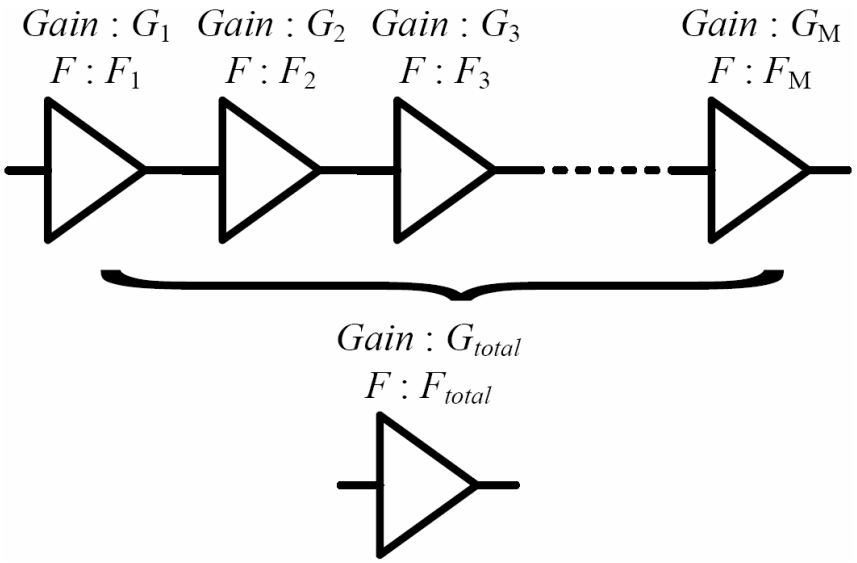


Fig. 4.1 The equivalent system for multi-stage system.

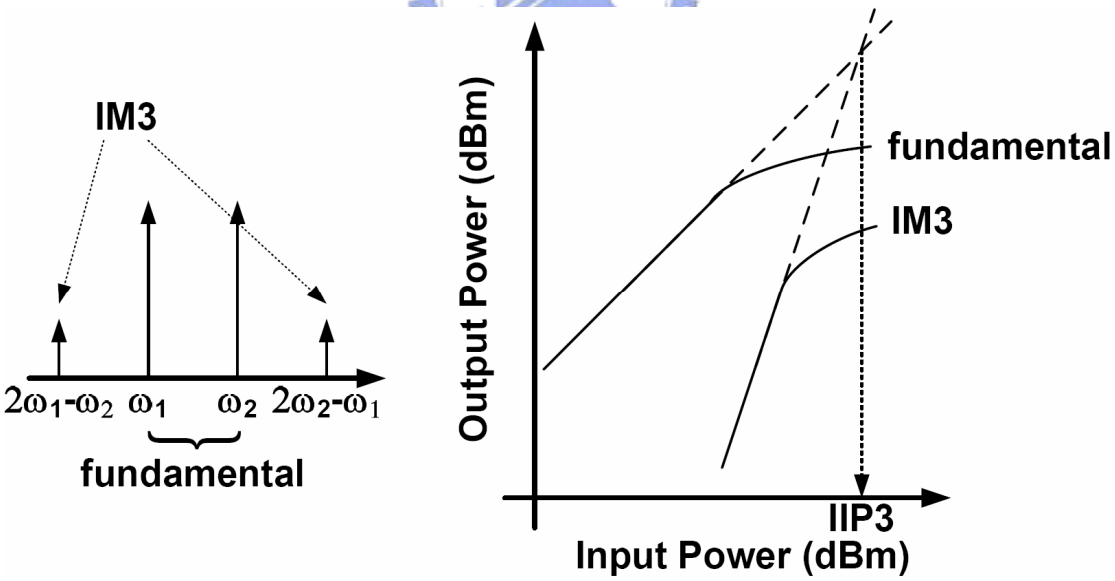


Fig. 4.2 The property and definition of IIP3.

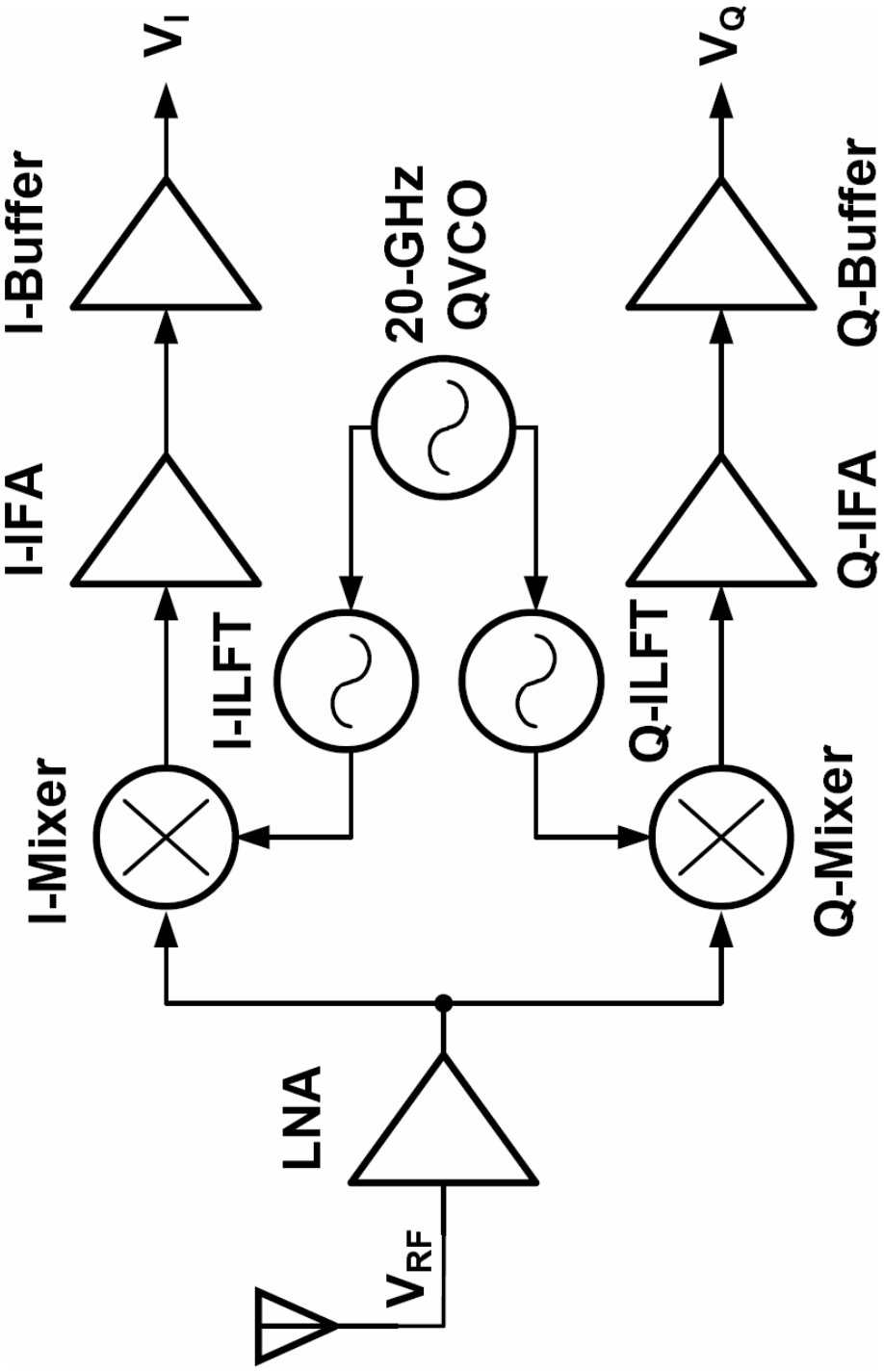


Fig. 4.3 Block diagram of the proposed direct-conversion receiver.

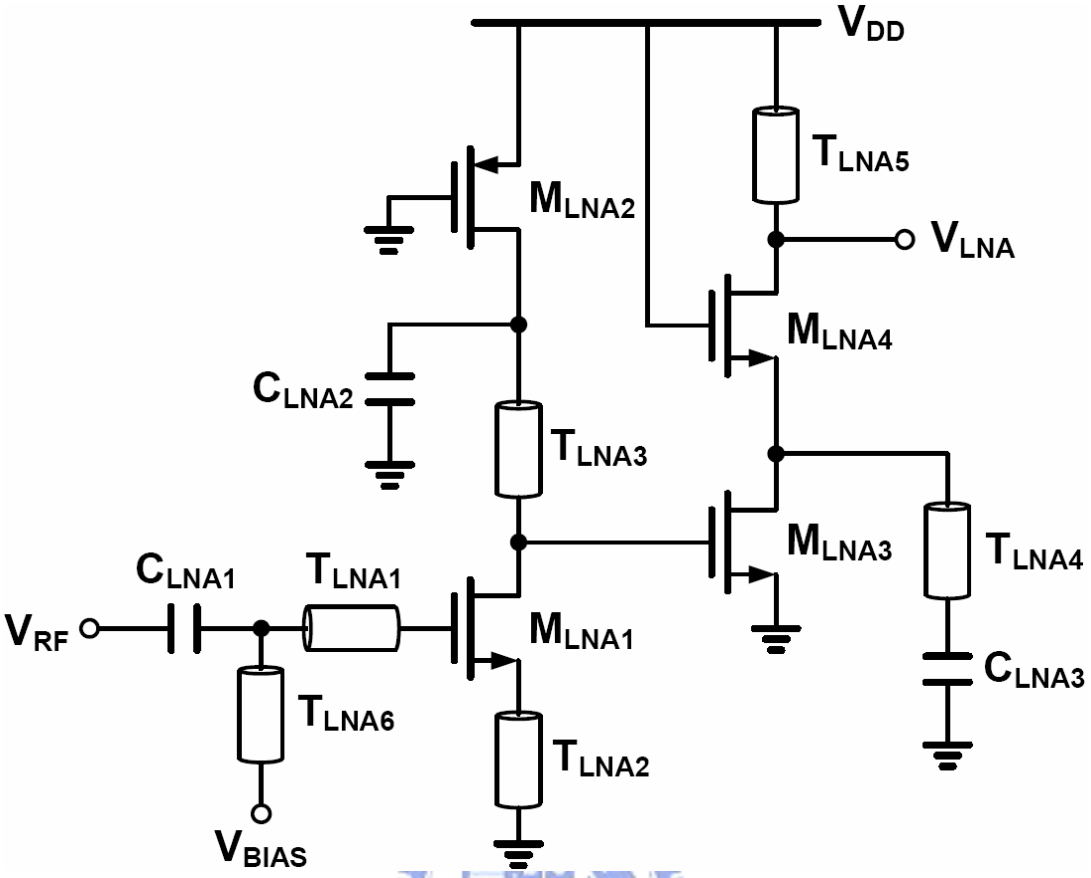


Fig. 4.4 Circuit diagram of the two-stage 60-GHz LNA.

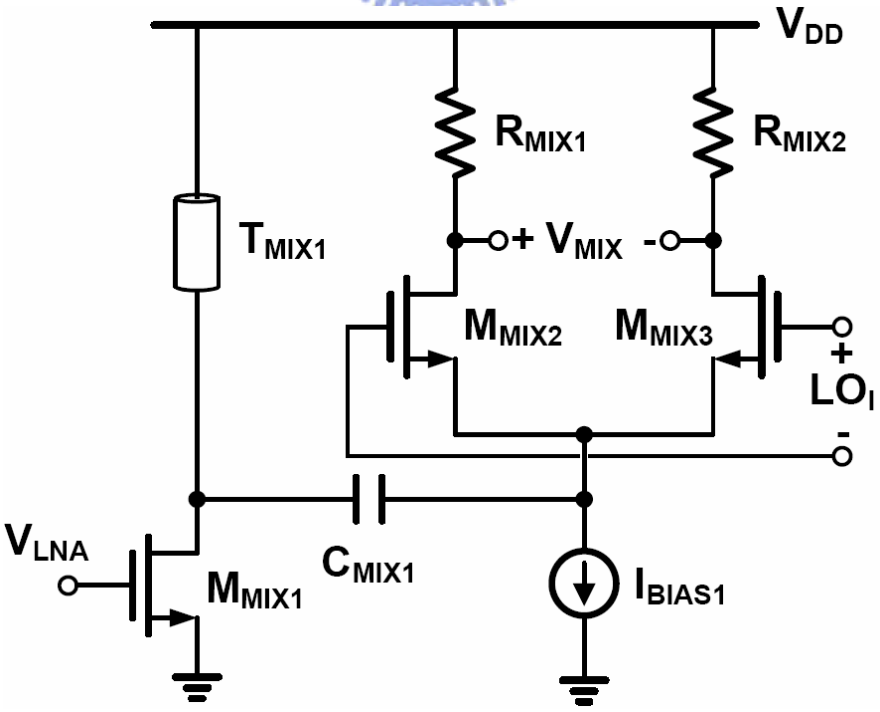


Fig. 4.5 Simplified schematic of down-conversion mixer.

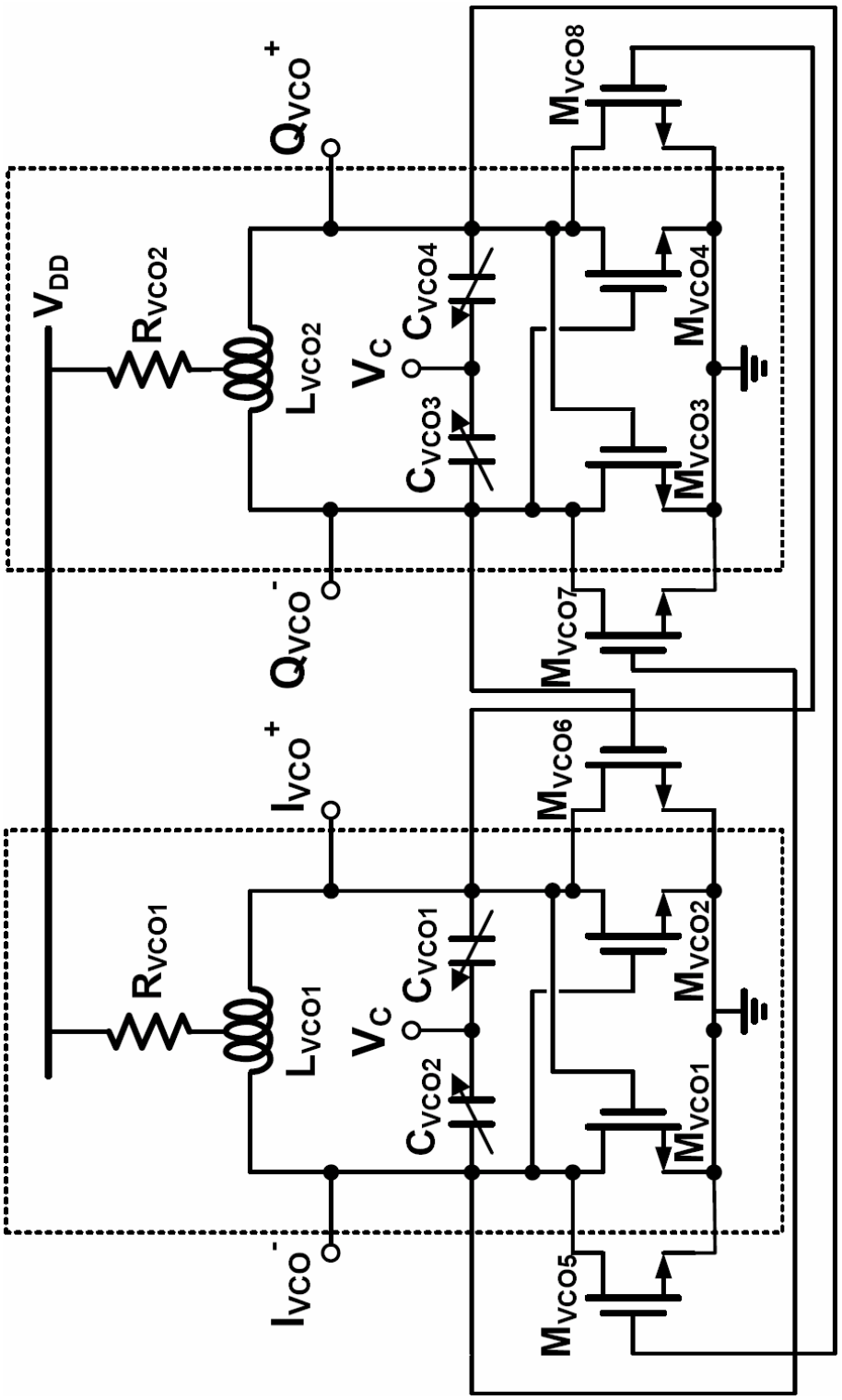


Fig. 4.6 Circuit diagram of the QVCO.

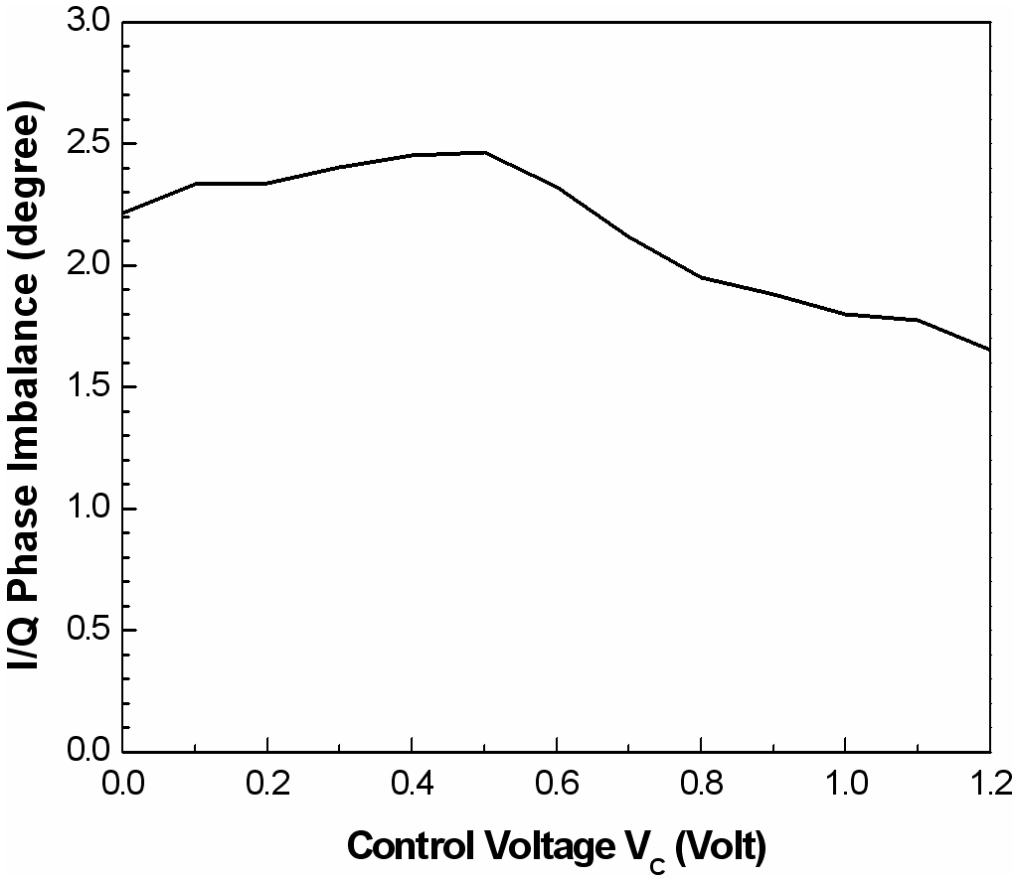


Fig. 4.7 Simulated I/Q phase imbalance with 10-% channel width mismatch of the transistor in the even-stage ring oscillator.

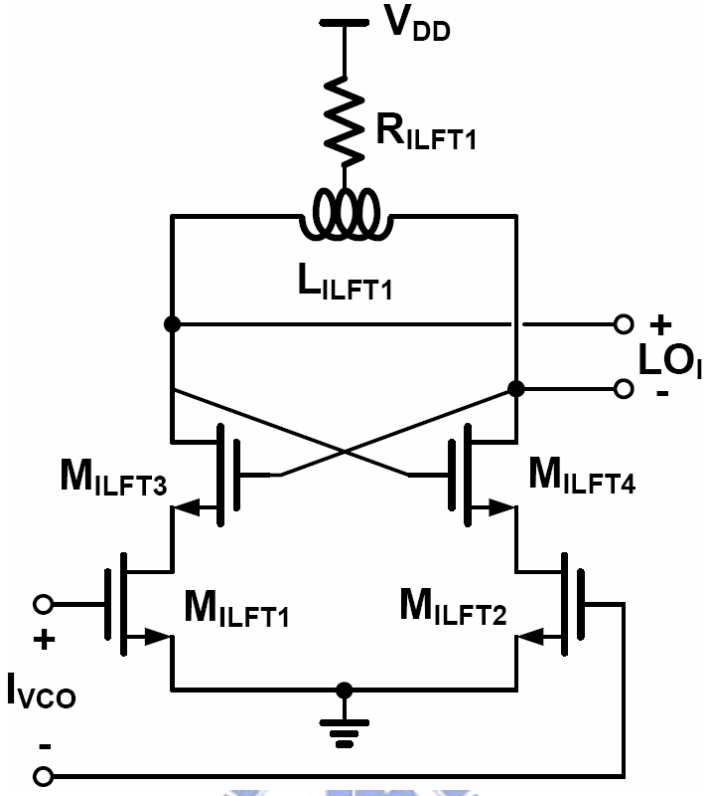


Fig. 4.8 Circuit diagram of the ILFT.

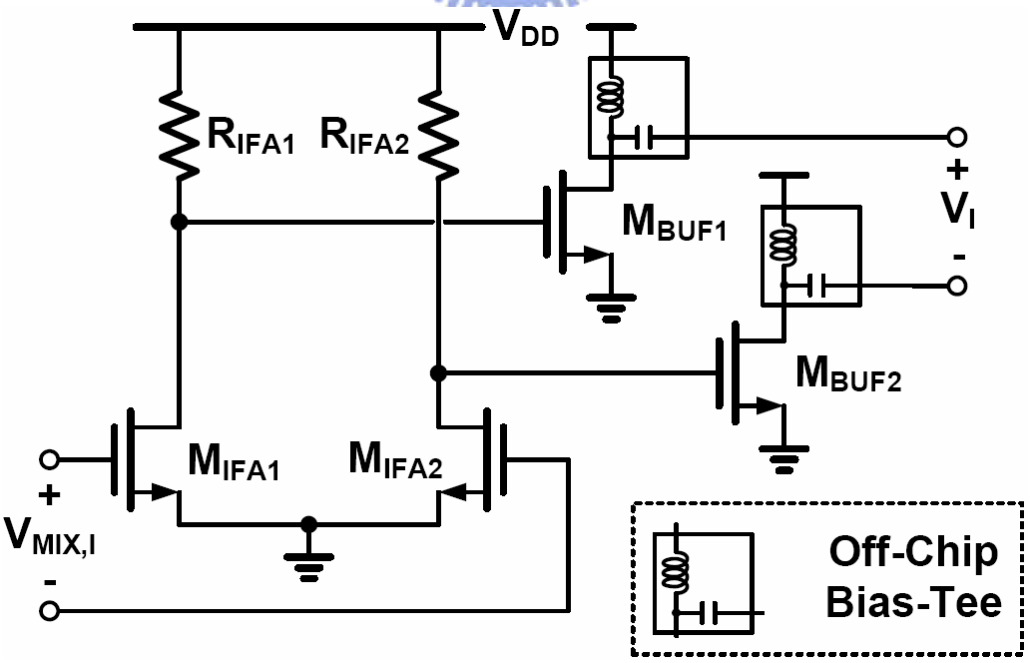


Fig. 4.9 Circuit diagram of the IF amplifiers and output buffers for I-channel.

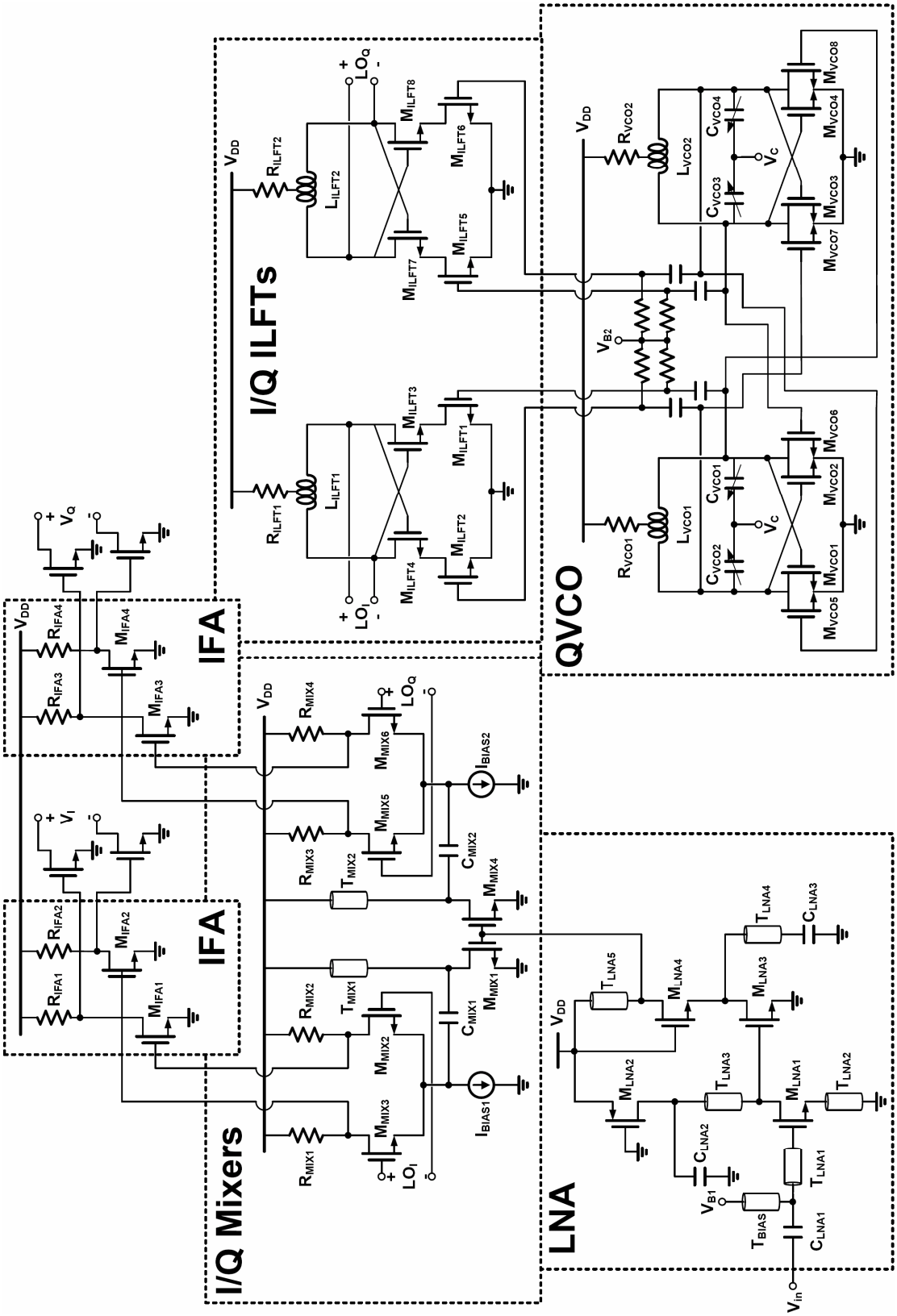


Fig. 4.10 Complete circuit diagram of the proposed 60-GHz direct-conversion receiver.

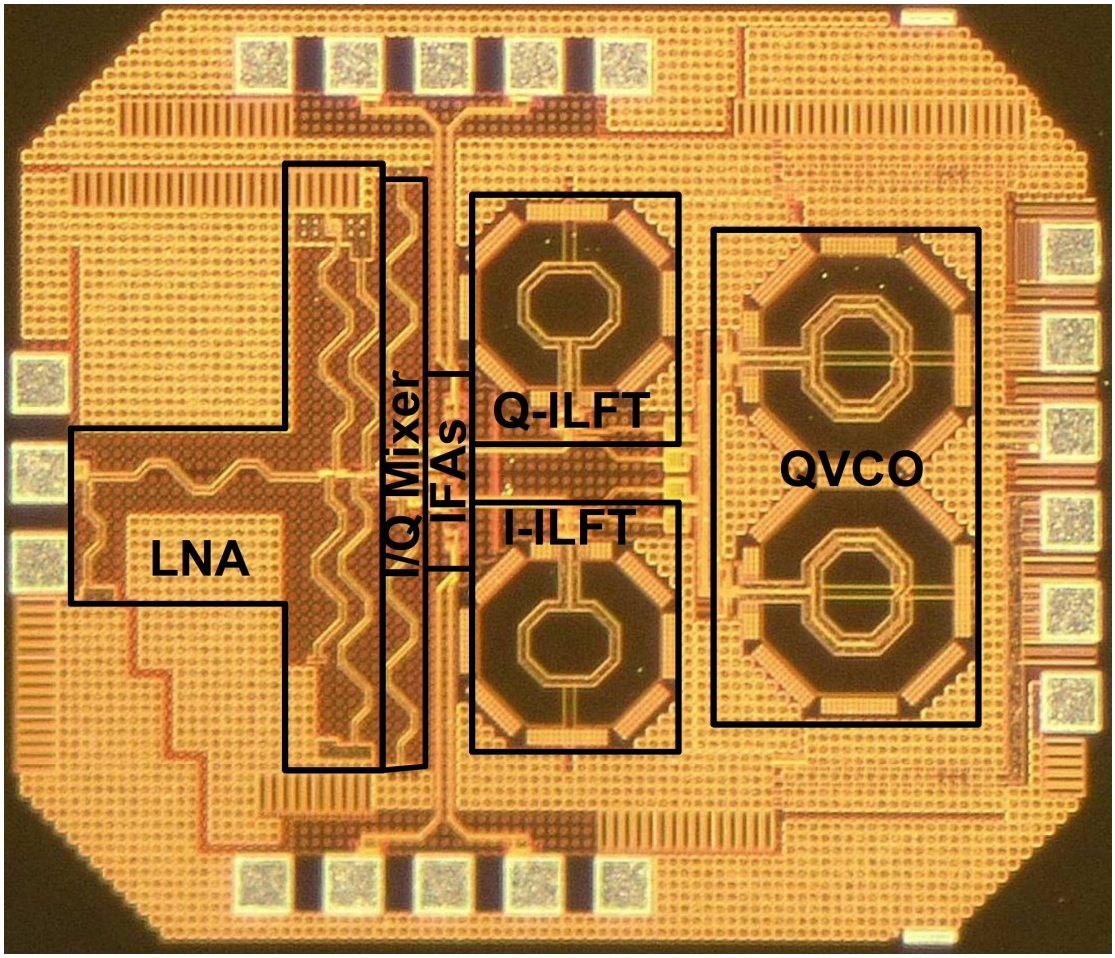


Fig. 4.11 Chip microphotograph of the 60-GHz direct-conversion receiver (1.21 mm × 1.03 mm).

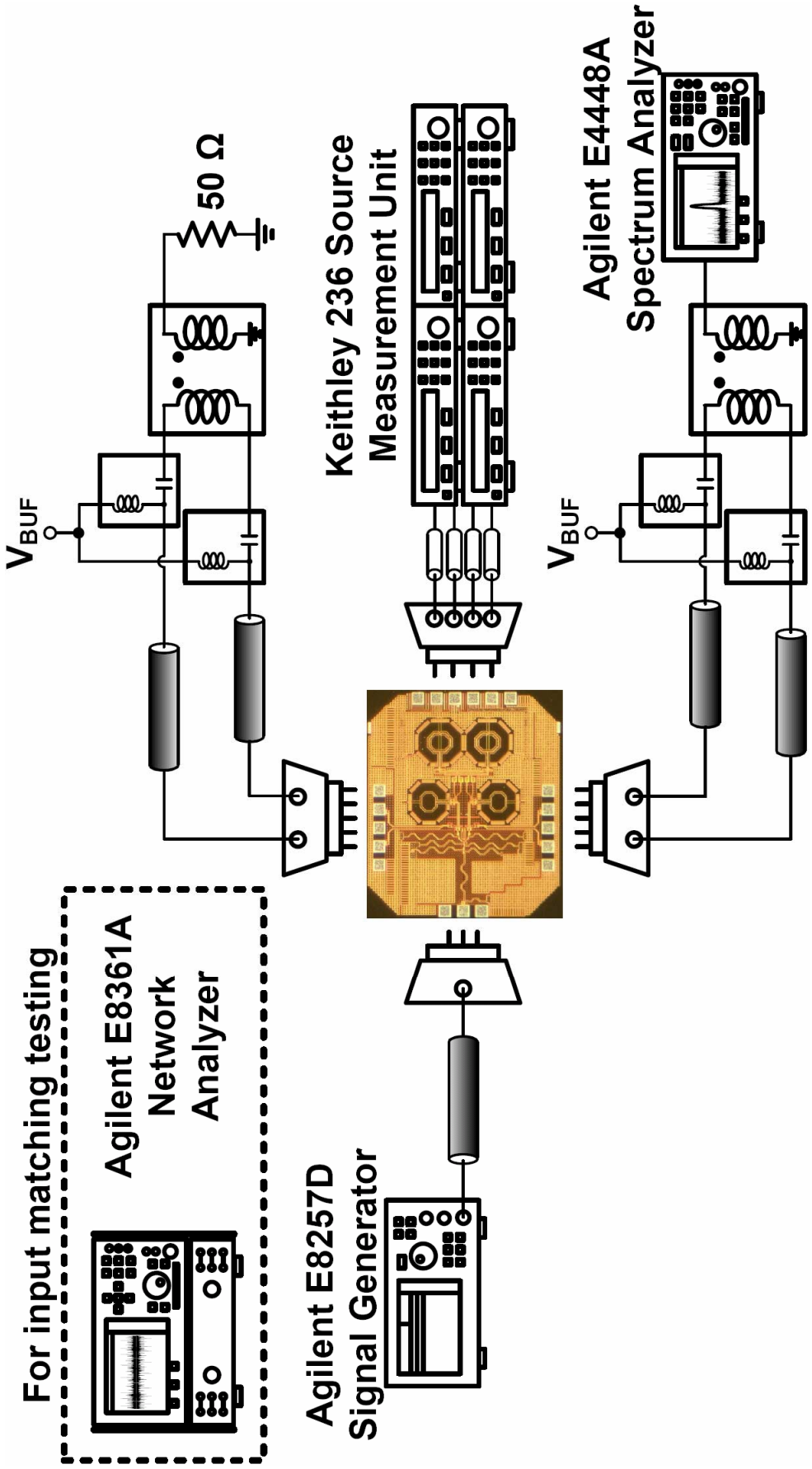


Fig. 4.12 Measurement setup for 60-GHz direct-conversion receiver testing.

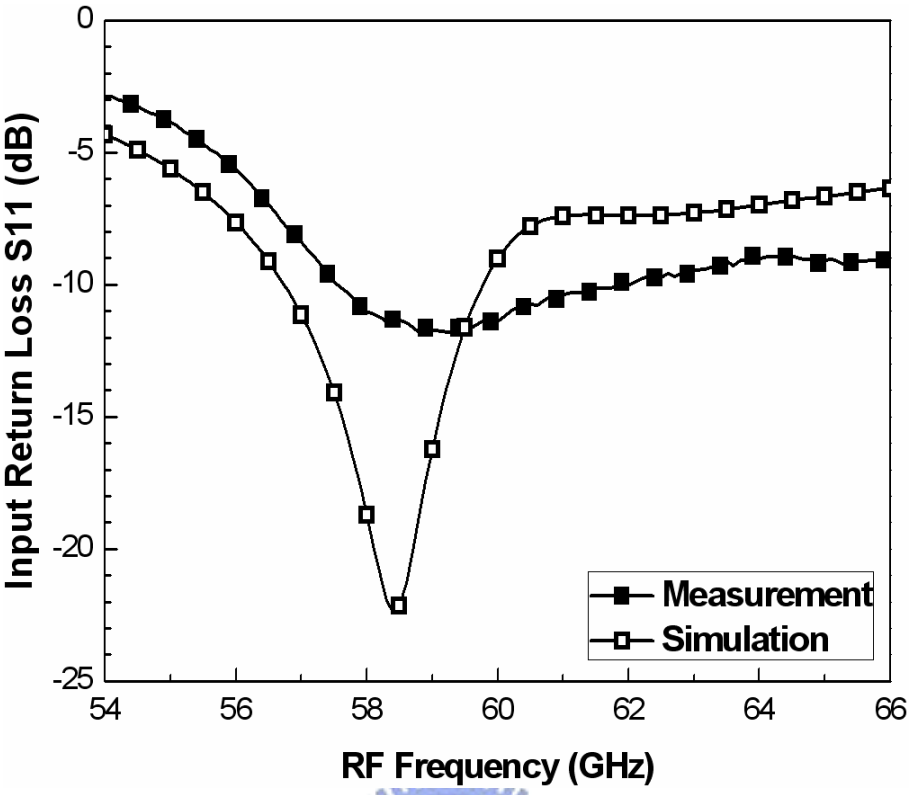


Fig. 4.13 Simulated and measured input matching (S11) with frequency range from 54 to 66 GHz.

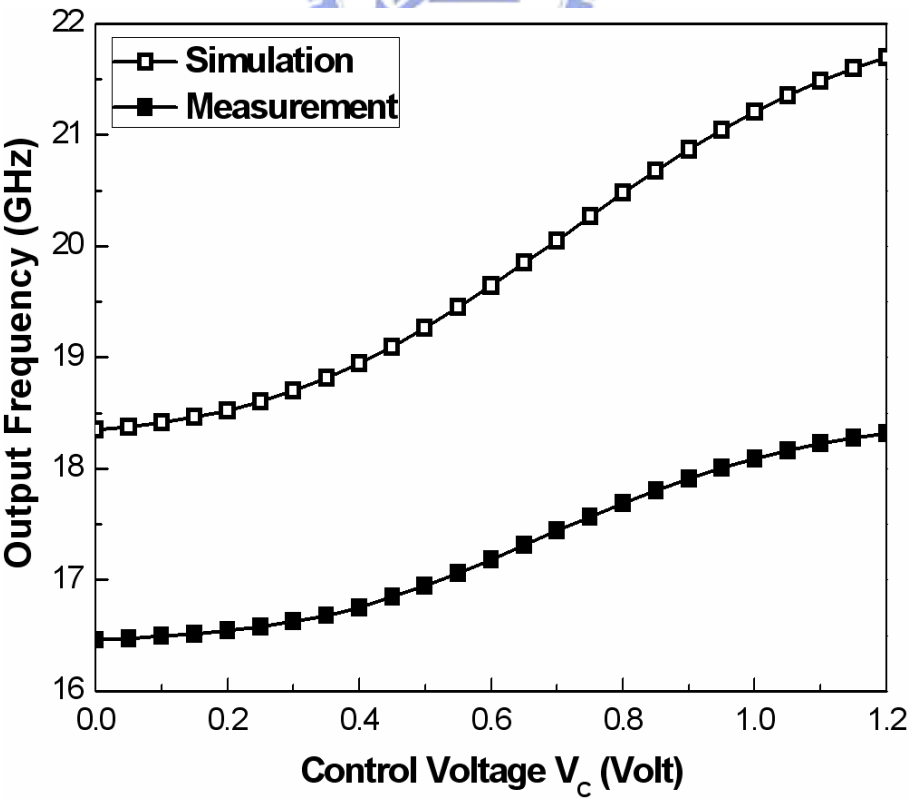


Fig. 4.14 Simulated and measured QVCO output frequency versus control voltage V_C.

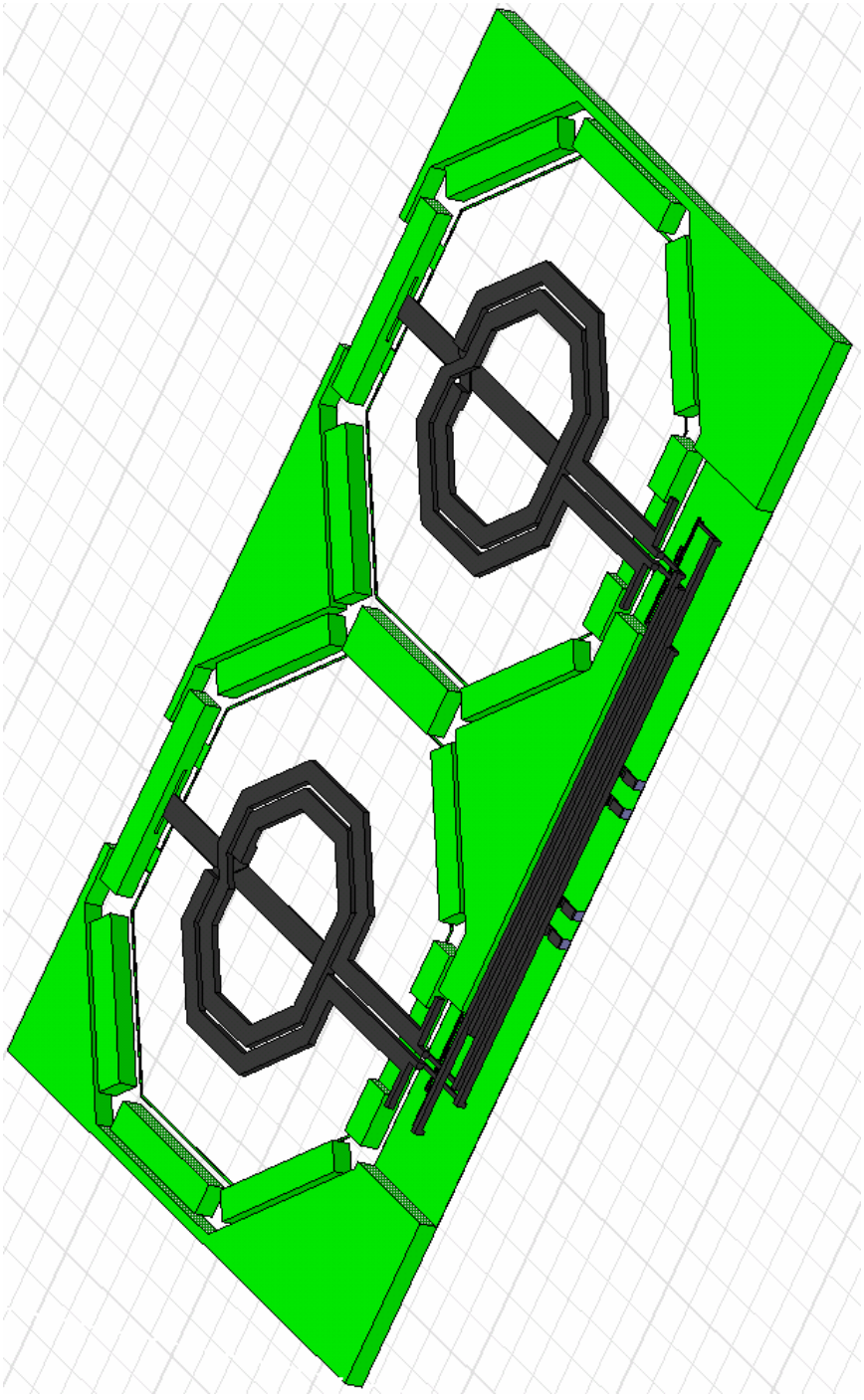


Fig. 4.15 3D-view of the inductors and interconnection metals for EM simulation.

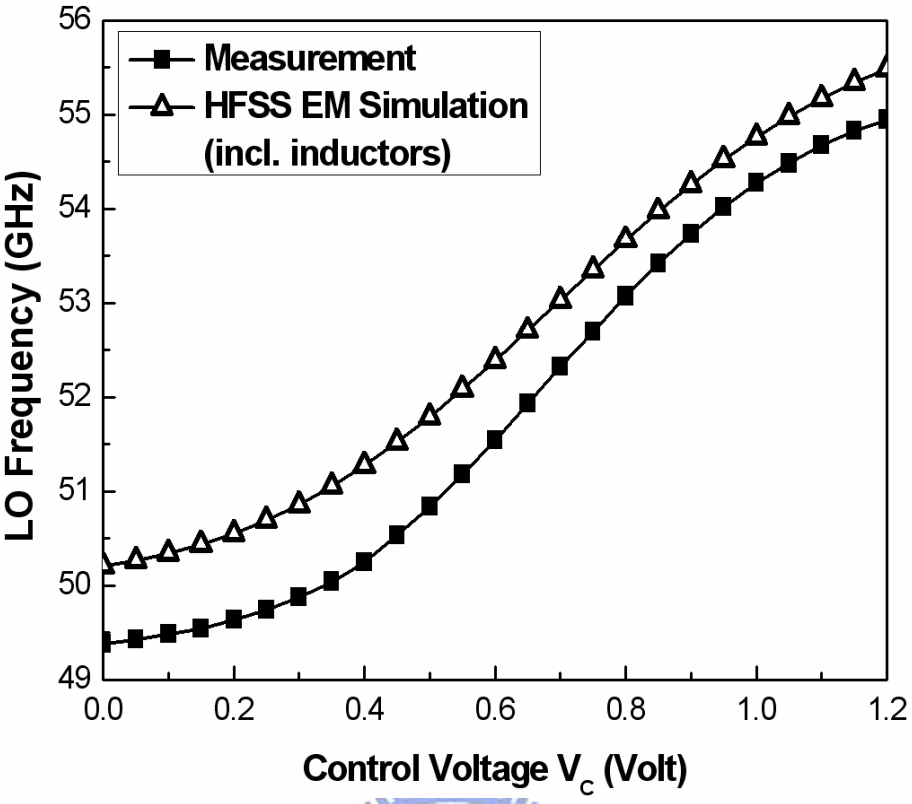


Fig. 4.16 Measured and EM simulated LO frequency versus control voltage V_C.

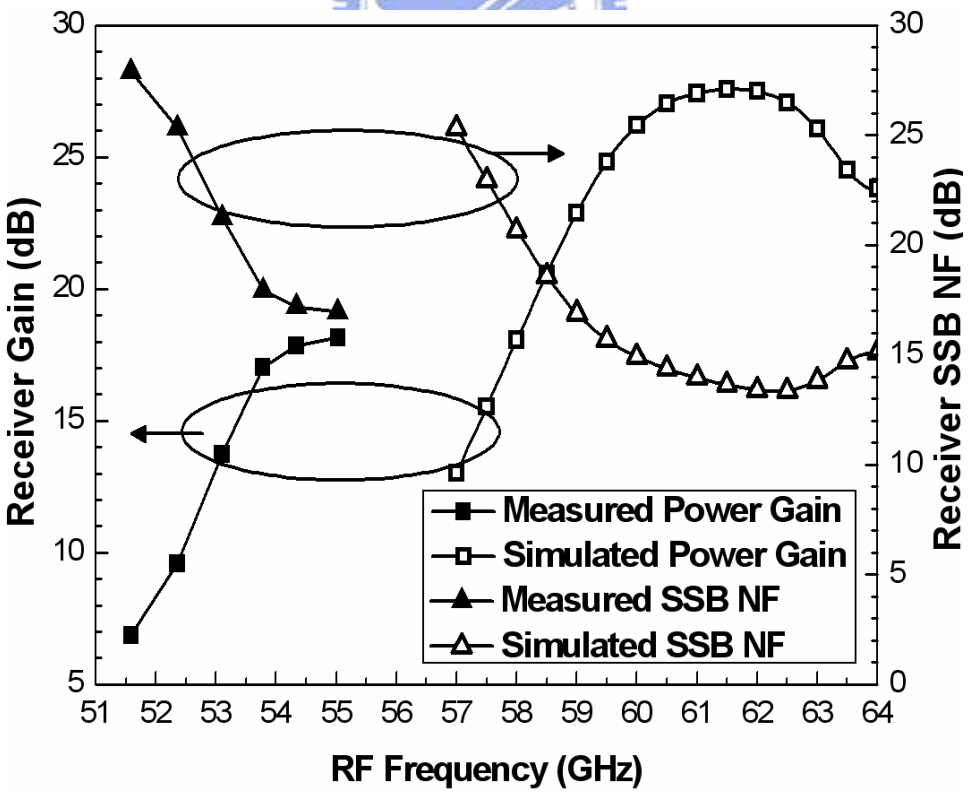


Fig. 4.17 Simulated and measured receiver gain and SSB *NF* with IF frequency of 100 MHz.

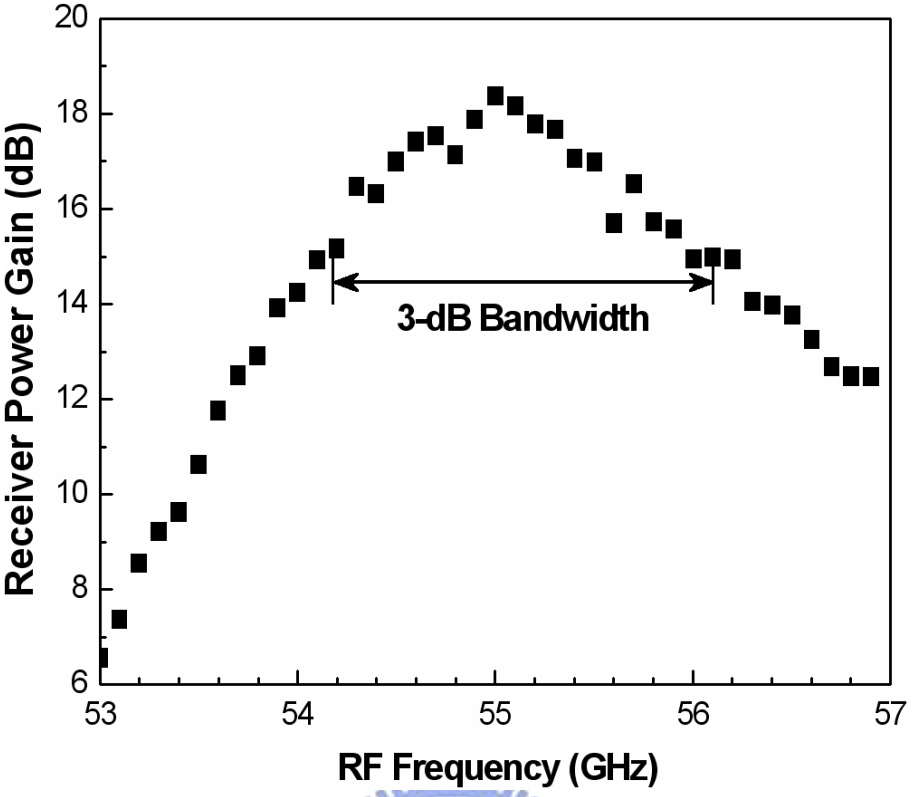


Fig. 4.18 Measured 3-dB channel bandwidth with LO frequency of 55.02 GHz.

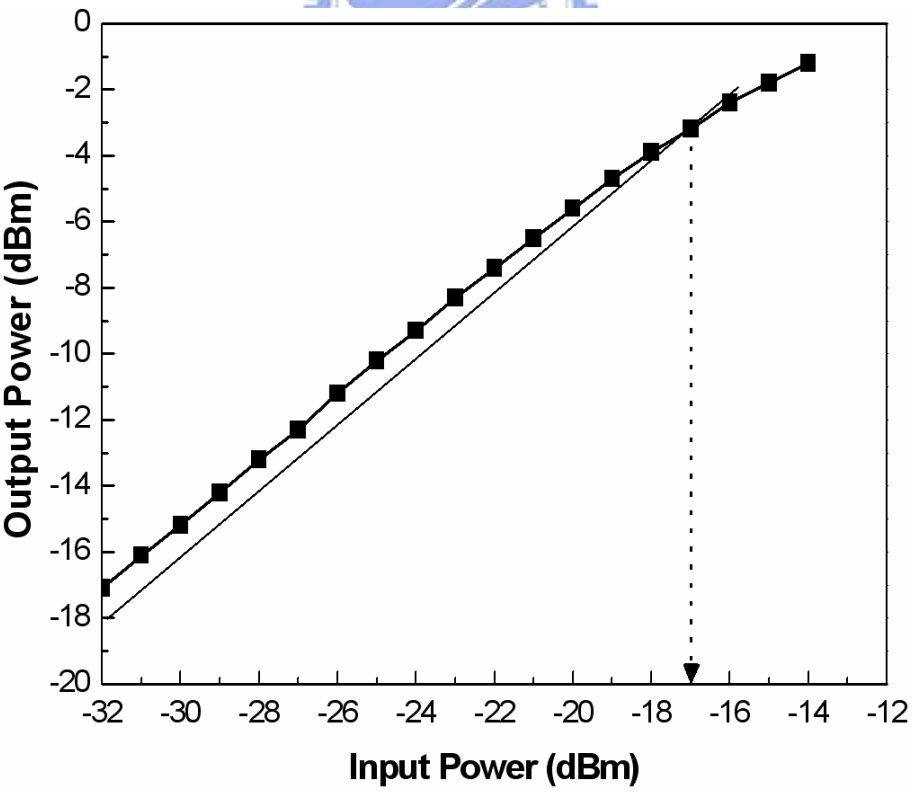


Fig. 4.19 Measured P1dB with RF frequency of 55.03 GHz and IF frequency of 100 MHz.

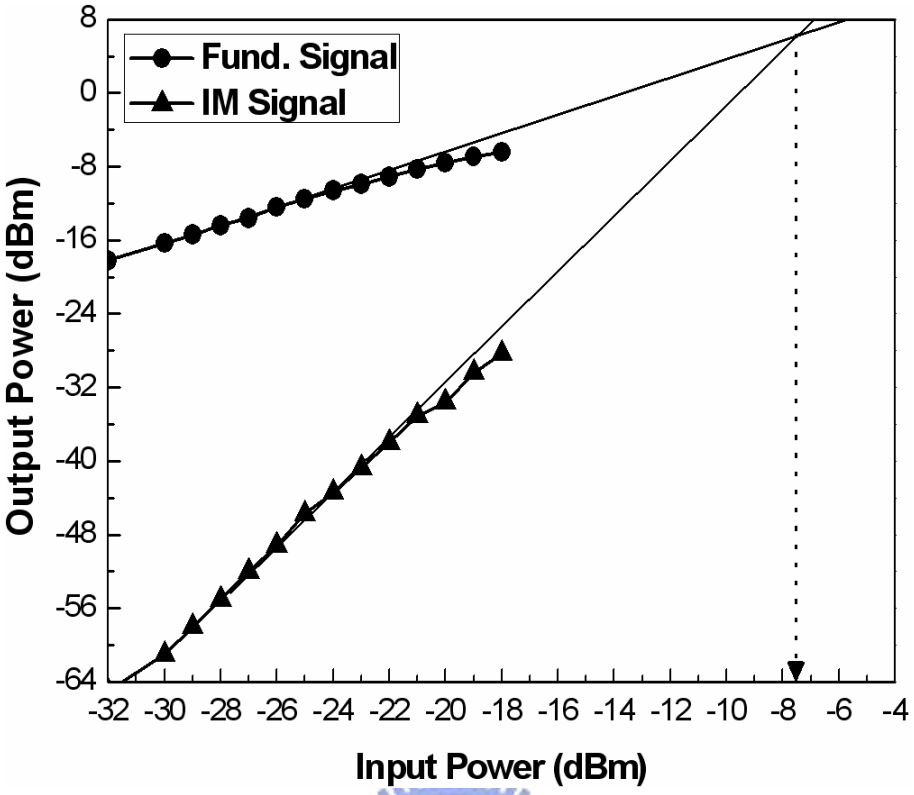


Fig. 4.20 Measured IIP3 with RF frequency of 55.03 and 55.04 GHz.

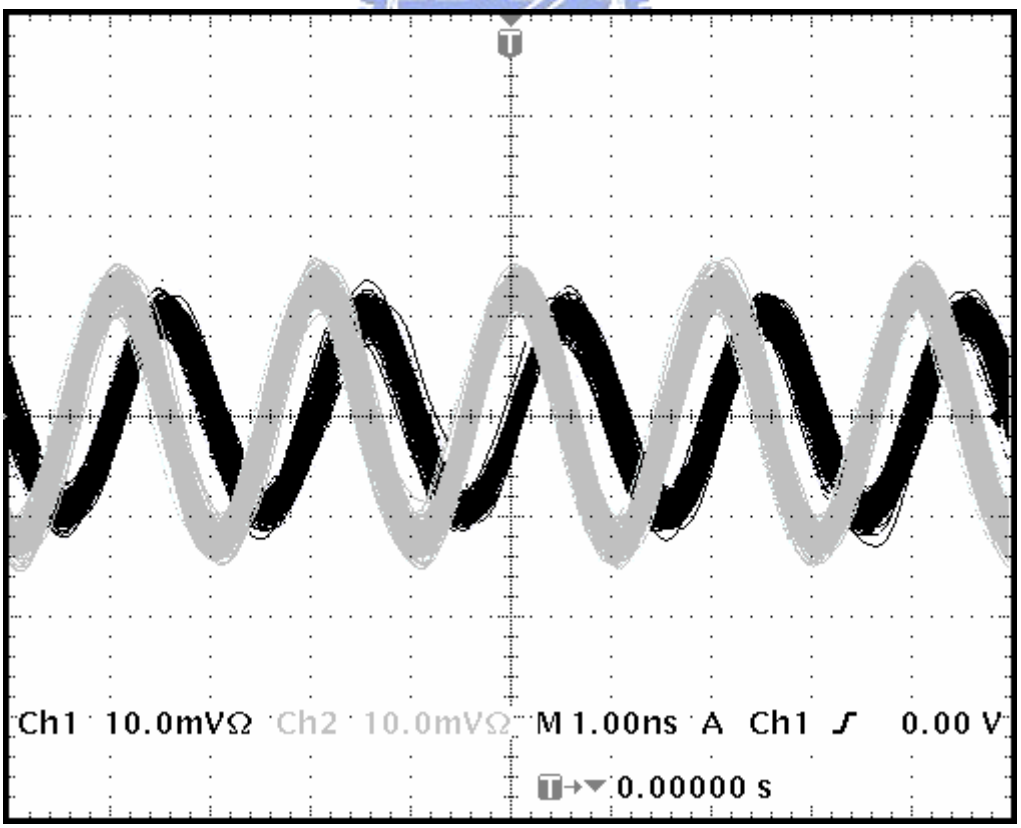


Fig. 4.21 Measured output waveforms with RF frequency of 55.07 GHz and IF frequency of 500 MHz.

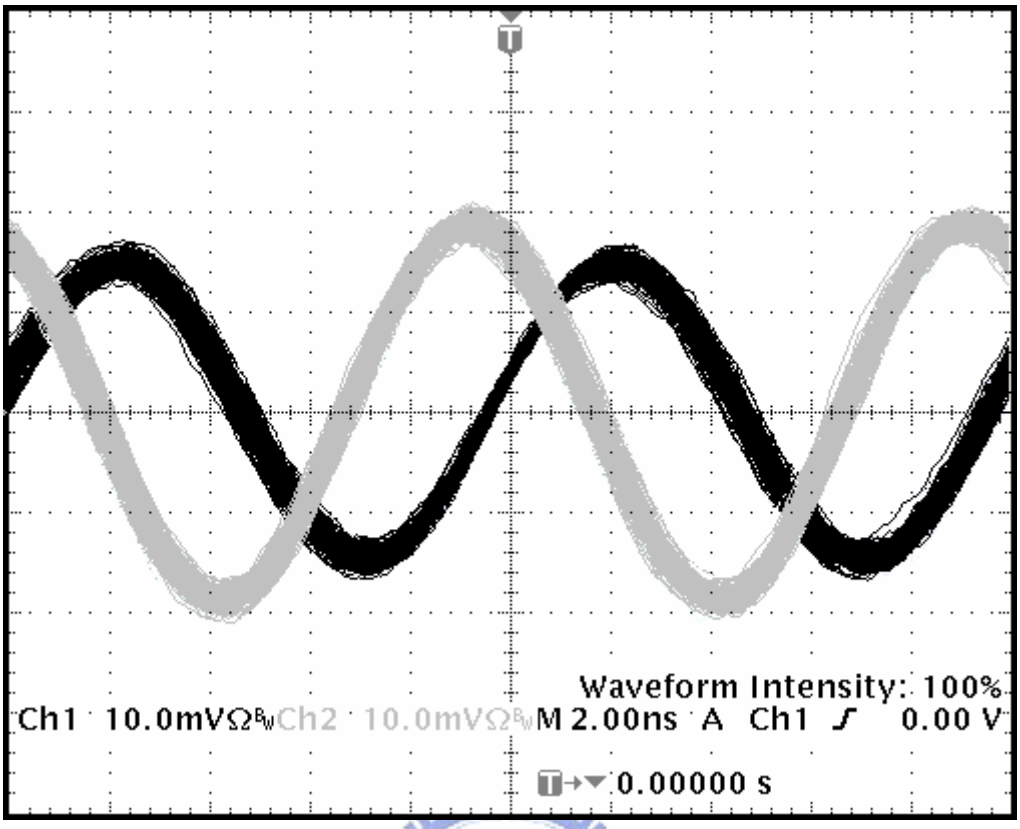


Fig. 4.22 Measured output waveforms with RF frequency of 55.03 GHz and IF frequency of 100 MHz.

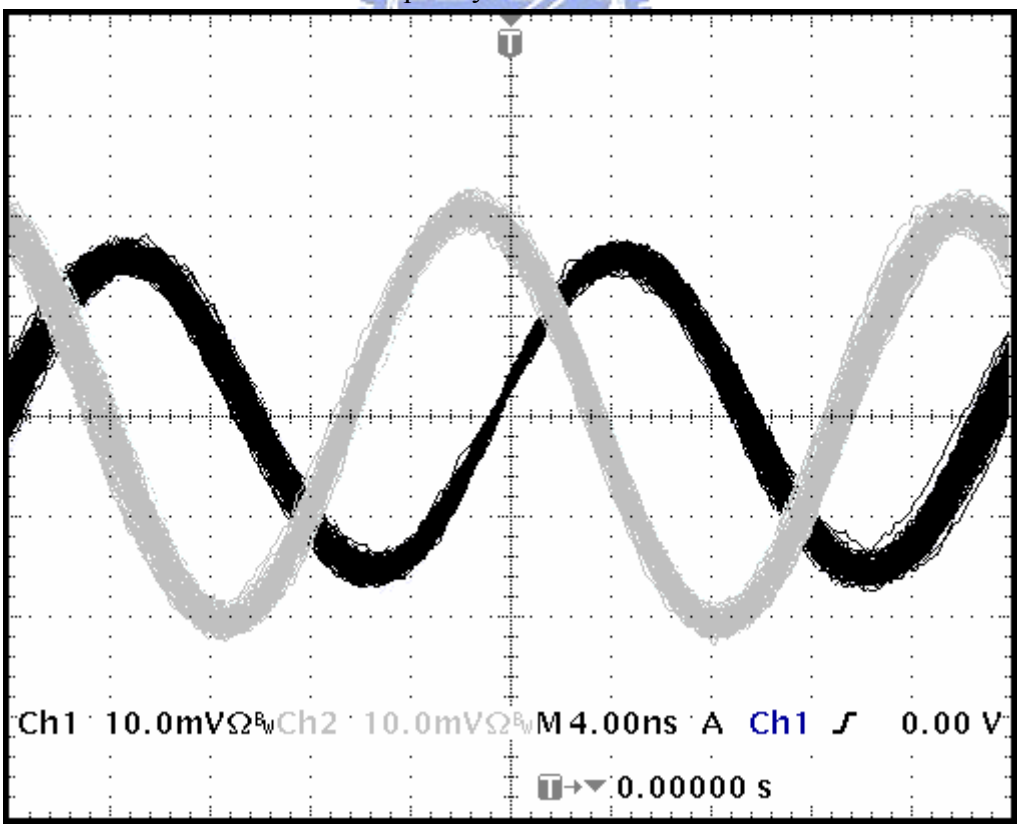
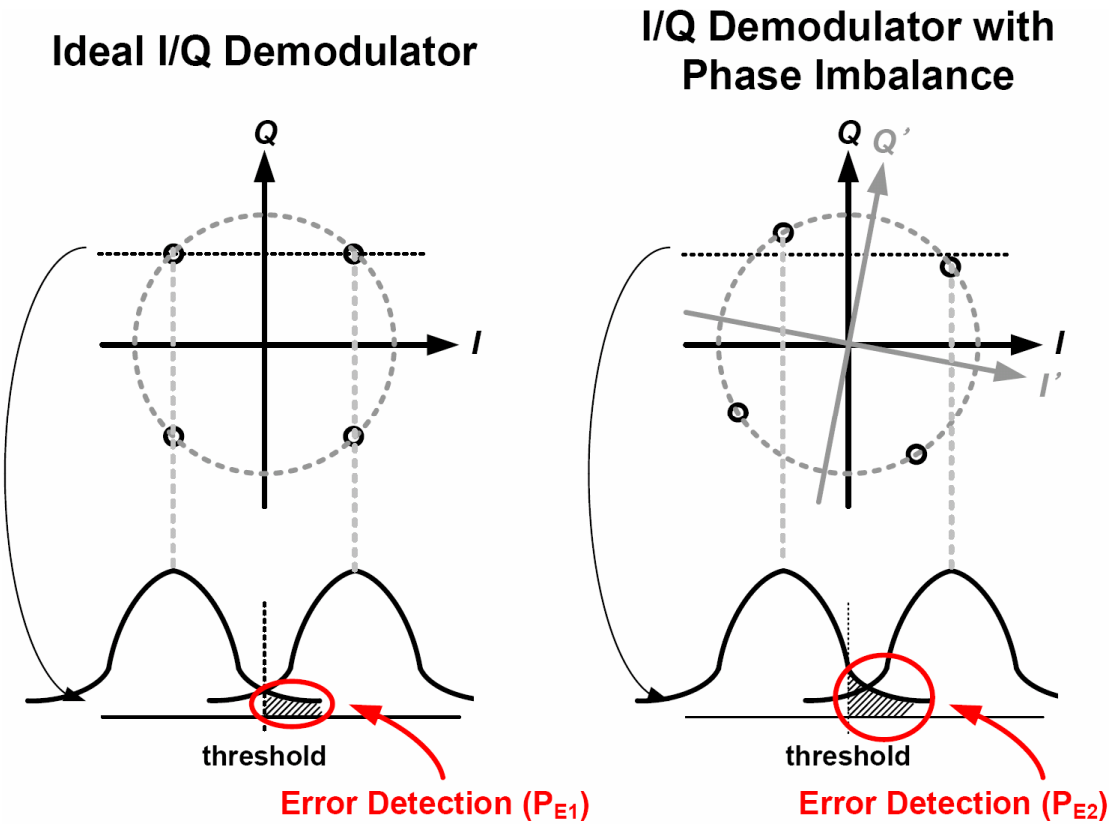


Fig. 4.23 Measured output waveforms with RF frequency of 55.025 GHz and IF frequency of 50 MHz.



(a) (b)

Fig. 4.24 The signal constellation and probability distribution of QPSK with (a) an ideal phase of I/Q channel and (b) a phase imbalance of I/Q channel.

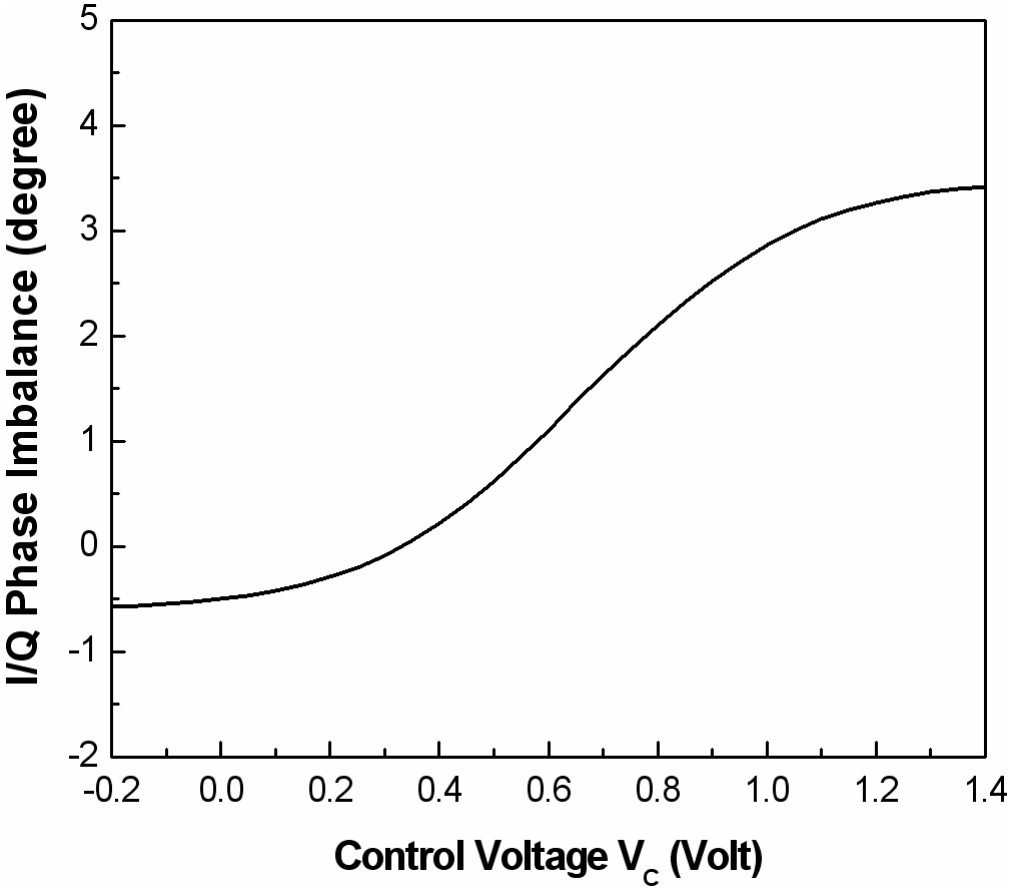


Fig. 4.25 EM simulated phase imbalance of QVCO outputs.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 MAIN CONTRIBUDTION

In this thesis, the design methodologies and implementations of subharmonic injection-locked frequency multiplier (ILFM) are presented. The proposed ILFM is successfully integrated with phase-locked loop (PLL) and direct-conversion receiver for 60-GHz applications.

Firstly, *K*- and *V*-band CMOS fully differential subharmonic injection-locked frequency triplers (ILFTs) are proposed, analyzed, and designed. A novel CMOS ILFT structure formed by frequency pre-generator stage and ILO stage is proposed. Based on the proposed ILFT structure, models for the locking range and the output phase noise are developed. In addition, the proposed ILFT has a current-reuse structure between the frequency pre-generator and the ILO for low power operation. A *K*-band ILFT is designed and fabricated using 0.18-μm CMOS technology. The measured locking range is 1092 MHz with a dc power consumption of 0.45 mW and an input power of 4 dBm. The harmonic rejection-ratios are 22.65, 30.58, 29.29, 40.35 dBc for the first, second, fourth, and fifth harmonics, respectively. The total locking range of the ILFT can achieve 3915 MHz when the varactors are used and the dc power consumption is increased to 2.95 mW. A *V*-band ILFT is also designed and fabricated using 0.13-μm CMOS technology. The measured locking range is 1422 MHz with 1.86-mW dc power consumption and 6-dBm input power. The locking range of the proposed ILFT is similar to the tuning range of a conventional

varactor-tuned bulk-CMOS VCO. Moreover, the proposed ILFT has a similar output power level to a VCO. As a result, it is feasible to use the proposed ILFT in low-power millimeter-wave synthesizers.

Secondly, a novel CMOS PLL integrated with ILFM that generates the *V*-band output signal is proposed and designed in 0.18-μm CMOS technology. The proposed 60-GHz PLL is composed of VCO, ILFM, 1/32 frequency divider, PFD, CP, and loop filter. Because the proposed ILFM can generate the fifth-order harmonic frequency of the VCO output, the operational frequency of the VCO can be reduced to only one-fifth of the desired frequency. Furthermore, the output frequency is higher than the transition frequency of device but the maximum operational frequency of frequency divider is only 11.6-GHz. The output frequency range of the proposed PLL is from 53.04 GHz to 58.0 GHz. The measured phase noises at 1 MHz and 10 MHz offset from the carrier are –85.2 and –90.9 dBc/Hz, respectively. The reference spur level of –40.16 dBc is measured. The dc power dissipation of the fabricated PLL is 35.7 mW under a 1.8-V supply. It can be seen that the performance of the proposed PLL is similar to previous woks but the power dissipation of the proposed PLL is only two-third of previous works [28]–[31]. Therefore, the proposed PLL structure is suitable for low power and high performance frequency synthesizer in 60-GHz applications.

Finally, a 60-GHz CMOS direct-conversion receiver front-end integrated with the ILFTs is designed and measured in 0.13-μm CMOS technology. The proposed direct-conversion receiver front-end is composed of a low-noise amplifier (LNA), I/Q quadrature down-conversion mixers, a 20-GHz QVCO, two ILFTs, two IF amplifiers, and two output buffers. A two-stage amplifier is used for LNA design to achieve the required gain and to dominate the receiver noise figure. The new method for

inter-stage bias is proposed to increase the voltage gain and reduce the extra noise source contribution to LNA. A shunt-peaking inductor for cascode device is designed to reduce the noise from cascode device. Therefore, the total noise figure of the whole is reduced. In the proposed receiver, the local oscillator signals are generated by the QVCO operated at only one-third of carrier frequency cascade with the two ILFTs. Based upon this approach, high frequency dividers operated at the carrier frequency with a significant amount of power dissipation are not needed while the proposed receiver is integrated with the frequency synthesizer. Because of the QVCO frequency shift, the maximum RF frequency is 55.03 GHz. The measured results show a receiver gain of 18.2 dB, a noise figure of 16.96 dB, and an input-referred 1-dB compression point of –17.0 dBm. The proposed receiver is implemented using 0.13-μm CMOS technology and draws 25.84 mA from a 1.2-V supply. The total chip area, including testing pads, is only 1.21 mm × 1.03 mm. As s result, the proposed receiver architecture provides a potential choice for high-integration, low-power, and small chip area in 60-GHz transceiver design..

In summary, using the proposed CMOS ILFM to realize the PLL and receiver, the power consumption can be reduced and performance can be similar to other structures. As the operational frequency is increased to 60-GHz or beyond, it is quite feasible to design high-performance, low-power, and high-integration CMOS transceivers in millimeter-wave band or even in the sub-millimeter-wave band.

5.2 FUTURE WORK

The simulation and measurement results have been shown that the proposed ILFT can achieve high output power with low power consumption. However, the

locking range of ILFT still can no be larger than 10-GHz even if the quality factor of *LC*-tank is decreased. The main reason is that the large parasitic capacitances between frequency pre-generator stage and ILO stage. The generated third-order harmonic signal is leaked to substrate. Thus, the locking range expressed in (2.15) should be considered the effect. To achieve larger locking range, the transformer-based ILFT will be designed to increase the injection current.

In the 60-GHz PLL design, the output power is too small to drive mixer directly. Moreover, the divide-ratio is not programmable and reference clock is higher than the commercial crystal oscillator. By using 130-nm CMOS technology or more advanced technology, the driving capability is increased to generate the 60-GHz signal with large output amplitude. The prescaler, program counter, and swallow counter will be used for channel selection. The increase of divide-ratio to reduce the reference frequency will be designed for system integration.

Finally, by careful whole chip EM simulation, the operational frequency will be moved to 60 GHz in the modified receiver chip. The I- and Q-channel outputs with small amplitude and phase imbalances will be redesigned by adding a ring oscillator between I/Q ILFTs or by careful layout plan in the future.

Therefore, a low-power, high-integration, high-performance single chip transceiver for 60-GHz applications will be designed and tape-out in the future.

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