高速低功率乘-累加器微架構與電路設計

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摘　　要

本論文針對處理器資料路徑提出一個在電路階層功率與速度最佳化的方法。利用高效率的乘法演算法，一個高速的乘-累加器微架構在本論文中被實現。根據此一高速的乘-累加器微架構設計，一個基於電晶體層次之高速低功率的乘-累加器也被實現。電晶體尺寸大小、電源電壓、以及臨界電壓作為調整參數，聯合這些參數採用本論文提出功率與速度最佳化的方法，可以使得動態的功率消耗減少原來的一半並使得速度提昇百分之二十。降低漏電流的設計方法於第四章被討論，針對在微架構階層一個資料路徑的功率與速度最佳化方法在第五章被討論。

本論文以 TSMC 0.13μm CMOS 技術實現。一個高速低功率 16X16+32 的乘-累加器利用微架構與電路的設計技巧在本論文中被實現，一個乘-累加的運算其最長路徑所需的時間在 2 奈秒內，動態功率消耗為 10 毫瓦。

High-Speed and Low-Power Multiplier-Accumulator Micro-Architecture and Circuit Design

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ABSTRACT

A power-speed optimization technique of circuit level for a datapath of processors is proposed in this thesis. By using efficient multiplication algorithms, a high-speed multiplier-accumulator micro-architecture is designed in this thesis. According to this high-speed micro-architecture design, a low-power transistor level multiplier-accumulator is also implemented. Take the transistor size, the supply voltage, and the threshold voltage as tuning variables which are optimized jointly in terms of power and speed in this thesis which can reduce the dynamic power to one half and can increase the speed to 20%. Design techniques of leakage current suppression are discussed in chapter 4. The micro-architecture optimization methods in terns of power and speed are also examined in chapter 5.

All the results are simulated in TSMC 0.13 μm CMOS technology. Making use of micro-architecture and circuit level design techniques, the critical path of a 16X16+32 multiplier-accumulator operation is within 2ns, the dynamic power consumption is below 10 mW.

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