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1989 Semicond. Sci. Technol. 4 177

(http://iopscience.iop.org/0268-1242/4/3/007)

Semicond. Sci. Technol. 4 (1989) 177–183. Printed in the UK

Characteristics of titanium silicide formed by Si/Mo/Ti trilayer metallisation

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Received 26 July 1988, in final form 19 October 1988, accepted for publication 16 November 1988

Abstract. The Si/Mo/Ti trilayer structure exhibits good oxidation resistance. The formed titanium silicide possesses a low resistivity of 16 $\mu\Omega$ cm after annealing for 30 min at 750 °C and good stability for wet and dry oxidation at temperatures above 900 °C. The barrier height of titanium silicides increases slightly as the annealing temperature is raised above 600 °C, and is about 0.6 eV at 750 °C for both the n-type and p-type substrates. With As^+ (or BF_2^+) ion implantation to increase the surface concentration of n-type (or p-type) substrate, the effective barrier height can be reduced to about 0.4 eV for an implantation dose of 1.0×10^{15} cm^{-2}. By means of As_2^+ (or BF_2^+) ion implantation to introduce a thin inversion layer on p-type (or n-type) silicon substrate, the effective barrier height is increased to about 0.9 (or 0.82) eV for a dose of 1×10^{12} cm^{-2}.

1. Introduction

Refractory-metal silicides with low resistivities and high stabilities have been under active investigation as interconnect and electrode materials for very-large-scale integration (VLSI) circuits [1–5]. Among them, $TiSi_2$ is probably the most attractive candidate for self-aligned silicide (salicide) application [4, 5]. It has relatively low resistivity (15–20 $\mu\Omega$ cm) and high thermal stability. Nevertheless, due to the high oxidation rate of Ti to some oxidants even by two-step annealing [6], the quality of the resultant $TiSi_2$ is very sensitive to oxidising gases in the sintering atmosphere. The undesired oxidation results in a non-uniform silicide formation and non-uniform etching due to variations in the oxidised Ti surface across a wafer. Park *et al* [7] proposed a Mo/Ti bilayer structure to solve this problem. However, as oxidants may penetrate the top Mo layer to react with the bottom Ti layer, it still requires some degree of ambient control. Lin *et al* [8] suggested a Si/Mo/Ti trilayer structure to overcome this problem. It is reported that a top Si layer can prevent the residual oxidants from reaching the bottom Ti layer and that an Mo layer can eliminate the undesired reaction between Si layer and Ti layer.

Silicides are attractive for gate metallisation because of the possibility of forming silicides directly on polysilicon, thus preserving the basic polysilicon MOS gate while decreasing the resistance. Hence, it is important to examine the compatibility and stability of titanium silicide as it is formed on polysilicon gate. In this work, the compatibility of $TiSi_2$ with polysilicon gate is studied on the basis of the Si/Mo/Ti structure for $TiSi_2$ formation as mentioned above. Oxidation properties of Ti silicide are examined in dry and wet oxygen atmospheres. Results of investigation on Schottky barrier heights for $TiSi_2$ contacting with ion-implanted silicon substrate are presented. This is aimed at potential applications in using a silicide–n–p (or silicide–p–n) Schottky barrier structure for solar cell and other IC usage [9].

2. Experimental procedures

For several experiments in this study, (100) n-type wafers with resistivity of 2–4 Ω cm were employed. Wafers were first oxidised to form a 500–1000 Å SiO_2 layer. A 2000 Å polysilicon layer was then deposited by LP CVD and doped by $POCl_3$ diffusion. A trilayer structure which consists of ≃400 Å Ti, ≃500 Å Mo and ≃1000 Å Si films was successively deposited with an ETE CL680 Dual E-gun multiple-crucible evaporator at $\simeq 10^{-6}$ Torr. For comparison, the trilayer structure was also deposited directly on the single-crystal silicon substrate of the same type and orientation. The film thickness was controlled by a IC 2000 thickness monitor. Several samples were then annealed in an N_2-flowing (5000 cm^3 min^{-1}) open-tube furnace from 550 to 1000 °C in 50 °C increments for 30 min, and other samples at 600 or 750 °C from 10 to 180 min to examine the change of sheet resistance with time.

After annealing the top Si layer of the samples was removed by CF_4/O_2 gas-plasma etching. The Mo layer and the unreacted Ti were then etched in a solution of $NH_4OH:H_2O_2:H_2O = 1:1:5$ in molar ratio for 20 min.

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The sheet resistance of the samples was measured with the four-point probe. The structural and morphological development of the samples was analysed with an x-ray diffractometer (Shimadzu XD-5), scanning electron microscope (Hitachi S-570), transmission electron microscope (JEOL 100-CXII) and Rutherford back-scattering (RBS) technique.

Samples annealed at 750 °C for 30 min were oxidised in dry or wet O_2 atmosphere from 700 to 1100 °C in 100 °C increments for 1 h after the removal of the Si/Mo layer. The sheet resistance of these samples was then measured again with the four-point probe, and microstructures were analysed with SEM, TEM and x-ray diffractometer.

In some other experiments, both (100) n-type (4–7 Ω cm) and (100) p-type (6–20 Ω cm) wafers were used. Wafers were first oxidised to form an SiO_2 layer of ≃4200 Å for passivation. The oxide on the back side was then removed. $POCl_3$ diffusion was performed on the n-type wafers to improve the ohmic contact on the back side. The front side of the SiO_2 layer was patterned into circles with a diameter of 350 μm.

Before ion implantation, a 620 Å SiO_2 layer was grown on the patterns as the barrier layer. Arsenic was implanted through the barrier layer on the n-type wafers at an energy of 140 keV with a dose ranging from 1.0×10^{12} to 1.0×10^{15} As^+ cm^{-2}. The same energy was applied on the p-type wafer, but with a dose in the range of 1.0×10^{11} to 1.0×10^{12} As^+ cm^{-2}. Boron implantation was performed on the n-type wafers at an energy of 90 keV with a dose ranging from 1.0×10^{11} to 1.0×10^{12} BF_2 cm^{-2}. On the p-type wafers, the same energy was used but with a dose in the range of 1.0×10^{12} to 1.0×10^{15} BF_2 cm^{-2}. All the wafers were then annealed at 900 °C for 30 min in O_2 ambient to activate the dopants. The active area of the diodes was defined again by aligning to the original patterns and the SiO_2 barrier layer was removed by buffer oxide etching (BOE). The trilayer structure was deposited and patterned by the lift-off technique. In this scheme, positive photoresist was used as mask material, and the trilayer structure was deposited in a vacuum chamber at a temperature of about 20 °C by a dual e-gun. The sintering of the samples was performed in an N_2-flowing (5000 cm^3 min^{-1}) open-tube furnace at temperatures from 600 to 900 °C in 50 °C increments and then the Si and Mo layers were removed as described above.

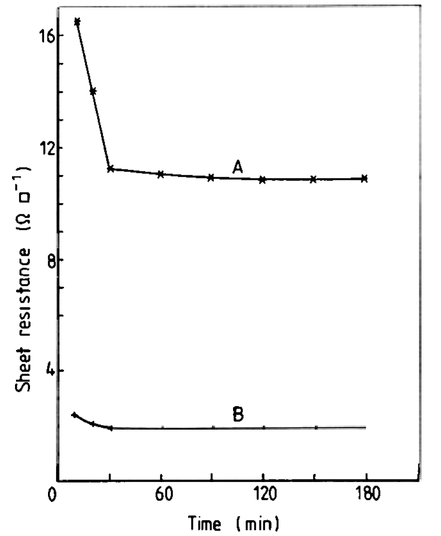

Figure 1. Sheet resistances of titanium polycide as a function of sintering time in N_2 atmosphere at temperatures of: A, 600 °C; B, 750 °C.

Finally, an aluminium film of about 6000 Å was deposited onto the back side of the wafers and sintered at 400 °C for 20 min. Current–voltage (I–V) measurements were performed on these diodes with a semiconductor parameter analyser (Hewlett Packard HP4145).

3. Results and discussion

Figure 1 shows the plot of the sheet resistance R_s for titanium polycide after the top Mo/Si layers were removed as a function of sintering time at 600 and

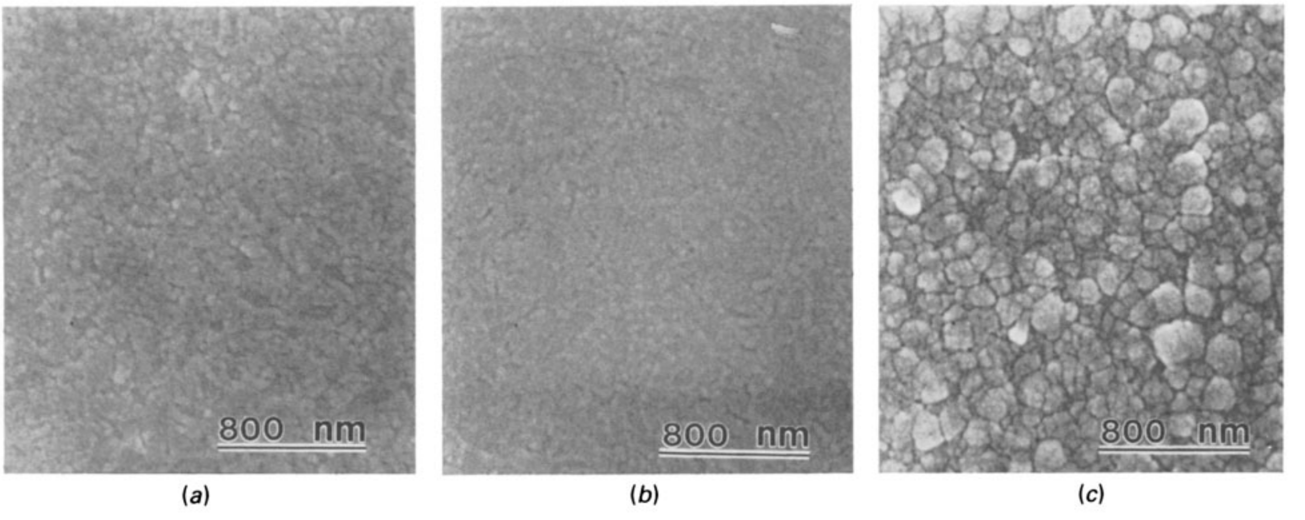

Figure 2. SEM micrographs of titanium silicides formed by sintering the Si/Mo/Ti trilayer structure on silicon at 600 °C for (*a*) 10 min, (*b*) 20 min and (*c*) 30 min in N_2 ambient.

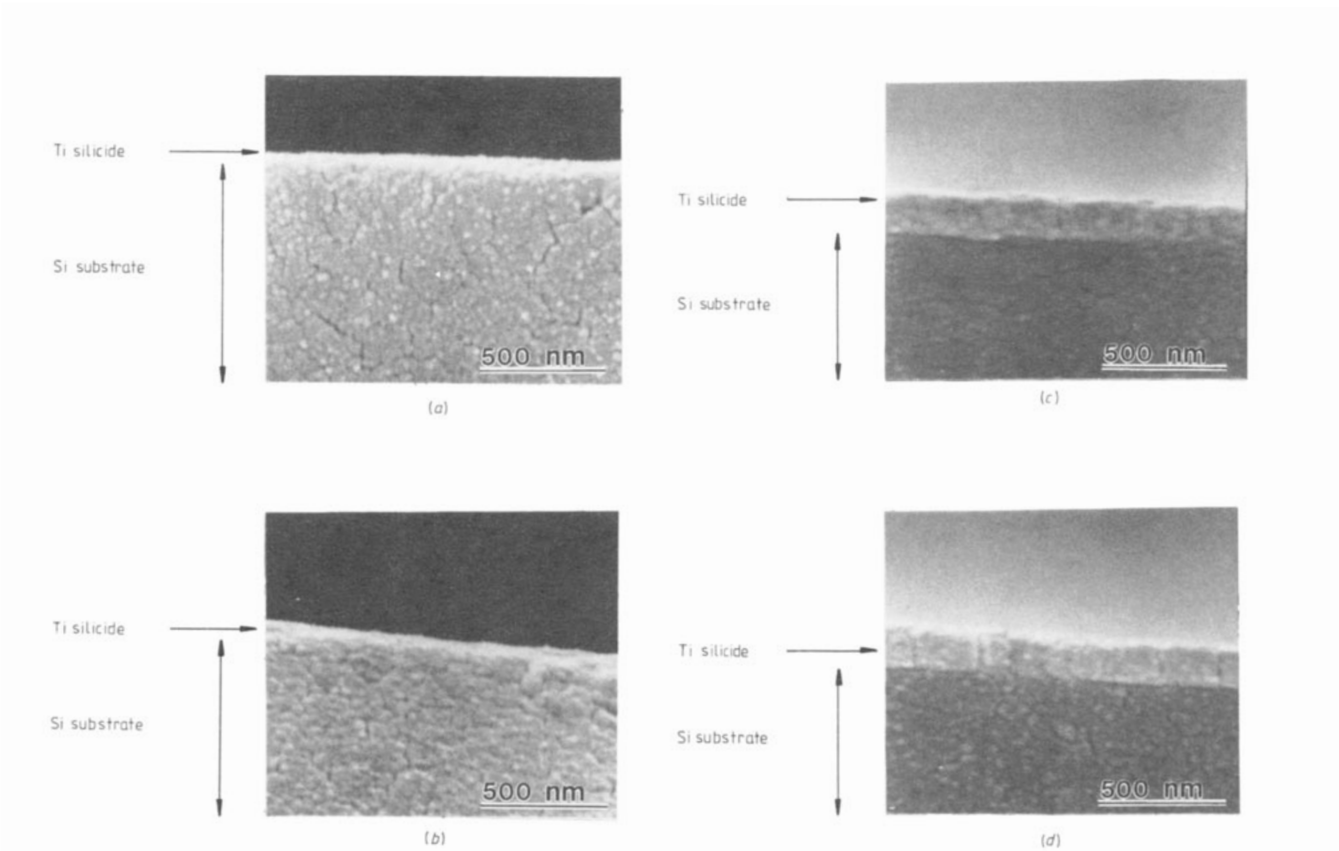

Figure 3. SEM cross-section micrographs of titanium silicides formed by sintering the Si/Mo/Ti trilayer structure on silicon at 600 °C in a N_2 atmosphere for (*a*) 10 min, (*b*) 20 min, (*c*) 30 min, (*d*) 120 min.

750 °C. At both temperatures, R_s decreases with time and eventually reaches a minimum value after sintering for longer than 30 min. This is similar to that reported by Murarka and Fraser. For less than 20 min sintering at 600 °C, neither silicide formation nor grain growth is observed, as shown in figures 2(*a*) and (*b*). After 30 min annealing, the grain becomes larger as presented in figure 2(*c*), and TiSi crystalline phase is detected by the x-ray diffraction [6]. The formation of silicide causes the low sheet resistance as shown in figure 1. Figure 3 presents a cross-sectional view of titanium silicide film annealed at 600 °C for different times. It is interesting to note that the thickness of the titanium silicide seems to be the same for samples annealed for longer than 30 min, as shown in figures 3(*c*) and (*d*). This implies that after 30 min annealing at 600 °C, the reaction between the Ti film and the silicon is nearly accomplished. This is consistent with

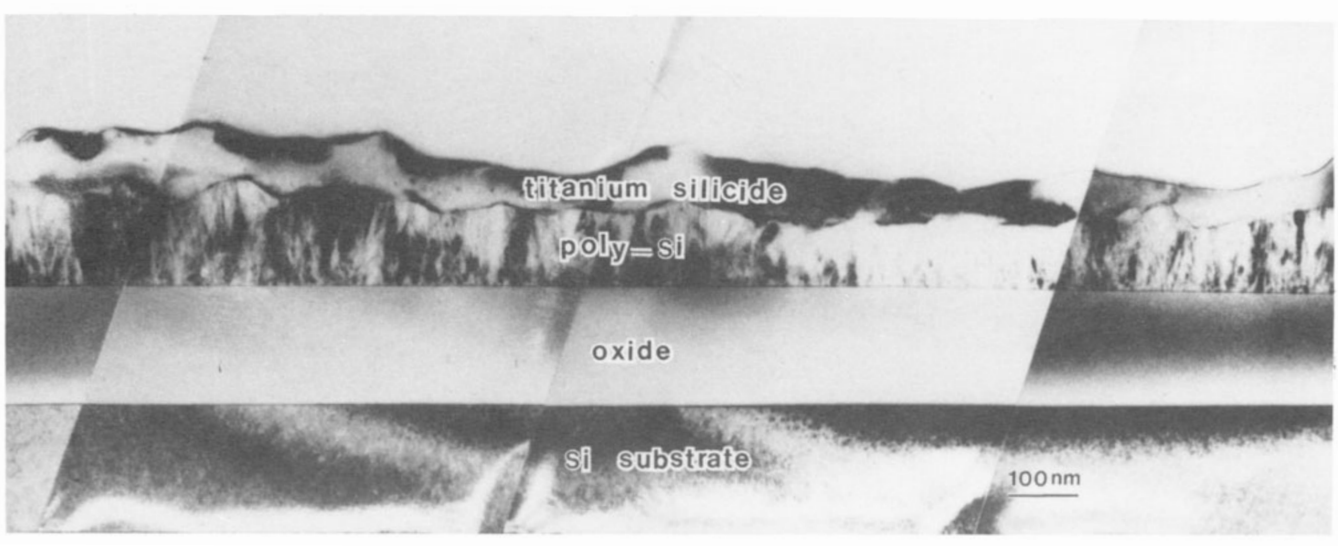

Figure 4. TEM cross-section of $TiSi_2$ polycide gate. The silicide was formed by sintering the trilayer structure Si/Mo/Ti on doped polysilicon at 750 °C for 30 min in a N_2 atmosphere.

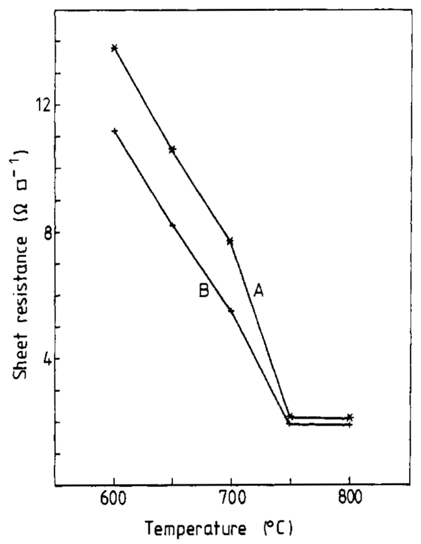

Figure 5. Plots of sheet resistances of titanium silicides as a function of the sintering temperature for 30 min in a N_2 atmosphere by depositing a trilayer structure Si/Mo/Ti on: A, single-crystal silicon; B, doped polycrystalline silicon.

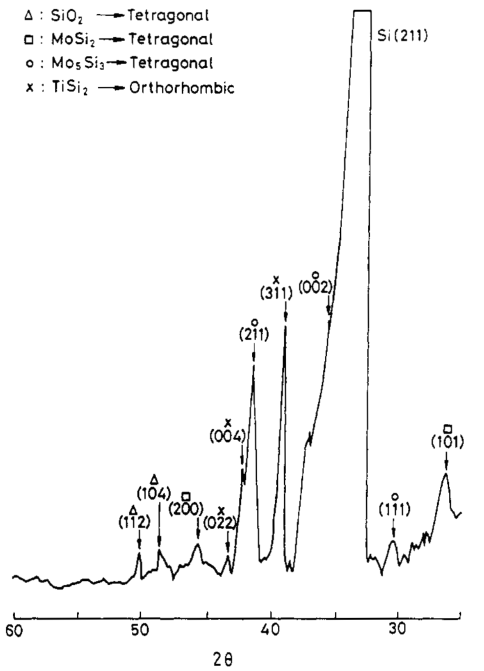

Figure 6. X-ray diffraction pattern for the sample derived from the Si/Mo/Ti trilayer structure on doped polysilicon gate sintered at 850 °C for 30 min in a N_2 atmosphere.

the trend in sheet resistance as presented in figure 1. Besides, it can be seen that the microstructure of the silicide consists of columnar grains.

The TEM cross section of $TiSi_2$ polycide gate is represented in figure 4. The silicide was formed by sintering the trilayer structure Si/Mo/Ti on doped polysilicon ($18\,\Omega\,\square^{-1}$) at 750 °C for 30 min in N_2 atmosphere. The polysilicon layer has a columnar structure which is a typical characteristic observed in the as-deposited polysilicon film. This suggests that the annealing treatment, i.e., 750 °C for 30 min, does not induce any grain growth in the polysilicon layer. A silicide film of about 800 Å is formed at the surface of poly-Si with a wavy polysilicon interface. TEM investigation of this sample indicates that there is a weak diffraction contrast in this layer, which is believed to be the result from the partial crystallisation of titanium silicide after annealing.

The crystallisation of titanium silicide depends on the annealing temperature. For samples annealed at a temperature lower than 600 °C, no crystalline titanium silicide that can withstand the etching of ($NH_4OH + H_2O_2$) is formed. On the basis of x-ray diffraction patterns, it is seen that from 600 to 700 °C, TiSi is the dominant phase along with a small amount of $TiSi_2$ present, while from 750 to 800 °C the TiSi phase disappears and only $TiSi_2$ exists [6]. The sheet resistance as a function of sintering temperature by depositing the trilayer structure Si/Mo/Ti on the single-crystal silicon and doped polycrystalline silicon is given in

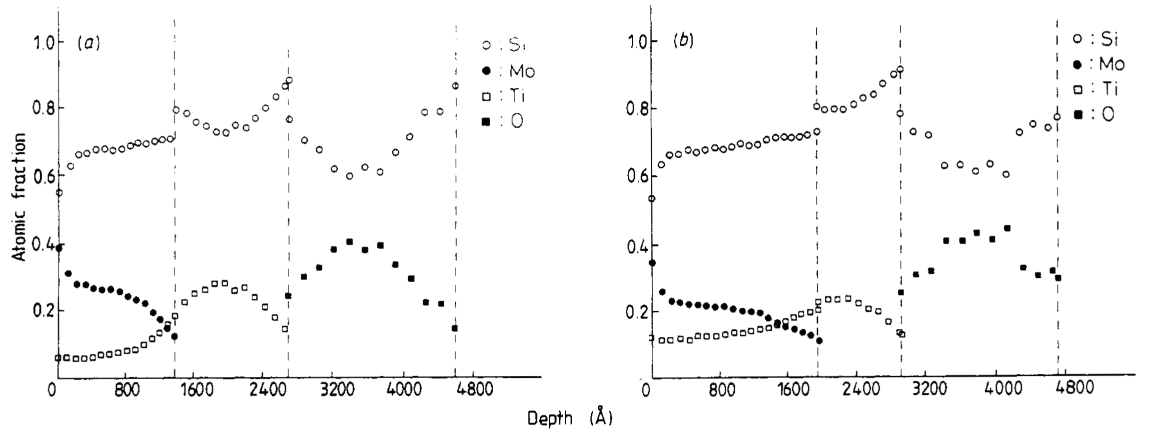

Figure 7. Depth profiles of the elements Si, Mo, Ti and O calculated from corresponding RBS spectra for the sample derived from the Si/Mo/Ti trilayer structure on doped polysilicon gate sintered for 30 min in a N_2 ambient at (*a*) 900 °C and (*b*) 1000 °C. The vertical lines are the original boundaries between different layers. The discontinuities in atomic fraction are attributed to the different initial concentrations in the deposited layers.

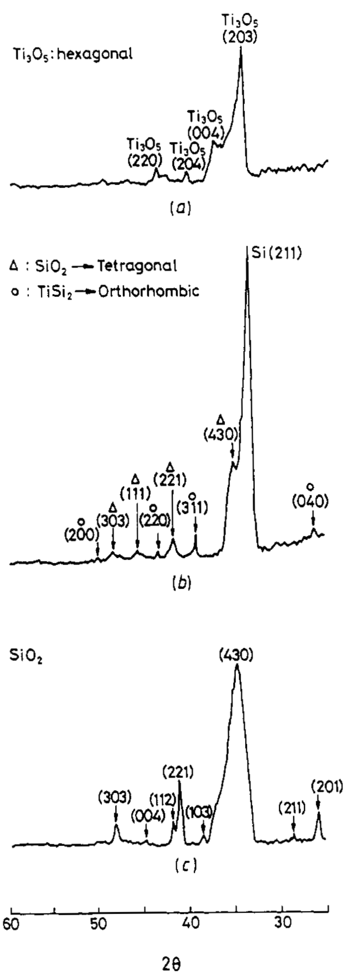

Figure 8. X-ray diffraction patterns of titanium disilicide oxidised in dry O_2 for 1 h at (*a*) 700 °C, (*b*) 800 °C and (*c*) 1000 °C. The $TiSi_2$ is formed on doped polysilicon at 750 °C annealing for 30 min.

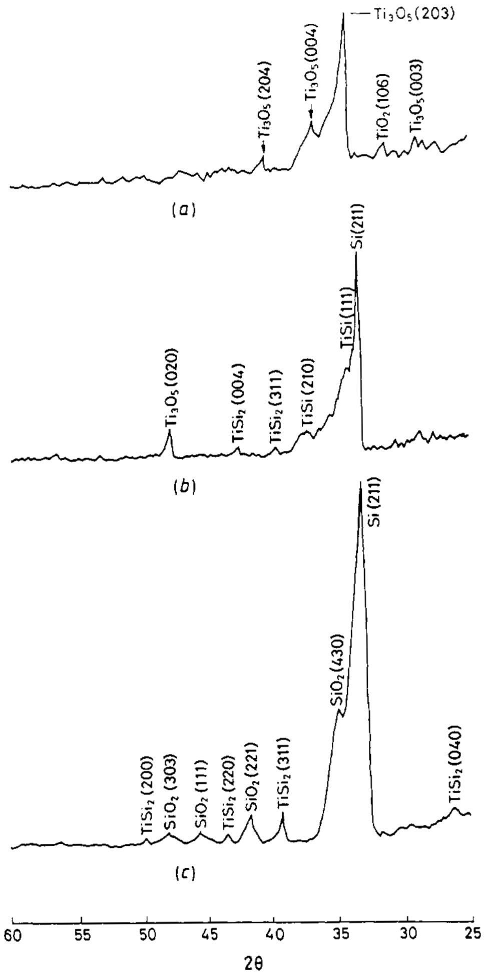

Figure 9. X-ray diffraction patterns of titanium disilicide oxidised at (*a*) 700 °C, (*b*) 800 °C and (*c*) 900 °C in wet O_2 for 1 h and then etched in BOE for 1 min. The $TiSi_2$ is formed on doped polysilicon at 750 °C annealing for 30 min.

figure 5. The sheet resistance decreases as the sintering temperature is raised above 600 °C, and a constant R_s is obtained at temperatures higher than 750 °C. R_s of silicide deposited on doped polysilicon is smaller than that on single-crystal silicon. This may be caused by the leakage current of the low-resistance polysilicon film during four-point probe measurements. It is argued that the formation of $TiSi_2$ at the expense of TiSi results in the decrease of the sheet resistance [10]. The resistivity calculated from R_s ($\simeq 2\,\Omega\,\square^{-1}$ in figure 5) and sample thickness ($\simeq$800 Å) is about 16 $\mu\Omega$ cm, which is comparable with the value, 13–16 $\mu\Omega$ cm, reported by Murarka *et al* [1,10].

When samples are sintered at higher temperatures, i.e., 850 °C or above, interdiffusion of Mo and Ti results in a mixed layer of Mo silicide and Ti silicide on the titanium silicide layer as indicated by x-ray diffraction and RBS analysis results presented in figures 6 and 7, respectively. On the basis of the depth profiles of the elements Si, Mo, Ti and O calculated from corresponding RBS spectra for samples annealed at 900 °C, and 1000 °C, as shown in figures 7(*a*) and (*b*), respectively, it is found that the out-diffusion of Ti atoms into the Mo layer increases as the sintering temperature increases. However, since Ti silicide with optimum properties can be obtained at a sintering temperature as low as 750 °C [1, 2, 10], the interdiffusion of Mo and Ti will not come into effect during practical applications.

One important test of the compatibility of a polycide structure with VLSI interconnect fabrication is the ability to grow a self-passivating oxide layer without degrading the polycide or the underlying gate oxide integrity. Figures 8 and 9 are the x-ray diffraction patterns of titanium disilicide after dry and wet oxidation from 700 to 1100 °C, respectively, for 1 h. It is found that titanium disilicide decomposes and titanium oxides are formed after both dry and wet oxidations at 700 °C for 1 h as shown in figures 8(*a*) and 9(*a*). For wet oxidation at 800 °C, parts of the $TiSi_2$ either reduce to TiSi and form SiO_2 or decompose to form SiO_2 and titanium oxides as indicated in figure 9(*b*). At 900 °C, SiO_2 can be produced on the silicide film without changing the stoichiometry of the titanium disilicide as presented in figure 9(*c*). It is presumed that at higher temperatures (>900 °C) silicon can diffuse from the Si substrate through the $TiSi_2$ to the surface where it reacts with oxygen, and dominates the oxidation mechanism before $TiSi_2$ dissociates [11,12]. Hence, the stoichiometry of titanium disilicide is thus preserved. At low temperatures, silicide dissociation dominates to form titanium oxides.

Both wet and dry oxidation seem to induce the grain growth of the $TiSi_2$ at higher temperature (>900 °C), as shown in figure 10. Mochizuki *et al* [13] also reported similar phenomena in molybdenum silicide oxidation. The rough silicide–silicon interface may be caused by different silicon diffusion rates through the silicide layer.

Forming good contact is essential to the operation of the devices. Small barrier height ensures small specific contact resistance. The Schottky barrier height and the ideality factor are obtained from the current–voltage characteristic of a Schottky diode. Figure 11 is the Schottky barrier height as a function of sintering temperature for titanium silicide formed on n-type and p-type substrates. For the n-type substrate, from 600 to 750 °C, the values of barrier heights are below 0.6 eV, which is comparable with that reported by Cowley *et al* [1, 14]. The slight change with temperature may be attributed to the change of the crystalline phase at the silicide–silicon interface or due to the associated phase transformation. Above 750 °C, the barrier heights

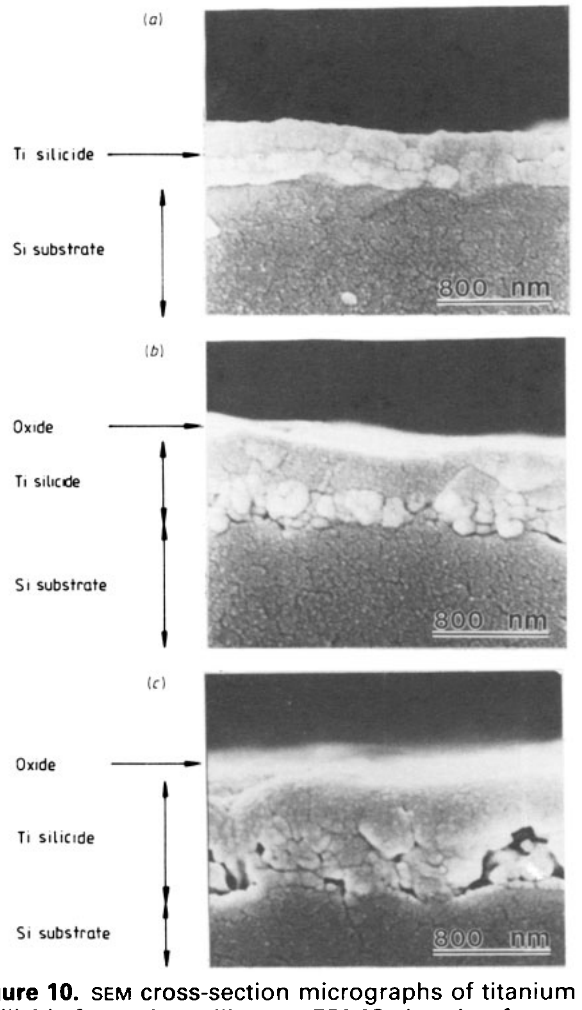

Figure 10. SEM cross-section micrographs of titanium disilicide formed on silicon at 750 °C sintering for 30 min: (*a*) before oxidation, (*b*) dry oxidation at 1000 °C for 2 h and (*c*) wet oxidation at 900 °C for 2 h.

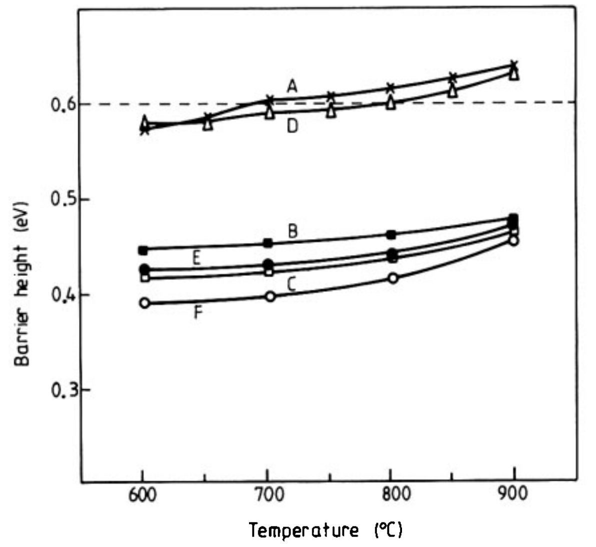

Figure 11. Plot of the Schottky barrier height φ_B of titanium silicide as a function of sintering temperature. The silicide was formed on: A, unimplanted n-type (100) Si substrate; B n-type (100) Si substrate, As^+ implanted, dose: 1×10^{14} cm^{-2}; C, n-type (100) Si substrate, As^+ implanted, dose: 1×10^{15} cm^{-2}; D, unimplanted p-type (100) Si substrate; E, p-type (100) Si substrate, BF_2^+ implanted, dose: 1×10^{14} cm^{-2}; and F, p-type (100) Si substrate, BF_2^+ implanted, dose: 1×10^{15} cm^{-2}. The φ_B values were calculated assuming the effective Richardson constant to be equal to the standard value of 120 A cm^2 K^{-2}. The average values of ideality factors *n* were 1.08 and 1.09 for n-type samples and p-type samples, respectively.

become larger than 0.6 eV and even reach 0.63 eV at 900 °C. It is argued that during sintering a doping level change occurs in the silicon near the silicide–silicon interface [15]. A similar result is also observed for titanium silicide formed on p-type substrate as demonstrated in curve A of figure 11.

As the Schottky barrier height depends on the doping level at the silicide–silicon interface [16], it can be varied by controlling the doping level in the surface layer of the silicon substrate. Several samples are ion-implanted with As^+ (or BF_2) ions to study the effect of doping level on Schottky barrier height, and the results are plotted in figure 12. It is observed that the effective barrier height are reduced by 'shallow' implantation of As^+ into an n-type substrate or by BF_2 into a p-type substrate. The effective barrier heights of the implanted diodes also vary slightly with the sintering temperatures as shown in curves B, C, E and F in figure 11. This could be explained on the basis of arguments similar to that of the unimplanted diode, in which the dopant concentration changes in the silicon near the silicide–silicon interface during sintering.

The effective barrier height in a $TiSi_2$–p-type (or $TiSi_2$–n-type) silicon Schottky diode is increased by ion implantation to introduce a thin inversion layer on silicon substrate. Experimental results in figure 12 show that the effective barrier heights increase from 0.6 eV for the $TiSi_2$–p–Si (or $TiSi_2$–n–Si) Schottky diode to 0.9 (or 0.82) eV for a $TiSi_2$–n–p–Si (or $TiSi_2$–p–n–Si)

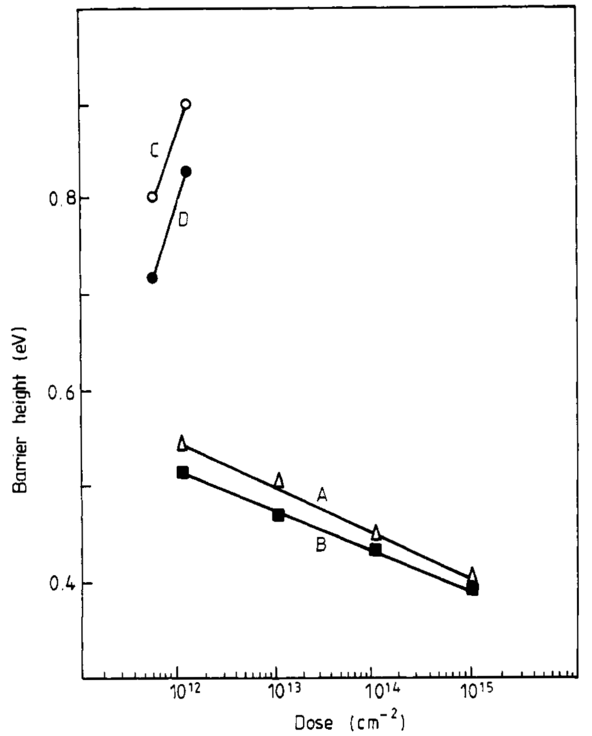

Figure 12. Plot of the effective Schottky barrier height φ_B of titanium silicide formed on: A, As^+-implanted n-type (100) Si wafer; B, BF_2^+-implanted p-type (100) Si wafer; C, As^+-implanted p-type (100) Si wafer; D, BF_2^+-implanted n-type (100) Si wafer as a function of dose concentrations. The $TiSi_2$ is formed at 750 °C annealing for 30 min. The φ_B values result from *I–V* measurement with average ideality factor *n* being 1.09.

Schottky diode with an As^+-implanted (or BF_2-implanted) layer and a dose of $1 \times 10^{12}\ cm^{-2}$. These data fall in the same range as those of Ti metal–p–Si (or Ti metal–n–Si) reported by Li *et al* [9].

4. Conclusions

Titanium silicide formed by depositing the Si/Mo/Ti trilayer structure on silicon or polysilicon exhibits a resistivity of $\simeq 16\,\mu\Omega$ cm when annealed at temperatures higher than 750 °C. $TiSi_2$ is observed to be the phase present to lower the sheet resistance in the Ti–Si system.

For self-passivation and compatibility with polysilicon gate, it is found that at temperatures above 900 °C, a self-passivating oxide layer can be grown without degrading the polycide or the underlying gate oxide integrity if the polysilicon beneath the silicide is sufficiently thick. At lower temperatures, some titanium disilicide decomposes or reduces to TiSi and titanium oxides are formed for both dry and wet oxidation. Diffusion of Si from the polysilicon layer through $TiSi_2$ to the surface to react with oxygen is believed to be the dominant mechanism for SiO_2 formation at elevated temperatures.

As the titanium silicide contacts with n- or p-type substrates, the barrier height increases slightly as the annealing temperature increases. The barrier height can be controlled by varying the dose concentration. Higher doping by ion implantation can be employed to reduce the barrier height. Enhancement of the effective barrier height in a $TiSi_2$–p-type (or $TiSi_2$–n-type) silicon Schottky diode is achieved by using As^+ (or BF_2) implantation to introduce a thin surface inversion layer between $TiSi_2$ and p-Si (or n-Si) substrate.

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