國 立 交 通 大 學

電子工程學系　電子研究所碩士班

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具基體雜訊考量之射頻電壓控制振盪器電路設計

CMOS RF VCO Design with Substrate Noise Consideration

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中華民國九十四年三月

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摘要

本論文主旨在探討不同結構的變容器對於基體雜訊的隔絕能力。就標準互補式金氧半導體製程而言，有四種金氧半導體結構可以作爲變容器，而且這四種變容器都具有可以隔絕基體雜訊的特定結構。本論文的第二章將探討與比較這四種變容器的高頻特性。

這四種變容器中，其中兩種生成於 n 型井上且利用介於 n 型井與基體的 p-n 接面隔絕基體雜訊；另外兩種生成於 p 型井上且被深層 n 型井與 n 型井所包圍以隔絕基體雜訊。本論文的第三章將比較這兩種結構對於基體雜訊的隔絕能力。

在本論文的第五章中，我們利用 0.25 微米互補式金氧半導體製程設計且實現了三個操作在 2.4GHz 頻段的電感電容共振型電壓控制振盪器電路。VCO1 與 VCO2 唯一不同的地方在於所使用的變容器，這兩種變容器以不同的結構來隔絕基體雜訊。將訊號產生器提供的一個射頻訊號注入基體中作爲基體雜訊，我們將探討耦合至變容器的基體雜訊對於 VCO1 與 VCO2 輸出頻譜的影響。VCO1 與 VCO3 採用相同結構的電感與變容器但是不同的電路架構，我們將利用 VCO1 與 VCO3 來比較不同電路架構的相位雜訊。

CMOS RF VCO Design with Substrate Noise Consideration

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Abstract

The isolation capabilities of varactors with different structures against substrate noise are investigated in this thesis. In chapter 2, four types of MOS structure varactor available in standard CMOS processes are investigated. They all have specific structures able to isolate substrate noise. High-frequency characteristics of them are compared. Among these four varactors, two of them are fabricated on n-well and use the p-n junction between n-well and substrate to isolate substrate noise. The other two are fabricated on p-well and surrounded by deep n-well and n-well in order to isolated substrate noise. Isolation capabilities of different isolation structures are compared in chapter 3.

In chapter 5, three 2.4GHz LC VCO circuits are designed and realized in a 0.25-um CMOS process. VCO1 and VCO2 differ only in the type of varactor. An RF signal provided by signal generator is injected into the substrate as substrate noise. The influences of substrate noise coupling to the varactors on the output spectrums of VCO1 and VCO2 are investigated. VCO1 and VCO3 use the same type of inductor and varactor, but they differ in the type of circuit topology. The phase noise of them is compared.

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Chapter 1

Introduction

1.1 Background

Recently, there has been considerable interest in the use of standard CMOS processes to implement RF transceiver components such as low-noise amplifiers (LNAs), mixers, and voltage-controlled oscillators (VCOs). The benefit is the potential for achieving high-levels of RF/analog/digital integration, rapidly approaching single-chip system implementations.

VCOs are key components of RF transceivers for wireless communications. The VCOs used in RF transceivers are usually embedded in a frequency synthesizer so as to generate a precise definition of the local oscillator (LO) signal for upconversion from and downconversion to the baseband. The role of frequency synthesizer in generic transceiver is illustrated in Fig. 1.1 [1]. The frequency synthesizer is conceptually a phase-locked loop. There are several frequency synthesizer architectures, including integer-N, fractional-N, and direct-digital synthesis techniques. Fig. 1.2 shows the architecture of a basic phase-locked frequency synthesizer. The channel control input is a digital word that varies the value of M. Since $f_{out} = Mf_{REF}$, the relative accuracy of f_{out} is equal to that of f_{REF}. For this reason, f_{REF} is derived from a stable, low-noise crystal oscillator [2].

Inductance-capacitance (LC) tank oscillator is a superior choice due to the inherent bandpass filtering of the LC resonator which can suppress side-band noise. Thus, for monolithic integration in CMOS, LC-tank VCOs are preferred over ring oscillators which are easier to integrated and less area consuming.

Despite the continuous improvement, VCOs still remain the bottleneck and, thus, the main challenge of RF transceivers. This is due to the combination of very demanding VCO parameters: low phase noise, low power consumption, and large frequency tuning range. In LC-tank VCOs, phase noise and power consumption depend primarily on the quality factor (Q) of the tank. The frequency tuning range is determined by the capacitance tuning range of the varactor (voltage-dependent capacitor) and parasitics in the VCO. Hence, a main task is to optimize the performance of inductors and varactors.

Monolithic inductors are usually implemented as spiral structures in the use of thick top metal in standard CMOS processes. Due to large energy loss to the substrate, they feature poor Q, compared to the varactors realized in standard CMOS processes. Therefore, it is expected that, independent of the type of varactor, the spiral inductor will determine the worst-case Q of the LC-tank and the worst-case phase noise of the VCO [3]. The Q of the inductor is defined as $\omega L/R_s$. A circular spiral inductor exhibits less metal resistance and thus higher Q for a given value of inductance and metal wire width. Despite extensive recent work, the Q of the inductors in standard CMOS processes has been limited to low value. Thus, the monolithic inductors still limits the phase-noise performance of fully integrated LC-tank VCOs. Research on monolithic inductors nevertheless continues.

The frequency tuning range of the LC-tank VCO is determined by the capacitance tuning range of the varactor in the VCO. VCO parasitics will deteriorate the effective tuning capabilities of the varactors. Further, process variations in the varactor itself and in the inductors need to be compensated. Therefore, the varactors with wide capacitance tuning range are required to guarantee specified center frequency and frequency tuning range. The varactor structures available in standard CMOS processes are p-n junction varactor and MOS structure varactors. The

capacitance value of the p-n junction varactor is controlled by the reverse-bias voltage. The technology scaling lowers the maximum circuit supply voltage and the maximum usable diode reverse-bias voltage. Therefore, the technology scaling decreases the capacitance tuning range of the p-n junction varactor. Tuning with the MOS structure varactors is the more promising approach. Strong capacitance variation within a few hundreds of millivolts makes the MOS structure varactors useful at low supply voltage [4].

1.2 Motivation

Most modern CMOS processes use a heavily-doped p+ substrate to minimize latch-up susceptibility. However, the low resistivity of the substrate (on the order of $0.1\,\Omega\cdot cm$) creates unwanted paths between various components in the same substrate, thereby corrupting sensitive components. Some people call this “substrate noise” because the unwanted signals from other components are a kind of noise. However, this noise has quite different physic meaning from the thermal noise, flicker noise, or shot noise.

Substrate noise resulting from other components, propagating in the substrate, and coupling to the varactors will affect the output spectrums of the VCOs. Of course, substrate noise also couples to the other constituent devices (transistors, and inductors) in the VCOs and thus influences the output spectrums. In this thesis, we focus on the influences of substrate noise coupling to the varactors on the output spectrums of the VCOs. The varactors fabricated on n-well can use the p-n junction between substrate and n-well to isolate substrate noise. Because of no isolation between p-well and substrate, it is obvious that the varactors fabricated on p-well are more sensitive to substrate noise. However, deep n-well can provide isolation between p-well and substrate for the varactors fabricated on p-well. In general, deep n-well is offered in

deep-submicrometer CMOS processes for better substrate noise isolation of p-well devices because of an additional p-n junction. Therefore, there are two types of isolation structure for varactors in standard CMOS processes (Fig. 1.3). In this thesis, the testkey-level method is used to verify which structure has better isolation capability by comparing the measured S_{21} parameters. The details of the testkey-level method are described in chapter 3. Furthermore, two 2.4GHz LC-tank VCOs (VCO1 and VCO2) are realized to investigate the influences of substrate noise coupling to the varactors on the output spectrums of the VCOs. VCO1 and VCO2 differ only in the type of varactor: n-type MOS varactor (VCO1) and NMOS varactor with deep n-well (VCO2). An RF signal injected into the substrate as substrate noise is provided by signal generator. The RF signal is injected into the substrate through the p+ ring surrounding the varactors. The details are described in chapter 5.

1.3 Organization of This Thesis

This thesis is organized as follows. In chapter 2, four types of MOS structure varactor are realized and the high-frequency characteristics of them are compared. In chapter 3, two testkeys corresponding to different isolation structures are designed to verify which structure has better isolation capability. The measured S_{21} parameters of the testkeys are shown. In chapter 4, design considerations for LC-tank VCO are discussed. In chapter 5, Three 2.4GHz LC-tank VCOs (VCO1, VCO2, and VCO3) are designed and realized in a 0.25-um CMOS process. VCO1 and VCO2 are realized to investigate the influence of substrate noise coupling to the varactors on the output spectrums. VCO3 adopting complementary topology is designed to compare with VCO1 adopting PMOS-only topology. The phase noise of them is compared. In chapter 6, the conclusions and future works are given.

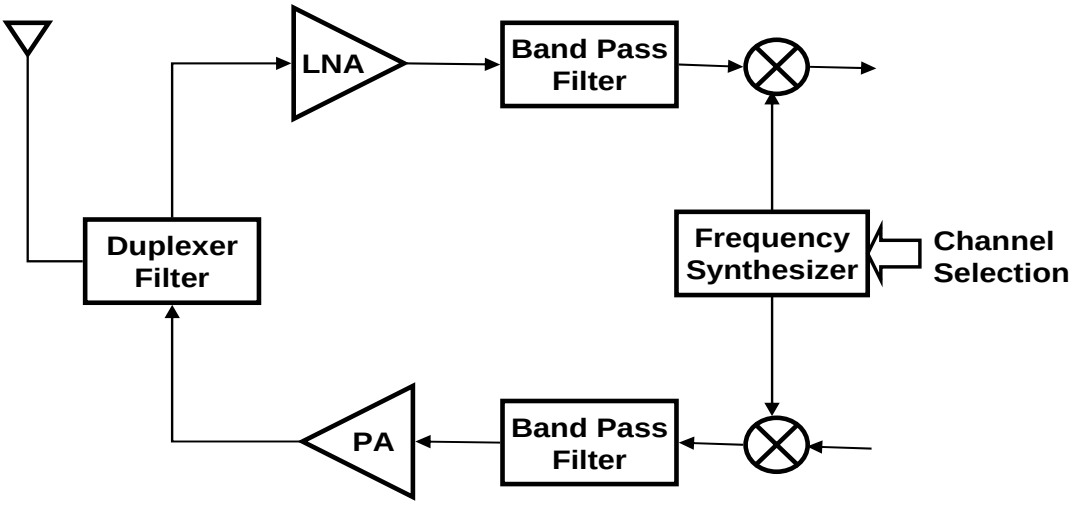


Fig. 1.1 Generic transceiver architecture.

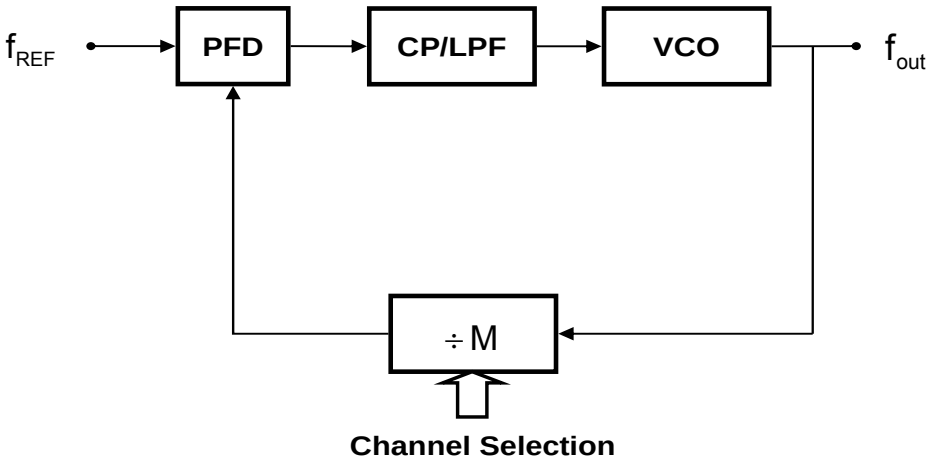
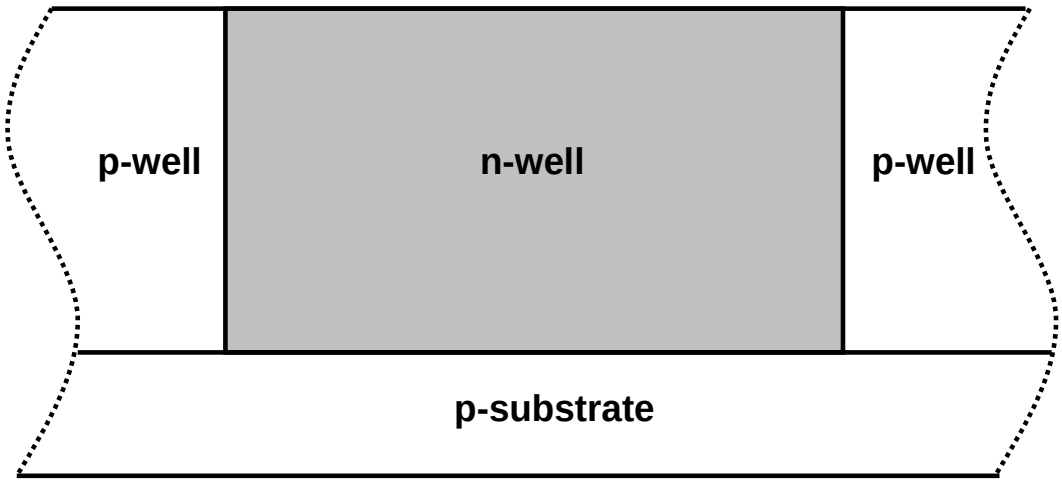
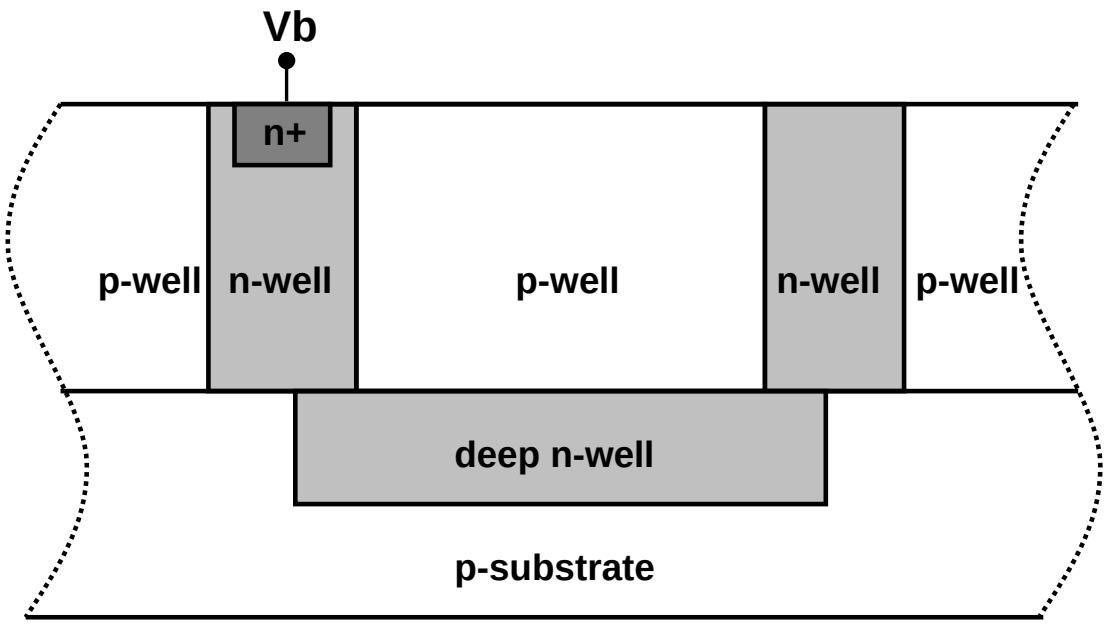


Fig. 1.2 Basic phase-locked frequency synthesizer.



(a)



(b)

Fig. 1.3 (a) Isolation structure for varactors fabricated on n-well and (b) Isolation structure for varactors fabricated on p-well with deep n-well.

Chapter 2

High-Frequency Characteristics of Varactors

2.1 Varactor Structures

2.1.1 General Considerations

Design considerations for varactors are summarized as follows [5]:

(1) A high quality factor.

(2) A control voltage range compatible with the supply voltage, ultimately 1 V for single battery cell operation.

(3) A good tunability over the available control voltage range.

(4) A small silicon area, to reduce cost.

(5) A reasonably uniform capacitance variation over the available control voltage range, to make the phase-locked-loop design easier.

Two classes of devices have to be considered: junction structure and MOS (metal-oxide-semiconductor) structure varactors, the latter tuning the capacitance by changing the operation regions (accumulation region, inversion region, and depletion region). In all cases, the devices should be placed in separated wells in order to use the p-n junction between substrate and n-well to isolate substrate noise. The five types of device are therefore p-n junction varactor, n-type MOS varactor (accumulation mode), p-type MOS varactor with deep n-well (accumulation mode), NMOS varactor with deep n-well, and PMOS varactor. The details are described as follows.

2.1.2 P-N Junction Varactor

The cross section of p-n junction varactor is shown in Fig. 2.1. The p-n junction used as varactor must be operated in reverse-biased region and the capacitance value

is controlled by the reverse voltage.

2.1.3 N-type MOS Varactor

The cross section of n-type MOS varactor (accumulation mode) is shown in Fig. 2.2. This structure is widely used as varactor in standard CMOS processes. The device capacitance is given by $C = C_0 WL$, where C_0 is given by

$$C_0 = \left(\frac{1}{C_{OX}} + \frac{1}{C_d} \right)^{-1}, \tag{2.1}$$

in which C_{OX} and C_d are, respectively, the oxide capacitance and the capacitance of the depletion layer under the gate, per unit area. By applying a positive voltage between the gate (V_{gate}) and the source/drain (V_{cont}) the surface is accumulated and the device capacitance equals the oxide capacitance. If the applied voltage is reversed, the surface layer is depleted and the series capacitance decreases. The maximum capacitance (C_{max}), per unit area, of the device corresponds to a heavily accumulated surface and equals $C_{OX} = \varepsilon / t_{OX}$. On the other side, a minimum value (C_{min}) is reached when the voltage difference between the electrodes equals the threshold voltage. Beyond this point, an inversion layer is formed under the gate. At low frequency this effect brings the value of the device capacitance close to the gate oxide capacitance. At high frequency, where the varactor is assumed to be operated, this effect is not seen and the device capacitance remains at its minimum value. The ratio between C_{max} and C_{min} defines the tuning range [4].

2.1.4 P-type MOS Varactor with Deep N-well

The cross section of p-type MOS varactor with deep n-well (accumulation mode) is shown in Fig. 2.3. Deep n-well and n-well surrounding the p-well isolate this device from substrate noise. By applying a negative voltage between the gate (V_{gate})

and the source/drain (V_{cont}) the surface is accumulated and the device capacitance equals the oxide capacitance. If the applied voltage is reversed, the surface layer is depleted and the series capacitance decreases. The maximum capacitance (C_{max}), per unit area, of the device corresponds to a heavily accumulated surface and equals $C_{OX} = \varepsilon / t_{OX}$. On the other side, a minimum value (C_{min}) is reached when the voltage difference between the electrodes equals the threshold voltage. Beyond this point, an inversion layer is formed under the gate. At low frequency this effect brings the value of the device capacitance close to the oxide one. At high frequency, where the varactor is assumed to be operated, this effect is not seen and the device capacitance remains at its minimum value.

This device has the advantage of a lower parasitic resistance than n-type MOS varactor mentioned in section 2.1.3.

2.1.5 NMOS Varactor with Deep N-well

The cross section of NMOS varactor with deep n-well is shown in Fig. 2.4. Deep n-well and n-well surrounding the p-well isolate this device from substrate noise. This device is a three-terminal device. These three terminals are gate (V_{gate}), source/drain (V_{cont}), and bulk respectively. The device capacitance is relative to not only the voltage difference between gate and bulk but also the bias voltage of source/drain. It should be noted that, with floating source/drain terminal and using bulk terminal as control voltage node, this device can work like p-type MOS varactor with deep n-well mentioned in section 2.1.4.

2.1.6 PMOS Varactor

The cross section of PMOS varactor is shown in Fig. 2.5. This device works in the strong, moderate, or weak inversion region only, and never enters the

accumulation region. Since the bulk is connected to the power supply V_{DD}, the device does not enter the accumulation region and remains in the weak inversion region for a very wide range of positive voltage between the gate (V_{gate}) and the source/drain (V_{cont}) [6]. When the voltage difference between the gate and the source/drain is smaller than the threshold voltage, the device enters the strong inversion region and the device capacitance, per unit area, equals $C_{OX} = \varepsilon / t_{OX}$.

2.1.7 Discussion on Varactors

Since the p-n junction varactor is realized in an n-well isolated from the substrate, both ports can be biased above ground. When the p-n junction varactor is used in a VCO circuit, the p+ contact must be connected to the "signal" electrode and the n+ contact must be connected to the "control voltage" electrode to get rid of the n-well to substrate capacitance.

When MOS structure varactors are used in a VCO circuit, the gate (V_{gate}) must be connected to the "signal" electrode and the source/drain (V_{cont}) must be connected to the "control voltage" electrode to get rid of the effect of the parasitic capacitance seen from the source/drain node to AC ground node. For n-type MOS varactor, the parasitic capacitance is the n-well to substrate capacitance. For NMOS varactor with deep n-well, the parasitic capacitance is the n+ contact to bulk capacitance. For PMOS varactor, the parasitic capacitance is the p+ contact to bulk capacitance. For p-type MOS varactor with deep n-well, the parasitic capacitance is the p-well to deep n-well and surrounding n-well capacitance.

Since the swings at "signal" electrodes of VCOs are typically large, the capacitance of varactors varies with time. Nonetheless, the "average" value of the capacitance is still a function of the control voltage. However, the capacitance variation over each oscillation period results in harmonic distortion of the oscillator

sine.

For MOS structure varactors, the variable capacitance between the gate (V_{gate}) and the source/drain (V_{cont}) is the series connection of the gate oxide capacitance and the depletion region capacitance. The parasitic capacitances between the gate (V_{gate}) and the source/drain (V_{cont}) are mainly overlap and fringing capacitances. They are assumed to be constant and parallel to the variable capacitance. Then the capacitance tuning range is given as

$$C_{ratio} = \frac{C_{max}}{C_{min}} = \frac{C_{variable,\,max} + C_{parasitic}}{C_{variable,\,min} + C_{parasitic}}. \qquad (2.2)$$

It is obvious that the parasitic capacitances of the varactor deteriorate the capacitance tuning range and therefore the frequency tuning range of the VCO. The C_{max}/C_{min} ratio can increase by increasing the channel length of MOS structure varactors, if the gate area remains the same (at the expense of a lower Q).

The p-n junction varactor suffers from a drawback: the technology scaling lowers the maximum circuit supply voltage and the maximum usable reverse voltage. However, for the MOS structure varactors, the oxide thickness is reduced and correspondingly the oxide capacitance is increased with the technology scaling. On the other hand, the value of the depletion capacitance underneath the gate, for a given biasing condition, increases at a lower rate. This means that the tuning range is expected, to a first order, to increase with scaling. Moreover, scaled technologies enable to realize MOS structure varactors with better quality factors because the parasitic resistance scales with the channel length [4].

2.2 Layout Designs

As mentioned in section 2.1.7, the p-n junction varactor suffers from a drawback with the technology scaling. Therefore, the p-n junction varactor is not

taken into consideration in this thesis.

All previously discussed MOS structure varactors are realized in a 0.25-um CMOS process. In order to facilitate the comparison among these MOS structure varactors, they all have the same size: L x W x S x B x G=1um x 5um x 1 x 6 x 6, and thus equal gate area. The layout of test structure of n-type MOS varactor is shown in Fig. 2.6. The layout of test structure of p-type MOS varactor with deep n-well is shown in Fig. 2.7. The layout of test structure of NMOS varactor with deep n-well is shown in Fig. 2.8. The layout of test structure of PMOS varactor is shown in Fig. 2.9.

N-type MOS varactor with the size: L x W x S x B x G=1um x 5um x 1 x 6 x 6, is available in the given 0.25-um CMOS process. Thus, for n-type MOS varactor, the measured results can be compared with ADS simulated results. For n-type MOS varactor, the RF model provided by the given 0.25-um CMOS process is capable of describing the behavior in all regions of operation from 100MHz to 20.1GHz.

2.3 Measurement Setup

The measurement of test devices has been done by microwave wafer probing on a bare silicon die (on-wafer measurement) to avoid bond wire, package, and fixture effects. Before an accurate measurement can be made, the test system must first be calibrated. With the impedance standard substrate (ISS), SOLT calibration method has been done to calibrate the test system errors.

Two-port S-parameter measurements are performed from 100MHz to 10GHz by using probe station and HP8510 network analyzer. The ports are defined by the gate (V_{gate}) and the source/drain (V_{cont}) terminals. An additional measurement on the OPEN structure has been carried out to de-embed the pad effects.

2.4 Pad De-Embedding

2.4.1 Pad De-Embedding Procedure

The test structures of these four devices shown in Fig. 2.6~Fig. 2.9 not only consist of the actual device-under-test (DUT), but also of parasitic components that largely influence the electrical behavior of the DUT. The parasitic components mainly originate from the contact pads, which connect the RF measurement probes and the silicon wafer. As shown in Fig. 2.10, the parasitic components originating from the contact pads are capacitors and resistors in parallel with the DUT. In order to model the RF behavior of the DUT accurately, the influence of the parasitic components must be subtracted from the measurements on the test structures. The procedure to get rid of the influence of the on-wafer parasitic components is called pad de-embedding. Contrary to III-V technologies which are manufactured on isolating substrates, the pad parasitic in silicon-based RF test structures is very difficult to calculate accurately by electromagnetic simulations. Therefore, an on-wafer de-embedding method for silicon-based technologies is essential.

All the MOS structure varactors need respective OPEN structures to de-embed the parasitic components originating from the contact pads. The pad de-embedding steps can be summarized as follows.

(1) Measure the S-parameters of the OPEN structure and convert them to Y-parameters.

(2) Measure the S-parameters of the DUT test structure and convert them to Y-parameters.

(3) Subtract the Y-parameters of the OPEN structure from that of the DUT test structure, and then the result is the de-embedded Y-parameters.

The de-embedded Y-parameters can be used to calculate the value of the components in equivalent circuit model. The details are described in section 2.5.

Conversion between Y-parameters and S-parameters is as follows.

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} Y_0 . \quad (2.3)$$

$$Y_{12} = \frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} Y_0 . \quad (2.4)$$

$$Y_{21} = \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} Y_0 . \quad (2.5)$$

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} Y_0 . \quad (2.6)$$

Y_0 is the characteristic admittance.

2.4.2 Discussion on Pad De-Embedding Methods

The pad de-embedding method used in this thesis is known as Y-parameter subtraction technique, in which the parasitic components in series with the DUT are assumed negligible. Thus, the parasitic components in series with the DUT are not presented in the equivalent circuit of the test structure shown in Fig. 2.10. The complete equivalent circuit of the test structure is shown in Fig. 2.11. The parasitic components in series with the DUT originate from the metal interconnections between the contact pads and the DUT. Y-parameter subtraction technique can de-embed the parasitic components in parallel with the DUT, but it can't de-embed the parasitic components in series with the DUT. At low frequency, the total impedance of the parasitic components in series with the DUT (not be de-embedded) is much less than that of the DUT. However, for high frequency measurement, the effects of the parasitic components in series with the DUT (not be de-embedded) become significant.

Fig. 2.12~Fig. 2.15 shows the measured and simulated C_S of n-type MOS varactor at 100MHz, 2.5GHz, 5GHz, and 10GHz respectively. C_S is the equivalent series capacitance as described in section 2.5. Of course, the simulated C_S is dependent of frequency due to the intrinsic parasitic inductive effect of the DUT (Fig.

2.16) [7]. Fig. 2.17 shows the measured and simulated Q of n-type MOS varactor at 2.5GHz. All the simulated results are produced by S-parameter simulation in ADS.

Due to Y-parameter subtraction technique, it should be noted here that the measured C_S and Q contain the effects of the parasitic components in series with the DUT. The difference between the measured results and the simulated results is mainly attributed to the effects of the parasitic components in series with the DUT. The measured C_S is strongly different from the simulated C_S at 10GHz. However, at 100MHz and 2.5GHz, the difference is much smaller.

An advanced pad de-embedding method called three-step de-embedding method [8] [9] can de-embed both the parasitic components in series with the DUT and the parasitic components in parallel with the DUT. The layout of the test structure with the DUT and the corresponding on-wafer de-embedding structures: open, short1, short2, and through, are shown in Fig. 2.18.

2.5 Equivalent Circuit Model

All these four MOS structure varactors are modeled by equivalent series $R_S - C_S$ circuit between port1 (V_{gate}) and port2 (V_{cont}). Using the de-embedded Y-parameters, the impedance between port1 and port2 can be calculated easily at each operating point and frequency as $Z = \frac{1}{Y_{11}}$. Impedance Z can be written as

$$Z = R_S + \frac{1}{j\omega C_S}. \tag{2.7}$$

R_S, C_S and Q can be extracted as

$$R_S = \mathrm{Re}(Z) \tag{2.8}$$

$$C_S = \frac{-1}{\omega \cdot \mathrm{Im}(Z)} \tag{2.9}$$

$$Q = \left|\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}\right| = \frac{1}{\omega C_S R_S}. \tag{2.10}$$

2.6 Measurement Results

The measured C_S of these four MOS structure varactors at 2.5GHz are shown respectively in Fig. 2.19~Fig. 2.22. As shown in section 2.4.2, at low frequency (100MHz, and 2.5GHz), the effects of the parasitic components in series with the DUT (not be de-embedded) result in small difference between the measured C_S and the real C_S. However, the difference between the measured Q and the real Q is obvious. Therefore, the measured Qs of these four MOS structure varactors don't make sense and are not shown.

The comparison of the measured characteristics among these MOS structure varactors is shown in Table 2.1. As shown in Table 2.1, PMOS varactor has the largest capacitance tuning range and the best area efficiency.

Since the signal swings in the VCOs are large, the instantaneous value of C_S changes throughout the signal period. The effective capacitance of the varactor is average over each period. It is not sufficient to predict the frequency tuning ranges of the VCOs by considering only the absolute maximum and minimum values of C_S. The frequency tuning curves of the VCOs depend on both the signal swings of the VCOs and the capacitance tuning curves of the varactors. For NMOS varactor with deep n-well, the nonmonotonicity of C_S shown in Fig. 2.21 will impair the tuning capability of the VCOs.

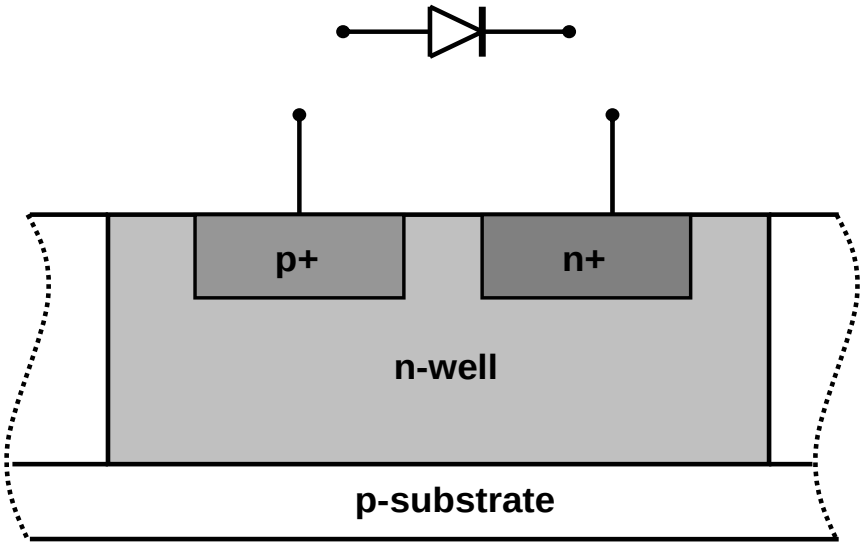


Fig. 2.1 Cross section of p-n junction varactor.

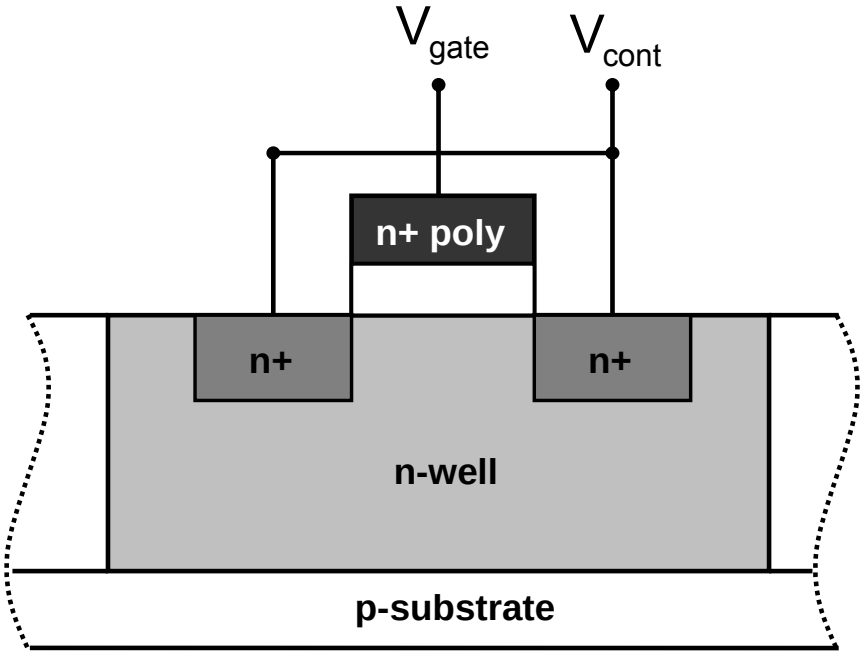


Fig. 2.2 Cross section of n-type MOS varactor.

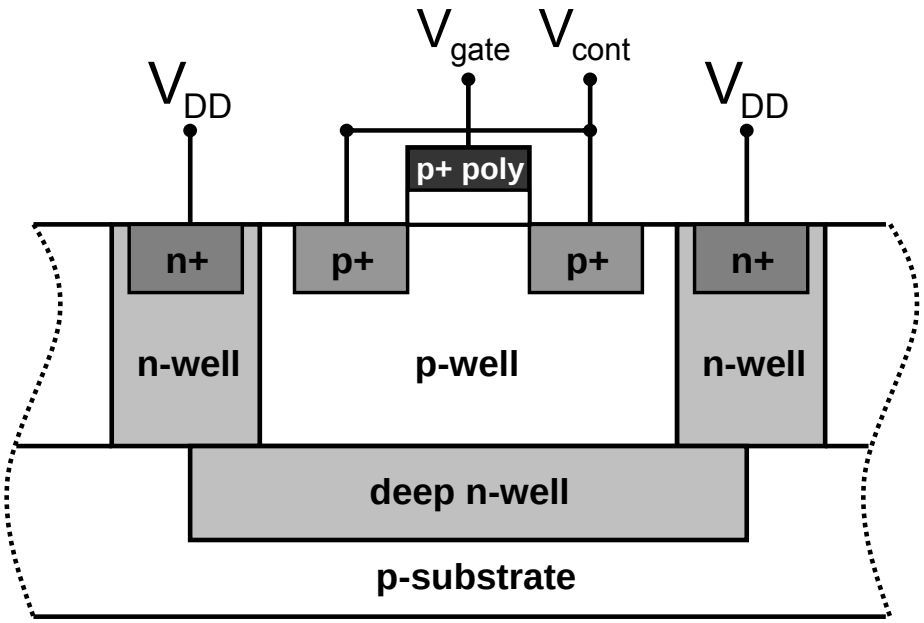


Fig. 2.3 Cross section of p-type MOS varactor with deep n-well.

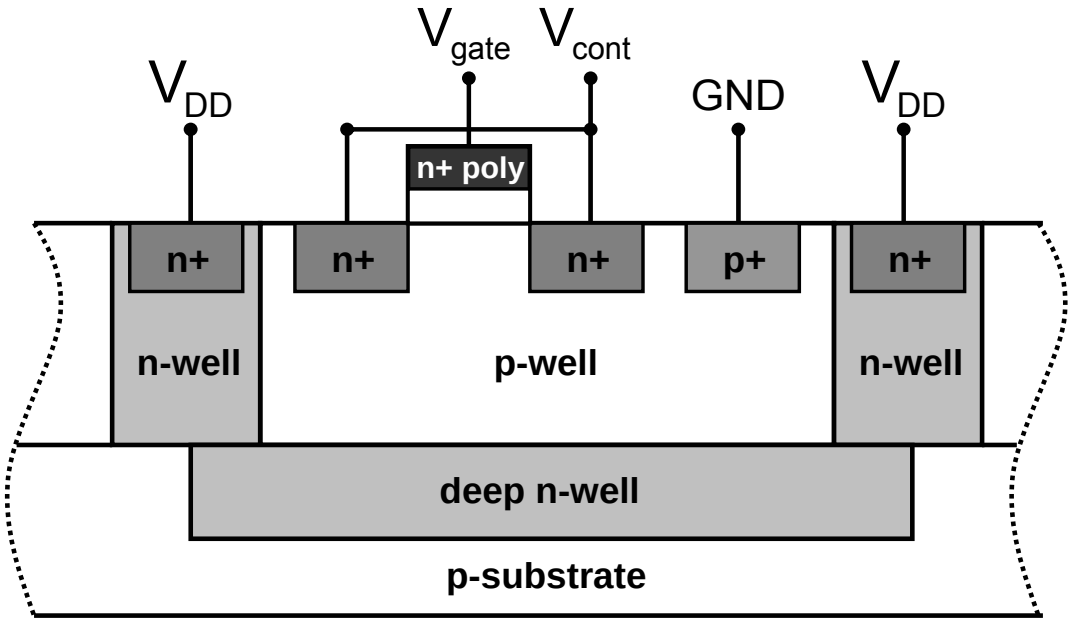


Fig. 2.4 Cross section of NMOS varactor with deep n-well.

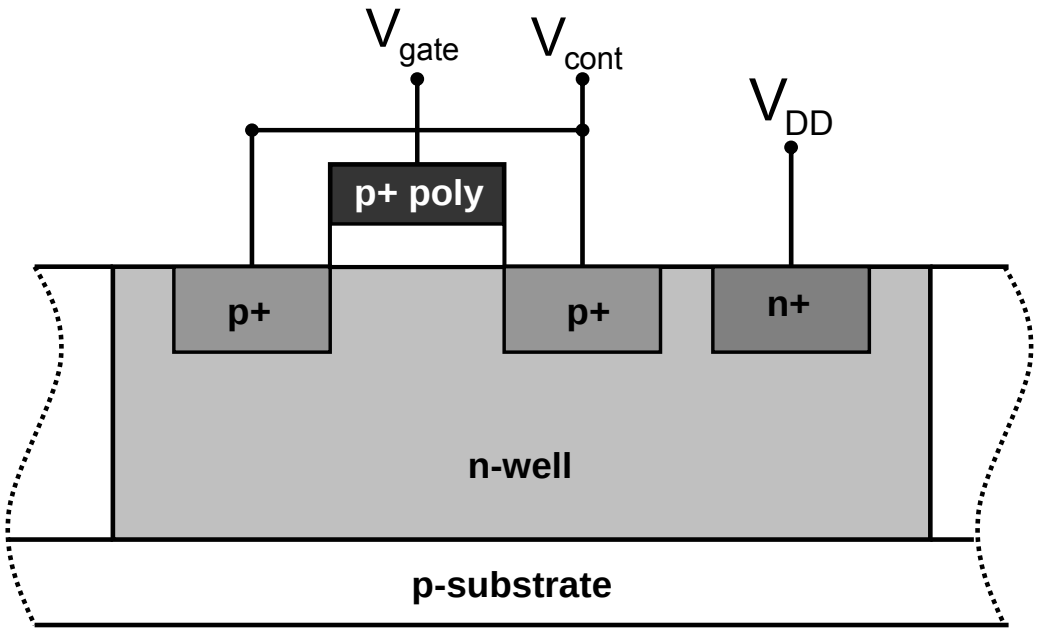


Fig. 2.5 Cross section of PMOS varactor.

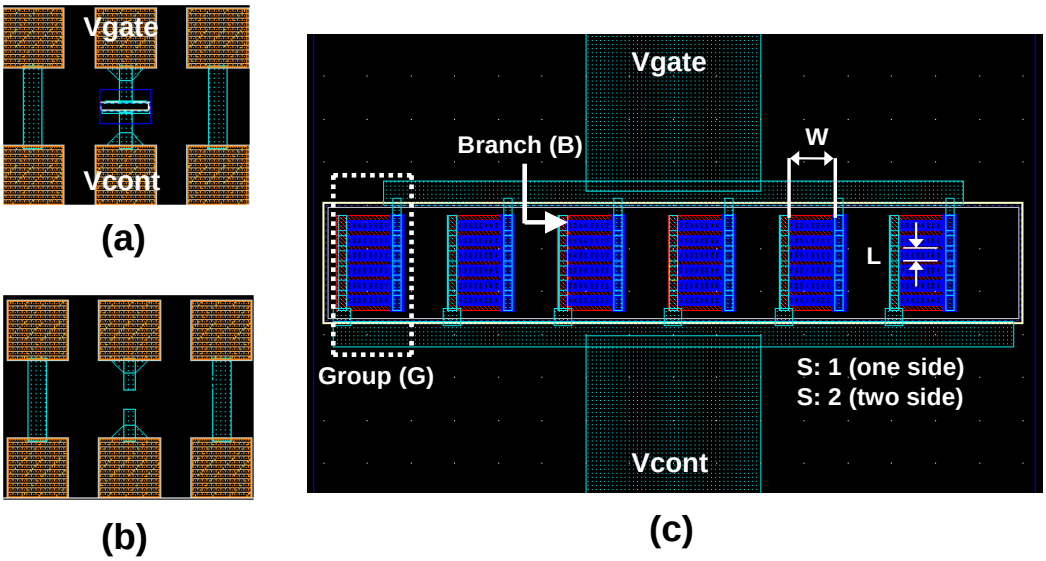


Fig. 2.6 The layouts of (a) test structure of n-type MOS varactor, (b) the corresponding de-embedding OPEN structure, and (c) the device.

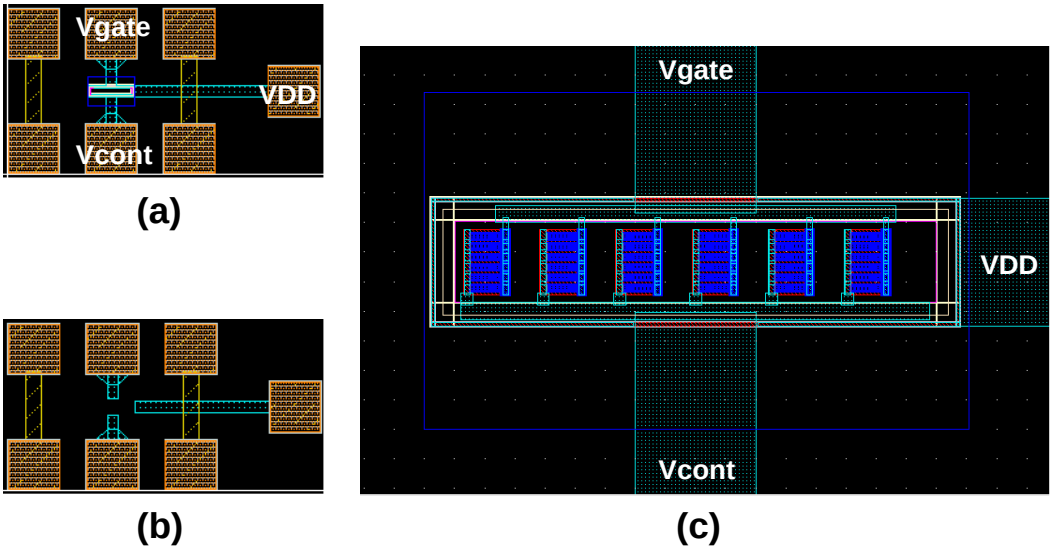


Fig. 2.7 The layouts of (a) test structure of p-type MOS varactor with deep n-well, (b) the corresponding de-embedding OPEN structure, and (c) the device.

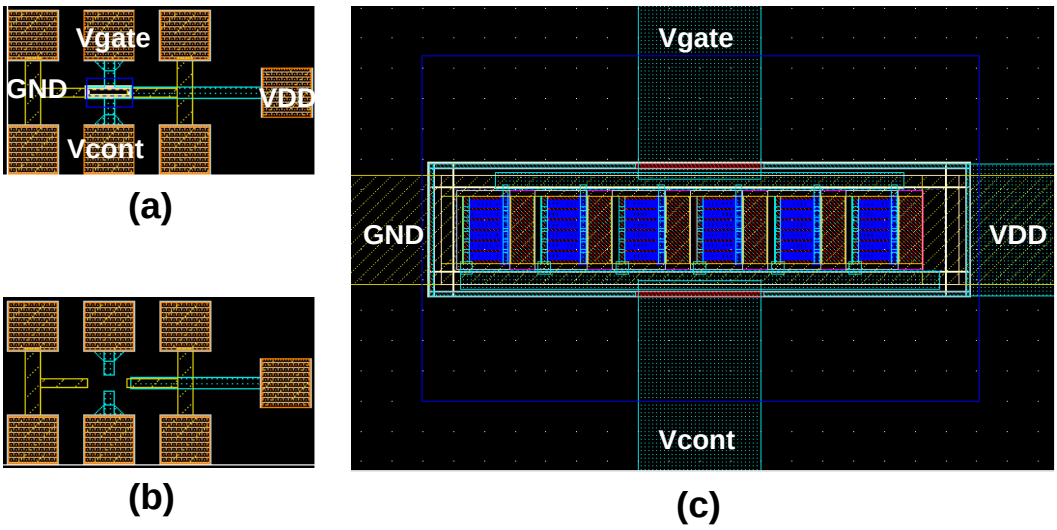


Fig. 2.8 The layouts of (a) test structure of NMOS varactor with deep n-well, (b) the corresponding de-embedding OPEN structure, and (c) the device.

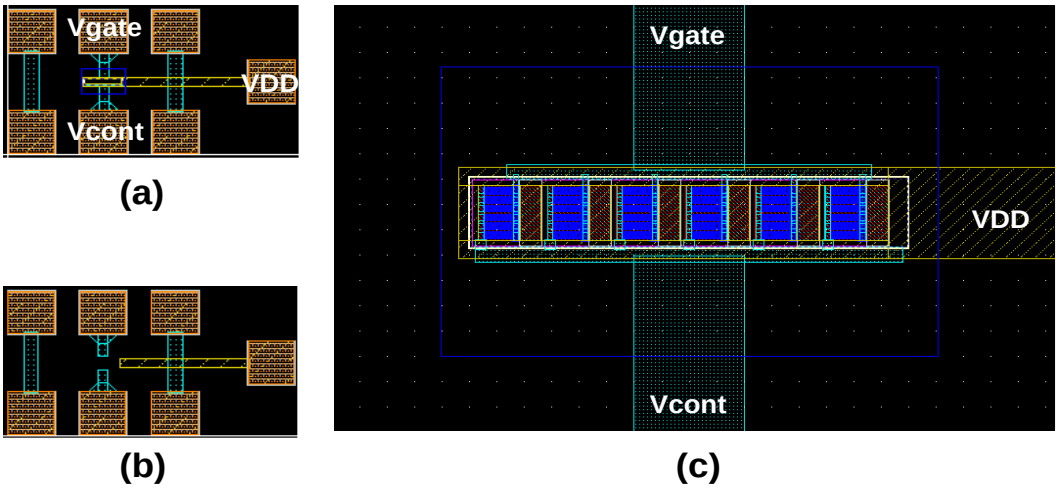


Fig. 2.9 The layouts of (a) test structure of PMOS varactor, (b) the corresponding de-embedding OPEN structure, and (c) the device.

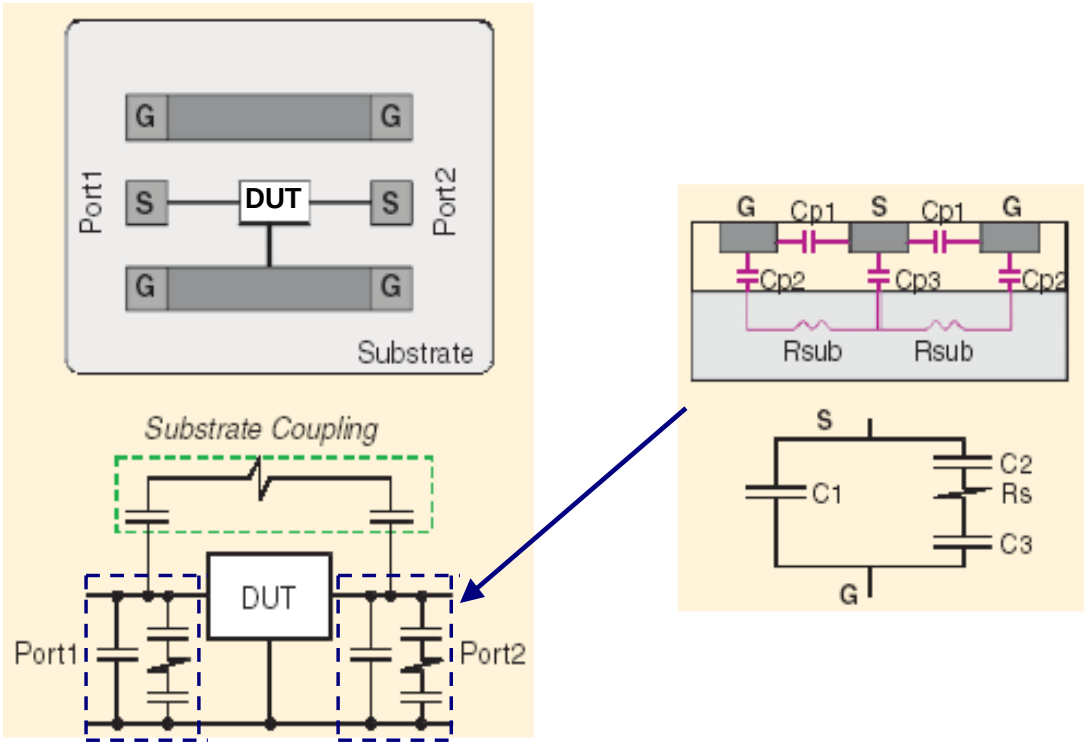


Fig. 2.10 The parasitic components originating from the contact pads.

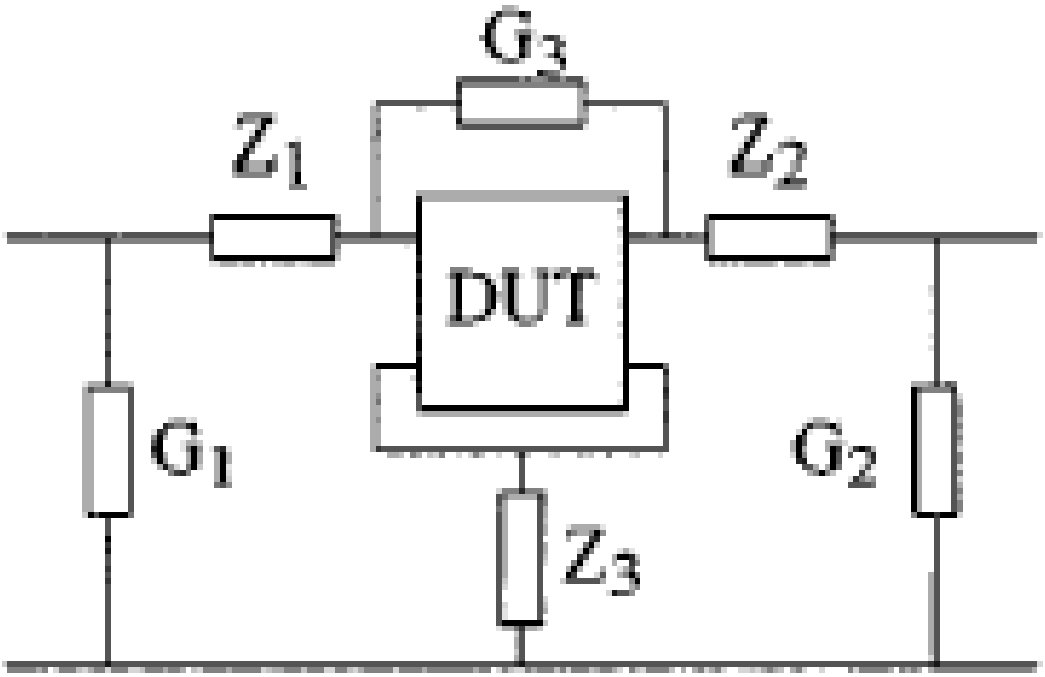


Fig. 2.11 The complete equivalent circuit of the RF test structure [8][9].

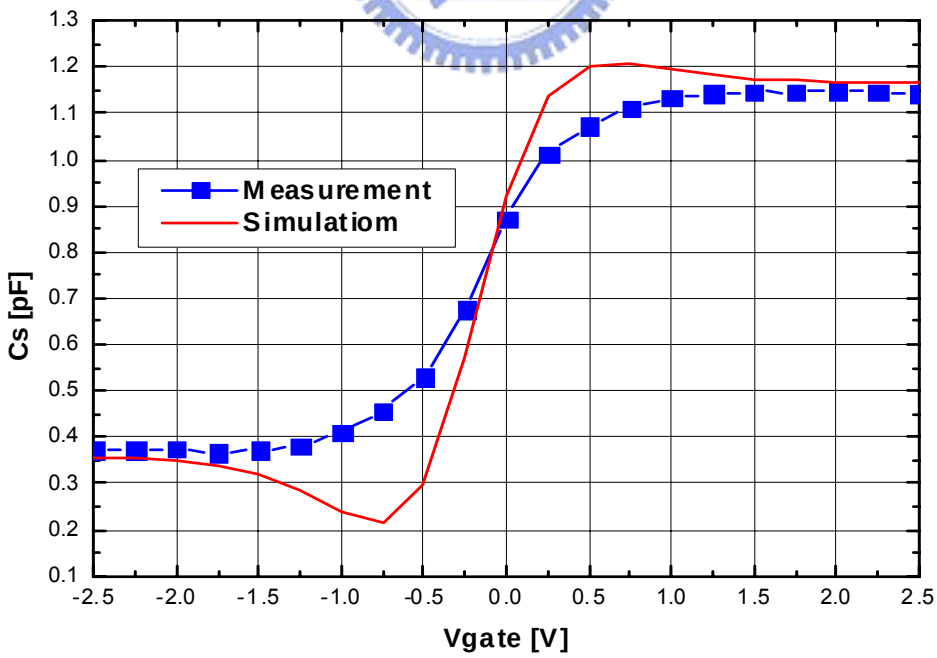


Fig. 2.12 The measured Cs and the simulated Cs of n-type MOS varactor at 100MHz.

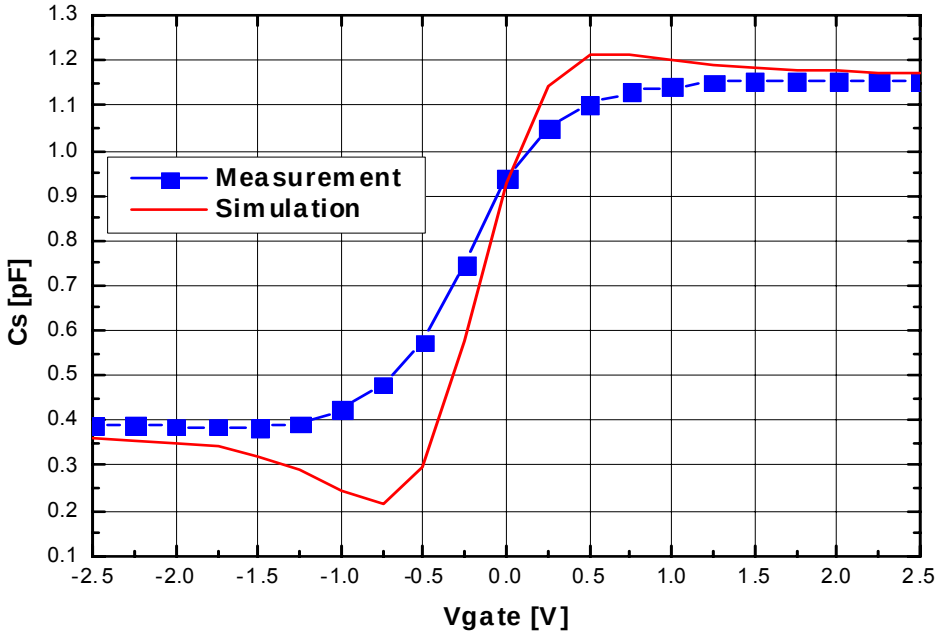


Fig. 2.13 The measured Cs and the simulated Cs of n-type MOS varactor at 2.5GHz.

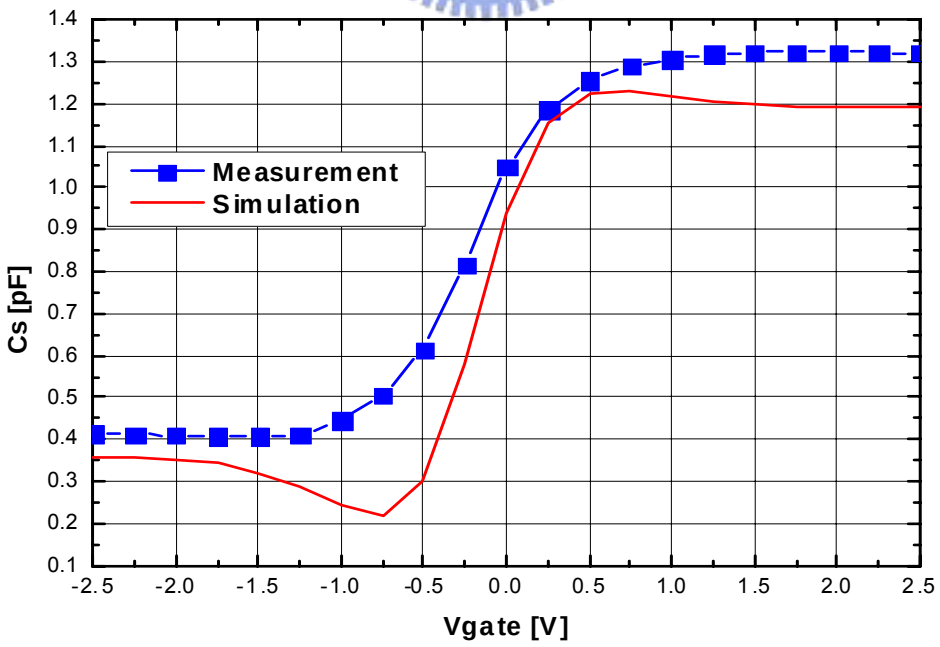


Fig. 2.14 The measured Cs and the simulated Cs of n-type MOS varactor at 5GHz.

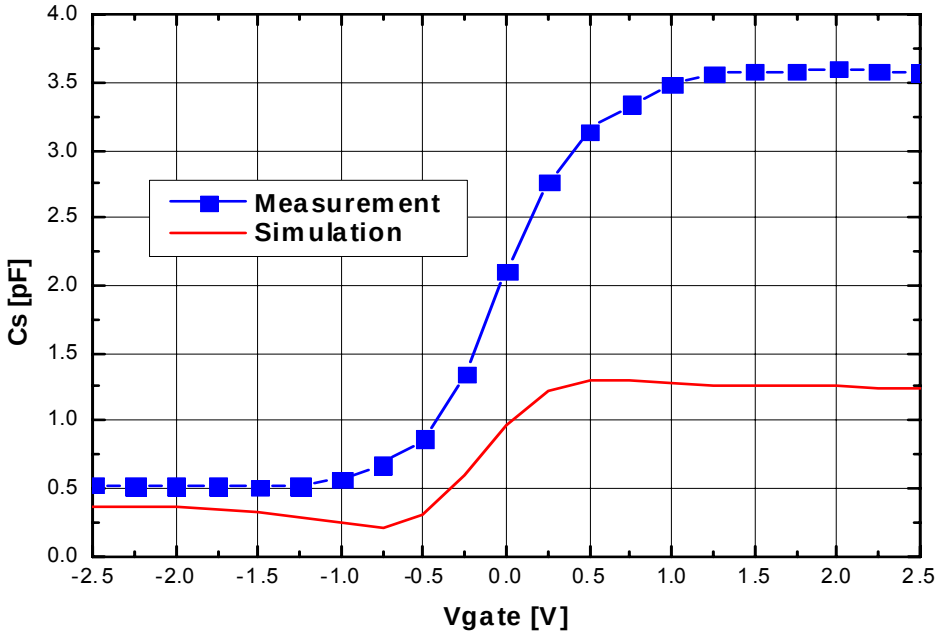


Fig. 2.15 The measured Cs and the simulated Cs of n-type MOS varactor at 10GHz.

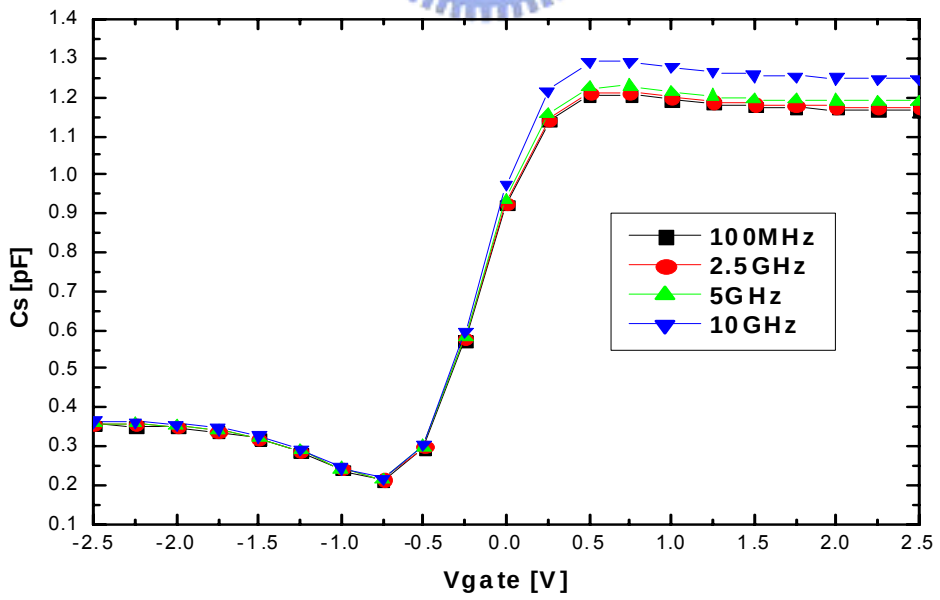


Fig. 2.16 The simulated Cs of n-type MOS varactor at 100MHz, 2.5GHz, 5GHz, and 10GHz respectively.

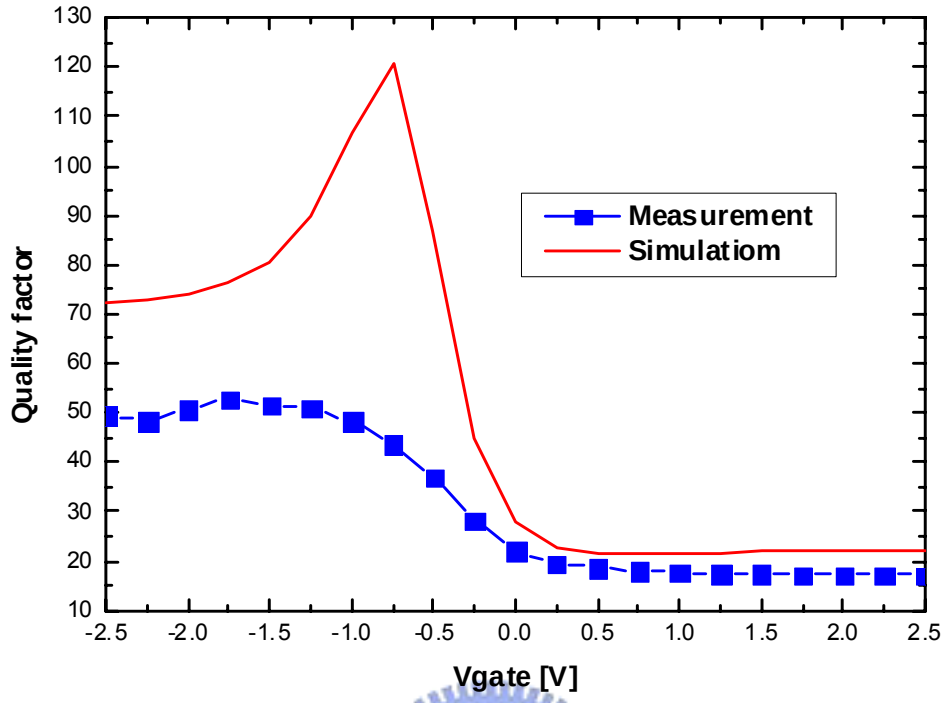


Fig. 2.17 The measured Q and the simulated Q of n-type MOS varactor at 2.5GHz.

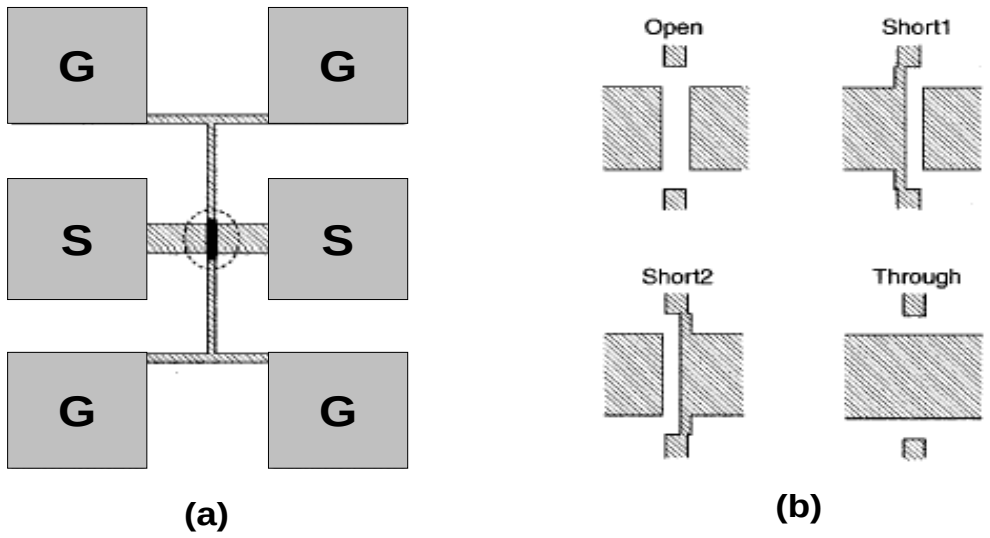


Fig. 2.18 (a) The layout of the test structure with the DUT. (b) Magnified view of the layout of the de-embedding structures. The pad layout and interconnection layout are equal to the test structure.

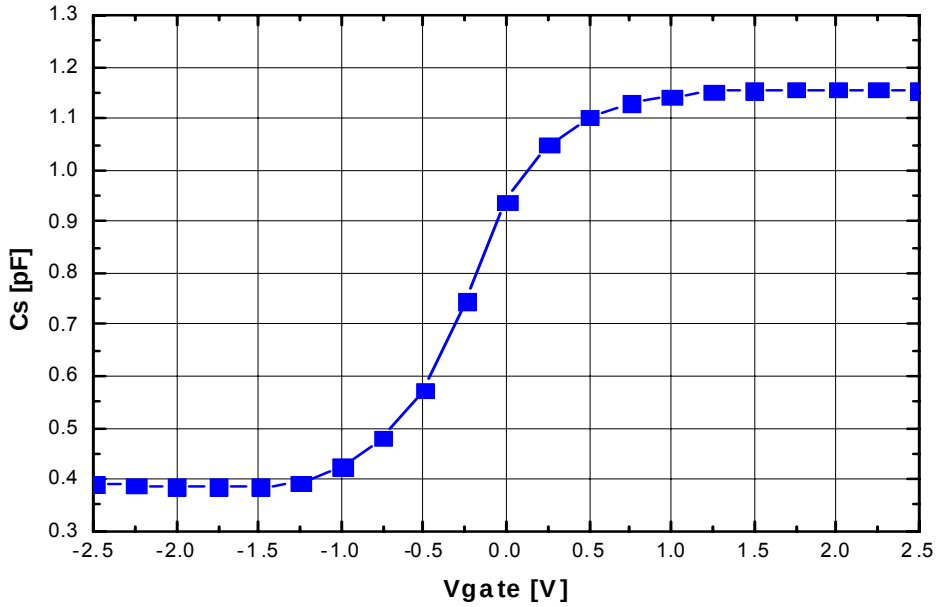


Fig. 2.19 The measured Cs of n-type MOS varactor at 2.5GHz.

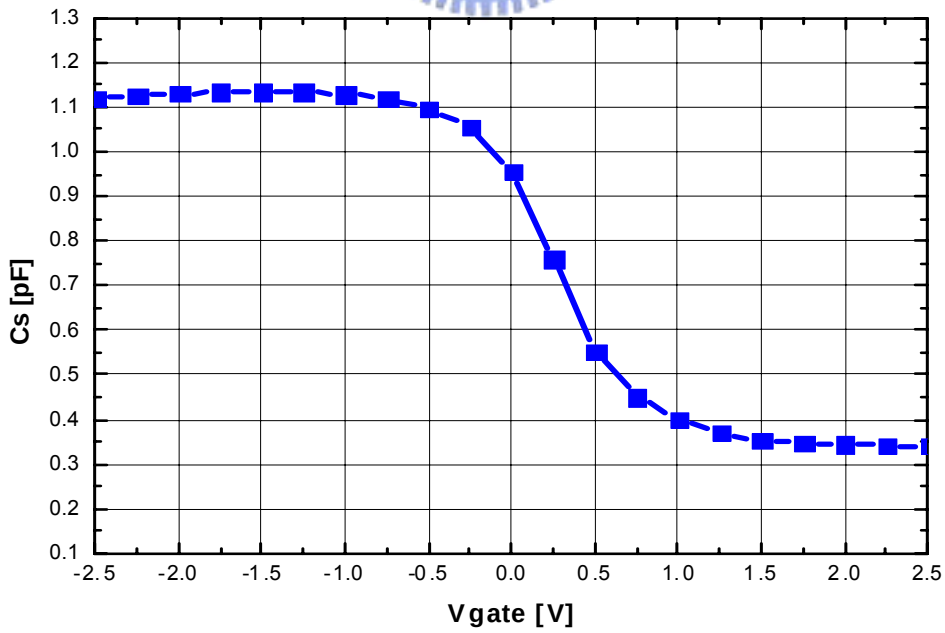


Fig. 2.20 The measured Cs of p-type MOS varactor with deep n-well at 2.5GHz.

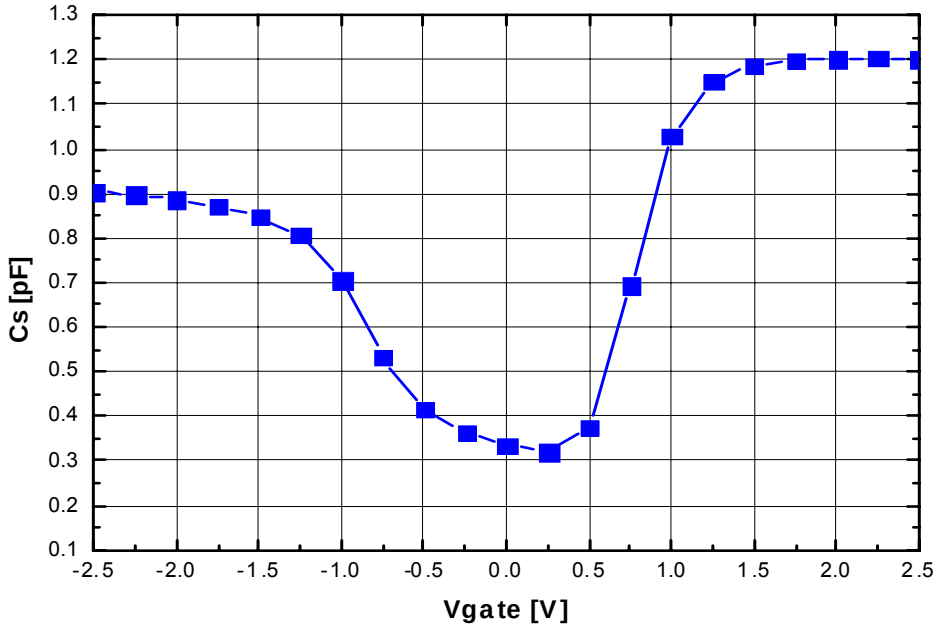


Fig. 2.21 The measured Cs of NMOS varactor with deep n-well at 2.5GHz.

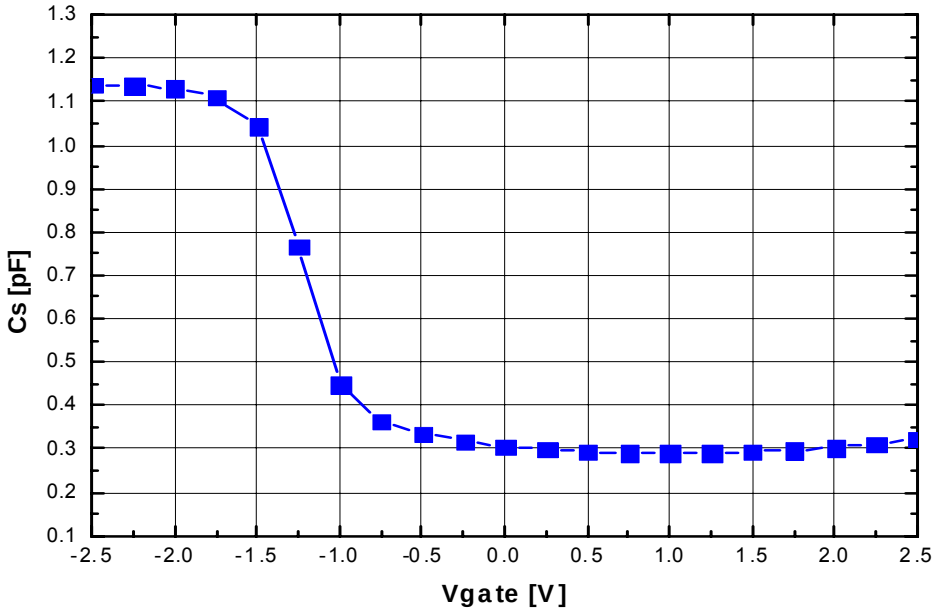


Fig. 2.22 The measured Cs of PMOS varactor at 2.5GHz.

Table 2.1 The comparison of the measured characteristics of different MOS structure varactors.

	$C_{s,min}$ (pF)	$C_{s,max}$ (pF)	$\frac{C_{s,max}}{C_{s,min}}$	well area (um^2)
n-type MOS varactor	0.3853	1.156	3	1121.2203
p-type MOS varactor with deep n-well	0.3403	1.134	3.33	1937.5403
NMOS varactor with deep n-well	0.3206	1.203	3.75	1937.5403
PMOS varactor	0.2914	1.139	3.91	1121.3604

Chapter 3

Substrate Noise Isolation Test

3.1 The Structures of Testkeys

All the MOS structure varactors mentioned in chapter 2 are placed in separate wells to isolate substrate noise. N-type MOS varactor and PMOS varactor fabricated on n-well use the p-n junction between n-well and substrate to isolate substrate noise. P-type MOS varactor with deep n-well and NMOS varactor with deep n-well are fabricated on p-well and surrounded by deep n-well and n-well in order to isolate substrate noise. An experiment is designed to compare the isolation capability of these two structures. The isolation testkey corresponding to n-type MOS varactor and PMOS varactor is show in Fig. 3.1. The isolation testkey corresponding to NMOS varactor with deep n-well and p-type MOS varactor with deep n-well is show in Fig. 3.2. The source window and the receiver window are 20um x 20um p+ or n+ region connected to GSG pads by metal. The space between the source window and the receiver window is 50um. These two testkeys are realized in a 0.25-um CMOS process.

3.2 Measurement Results

The measured S_{21} parameters of the testkey shown in Fig. 3.1 are shown in Fig. 3.3. The n-well is biased at 0V, 1.25V, and 2.5V respectively. The measured S_{21} parameters of the testkey shown in Fig. 3.2 are shown in Fig. 3.4. The deep n-well is biased at 0V, 1.25V, 2.5V, and floating respectively. The isolation capability is determined by the value of the p-n junction capacitance between n-well and substrate. At higher frequency, it is more difficult to isolate substrate noise by p-n junction

between n-well and substrate, as shown in Figs. 3.3, and 3.4. Thus, the larger the voltage difference between n-well and substrate, the better the isolation capability is. The comparisons of the isolation capability of different isolation structures are presented in Fig. 3.5 and Fig. 3.6. At low frequency (<1GHz), the isolation structure shown in Fig. 3.2 has better isolation capability. However, these two isolation structures have almost equal isolation capability from 1GHz to 10GHz.

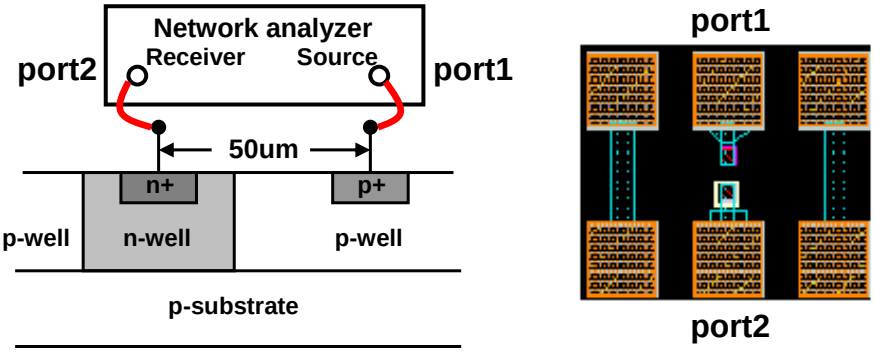


Fig. 3.1 The isolation testkey corresponding to n-type MOS varactor and PMOS varactor

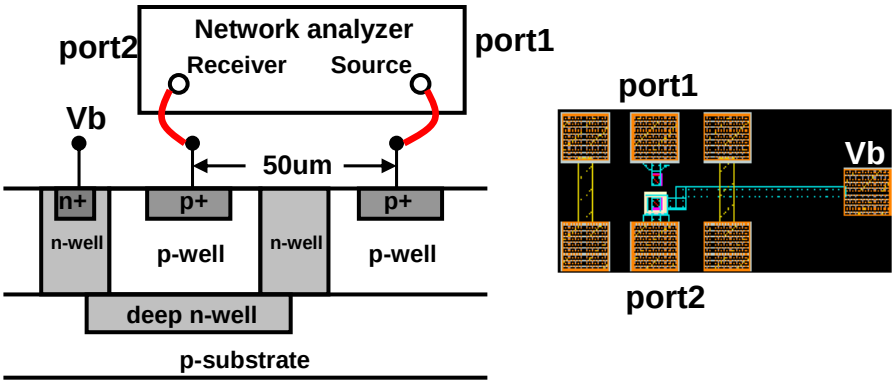


Fig. 3.2 The isolation testkey corresponding to p-type MOS varactor with deep n-well and NMOS varactor with deep n-well.

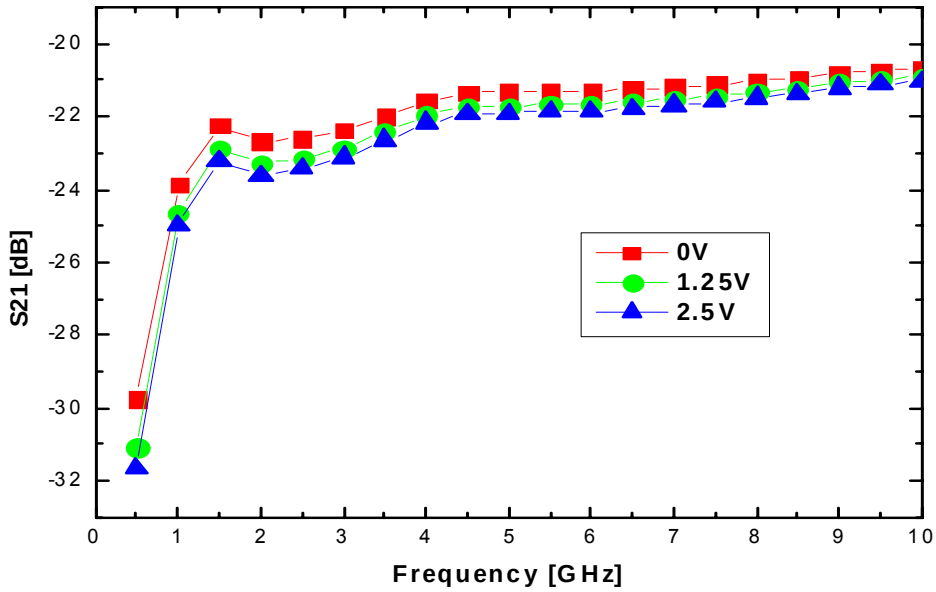


Fig. 3.3 The measured S_{21} parameters of the testkey shown in Fig. 3.1. The n-well is biased at 0V, 1.25V, and 2.5V respectively.

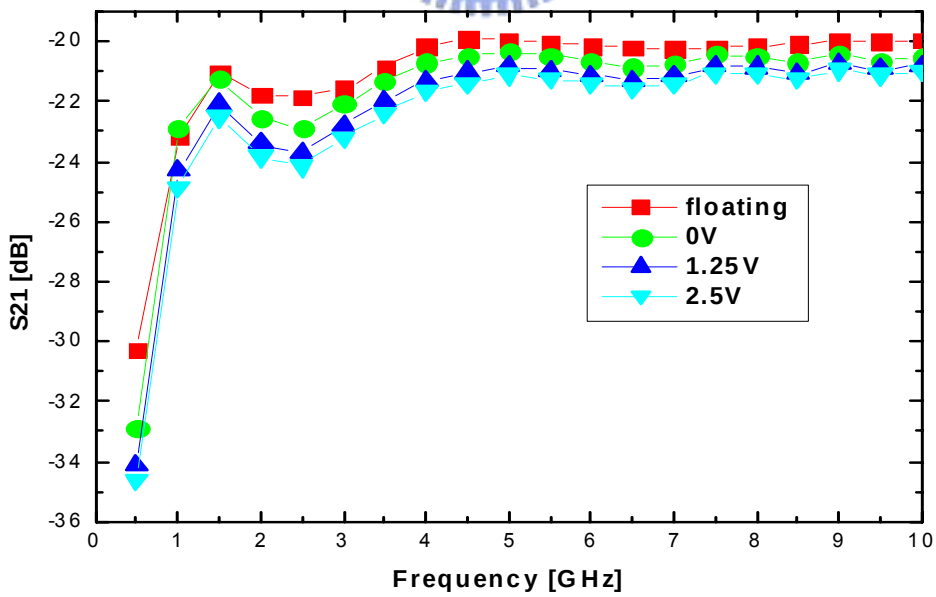


Fig. 3.4 The measured S_{21} parameters of the testkey shown in Fig. 3.2. The deep n-well is biased at 0V, 1.25V, 2.5V, and floating respectively.

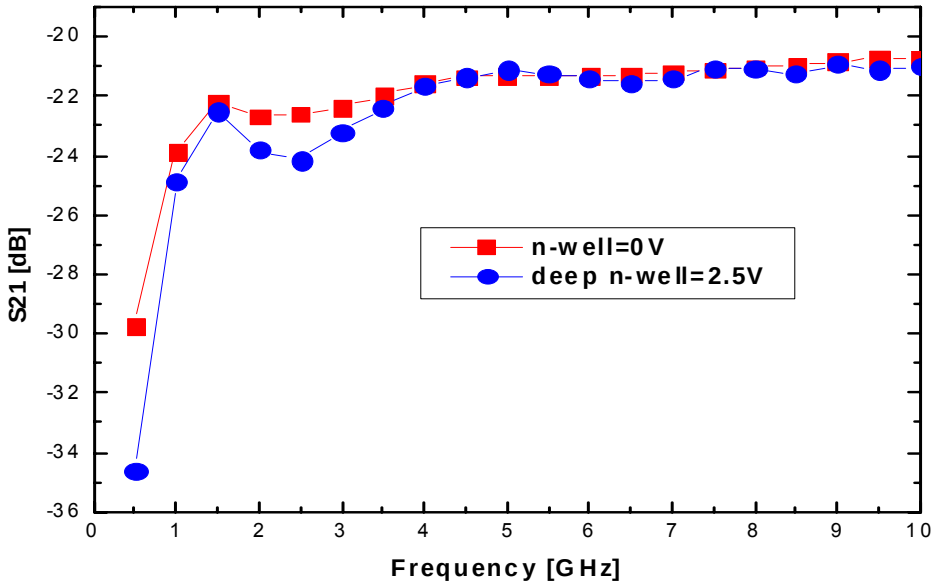


Fig. 3.5 The comparison of the isolation capability of different isolation structures. The n-well in Fig. 3.1 is biased at 0V. The deep n-well in Fig. 3.2 is biased at 2.5V.

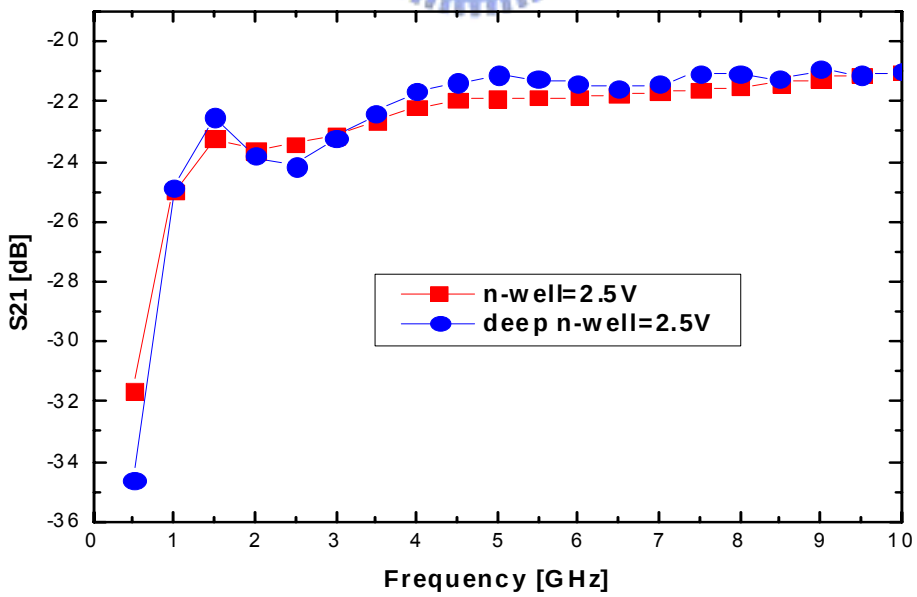


Fig. 3.6 The comparison of the isolation capability of different isolation structures. The n-well in Fig. 3.1 is biased at 2.5V. The deep n-well in Fig. 3.2 is biased at 2.5V.

Chapter 4

Design Considerations for LC-tank VCOs

4.1 LC-tank VCO Basics

Oscillators utilized in RF applications often fall in the feedback category (Fig. 4.1), but, where applicable, the one-port model can give additional insight into their operation. The “one-port model” treats the oscillator as two one-port networks connected to each other, as shown in Fig. 4.2(a). To understand this model, suppose the resonator is a simple tank, as shown in Fig. 4.2(b) along with its parasitic resistances. For a narrow band of frequencies, the circuit can be converted to the parallel combination depicted in Fig. 4.2(c). The tank by itself does not oscillate indefinitely because some of the stored energy is dissipated in R_P in every cycle. The idea in the one-port model is that an active network generates an impedance equal to $-R_P$ so that the equivalent parallel resistance seen by the intrinsic, lossless resonator is infinite. In essence, the energy lost in R_P is replenished by the active circuit in every cycle, allowing steady oscillation [10].

As the capacitor C in Fig. 4.2(c) is proportional to a tuning input voltage, the circuit results in a VCO with center frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{4.1}$$

The capacitor C in Fig. 4.2(c) not only consists of a variable capacitor to tune the oscillator, but it also includes the parasitic or fixed capacitances of the inductor, the active elements, and the load (output driver, mixer, prescaler, etc.). The self-sustaining effect allows the circuit’s noise to grow initially, but another mechanism is necessary to limit the growth at some point. To ensure oscillation start-up, the small-signal loop

gain must be somewhat greater than one, but to achieve stable amplitude, the "average" loop gain must return to unity.

4.2 Phase Noise

4.2.1 Definition

As other analog circuits, oscillators are susceptible to noise. Noise injected into an oscillator by its constituent devices or by external means may influence both the frequency and the amplitude of the output signal. In most cases, the disturbance in the amplitude is negligible or unimportant, and only the random deviation of the frequency is considered.

In RF applications, phase noise is usually characterized in the frequency domain. For an ideal sinusoidal oscillator operating at ω_0, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skirts" around the carrier frequency ω_0, as shown in Fig. 4.3. To quantify phase noise, we consider a unit bandwidth at an offset $\Delta\omega$ with respect to ω_0, calculate the noise power in this bandwidth, and divide the result by the carrier (average) power.

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right], \tag{4.2}$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ represents the single sideband power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1Hz.

4.2.2 Conversion of Noise to Phase Noise

Oscillator phase noise is generated primarily through two mechanisms, distinguished by the path into which the noise is injected. Illustrated in Fig. 4.4, the noise, $x(t)$, appearing in these paths gives rise to distinctly different effects.

4.2.2.1 Noise Mixing and Noise Folding

If we treat VCO as a linear time-invariant (LTI) system, the noise injected into the signal path [Fig. 4.4(a)] simply mixes with the carrier (Fig. 4.5).

Oscillators usually experience amplitude limiting and hence nonlinearity, thus "folding" the noise components. If the open-loop input/output characteristic of VCO is expressed as $V_{out} = \alpha_1 V_{in} + \alpha_2 V_{in}^{\ 2} + \alpha_3 V_{in}^{\ 3}$, then for an input consisting of the carrier and a noise component, e.g., $V_{in}(t) = A_0 \cos\omega_0 t + A_n \cos\omega_n t$, the output exhibits the following important terms:

$$V_{out1}(t) \propto \alpha_2 A_0 A_n \cos(\omega_0 \pm \omega_n)t \tag{4.3}$$

$$V_{out2}(t) \propto \alpha_3 A_0 A_n^2 \cos(\omega_0 - 2\omega_n)t \tag{4.4}$$

$$V_{out3}(t) \propto \alpha_3 A_0^2 A_n \cos(2\omega_0 - \omega_n)t. \tag{4.5}$$

Note that $V_{out1}(t)$ appears in band if ω_n is small. However, in a fully differential configuration usually used, $V_{out1}(t) = 0$ because $\alpha_2 = 0$. Also, $V_{out2}(t)$ is negligible because $A_n \langle\langle A_0$. Therefore, $V_{out3}(t)$ is the only significant cross-product. Thus, the nonlinearity folds all the noise components below ω_0 to the region above and vice versa. Such components are significant if they are close to ω_0. This phenomenon is illustrated in Fig. 4.6. This simplified analysis predicts the frequency of the components in response to injected noise, but not their magnitude. When noise is injected into the signal path of VCO, the magnitude of the observed response at ω_n and $2\omega_0 - \omega_n$ depends on the noise shaping property of the VCO [11].

4.2.2.2 Frequency Modulation

When the noise is injected into the control path [Fig. 4.4(b)], viewed as analog frequency modulation, this effect translates the noise in the control path to the region around the carrier, as described as follows.

Frequency is defined as the derivative of phase with respect to time:

$$\omega = d\varphi / dt . \tag{4.6}$$

Equation (4.5) indicates that, if the frequency of a waveform is known as a function of time, the phase can be computed as

$$\varphi = \int \omega dt + \varphi_0 . \tag{4.7}$$

Let's use K_{VCO} to denote the VCO gain and V_{cont} to denote the control voltage. In particular, since for a VCO, $\omega_{out} = \omega_0 + K_{VCO} \times V_{cont}$, we have

$$V_{out}(t) = V_0 \cos(\int \omega_{out} dt + \varphi_0)$$

$$= V_0 \cos(\omega_0 t + K_{VCO} \int V_{cont} dt + \varphi_0) . \tag{4.8}$$

The initial phase ϕ_0 is usually unimportant and is assumed zero hereafter.

When a VCO sense a small sinusoidal control voltage $V_{cont} = V_n \cos\omega_n t$, the output is expressed as

$$V_{out}(t) = V_0 \cos(\omega_0 t + K_{VCO} \int V_{cont} dt) \tag{4.9}$$

$$= V_0 \cos(\omega_0 t + K_{VCO} \frac{V_n}{\omega_n} \sin\omega_n t) \tag{4.10}$$

$$= V_0 \cos\omega_0 t \cos(K_{VCO} \frac{V_n}{\omega_n} \sin\omega_n t)$$

$$- V_0 \sin\omega_0 t \sin(K_{VCO} \frac{V_n}{\omega_n} \sin\omega_n t) \tag{4.11}$$

If V_n is small enough that $K_{VCO} V_n / \omega_n \langle\langle 1$ radius, then

$$V_{out}(t) \approx V_0 \cos\omega_0 t - V_0 (\sin\omega_0 t)(K_{VCO} \frac{V_n}{\omega_n} \sin\omega_n t) \tag{4.12}$$

$$= V_0 \cos\omega_0 t$$

$$- \frac{K_{VCO} V_n V_0}{2\omega_n} [\cos(\omega_0 - \omega_n)t - \cos(\omega_0 + \omega_n)t] . \tag{4.13}$$

The output consists of three sinusoidal having frequencies of ω_0, $\omega_0 - \omega_n$, and $\omega_0 + \omega_n$. The spectrum is shown in Fig. 4.7. The components at $\omega_0 \pm \omega_n$ are called "sidebands" [12].

In practice, K_{VCO} is proportional to the carrier frequency because for a given

control voltage range, the tuning range must be a constant percentage of the center frequency so as to compensate for process and temperature variations. This effect makes flicker noise (low-frequency noise) in the control path particularly detrimental. Called flicker noise upconversion, this phenomenon deteriorates the phase noise at low offset from the carrier.

As we have seen, the MOS structure varactors allow a high tuning range in a small control voltage range. This is highly desirable for designs of the scaled technologies. On the other hand, the VCO gain can become excessively high, especially for high operation frequency band. This can constitute a problem because of the high sensitivity of the MOS structure varactors to the control voltage. The bandswitching topology is suggested to decrease the sensitivity of the varactor [13], and hence, the low-frequency noise upconversion is reduced.

4.2.3 Phase noise model

The semi-empirical model reported in [14]-[16], known also as the Leeson-Cutler phase noise model, is based on an LTI assumption for tuned tank oscillators. It predicts the following behavior for $L\{\Delta\omega\}$:

$$L\{\Delta\omega\} = 10 \cdot \log\left\{\frac{2FkT}{p_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L \Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \qquad (4.14)$$

where F is an empirical parameter (often called the “device excess noise number”), k is Boltzmann’s constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_L is the effective quality factor of the tank with all the loadings in place (also known as loaded Q), $\Delta\omega$ is the offset from the carrier and $\Delta\omega_{1/f^3}$ is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions, as shown in the sideband spectrum of Fig. 4.8 [17].

4.3 LC-tank VCO Topologies

Cross-coupled NMOS and PMOS transistors can provide negative resistance to compensate the losses in the tank. Fig. 4.9 shows three types of LC-tank VCO topology.

The tail current sources are omitted because they are an important flicker-noise source. The upconversion of flicker noise to $1/f^3$ phase noise is an important issue in LC-tank VCOs. In the topologies with tail current sources, the cross-coupled NMOS and PMOS transistors are expected to feature lower flicker noise than the tail transistors for two main reasons. First, the cross-coupled NMOS and PMOS transistors operate in triode region for large portions of the oscillation period; hence, they exhibit lower current flicker noise than the tail transistors that continuously operate in saturation. Second, switched MOS transistors are known to have lower flicker noise than transistors biased in the stationary condition [18]. In other words, tail current sources dominate $1/f^3$ phase noise. Thus, from the phase-noise point of view, the topologies without tail current sources are expected to show better phase-noise performance than those with tail current sources. The main drawback often attributed to the topologies without tail current sources is a higher sensitivity of the frequency to the supply voltage (frequency pushing). This effect can be reduced by using a supply voltage regulator [19].

Compared to NMOS-only topology and PMOS-only topology, complementary topology has less power consumption, as current is reused. However, complementary topology uses more transistors (4 transistors) to realize negative resistance and thus results in more noise sources, compared to NMOS-only topology (2 transistors) and PMOS-only topology (2 transistors). Furthermore, PMOS transistors inherently show lower flicker noise (approximately 10 dB), compared to NMOS transistors. Thus,

among these three types of topology, PMOS-only topology is expected to have the best phase-noise performance.

Apart from the advantage mentioned above, two additional advantages in using PMOS-only topology are list below:

(1) The inductors force the average value of the outputs to ground and no modulation of the varactor bias point is induced by the supply voltage. Therefore, frequency pushing is reduced.

(2) Being inside an n-well, the PMOS transistor is less susceptible to substrate coupling noise pickup than the NMOS transistor.

4.4 Output Buffer

The placement of a 50-ohm load directly at the terminals of the tank such as when testing with a spectrum analyzer would reduce the Q of the circuits and influence the oscillation frequency. For this reason, output buffers must be added to the circuits. Too small transistor can not provide enough output current drive. However, the gate oxide capacitance and parasitic capacitances of the transistors used as output buffers will lower oscillation frequency and reduce frequency tuning range.

The outputs can be buffered by using source followers for measurement purposes. The current sources of the source followers are replaced with external Bias Tees to provide high ac impedance. In this way, small transistors can be used to provide enough output current drive without loading the VCO core excessively [20]. However, linearity is the main consideration for output buffers. Thus, the common source configuration is better than the source follower configuration because the body effect of the source follower is damaged to the circuit linearity. At high frequency, active devices present more serious nonlinearity due to nonlinear parasitic. Thus, active load is replaced with passive load (inductor). The dc feed inductor force the

drain voltage of output buffer to V_{DD}. Therefore, the bias point of output buffer is less susceptible to process variation and temperature variation.

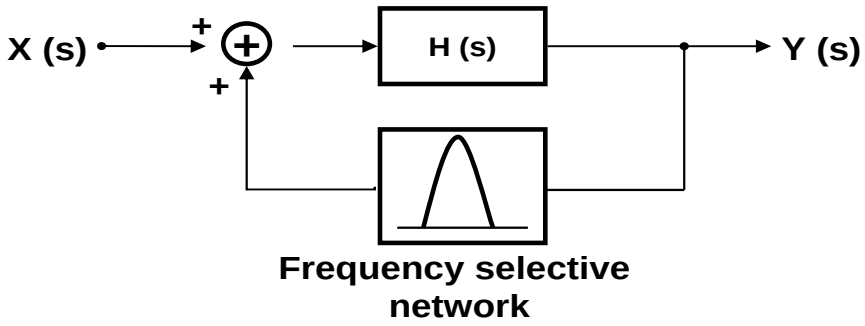


Fig. 4.1 Feedback oscillatory system with frequency-selective network.

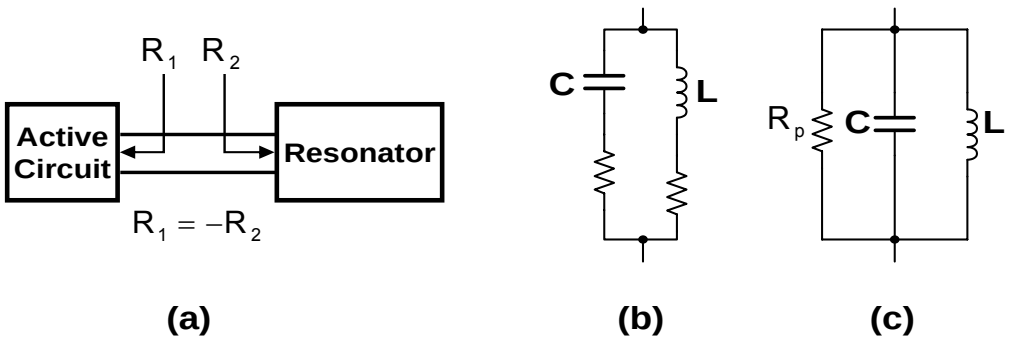


Fig. 4.2 (a) One port view of oscillators, (b) LC resonator, and (c) equivalent circuit of (b).

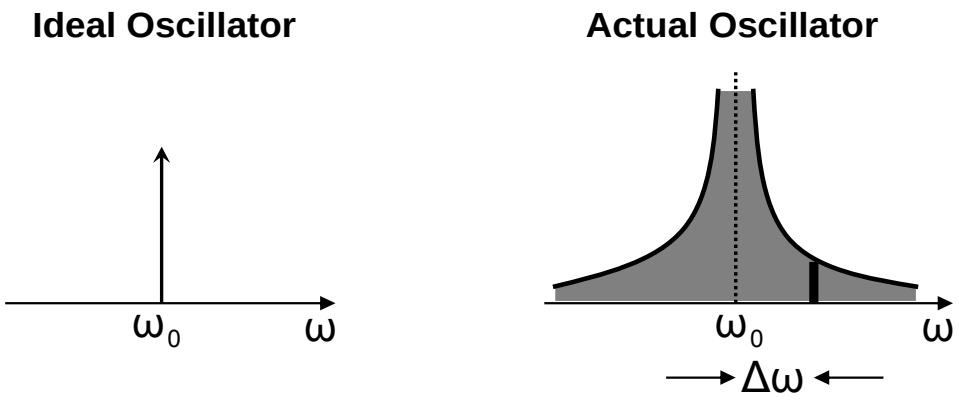


Fig. 4.3 Output spectrum of ideal and actual oscillators.

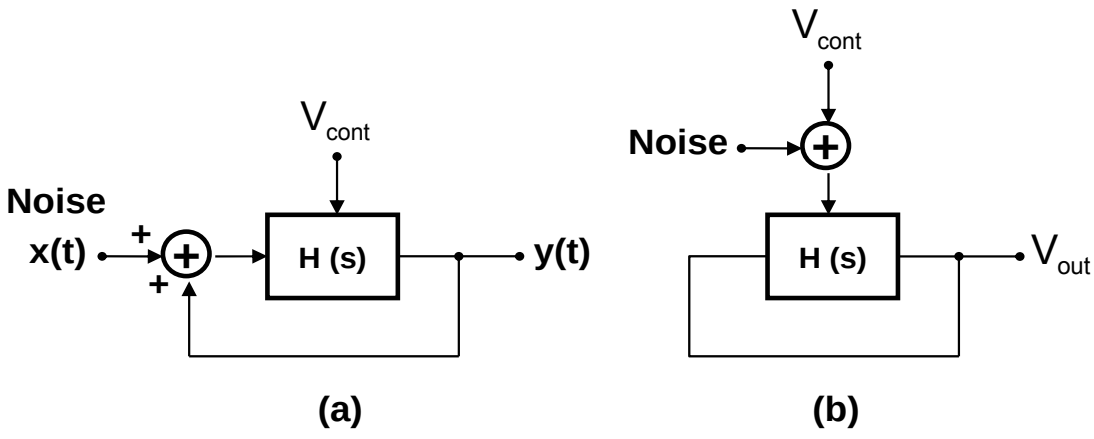


Fig. 4.4 Phase noise in (a) signal path, and (b) control path.

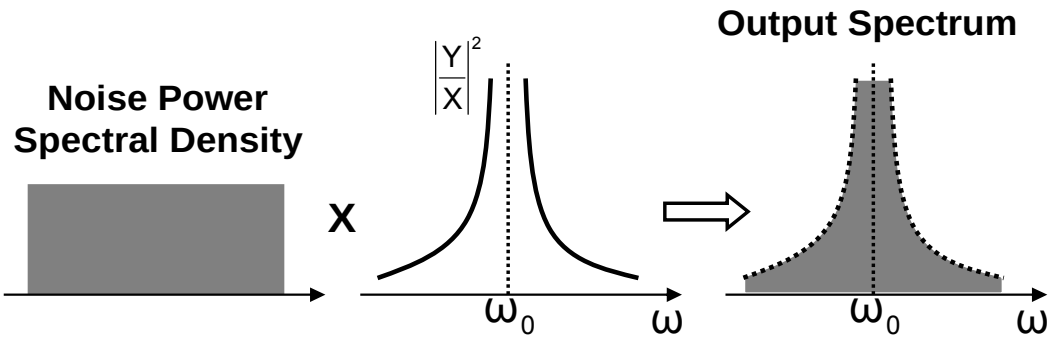


Fig. 4.5 Noise shaping in oscillators.

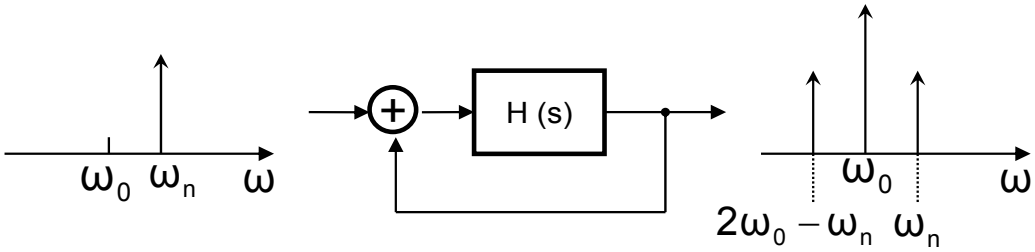


Fig. 4.6 Noise folding in an oscillator.

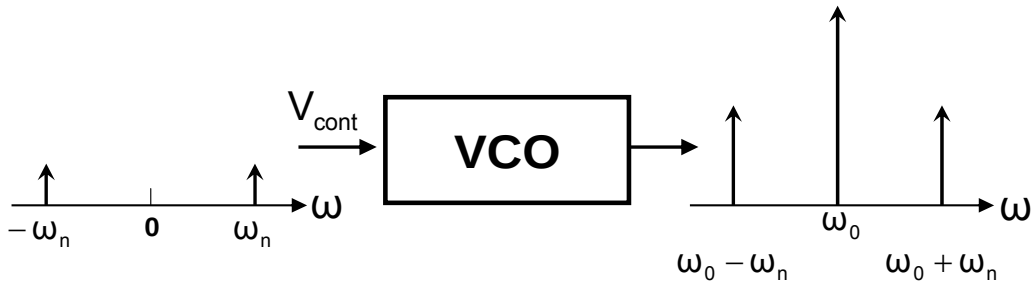


Fig. 4.7 Modulation of VCO frequency by noise on control line.

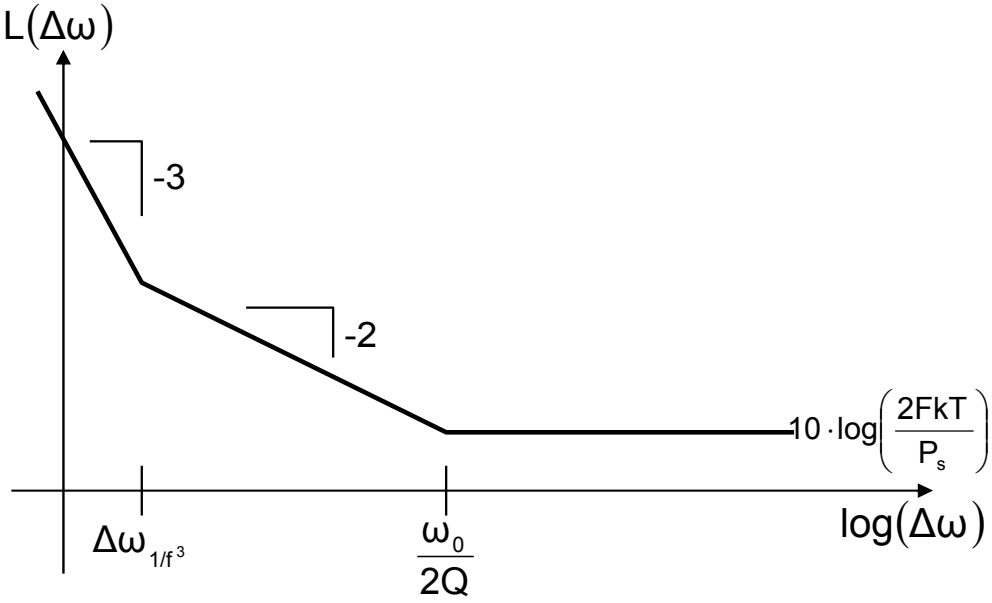


Fig. 4.8 Phase noise spectrum according to Leeson-Cutler phase noise model.

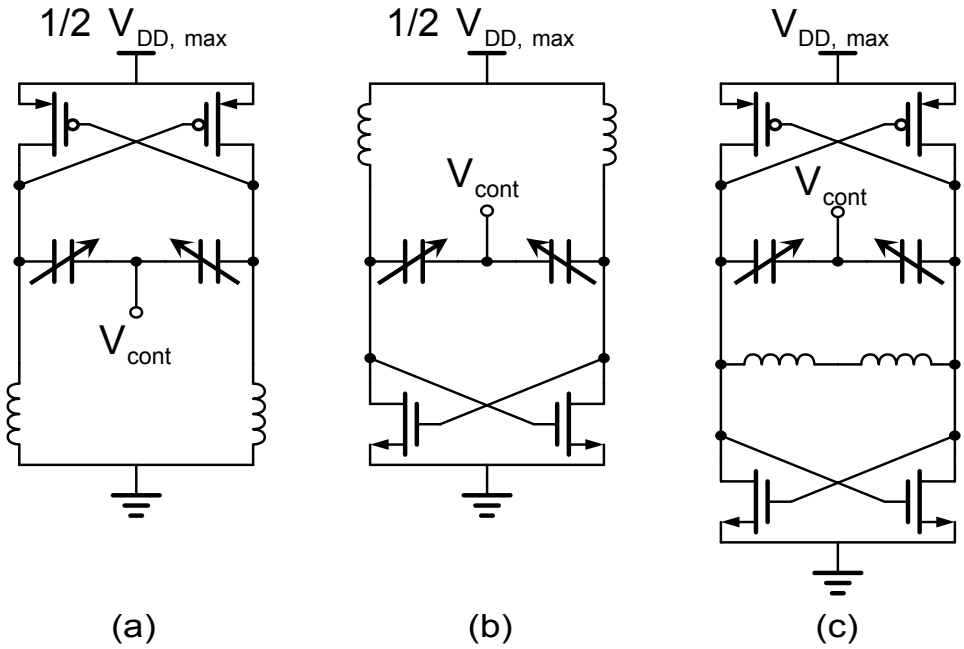


Fig. 4.9 (a) PMOS-only topology, (b) NMOS-only topology, and (c) complementary topology.

Chapter 5

Circuit Designs and Implementation

5.1 Circuit Designs

Three 2.4GHz LC VCOs (VCO1, VCO2, and VCO3) are realized in a 0.25-um CMOS process for comparison. The topology of VCO1 and VCO2 with output buffers is shown in Fig. 5.1 (PMOS-only topology). VCO1 and VCO2 differ only in the type of varactor: n-type MOS varactor (VCO1) and NMOS varactor with deep n-well (VCO2). Their sizes are equal (L x W x S x B x G=1um x 5um x 1 x 6 x 6). Each side of the control voltage node has two varactors in parallel. The top view of the spiral inductor used is shown in Fig. 5.2 with key design parameters. The key design parameters are depicted in the following:

N: number of the coil turn, which is 2.5 in Fig. 5.2.

W: width of the top metal, which is 10um in Fig. 5.2.

S: space of top metal, which is 2um in Fig. 5.2.

R: radius of inner coil, which is 60um in Fig. 5.2.

The size of the cross-coupled PMOS transistors is 0.24um x 5um x 24 (L x W x Finger). The open-drain PMOS transistors are used as output buffers. Power supply provides bias voltages for the open-drain PMOS transistors with the use of external Bias Tees. The size of the open-drain PMOS transistors is also 0.24um x 5um x 24 (L x W x Finger).

In VCO1 and VCO2, the RF signal injected into the substrate as substrate noise is provided by signal generator. The RF signal is injected into the substrate through the p+ ring surrounding the varactors. In this thesis, we focus on the influences of

substrate noise coupling to the varactors on the output spectrums of VCO1 and VCO2. Thus, the varactors and the surrounding p+ ring are placed apart from the rest of the circuit. Furthermore, in order to prevent the injected substrate noise from coupling to the cross-coupled PMOS transistors, the cross-coupled PMOS transistors are surrounded by another p+ guard ring. The arrangement described above is shown in Fig. 5.3. In order to facilitate comprehension, the topology shown in Fig. 5.1 is redrawn to the combination of a feedback loop, varactors, and output buffers.

An additional 2.4GHz VCO circuit (VCO3) adopting complementary topology is designed (Fig. 5.4). The type of varactor is n-type MOS varactor. Each side of the control voltage node has single varactor (L x W x S x B x G=1um x 5um x 1 x 6 x 6). The core spiral inductor is the same as that used in VCO1 and VCO2. The size of the cross-coupled NMOS transistors is 0.24um x 5um x 8 (L x W x Finger). The size of the cross-coupled PMOS transistors is 0.24um x 5um x 24 (L x W x Finger). The open-drain NMOS transistors (L x W x Finger=0.24um x 5um x 8) are used as output buffers. As mentioned in section 4.3, PMOS-only topology is expected to have lower phase noise than complementary topology. Therefore, VCO3 is designed to compare with VCO1.

5.2 Simulation Results

For comparison reason, the structure and layout of NMOS with deep n-well used as varactor in VCO2 is different from that of NMOS with deep n-well used as transistor in the given 0.25um CMOS process. Therefore, there is no model for simulation. The simulated results of VCO1 and VCO3 are summarized in Table 5.1 and Table 5.3 respectively. It should be noted that the simulated phase noise of VCO1 is lower than that of VCO3. The simulation tool is Agilent Advance Design System.

5.3 Layout Designs

Fig. 5.5 shows the layout of VCO1. The total area is 1110um x 1000um. The arrangement of the component devices is spiral inductors, all transistors, and varactors respectively from the top to the bottom of the layout. The symmetry of the layout is well considered. In order to conform the specific layout rules of the on-wafer measurement in National Nano Device Laboratories (NDL), the RF GSG pads of output signals are arranged on left and right side, the RF GSG pads of input signal used as substrate noise are arranged on top side, the PGPPGP DC pads are arranged on bottom side, and the single DC pad on top side is connected to the ground node of the spiral inductors.

Fig. 5.6 shows the layout of VCO2. The total area is 1110um x 1000um. The arrangement of the layout is similar to that of VCO1.

Fig. 5.7 shows the layout of VCO3. The total area is 1110um x 1000um. The arrangement of the component devices is spiral inductors, all transistors, and varactors respectively from the top to the bottom of the layout. The symmetry of the layout is well considered. In order to conform the specific layout rules of the on-wafer measurement in National Nano Device Laboratories (NDL), the RF GSG pads of output signals are arranged on left and right side, and the PGPPGP DC pads are arranged on bottom side.

5.4 Measurement Results

The output spectrums and the phase noise of the VCO circuits are measured using Agilent E4407B spectrum analyzer. The RF signal injected into the substrate as substrate noise is provided by signal generator.

Fig. 5.8 shows the measured output spectrum of VCO1 at 1.9358-GHz oscillation frequency. Fig. 5.9 shows the measured and simulated oscillation frequency of VCO1 versus the control voltage V_{cont}. Fig. 5.10 shows the measured

phase noise of VCO1 at 1.9368-GHz carrier frequency. The phase noise at 1-MHz offset from the carrier is -93.39dBc/Hz. The phase noise at 100-KHz offset from the carrier is estimated at about -70dBc/Hz according to Fig. 5.10.

Fig. 5.11 shows the measured output spectrum of VCO2 at 2.548-GHz oscillation frequency. Fig. 5.12 shows the measured oscillation frequency of VCO2 versus the control voltage V_{cont}. Fig. 5.13 shows the measured phase noise of VCO2 at 2.5493-GHz carrier frequency. The phase noise at 1-MHz offset from the carrier is -98.56dBc/Hz. The phase noise at 100-KHz offset from the carrier is estimated at about -85dBc/Hz according to Fig. 5.13.

Fig. 5.14 shows the measured output spectrum of VCO3 at 2.2327-GHz oscillation frequency. Fig. 5.15 shows the measured and simulated oscillation frequency of VCO3 versus the control voltage V_{cont}. Fig. 5.16 shows the measured phase noise of VCO3 at 2.4333-GHz carrier frequency. The phase noise at 1-MHz offset from the carrier is -102.82dBc/Hz. The phase noise at 100-KHz offset from the carrier is estimated at about -80dBc/Hz according to Fig. 5.16.

The measured and simulated results of VCO1, VCO2, and VCO3 are summarized in Table 5.1, Table 5.2, and Table 5.3, respectively. It should be noted that the measured phase noise is much higher than the simulated phase noise. This problem is attributed to the extra noise on DC pads generating by current switching through the parasitics of DC probes. However, the DC voltage sources in the simulator are ideal and noiseless. Thus, the extra noise on DC pads deteriorates the measured phase noise. The parasitics of DC probes also results in the shift of the measured oscillation frequency from the simulated oscillation frequency. This problem can be improved by adding bypass capacitors between DC pads and ground pads in the layouts. As shown in Table 5.1 and Table 5.3, the simulated phase noise of VCO1 is lower than that of VCO3 because VCO1 has fewer constituent devices and

thus less noise source. However, the measured phase noise of VCO1 is higher than that of VCO3. This problem is attributed to the higher VCO gain of VCO1. The higher VCO gain makes VCO1 more sensitive to the extra noise on DC pads. Table 5.1 shows that the frequency tuning range of VCO1 is 548MHz, at 1.3-V control voltage range. Table 5.3 shows that the frequency tuning range of VCO3 is 505MHz, at 2.5-V control voltage range.

In VCO1, at 2.499-GHz oscillation frequency, the measured output spectrum without substrate noise injection and the measured output spectrum with substrate noise injection are shown in Fig. 5.17.

In VCO2, at 2.5713-GHz oscillation frequency when the deep n-wells of NMOS varactors are biased at 2.5V, the measured output spectrum without substrate noise injection and the measured output spectrum with substrate noise injection are shown in Fig. 5.18. At 2.5692-GHz oscillation frequency when the deep n-wells of NMOS varactors are biased at 0V, the measured output spectrum without substrate noise injection and the measured output spectrum with substrate noise injection are shown in Fig. 5.19. At 2.5686-GHz oscillation frequency when the deep n-wells of NMOS varactors are floating, the measured output spectrum without substrate noise injection and the measured output spectrum with substrate noise injection are shown in Fig. 5.20. It is noted here that the oscillation frequency shifts when the deep n-wells are biased at different conditions (without substrate noise injection). Therefore, the shift of oscillation frequency doesn't result from substrate noise injection. When power supply is off, the measured output spectrum with substrate noise injection is shown in Fig. 5.21. This shows that the injected substrate noise travels through the substrate and then couples to the output pads.

A 2.6-GHz signal with 0-dBm power provided by signal generator is injected into the substrate as substrate noise. It is obvious that "noise folding" happens when

substrate noise is injected. As mentioned in section 4.2.2, the magnitudes of the components at ω_n and $2\omega_0 - \omega_n$ depends on the noise shaping properties of VCO circuits. Noise shaping property is relative to the quality factor of LC tank. VCO1 and VCO2 differ in the type of varactor. Thus, they have different noise shaping properties.

In VCO2, the magnitudes of the components at $2\omega_0 - \omega_n$ in Figs. 5.18, 5.19, and 5.20 are almost equal. This shows that different bias conditions of the deep n-wells have little influence on the magnitudes of the components at ω_n and $2\omega_0 - \omega_n$. As shown in Fig. 3.4, deep n-well biased at 2.5V has best isolation capability, and floating deep n-well has worst isolation capability. However, the difference of their measured S_{21} is small at high frequency (>1GHz).

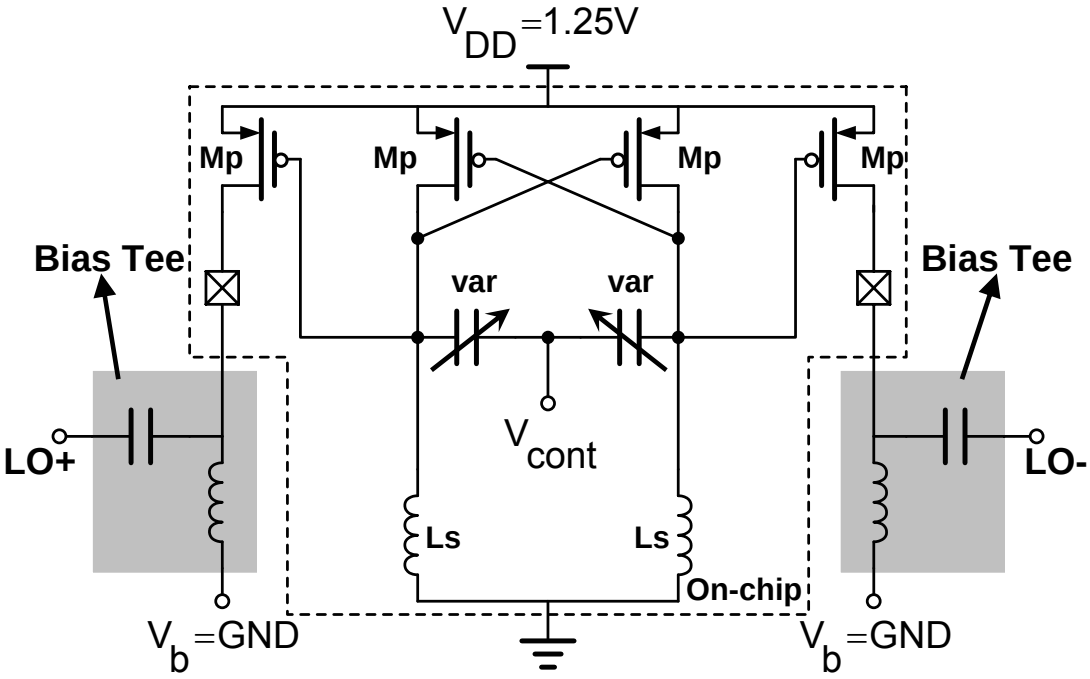


Fig. 5.1 The circuit topology of VCO1 and VCO2.

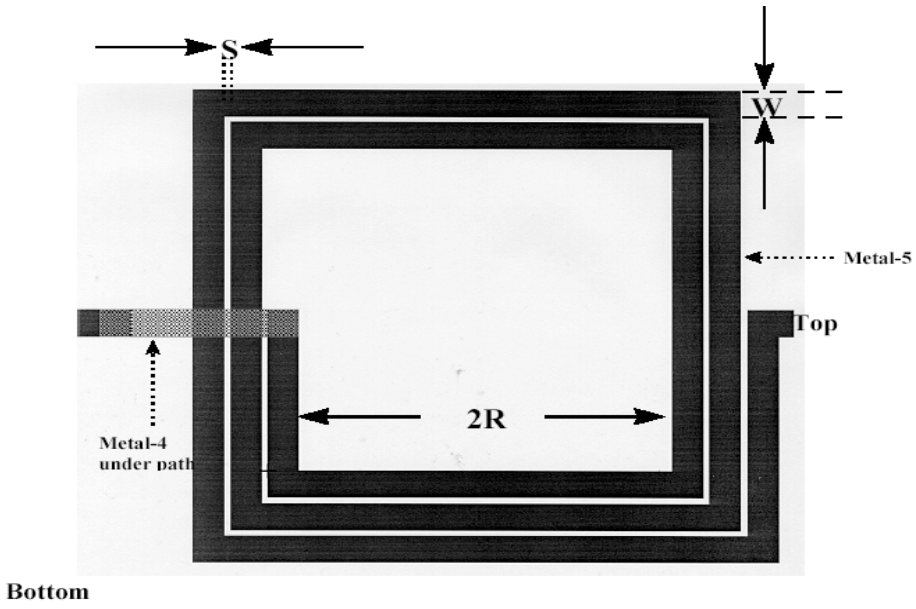


Fig. 5.2 The top view and physical dimension of spiral inductor.

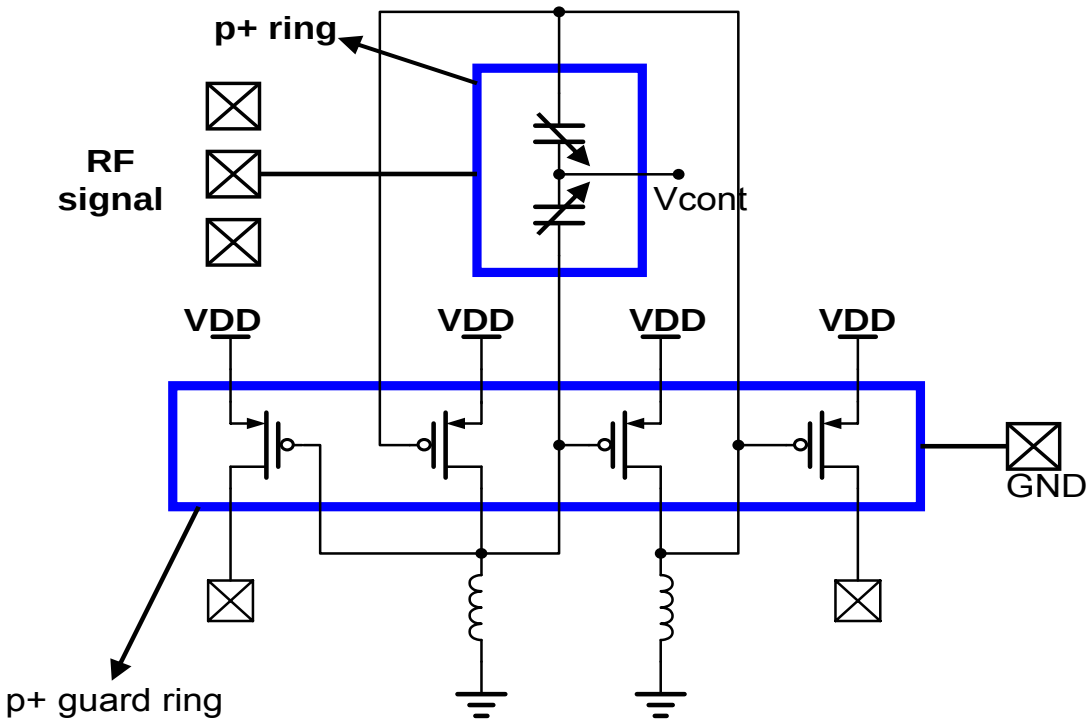


Fig. 5.3 The circuit topology of VCO1 and VCO2 with substrate noise injection, and the Bias Tees are not drawn.

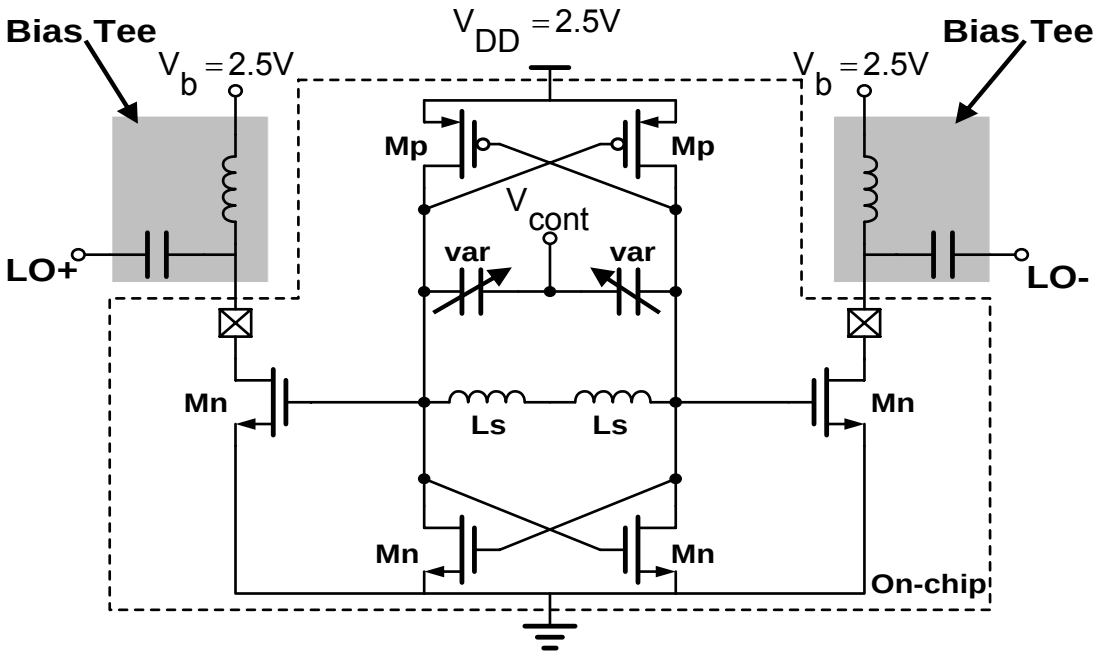


Fig. 5.4 The circuit topology of VCO3.

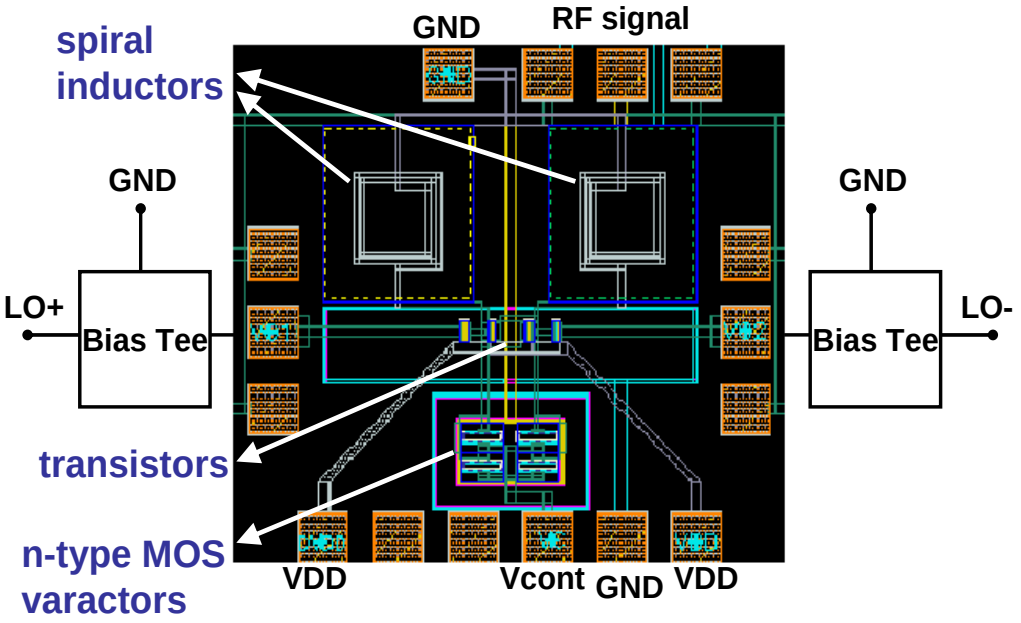


Fig. 5.5 The layout of VCO1.

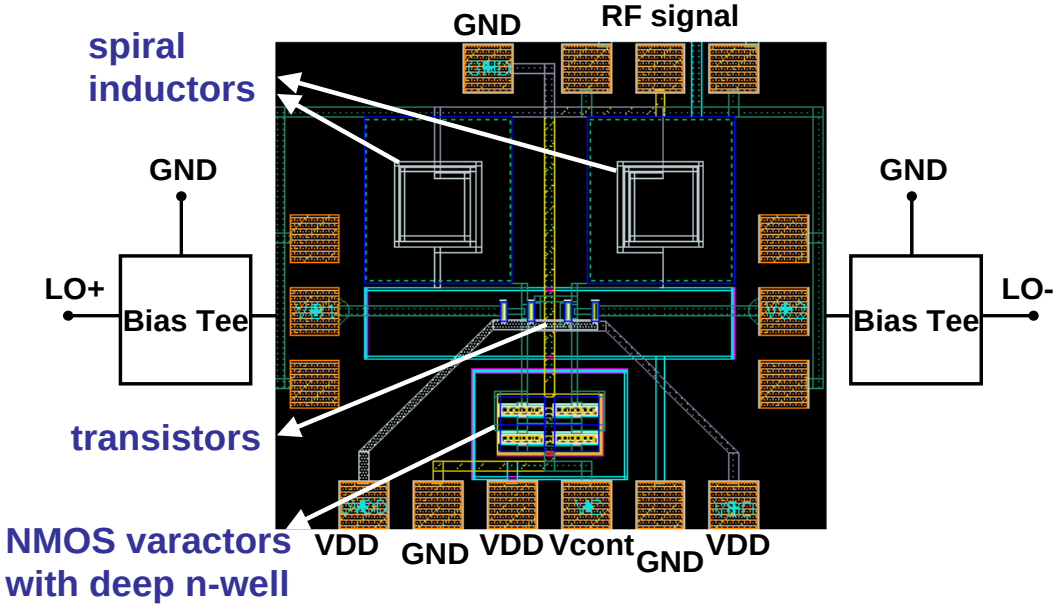


Fig. 5.6 The layout of VCO2.

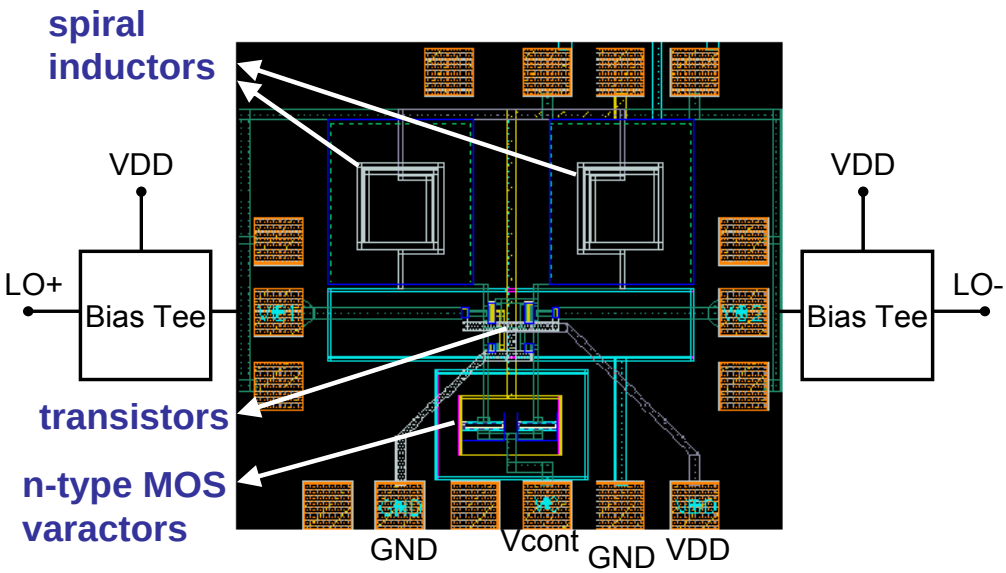


Fig. 5.7 The layout of VCO3.

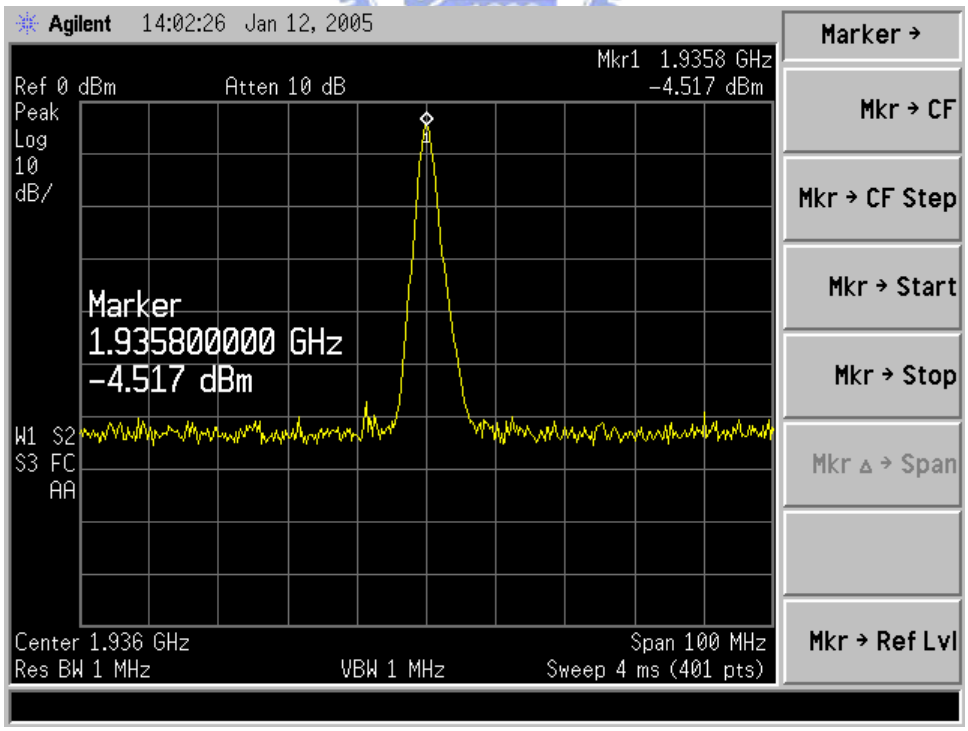


Fig. 5.8 The measured output spectrum of VCO1 at 1.9358-GHz oscillation frequency.

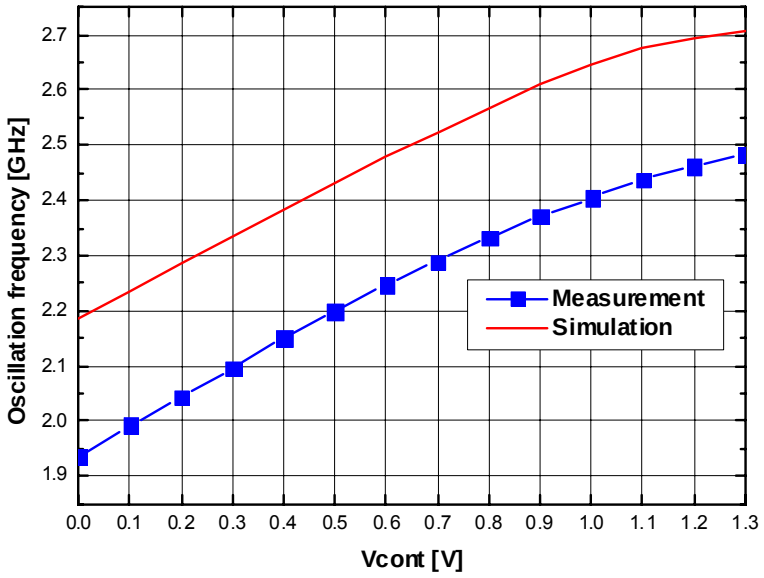


Fig. 5.9 The measured and simulated oscillation frequency of VCO1 versus the control voltage V_{cont}.

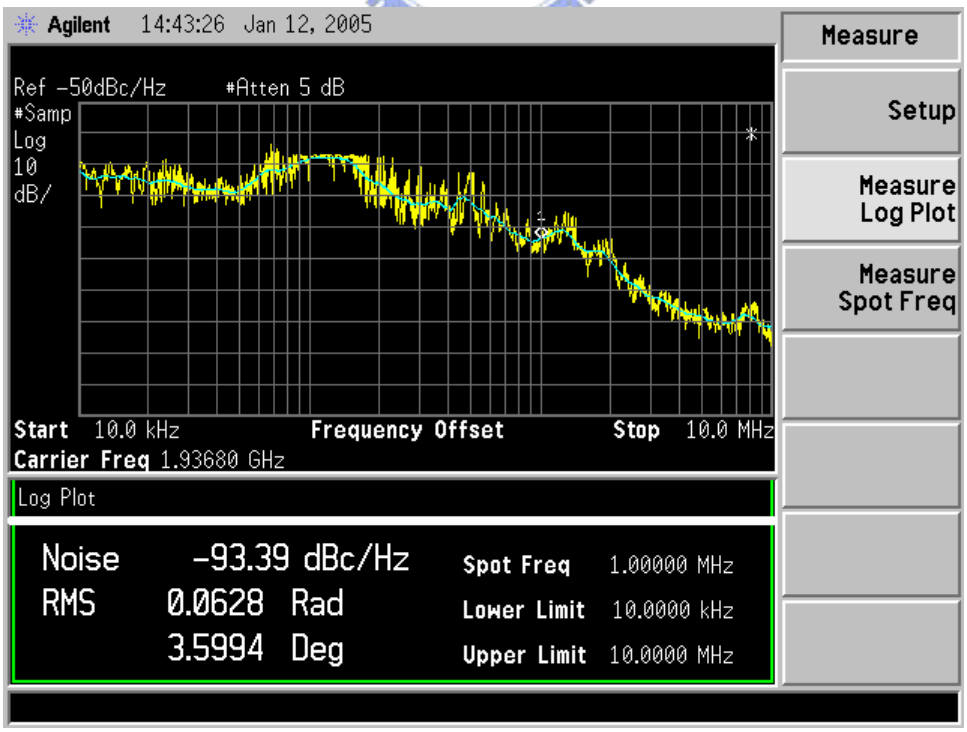


Fig. 5.10 The measured phase noise of VCO1 at 1.9368-GHz carrier frequency.

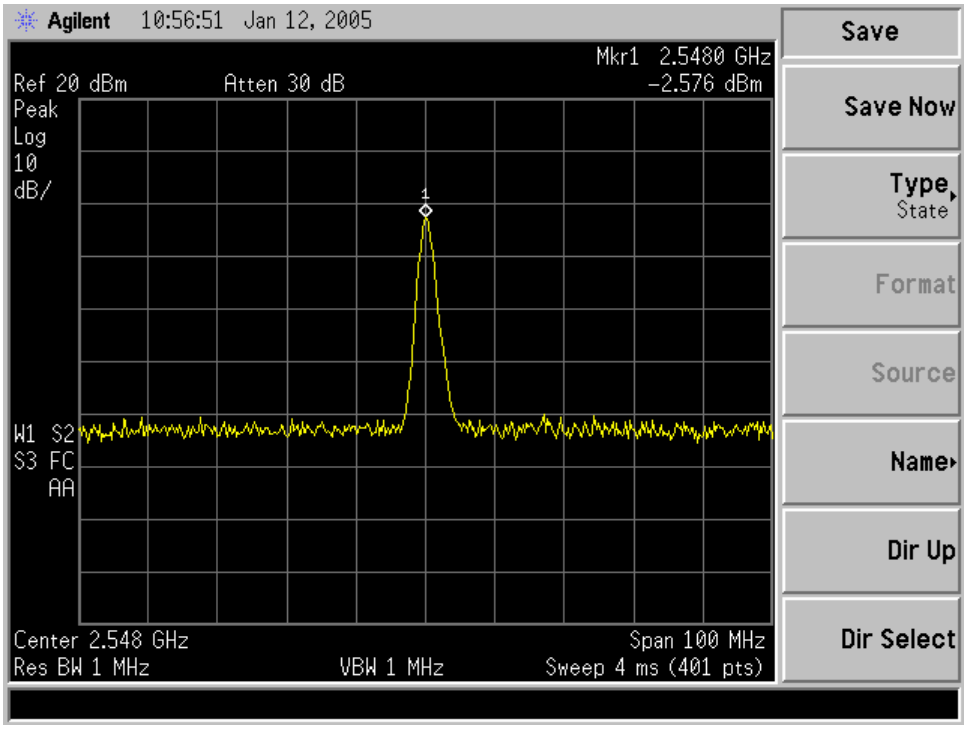


Fig. 5.11 The measured output spectrum of VCO2 at 2.548-GHz oscillation frequency.

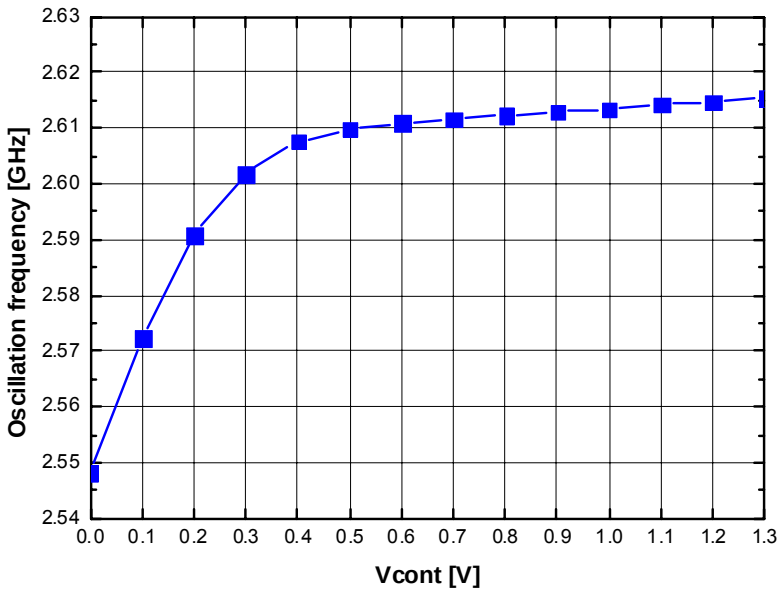


Fig. 5.12 The measured oscillation frequency of VCO2 versus the control voltage V_{cont}.

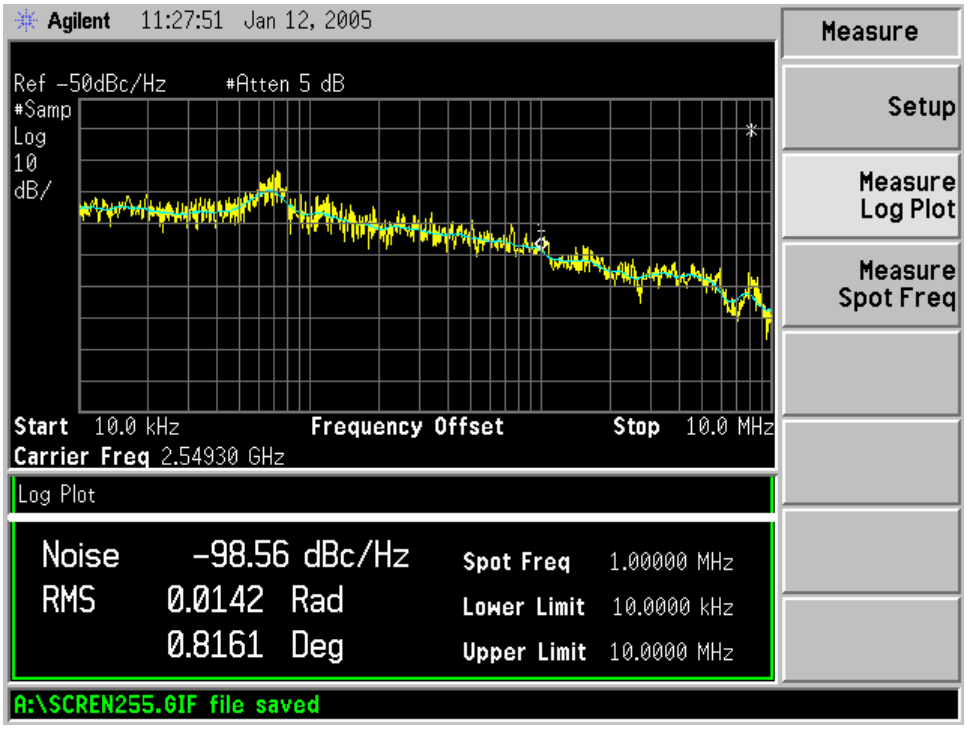


Fig. 5.13 The measured phase noise of VCO2 at 2.5493-GHz carrier frequency.

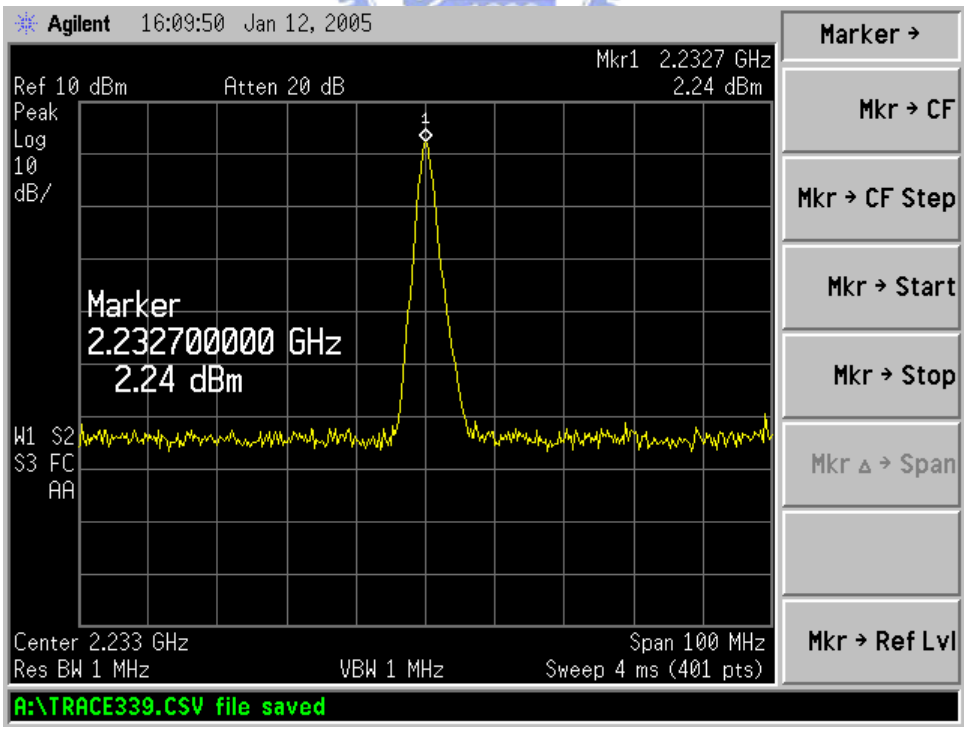


Fig. 5.14 The measured output spectrum of VCO3 at 2.2327-GHz oscillation frequency.

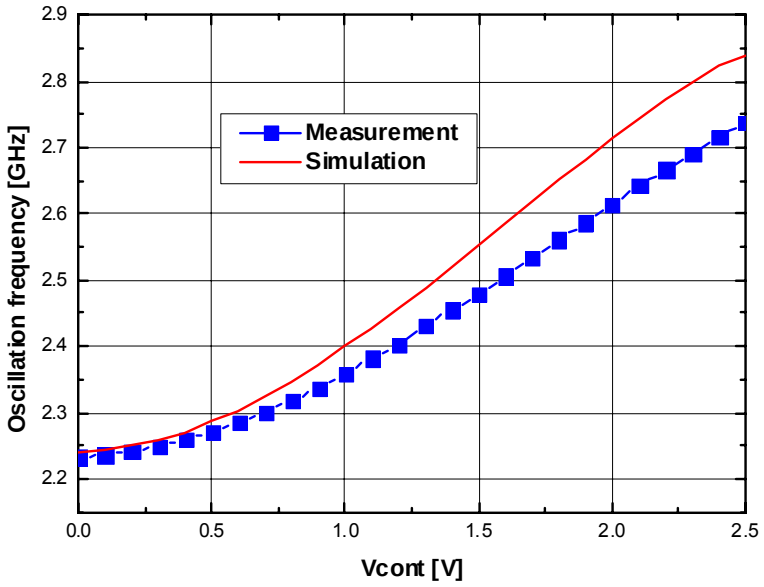


Fig. 5.15 The measured and simulated oscillation frequency of VCO3 versus the control voltage V_{cont}.

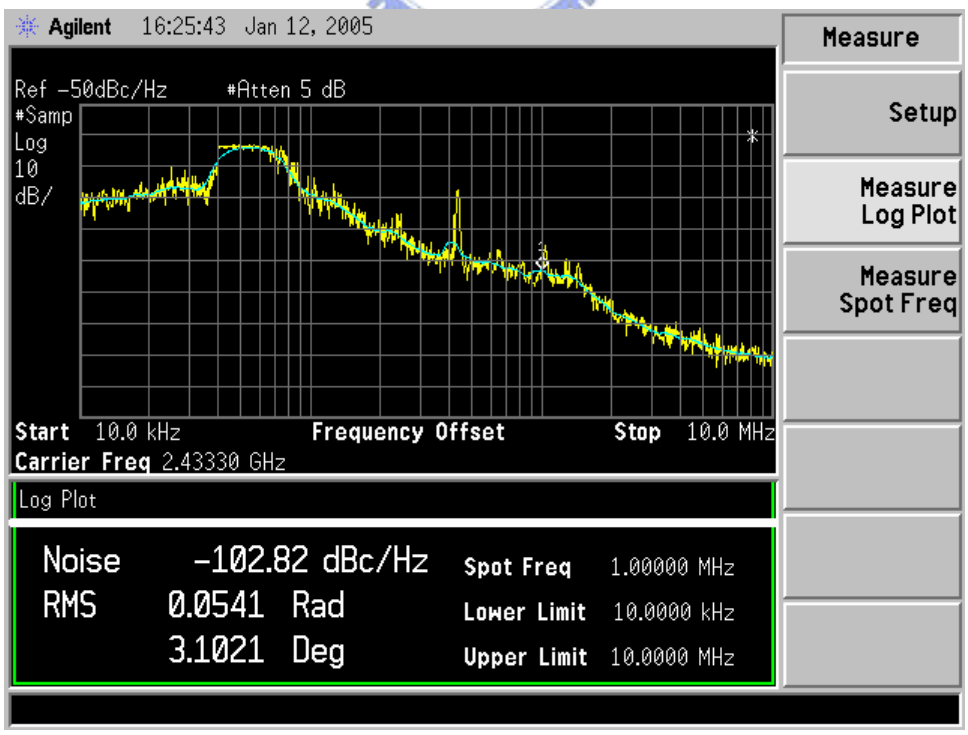
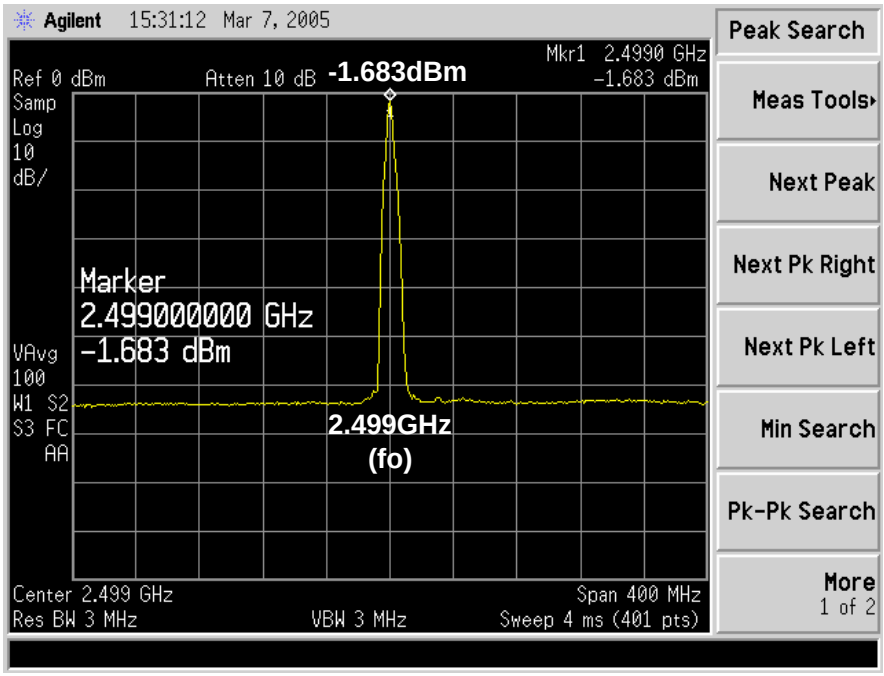
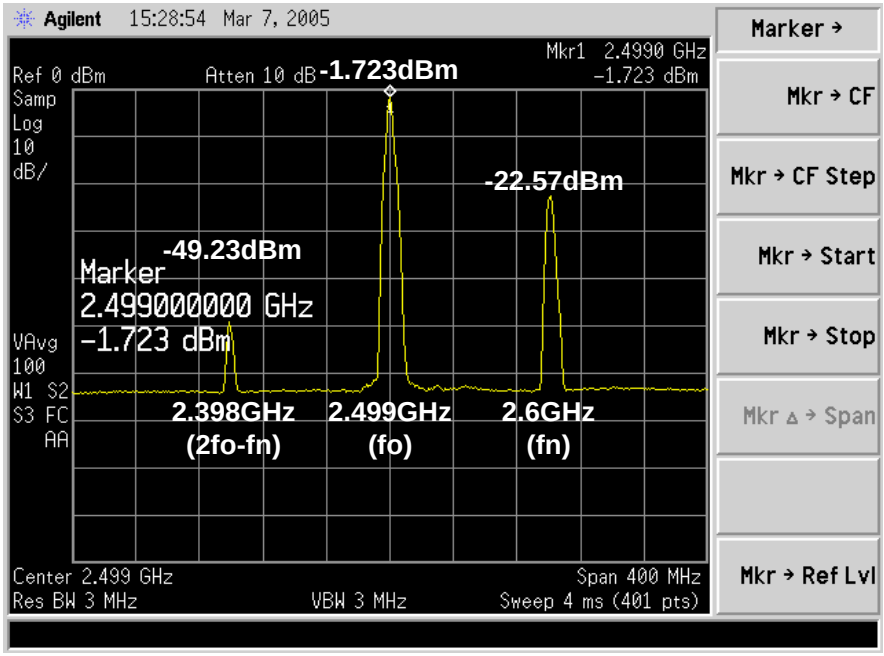


Fig. 5.16 The measured phase noise of VCO3 at 2.4333-GHz carrier frequency.

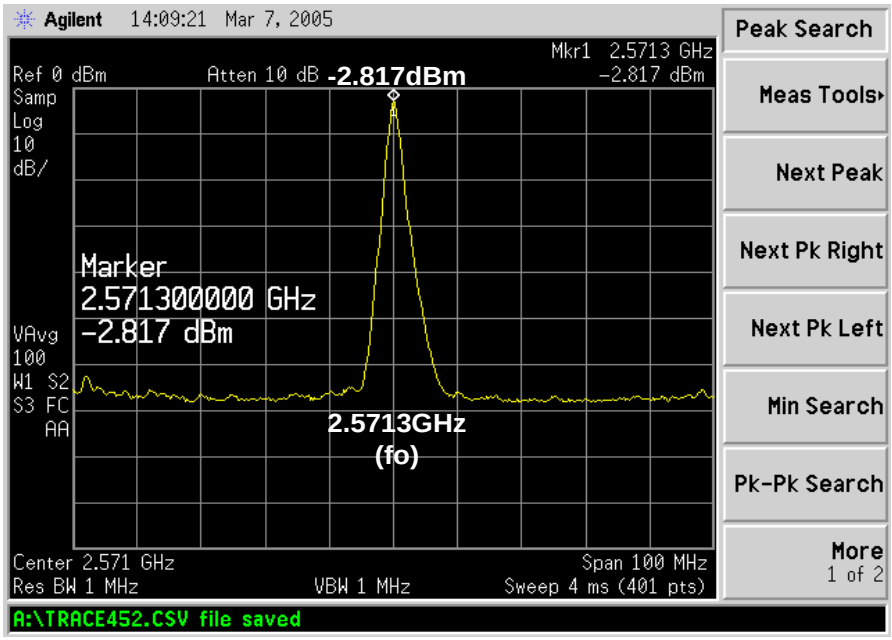


(a)

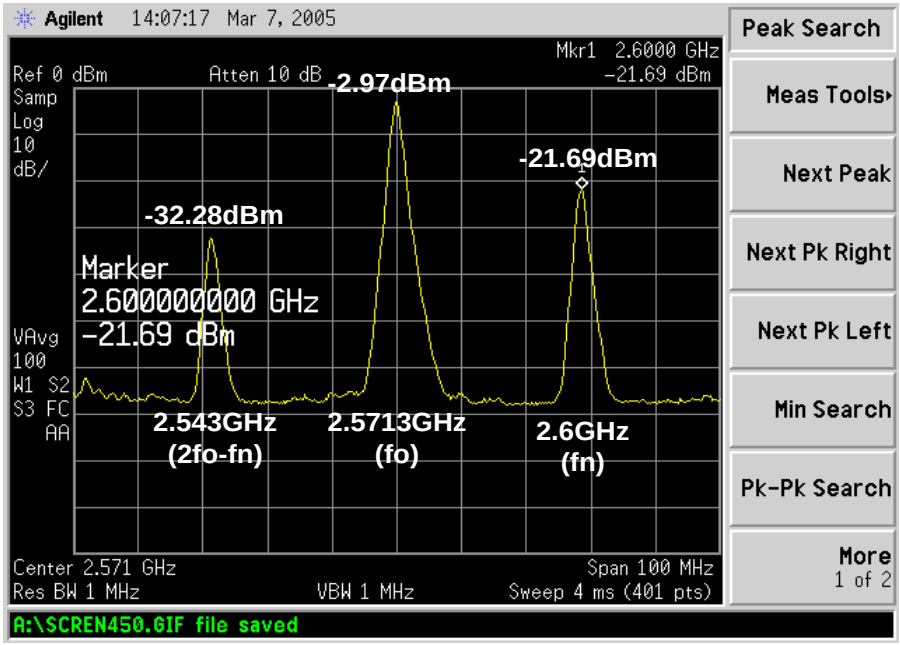


(b)

Fig. 5.17 In VCO1, at 2.499-GHz oscillation frequency, (a) the measured output spectrum without substrate noise injection and (b) the measured output spectrum with substrate noise injection.

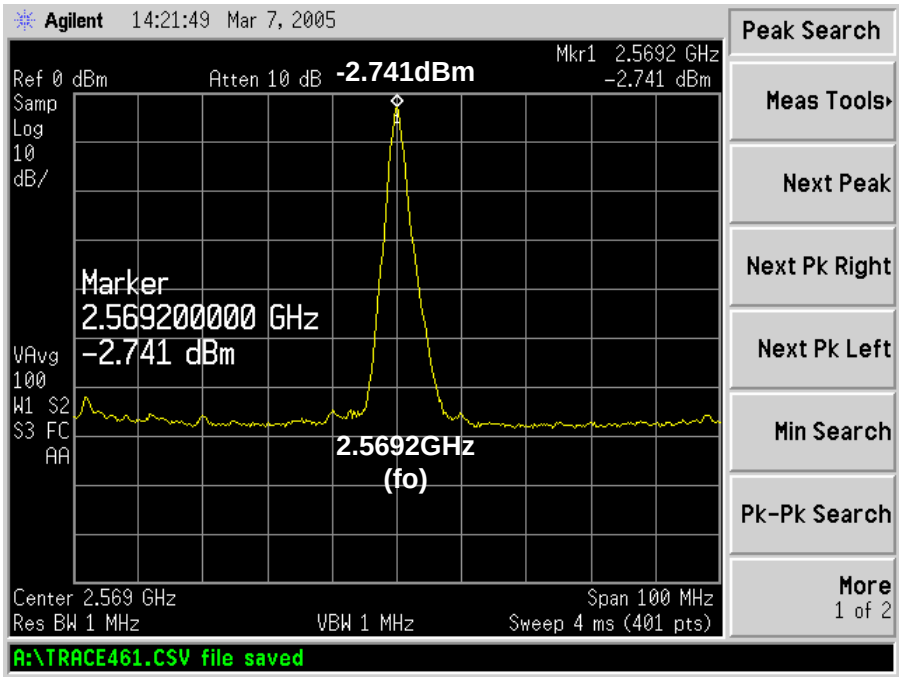


(a)

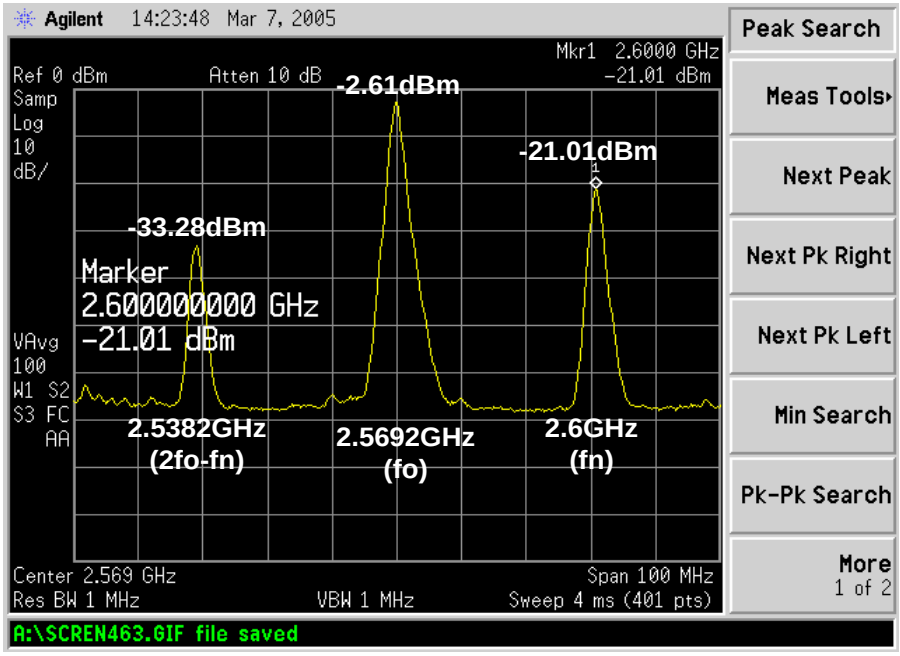


(b)

Fig. 5.18 In VCO2, at 2.5713-GHz oscillation frequency when the deep n-wells of NMOS varactors are biased at 2.5V, (a) the measured output spectrum without substrate noise injection and (b) the measured output spectrum with substrate noise injection.

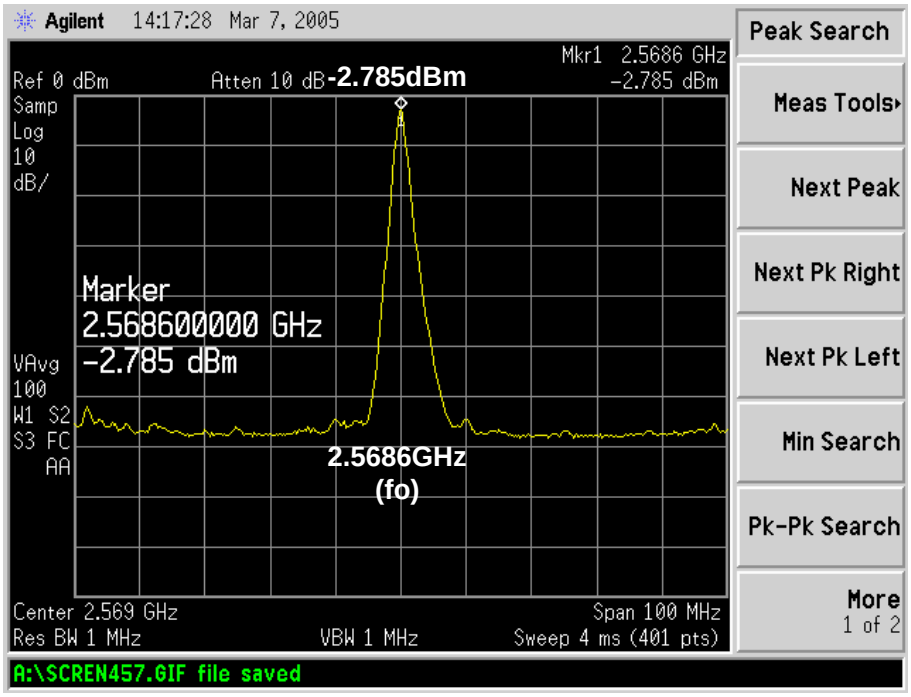


(a)

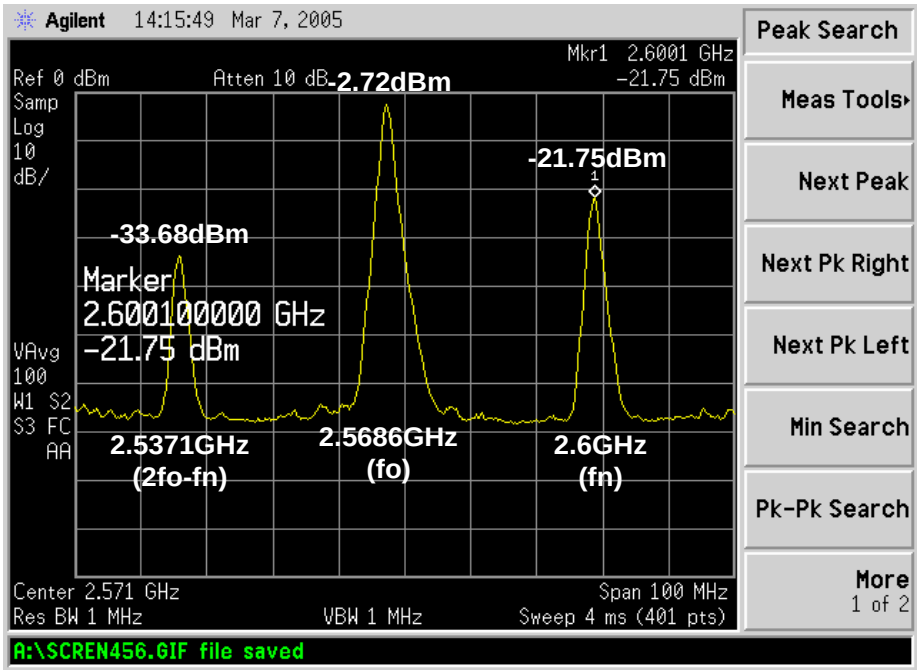


(b)

Fig. 5.19 In VCO2, at 2.5692-GHz oscillation frequency when the deep n-wells of NMOS varactors are biased at 0V, (a) the measured output spectrum without substrate noise injection and (b) the measured output spectrum with substrate noise injection.



(a)



(b)

Fig. 5.20 In VCO2, at 2.5686-GHz oscillation frequency when the deep n-wells of NMOS varactors are floating, (a) the measured output spectrum without substrate noise injection and (b) the measured output spectrum with substrate noise injection.

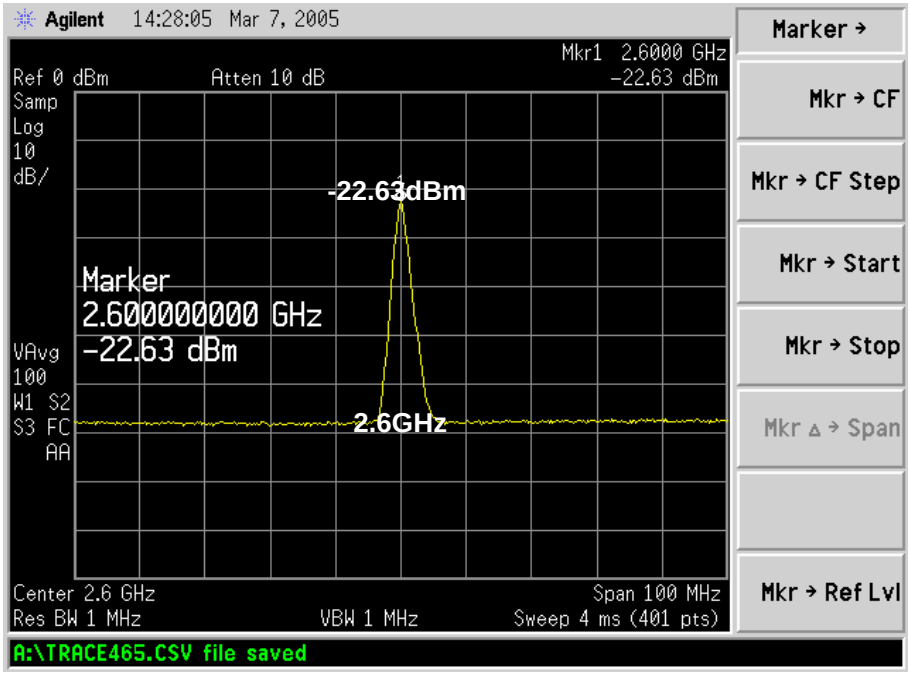


Fig. 5.21 In VCO2, when power supply is off, the measured output spectrum with substrate noise injection.

Table 5.1 A summary of the measured and simulated results of VCO1.(*estimated)

	Simulation	Measurement
Power supply	**1.25V**	**1.25V**
Control voltage	**0~1.3V**	**0~1.3V**
Frequency range	**2.187~2.706GHz**	**1.936~2.484GHz**
Tuning range	**519MHz**	**548MHz**
Phase noise@100KHz	**-106.86dBc/Hz**	*** -70dBc/Hz**
Phase noise@1MHz	**-126.86dBc/Hz**	**-93.39dBc/Hz**
VCO bias current	**9mA**	**11mA**

Table 5.2 A summary of the measured results of VCO2.(*estimated)

	Measurement
Power supply	**1.25V**
Control voltage	**0~1.3V**
Frequency range	**2.548~2.615GHz**
Tuning range	**67MHz**
Phase noise@100KHz	***-85dBc/Hz**
Phase noise@1MHz	**-98.56dBc/Hz**
VCO bias current	**11mA**

Table 5.3 A summary of the measured and simulated results of VCO3.(*estimated)

	Simulation	Measurement
Power supply	**2.5V**	**2.5V**
Control voltage	**0~2.5V**	**0~2.5V**
Frequency range	**2.242~2.84GHz**	**2.233~2.738GHz**
Tuning range	**598MHz**	**505MHz**
Phase noise@100KHz	**-93.24dBc/Hz**	***-80dBc/Hz**
Phase noise@1MHz	**-120.66dBc/Hz**	**-102.82dBc/Hz**
VCO bias current	**8mA**	**8mA**

Chapter 6

Conclusions and Future Works

6.1 Conclusions

Isolation capabilities of two different structures for substrate noise are compared. One structure is n-well on substrate, and the other structure is p-well surrounded by deep n-well and n-well. The measured results show that they have almost equal isolation capabilities from 1GHz to 10GHz.

Three 2.4GHz LC VCOs are realized in a 0.25-um CMOS process. VCO1 (n-type MOS varactor) and VCO2 (NMOS varactor with deep n-well) differ only in the type of varactor. The influences of substrate noise coupling to the varactors on the output spectrums of VCO1 and VCO2 are investigated. The measured output spectrums show that “noise folding” happens when a RF signal provided by signal generator is injected into the substrate as substrate noise. VCO1 (PMOS-only topology) and VCO3 (complementary topology) differ in the type of circuit topology. In simulation, the DC voltage sources are ideal and noiseless. VCO3 has higher simulated phase noise than VCO1 due to more transistors and thus more noise sources. However, VCO3 has lower measured phase noise than VCO1 due to smaller VCO gain and thus less sensitivity to the extra noise on DC pads. The extra noise on DC pads is generated by current switching through the parasitics of DC probes.

6.2 Future works

At higher frequency, it is more difficult to isolate substrate noise by wells and guard rings. Therefore, substrate noise coupling is inevitable. The measured results show that “noise folding” happens when substrate noise couples to the constituent

devices of LC VCOs. If the frequency of substrate noise is close to the oscillation frequency of LC VCO, the phase noise at small offset is deteriorated. However, the influence of substrate noise coupling on the output spectrums of LC VCOs can be decreased by increasing the overall quality factor of LC tank. As mentioned in section 4.2.2.1, the magnitude of the unwanted components generated through “noise folding” depends on the noise shaping property of the VCO. The noise shaping properties of LC VCOs is determined by the overall quality factor of LC tank. The higher the overall quality factor of LC tank, the sharper the noise shaping is. Thus, on chip inductors and varactors with high quality factor are required to suppress the influence of substrate noise coupling.

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