

國立交通大學
理學院應用科技學程

碩士論文

整合型溝渠式功率接面場效電晶體與蕭特基阻障
二極體

Power Trench Junction Field Effect Transistor Integrated with
Schottky Barrier Diode

研究生：劉莒光

指導教授：羅正忠 教授

龔 正 教授

中華民國 九十八年六月

整合型溝渠式功率接面場效電晶體與蕭特基阻障二極體

Power Trench Junction Field Effect Transistor Integrated with Schottky Barrier Diode

研究 生：劉 莒 光

Student : Chu-Kuang Liu

指 導 教 授：羅 正 忠

Advisor : J. C. Lou

龔 正

Advisor : J. Gong

國 立 交 通 大 學
理 學 院 應 用 科 技 學 程
碩 士 論 文

Submitted to Degree Program of Applied Science and Technology

College of Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Degree Program of Applied Science and Technology

June 2009

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 八 年 六 月

整合型溝渠式功率接面場效電晶體與蕭特基阻障二極體

學生：劉莒光

指導教授：羅正忠

龔 正

國立交通大學理學院應用科技學程

摘要

現今在電源供應之開關應用方面，以功率式金氧半導體場效電晶體為主要產品。為了追求更高的轉換效率與操作頻率，採用同步壓降轉換器設計可以達到此要求。然而，對同步壓降轉換器之下橋開關元件而言，仍然有一些缺點仍需要克服，譬如物理限制的元件通道導通電阻、以及來自於本身具有的PN二極體在遲滯期間的造成的高功率損失。

本篇研究首先提出一個新穎的元件結構，以整合型的溝渠式接面場效電晶體與蕭特基二極體來改善上述之缺點。本設計可提供另一個吸引人的方法來實現同步壓降轉換器之下橋開關元件。

從模擬的結果得知，較大的接面場效電晶體間距與蕭特基二極體之主動區平台寬度會得到較高的通道截止電壓，以及在不變動通道截止電下的條件下，會得到較低的汲極與源極之間崩潰電壓。另一方面，較大的通道寬度會得到較小的通道導通電阻。而蕭特基二極體的平台寬度與二極體的反向回復

特性無顯著相關性。至於磊晶層方面，低摻雜的磊晶層濃度會造成低的通道截止電壓；磊晶層的電阻率與汲極與源極之間崩潰電壓成反比，與通道導通電阻成正比。

此新穎之結構可做成超高主動區元件密度、可具競爭的導通電阻、期望的崩潰電壓、極好的低反向漏電流、以及低的順偏電位壓降。從整體的特性比較中可得知，對直流轉直流轉換器之應用，本元件結構可做為好的元件開關取代方案。



Power Trench Junction Field Effect Transistor Integrated with Schottky Barrier Diode

Student : Chu-Kuang Liu

Advisors : Dr. J. C. Lou

Dr. J. Gong

Degree Program of Applied Science and Technology
National Chiao Tung University



Nowadays, Power MOSFETs are dominant products of switching converters in the application field of power supply. For high power conversion efficiency and high frequency operating consideration, adopting synchronous buck converter (SBC) design would meet this requirement. However, for the low-side switch device of SBC, there are still some drawback characteristics such as physical limit of on-state resistance of channel, high power loss during the dead time due to the inherent PN body diode etc.

In this study, a novel structure of power trench junction field effect transistor (JFET) integrated with Schottky barrier diode (SBD) is the first time being proposed. This design provides a new alternative solution for the low side switch

of synchronous buck converter.

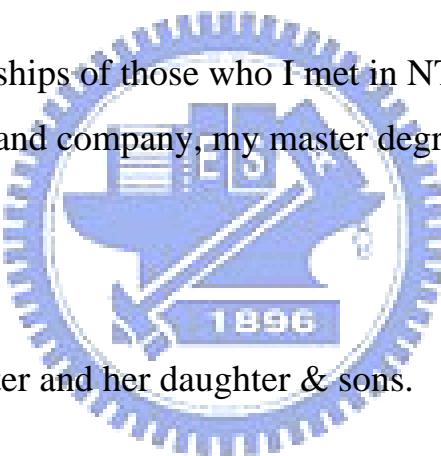
From the simulation result, we find the larger pitch size of JFET and mesa width of SBD causing higher pinch-off voltage, lower breakdown voltage of drain to source if it was under the same pinch-off voltage. On the other hand, it would result in lower specific on-resistance due to the larger channel width. There is no significant correlation between different mesa widths of Schottky diode and reverse recovery characteristics of diode. The lighter epitaxial doping concentration would get the lower pinch-off voltage. The lower resistivity of epitaxial layer is in inverse proportional to breakdown voltage, but is in proportional to on-state resistance of drain to source.

This novel structure is achievable for ultra high cell density, competitive on-state resistance, desirable breakdown voltage, excellent low reverse leakage level and lower forward voltage drop. The overall characteristic comparison shows it is a good candidate for switch device of DC-DC convertor application.

Acknowledge

感謝清大電子所龔正教授這兩年的研究指導與交大電子所羅正忠教授的共同指導。感謝交大電物所碩士在職專班班主任陳永富教授在碩士專題研究的建解，受益匪淺。感謝清大電子所雜訊實驗室的同學智閩、阿祐、如意、文山、克濤、彥宏、長鑫、范姜、祐霖、建豪、冠宇、士豪、麗珍、阿鴻、仲璘、崢渝。感謝漢磊科技與杰力科技的長官們，於我在職唸書間的包容與體諒，由衷感謝。

Thanks for the friendships of those who I met in NTHU & NCTU. Without yours friendly welcome and company, my master degree program can not be memorable.



Finally, thank my sister and her daughter & sons.

Table of Contents

Abstract (In Chinese).....	<i>i</i>
Abstract (In English).....	<i>ii</i>
Acknowledge.....	<i>iii</i>
Table of Contents.....	<i>iv</i>
Figure captions.....	<i>v</i>
Table captions.....	<i>vi</i>
Chapter 1 Introduction.....	1
1.1 Markets and Application of Low Voltage Power Device.....	1
1.2 Motivation.....	2
1.3 Application Guideline.....	4
Chapter 2 Review of Junction Field Effect Transistor and Schottky Diode.....	9
2.1 Introduction.....	9
2.2 Vertical Channel Metal-Oxide-Semiconductor Transistors....	10
2.2.1 Basic MOSFET.....	11
2.2.2 VMOS.....	11
2.2.3 DMOS.....	12
2.2.4 UMOS.....	12
2.3 Junction Field Effect Transistor.....	13
2.3.1 Lateral Channel Junction Field Effect Transistor.....	13
2.3.2 Vertical Channel Junction Field Effect Transistor.....	14
2.3.3 Trench Junction Field Effect Transistor.....	14
2.4 Schottky Diode.....	15
2.4.1 Conventional Schottky Diode.....	15
2.4.2 Junction Barrier Schottky Diode.....	15
2.4.3 Trench MOS Schottky Diode.....	16

2.5	Conclusion.....	17
Chapter 3 Fabrication of Power Trench JFET Integrated with SBD.....		24
3.1	Device Structure.....	24
3.2	Process Flow.....	25
Chapter 4 Simulation of Power Trench JFET Integrated with SBD.....		40
4.1	Introduction.....	40
4.2	Two Dimension Simulation.....	41
4.2.1	Two-Dimension Process Simulation.....	41
4.2.2	Two-Dimension Electric Characteristic Simulation.....	43
4.2.2.1	Two-Dimension Area Factor (α).....	43
4.2.2.2	Breakdown Voltage of Drain to Source (BV_{DSX}).....	44
4.2.2.3	Breakdown Voltage of Gate to Source (BV_{GSO}).....	44
4.2.2.4	Gate Threshold Voltage ($V_{GS(TH)}$).....	45
4.2.2.5	Specific On-Resistance ($R_{on,sp}$) and Drain to Source On Resistance ($R_{ds,on}$).....	46
4.2.2.6	Reverse Leakage Current (I_R).....	47
4.2.2.7	Forward Voltage Drop (V_F).....	48
4.2.2.8	Turn-on I_D - V_D Curve.....	49
4.3	Three Dimension Simulation.....	49
4.3.1	Three-Dimension Process Simulation.....	49
4.3.2	Three-Dimension Electric Characteristic Simulation.....	50
4.3.2.1	Three-Dimension Area Factor (β).....	50
4.3.2.2	Breakdown Voltage of Drain to Source (BV_{DSX}).....	50
4.3.2.3	Gate Threshold Voltage ($V_{GS(TH)}$).....	51
4.3.2.4	Specific On-Resistance ($R_{on,sp}$) and Drain to Source On Resistance ($R_{ds,on}$).....	51

4.3.2.5 Reverse Leakage Current (I_R).....	52
4.3.2.6 Forward Voltage Drop (V_F).....	53
4.4 Study of Key Process Parameters.....	53
4.4.1 Definition of Key Process Parameters.....	53
4.4.2 JFET Pitch Size.....	54
4.4.3 P+ Gate Implant Energy.....	54
4.4.4 Schottky Mesa Width.....	54
4.4.5 Resistivity of Epitaxial Layer.....	55
4.5 Conclusion.....	55
Chapter 5 Conclusion.....	81
5.1 Conclusion.....	81
5.2 Future work.....	82
References.....	83



Figure Captions

Chapter 1

Figure1.1 Discrete component markets.....	6
Figure1.2 Major types of power devices and its markets.....	6
Figure1.3 Application for power devices in relation to their voltage and current rating.....	7
Figure1.4 Synchronous buck converter implemented by MOSFET.....	7
Figure1.5 Synchronous buck converter implemented by JFET integrated with JBS.....	8

Chapter 2

Figure2.1 A basic MOSFET structure.....	18
Figure2.2 A VMOSFET structure.....	18
Figure2.3 A DMOSFET structure.....	19
Figure2.4 A UMOSFET structure.....	19
Figure2.5 A junction field effect transistor (JFET).....	20
Figure2.6 A modern version of lateral channel junction field effect transistor	20
Figure2.7 A vertical channel JFET structure using silicon planar technology	21
Figure2.8 A trench-type JFET structure.....	21
Figure2.9 An Al-Si Schottky structure.....	22
Figure2.10 Junction barrier Schottky diode structure.....	22
Figure2.11 A Trench MOS barrier Schottky diode (TMBS) structure.....	23
Figure2.11 An Integration structure between trench MOSFET and trench MOS barrier Schottky diode (TMBS).....	23

Chapter 3

Figure3.1 Proposed power trench JFET integrated with SBD structure...	24
Figure3.2 Prepare N+ substrate and N-Epi.....	26
Figure3.3 Grow field oxide.....	26
Figure3.4 AA patterning.....	27
Figure3.5 AA wet etching.....	27
Figure3.6 AA cleaning.....	28
Figure3.7 Source patterning.....	28
Figure3.8 Source implant.....	29
Figure3.9 Source cleaning.....	29
Figure3.10 Deposit hard mask oxide.....	30
Figure3.11 Trench patterning.....	30
Figure3.12 Hard mask oxide etching.....	31
Figure3.13 Trench cleaning.....	31
Figure3.14 Trench etching.....	32
Figure3.15 Source patterning.....	32
Figure3.16 P+ gate implant.....	33
Figure3.17 Source cleaning.....	33
Figure3.18 Remove hard mask oxide.....	34
Figure3.19 Deposit ILD-CVD oxide.....	34
Figure3.20 Contact patterning.....	35
Figure3.21 Contact etching.....	35
Figure3.22 Contact cleaning.....	36
Figure3.23 Deposit front side metal.....	36
Figure3.24 Metal patterning.....	37
Figure3.25 Metal etching.....	37
Figure3.26 Metal cleaning.....	38
Figure3.27 Alloy.....	38
Figure3.28 Backside grinding and backside metal deposition.....	39

Chapter 4

Figure4.1 Trench etching with hard mask oxide.....	57
Figure4.2 P ⁺ gate implant that with self-align hard mask oxide and source pattern.....	57
Figure4.3 Remove hard mask oxide.....	58
Figure4.4 Deposit the LPCVD oxide as ILD.....	58
Figure4.5 Contact dry etching.....	59
Figure4.6 Define 2 nd source pattern and source implant.....	59
Figure4.7 Strip source pattern.....	60
Figure4.8 Sputter front-side metal as source electrode and alloy.....	60
Figure4.9 The schematic of two-dimension unit cell.....	61
Figure4.10 The breakdown voltage of drain to source.....	61
Figure4.11 The electric potential profile of BV _{DSX} (V _G =-4.0V).....	62
Figure4.12 The electric field magnitude at BV _{DSX} (V _G =-4.0V).....	62
Figure4.13 The breakdown voltage of gate to source.....	63
Figure4.14 The gate threshold voltage.....	63
Figure4.15 The turn-on I _D -V _D curve for R _{on,sp}	64
Figure4.16 The reverse leakage current magnitude when V _G =-0.4V and V _D =20V.....	64
Figure4.17 The forward voltage drop when I _S =10A.....	65
Figure4.18 The forward voltage drop when I _S =20A.....	65
Figure4.19 The turn-on I _D -V _D curve.....	66
Figure4.20 The turn-on electron current magnitude.....	66
Figure4.21 Trench pattern.....	67
Figure4.22 Trench hard mask oxide etching.....	67
Figure4.23 Trench etching.....	68
Figure4.24 Source pattern & P ⁺ gate implant.....	68
Figure4.25 ILD CVD oxide deposition.....	69
Figure4.26 Contact etching.....	69

Figure4.27 Source pattern & source implant.....	70
Figure4.28 Sputter front-side metal.....	70
Figure4.29 The unit cell size of three dimension simulation.....	71
Figure4.30 The BV_{DSX} curve of three dimension simulation.....	71
Figure4.31 The electric potential profile at BV_{DSX}	72
Figure4.32 The electric field magnitude profile at BV_{DSX}	72
Figure4.33 The $BV_{GS(TH)}$ curve.....	73
Figure4.34 The on-state I_D-V_D curve for $Rd_{s,on}$	73
Figure4.35 The $V_F(10A)$ curve.....	74
Figure4.36 The $V_F(20A)$ curve.....	74
Figure4.37 The schematic diagram of JFET pitch size and SBD mesa width.....	75
Figure4.38 The chart diagram of JFET pitch size vs. BV_{DSX} & $V_{GS(TH)}$	75
Figure4.39 The chart diagram of JFET pitch size vs. BV_{DSX} & $R_{on,sp}$	76
Figure4.40 The chart diagram of P^+ gate implant energy vs. BV_{DSX} & $V_{GS(TH)}$	76
Figure4.41 The chart diagram of P^+ gate implant energy vs. BV_{DSX} & $R_{on,sp}$	77
Figure4.42 The net doping profile at different P^+ gate implant energy.....	77
Figure4.43 The chart diagram of Schottky mesa width vs. BV_{DSX} & $V_{GS(TH)}$	78
Figure4.44 The chart diagram of Schottky mesa width vs. BV_{DSX} & $R_{on,sp}$	78
Figure4.45 The reverse recovery waveforms at different Schottky mesa width.....	79
Figure4.46 The chart diagram of Epitaxy resistivity vs. BV_{DSX} & $V_{GS(TH)}$	79
Figure4.47 The chart diagram of Epitaxy resistivity vs. BV_{DSX} & $R_{on,sp}$	80

Table Captions

Chapter 3

Table 3.1 Process flow of power trench JFET integrated with SBD structure	25
--	----

Chapter 4

Table 4.1 Summary table of electrical characteristics of this proposal structure compared with prior structures.....	80
--	----

