Chapter 1

Introduction

1.1 Markets and Application of Low Voltage Power Devices

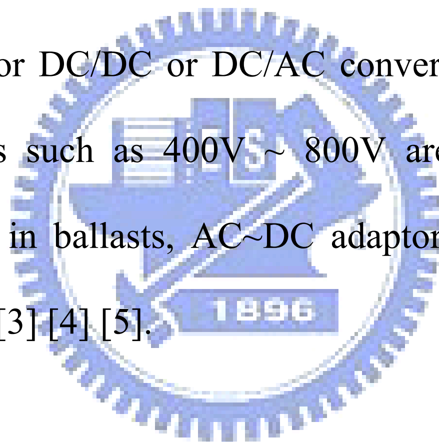
Nowadays, semiconductor industry is based on the material "silicon" of solid-state transistor to form some electrical function. Not only it has the characteristic of very small, but also lightweight, high reliability, low power consumption and easy to integrate. Those advantages make semiconductor industry growing rapidly, also is applied extensively.

In terms of electrical characteristic and application, semiconductor devices can be distinct into two groups roughly, which are integrated circuits (IC) and discrete components. The integrated circuits are made from many different semiconductor devices on the silicon surfaces, such as resistors, diodes, capacitors and transistors [1]. The integrated circuits are suitable in the application of low current rating, low power consumption and signal processing. Another type of semiconductor is discrete component. It's made from single-type device function on silicon wafers. The major application is for the different types of power supply requirement of high power, high voltage and high current rating capability.

In past several years, the discrete component devices have about 10 percentage markets of semiconductor field as showing below in Fig. 1.1 [2]. In those 10 percents of semiconductor power devices, the power transistors are dominant

products and have significant growth as shown in Figure. 1.2 [2]

The category of applications for power semiconductors in relation to their breakdown voltage and current rating is shown in Figure. 1.3, where the voltage of the devices fall around 20V ~ 30V are extensively in the applications such as boost or buck switches of DC/DC converters for CPU, peripherals of mother board, VGA card, note book, battery pack, portable and consumer products. Backside light inverter for LCD CCFL module needs 40V devices as DC/AC converter application. These devices of 20V ~ 40V are dominant products in the power application and market field. The 75V devices are made for boosters of electrical bicycles, 100V ~ 200V device are suitable for DC/DC or DC/AC converters, motor controls. In the higher breakdown voltages such as 400V ~ 800V are suitable for over-voltage protection of primary side in ballasts, AC~DC adaptors, power factor correction, switch mode power supply [3] [4] [5].



1.2 Motivation

As the abilities of semiconductor process and circuit design improved greatly, the microprocessor units are required in terms of Systems-on-One-Chip (SOC) consideration and also be faster and more powerful. Consequently, the chip designers design million or billion transistors into specific chip area. When boosting such many operations of transistors carried out every second, the load current must be increased [6]. In the point view of power supply, the low voltage power devices

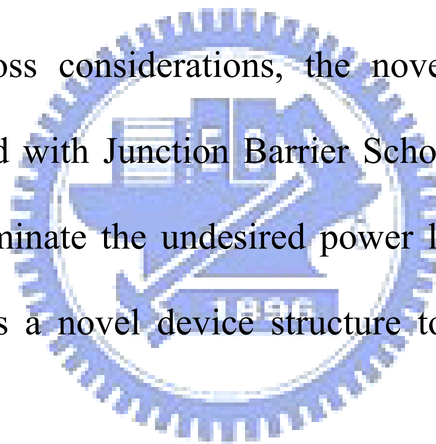
also have same kind of destiny. The challenge has been firmly required tinier and higher current density such as supporting 100A capability in the given package size for the next generation DC-to-DC converter application [7].

In term of synchronous buck converter structure of power supply, it is good candidate for step down DC-to-DC conversion application. Conventionally, we adopt Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) to be either Control-FET (High-side switch) or Sync-FET (Low-side switch) for the synchronous buck converter as showing below Fig. 1.4. But there are some major issues when designing buck converters with MOSFET devices:

- **On-state channel resistance:** In physical point of view, the on-state current from drain to source which passes few nanometers depth of surface silicon and the channel resistance exits when gate biasing. At this meanwhile, we repeat lots of unit cell of MOSFET to increase its channel width in order to approach low on-resistance ($R_{ds,on}$) of MOSFET, which requires large chip size, especially for the Sync-FET. In the finite package size and PCB area, cost effectiveness is major consideration.
- **Conduction power loss:** When the MOSFET enters the ohmic region from the active region to complete the transient, the inherent body diode of MOSFET results in conduction loss are proportional to its forward voltage drop (V_F) multiplied by the loading current [8]. The conducting power loss affects the power efficiency directly. However, the typical forward voltage drop of silicon PN junction is around 0.7V ~ 0.8V.

- **Transition power loss:** Another power loss source of MOSFET is coming from diode reverse recovery effectiveness. It is inherently existed in the body diode. The reverse recovery characteristic is forward conducting body diode transited from forward bias to reverse bias, which results in undesired current flowing when diode turns off. There are several techniques developed to eliminate the reverse recovery [9] [10]. The simplest method of limiting the effectiveness is to embed Schottky diode into MOSFET according to Schottky diode has very low reverse recovery charge (Q_{rr}) that is able to decrease undesired current magnitude directly.

Based on above power loss considerations, the novel structure junction effect transistor (JFET) embedded with Junction Barrier Schottky Diode (JBS) is a good alternative solution for eliminate the undesired power loss and improve efficiency [8]. This research proposes a novel device structure to implement the improving characteristics.



1.3 Application Guideline

With high cell density of trench junction field effect transistor can implement ultra-low on-resistance for DC-to-DC switching application, especially for low side FET of synchronous buck converters. Adding Schottky diode is good solution for improving reverse recovery problem. The structure of Junction Field Effect Transistor (JFET) integrated with Junction Barrier Schottky diode (JBS) can

eliminate the diode reverse recovery issue and implement the low reverse leakage current, low forward voltage drop and low on-resistance embedded in internal FET structure. The structure of JFET integrated with JBS allows the same current handling area of switch transistor without compromising the size of the transistor or its $R_{ds, on}$ value [8]. Fig. 1.5 is the topology of synchronous buck converter with JFET integrated with JBS used for step down DC-to-DC conversion application [11].

Another suitable application is designed for stand-by power module in some special requirement such as stand-by mode of DDR module. It is implemented by using normal-on characteristic of junction field effect transistor, which dissipates very low power and provides an enhanced efficiency [11] [12].

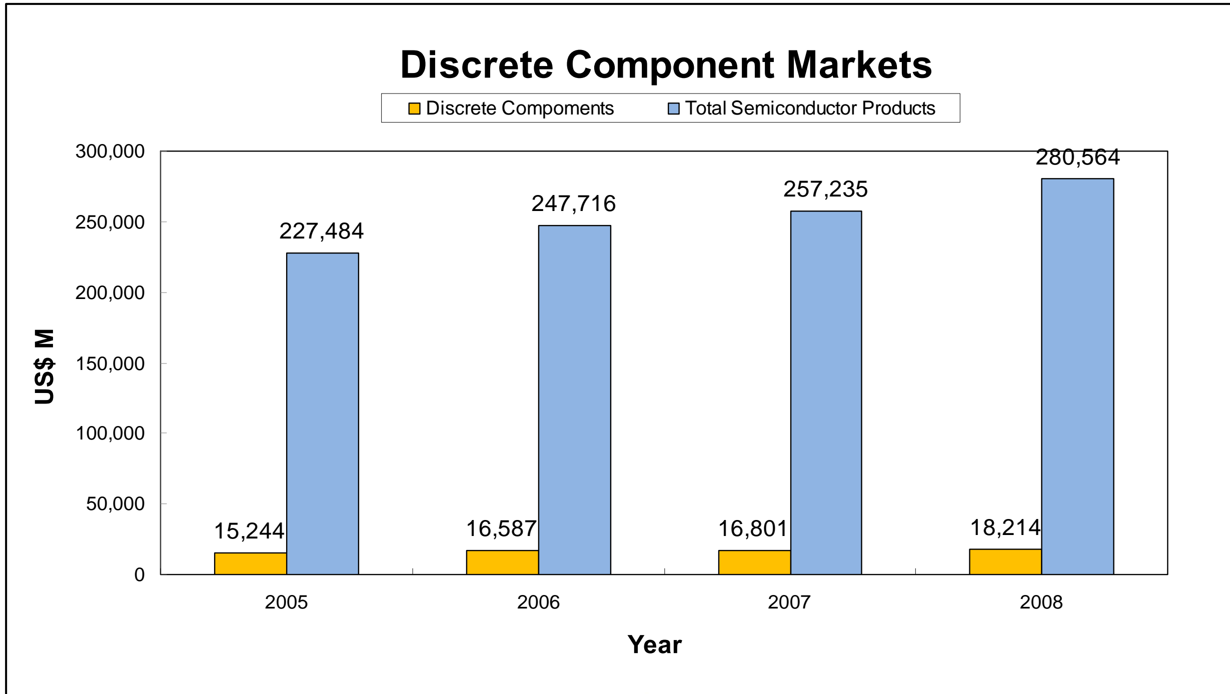


Figure 1.1 Discrete component markets.

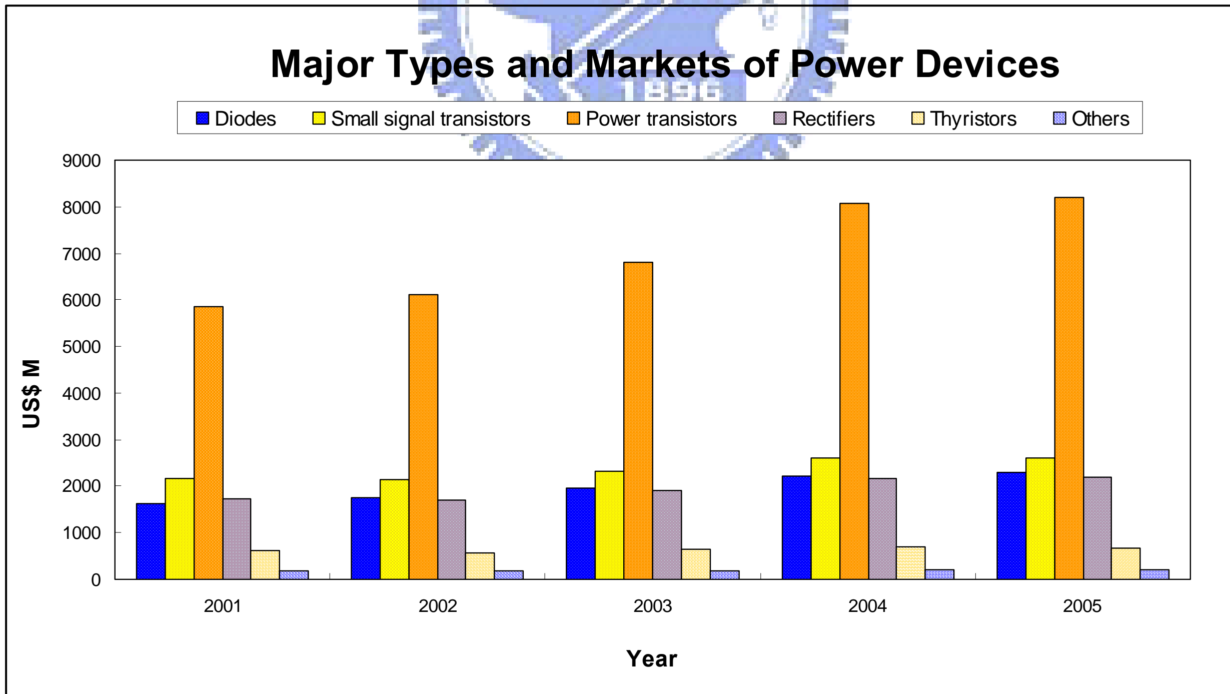


Figure 1.2 Major types of power devices and its markets.

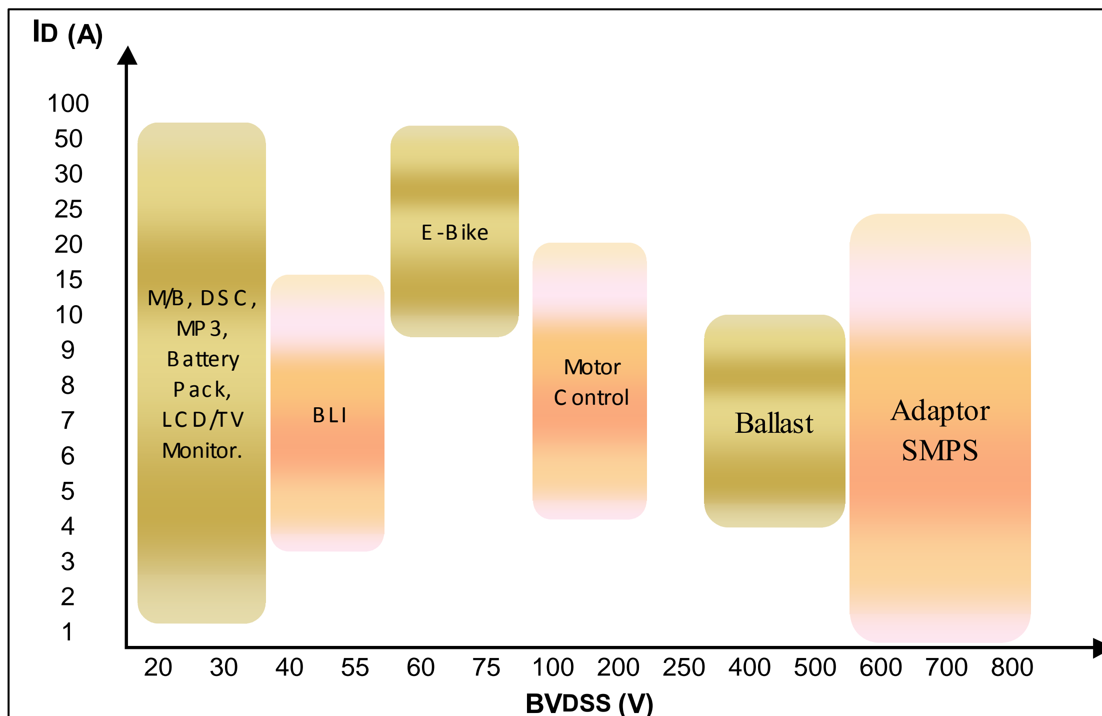


Figure 1.3 Application for power devices in relation to their voltage and current rating.

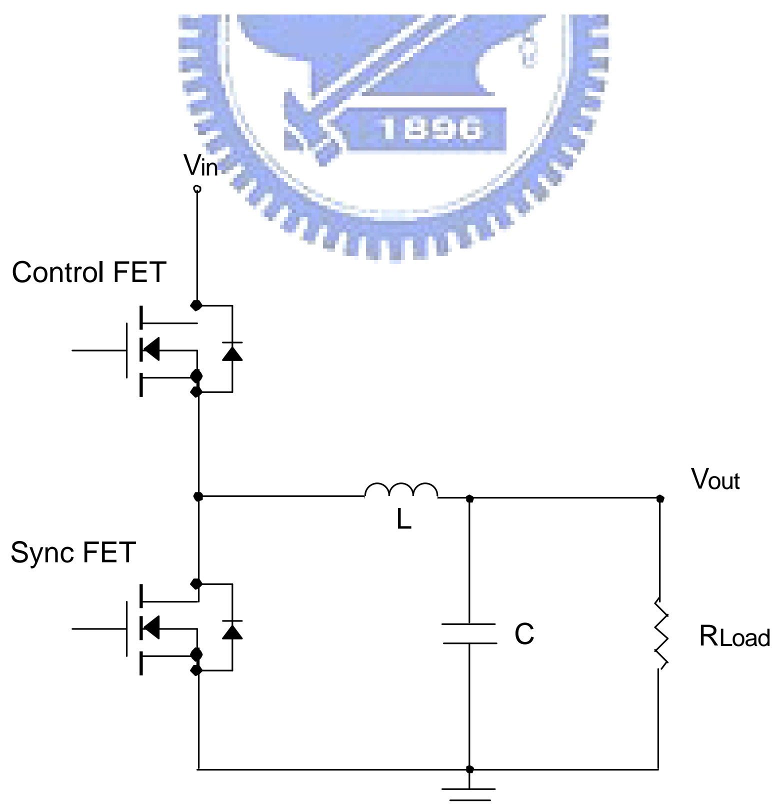


Figure 1.4 Synchronous buck converter implemented by MOSFET.

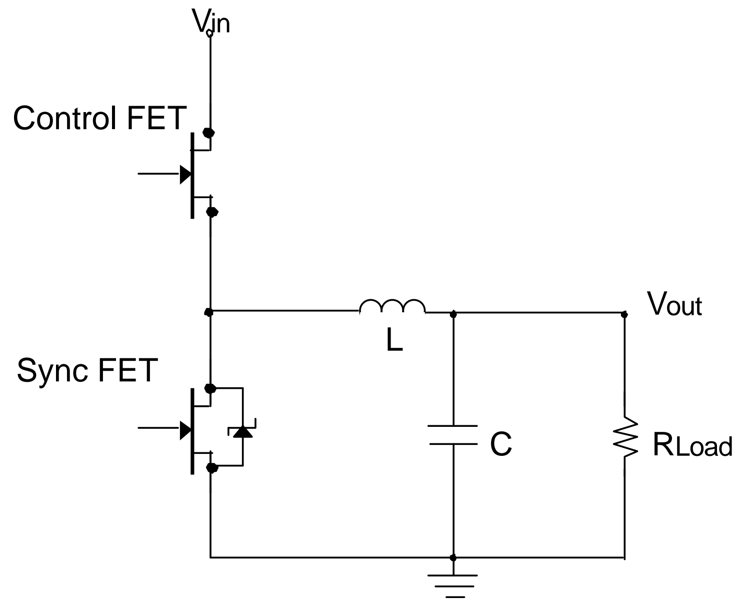


Figure 1.5 Synchronous buck converter implemented by JFET integrated with JBS.

Chapter 2

Review of Junction Field Effect Transistor and Schottky Diode

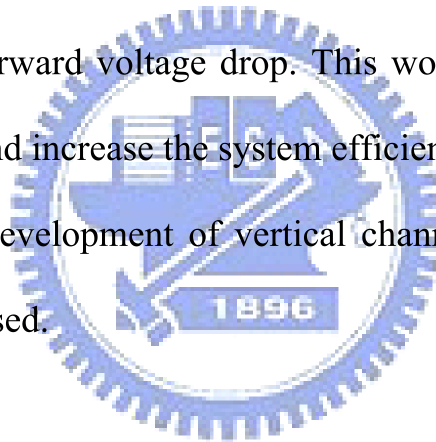
2.1 Introduction

In 1925, the Austro-Hungarian physicist J. E. Lilienfeld invented a transistor structure which was controlled by electric field. This structure has a metallic plate on the top of semiconductor and two metal contacts on each side. Forcing voltage on metallic plate makes electric field forming at the surface of semiconductor and controls the current flow between these two contact pads. This was the first concept of field effect transistor [14]. In 1952, William Shockely introduced Junction Field Effect Transistors (JFETs) [15]; Dacay and Ross improved the JFET structure in 1953 [16]. With the great improvement of Metal-Oxide-Semiconductor technology initially developed for integrated circuits (ICs), the Power MOSFETs become available in the late 1970s.

In 1938, Boris Davydov, Nevill Mott and Walter Schottky explained the phenomenon and theories of electron concentration on semiconductor surface separately. The theories are about forming an asymmetric barrier of hetero-junction between metal and semiconductor [17]. Until 1964, J. R. Baird of Texas Instruments proposed using a metal-semiconductor diode, named Schottky Barrier Diode, to

shunt charge around the bipolar transistor [18]. Therefore, Schottky's name became to a familiar technique that works through eponymous diode theory, which was developed in 1930s. The current in Schottky diode is based on major carrier transport, which is different from inherent minority carrier storage characteristic of PN junction diode that has a limitation of maximum operation frequency. Thus, Schottky diode can switch faster than PN junction diode. Another characteristic consideration of PN junction diode is its on-state forward voltage drop just about 0.7V ~ 0.8V, even if the device is in the low reverse blocking mode application. Due to the lower barrier height is between metal and semiconductor, Schottky diode can implement 0.3V ~ 0.6V forward voltage drop. This would make lower power loss during on-state operation and increase the system efficiency greatly.

In this chapter, the development of vertical channel MOSFET and Schottky barrier diode will be discussed.



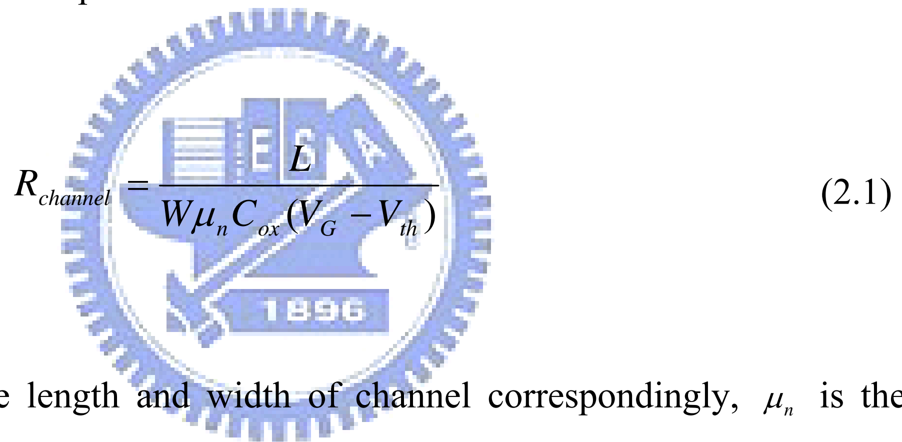
2.2 Vertical Channel MOSFETs

Planar technology of semiconductor process is based on lateral channel structure concept, such as devices with gate, drain and source electrode on the same surface of silicon wafer. Its advantage is available for integrated circuits, but not for high power rating. On the other hand, MOSFET can be implemented in vertical channel structure when source and drain electrode are on the opposite surfaces of the silicon wafer. This is more suitable for high power rating as more available area

between source and drain region.

2.2.1 Basic MOSFET

Consider a basic n-channel enhancement Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) having a P-type base region and N^+ source/drain structures as shown in Fig. 2.1, the conducting channel current under gate terminal is controlled by electrons transport in inversion layer of P-type base silicon surface when the gate biasing at positive voltage. The channel resistance from drain to source of MOSFET can be expressed as



$$R_{channel} = \frac{L}{W\mu_n C_{ox}(V_G - V_{th})} \tag{2.1}$$

where L and W are the length and width of channel correspondingly, μ_n is the surface mobility of electrons, C_{ox} is the oxide capacitance, V_G is gate voltage and V_{th} is threshold voltage [13]. However, if L is too small, punch-through phenomenon occurs easily. This conventional MOSFET structure is not suitable for high voltage application.

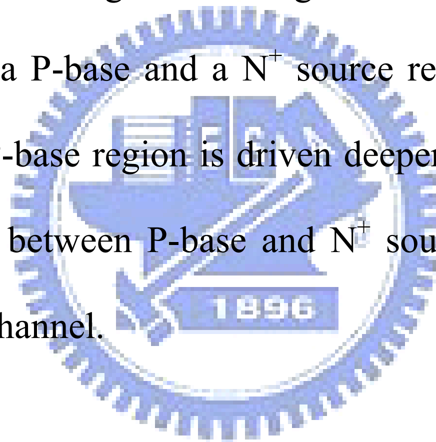
2.2.2 VMOS

The VMOSFET is fabricated from the blanket P-base region first, which followed the N^+ source region. The V-shape grooves etch through N^+ region by

preferential etch (KOH-alcohol solvent) and aligned with the [110] orientation on the surface of the slice, as shown in Fig. 2.2 [19]. However, VMOSFET was 1st commercialized power MOSFETs. But, it has the unstable process window during manufacturing and high electric field occurred in the tip of gate, which resulted in reliability problems.

2.2.3 DMOS

As the cross-section of device structure in Fig. 2.3, it is fabricated with double diffusion process by using self-alignment along the common window between two poly-silicon gates forming a P-base and a N^+ source region. Normally it is named DMOS. According to the P-base region is driven deeper than N^+ source region, the lateral diffusion difference between P-base and N^+ source regions that under gate electrode is called surface channel.



2.2.4 UMOS

In the early 1990s, the reactive ion etching technology was developed and widely being used in semiconductor process. The U-shape groove MOSFET has been explored in the power MOSFET application.

The fabrication of UMOSFET is etching a trench structure into silicon first, then forms gate oxide along the U-groove shape and fill-in doped poly-silicon. It finally forms blanket P-base region and N^+ source island as the cross-section shown in Fig. 2.4. The major advantage of UMOSFET structure is having a higher channel

density than either VMOS or DMOS structures, which allows great reduction of on-resistance.

2.3 Junction Field Effect Transistors

The phenomenon that about conductivity of a semiconductor is modulated by an electrical field applied perpendicular to surface of semiconductor, which is called field effect. This section focuses on the development of junction field effect transistors.

2.3.1 Lateral Channel Junction Field Effect Transistor

The first junction field effect transistor (JFET) was proposed by W. Schokley in 1952 [15]. Dacey and Ross built more operation analysis of JFET in 1953. Schematic diagram is showing in Fig. 2.5 [16]. PN junctions forms underlying semiconductor of metallic plates. Right and left contacts are named as source and drain terminals respectively. In this JFET structure, the depletion regions formed by PN junctions and modulate channel conductivity directly. The modern version of JFET is showing in Fig. 2.6. Although its structure is different from the one mentioned above, its electric operation is originally coming from Schokley's proposal.

2.3.2 Vertical Channel Junction Field Effect Transistor

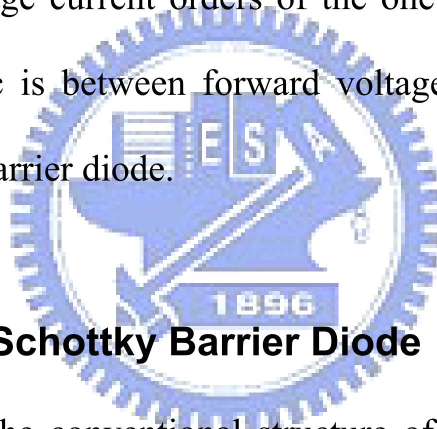
As the requirement of high current rating capability on a single chip, integrating many channels is the most popular solution; therefore, vertical channel JFET is more suitable for this sort of structure. The well-known structure is using buried diffused gate region, where is under source implant region. In spite of the diffused gate and source regions are fabricated easily, low source-to-gate breakdown voltage becomes to its major disadvantage. Base on this situation, O. Ozawa ed. proposed a structure with self-aligned process and planar doped poly-silicon technology to achieve high channel density, current capability and high source-to-gate breakdown voltage. Its structure is showing in Fig. 2.7 [17].

2.3.3 Trench-Type Junction Field Effect Transistor

Based on the structure of trench-type MOSFET, one novel structure of trench-type JFET has been proposed as shown in Fig. 2.8 [7]. In this JFET structure, the diffused trench gate is fabricated by using heavy P^+ implantation after trench etching. Then, fill CVD oxide into the trench structure as isolation layer between gate and source terminals. The channel exists in the adjacent two P^+ gates, and while the reverse bias applied on P^+ gates, the channel is depleted. Soon after, the transistor turns off.

2.4 Schottky Barrier Diodes

A metal in contact with a low doped semiconductor would form rectifying contact, i.e. Schottky Barrier Diode. The current transport mechanism in the Schottky barrier diode is different from the one in the PN junction. Because the unipolar carrier transport characteristic of Schottky barrier diode inherently, it can switch faster than PN junction diode. Additionally, the low metal-semiconductor barrier height of Schottky diode, its turn-on voltage is smaller than the one in the PN junction diode. However, according to this low barrier height of Schottky diode, its magnitude of reverse leakage current orders of the one in the PN junction diodes. The trade-off characteristic is between forward voltage drop and reverse leakage current exists in Schottky barrier diode.



2.4.1 Conventional Schottky Barrier Diode

The Fig. 2.9 shows the conventional structure of Schottky barrier diode. Its disadvantage is low reverse breakdown voltage, and large reverse leakage current. Several studies focus on adding PN junction guard ring around the metal semiconductor junction to improve its reverse breakdown voltage and reverse leakage current as shown in Fig. 2.10 [20] [21] [22].

2.4.2 Junction Barrier Schottky Diode

The low Schottky barrier height makes decreasing of the forward voltage drop, increasing of reverse leakage current, and reduction of maximum operating

temperature. In addition, the barrier-height lowering effect also is able to soften breakdown characteristic under reverse biasing. An improving structure of Schottky barrier diode integrated PN junction grid into drift region is called Junction Barrier Schottky Diode (JBS), its structure shows in Figure 2.10 [13].

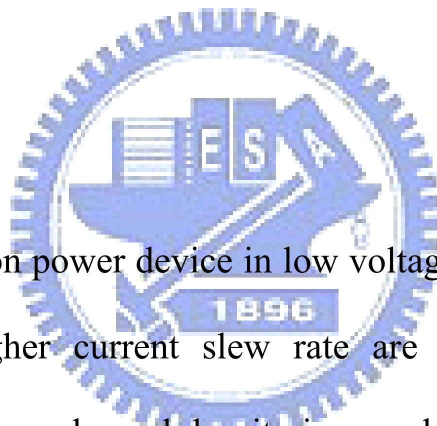
In the JBS structure, the depletion region of PN junction grids would pinch-off the n-channel drift region in a positive voltage applied on the N^+ substrate. The pinching-off channel prevents the image force lowering phenomenon and decreases the magnitude of reverse leakage current. It allows the JBS to design for high reverse blocking voltage and less soft breakdown characteristic.

2.4.3 Trench MOS Barrier Schottky Diode

Although, the Junction Barrier Schottky Diode (JBS) is good candidate for very low forward voltage drop, high switching speed and low blocking voltage capability, but it is difficult to shrink the feature size due to the quite amount of dead space under the P^+ junction region. In order to achieve smaller PN junction grid, M. Mehrotra and B. J. Baliga domo a novel structure, Trench MOS Barrier Schottky Rectifier (TMBS) [23]. Its structure shows in Figure 2.11. Compared TMBS structure with JBS, TMBS has absence of lateral diffusion from the P^+ junction grid under the Schottky interface, the process-controlled mesa width and the doping concentration of epitaxial layer can modulate the forward conduction characteristics. The reverse blocking voltage can be modulated by epitaxial doping concentration, trench depth and oxide thickness in the trench structure. Additionally, the high

electric field occurs in the sharp corners of trench bottom, far away the Schottky interface. It can reduce the barrier-height lowering phenomenon greatly.

More recent research shows that the TMBS structure can be easily integrated into trench MOSFET structure, which is for forming the integration structure of MOSFET and Schottky Barrier Diode (MOSBD). Its cross section shows in Figure 2.12 [24]. This novel integrating structures of MOSFET and SBD are effective to reduce the reverse recovery charge (Q_{rr}), the forward voltage drop (V_f) and parasitic inductance in conventional multi-chip package design.



2.5 Conclusion

For the next generation power device in low voltage regulator module (VRM), the large current and higher current slew rate are required for high loading microprocessors. Having more channel density in one chip is necessary. Trench-like structure is good solution for this purpose and good candidate for minimizing the device feature size, lower cost effectiveness in further.

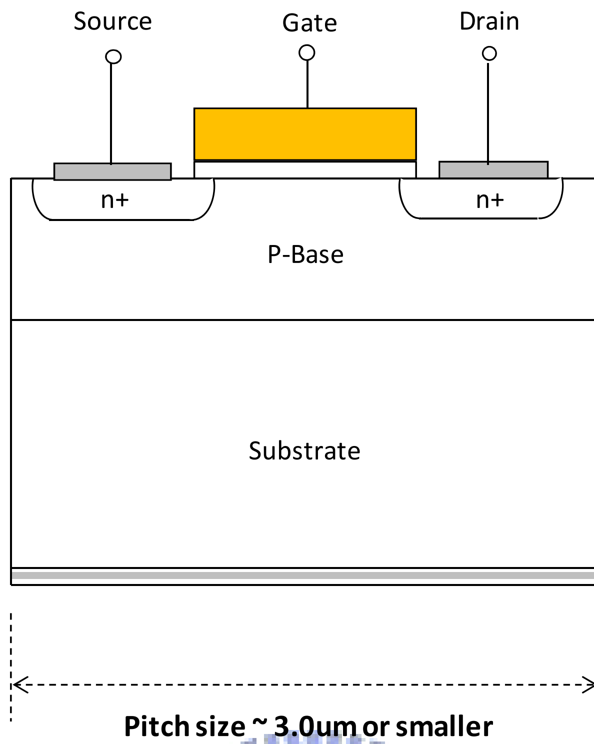


Figure 2.1 A basic MOSFET structure.

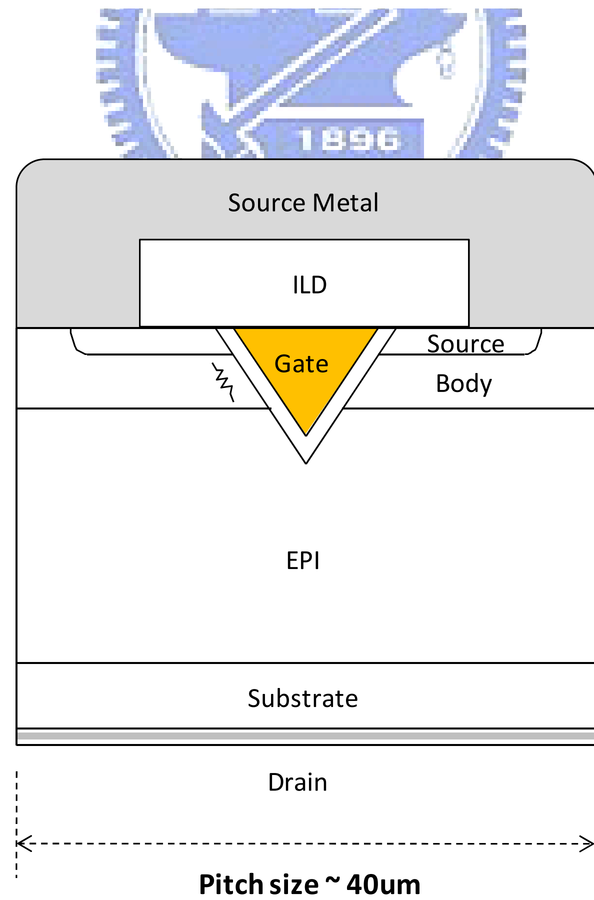


Figure 2.2 A VMOSFET structure.

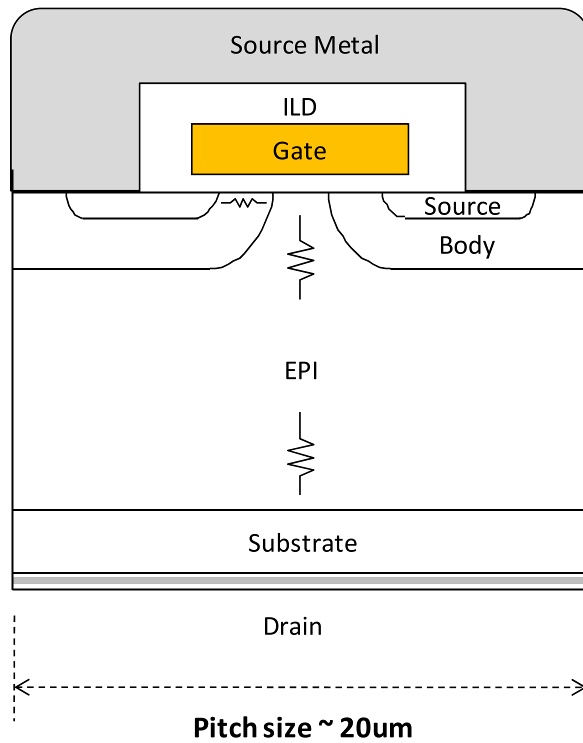


Figure 2.3 A DMOSFET structure.

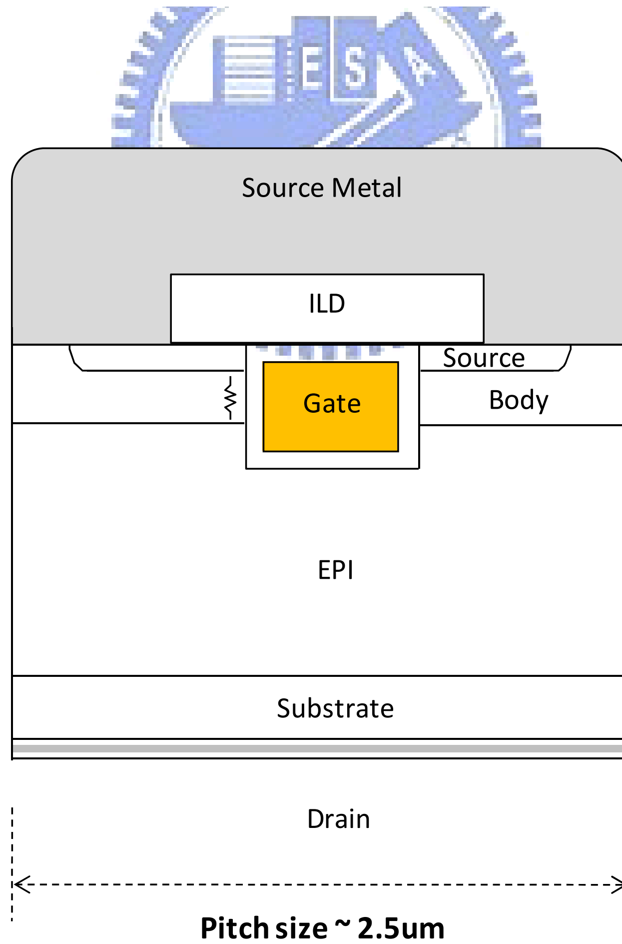


Figure 2.4 A UMOSFET structure.

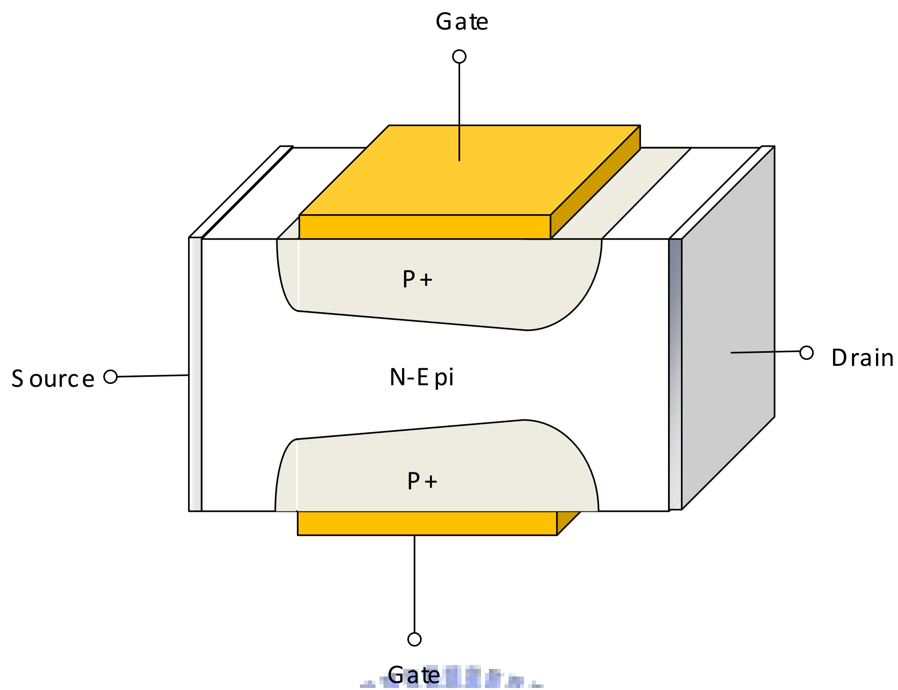


Figure 2.5 A junction field effect transistor (JFET) [15] [16].

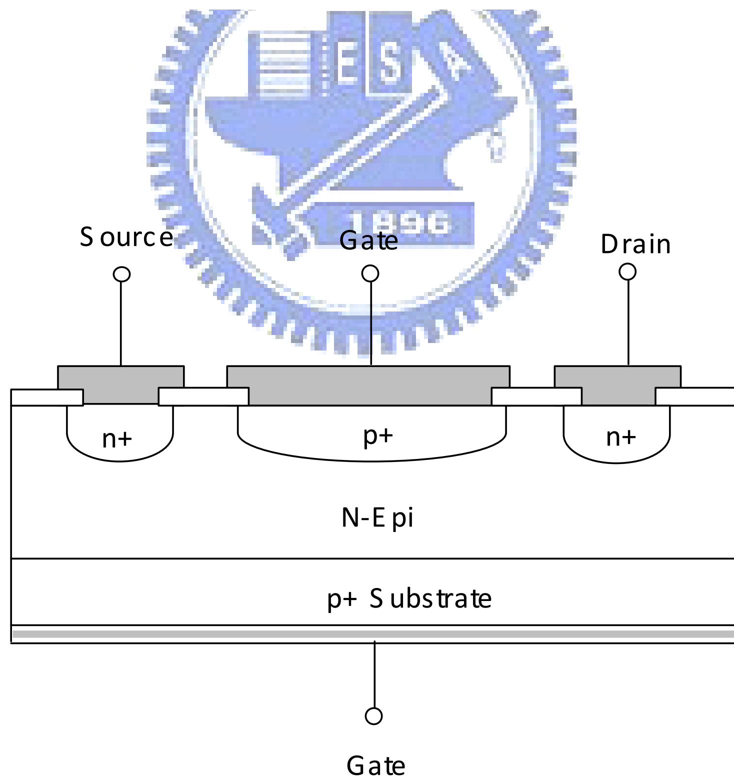


Figure 2.6 A modern version of lateral channel junction field effect transistor.

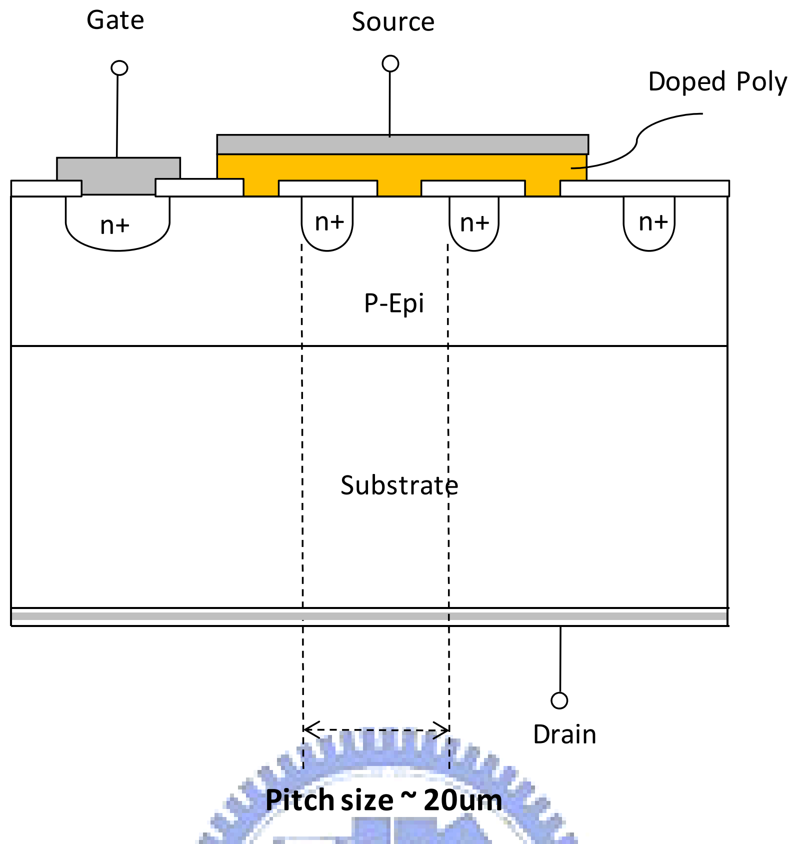


Figure 2.7 A vertical channel JFET structure using silicon planar technology [17].

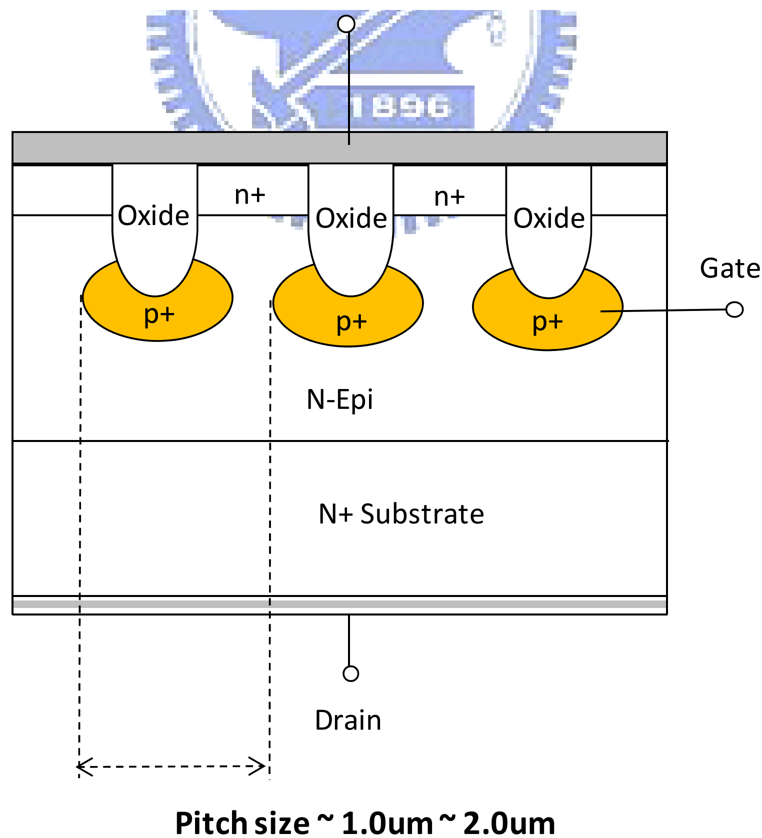


Figure 2.8 A trench-type JFET structure [7].

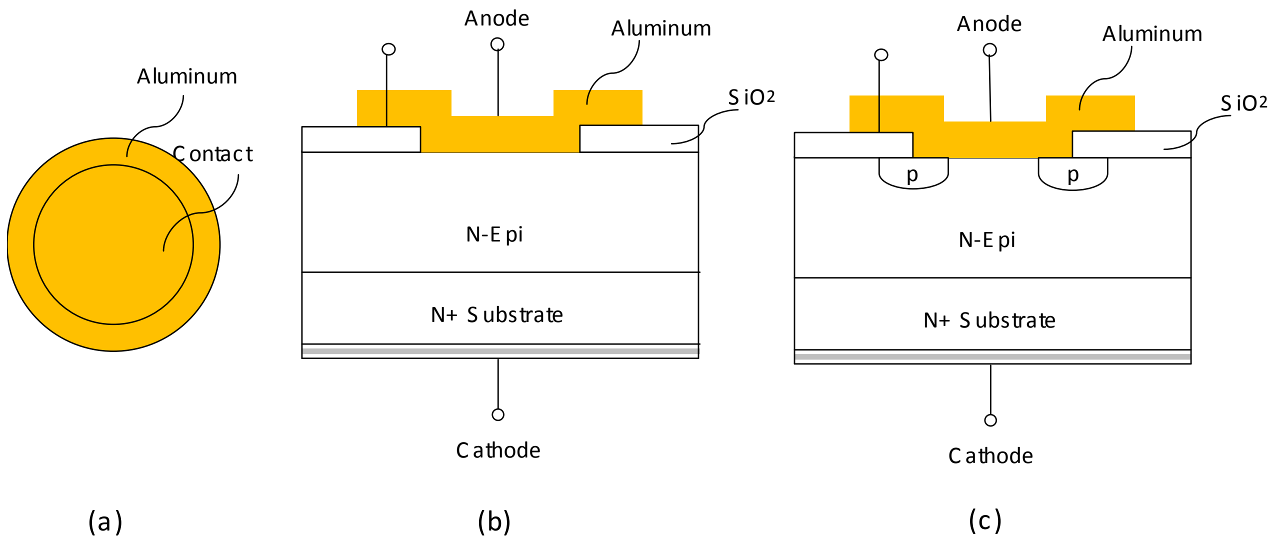


Figure 2.9 An Al-Si Schottky structure: (a) Top view geometry; (b) Conventional metal overlap Schottky diode; (c) Schottky diode with guard ring [20] [21[[22].

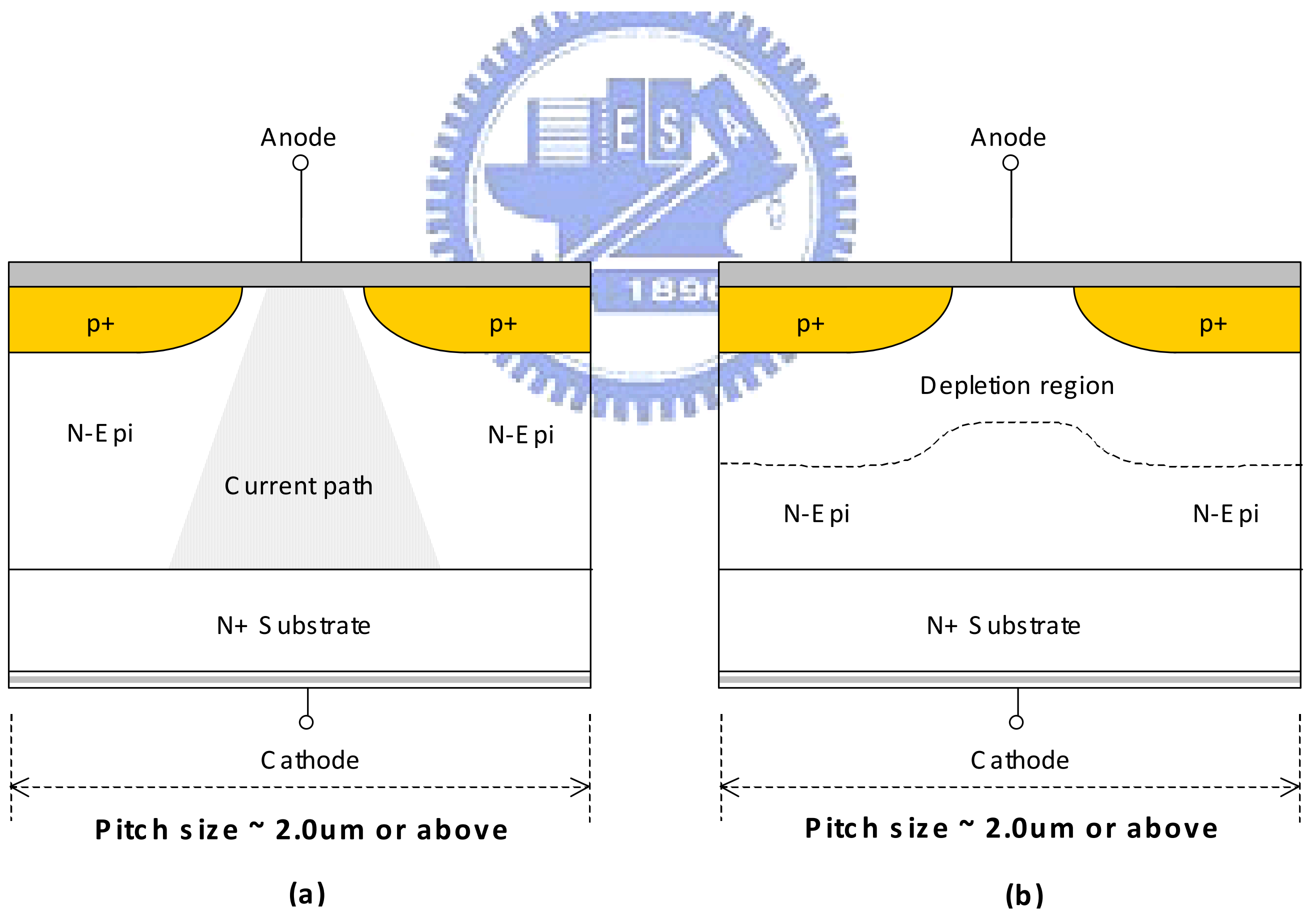


Figure 2.10 Junction barrier Schottky diode structure: (a) Forward conduction mode; (b) Reverse blocking mode.

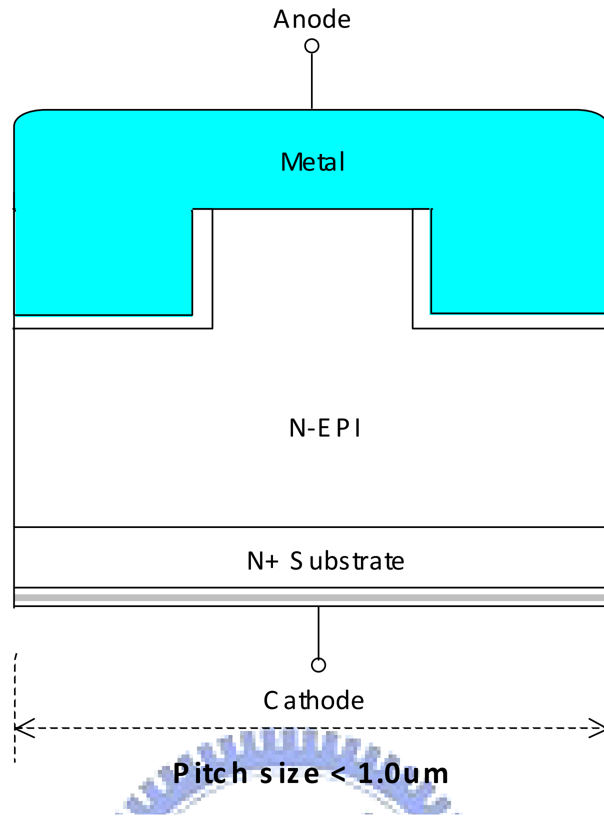


Figure 2.11 A Trench MOS barrier Schottky diode (TMBS) structure.

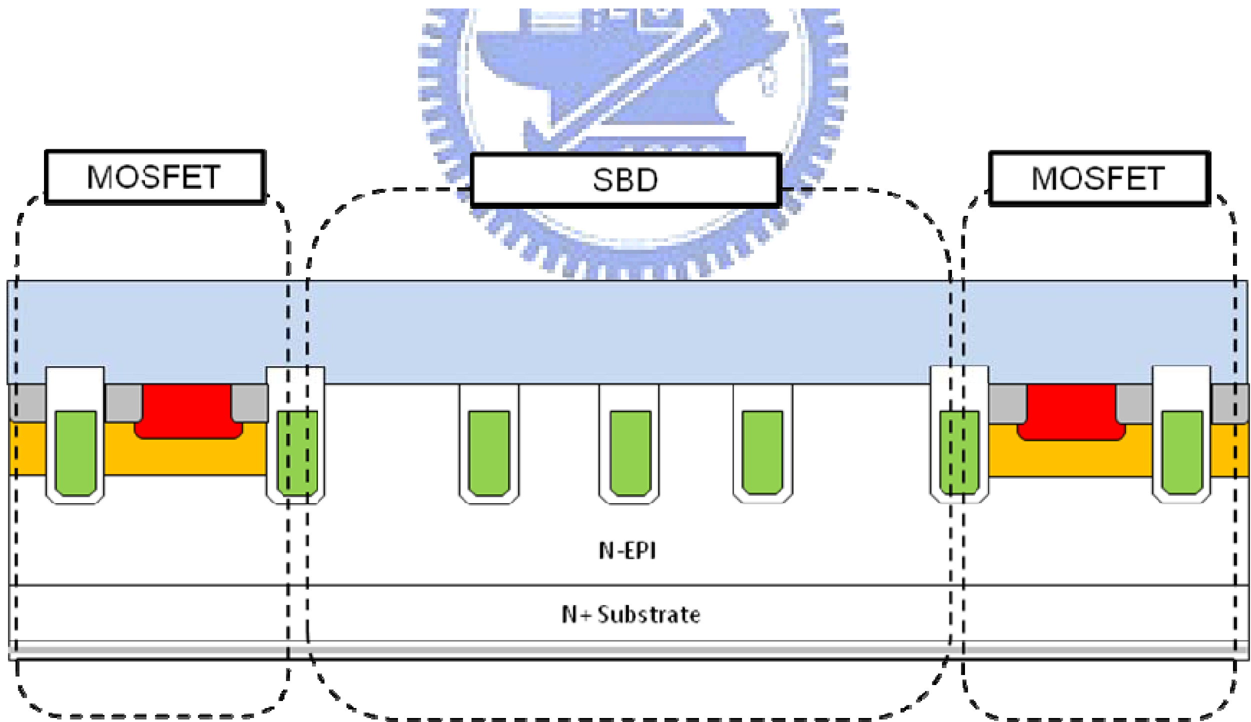


Figure 2.12 An integration structure between trench MOSFET and trench MOS barrier Schottky diode (TMBS) [24].

Chapter 3

Fabrication of Trench JFET Integrated with Schottky Barrier Diode

3.1 Device Structure

The proposed device structure in this research is shown in Figure 3.1. There are two portions in the main cell area, one is Junction Field Effect Transistor (JFET); the other is Schottky Barrier Diode (SBD).

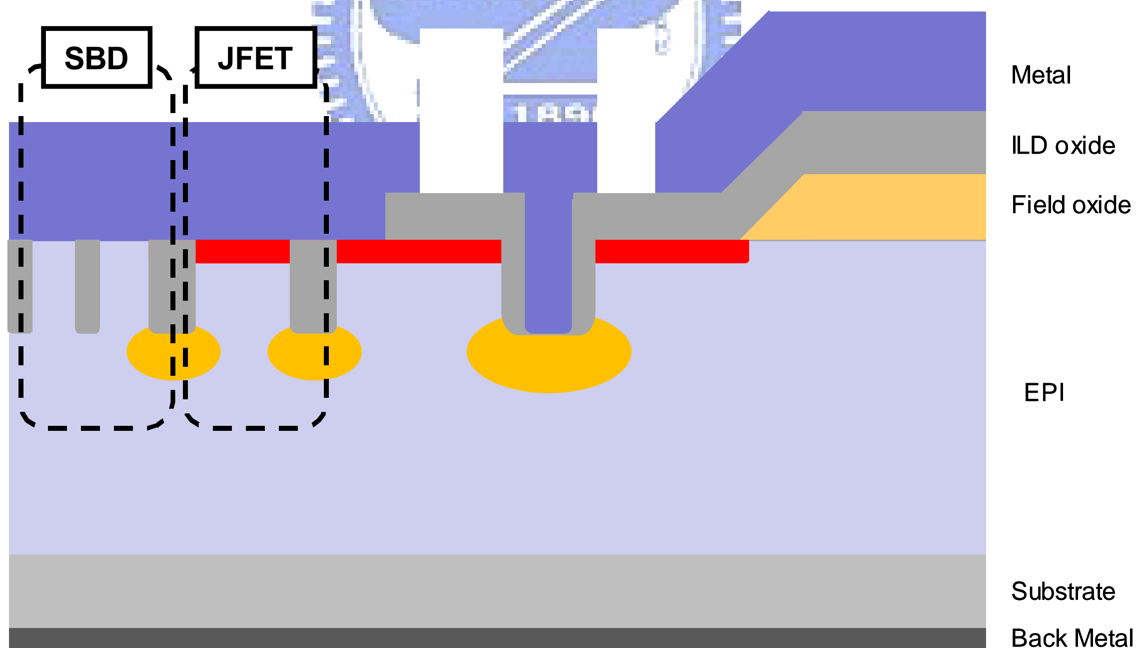


Figure 3.1 Proposed power trench JFET integrated with SBD structure.

3.2 Process Flow

The process flow of power trench JFET integrated with SBD in this experiment is shown in the following table:

Sequence	Process Description	Mask	Schematic
1	Heavily doped N-type substrate wafer.	-	Fig 3.2
2	Growth of a lightly doped N-type epitaxial layer.	-	
3	Growing and patterning of a thick field oxide.	AA	Fig 3.3~3.6
4	Source patterning and source implantation.	NP	Fig 3.7~3.9
5	Deposit hard mask oxide.	-	Fig 3.10
6	Trench patterning, hard mask oxide etching & cleaning.	TR	Fig 3.11~3.13
7	Trench etching.	-	Fig 3.14
8	Source patterning.	NP	Fig 3.15
9	P^+ gate implantation and cleaning.	-	Fig 3.16~3.17
10	Remove hard mask oxide.	-	Fig 3.18
11	Deposit ILD CVD oxide.	-	Fig 3.19
12	Contact patterning, contact etching & contact cleaning.	CT	Fig 3.20~3.22
13	Deposit front-side metal.	-	Fig 3.23
14	Metal patterning, etching & cleaning.	M1	Fig 3.24~3.26
15	Alloy.	-	Fig 3.27
16	Backside grinding & backside metal	-	Fig 3.28

Table 3.1 Process flow of power trench JFET integrated with SBD structure.

Figure 3.2 Prepare N^+ substrate and N-Epi.

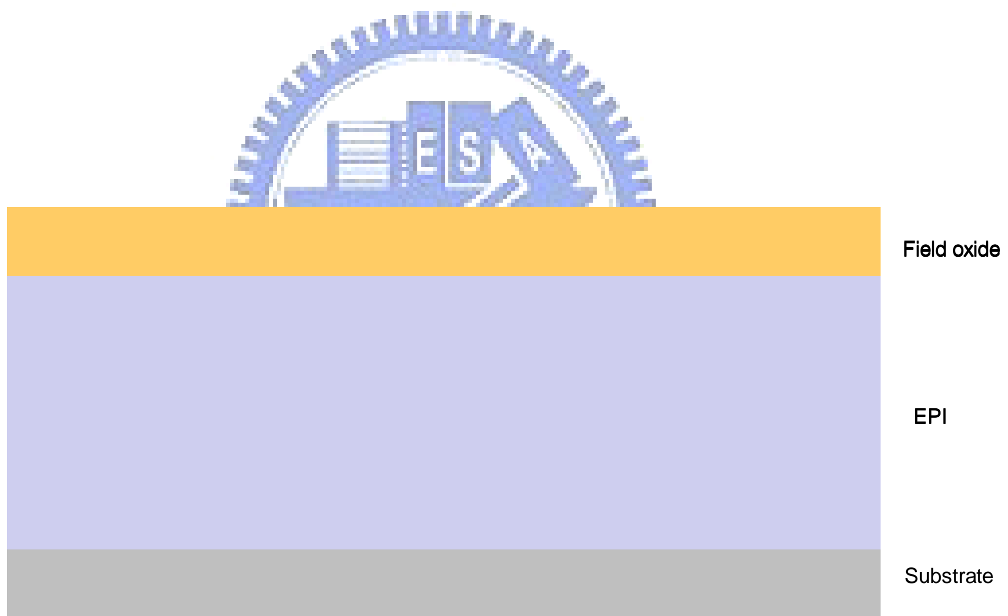


Figure 3.3 Grow field oxide.

Figure 3.4 AA patterning.

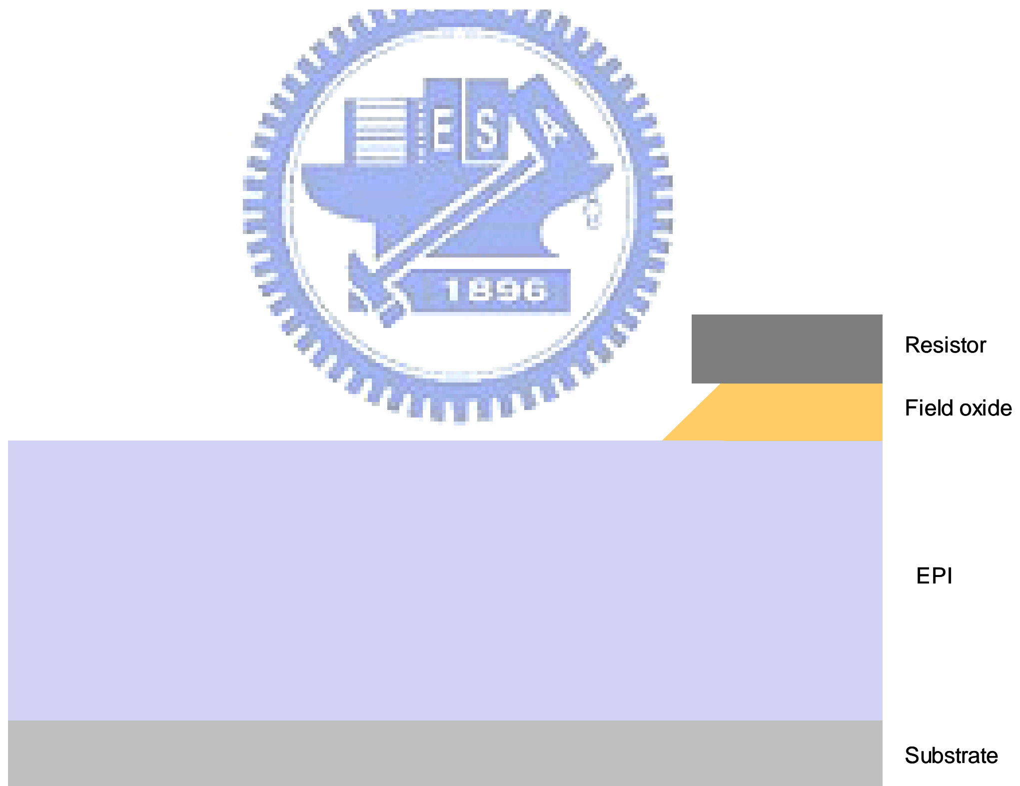


Figure 3.5 AA wet etching.

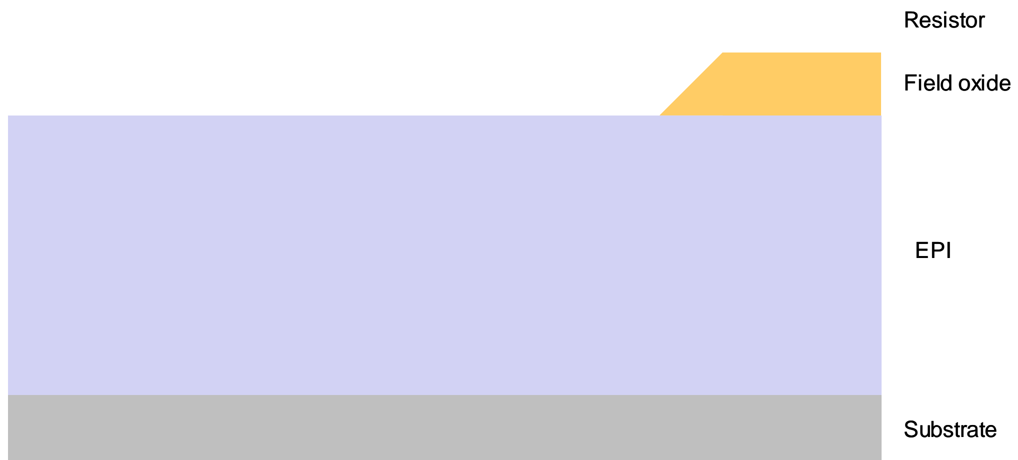


Figure 3.6 AA cleaning.

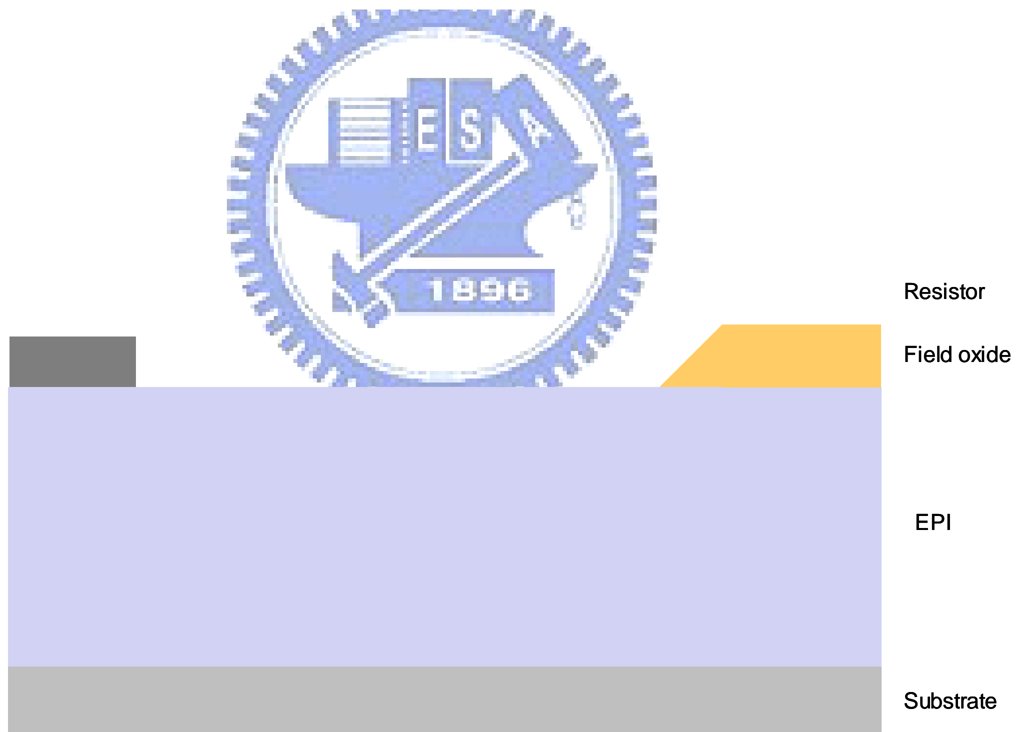


Figure 3.7 Source patterning.

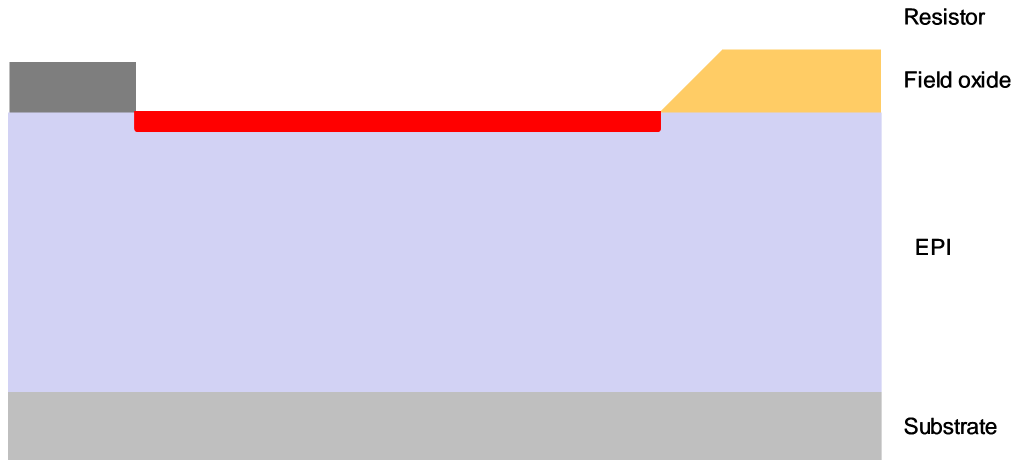


Figure 3.8 Source implant.

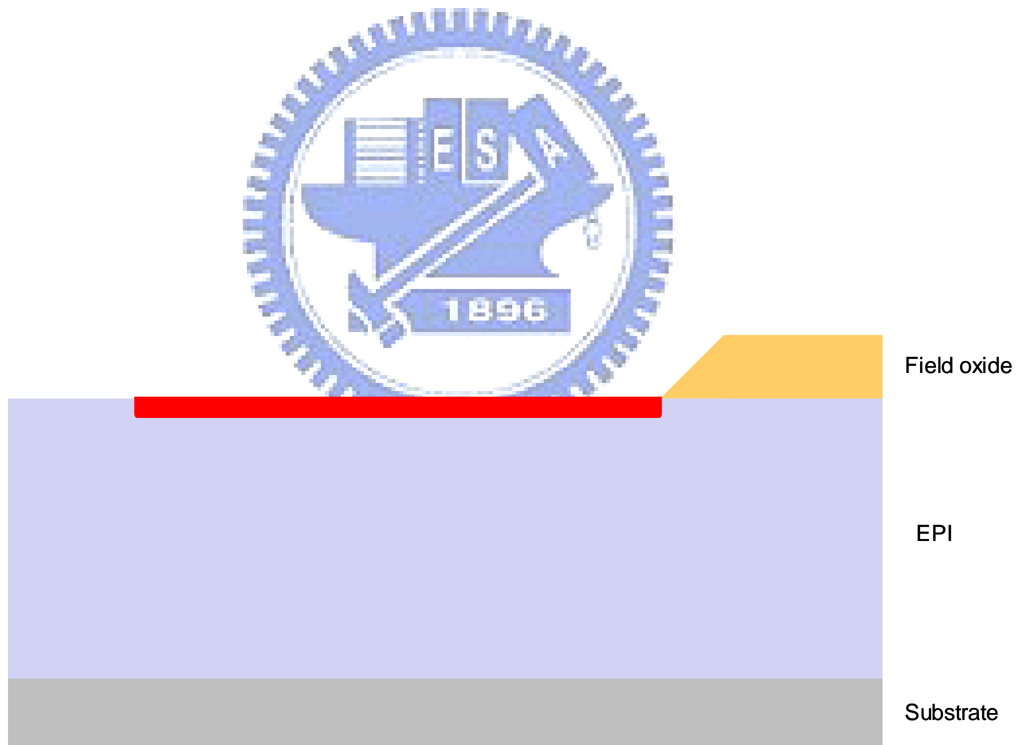


Figure 3.9 Source cleaning.

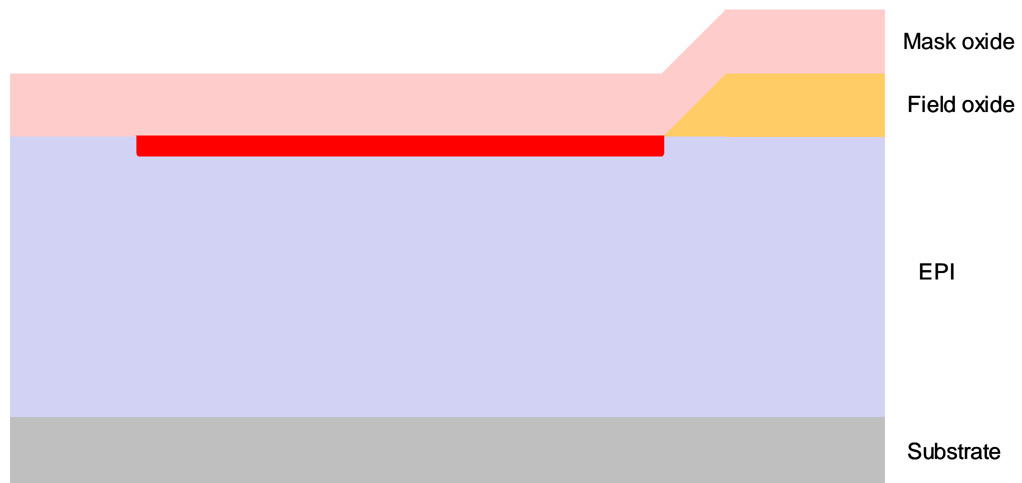


Figure 3.10 Deposit hard mask oxide.

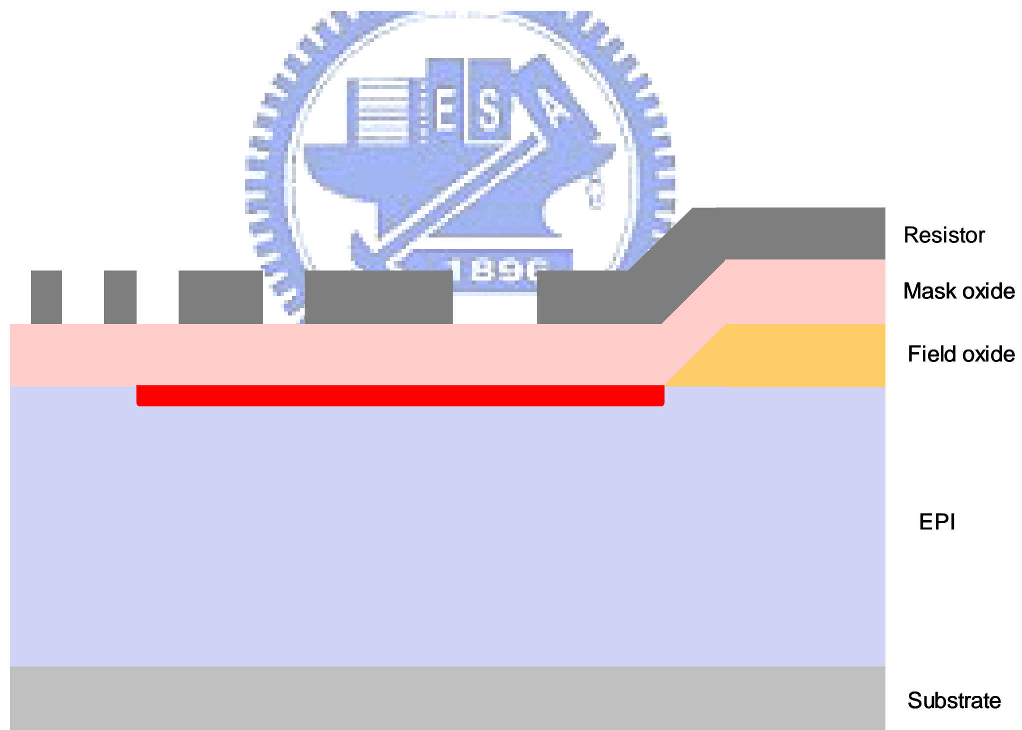


Figure 3.11 Trench patterning.

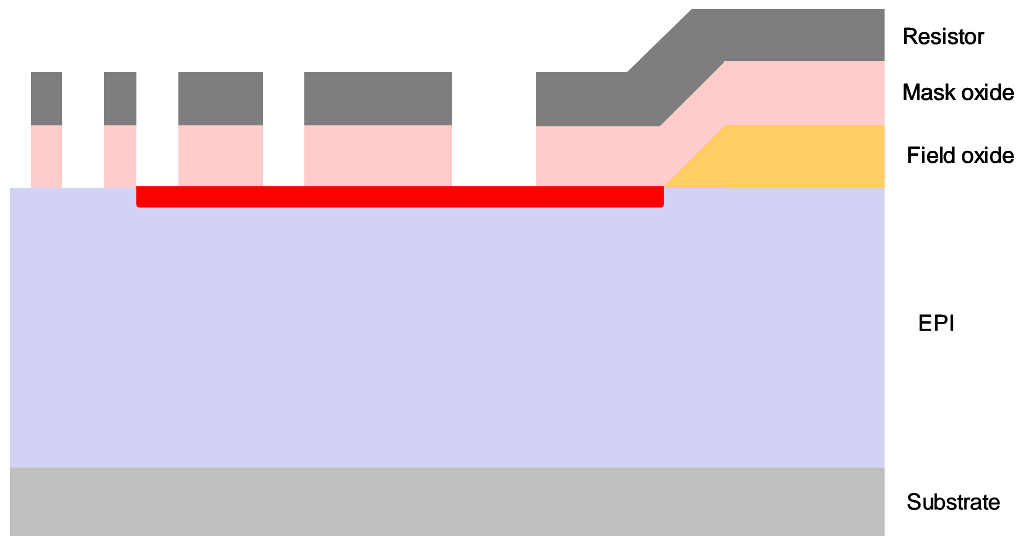


Figure 3.12 Hard mask oxide etching.

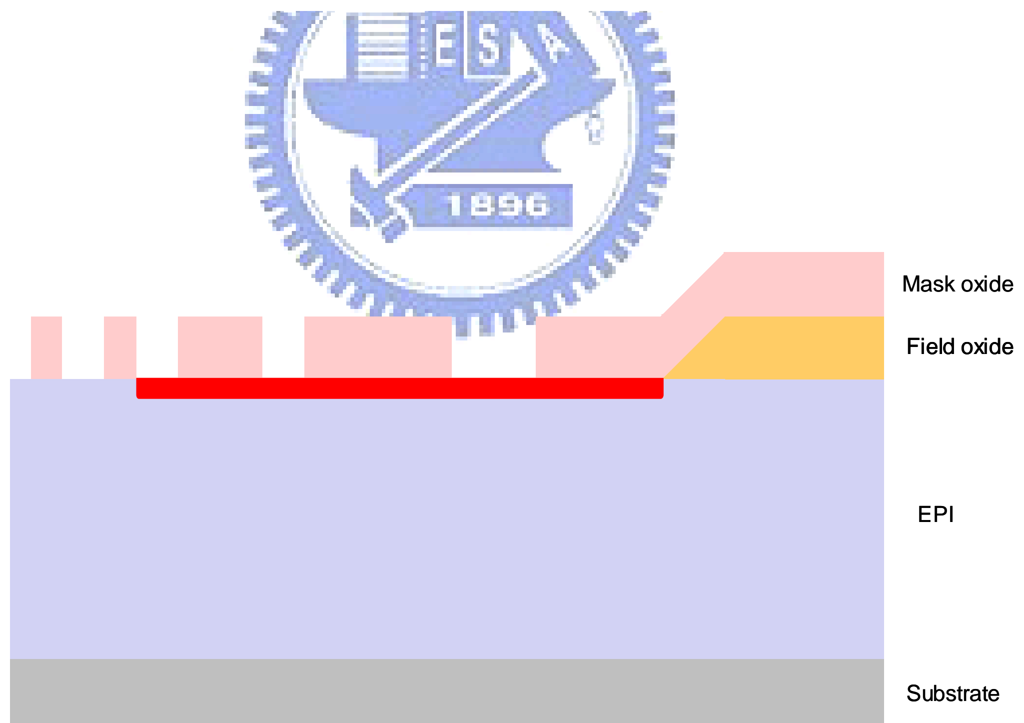


Figure 3.13 Trench cleaning.

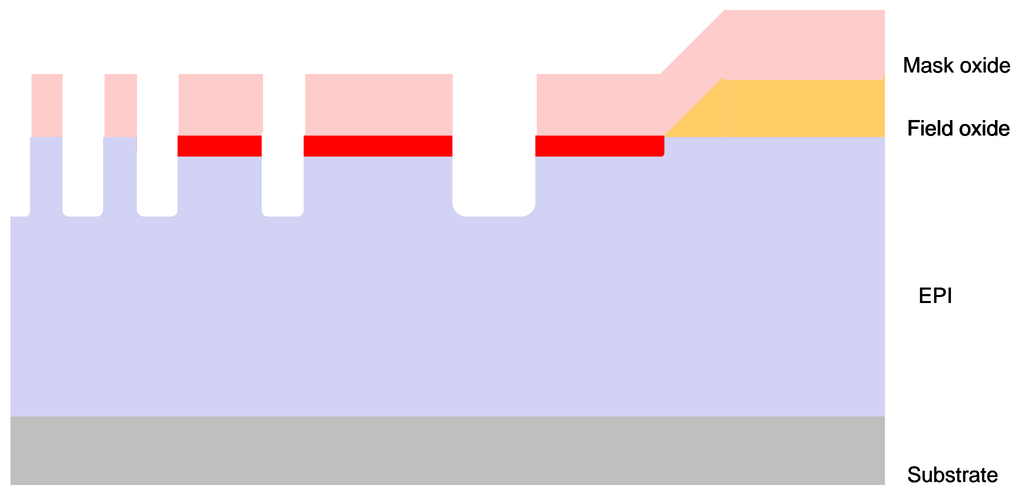


Figure 3.14 Trench etching.

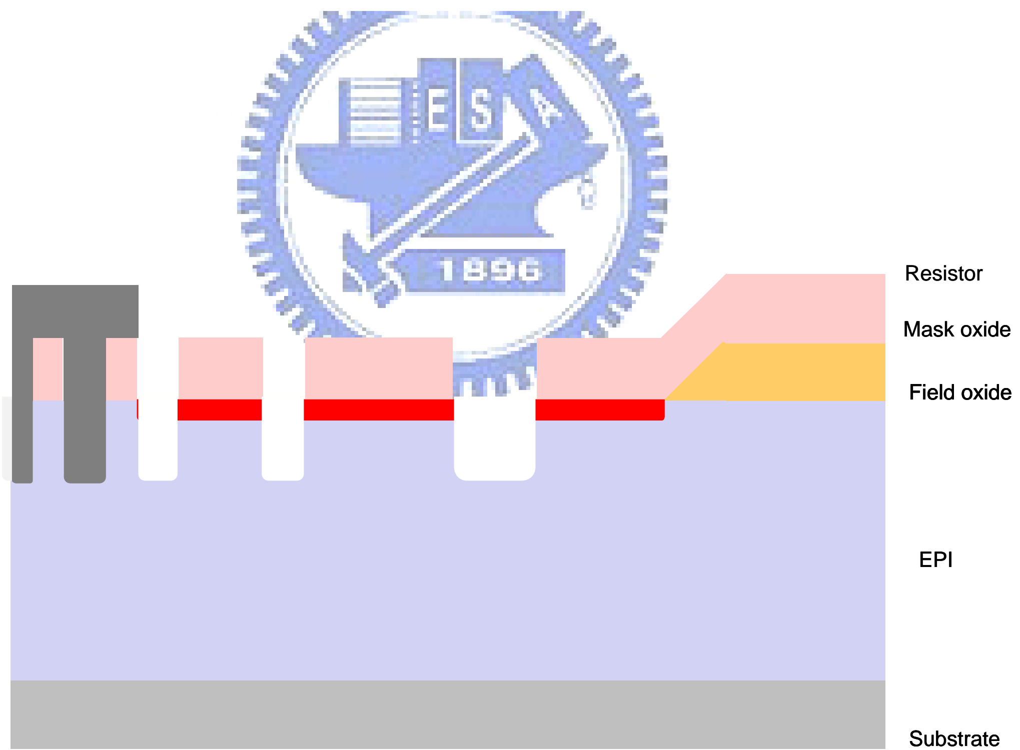


Figure 3.15 Source patterning.

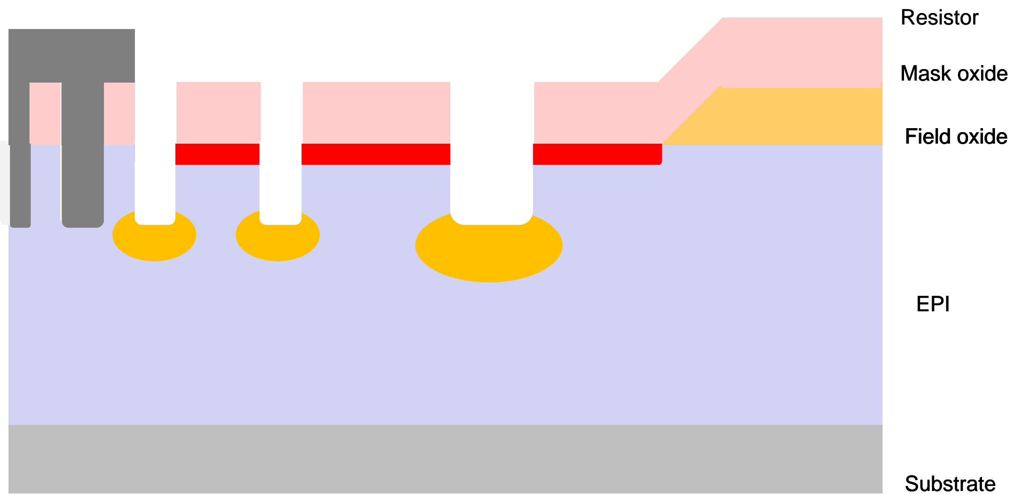


Figure 3.16 P^+ gate implant.

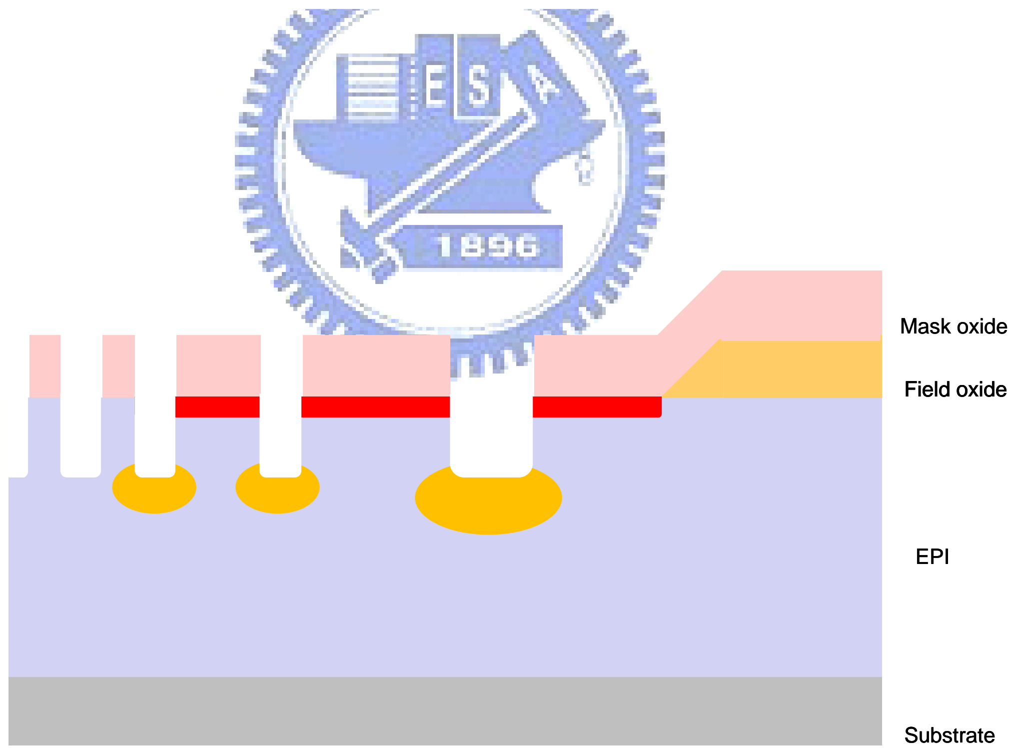


Figure 3.17 Source cleaning.

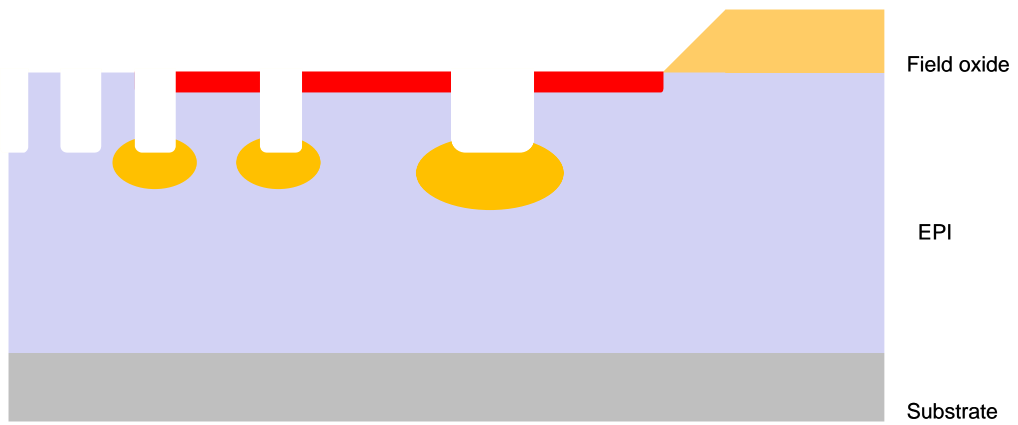


Figure 3.18 Remove hard mask oxide.

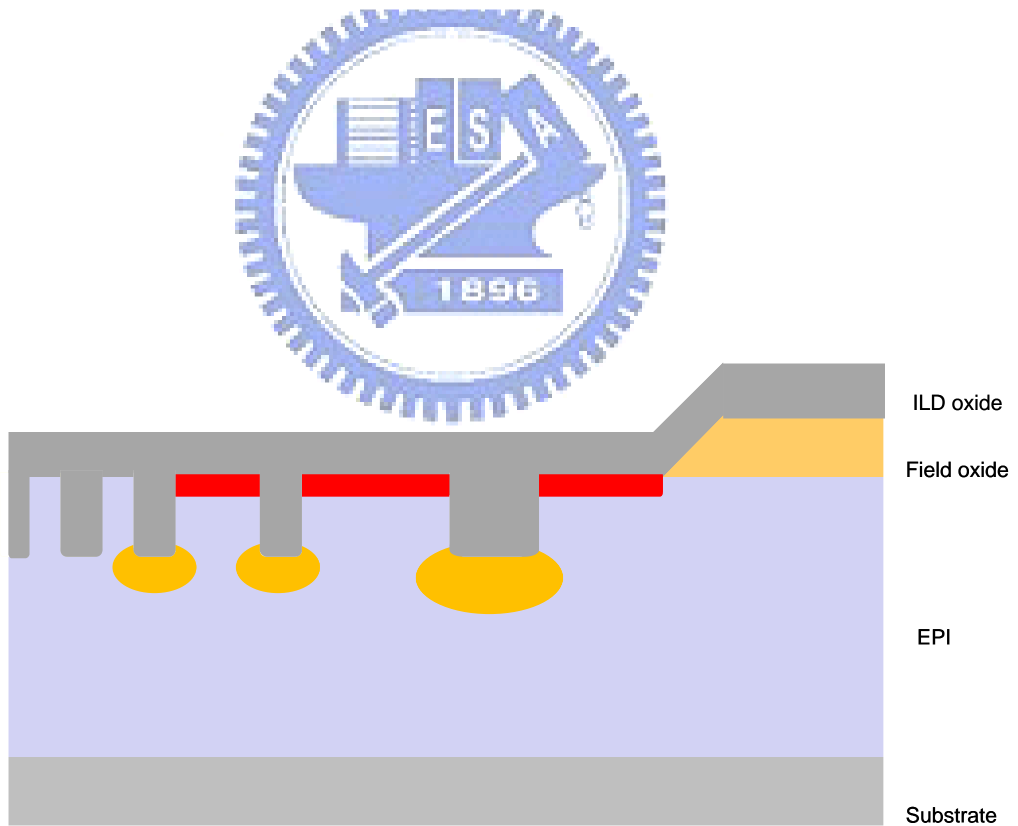


Figure 3.19 Deposit ILD-CVD oxide.

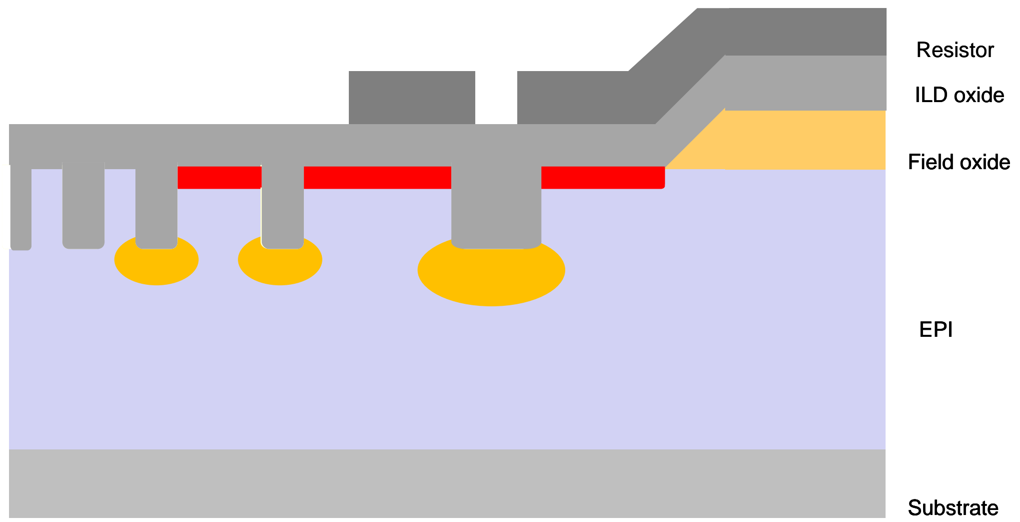


Figure 3.20 Contact patterning.

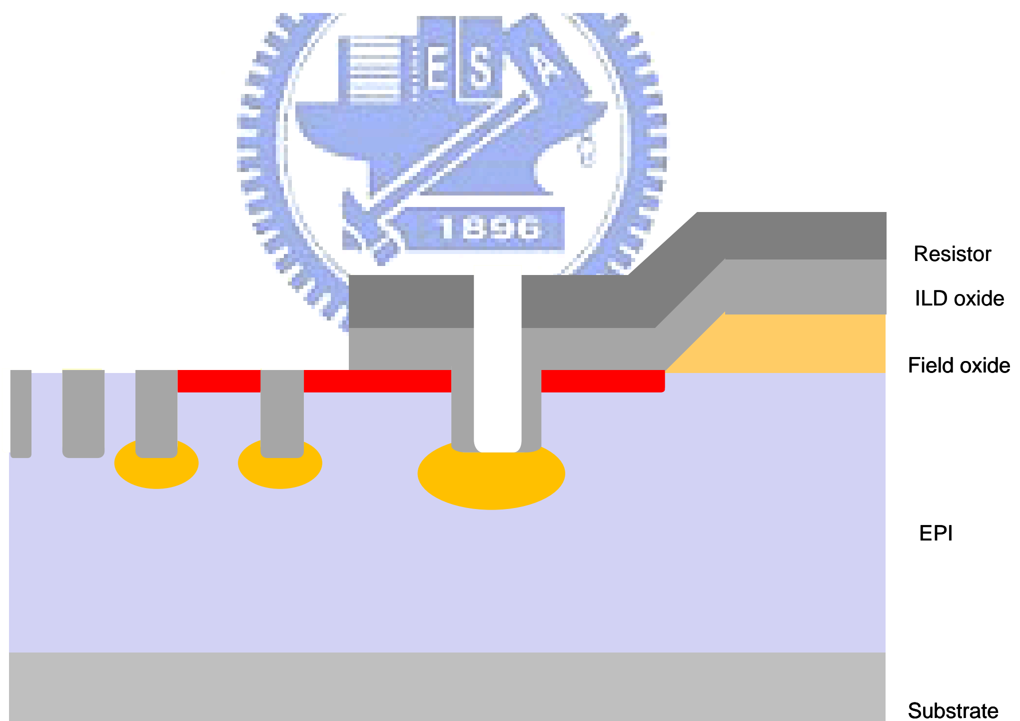


Figure 3.21 Contact etching.

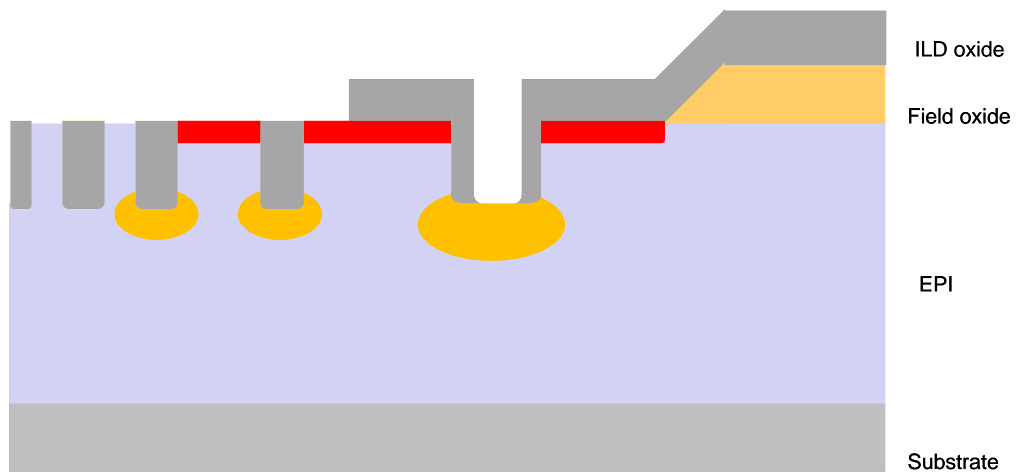


Figure 3.22 Contact cleaning.

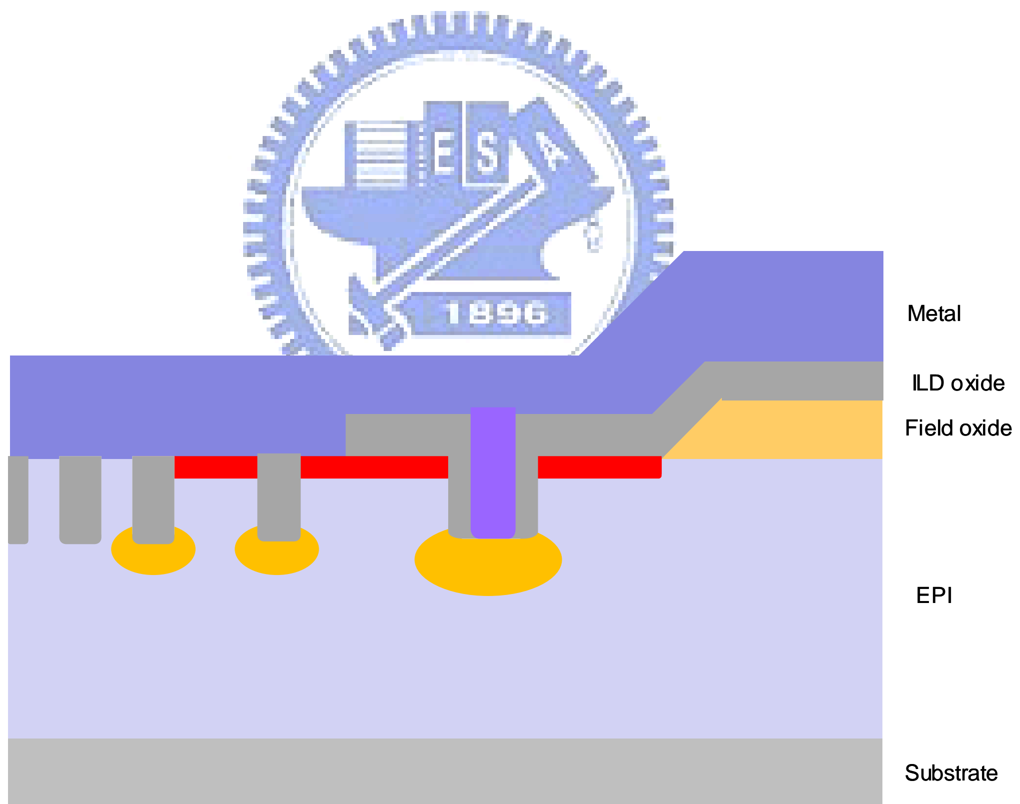


Figure 3.23 Deposit front side metal.

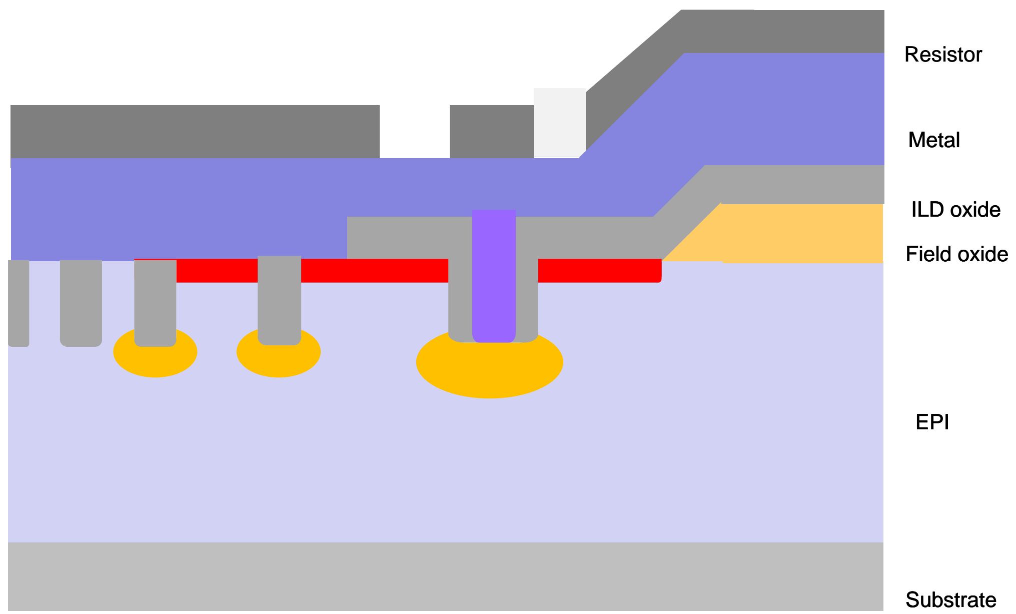


Figure 3.24 Metal patterning.

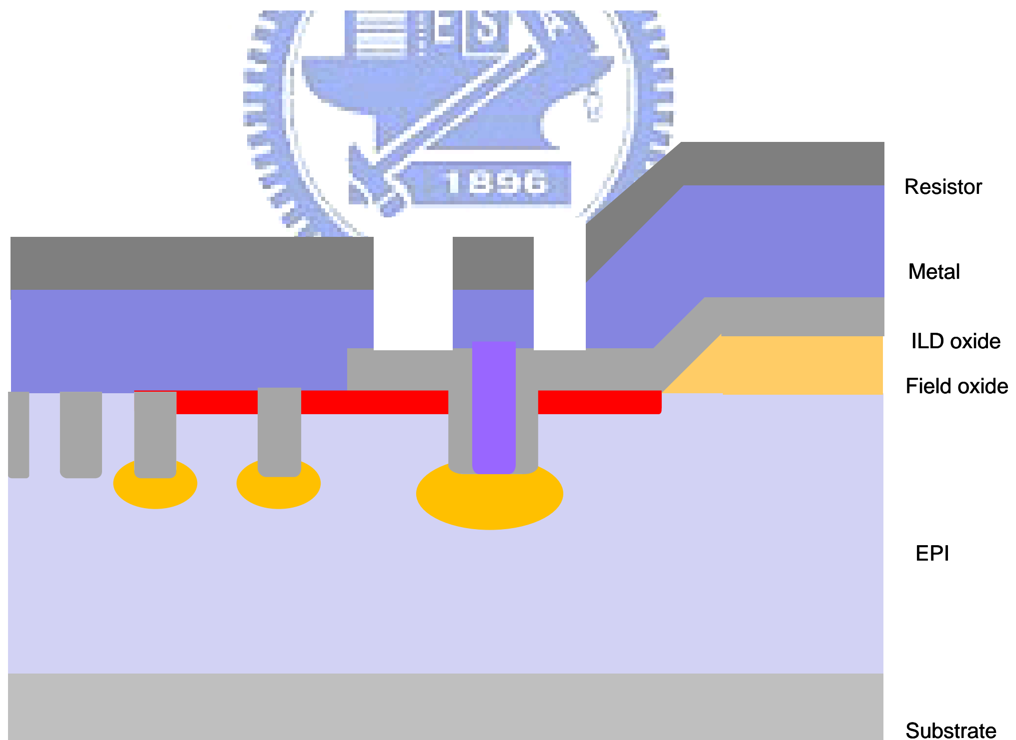


Figure 3.25 Metal etching.

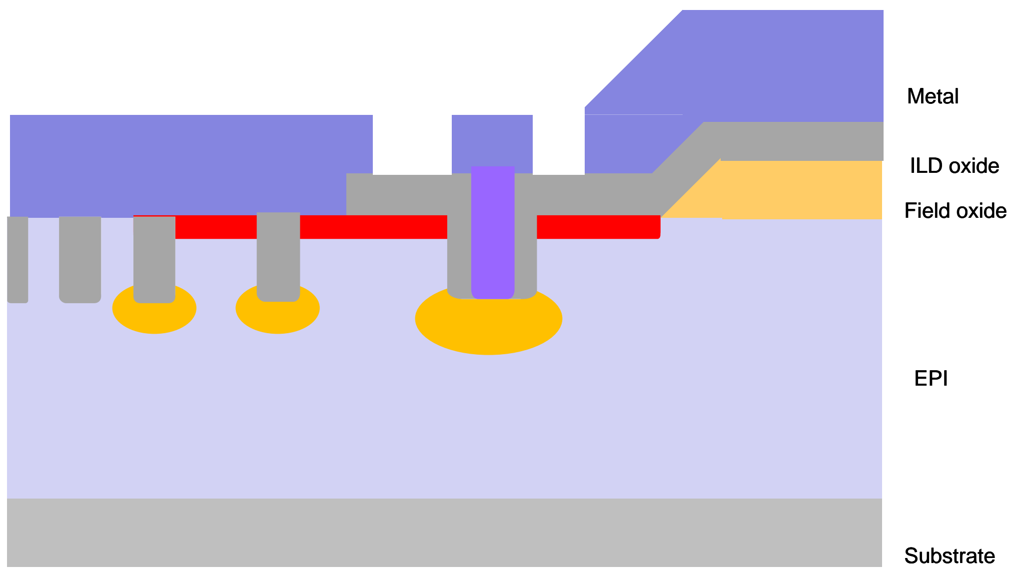


Figure 3.26 Metal cleaning.

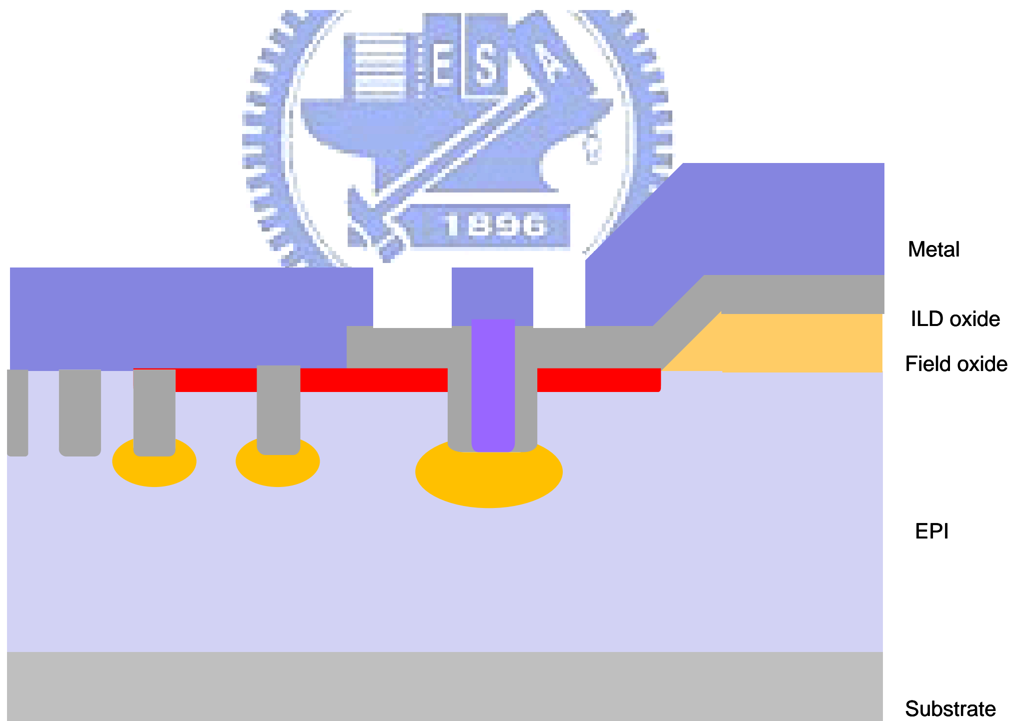


Figure 3.27 Alloy.

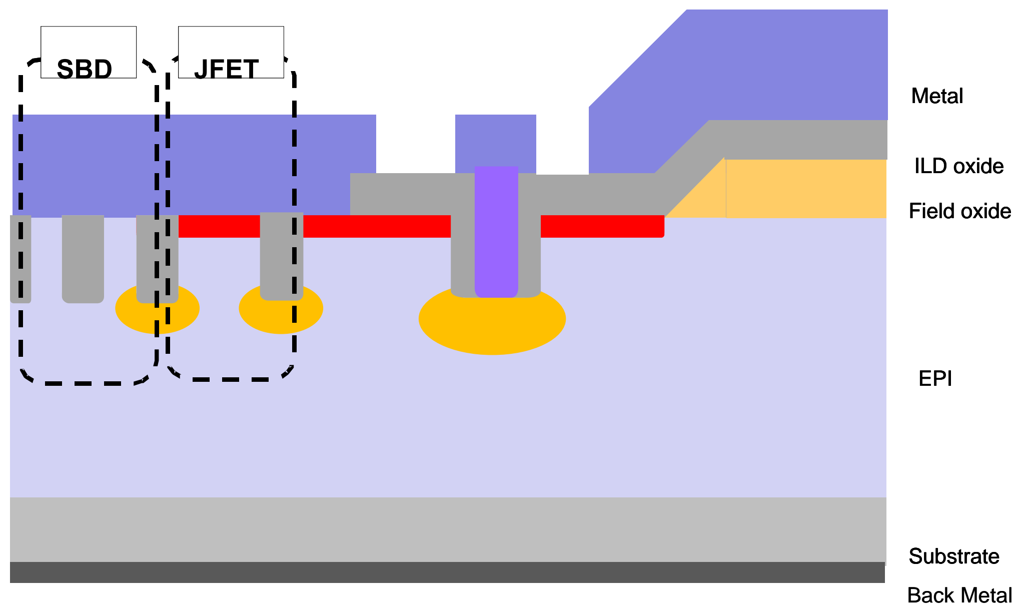


Figure 3.28 Backside grinding and backside metal deposition.

Chapter 4

Simulation of Power Trench JFET Integrated with SBD

4.1 Introduction

In this research, the device structure is constructed by Technology Computer Aided-Design (TCAD) tools, which based on Finite Element Analysis (FEA) model. There are two kinds of software adopted for different requirements to simulate the entire structures and their electric characteristics:

■ 2D simulation tool:

— Taurus Tsuprem4^{TM}: It's a powerful 1D & 2D simulator for semiconductor process simulation [25].

— Medici^{TM}: It simulates the 1D & 2D electrical behavior of semiconductor devices by solving the basic electrical equations [26].

■ 3D simulation tool:

— Sentaurus process^{TM}: It's an advanced 1D, 2D, and 3D process simulator, which providing an easy Monte Carol calculation to simulate the desired devices from nano-scale CMOS to large-scale high-voltage power devices [27].

－Sentaurus device^{TM}: It's an advanced 1D, 2D, and 3D device simulator. This simulator is able to simulate electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices [28].

4.2 Two-Dimension Simulation

4.2.1 Two-Dimension Process Simulation

This two-dimension process simulation is realized by Tsuprem4^{TM} software and its detailed process step with recipe that are showing in below:

(1) To prepare N-type substrate material with heavy arsenic dopant, that has 4m Ω resistivity and (100) orientation of primary flat location.

(2) To deposit epitaxial layer with 10mins of 1150℃ temperature, 0.25Ω resistivity and thickness of 5.5μm. The purpose of this epitaxial layer is to sustain about 25V breakdown voltage.

(3) To grow field oxide by thermal diffusion with conditions of 850℃ temperature, 720 minutes and wet oxide. The thickness of thermal oxide is about 0.8μm.

(4) Using 1st mask to define active area, then oxide wet etch by BOE solvent and strip out the photo-resistor. After this stage, it would define the active area and peripheral termination area.

(5) To deposit 0.6 μm TEOS-CVD oxide as hard mask oxide for trench etching.

(6) Using 2nd mask to define trench pattern.

(7) Using anisotropic oxide dry etcher to etch hard mask oxide.

(8) Strip out photo-resistor of trench.

(9) To etch 0.6 μm depth of trench by using anisotropic silicon etcher, as showing in Figure 4.1.

(10) Using 3rd mask to define source pattern.

(11) To implant heavy BF2 ions by using self-aligned structure with hard mask oxide and source pattern, 6.0×10^{15} dose amount, 50 KeV energy and 0° title angle. The implanted area at the bottom of trench forms P^{+} gate electrode as showing in Figure 4.2.

(12) Strip out photo-resistor of source.

(13) Removing trench hard mask oxide by HF solvent as showing in Figure 4.3.

(14) To deposit 0.6 μm LPCVD TEOS oxide as ILD layer. The oxide would fill into the trench structure as showing in Figure 4.4.

(15) Using 4th mask to define contact pattern.

(16) Etching 0.65 μm ILD layer by anisotropic oxide etch, as showing in Figure 4.5.

(17) Strip out photo-resistor of contact.

(18) Using same 3rd mask to re-define source pattern.

(19) To implant arsenic ions to form source junction with 6.0×10^{15} dose amount, 20 KeV energy and 0° title angle as showing in Figure 4.6.

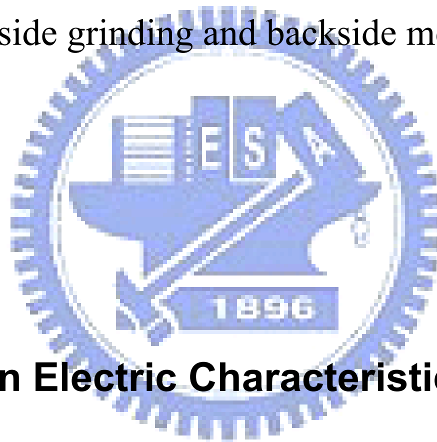
(20) Strip out photo-resistor of source.

(21) Using rapid high anneal temperature to activate the implanted dopants with temperature 850℃, 10 seconds, N_2 gas as showing in Figure 4.7.

(22) To sputter front-side metal with 3.0 μm as source electrode.

(23) Final alloy with 410℃, 30 minutes, N_2 gas as showing in Figure 4.8.

(24) To do wafer backside grinding and backside metal evaporation as backside drain electrode.



4.2.2 Two-Dimension Electric Characteristic Simulation

The two-dimension simulation of electric characteristics is realized by Medeci™ software, and its detailed simulated items are showing below.

4.2.2.1 Two-Dimension Area Factor (α)

The desired active area size of this study is assumed 8.1 ㎜ ^{2}. In this two dimension simulation, the width of each unit cell is 1 μm and the length of each unit cell is 3.35 μm as showing in Figure 4.9. The two-dimension area factor is

$$\alpha = \frac{Chip \quad size}{Unit \quad cell \quad size} = \frac{8.1mm^2}{3.35\mu m^2} = 2.418 \times 10^6 \qquad (4.1)$$

4.2.2.2 Breakdown Voltage of Drain to Source (BV_{DSX})

To take source as ground and gate with condition of -4.0V bias, sweep the drain voltage from 0V, and keep adding voltage of drain current until it is rising to 0.5mA in measurement. This voltage is defined as breakdown voltage of drain to source (BV_{DSX}).

In the two-dimension simulation, if the drain current of each unit cell with 1 μ m width is considered, the equation will be

$$I_D = \frac{0.5mA}{Area \quad factor(\alpha)} = \frac{0.5mA}{2.418 \times 10^6} = 2.068 \times 10^{-10} (A/um) \qquad (4.2)$$

To snap the drain voltage shut when drain current is $2.068 \times 10^{-10} (A/um)$, the breakdown voltage of drain to source (BV_{DSX}) is about 27.5V as showing in Figure 4.10. The electric potential profile is showing in Figure 4.11. Figure 4.12 shows that the highest electric field magnitude occurs in the bottom of P^+ gate electrode.

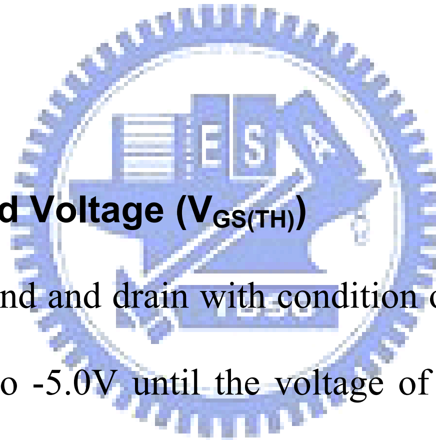
4.2.2.3 Breakdown Voltage of Gate to Source (BV_{GSO})

To take source and gate as ground initially, sweep the gate voltage from 0V, and keep adding voltage of drain current until it is -1mA in measurement. This voltage is defined as breakdown voltage of gate to source (BV_{GSO}).

In the two-dimension simulation, with consideration of drain current of each unit cell with 1 μm width, the equation will be

$$I_D = \frac{-1mA}{Area \quad factor(\alpha)} = \frac{-1mA}{2.418 \times 10^6} = -4.136 \times 10^{-10} (A/um) \qquad (4.3)$$

To snap the drain voltage shut when gate current is $-4.136 \times 10^{-10}(A/um)$, the breakdown voltage of gate to source (BV_{GSX}) is about -11.0V as showing in Figure 4.13. The factor is determined by distance that between N^+ source and P^+ gate. e.g trench depth.



4.2.2.4 Gate Threshold Voltage ($V_{GS(TH)}$)

To take source as ground and drain with condition of 0.1V bias initially, sweep the gate voltage from 0V to -5.0V until the voltage of drain current is 250 μA in measurement. This voltage is defined as gate threshold voltage ($V_{GS(TH)}$).

In the two-dimension simulation, consider the drain current of each unit cell with 1 μm width, the equation will be

$$I_D = \frac{250\mu A}{Area \quad factor(\alpha)} = \frac{250\mu A}{2.418 \times 10^6} = 1.034 \times 10^{-10} (A/um) \qquad (4.4)$$

To snap the gate voltage shut when drain current is $1.034 \times 10^{-10}(A/um)$, the

breakdown voltage of gate to source ($V_{GS(TH)}$) is about -1.5V as showing in Figure 4.14. The magnitude of $V_{GS(TH)}$ is determined by the epitaxial concentration, P^+ gate energy, its concentration and width of trench mesa.

4.2.2.5 Specific On-Resistance ($R_{on,sp}$) and Drain to Source On Resistance ($R_{ds,on}$)

To take source as ground and gate with condition of 0.6V bias initially, sweep the drain voltage from 0V to 5.0V until the voltage of drain current is 10A in measurement. The reciprocal of slope is defined as drain to source on-resistance ($R_{ds,on}$). If the drain to source on resistance multiplied with active area size, it would be specific on-resistance ($R_{on,sp}$).

In the two-dimension simulation, with consideration of the drain current of each unit cell with 1 μm width, the equation will be

$$I_D = \frac{10A}{Area \quad factor(\alpha)} = \frac{10A}{2.418 \times 10^6} = 4.135 \times 10^{-6}(A/um) \tag{4.5}$$

To snap the slope value shut when drain current is $4.135 \times 10^{-6}(A/um)$, the slope as showing in Figure 4.15 is

$$Slope = 1.976 \times 10^{-4}\left(\frac{A/\mu m}{V}\right) \tag{4.6}$$

$$1/Slope = 5.061 \times 10^{3} (\Omega * \mu m) \tag{4.7}$$

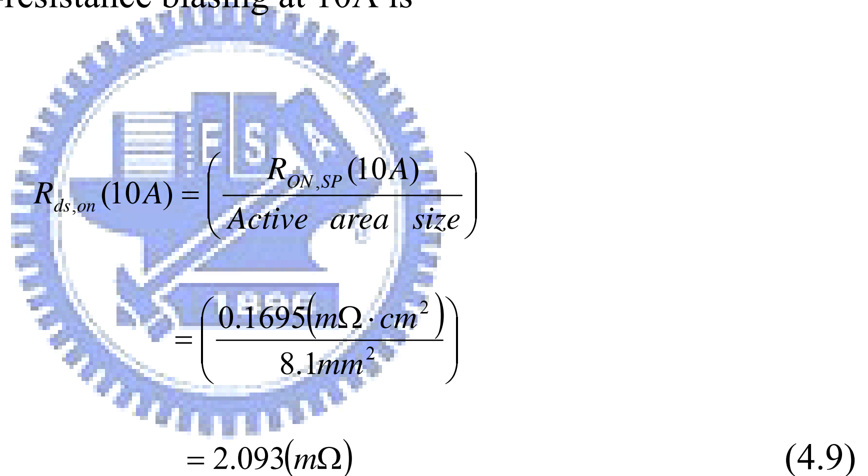
The specific on-resistance biasing at 10A is

$$R_{on,sp}(10A) = (1/Slope) * L$$

$$= (5.061 \times 10^{3} \Omega \cdot cm) \times (3.35 \mu m)$$

$$= 0.1695 (m\Omega \cdot cm^{2}) \tag{4.8}$$

The drain to source on-resistance biasing at 10A is



$$R_{ds,on}(10A) = \left(\frac{R_{ON,SP}(10A)}{Active \quad area \quad size} \right)$$

$$= \left(\frac{0.1695 (m\Omega \cdot cm^{2})}{8.1 mm^{2}} \right)$$

$$= 2.093 (m\Omega) \tag{4.9}$$

The magnitude of $R_{ds,on}$ depends on the epitaxial concentration and channel width.

4.2.2.6 Reverse Leakage Current (I_R)

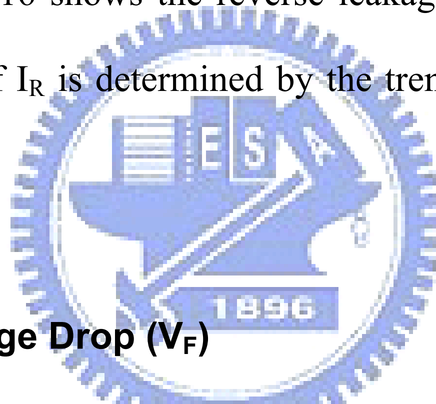
To take source as ground and gate with condition of -0.4V biasing initially, sweep the drain voltage from 0V to 30.0V. To snap the drain current magnitude shut

when V_D=20V in measurement, this current is defined as reverse leakage current (I_R).

In the two-dimension simulation, snap the drain current magnitude shut when drain voltage is 20V with 1 μm width each unit cell

$$I_R = \left[1.412\times10^{-13}(A/um)\right]\times\alpha = 3.412\times10^{-7}(A) \tag{4.10}$$

That's the reverse leakage current magnitude of this schemed structure when gate biasing is –0.4V. Figure 4.16 shows the reverse leakage current magnitude of one unit cell. The magnitude of I_R is determined by the trench mesa width of Schottky barrier diode.



4.2.2.7 Forward Voltage Drop (V_F)

To take source, gate and drain as ground initially, sweep the gate and source voltage from 0V to 1.0V simultaneously. To snap the source voltage shut when the drain current is 0.5mA in measurement. In this condition, the voltage is defined as forward voltage drop (V_F).

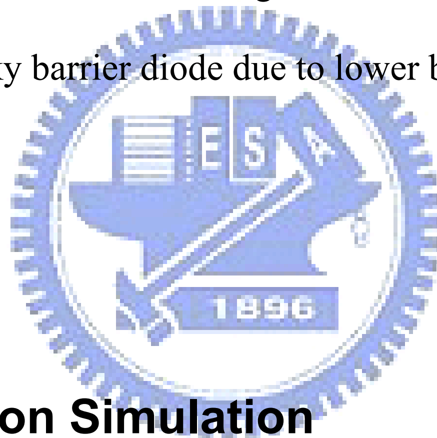
In the two-dimension simulation, with consideration of 10A source current of each unit cell with 1 μm width, the equation will be.

$$I_S = \frac{10A}{Area\quad factor(\alpha)} = \frac{10A}{2.418\times10^{6}} = 4.135\times10^{-6}(A/um) \tag{4.11}$$

To snap the source voltage shut when source current is $4.135\times10^{-6}(A/um)$, the forward voltage drop V_F(10A) is about 0.03V. Using same method to extract the 20A forward voltage drop, the V_F(20A) is 0.06V. Their forward I_D-V_D curve is showing in Figure 4.17 and Figure 4.18.

4.2.2.8 Turn-on I_D-V_D Curve

Figure 4.19 is showing the turn-on I_D-V_D curve at different gate biases. The drain current becomes significant small when the gate bias is smaller than -2.0V. Figure 4.20 shows the electronic current magnitude of turn-on maximum value that occurs at the part of Schottky barrier diode due to lower barrier high of its.



4.3 Three-Dimension Simulation

4.3.1 Three-Dimension Process Simulation

The three-dimension process simulation is realized by Senturaus^{TM} process software and its key process steps are showing below:

- Figure 4.21 shows trench pattern.
- Figure 4.22 shows trench hard mask oxidation etching.
- Figure 4.23 shows trench etching.
- Figure 4.24 shows source pattern & P+ gate implant.
- Figure 4.25 shows ILD CVD oxide.

- Figure 4.26 shows contact etching.
- Figure 4.27 shows source pattern & source implant.
- Figure 4.28 shows front-side metal sputter.

4.3.2 Three-Dimension Electric Characteristic Simulation

The three-dimension simulation of electric characteristics is realized by Sentaurus™ device software, and its detailed simulated items are showing below.

4.3.2.1 Three-Dimension Area Factor (β)

The desired active area size of this study is assumed 8.1 mm^2. In this three dimension simulation, the width of each unit cell is 1 μm and the length of each unit cell is 1.675 μm as showing in Figure 4.29. The three-dimension area factor is

$$\beta = \frac{Chip \quad size}{Unit \quad cell \quad size} = \frac{8.1mm^2}{1.675\mu m^2} = 4.836 \times 10^6 \qquad (4.12)$$

4.3.2.2 Breakdown Voltage of Drain to Source (BV_{DSX})

In the three-dimension simulation, if we consider the drain current of each unit cell, the drain to source current can be calculate

$$I_D = \frac{0.5mA}{Area \quad factor(\beta)} = \frac{0.5mA}{4.836\times10^{6}} = 1.034\times10^{-10}(A) \quad (4.13)$$

To snap the drain voltage shut when drain current is $1.034\times10^{-10}A$, the breakdown voltage of drain to source (BV_{DSX}) is about 55V as showing in Figure 4.30. The electric potential profile and electric field magnitude profile are showing in Figure 4.31 and Figure 4.32 respectively.

4.3.2.3 Gate Threshold Voltage ($V_{GS(TH)}$)

Consider the drain current of each unit cell, it would be

$$I_D = \frac{250\mu A}{Area \quad factor(\beta)} = \frac{250\mu A}{4.836\times10^{6}} = 5.169\times10^{-11}(A) \quad (4.14)$$

Snap the gate voltage shut when drain current is $5.169\times10^{-11}A$, the $V_{GS(TH)}$ is about -0.324V as showing in Figure 4.33.

4.3.2.4 Specific On-Resistance ($R_{on,sp}$) and Drain to Source On Resistance ($R_{ds,on}$)

Consider the drain current of each unit cell, its value becomes

$$I_D = \frac{10A}{Area \quad factor(\beta)} = \frac{10A}{4.836\times10^{6}} = 2.068\times10^{-6}(A) \quad (4.15)$$

To snap the slope value shut when drain current is $2.068\times10^{-6}(A)$, the slope is showing in Figure 4.34, and its equations are

$$Slope = 7.7\times10^{-5}\left(\frac{A}{V}\right) \tag{4.16}$$

$$1/Slope = 12.987\times10^{3}(\Omega) \tag{4.17}$$

The specific on-resistance biasing at 10A is

$$\begin{aligned} R_{on,sp}(10A) &= (1/Slope)*(L\times W) \\ &= (12.987\times10^{3}\Omega)\times(3.35\mu m^{2}) \\ &= 2.175\times10^{-4}(m\Omega\cdot cm^{2}) \end{aligned} \tag{4.18}$$

The drain to source on-resistance biasing at 10A is

$$\begin{aligned} R_{ds,on}(10A) &= \left(\frac{R_{on,sp}(10A)}{Active\ \ area\ \ size}\right) \\ &= \left(\frac{2.175\times10^{-4}(m\Omega\cdot cm^{2})}{8.1mm^{2}}\right) \\ &= 2.691(m\Omega) \end{aligned} \tag{4.19}$$

4.3.2.5 Reverse Leakage Current (I_R)

Snap the drain current magnitude shut when drain voltage equals to 20V, the I_R of one chip gives

$$I_R = \left[5.0\times10^{-16}(A)\right]\times\beta = 2.418\times10^{-9}(A) \tag{4.20}$$

Figure 4.30 shows the reverse leakage current in one unit cell.

4.3.2.6 Forward Voltage Drop (V_F)

Consider 10A source current in measurement, the source current magnitude of unit cell can be

$$I_S = \frac{10A}{Area\quad factor(\beta)} = \frac{10A}{4.836\times10^{6}} = 2.068\times10^{-6}(A) \tag{4.21}$$

Consider the source current is $2.068\times10^{-6}(A)$, while snap the source voltage shut, the forward voltage drop V_F (10A) can be about 0.174V. Using same method to extract the 20A forward voltage drop, the V_F (20A) becomes 0.236V. Forward I_D-V_D curves are shown by Figure 4.35 and Figure 4.36.

4.4 Study of Key Process Parameters

4.4.1 Definition of Key Process Parameters

This section focuses on some key parameters, which are related to electrical characteristics of this JFET integrated with SBD structure; the key parameters are showing below:

- JFET pitch size (Figure 4.37)
- P^+ gate implant energy.
- Schottky mesa width (Figure 4.37)
- Epitaxial resistivity.

4.4.2 JFET Pitch Size

The pitch size of JFET would affect the channel width directly, the larger pitch size the larger channel width and higher threshold voltage of gate to source ($V_{GS(TH)}$). Besides, the larger channel width would result in lower on-state resistance ($R_{ds,on}$). The relationships are showing in Figure 4.38 & Figure 4.39.

4.4.3 P^+ Gate Implant Energy

Figure 4.40 and Figure 4.41 show that there is no linear relationship between P^+ gate implant energy, threshold voltage of gate to source ($V_{GS(TH)}$), breakdown voltage of drain to source (BV_{DSX}) and specific on-resistance ($R_{on,sp}$). That is because the P^+ gate implant energy affects the high doping shape of P^+ gate region. The actual electrical characteristics are determined by their final net doping profile of P^+ gate region. Figure 4.42 shows the situation. .

4.4.4 Schottky Mesa Width

The Schottky mesa width affects the channel width of Schottky's part. The larger mesa width would result the higher threshold voltage of gate to source ($V_{GS(TH)}$) and lower breakdown voltage of drain to source (BV_{DSX}). Their relationship shows in Figure 4.43 & Figure 4.44.

Especially mention that another source of power loss is come from reverse recovery of diode. Reverse recovery results when the diode transited from forward biasing to reverse biasing. The Figure 4.45 shows the reverse recovery waveforms at different mesa width of Schottky diode, there is no significant correlation between mesa width and reverse recovery charge. The simulated Q_{rr} is about 0.147nC.

4.4.5 Resistivity of Epitaxial Layer

The electrical characteristics of different resistivity of epitaxial layer are showing in Figure 4.45 and Figure 4.46. The lighter doping concentration of epitaxial layer would obtain the smaller channel width, e.g. Lower threshold voltage of gate to source ($V_{GS(TH)}$). At this meanwhile, BV_{DSX} is inverse proportional to epitaxial doping concentration; $R_{on,sp}$ is proportional to epitaxial resistivity.

4.5 Conclusion

Table 3 shows the summary of electrical characteristics of this proposed structure, which is compared with prior structure. This study uses embedded

Schottky barrier diode that is major different than others. Some excellent characteristics were found in this proposed structure, but some unreasonable characteristics may come from the non-proper physical model, syntax or mesh definition. Those theories need actual sample to verify each simulation result.

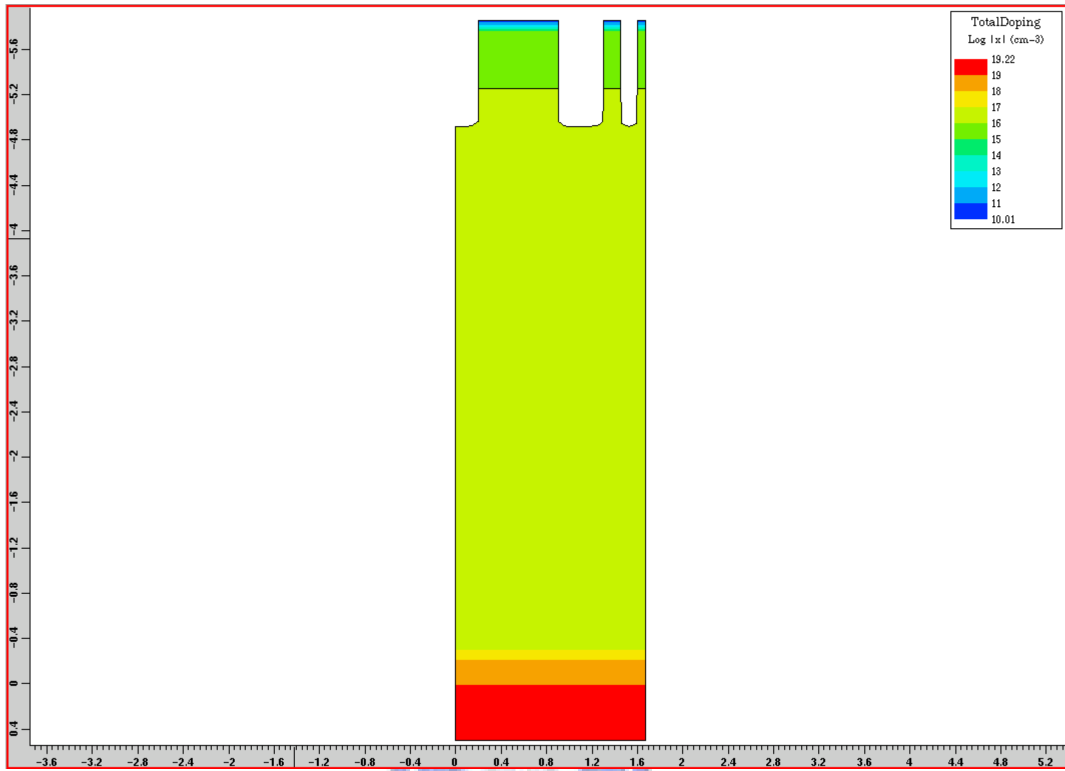


Figure 4.1 Trench etching with hard mask oxide.

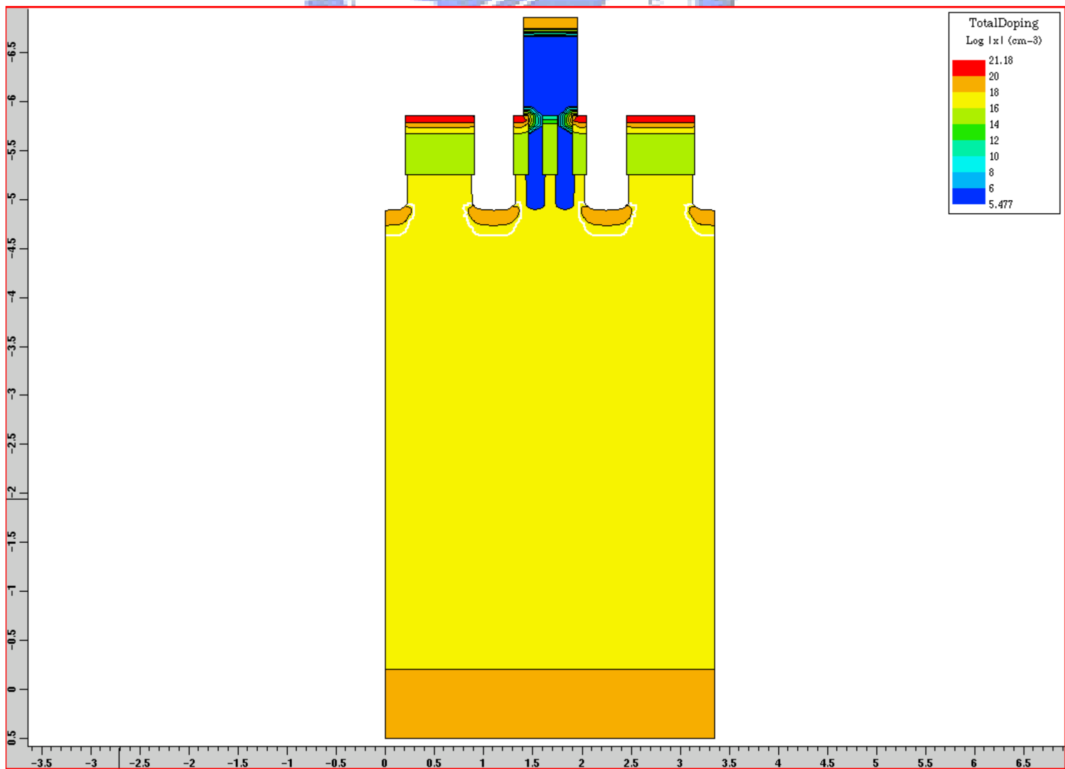


Figure 4.2 P^+ gate implant that with self-align hard mask oxide and source pattern.

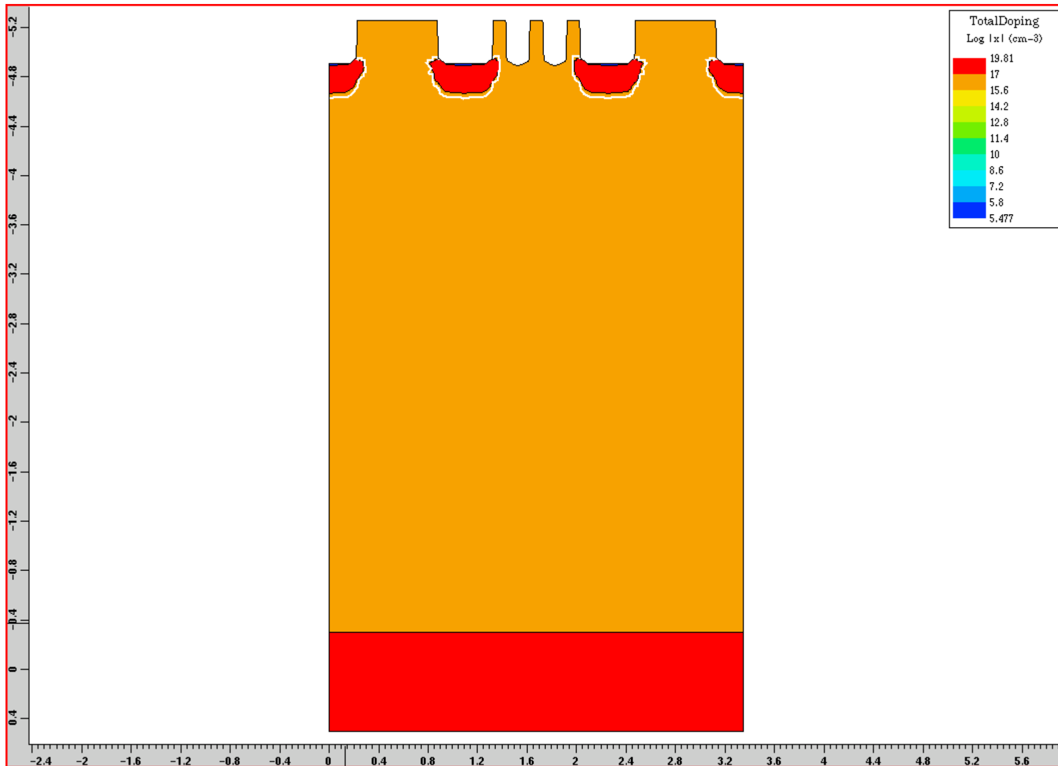


Figure 4.3 Remove hard mask oxide.

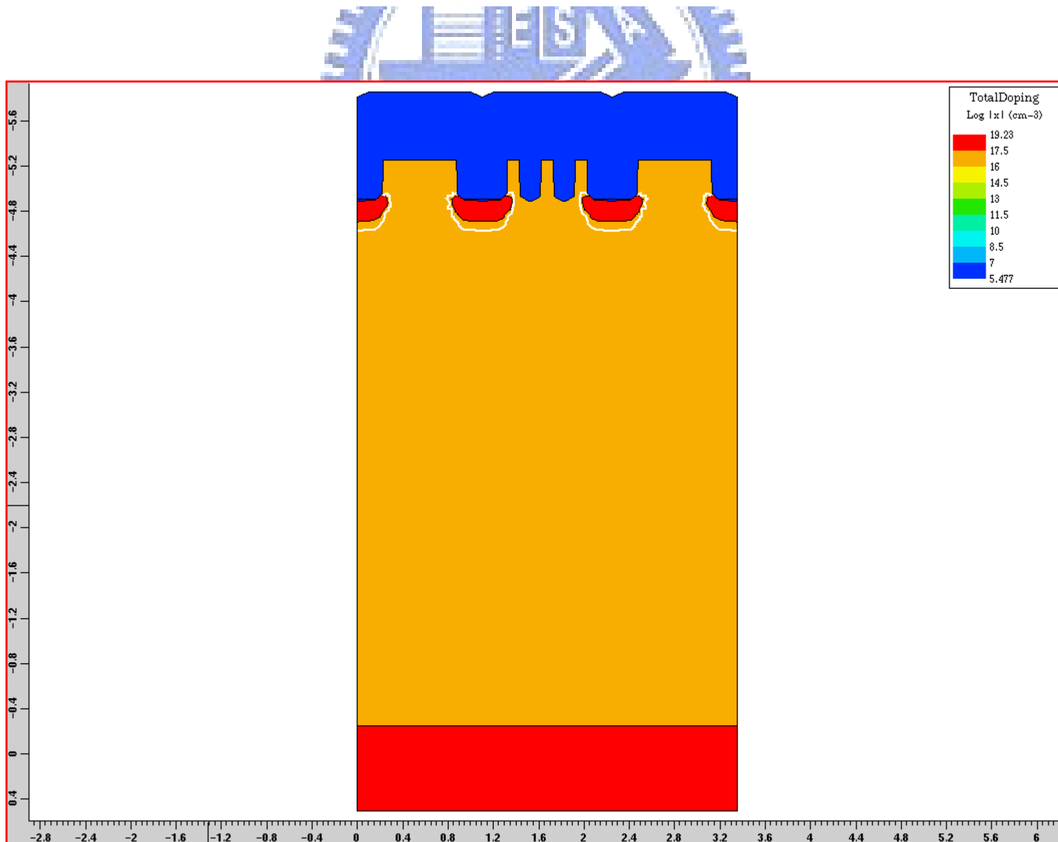


Figure 4.4 Deposit the LPCVD oxide as ILD.

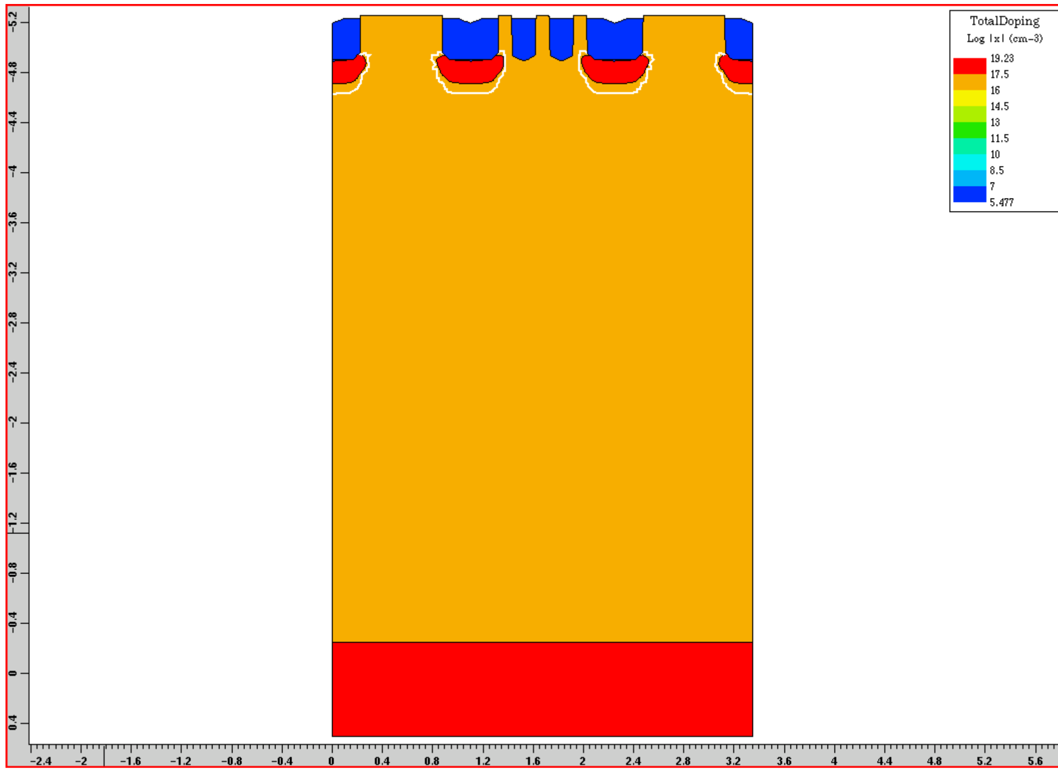


Figure 4.5 Contact dry etching.

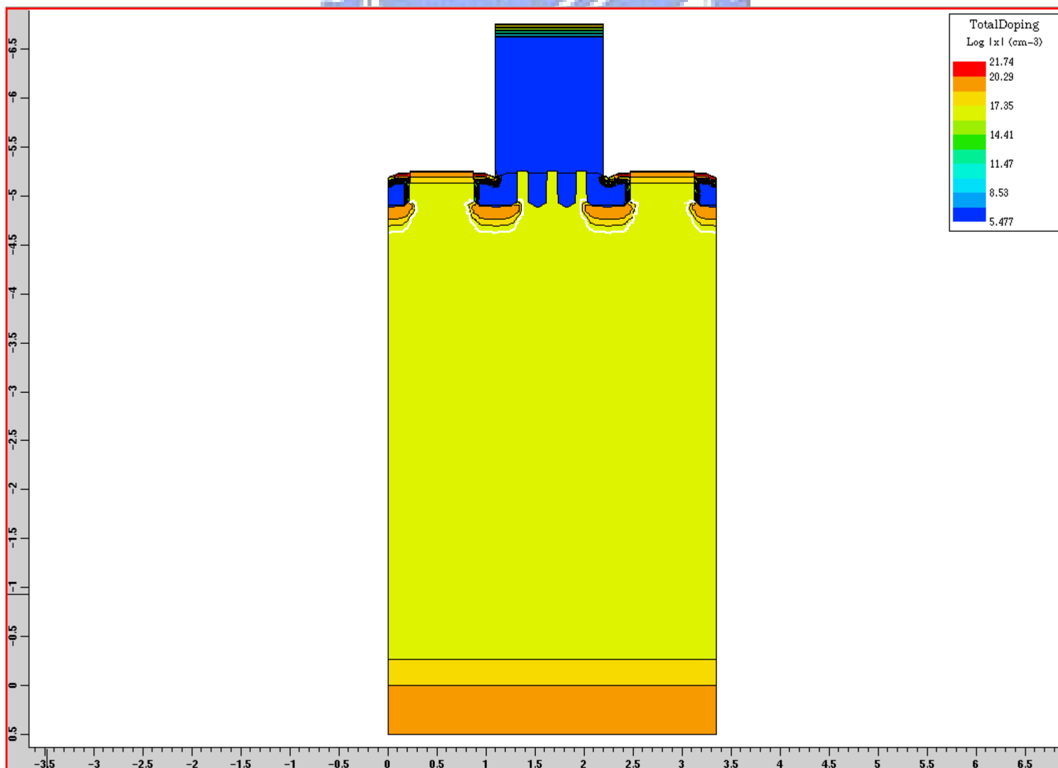


Figure 4.6 Define 2nd source pattern and source implant.

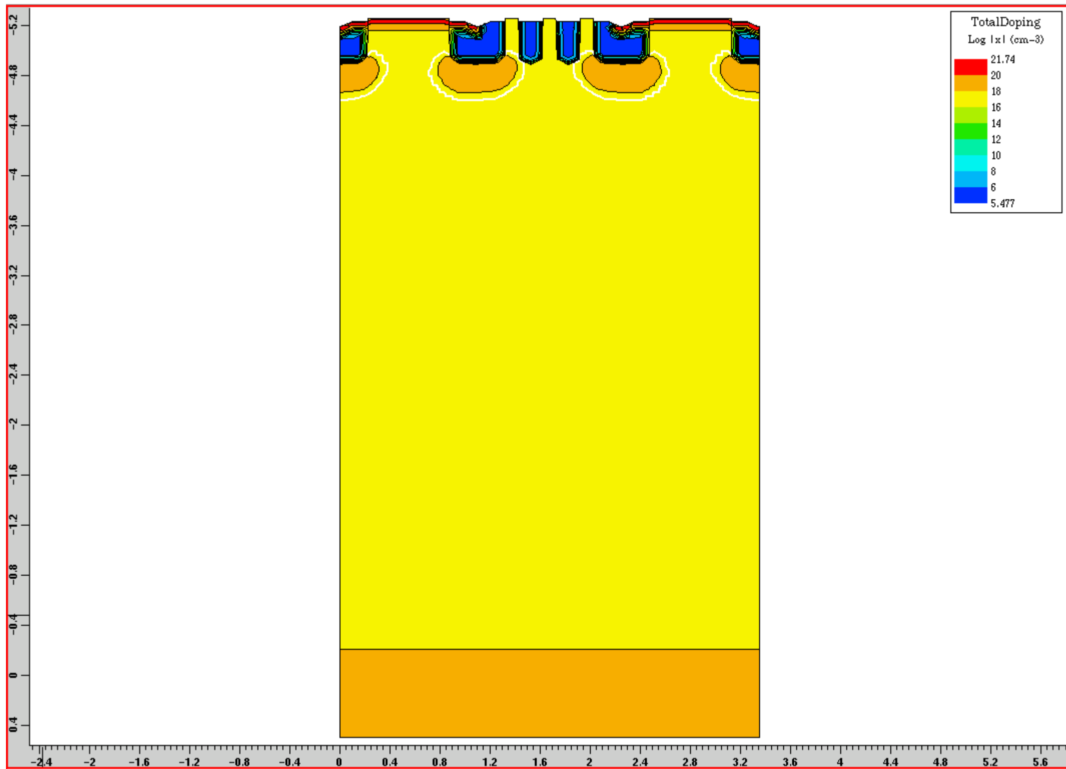


Figure 4.7 Strip source pattern.

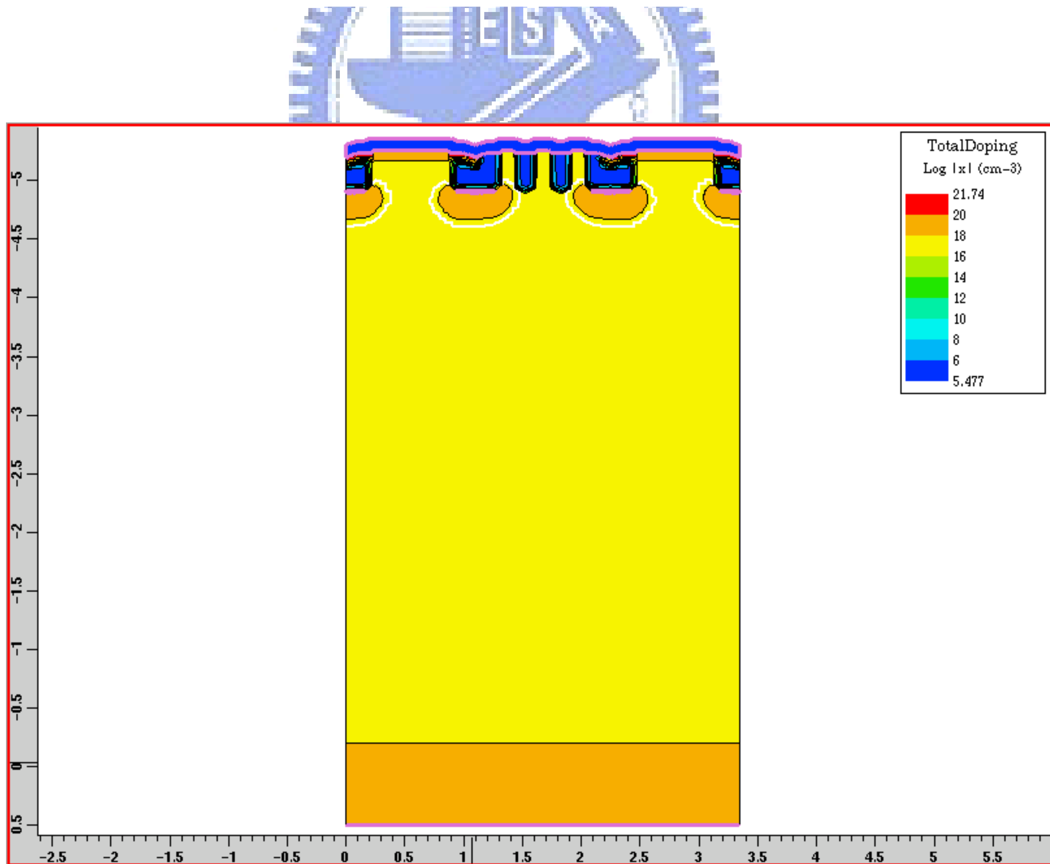


Figure 4.8 Sputter front-side metal as source electrode and alloy.

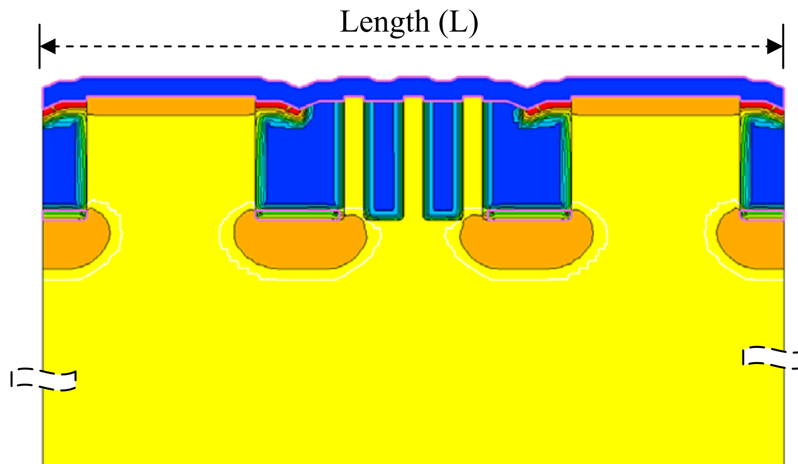


Figure 4.9 The schematic of two-dimension unit cell.

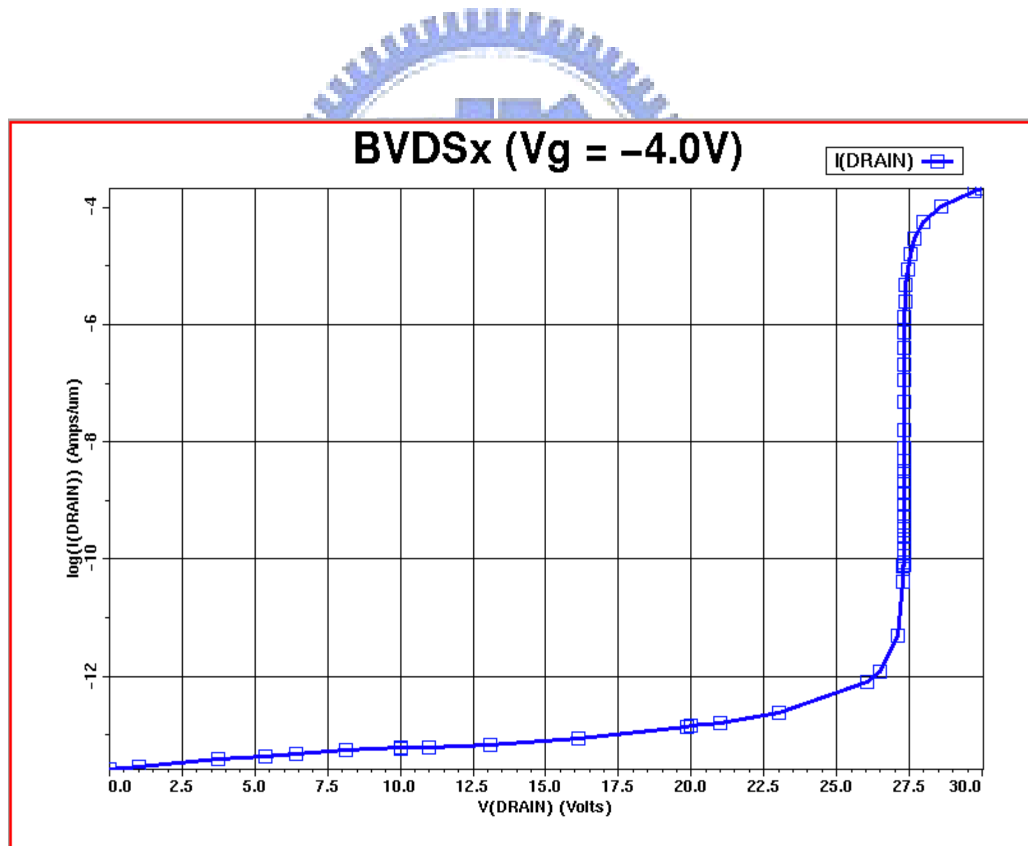


Figure 4.10 The breakdown voltage of drain to source.

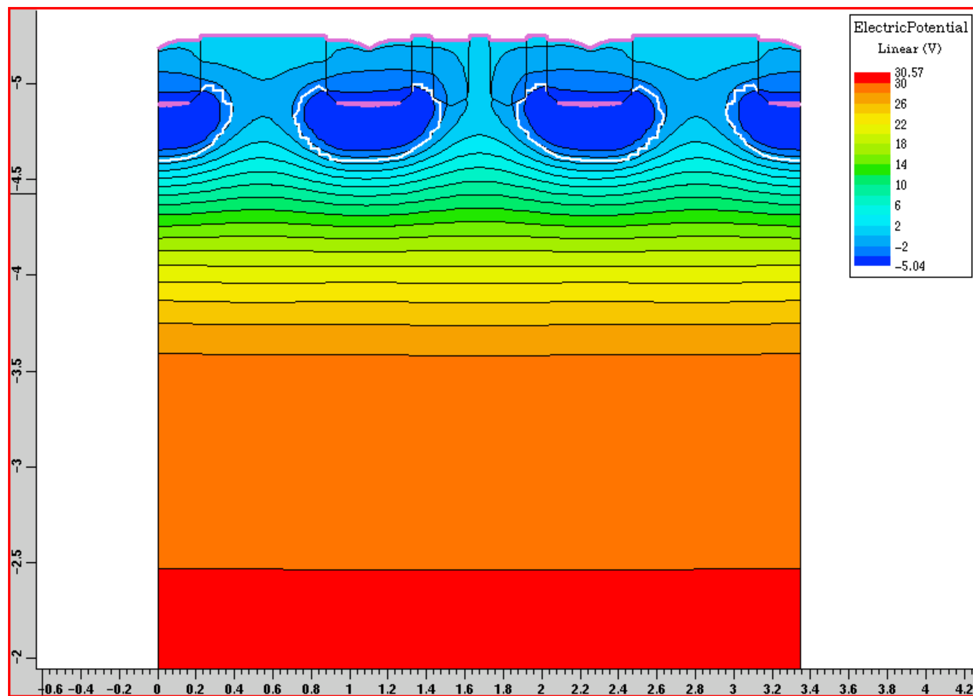


Figure 4.11 The electric potential profile of $BV_{DSX}(V_G=-4.0V)$.

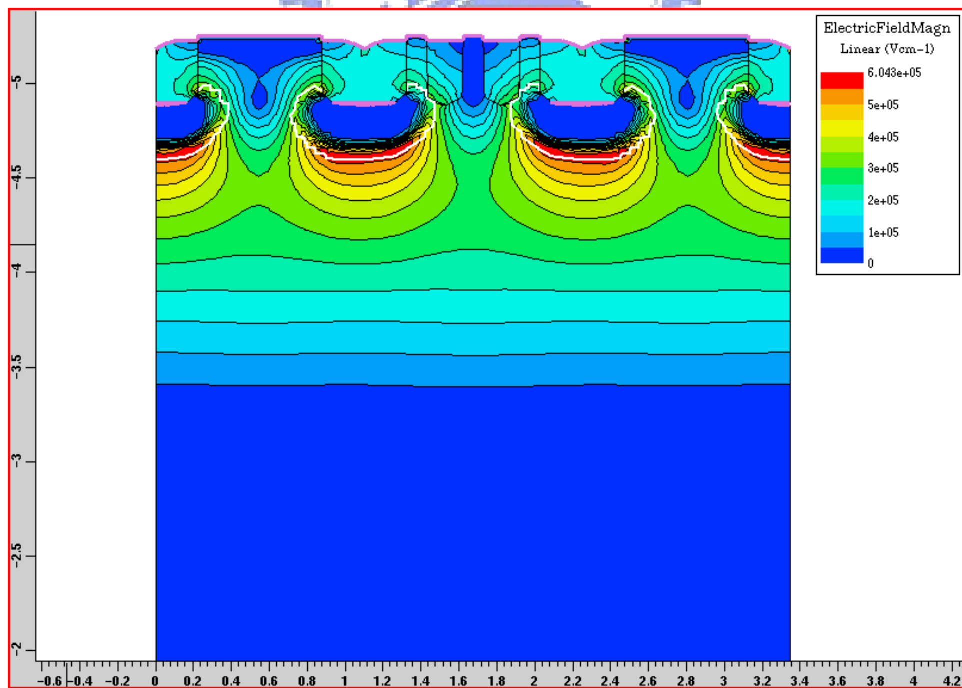


Figure 4.12 The electric field magnitude at $BV_{DSX}(V_G=-4.0V)$.

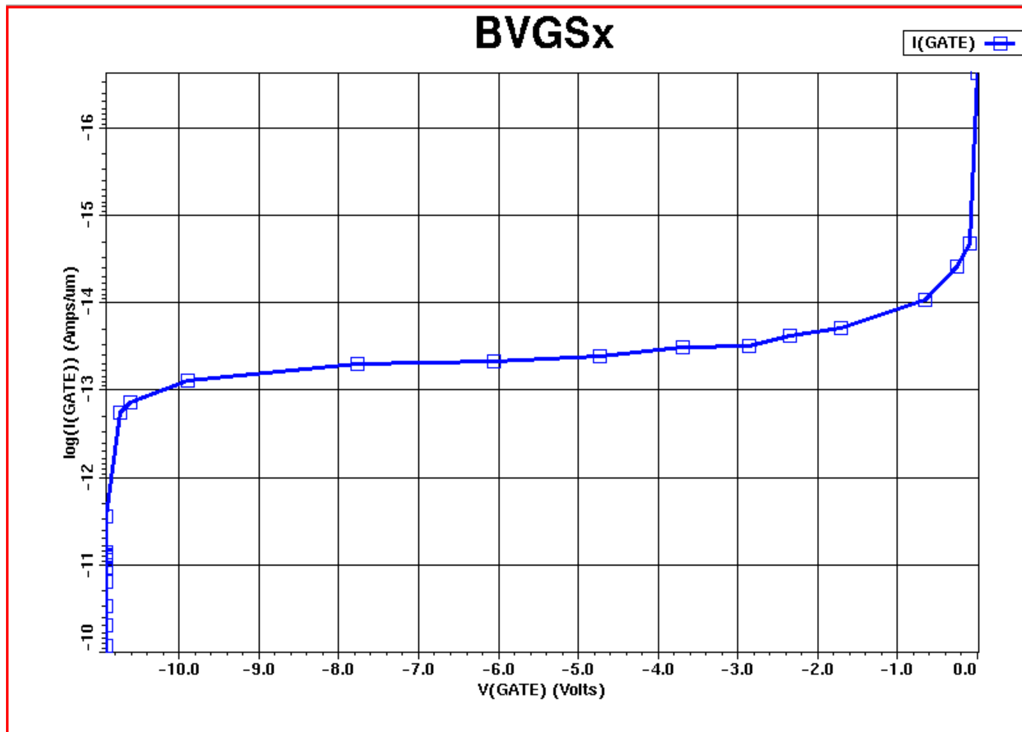


Figure 4.13 The breakdown voltage of gate to source.

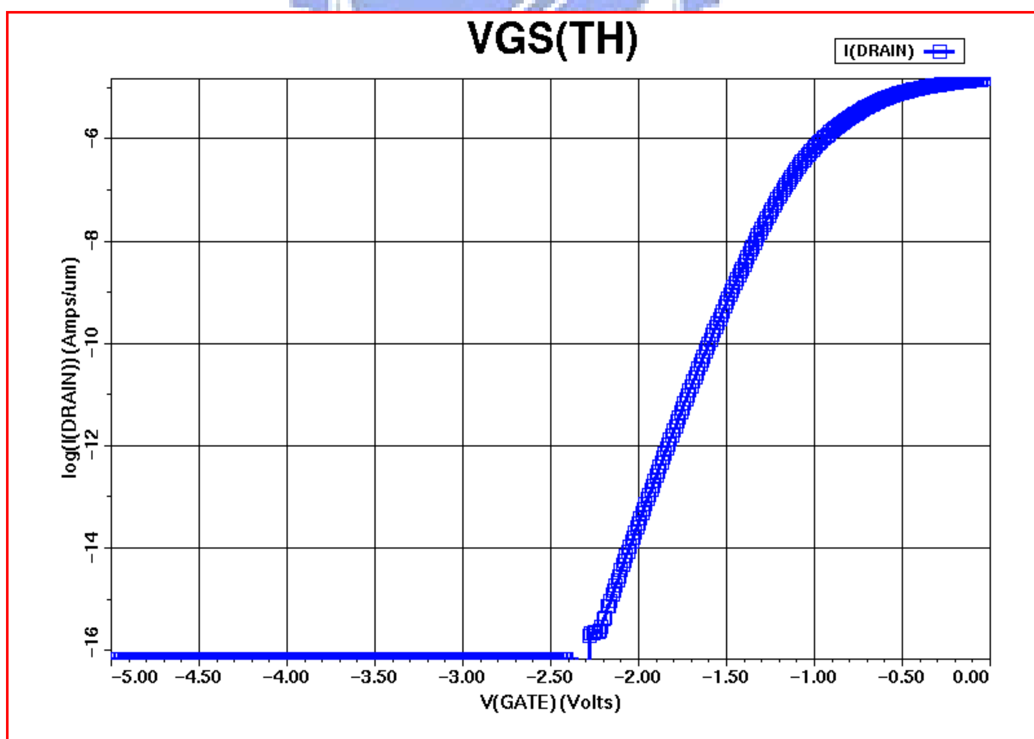


Figure 4.14 The gate threshold voltage.

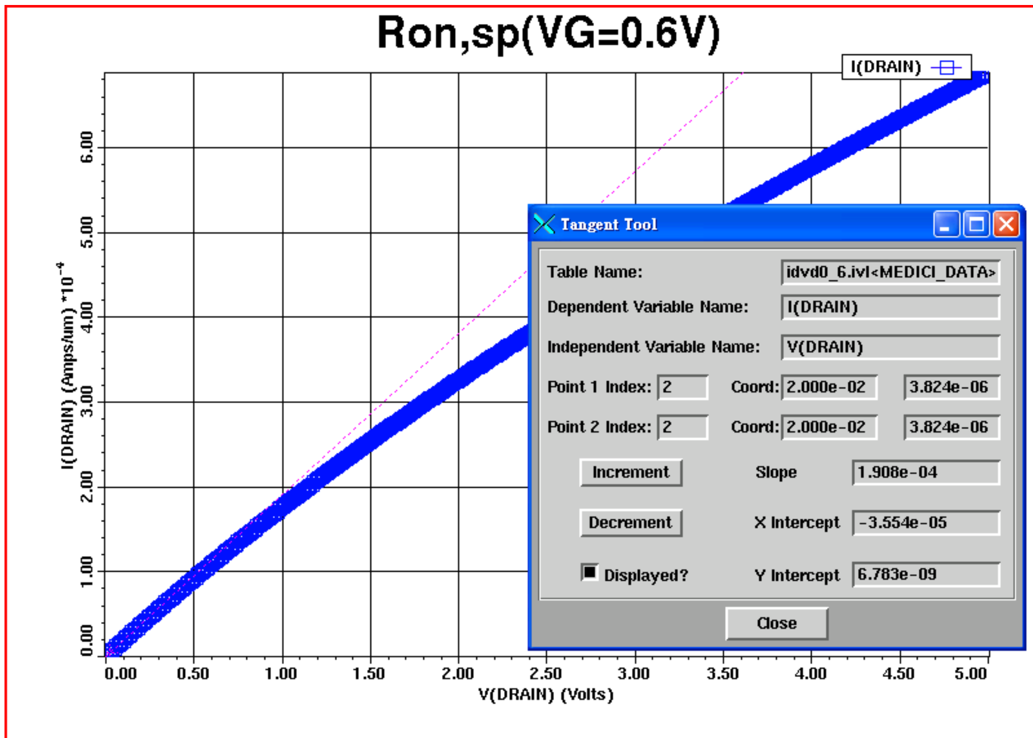


Figure 4.15 The turn-on I_D-V_D curve for $R_{on,sp}$.

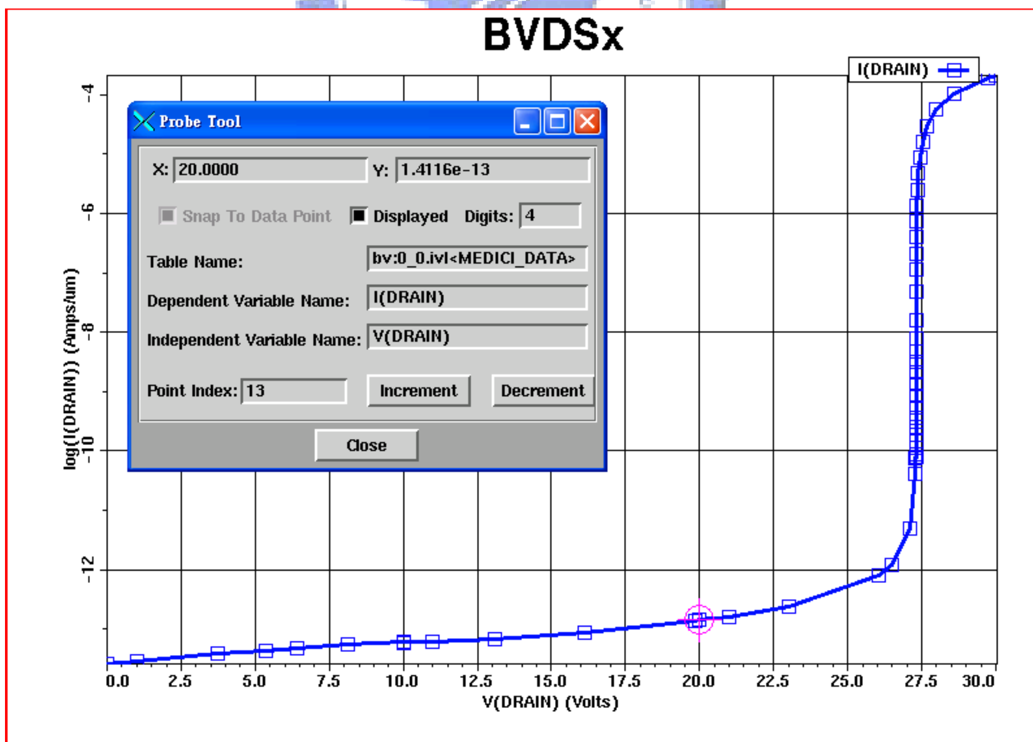


Figure 4.16 The reverse leakage current magnitude when V_G=-0.4V and V_D=20V.

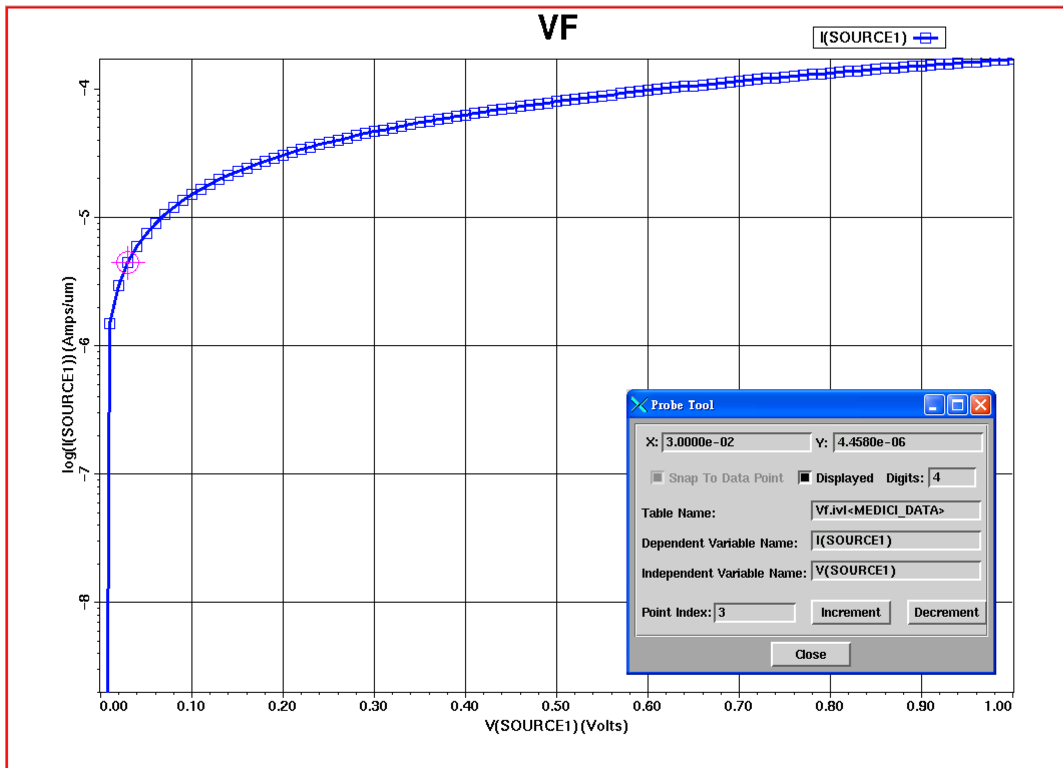


Figure 4.17 The forward voltage drop when I_S=10A.

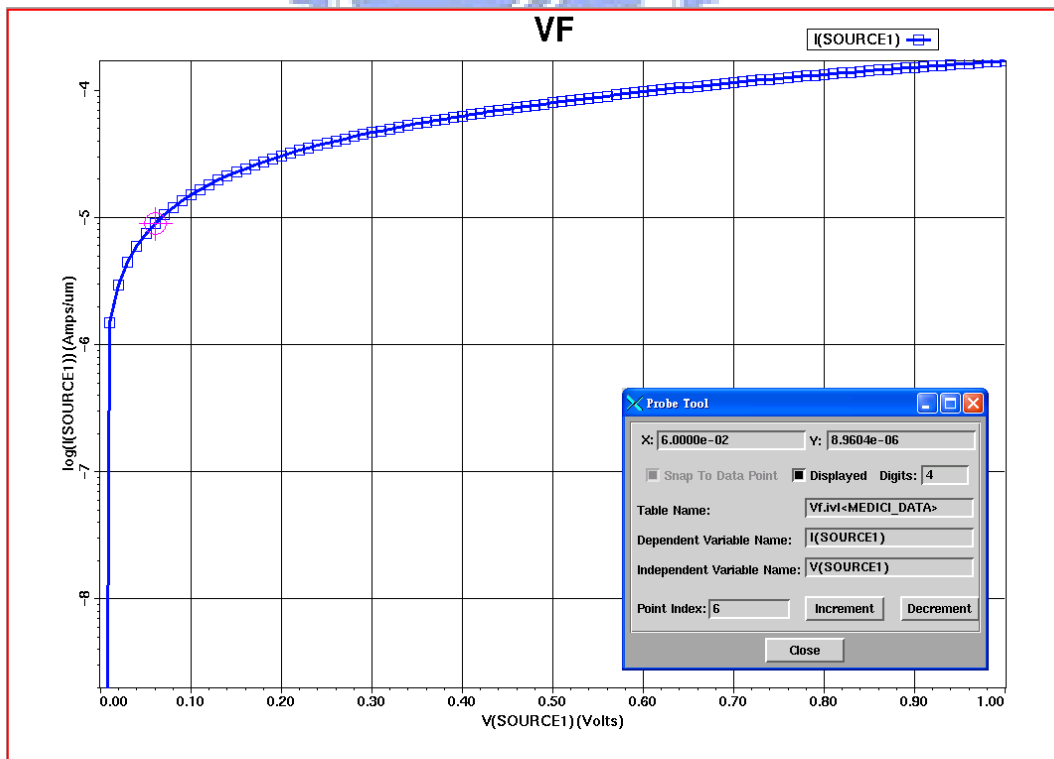


Figure 4.18 The forward voltage drop when I_S=20A.

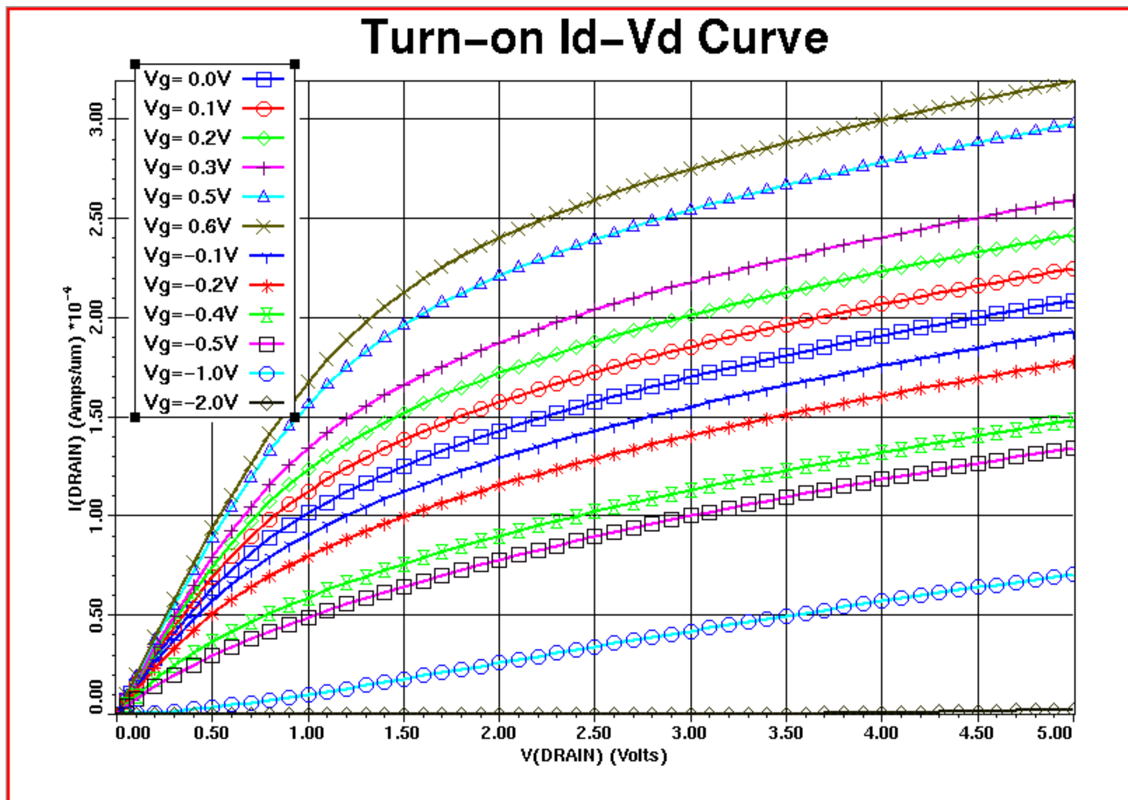


Figure 4.19 The turn-on I_D-V_D curve.

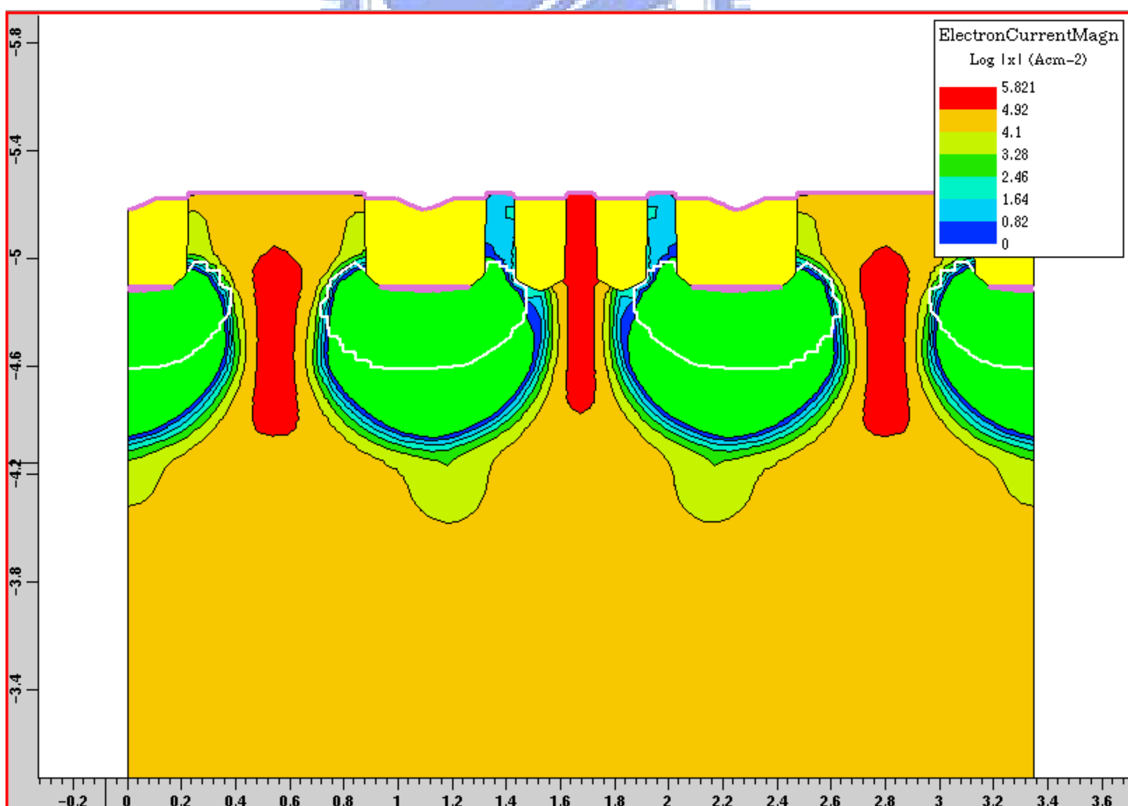


Figure 4.20 The turn-on electron current magnitude.

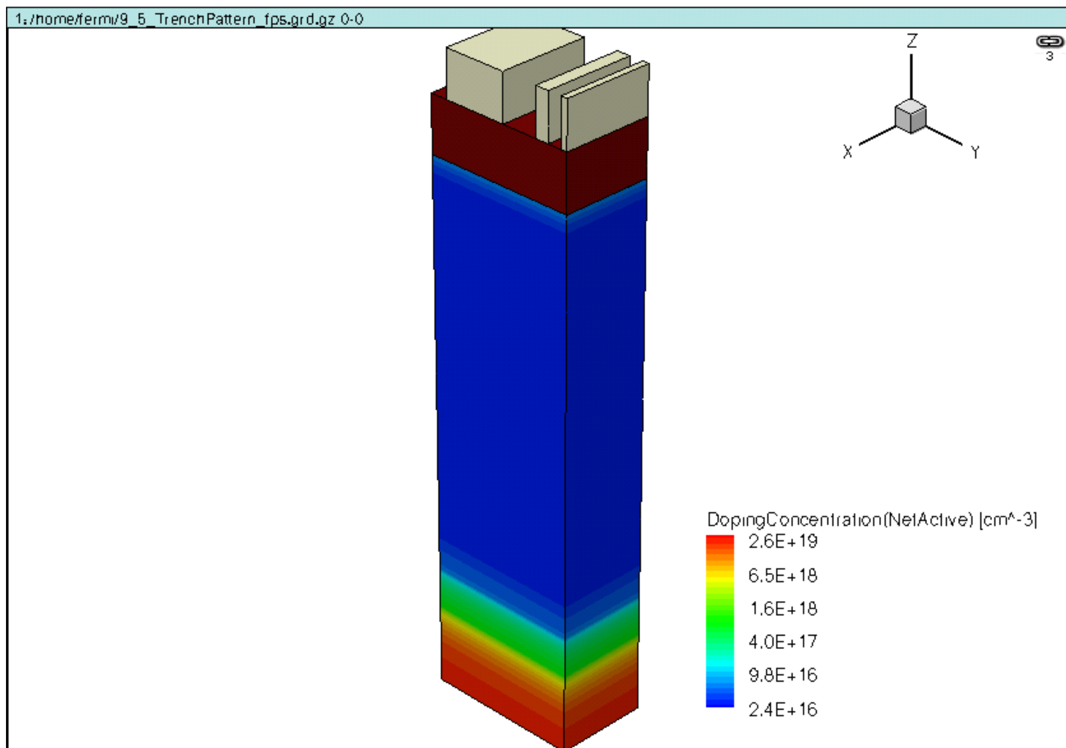


Figure 4.21 Trench pattern.

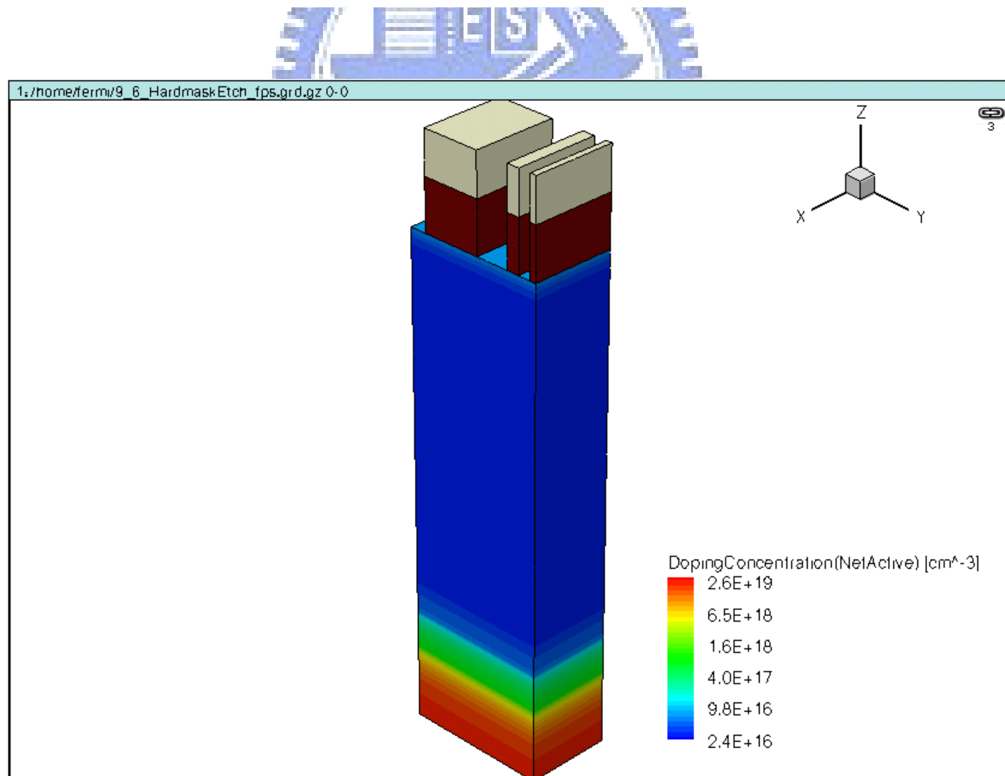


Figure 4.22 Trench hard mask oxide etching.

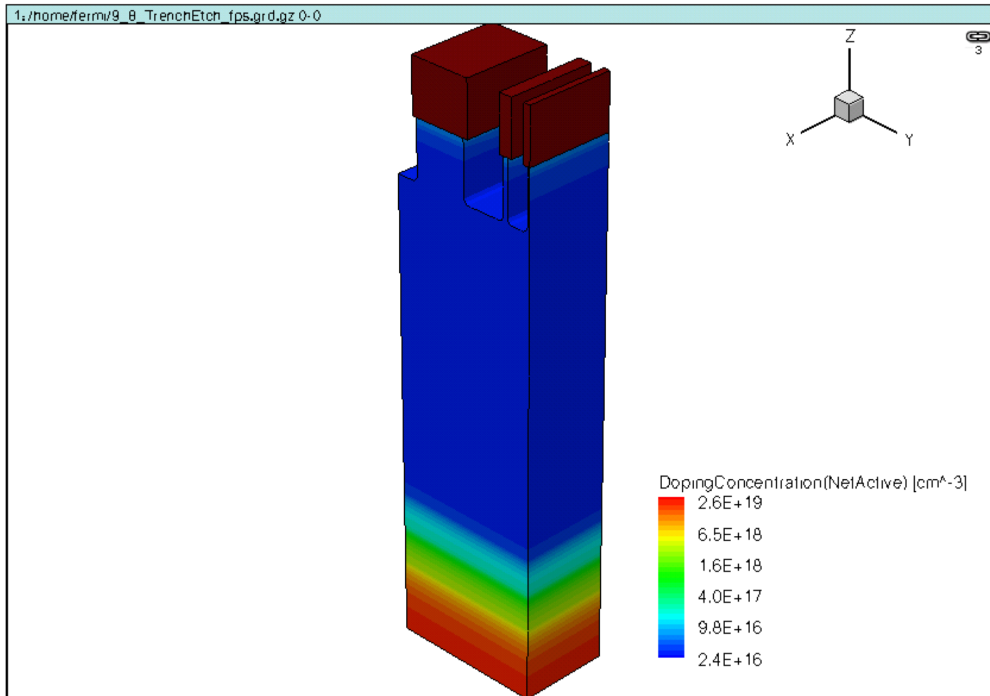


Figure 4.23 Trench etching.

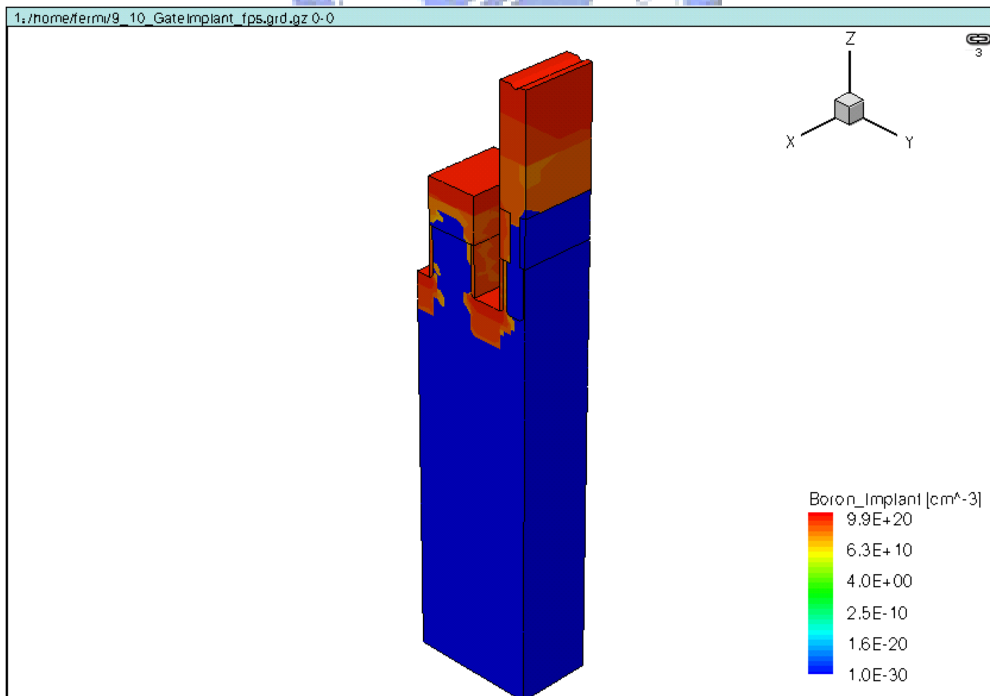


Figure 4.24 Source pattern & P^+ gate implant.

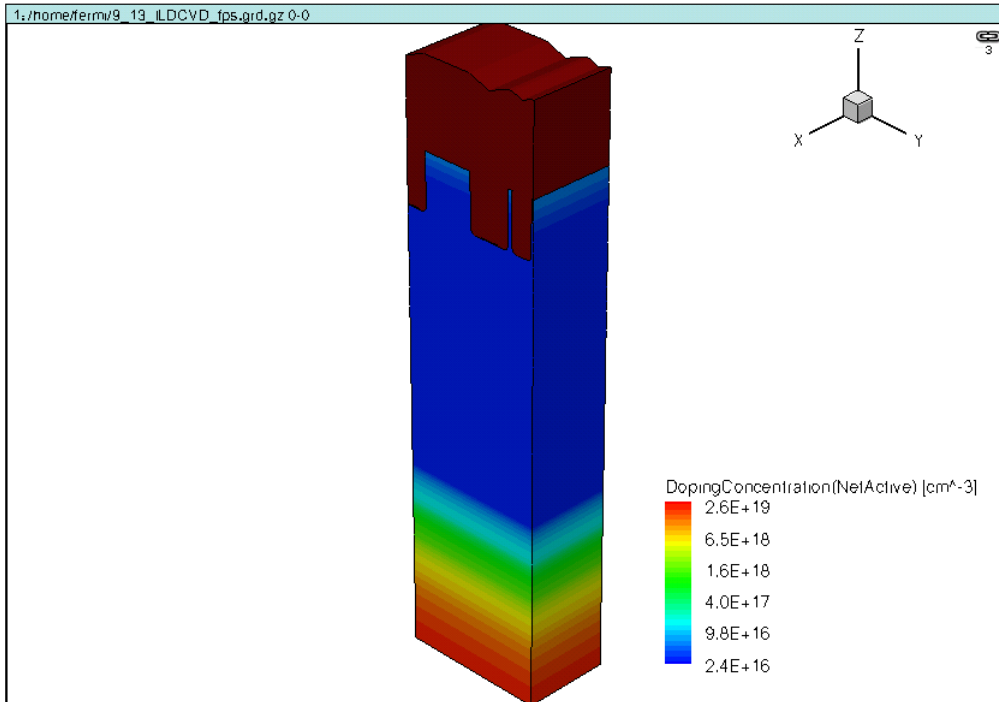


Figure 4.25 ILD CVD oxidation.

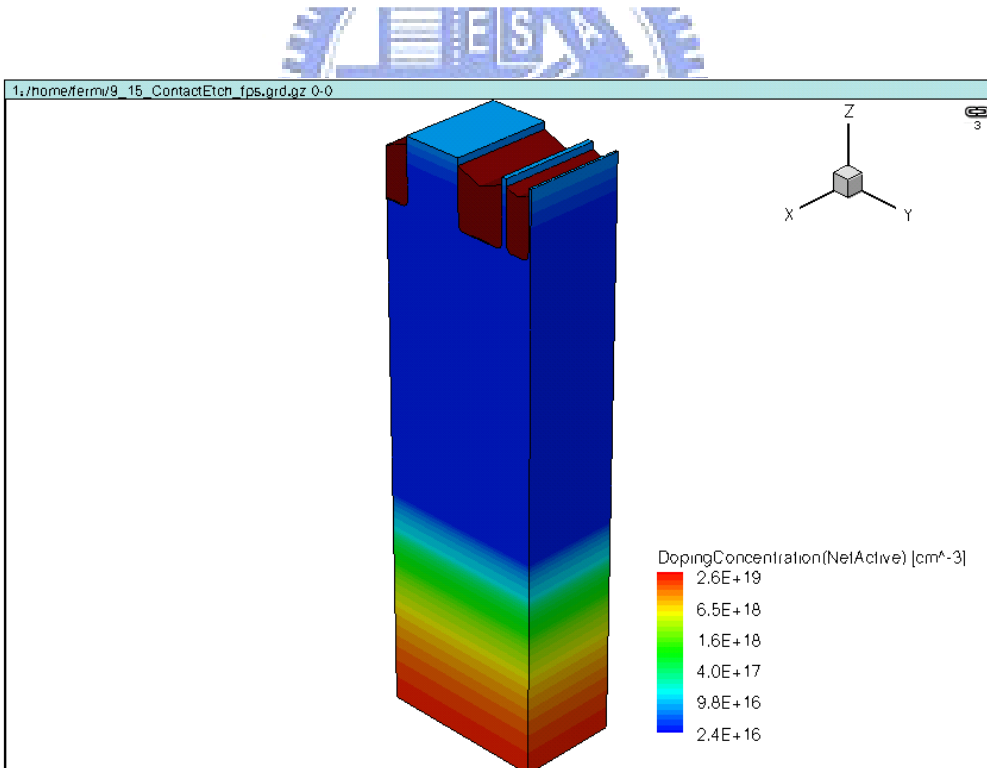


Figure 4.26 Contact etching.

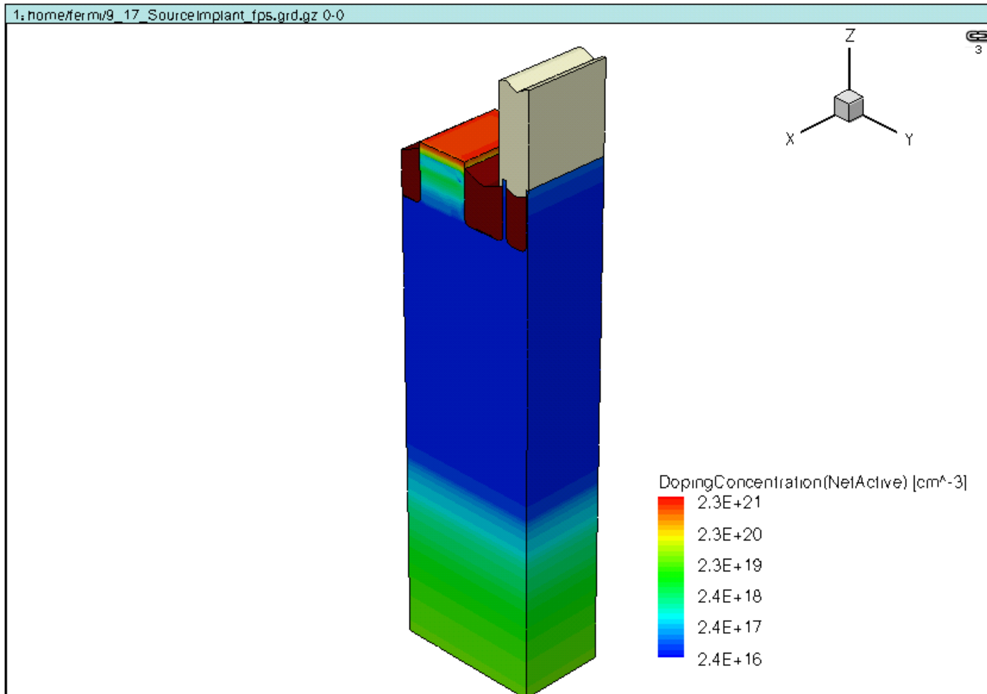


Figure 4.27 Source pattern & source implant.

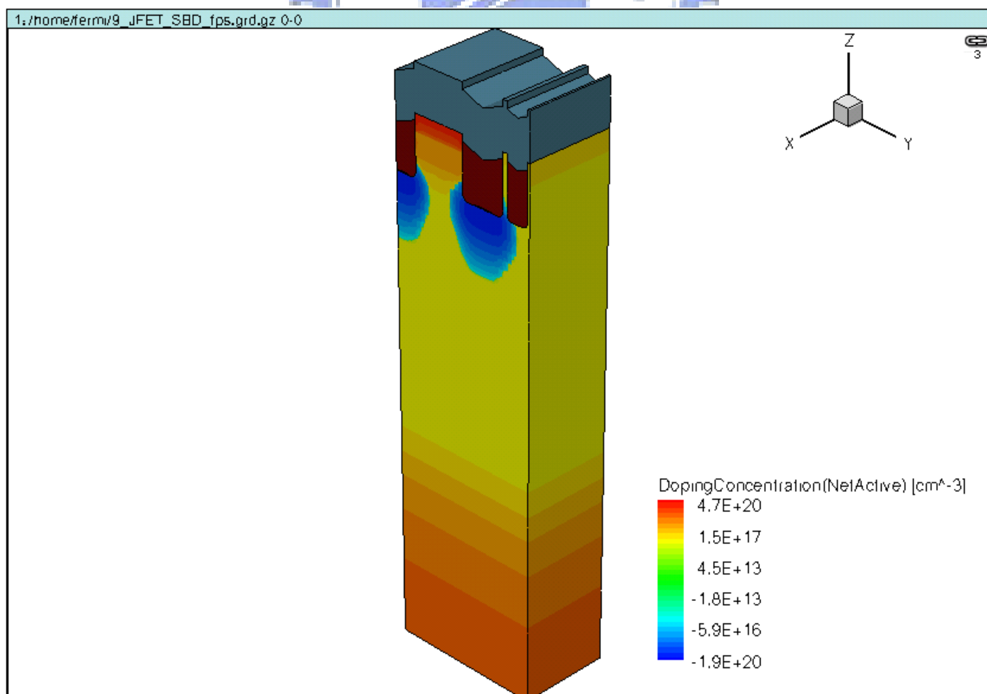


Figure 4.28 Sputter front-side metal.

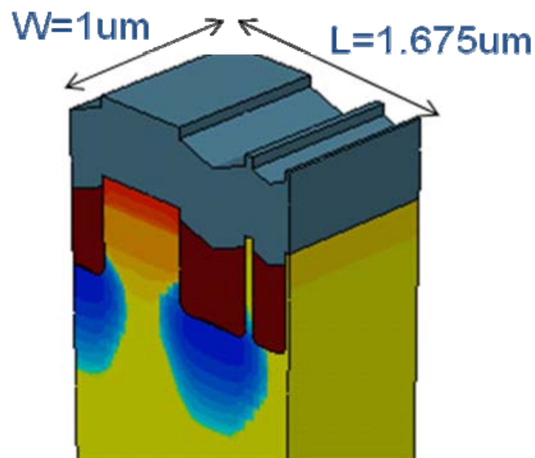


Figure 4.29 The unit cell size of three dimension simulation.

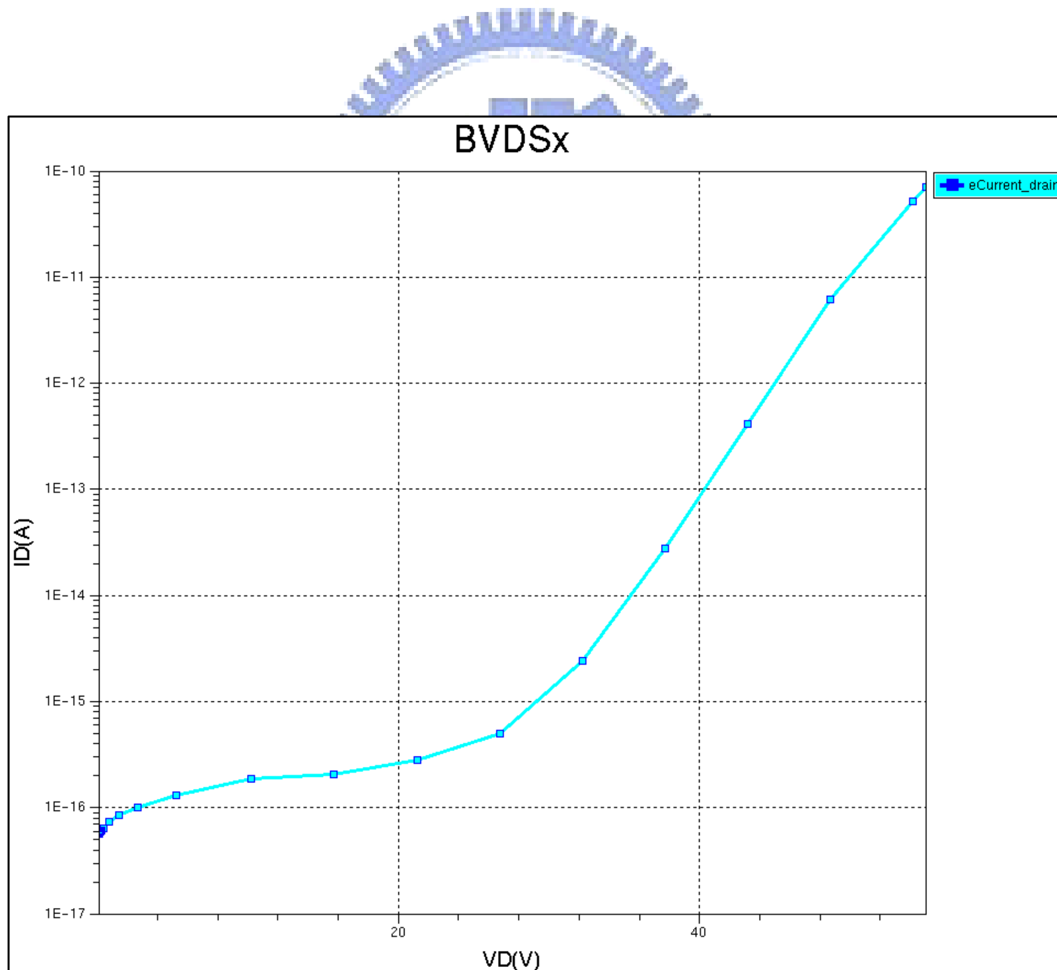


Figure 4.30 The BV_{DSX} curve of three dimension simulation.

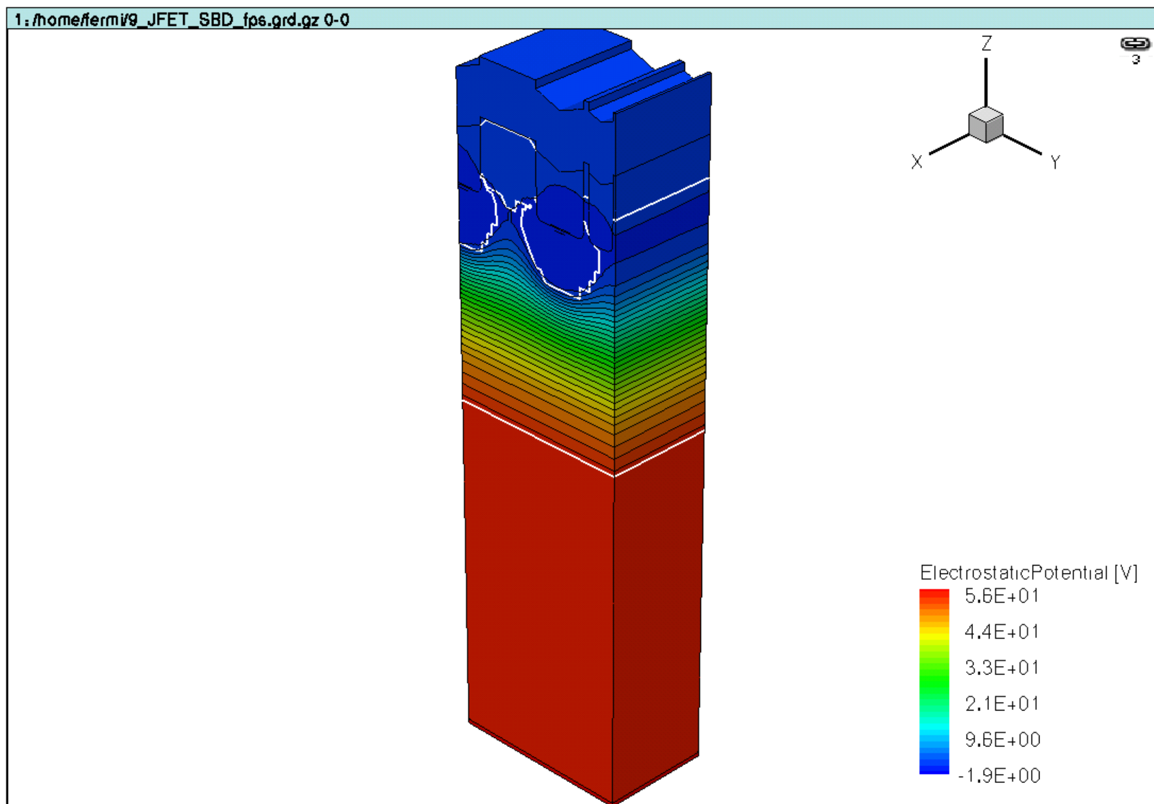


Figure 4.31 The electric potential profile at BV_{DSX}.

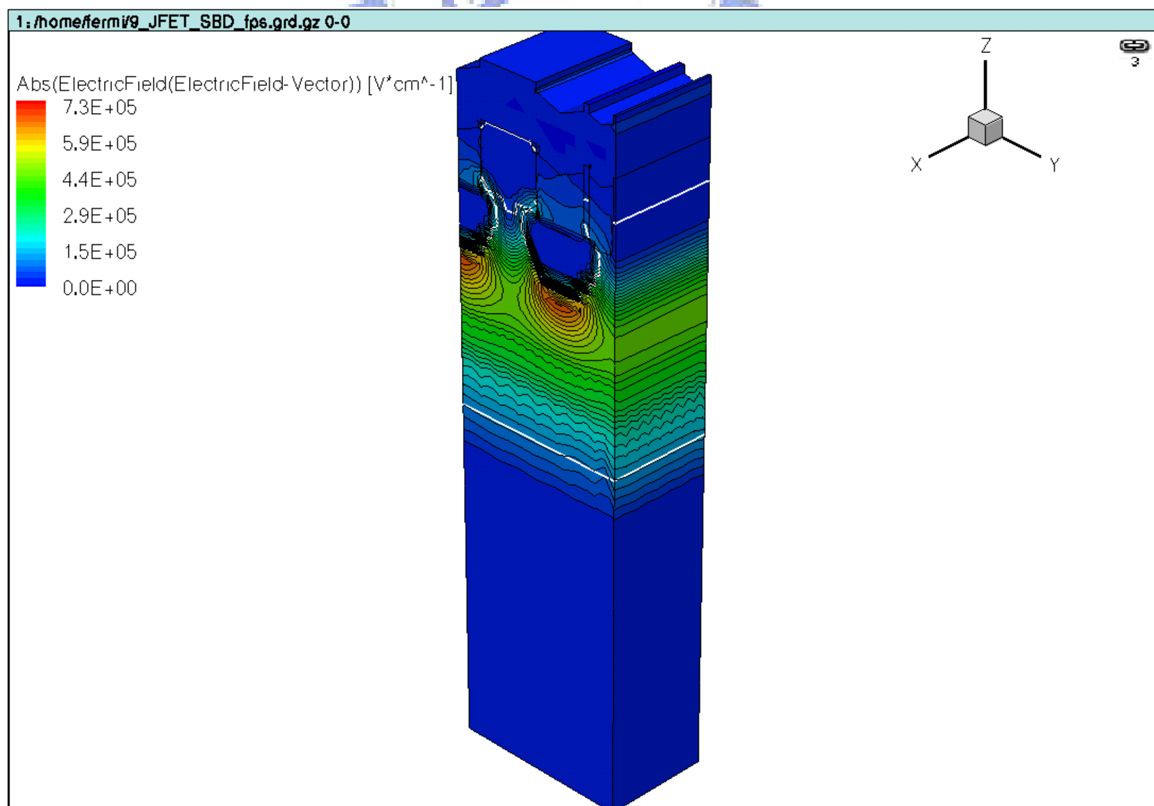


Figure 4.32 The electric field magnitude profile at BV_{DSX}.

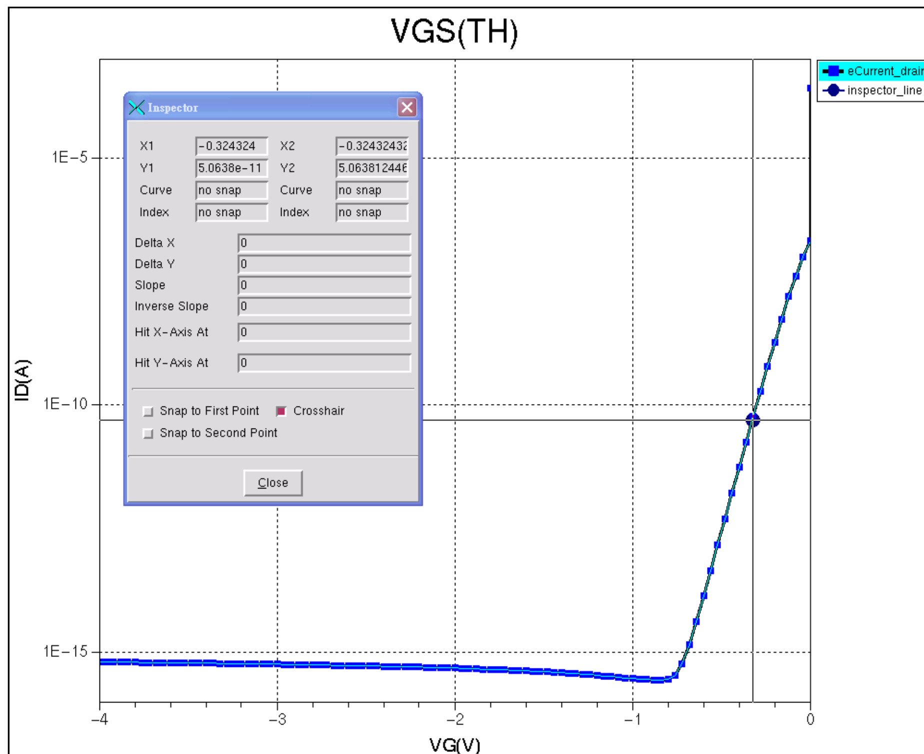


Figure 4.33 The $BV_{GS(TH)}$ curve.

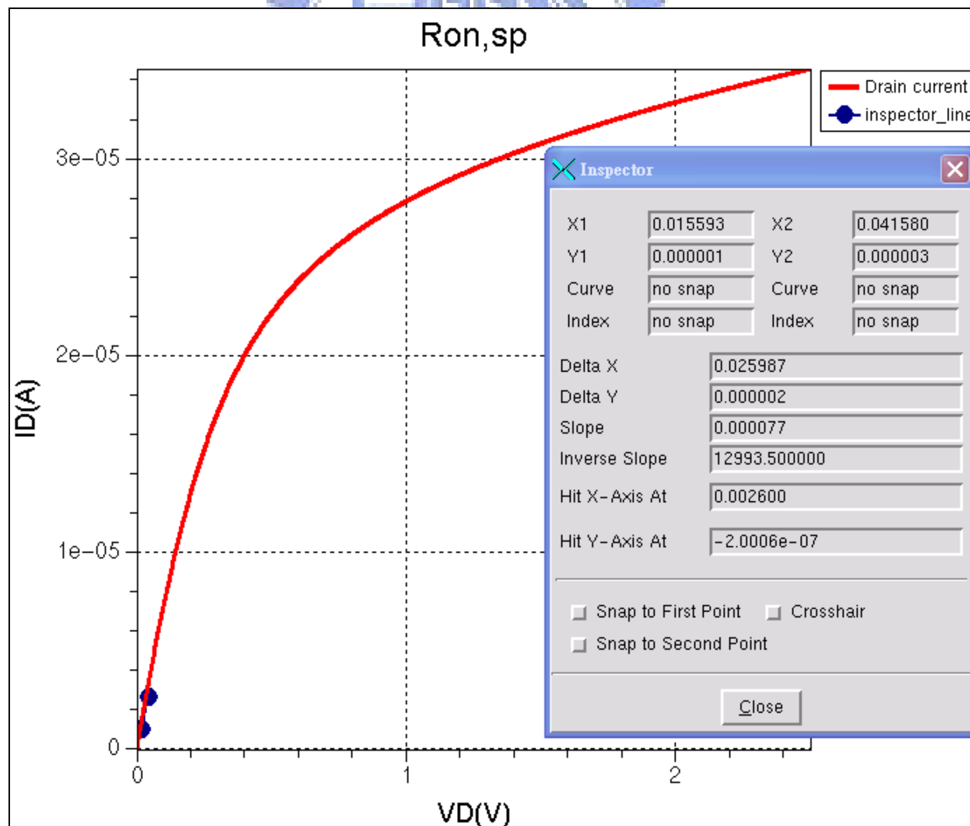


Figure 4.34 The on-state I_D-V_D curve for $R_{ds,on}$.

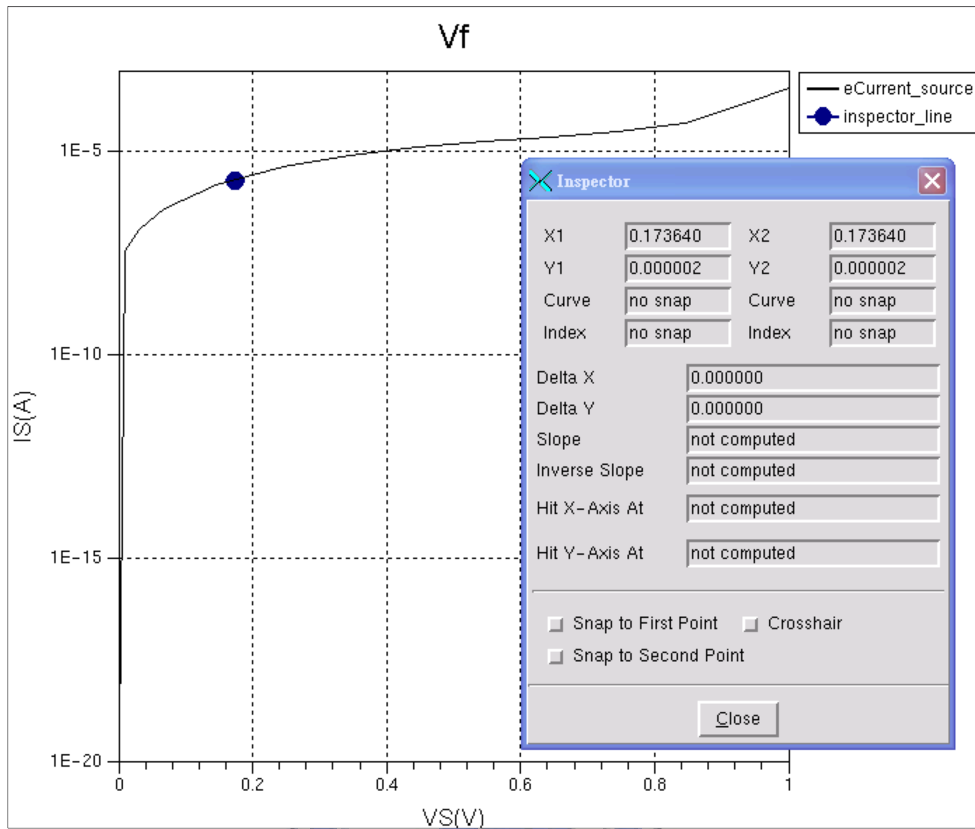


Figure 4.35 The V_F(10A) curve.

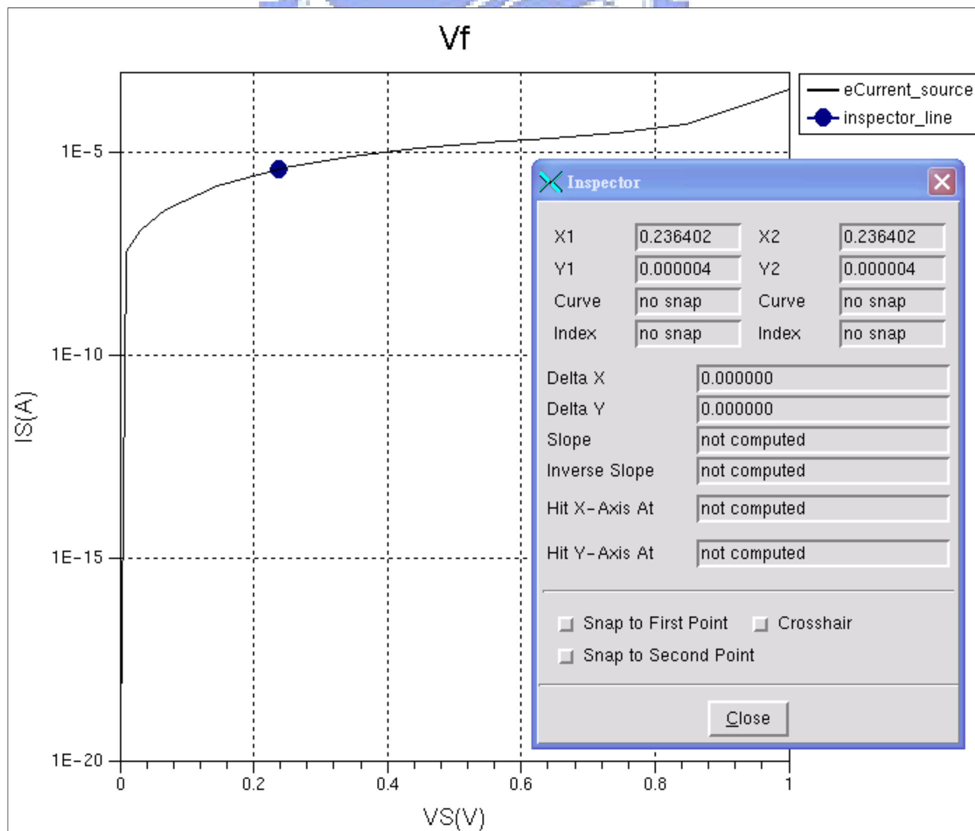


Figure 4.36 The V_F (20A) curve.

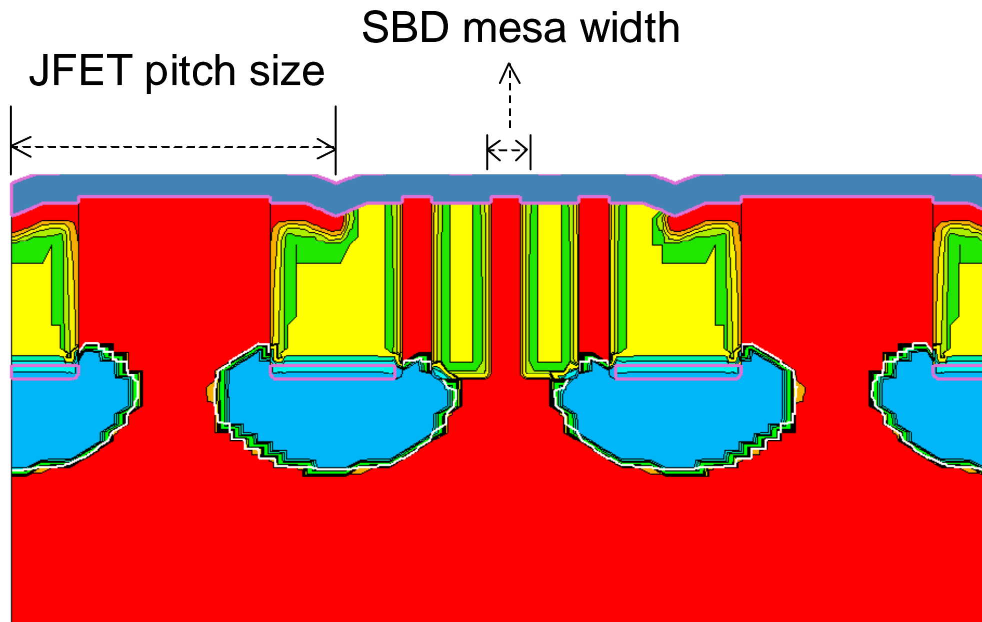


Figure 4.37 The schematic diagram of JFET pitch size and SBD mesa width.

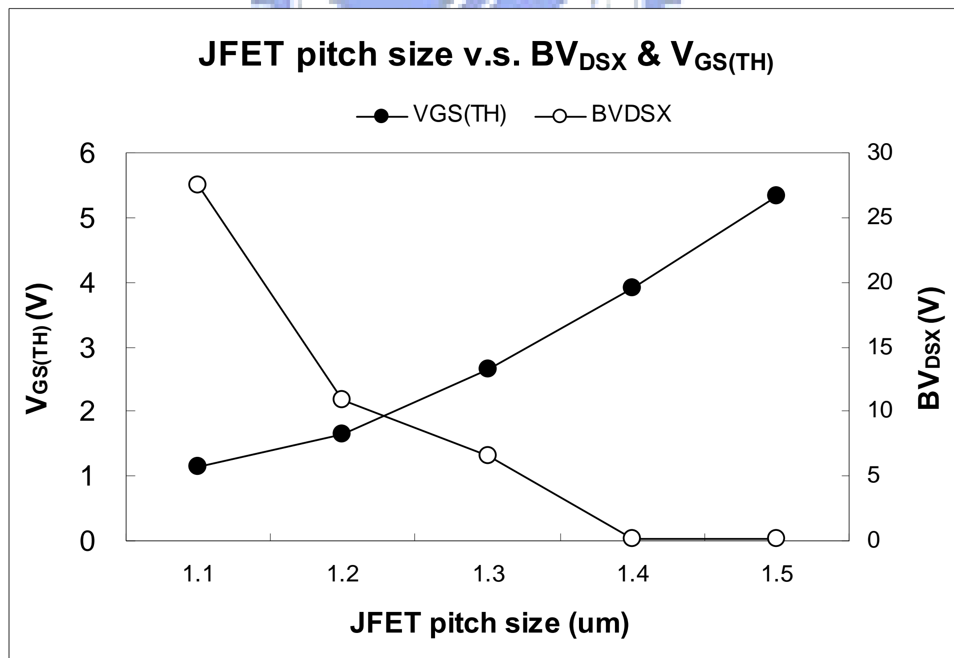


Figure 4.38 The chart diagram of JFET pitch size vs. BV_{DSX} & $V_{GS(TH)}$.

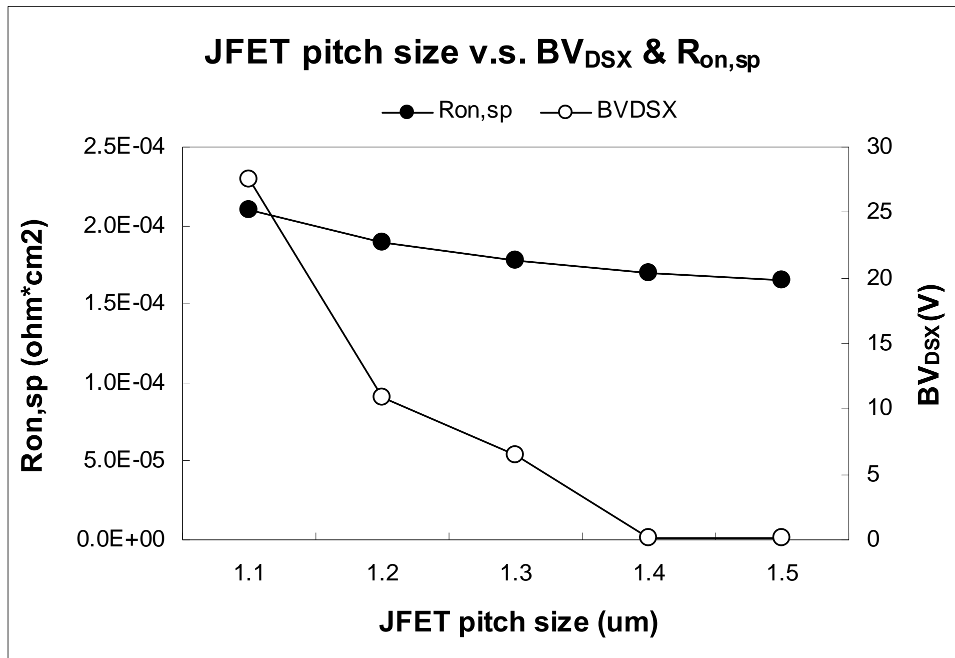


Figure 4.39 The chart diagram of JFET pitch size vs. BV_{DSX} & $R_{on,sp}$.

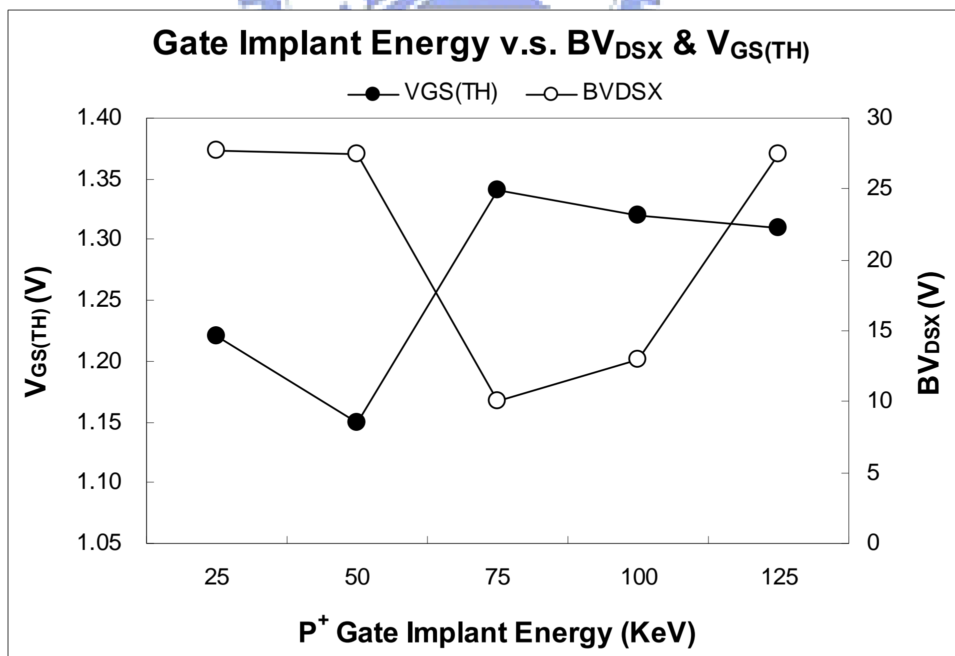


Figure 4.40 The chart diagram of P^+ gate implant energy vs. BV_{DSX} & $V_{GS(TH)}$.

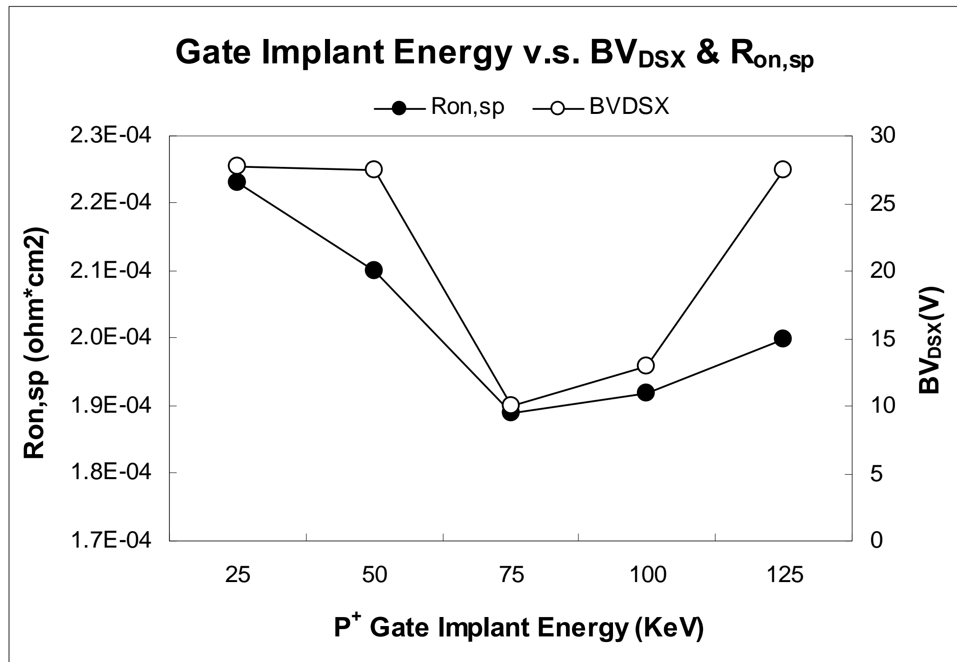


Figure 4.41 The chart diagram of P^+ gate implant energy vs. BV_{DSX} & $R_{on,sp}$.

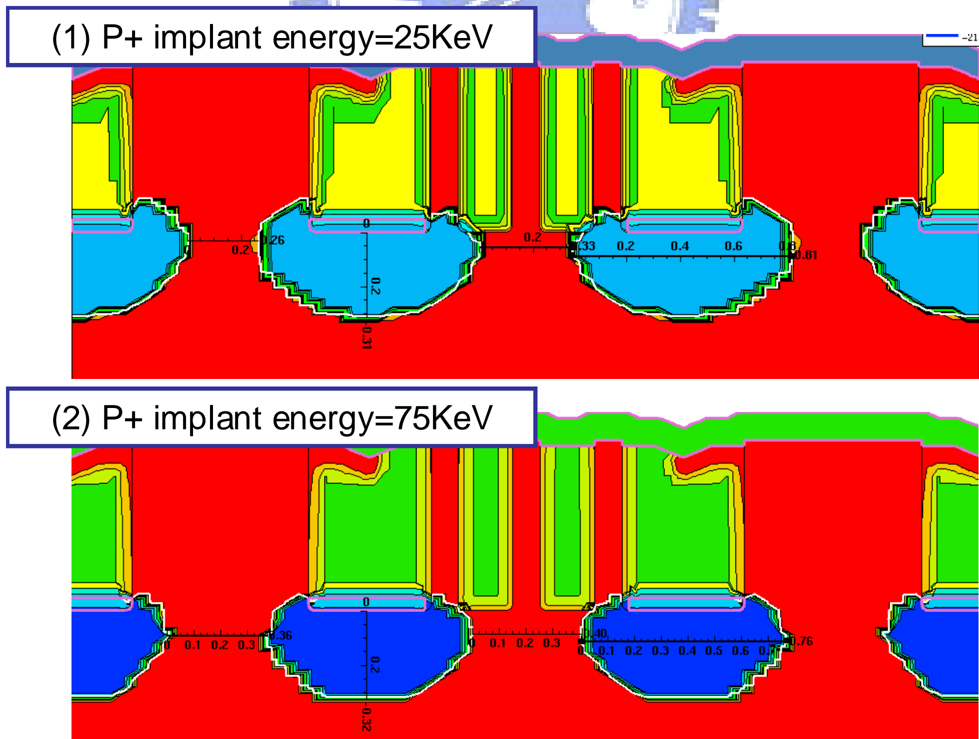


Figure 4.42 The net doping profile at different P^+ gate implant energy.

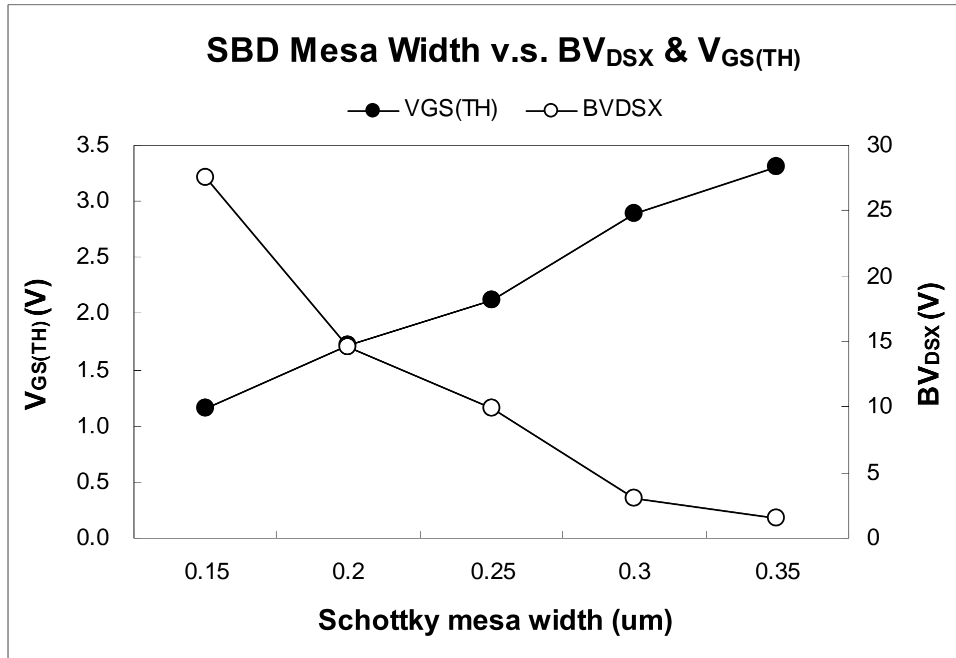


Figure 4.43 The chart diagram of Schottky mesa width vs. BV_{DSX} & $V_{GS(TH)}$.

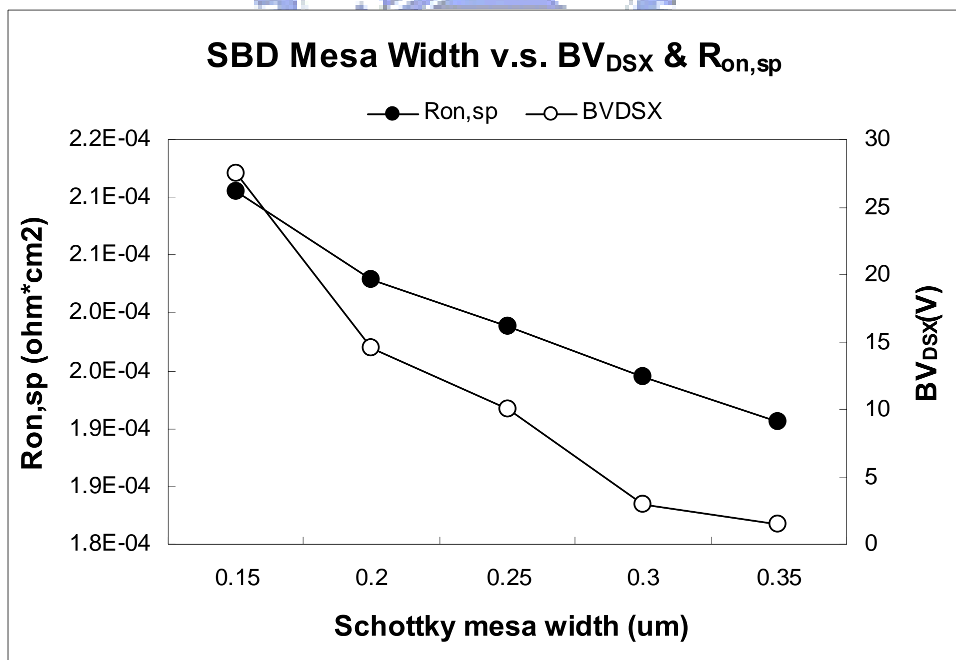


Figure 4.44 The chart diagram of Schottky mesa width vs. BV_{DSX} & $R_{on,sp}$.

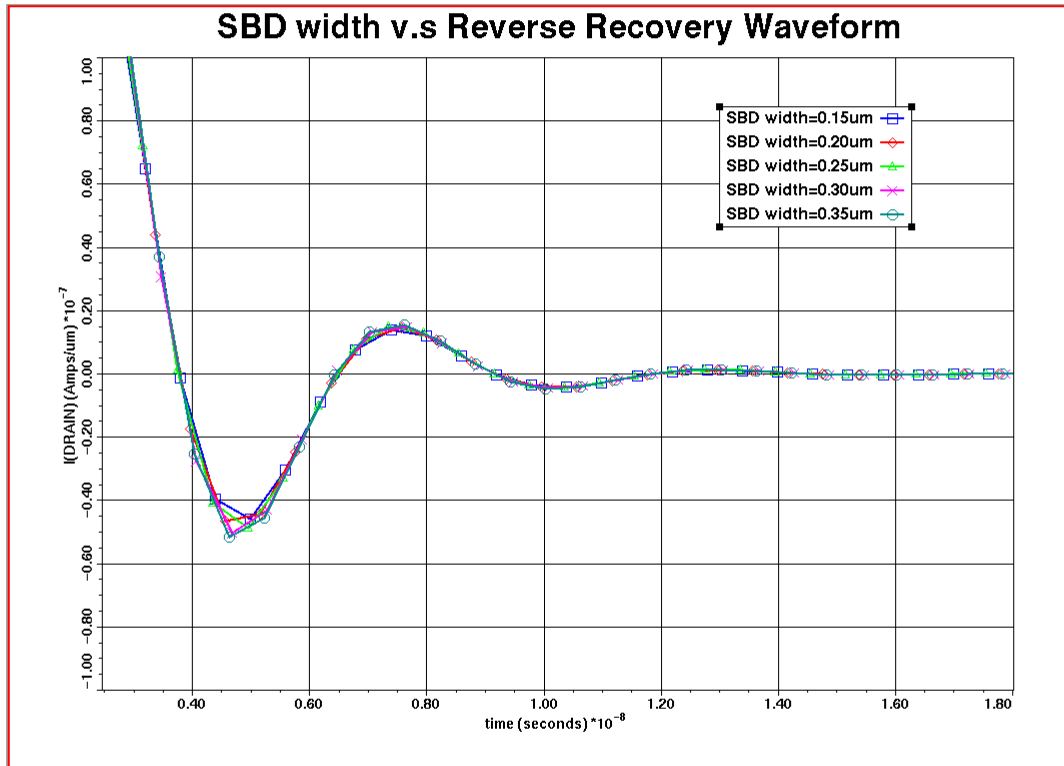


Figure 4.45 The reverse recovery waveforms at different Schottky mesa width.

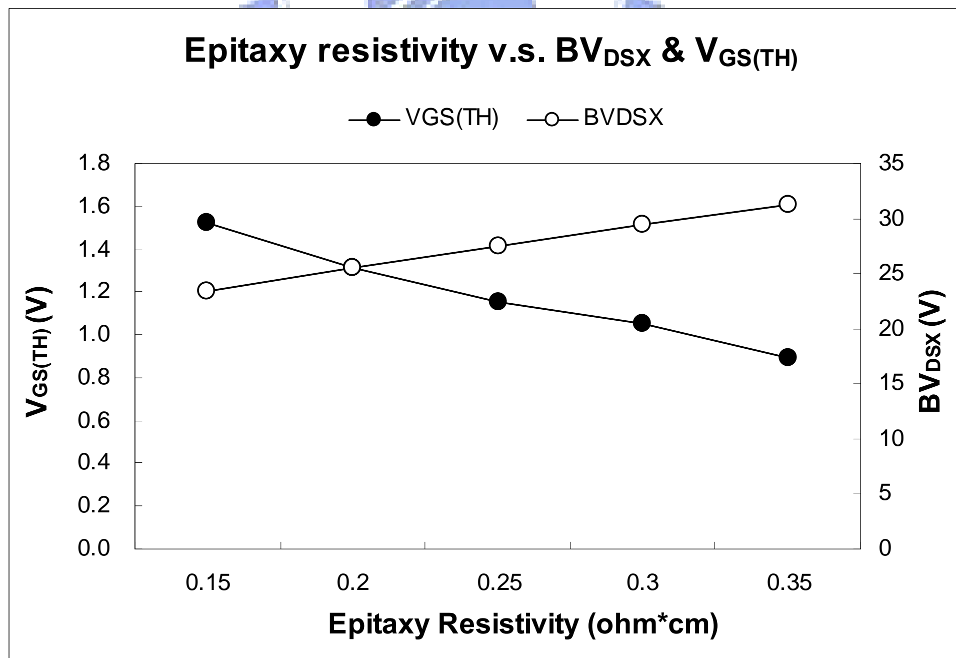


Figure 4.46 The chart diagram of Epitaxy resistivity vs. BV_{DSX} & $V_{GS(TH)}$.

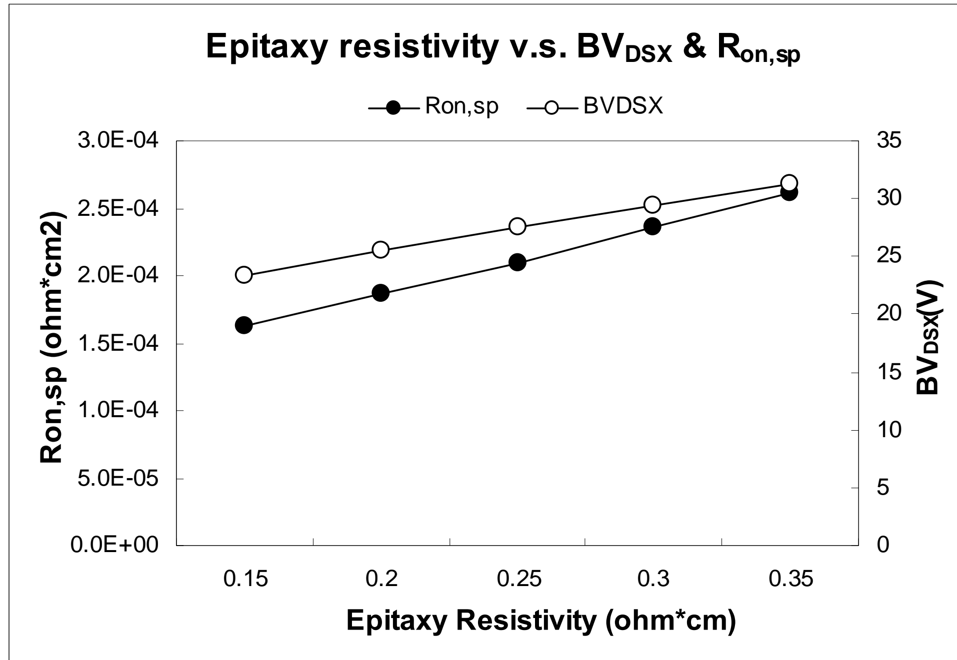
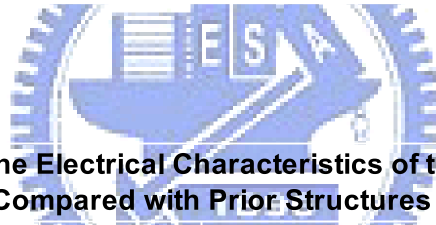


Figure 4.47 The chart diagram of Epitaxy resistivity vs. BV_{DSX} & $R_{on,sp}$.



Summary Teble of the Electrical Characteristics of the Proposal Structure Compared with Prior Structures [7]

	Lovoltech Trench JFET	IR IRF7382	Yang's JFET+JBS	This study JFET + SBD in 2D(b)	This study JFET + SBD in 3D(c)
Brief description of Schottky	Paralled SBD	PN diode	Integrated JBS	Integrated SBD	Integrated SBD
Active Area	$8.1mm^2$	-	$8.1mm^2$	$8.1mm^2$	$8.1mm^2$
BV_{DSX} (I_D=0.5mA, V_{GS}=-4V)	24V	30V	27V	27.5V	55.0V
BV_{GSO} (I_G=-1mA)	-12V	±20V	-12V	-11V	TBD
$V_{GS(TH)}$ (V_D=0.1V, I_D=250μA)	-1.0V	2.0V	-0.84V(a)	-1.2V	-0.324V
Rds,on (I_G=10mA, I_D=10A)	4.5mΩ	3.1mΩ	1.8mΩ	2.156mΩ	2.691mΩ
Ron,sp (I_G=10mA, I_D=10A)	$0.365m\Omega*cm^2$	-	$0.146m\Omega*cm^2$	$0.170m\Omega*cm^2$	$0.218m\Omega*cm^2$
I_R(V_R=20V, V_{GS}=-4V)	0.25mA	-	0.1mA	$3.412x10^{-7}A$	$2.418x10^{-9}$
V_F (I_F=10A)	0.7V	-	0.58V	0.033V	0.157V
V_F (I_F=20A)	0.9V	> 1.0V	0.72V	0.065V	0.246V
Q_{rr} (di/dt=100A/μs)	8nC	39nC	3nC	0.147nC	TBD

PS. (a) Yang's model didn't mention the biasing condition of gate threshold voltage.
(b) 2D simulation is made by Tsuprem4 and Medici.
(c) 3D simuation is made by Senturaus.

Table 4.1 Summary table of electrical characteristics of this proposal structure compared with prior structures.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this study, a novel structure of power trench junction field effected transistor integrated with Schottky barrier diode is the first time being proposed. This design provides a new alternative solution for the low side switch of synchronous buck converter. The adoption of this structure is a good solution of buck converter when considering the existed diodes. There is no parasitic inductance problem in this structure, also it has low forward voltage drop due to the embedded Schottky barrier diode on the same chip. This study includes synergetic integration technology, originality and foresight.

We use the 2D simulation tools (Tsuprem4^{TM} and Medici^{TM}) and 3D simulation tools (Sentaurus TCAD) to implement this idea. This structure not only reduces the parasitic inductances compared with Lovoltech's one [11], but also improves the reverse leakage characteristics of Yang's one [7].

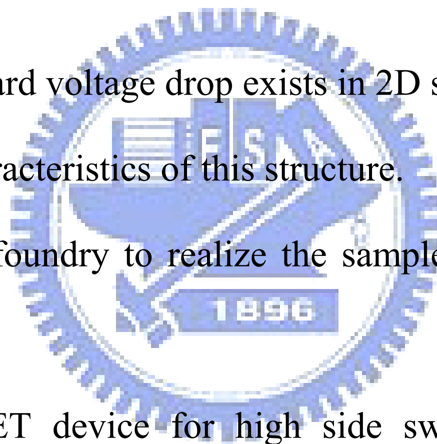
From the simulation results, we find the larger pitch size of JFET and mesa width of SBD causing higher pinch-off voltage and lower breakdown voltage of drain to source. On the other hand, it would result in lower specific on-resistance due to the larger channel width. The lighter epitaxial doping concentration would get the lower pinch-off voltage; low resistively of epitaxial layer is inversely proportional to

breakdown voltage, but proportional to on-state resistance of drain to source.

5.2 Future Work

In this dissertation, we use TCAD simulation software to realize the electrical characteristics of power trench junction field effect transistor integrated with Schottky barrier diode; this provides a pathfinder before wafer starting. However, there are some things that still need to be overcome:

1. Non-converge issue of breakdown voltage of gate to source in 3D simulation.
2. Unreasonable forward voltage drop exists in 2D simulation.
3. Study dynamic characteristics of this structure.



4. Find a cooperator foundry to realize the sample and measure its electrical characteristics.
5. Design a new JFET device for high side switch of synchronous buck converter
6. It needs a new design of gate driver circuit to drive this synchronous buck converter that configured by JFET devices.

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