國立交通大學

電子工程學系 電子研究所

碩 士 論 文

光纖通訊類比前端電路設計與製作

Design and Implementation of Analog Front-end Circuits for Optical Communication System

研 究 生：林 大 新

指導教授：陳 巍 仁 教授

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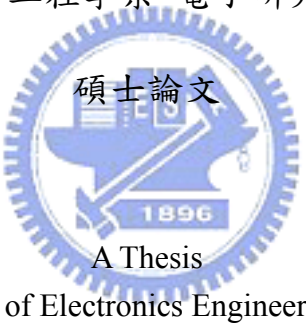

碩士論文

A Thesis

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光纖通訊類比前端電路設計與製作

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摘要

這篇論文分成兩個部分。 首先,我們將介紹一個差動主動回授轉阻放大器。轉阻放大器差動直流耦合光二極體電流, 所使用的製程為0.18微米CMOS技術。轉阻增益為56dBΩ, 在光二極體寄生電容為0.2pF的條件下操作的資料傳輸速度能達到3.125Gbps。 輸入端的參考雜訊電流為1.2μArms。 操作電壓為 3..3(V)伏特, 總功率耗損是79(mW)毫瓦。 晶片尺寸是738乘1522(μm^2)微米平方。

第二, 我將討論一個增益為90dBΩ光纖前級接收端電路所使用的製程為0.18微米CMOS技術。 在此設計中我將轉阻放大器度(TIA)與自動增益控制電路(AGC)以及限幅放大器(LA)整合成單一晶片, 當驅動50Ω系統時, 接收器前端電路直接把光電流轉化成一個900 mV(pp)的差動輸出信號。 在輸入信號為2^{31}-1假亂數訊號時接收器的最小輸入光功率是-13 dBm被容忍的輸入功率能達到0 dBms所能達到的位元錯誤率小於10^{-12}。 接收者前端提供的頻寬為7.86 GHz兒而增益頻寬乘積為248.5THz超過到目前為止所發表設計。 為了達到展延頻寬的目地我们在接收器電路裡採用了立體對稱式電感。 在1.8(V)伏特的供應電壓操作下, 總功率耗損是199(mW)毫瓦。 小片尺寸是1300乘1566(μm^2)微米平方。

Design and Implementation of Analog Front-end Circuits for Optical Communication System

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Abstract

This thesis is divided into two part. First, a design of the differential active feedback trans-impedance amplifier is discussed. A trans-impedance amplifier with differential dc-coupled photocurrent sensing was integrated in 0.18μm CMOS technology. It achieves 56dBΩ trans-impedance gain and the operating data rate is up to 3.125Gbps with a 0.2pF photodiode capacitance. The input referred noise current is 1.2μArms. Operating under a 3.3V supply, the total power dissipation is 79mW. Chip size is 738μm×1522μm.

Secondly, the 90dBΩ optical receiver analog front-end fabricated in a 0.18 μm CMOS technology is discussed. Integrating trans-impedance amplifier (TIA), automatic gain control circuit, and post limiting amplifier (LA) on a single chip, the receiver front-end converts photo current to a differential output signal of 900 mV (pp) directly when driving 50 Ω output load. The sensitivity of the optical receiver is -13 dBm at a bit-error rate of 10^{-12} with $2^{31} - 1$ pseudo-random bits input, and the tolerated input power is up to 0 dBm. The receiver front-end provides a -3 *dB* bandwidth of 7.86 GHz and a corresponding GBW of 248.5 THz that exceeds prior arts reported to date. 3-D symmetric transformers are utilized in the AFE design for bandwidth enhancement. Operating under a 1.8V supply, the total power dissipationis 199 mW. Chip size is 1300 μm × 1566 μm.

誌謝

回顧兩年多的研究生生涯過程充滿了許多令人難忘的回憶與經驗。兩年應該是一個很長的時間可是我卻覺得時間過的很快，因為總有做不完的事在後面等著。在這兩年當中，修課，做研究，一直是整個生活的重心。我想在我們老師的嚴格帶領下應該是很少有人能夠覺得輕鬆的。不過也正因為老師的治軍嚴僅， 讓我能夠在混合訊號電路設計的領域能夠有扎實的基本訓練。所設計的電路也能有不錯的成果，例如 2004ESSCIRC 我们發表了一篇論文，讓我能有機會前往比利時，用著還可以的英文來發表我们的研究成果。當然也順道瀏覽了比利時明媚的風光，這趟旅程是很值得回億的一趟知性之旅。

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Chapter 1

Introduction

Motivation

Recently, the rapid increase of data traffic, as a result of the dramatic growth of Internet and intranet, has stressed the need for a drastic increase in network bandwidth. The constantly increasing demand for high speed data rates in communication applications leads to the wide development of optical data transmission. Optical fiber is the preferred physical medium since its robustness and simpler system implementation due to its almost unlimited bandwidth. For such demands, the system with data rates greater than 10 Gb/s are actively investigated, e.g., in [1][2][3]. Although such circuits do exist in Si-Bipolar or GaAs processes for several years, with the blooming progress in VLSI technology, the successful use of standard CMOS will provide the low cost solution required for mass installation of such systems [4][5]. Moreover, the most attractive aspect of using CMOS

technology is its capability of high-level integration. In this thesis, the design and implementation of the optical front-end receiver carried out by a single CMOS chip is proposed.

Synchronous Optical Network (SONET) is the standard defining the rates and formats for optical communication. A similar standard, Synchronous Digital Hierarchy (SDH), has established in Europe as well. SONET and SDH are technically consistent standards. With the worldwide acceptance of the SONET/SDH and ATM standards, fiber optical networks operating at 155.52 Mb/s, 622.08Mb/s and 2.48832 Gb/s and 9.95328 Gb/s are being widely deployed for service, as listed in **Table 1-1**. In this thesis, the design of 10 Gb/s (SONET OC-192) is investigated and explored.

SONET STANDARD	SDH STANDARD	BIT RATE
OC1	-	51.84Mbps
OC3	STM1	155.52Mbps
OC12	STM4	622.08Mbps
OC48	STM16	2.4883Gbps
OC192	STM64	9.9533Gbps
OC768	STM256	39.813Gbps

Table 1-1 SDH/SONET fiber system.

Thesis Organization

Fig.1-1 shows a typical optical communication system. Digital data is firstly decoded, amplified, then drives the laser source. A photodetector and a transimpedance amplifier at receiving end translate the optical signal to a voltage data. Limiting amplifier serves as an amplitude control function to keep a constant output level, which helps the following CDR to extract the correct timing sequence. At last, the transmitting digital data is recovered. In this thesis, design issues of receiver front-end are divided into five chapters, of which this is the first.

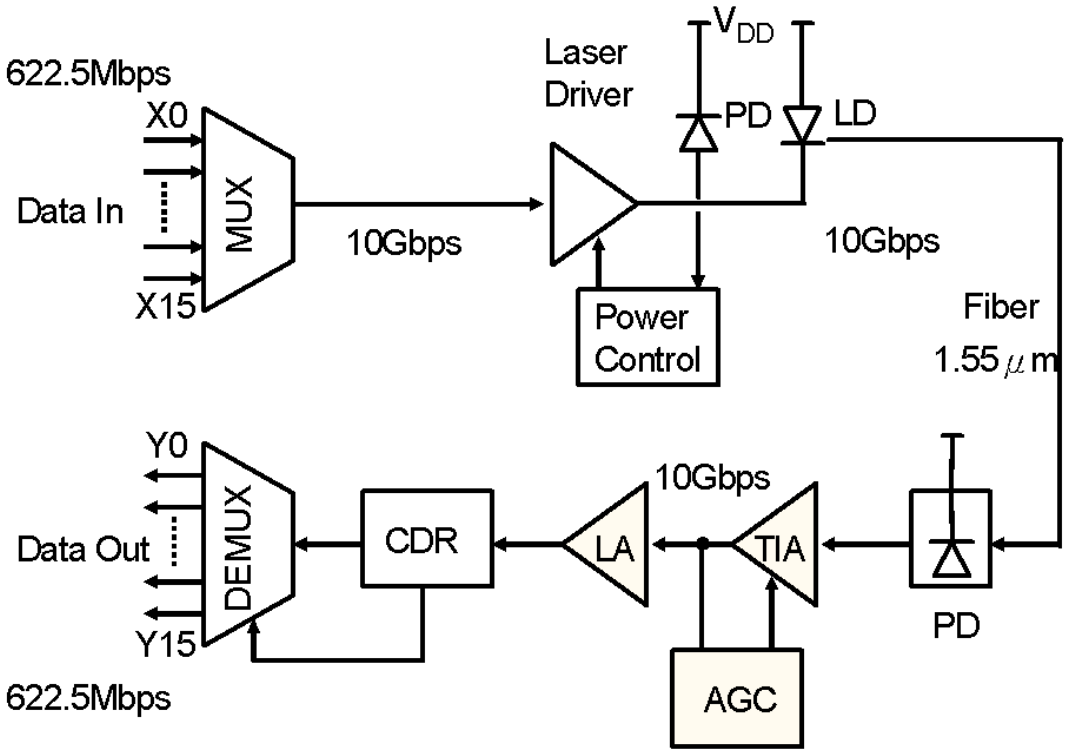
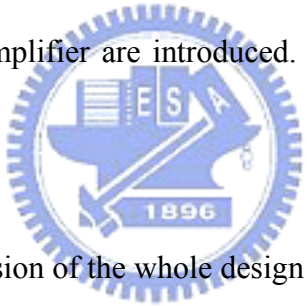


Fig. 1-1 The fiber optical communication system

Chapter 2 describes the specifications and design considerations of front-end receiver.

Chapter 3 introduces trans-impedance amplifier (TIA). First, I will point out the design issues. Second, differential active feedback TIA architecture will be described. Noise analysis is analyzed then. At last, experimental results will be showed.

Chapter 4 introduces the architecture of receiver analog front-end. Inductive peaking is adopted for bandwidth enhancement in the broadband amplifier design. Then, this chapter describes a novel 3-dimensional fully-symmetric transformer that is utilized in this design. Compared to the prior arts of plannar symmetric[6] or stacked asymmetric [7][8] structures, chip area can be drastically reduced using the proposed transformers. Next, the design of transimpedance amplifier, automatic gain control circuit and limiting amplifier are introduced. And finally, the experimental results is describes.



In chapter 5, final conclusion of the whole design is given.

Chapter 2

Receiver Front-End and Design Considerations

2.1. Introduction

Today, optical communications, in combination with microwave and wireless technologies, are enabling the construction of high capacity networks with global connectivity. Report says, the load on the global Internet backbone will be as high as 11Tb/s by the year 2005 [9]. Among the available transmission media, optical fibers achieve the highest bandwidth and the lowest loss. These characteristics make them an attractive medium for transmission of data over long distance.

In this chapter, the optical transceiver will be introduced briefly, and the design challenges and system specifications of the receiver front-end will be listed. At last, the frequently used passive component, inductor and transformer, will be compared.

2.2. Optical Transceiver Architecture

The goal of an optical communication system is to carry large volumes of data across a long distance. Despite the unique transmission capabilities of optical fibers, the data gets distorted as it travels through the fiber. To alleviate the distortion mostly due to the fiber dispersion, a wavelength of 1.55μm is appropriate. Depicted in Fig. 2-1 is a fiber optical transceiver. The data provided to the transmitter is in the form of many low-speed (622.5Mbps) channels (parallel data) since it is generated by multiple users. A multiplexer converts the parallel signal to serial high speed (10Gbps) bit stream. The bit stream is then converted to optical power through laser driver and laser diode. The CMU provides the clock signals at 10GHz for the multiplexer.

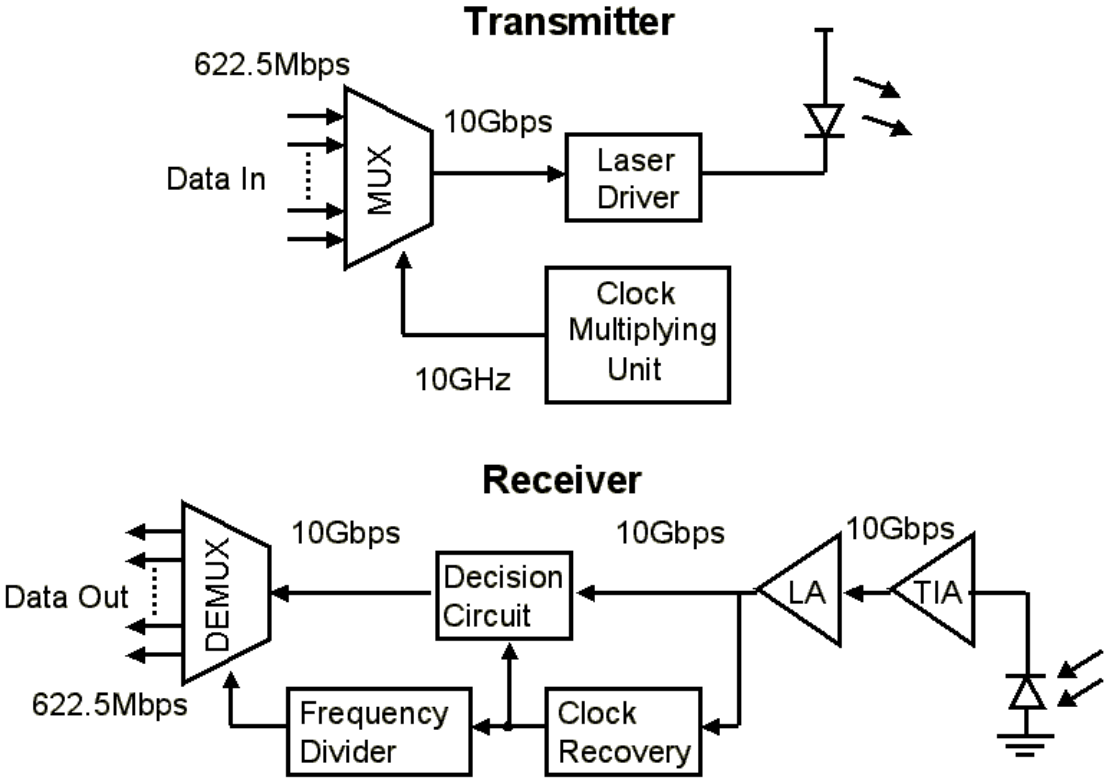


Fig. 2-1 Fiber optical transceiver

In the receiver, the received light is transformed to an electric current by the photodiode. The current is then converted into a voltage signal with sufficient swing for the proceeding blocks by the trans-impedance amplifier and limiting amplifier. Moreover, since the received data may exhibit substantial noise, a decision circuit is interposed between the limiting amplifier and the DEMUX. A clock recovery generates a clock whose rising/falling edges fall at the midpoint of each point to the decision circuit. And similar to multiplexing, the retimed high speed data is subsequently split among parallel sequences of lower speed by the demultiplexer. In this thesis, my work is focus on the receiver front-end including TIA and LA.

While the system topology of Fig. 2-1 has not changed much over the past several decades, the design of its block and the level of integration have. Typically, the optical transceiver is divided into four single-chip blocks: (i) the PLL/MUX circuit, (ii) the laser driver along with its power control circuitry, (iii) the TIA/LA combination, and (iv) the CDR/DEMUX circuit. As the supply voltage scales down, the difficulty of circuit design for each block increases relatively

2.3. Specifications of Receiver Front-End

. Before designing a circuit, some systematic requirements should be described. In this section, some specifications of receiver front-end will be listed. Since noise, sensitivity, gain, and bandwidth of the receiver front-end dominate the performance of the overall receiver, we focus the design issues on these aspects.

1. ***Sensitivity and noise:*** In the receiver, one of the most important requirements is its sensitivity. The sensitivity of the receiver is the minimal input power of light for a given bit error rate (BER), 10^{-12} for system required. The minimal accepted

input power and the corresponding sensitivity can be described as [10]

$$Pin = \frac{SNR \cdot \sqrt{\overline{I_{n,total}^2}}}{R} \tag{2-1}$$

$$Sensitivity = 10\log\frac{P_{in}}{2\times 1mW}(dBm) \tag{2-2}$$

Where Pin is the minimum input power, R is the responsivity of photodiode, SNR indicates a ratio of signal (peak-to-peak signal swing) to noise (root-mean-square value, which can be obtained by integrating the noise across the entire bandwidth), and $\sqrt{\overline{I_{n,total}^2}}$ denotes the total input referred noise current of the receiver. The noise current of the receiver can be described as

$$\sqrt{\overline{I_{n,total}^2}} = \sqrt{\overline{I_{PD}^2} + \overline{I_{TIA}^2} + \overline{V_{LIA}^2}/R_T^2} \tag{2-3}$$

It includes the noise contributed from the photodiode, TIA, and LA divided by TIA transimpedance. Usually, TIA dictates this noise performance.

According to OC-192 SONET standard, the sensitivity required for short-haul (10km~40km) [11] communication system is –12dBm. If we assume the sensitivity of TIA is –13dBm. From (Eq. 2-1) one can get the noise current should be smaller than ***7μA*** under the assumption of R=1A/W, and SNR=14.1 (BER=10^{-12}) [12]. Hence the minimum input current to TIA is about ***98.7μA***.

2. ***Gain:*** Divide the receiver gain into two part, transimpedance gain and additional voltage gain of LA. The sensitivity of LA at BER=10^{-12} is generally about 5mV, in order to achieve the sensitivity of receiver below -12dBm the transimpedance gain must be ***178Ω (45dBΩ)***. However, the higher the transimpedance gain less

the contribution of noise from the other blocks in the receiver. This forces one to design a TIA with transimpedance gain higher than 178Ω. On the viewpoint of LA gain, to achieve a sufficient output voltage swing (e.g. 400mV), the voltage gain must be higher than ***80 (38dB)*** in the worst case.

3. ***Bandwidth:*** The overall receiver must have a bandwidth of ***6.5GHz*** [13] to avoid intersymbol interference (ISI) but must meet the minimum sensitivity requirement which is –12dBm for short-haul communication at BER of 10^{-12}. The bandwidth of the overall receiver is determined mostly by the transimpedance amplifier. The TIA bandwidth is typically chosen to be equal to 0.7 times the bit rate under the compromise between noise and ISI. Hence, the LA bandwidth is typically designed >10GHz to cause no ISI. Table 2-1 lists the summary of receiver front-end specifications.

Specifications of receiver front-end			
Features	Receiver Overall	TIA	LIA
Gain	>83dBΩ	>45dBΩ	>38dB
Bandwidth	6.5GHz	>7GHz	>10GHz
Sensitivity @ BER=10^{-12}	-12dBm	-13dBm	5mVp-p
Noise	<9μA	<7μA	<0.354mV
Dynamic Range	-12dBm ~ >0dBm	-13dBm ~ >0dBm	-

Table 2-1 Summary of receiver front-end specifications

2.4. Design Consideration

2.4.1. Jitter

2.4.1.1. Introduction

Timing jitter, edge speeds, aberrations, optical dispersion, and attenuation all impact the performance of high-speed clock recovery for SDH/SONET receivers (Figure 2-2). These effects decrease the time available for error-free data recovery by reducing the received “eye opening” of nonreturn-to-zero (NRZ) transmitted signals.

Optical receivers, incorporating transimpedance preamplifiers and limiting postamplifiers, can significantly clean up the effects of dispersion and attenuation. In addition, these amplifiers can provide fast transitions with minimal aberrations to the

subsequent clock/data recovery (CDR) blocks. However, these stages also add distortions to the midpoint crossing, contributing to timing jitter. Timing jitter is one of the most critical technical issues to consider when developing optical receivers and CDR circuits.

A better understanding of the different sources of jitter helps in the design and application of optical receiver modules and integrated CDR solutions. SDH/SONET specifications are well defined regarding the amount of jitter tolerance allowed at the inputs of optical receivers, as well as jitterpeaking requirements, but they do little to define the different sources of jitter. The jitter that must be tolerated at an optical receiver input involves three significant sources, all of which are present to varying degrees in typical receiver systems [14]:

1) Random jitter (RJ)

2) Pattern-dependent jitter (PDJ)

3) Pulse-width distortion (PWD)

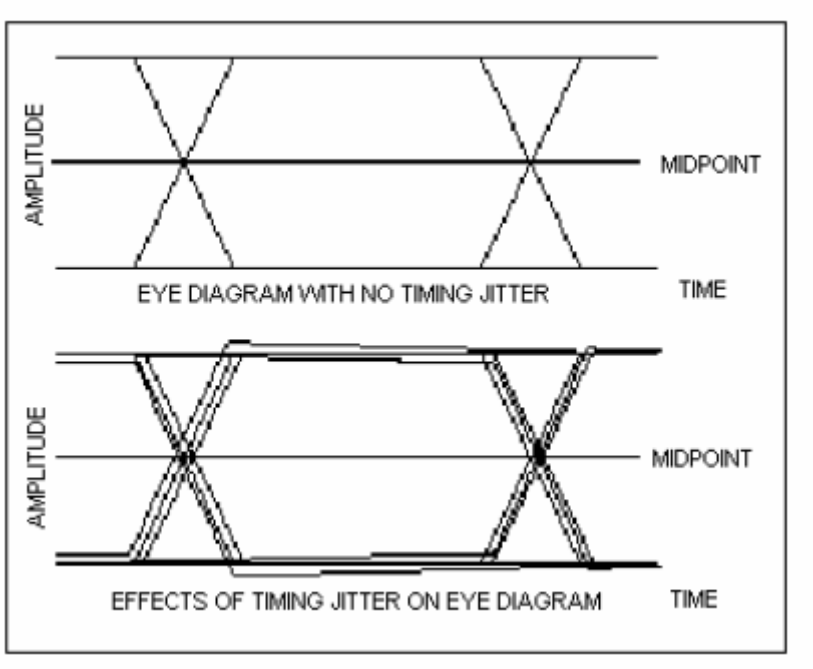


Fig. 2-2 Eye diagram with and without timing jitter

2.4.1.2. Random Jitter(RJ)

RJ is caused by random noise present during edge transitions (Figure 2-3). This random noise results in random midpoint crossings. All electrical systems generate some random noise; however, the faster the speed of the transitions, the lower the effect of noise on random jitter. The following equation is a simple worst-case estimation of random jitter:

RJ (RMS) = (RMS noise) / (slew rate)

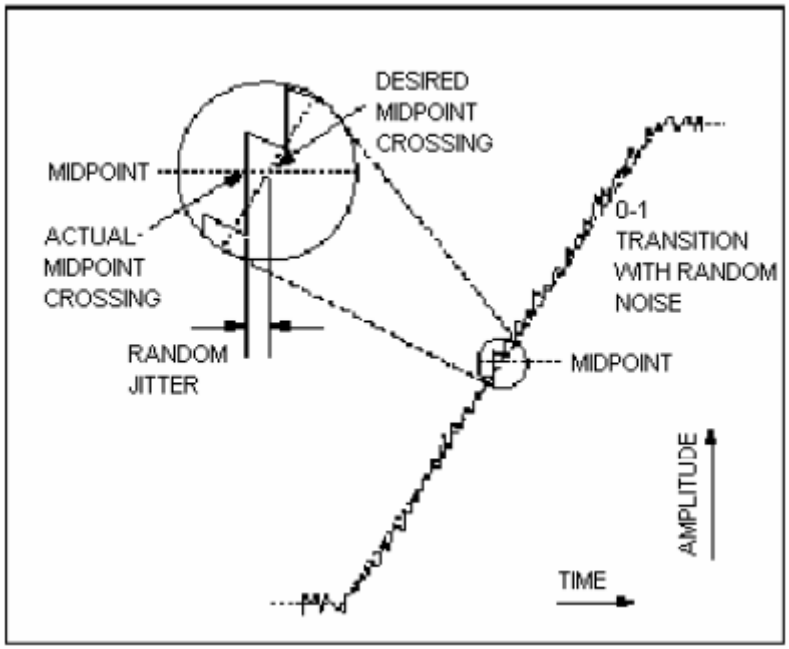


Fig. 2-3 Random jitter on edge transition

2.4.1.3. Pattern-Dependent Jitter(PDJ)

PDJ results from wide variations in the number of consecutive bits contained in NRZ data streams working against the bandwidth requirements of the receiver (Figure 2-4). The location of the lower -3dB cutoff frequency is important and must be set to pass the low frequencies associated with long, consecutive bit streams. AC-coupling is common in optical receiver design.

When using a limiting preamplifier with a highpass frequency response, select the input AC-coupling capacitor into the postamplifier, C_{AC}, in order to provide a low-frequency cutoff (f_C) one decade lower than the preamplifier low-frequency cutoff. As a result, the PDJ is dominated by the low-frequency cutoff of the preamplifier.

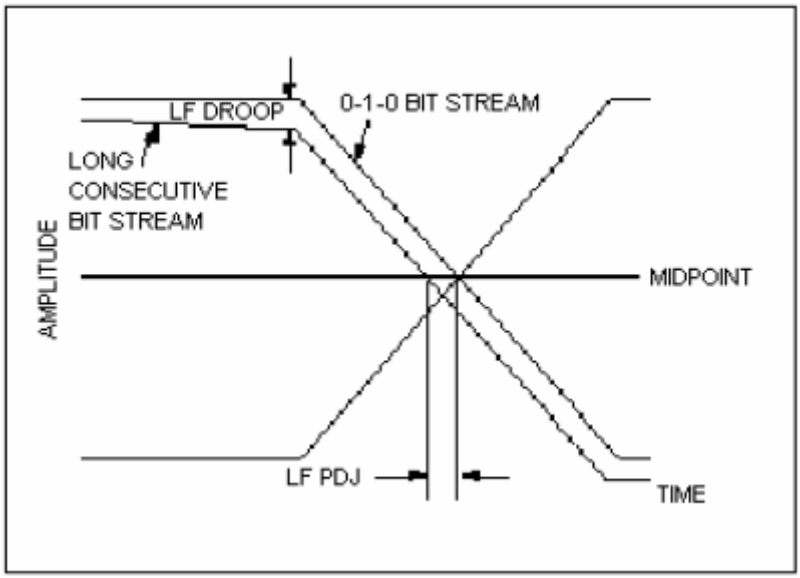


Fig. 2-4 Pattern-dependent jitter due to low-frequency cutoff

When using a preamplifier without a highpass response, the following equation provides a good starting point for choosing C_{AC} into the postamplifier:

$$C_{AC} \geq \frac{-t_L}{Rin \ln\left[1 - \frac{(PDJ)(BW)}{0.5}\right]}$$

where t_L = duration of the longest run of consecutive bits of the same value (seconds); Rin = input resistance of the postamplifier; PDJ = maximum allowable pattern-dependent jitter, peak-to-peak (seconds); and BW = typical system bandwidth, normally 0.6 to 1.0 times the data rate (hertz). If the PDJ is still larger than desired, continue increasing the value of C_{AC}. Note that to maintain stability, it is important to keep the low-frequency cutoff well below the corner frequency associated with the postamplifier.

PDJ can also be present due to insufficient highfrequency bandwidth (Figure 2-5). If the amplifiers are not fast enough to allow for complete transitions during single-bit patterns, or if the amplifier does not allow adequate settling time, high-frequency PDJ can result.

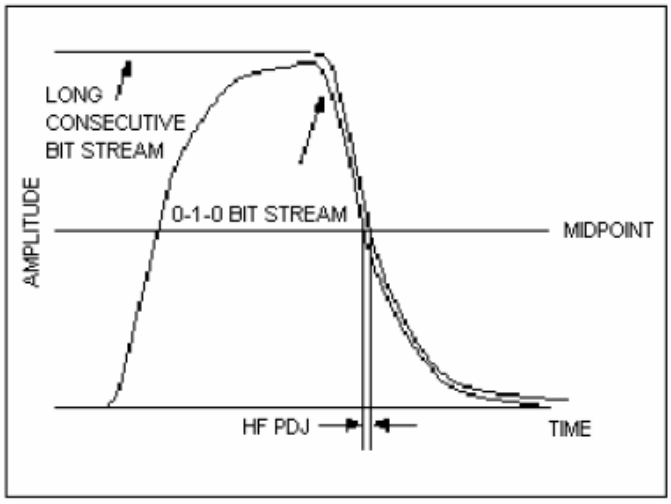


Fig. 2-5 Pattern-dependent jitter due to low-frequency cutoff

2.4.1.4. Pulse-Width Distortion(PWD)

Finally, PWD occurs when the midpoint crossing of a 0–1 transition and a 1–0 transition do not occur at the same level (Figure 2-6). DC offsets and nonsymmetrical rising and falling edge speeds both contribute to PWD. For a 1–0 bit stream, calculate PWD as follows:

PWD = [(width of wider pulse) –(width of narrower pulse)] / 2

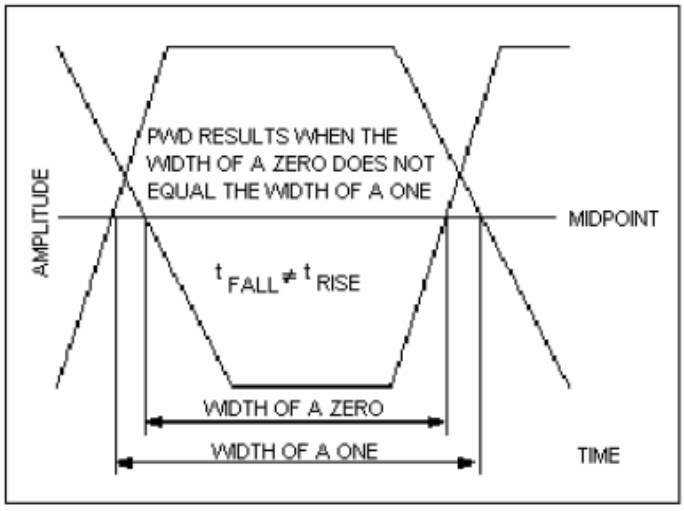


Fig. 2-6 Pulse-width distortion

2.4.2. Sensitivity

2.4.2.1. Introduction

In optical communication systems, sensitivity is a measure of how weak an input signal can get before the bit-error ratio (BER) exceeds some specified number. The standards body governing the application sets this specified BER. For example, SONET specifies that the BER must be 10^{-10} or better. Gigabit Ethernet and Fibre Channel specifications require a BER of 10^{-12} or better. This BER is the foundation for determining a receiver's sensitivity.

In the design of an optical receiver, such as a small form factor optical transceiver module, it is vital that the module be capable of converting and shaping the optical signal while meeting or surpassing the maximum BER. Ultimately, the influence of noise on the signal will determine the sensitivity of the system. The portion of the receiver that contributes the most noise is the optical-to-electrical conversion provided by the photodetector and the transimpedance amplifier (TIA). More often than not, designers will use a combination of simple estimation and "rules of thumb" to predict performance and select components. This discussion presents a reliable method for estimating the receiver's sensitivity. [15]

2.4.2.2. Traditional Analysis

Sensitivity can be expressed as average power (P_{AVG}) in dBm or as optical modulation amplitude (OMA) in Wpp. Each gives a figure of merit for the receiver. The sensitivity is the minimum OMA or PAVG at which the maximum (worst tolerable) BER can be maintained. Optical transmission system designers use sensitivity to determine the maximum distance or link margin available in their

system. Expressing the sensitivity in terms of average power is useful, because the average power of a laser is more easily measured than peak-to-peak power. Measuring the peak-to-peak power of a laser at high data rates requires expensive equipment that is error-prone due to the amount of operator intervention. Average optical power can be measured easily and reliably with a relatively inexpensive optical power meter.

Figure 2-7 shows a simple block diagram of the front end of an optical receiver. The dominant noise sources in this section are the linear components that provide the optical-to-electrical conversion, namely, the photodiode and the transimpedance amplifier.

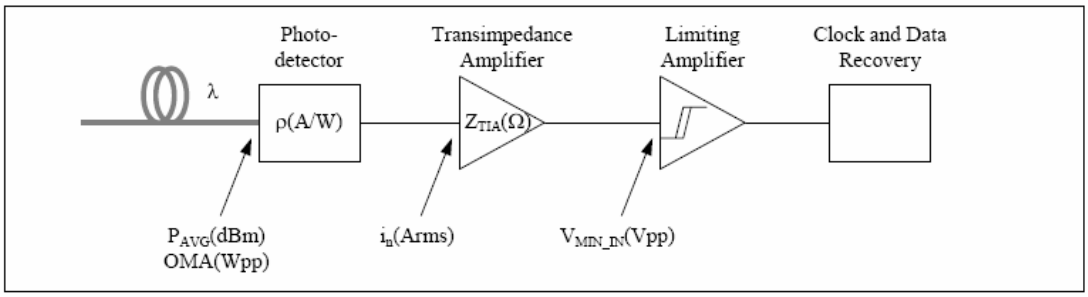


Fig. 2-7 Simplified block diagram of the major functional blocks in an optical receiver

Transimpedance amplifiers (TIAs) are used to amplify and convert the photodiode current into a voltage. Usually included within the data sheets for a TIA is an equation for calculating the receiver's sensitivity. The equation for calculating sensitivity is as follows:

$$Sensitivity = 10Log\left[\frac{i_n SNR(r_e+1)}{\rho(r_e-1)2}1000\right]dBm$$

This equation assumes that all of the noise in the system is due to the TIA. It also assumes that the limiting amp following the TIA has a decision threshold of zero. In

reality, the result given by this equation is rarely obtainable; however, it is useful in comparing the relative differences among TIAs. The noise of the TIA, i_n, is expressed as "input referred noise" in RMS current (A_{RMS}) or "input referred noise density" in ($A_{RMS}/\sqrt{}$Hz). This is the inherent noise of the amplifier. Input referred noise is directly proportional to the value of the photodiode capacitance and bandwidth of the TIA. The noise density has removed the bandwidth component so that it can be scaled to the specific bandwidth used in the application. For this discussion, input referred noise will be used. The process in estimating the minimum peak-topeak swing of the optical signal begins with the choice of the maximum BER. This determines the signal-to-noise ratio (SNR). Next, the RMS input referred noise, i_n, of the TIA and the responsivity (ρ) of the photodetector must be found from the vendor's data sheets. These are related by:

$$OMA_{MIN} = \frac{i_n SNR}{\rho} \tag{1}$$

The dimensions are as follows:

$$OMA_{M\,IN} = \frac{(Arms)(pp/rms)}{(A/W)} = Wpp$$

This relationship assumes that the noise is Gaussian. Therefore, the erred population of a logic one and a logic zero of a nonreturn-to-zero (NRZ) data stream can be estimated.

In Figure 2-8, the relationship of the normal probability to the erred population (1-cummmulative probability) is shown as the region at which the occurrence rate of the erred bits equals the desired BER limit. The right side of Figure 2 shows the region overlapping where the BER = 10^{-12}. The logic-one and logic-zero levels are each seven standard deviations (±7σ) away from a theoretical decision point shown at midscale.

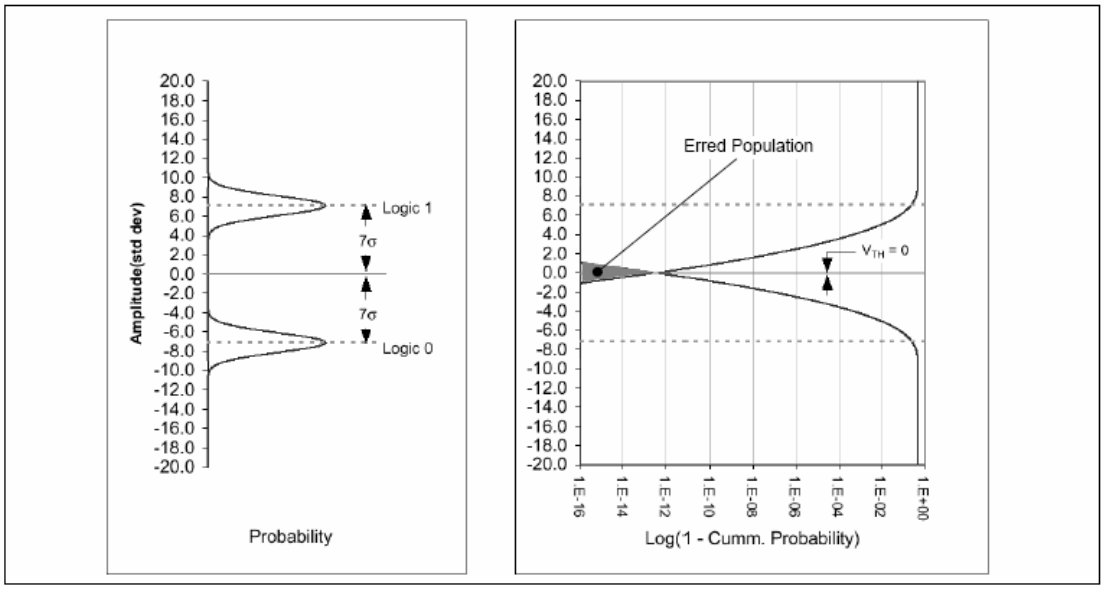


Fig. 2-8 Noise distribution, as viewed linearly at the left, exhibits the familiar Gaussian distribution. Plotting the log(1-cummulative probability), at the right, reveals where the erred population is near the desired BER. With the decision threshold (VTH) of 0V, a BER<10-12 is theoretically possible.

Example A

Consider this example: If the desired BER = 10^{-12}, the input referred noise i_n = 400nArms, and the responsivity ρ = 0.5A/W, what is the minimum optical modulation amplitude (OMA) and the minimum average optical power (P_{AVG})? For a BER of 10^{-12}, the required SNR is 14.1

Applying Equation 1,

$$OMA_{MIN} = \frac{i_n SNR}{\rho} = \frac{(400nA)(14.1)}{(0.5A/W)} = 11.3\mu Wpp$$

Furthermore, if the extinction ratio, (P_1 / P_0), is 8 (9dB), the average optical power is as follows:

$$P_{AVG} = \frac{OMA(r_e + 1)}{2(r_e - 1)} = \frac{(11.3\mu W)(8+1)}{2(8-1)} = 7.25\mu W = -21.4dBm$$

The traditional analysis leads us to conclude that the optical sensitivity is

-21.4dBm. In reality, it is not. Although there might be many factors contributing to this, one glaring element has been omitted. In Figure 2-8, it is obvious that the vertical distance between a logic one and a logic zero is 0V. This means that the vertical eye is closed completely at the desired BER. The notion that a logic one and a logic zero can be detected with a threshold of 0V is preposterous!

2.4.2.3. Corrected Analysis

Once again, refer back to Figure 2-7. Note that the TIA is followed by a limiting amplifier. It has an input operating range over which the peak-to-peak signal at its input is amplified and clipped to maintain a constant amplitude. This range has a minimum signal swing below which the amplifier output is not held constant. This is the sensitivity of the limiting amplifier. To maintain the desired BER, the nonerred population must not cross into the sensitivity region of the limiting amplifier. In other words, the eye presented to the limiting amplifier must open by at least an amount equal to the limiting amplifier's sensitivity.

Figure 2-9 illustrates the impact of having a decision threshold greater than zero. Taking this into account, Equation 1 becomes

$$OMA_{MIN} = \frac{\left[i_n SNR + (\frac{V_{TH}}{Z_{TIA}}) \right]}{\rho} \qquad (2)$$

where VTH is the sensitivity of the limiting amplifier and ZTIA is the transimpedance gain of the TIA.

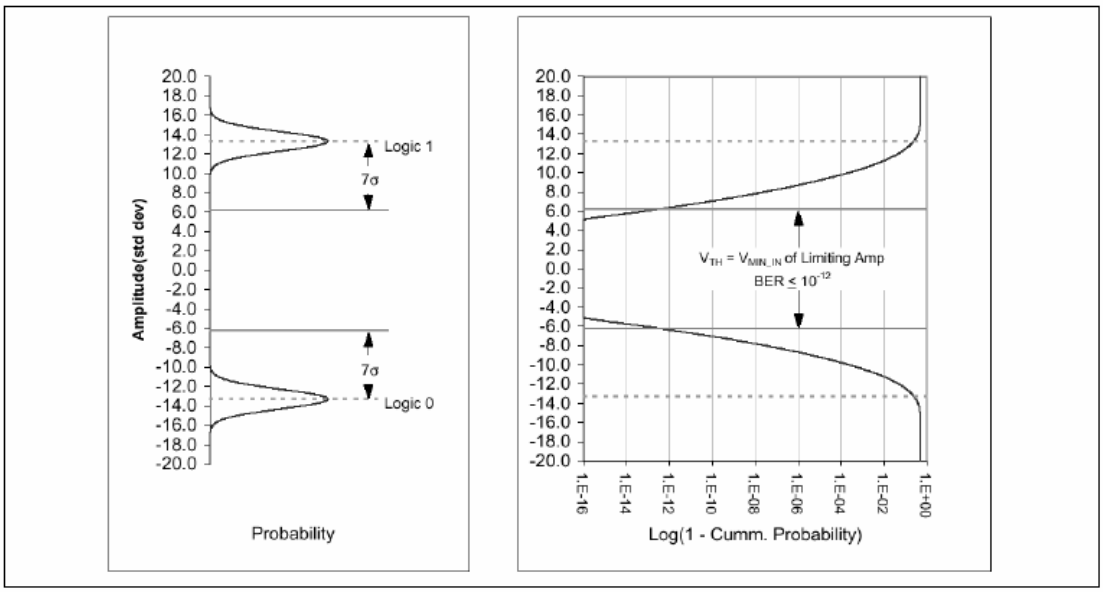


Fig. 2-9 When the decision threshold is non-zero, the sensitivity of the next stage of the receiver must be considered. To achieve the desired BER for the receiver, the minimum input amplitude must be increased by an amount equal to the minimum input of the limiting amp, VMIN_IN.

Example B

Now consider Example A but with a decision threshold VTH = 10mVpp and ZTIA = 2k:. Applying Equation 2,

$$OMA_{MIN} = \frac{\left[i_n SNR + (\frac{V_{TH}}{Z_{TIA}}) \right]}{\rho} = \frac{\left[(400nA)(14.1) + (10mV / 2K\Omega) \right]}{(0.5A/W)} = 21.3\mu W$$

The average optical power is

$$P_{AVG} = \frac{OMA(r_e + 1)}{2(r_e - 1)} = \frac{(21.3\mu W)(8+1)}{2(8-1)} = 13.7\mu W = -18.6dBm$$

The difference between Examples A and B is nearly 3dB. This is a 2x change in optical sensitivity and cannot be ignored! This could be why many designers have adopted a rule of thumb to require an additional 3dB of sensitivity in the optical receiver section.

2.4.2.4. Conclusion

It is clear that the traditional analysis approach is oversimplified. With little effort, a more accurate estimate of optical sensitivity can be made. So, relying on a vendor specification meant for comparison-shopping or someone's rule of thumb should sound the alarm. By applying the technique presented in this discussion, it is easy to estimate and predict more realistic optical receiver sensitivity. In the end, there won't be any big surprises when you test your first parts!

Chapter 3

Differential Active Feedback TIA

3.1. Introduction

This chapter describes a differential active feedback transimpedance amplifier. Differential architecture have been proposed to improve sensitivity at the input of transimpedance amplifiers. Compared to conventional single ended architecture [16] [17], this work reject common mode substrate and power supply noise, Due to differential dc coupled, transimpedance sensing photodiode current directly , and achieved twice output swing. In comparison, an ac coupled photodiode current sensing configuration in [18] [19], suffers from the difficulty of realizing on chip capacitors and photodiode bias fluctuation with ambient light variation.

To achieve the required bandwidth, transimpedance amplifier incorporates two high-speed techniques: inductive peaking, and active negative feedback. In conventional resistive feedback techniques, the strength of the feedback directly

trades with the open loop gain. Alternatively, the unilateral feedback in an active stage avoids this trade off.. It achieves better gain bandwidth product.

3.2. Differential Active Feedback TIA Architecture

The conceptual architecture of the TIA is depicted in Figure 3-1. It consists of a regulated cascade (RGC) input stage(M1, M2), a core amplifier stage(TIA), an active negative feedback stage(Mf1, Mf2), and the output buffer stage(B1). The photo diode is connected to node Vin+ and node Vin- for dc–coupled differential photodiode current sensing.

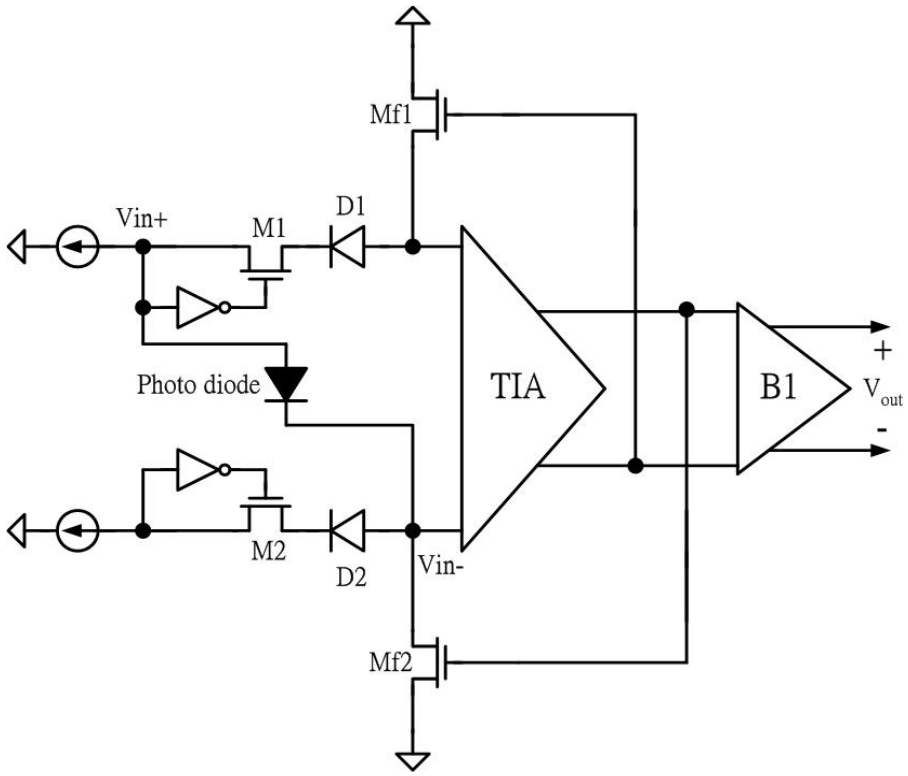


Fig. 3-1 Differential active feedback TIA architecture

It is well known that tradeoffs between bandwidth and photodiode capacitance are inevitable in a conventional common-source TIA. Even though common-gate (CG) input configuration helps a TIA to relax the tradeoffs, it cannot yet effectively isolate

the large photodiode capacitance from the bandwidth determination because of small of the input transistor. Meanwhile, the RGC input configuration reported in [22]–[24] enhances the input significantly due to the local feedback mechanism, so that the RGC TIA can achieve better isolation of the photodiode capacitance than other configurations. Namely, the RGC circuit enables the TIA to avoid the need of a dummy input capacitor due to the virtual-ground input impedance, thus facilitating the realization of an optical interconnect system in a single chip. Also, the virtual ground input reduces the noise coupling from through the photodiode into the TIA so much that there is no longer a need to balance it out. Furthermore, proper sizing of the local feedback stage reduces the dominant high-frequency noise contribution of the RGC TIA without deteriorating the stability [24].

In conventional resistive feedback techniques, the strength of the feedback directly trades with the open loop gain. Alternatively, the unilateral feedback in an active stage avoids this trade off.. In Figure 3-1, the differential pair M3-M4 provides active feedback. It can be proved that active feedback results in a gain-bandwidth product of roughtly $f_T/(C_1BW)$ [25].

In high speed circuit design, the output stage must deliver large currents to the 50Ω loads. Therefore, large transistor size is necessary to achieve such a large current. Unfortunately, the large size will produce substantial parasitic capacitance that will decrease the signal bandwidth. To alleviate the load to preceding gain stages, a f_T-doubler [26] circuit shown in Fig.3-2 is adopted. Compare f_T-doubler with a simple differential stage, one can get the idea that with the same drive capability f_T-doubler has smaller input capacitance.

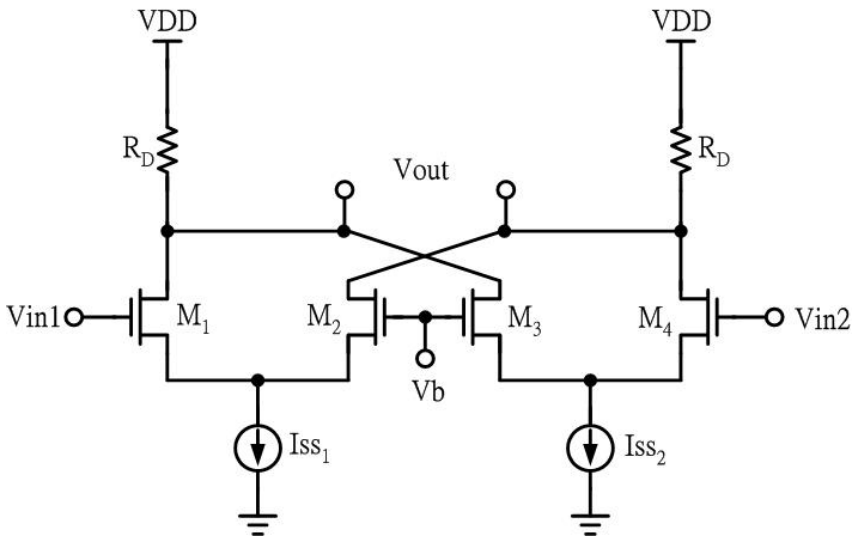


Fig. 3-2 f_T doubler schematic

3.3. 3-D Transformer

To achieve both wide band and high gain design goals, 3-D symmetric transformers [27] are utilized for bandwidth enhancement. Compared to using two asymmetric or one planar symmetric counterparts in a fully differential architecture, it greatly saves chip area. The distributed and lumped circuit models of the 3-D transformer are illustrated in Figure.3-3 (a) and Figure.3-3(b) respectively. Here $R_{s1,i}$ and $R_{s2,i}$ represent the distributed resistance of L_1 and L_2 on metal layer i. $C_{1,jk}$ and $C_{2,jk}$ denotes the parasitic capacitance of L_1 and L_2 between metal layer j(= 6, 5, 4, 3, 2), k(= 4, 3, 2) and substrate k(= 0). The outer radius of loops on adjacent layers are offset by the metal width. Thus the parasitic capacitance between adjacent metal layers can be eliminated. Besides, $C_{1,jk}$ and $C_{2,\mathrm{jk}}$ are reduced by increasing the distance between metal plate, so as to have better self resonant frequency (f_{sr}). Furthermore, by means of the interleaving architecture in a relatively small area, the effective inductance in each branch is increased by enhancing the mutual coupling of the

transformer (*M*), including the magnetic coupling on the same layer (M_1) and adjacent layer (M_2 −M_9). Thus the total wired length of the 3-D transformer can be reduced to be configured in a small area. And the parasitic capacitance to substrate can be minimized.

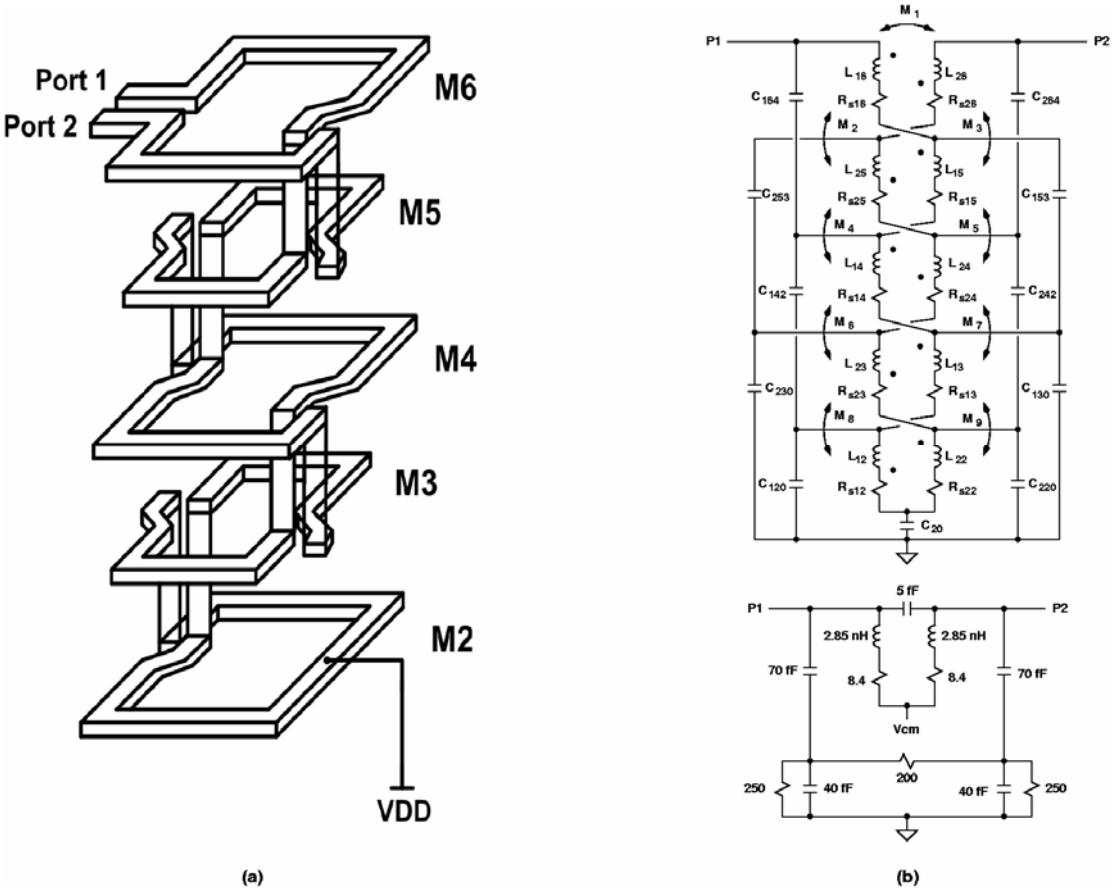


Fig. 3-3 (a) 3-D symmetric transformer (b)Distributd and lumped circuit model

Figure.3-4 illustrates the cross sectional view of planar transformer and its electrical potential distribution. The equivalent parasitic capacitance can be derived as

$$C_{eq1} = \sum_{k=0}^{n-1} C_{mk}\left[(2n-2k)\frac{1}{2n}\right]^2 + \sum_{k=1}^{n} C_{mk}\left[(2n-2k+1)\frac{1}{2n}\right]^2 \qquad (3\text{-}1)$$

where C_{mk} denotes the metal to substrate parasitic capacitance.

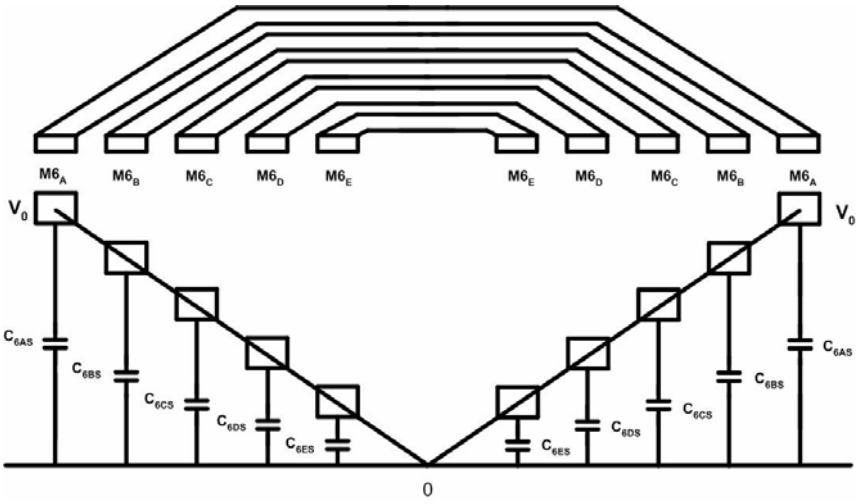


Fig. 3-4 Cross section view of planar transformer and potential distribution.

Figure.3-5 Cross sectional view of 3-D symmetric transformer and its electrical potential distribution. The equivalent parasitic capacitance can be derived as

$$C_{eq2} = \sum_{i=1}^{2(n-2)} C_{mtmi}\left(\frac{1}{n}\right)^2 + \sum_{j=n-1}^{n+2} C_{mtsj}\left(\frac{j}{2}\right)^2 \qquad (3\text{-}2)$$

where Cmtm and Cmts respectively denotes the metal to metal and metal to substrate capacitance. C_{eq2} is proven to be smaller than C_{eq1} due to smaller potential difference between conducting plate.

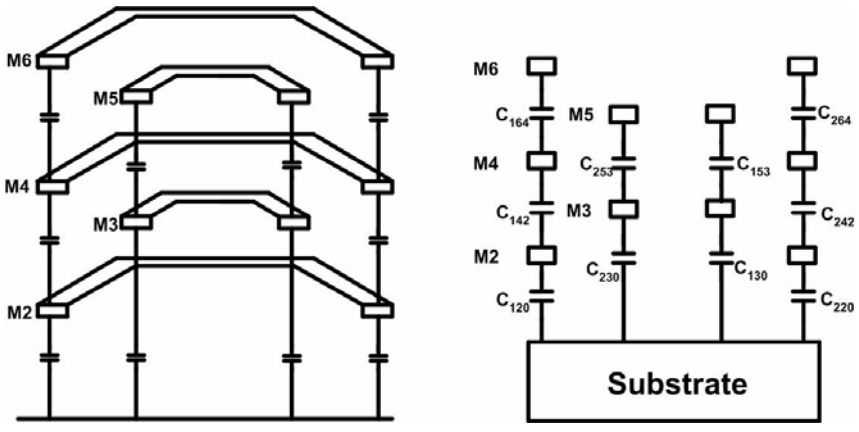
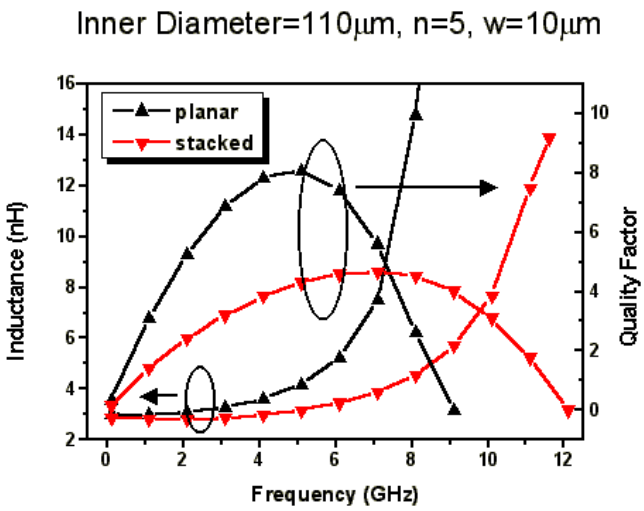


Fig. 3-5 Cross section view of 3-D symmetric transformer and potential distribution.

Figure.3-6 illustrates the simulated performance of the proposed 3-D transformer and a conventional planar counterpart. For an inductor pair with inductance of 2.85 nH in each branch, 5 turns, metal width = 10 μm, metal spacing = 1.5 μm, and inner diameter of 110 μm, the chip area of 3-D transformer is only 47% compared to that of its planar counterparts. Also it manifests higher self resonant frequency (12 GHz v.s. 9 GHz). Though its quality factor may become worse for the sake of using lower metal layer, this is not an issue for bandwidth enhancement applications.



	planar	stack
Inductance (nH)	2.98	2.86
Resonate Frequency	9 GHz	12.1 GHz
Q_{max}	8	4.7
$\frac{A_{stack}}{A_{planar}}$	-	47%

Fig. 3-6 Planar v.s. 3-D symmetric transformer performance comparison.

3.4. Circuit Design

To alleviate bandwidth degradation caused by the parasitic capacitance of photo detector and IC package, a regulated cascode (RGC) topology is adopted as the input stage. The TIA architecture is in differential configuration with active-feedback for better sensitivity and higher common mode noise immunity.

The detailed circuit schematic of the TIA is as shown in Figure.3-7, which is

composed of a regulated cascode (RGC) input stage (M1, M2) followed by a common source gain stage (M5,M7) with active feedback stage(Mf1,Mf2). For bias photo diode, the operating voltage is 3.3V under 0.18 m CMOS technology. The diode (MD1, MD2) is for voltage level shift, preventing M1 M2 operating in high voltage level. The Source followers (MS1, MS2) is for suitable voltage level shift and avoid loading effect.

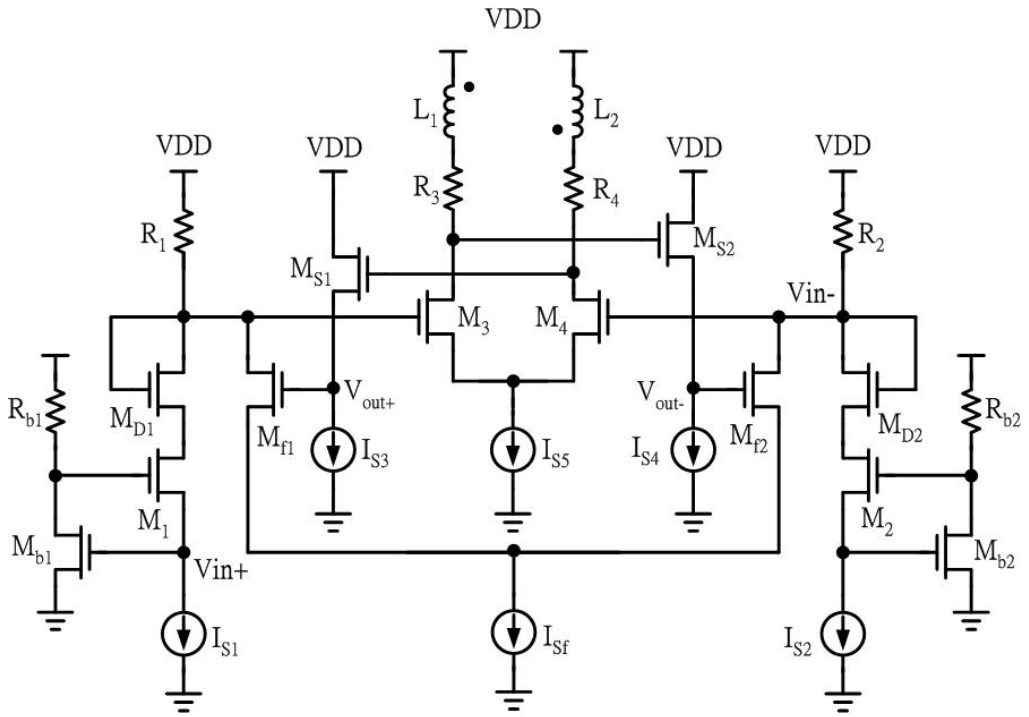


Fig. 3-7 Differential active feedback TIA schematic

Node Vin+ and Vin- are connect to both side of photo diode, for dc–coupled differential photodiode current sensing. Due to the current of photodiode is from TIA circuit itself, the current of photodiode will be limited by TIA circuit. The maxim current is describe as equation 3-3:

$$I_{\max} = \frac{VDD - Vpd_{bias} - Vin_{+}}{R_2} \tag{3-3}$$

The closed loop conversion gain of the TIA can be approximated by

$$T_z = \frac{-g_{m3}R_3R_1}{1+g_{mf}(g_{m3}R_3R_1)} \tag{3-4}$$

Before analysis the frequency response, we assume the TIA circuit compose of common gate stage Ai and shunt feedback stage Az show in Figure. 3-8. Because the bandwidth of common gate stage Ai is enhance by RGC input stage, the dominate pole occurs in shunt feedback stage Az. We analysis the shunt feedback stage show in Figure. 3-9 and assume A(s) is one pole core amplifier.

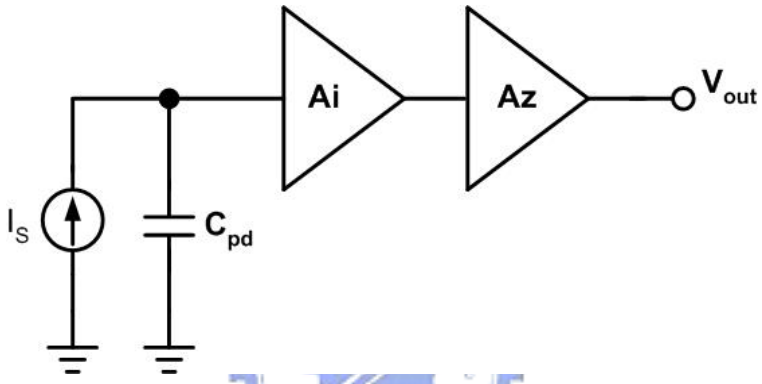


Fig. 3-8 Simple architecture of TIA

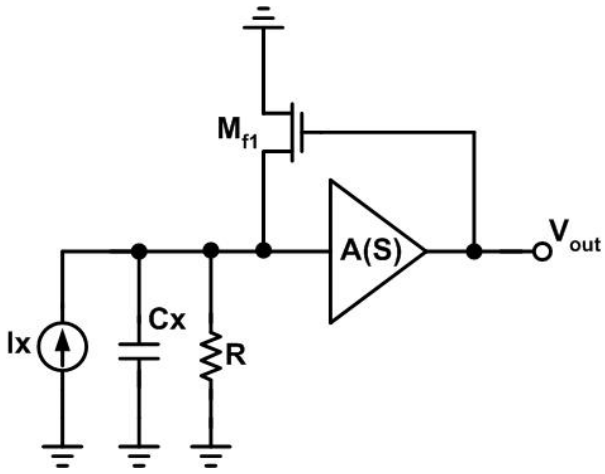


Fig. 3-9 Shunt feedback stage

$$\frac{V_o}{I_X} = \frac{A(S)\times R}{1 + A(S)\times R\times gm_{f1} + SRC_x}$$

$$A(S) = \frac{A_0}{1+\frac{S}{\omega_0}}$$

$$\frac{V_o}{I_X} = \frac{\frac{A_0\omega_0}{C_x}}{S^2 + S(\frac{RC_x + \frac{1}{\omega_0}}{RC_x/\omega_0}) + \frac{(1+A_0\times R\times gm_{f1})}{RC_x/\omega_0}}$$

$$\omega_n{}^2 = \frac{(1+A_0 Rgm_{f1})\omega_0}{RC_x}$$

$$\delta = \frac{1}{2}\times\frac{1}{\sqrt{(1+A_0\times R\times gm_{f1})\omega_0 RC_x}}$$

For critically damped-response,

$$\delta = \frac{\sqrt{2}}{2}$$

$$\Rightarrow \omega_0 = \frac{2A_0 gm_{f1}}{C_x}$$

$$\Rightarrow \omega_n = \sqrt{2}\frac{A_0 gm_{f1}}{C_x}$$

According upon analysis, we can design our circuit correctly.

3.4.1. Inductive Peaking Technique

With the advent of monolithic inductors, inductive peaking techniques have become feasible in integrated circuits. Take Fig. 3-10 as an example to understand the principle of shunt-peaking. The amplifier is just a standard common source configuration with the addition of the inductance.

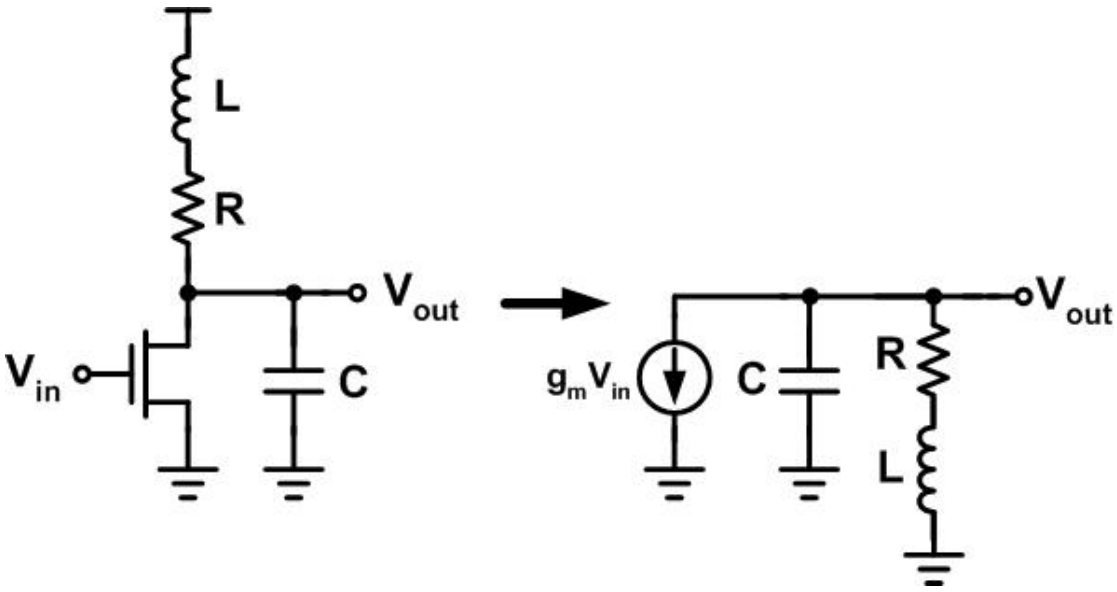


Fig. 3-10 A shunt-peaked amplifier and its small-signal model

One can think about why adding an inductor this way will give us a bandwidth extension intuitively. First, with an input step waveform, the inductor delays current flow through the branch containing the resistor, which makes more current available for charging the capacitor and thus reduces the risetime. It follows that a faster risetime implies a greater bandwidth. Second, one knows that the gain of an amplifier with purely resistively load will degrade at high frequency because the load capacitor's impedance diminishes. The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency, which helps offset the decreasing impedance of the capacitance. So, the total impedance can remain roughly constant over a broader frequency range just like that the bandwidth is enhanced.

Formally, the impedance of the RLC network may be written as

$$Z(s) = (sL + R) \left\| \frac{1}{sC} = \frac{R[s(L/R)+1]}{s^2 LC + sRC + 1} \right. \tag{3-5}$$

Compared with a simple common source amplifier without inductive peaking, the amplifier in Fig. 3-10 enhances the bandwidth by transforming the frequency response from that of a single pole to one with two poles and a zero. The frequency response can be characterized by the ratio of the RC and L/R time constants, that is

$$m = \frac{RC}{L/R} \tag{3-6}$$

Then, the relation between bandwidth of an amplifier with and without inductive peaking can be derived as

$$\frac{\omega_2}{\omega_1} = \sqrt{\left(-\frac{m^2}{2} + m + 1\right) + \sqrt{\left(-\frac{m^2}{2} + m + 1\right)^2 + m^2}} \tag{3-7}$$

Where ω_1, ω_2 are the bandwidths without and with inductive peaking individually. Under different design requirements, there is a range of useful inductance values as listed in Table 3-1 [28]. However, since monolithic inductors suffer from parasitic capacitance and a low quality factor, inductive peaking improves the speed to a lesser extent.

In 10Gbps design, an inductor smaller than 3nH is accepted from the resonate-frequency viewpoint. Under maximally flat condition, the load resistance should smaller than 250Ω if total capacitance at output node is assumed 100fF. It means that the bias current may be larger than 3.6mA.

Conditions	$m=R^2C/L$	Bandwidth Improvement	Overshoot
Max. Bandwidth	1.41	85%	20%
Maximally Flat	2.41	72%	-
Best Group Delay	3.1	60%	-
No Shunt Peaking	∞	-	-

Table 3-1 Shunt-peaking summary

3.4.2. Active Feedback Technique

This work introduce active negative feedback as a means of improving the GBW of amplifiers. Illustrated in Figure 3-11, such an arrangement employs a transconductance stage G_{mf} to return a fraction of output to the input of Gm1. Unlike the conventional resistor-feedback amplifier, active feedback does not resistively load the transimpedance stage. The transfer function of the overall amplifier is given by

$$\frac{V_{out}}{I_S} = \frac{A_{zo}\omega_n^{\,2}}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \tag{3-8}$$

Where

$$A_{zo} = \frac{G_{m1}R_1R_2}{1 + G_{m1}G_{mf}R_1R_2} \tag{3-9}$$

$$\zeta = \frac{1}{2}\frac{R_1C_1 + R_2C_2}{\sqrt{R_1R_2C_1C_2(1 + G_{mf}G_{m1}R_1R_2)}} \tag{3-10}$$

$$\omega_n^{\,2} = \frac{1 + G_{mf}G_{m1}R_1R_2}{R_1R_2C_1C_2} \tag{3-11}$$

For a maximally-flat Butterworth response, $\zeta=\sqrt{2}/2$ and the -3dB bandwidth, $\omega_{-3dB}= 2\pi f_{-3dB}=\omega_n/(2\pi)$. Multiplying (3-9) by (3-11), we thus have

$$A_{zo}\omega_{-3dB}{}^{2} = \frac{G_{m1}}{C_1 C_2} \tag{3-12}$$

$$A_{zo}\omega_{-3dB} = \frac{G_{m1}}{C_1 C_2}\frac{1}{\omega_{-3dB}} \tag{3-13}$$

Since Gm1/C1≈2πfT, (3-13) can be rewritten as

$$A_{zo}\omega_{-3dB} = f_T \frac{1}{C_1 f_{-3dB}}$$

This result reveals that active feedback increases the GBW beyond the technology f_T by a factor equal to $1/(C_1 f_{-3dB})$.

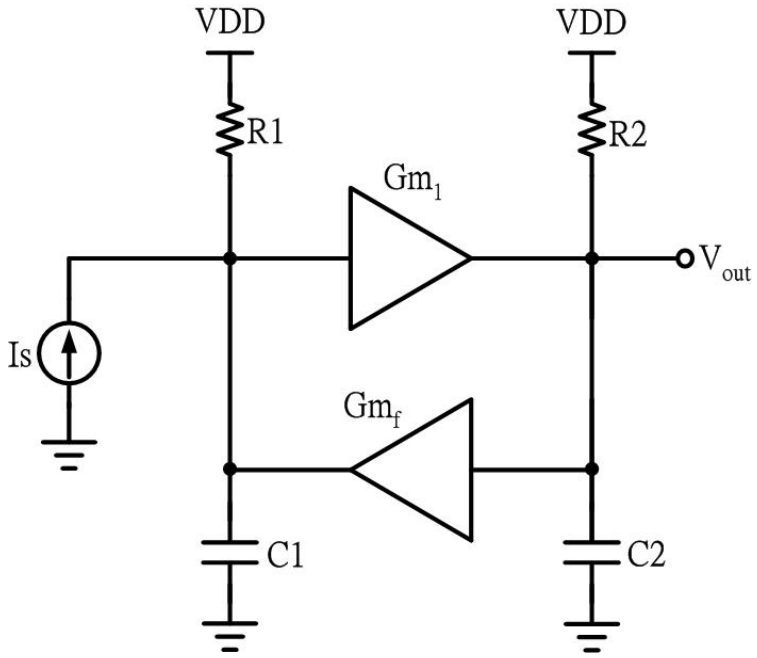


Fig. 3-11 Active feedback architecture

3.4.3. Noise Analysis

As introduced before, the accepted minimum input current is relative to the noise contributed by the TIA itself. Fig. 3-12 illustrates the TIA schematic with noise

source.

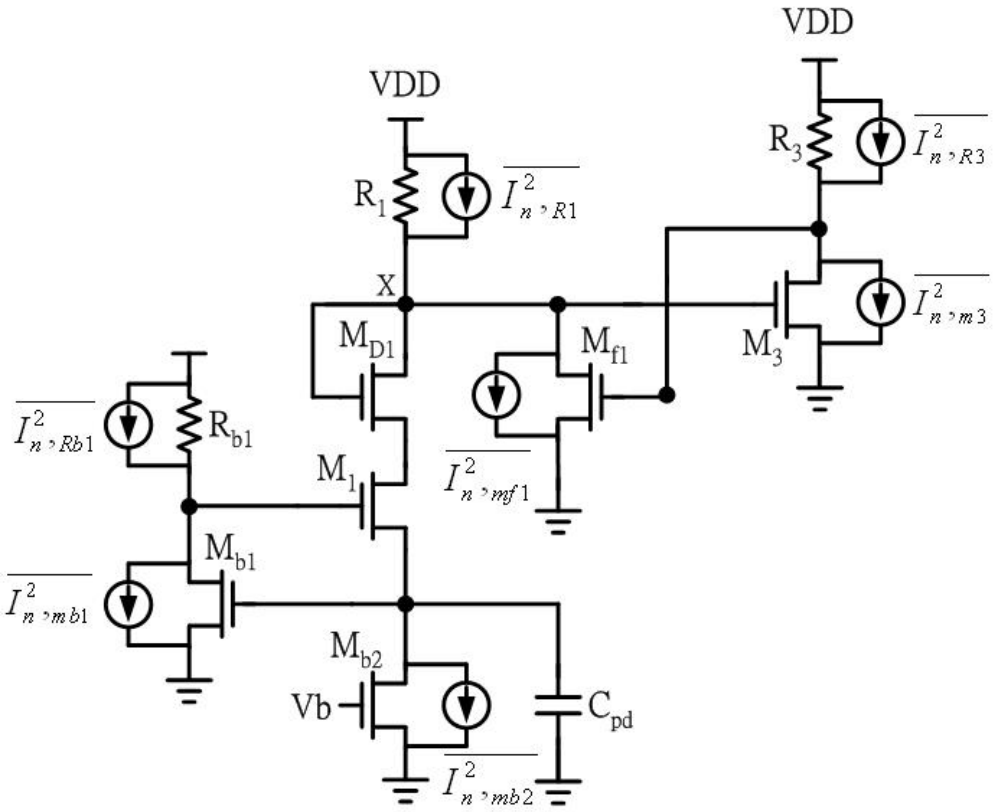


Fig. 3-12 Schematic diagram of TIA including noise source

The input referred noise current spectral density can be described as

$$\overline{I_{in}^2} = \overline{I_{n,mb2}^2} + \overline{I_{n,R1}^2} + \overline{I_{n,mf1}^2} + \frac{\overline{I_{n,m3}^2} + \overline{I_{n,R3}^2}}{g_{m3}^2}\left(\omega^2 C_X^2 + \frac{1}{R_1^2} + g_{mf}^2\right) + \frac{\overline{I_{n,mb1}^2} + \overline{I_{n,Rb1}^2}}{g_{mb1}^2}\left(\omega^2 C_{in}^2\right)$$

$$= \frac{4kT}{R_1} + 4kT\gamma\left(g_{mf} + g_{mb2}\right) + \frac{4kT(\gamma g_{m3} + 1/R_3)}{g_{m3}^2}\left(\omega^2 C_X^2 + \frac{1}{R_1^2} + g_{mf}^2\right) + \frac{4kT(\gamma g_{mb1} + 1/R_{b1})}{g_{mb1}^2}\left(\omega^2 C_{in}^2\right)$$

Where Cin denotes the total capacitance at input node.

Although the proposed transimpedance amplifier with regulated cascode input stage and shunt-feedback to the second stage overcomes the trade-off among gain, bandwidth, and noise as described in section 3.2, the price paid is that the input noise increases anyway especially at high frequency. To alleviate the last term above

equation, the transconductance of m_{b1} should be as large as possible.

3.5. Experimental Results

With Oepic-P5030A photo detctor, whose responsivity is 1 A/W, the input referred noise current (IN) of TIA is 1.2μArms. The input sensitivity of the TIA is derived from its input referred noise current (IN). As

$$Sensitivity \approx 10\log\left[\frac{14.1I_N(r_e+1)}{2\rho(r_e+1)}1000\right]dBm$$

where ρ is the responsivity of photo detector, and re is the extinction ratio. The corresponding sensitivity is approximately -20 dBm.

Figure.3-13 illustrate the measured frequency response, the -3dB bandwidth is 2.5GHz. Figure.3-14 illustrate the measured output noise spectrum, the input referred noise current can be derived from

$$i_{n,in-rms} = \frac{\sqrt{\frac{50}{BW}\int P_n df}}{Transimpedance_{50}}$$

where Pn is noise power, Bw is TIA -3dB bandwidth. Transimpedance50 is enacts transimpedance measured in 50-ohm systems.

Operating under a 3.3V supply, the power dissipation is 79 mW, among which 40 mW is consumed by output buffer. Figure.3-15, Figure.3-16, Figure.3-17, Figure.3-18, and Figure.3-19, Figure.3-20, Figure.3-21 illustrate the corresponding eye diagram at 1.25Gbps, 2.5Gbps, 3.125Gbps, 5Gbps, 6Gbps, 7Gbps, and 8Gbps with 231-1 PRBS input. Figure.3-22 illustrates the chip photo. Fabricated in a 0.18μ m CMOS technology, chip size is 738 μm × 1522 μm.

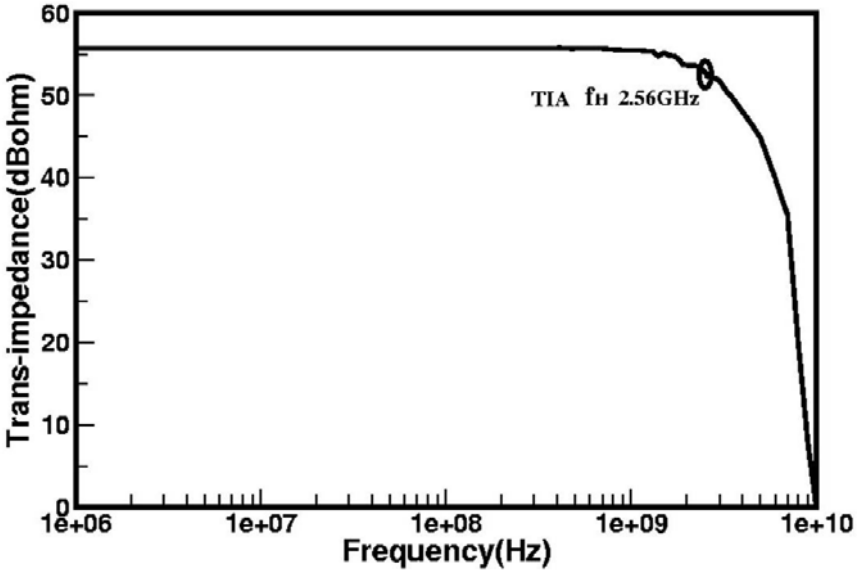


Fig. 3-13 Measured frequency response

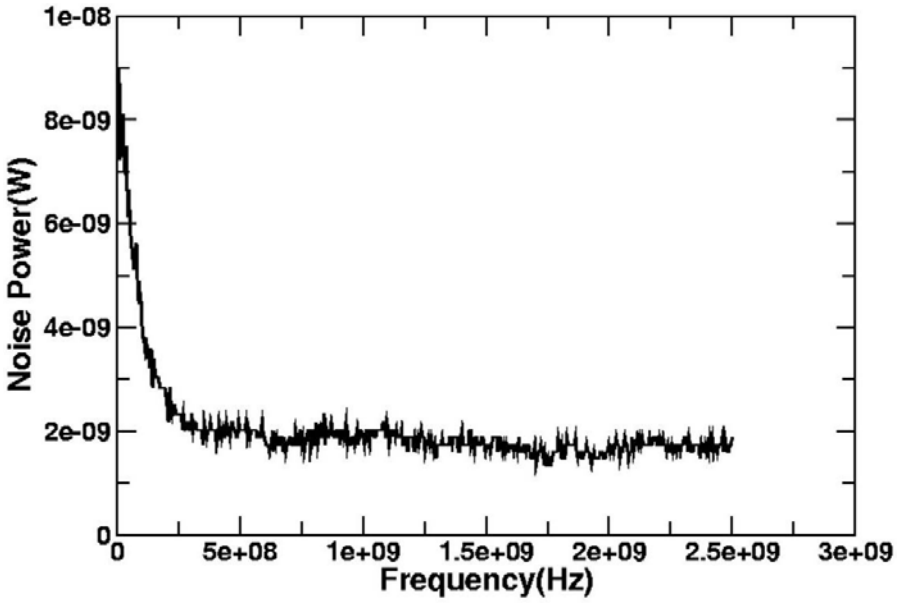


Fig. 3-14 Measured output noise spectrum

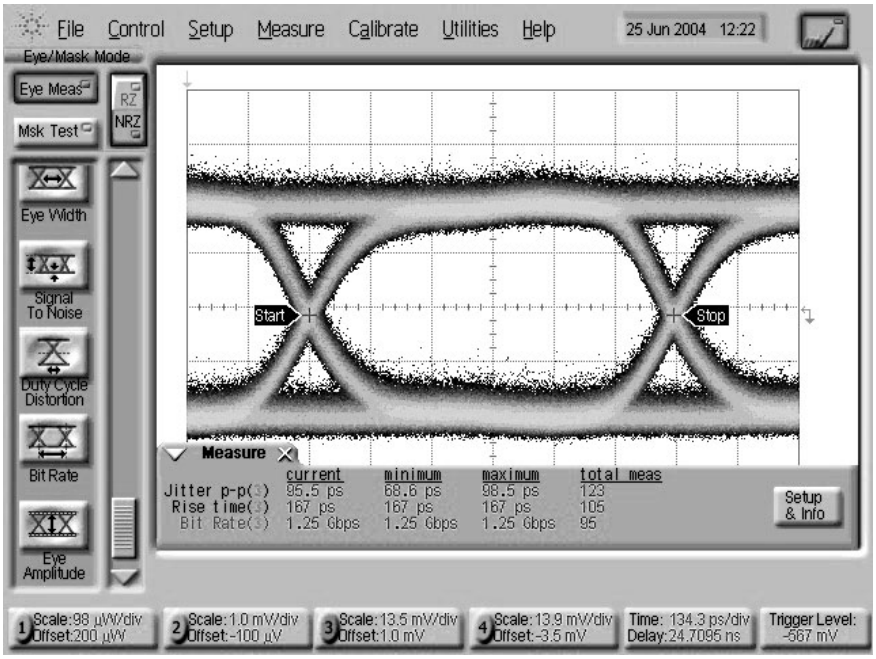


Fig. 3-15 1.25Gbps eye diagram with -7.4dBm input power (X axis: 134.3ps/div, Y axis: 13.5mV/div, Jitter(pp)=95.5ps).

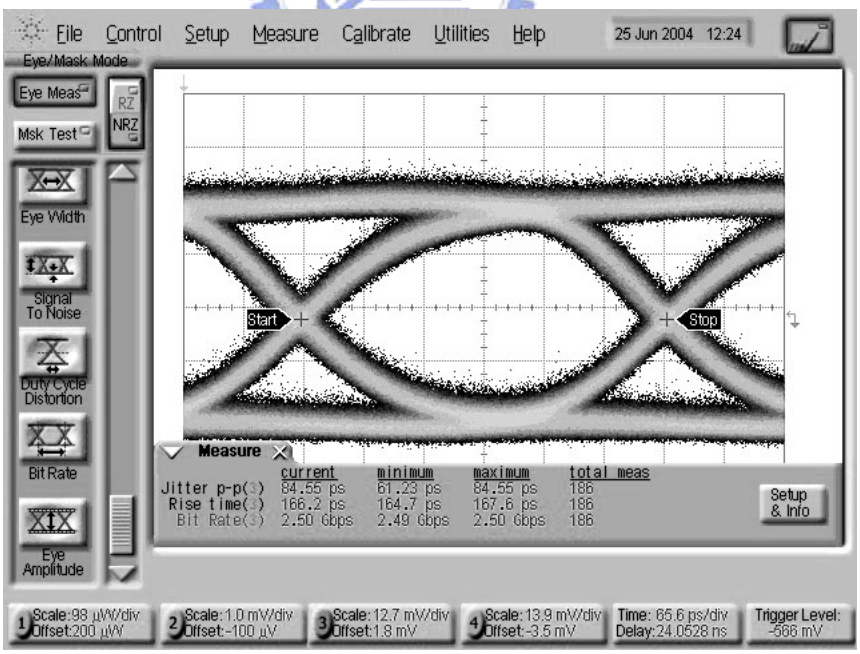


Fig. 3-16 2.5Gbps eye diagram with -7.4dBm input power (X axis: 65.6ps/div, Y axis: 12.7mV/div, Jitter(pp)=84.55ps).

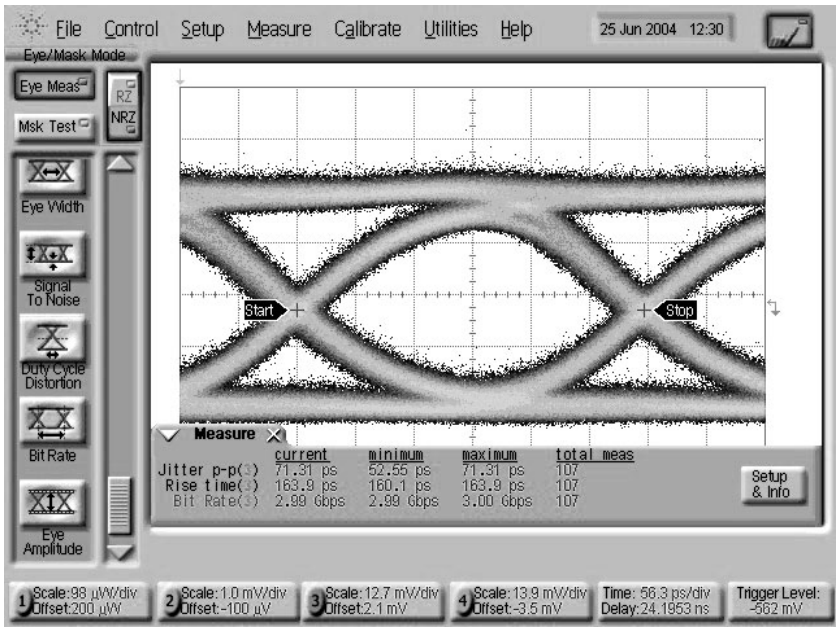


Fig. 3-17 3.125Gbps eye diagram with -7.4dBm input power (X axis: 56.3ps/div, Y axis: 12.7mV/div, Jitter(pp)=71.3ps).

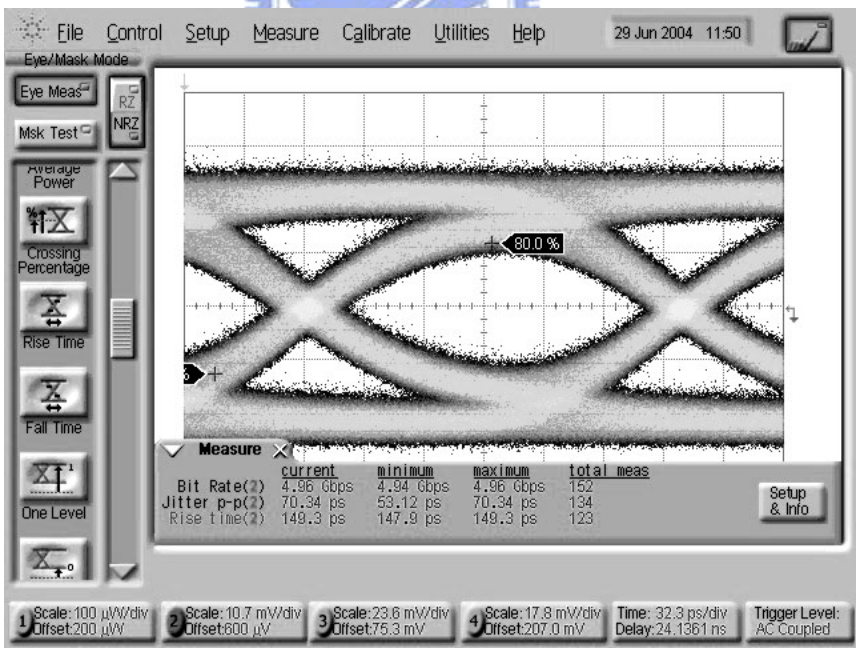


Fig. 3-18 5Gbps eye diagram with -7.4dBm input power (X axis: 32.3ps/div, Y axis: 10.7mV/div, Jitter(pp)=70.34ps).

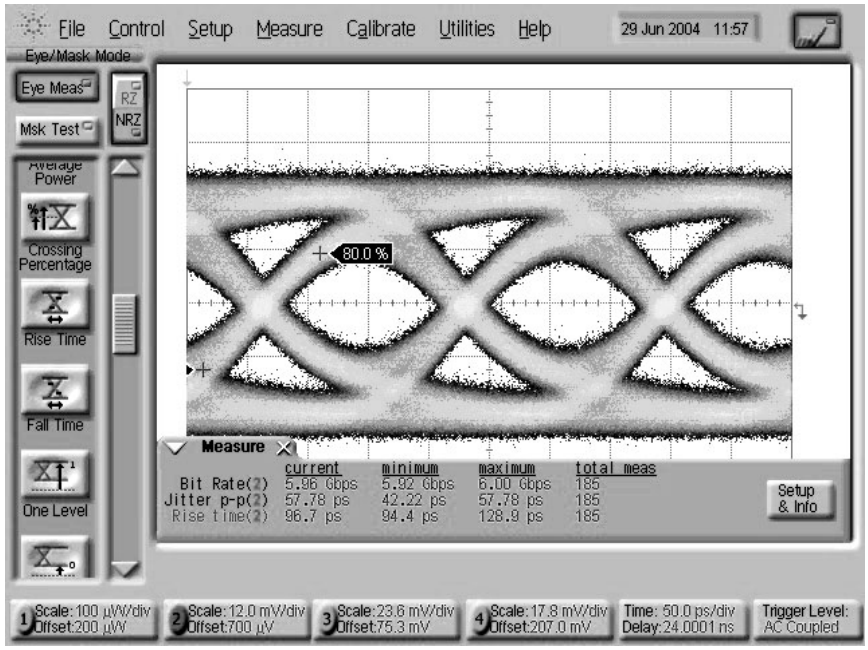


Fig. 3-19 6Gbps eye diagram with -7.4dBm input power (X axis: 50.0ps/div, Y axis: 12.0mV/div, Jitter(pp)=57.7ps).

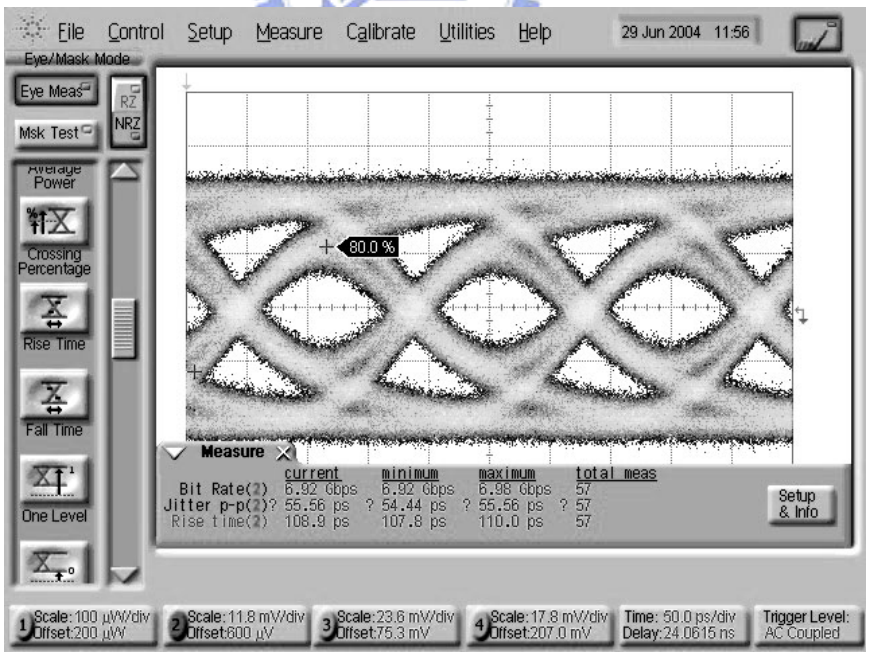


Fig. 3-20 7Gbps eye diagram with -7.4dBm input power (X axis: 50.0ps/div, Y axis: 11.8mV/div, Jitter(pp)=55.56ps).

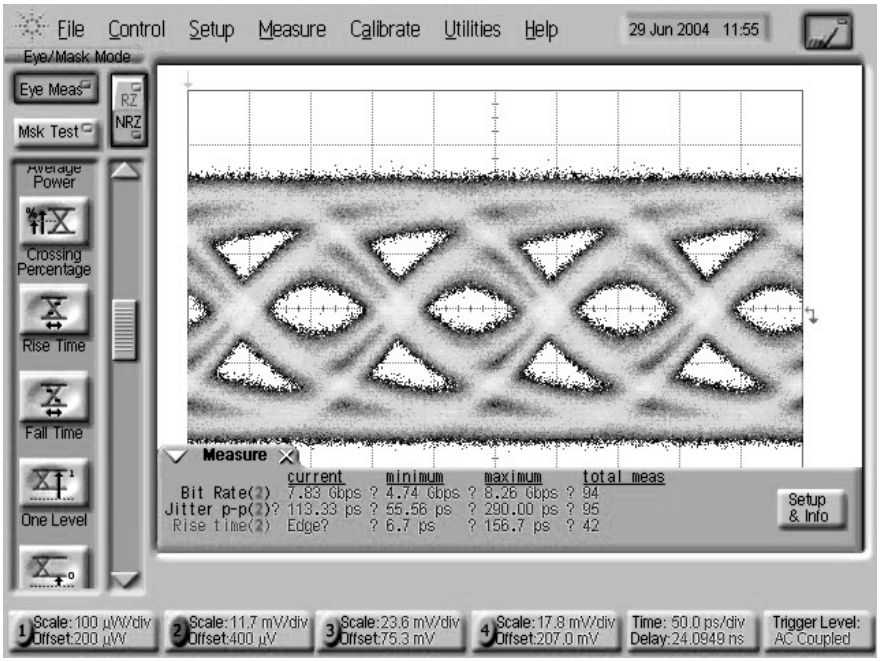


Fig. 3-21 8Gbps eye diagram with -7.4dBm input power (X axis: 50.0ps/div, Y axis: 11.7mV/div, Jitter(pp)=113.33ps).

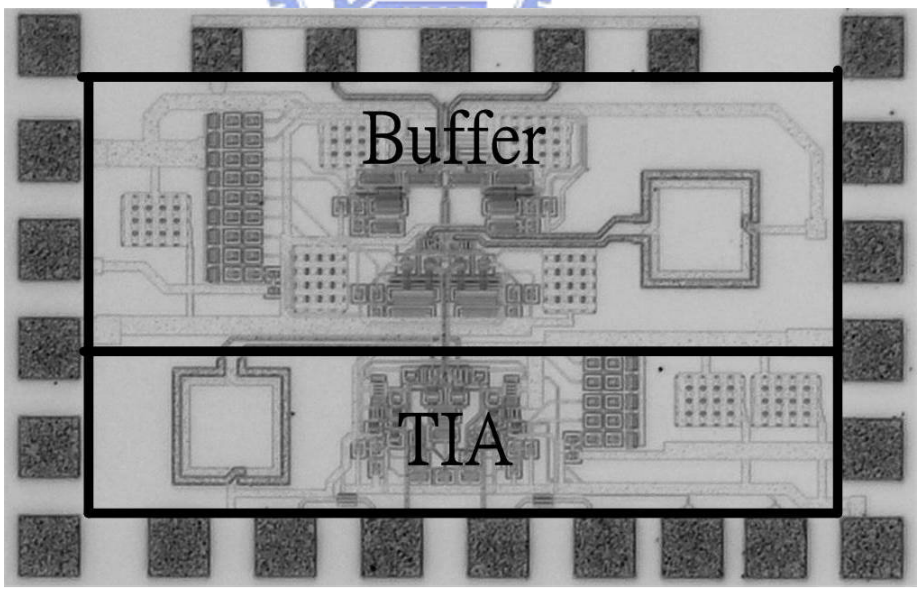
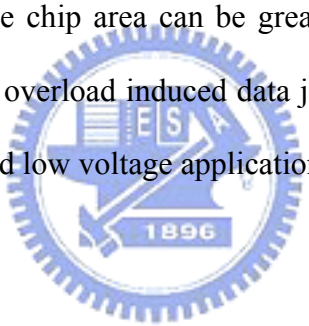


Fig. 3-22 TIA chip photograph.

3.6. Conclusion

This chapter describes the design of a fully-integrated 3.125 Gbps differential active feedback transimpedance in a generic 0.18 μ m CMOS technology. The TIA provides a conversion gain of 56 dBΩ and -3 dB bandwidth of about 2.5 GHz. A regulated cascode input stage is utilized to decouple the loading effect at the input node, and wide bandwidth is achieved by means of active feedback and inductive peaking. Instead of using bulky planar inductors or two asymmertric 3-D inductors, this paper proposes a novel fully symmetric 3-D transformer for inductive peaking in each differential pair. Thus the chip area can be greatly reduced. Moreover, an self limiting is built in to alleviate overload induced data jitter. The proposed architecture is suitable for both low cost and low voltage applications.



Chapter 4

90dBΩ, 10Gbps Optical Receiver Analog Front-End

4.1. Introduction

This chapter describes a 90 dB Ω, 10 Gbps fully integrated optical receiver that incorporates transimpedance amplifier, automatic gain control circuit, and limiting amplifier on a single chip. The single chip optical receiver provides several advantages over conventional multiple chips solutions [25] [30] [31]. First, tiny photo current generated from photo detector can be on-chip enlarged to a logic level to increase noise immunity and alleviate off-chip disturbances. Second, no interstage matching networks are required at the TIA output stage and LA input stage. Broad band matching networks in general induce gain loss and are power hungry. Third, gain

requirements of the transimpedance stage and post amplifier can be further optimized, and their bandwidth requirements are relatively relaxed.

4.2. Receiver Analog Front-end Architecture

The receiver architecture is shown in Figure.4-1 To achieve an input sensitivity of -13 *dBm* with a photo detector whose responsivity is 1 *A/W*, the transimpedance gain stage is designed to provide a conversion gain of 50 *dB*Ω and -3dB bandwidth of about 8*GHz*. The TIA bandwidth is chosen to compromise between noise performance and ISI, and the conversion gain is chosen to make its output swing overpass the input sensitivity of the post amplifier. The limiting amplifier is constructed of a voltage amplifier followed by a slicer. The over-drive voltage of the slicer is designed to be about 200 *mV* . Thus the voltage amplifier only needs to provide 25 *dB* conversion gain to fully switch the slicer. The small signal voltage amplifier is comprised of 3 stage gain cell in cascade and manifest -3 dB bandwidth of 14 GHz. The required GBW per stage is about 35 GHz . Bandwidth degradation caused by the slicer is negligible, and it's overall dominated by the transimpedance gain stage. Compared to a conventional stand alone limiting amplifier with identical gain stages, gain-bandwidth requirement of the gain cells herein are much relaxed. Thus no special bandwidth enhancement techniques are required in the front stage of voltage amplifier. The slicer stage in further provides about 15 dB conversion gain before driving the output buffer stage. In summary the overall receiver provides 90 *dB*Ω conversion gain and delivers 900 *mV* differential output swings to a 50 Ω output load. The DC offset of the gain chain is removed by on-chip low-pass filter and feedback amplifier, the low-end corner frequency is about 530 kHz.

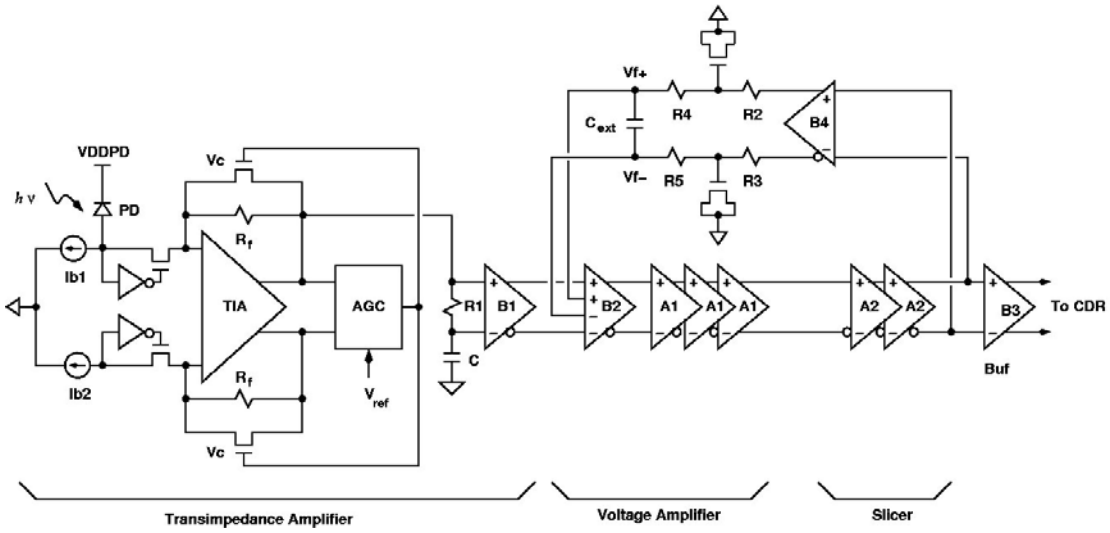


Fig. 4-1 Optical receiver analog front-end architecture.

4.3. 3-D Transformer

To achieve both wide band and high gain design goals, 3-D symmetric transformers [27] are utilized for bandwidth enhancement. Compared to using two asymmetric or one planar symmetric counterparts in a fully differential architecture, it greatly saves chip area. The distributed and lumped circuit models of the 3-D transformer are illustrated in Figure.4-2 (a) and Figure.4-2(b) respectively. Here $R_{s1,i}$ and $R_{s2,i}$ represent the distributed resistance of L_1 and L_2 on metal layer i. $C_{1,jk}$ and $C_{2,jk}$ denotes the parasitic capacitance of L_1 and L_2 between metal layer j(= 6, 5, 4, 3, 2), k(= 4, 3, 2) and substrate k(= 0). The outer radius of loops on adjacent layers are offset by the metal width. Thus the parasitic capacitance between adjacent metal layers can be eliminated. Besides, $C_{1,jk}$ and $C_{2,\mathrm{jk}}$ are reduced by increasing the distance between metal plate, so as to have better self resonant frequency (f_{sr}). Furthermore, by means of the interleaving architecture in a relatively small area, the effective inductance in each branch is increased by enhancing the mutual coupling of the transformer (M), including the magnetic coupling on the same layer (M_1) and adjacent

layer ($M_2 - M_9$). Thus the total wired length of the 3-D transformer can be reduced to be configured in a small area. And the parasitic capacitance to substrate can be minimized.

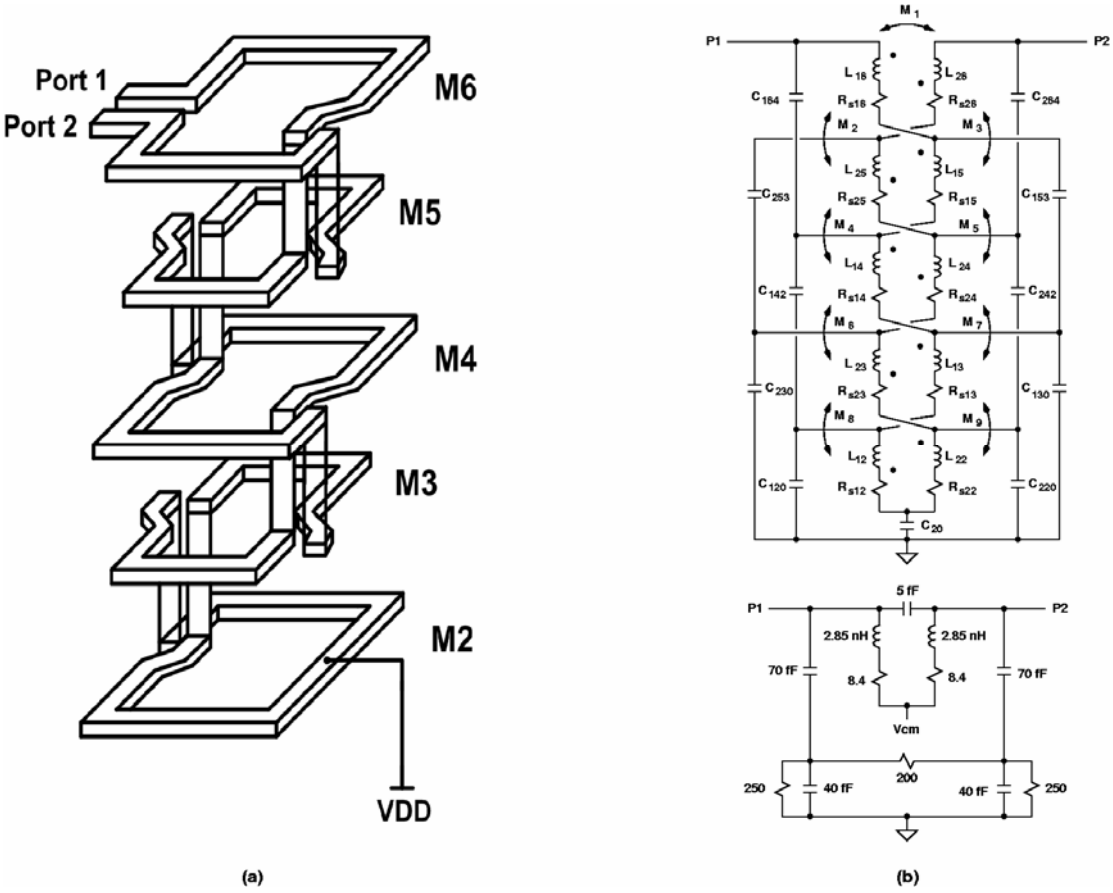


Fig. 4-2 (a) 3-D symmetric transformer (b)Distributd and lumped circuit model

Figure.4-3 illustrates the cross sectional view of planar transformer and its electrical potential distribution. The equivalent parasitic capacitance can be derived as

$$C_{eq1} = \sum_{k=0}^{n-1} C_{mk}\left[(2n-2k)\frac{1}{2n}\right]^2 + \sum_{k=1}^{n} C_{mk}\left[(2n-2k+1)\frac{1}{2n}\right]^2 \quad (1)$$

where C_{mk} denotes the metal to substrate parasitic capacitance.

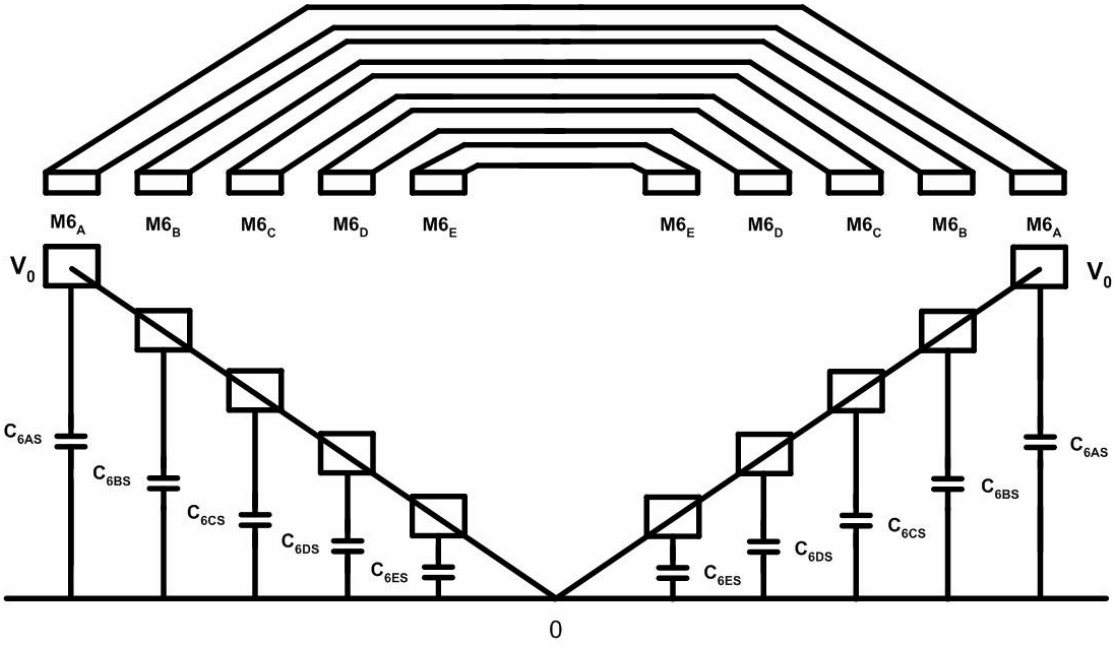


Fig. 4-3 Cross section view of planar transformer and potential distribution.

Figure.4-4 Cross sectional view of 3-D symmetric transformer and its electrical potential distribution. The equivalent parasitic capacitance can be derived as

$$C_{eq2} = \sum_{i=1}^{2(n-2)} C_{mtmi}\left(\frac{1}{n}\right)^2 + \sum_{j=n-1}^{n+2} C_{mtsj}\left(\frac{j}{2}\right)^2 \qquad (2)$$

where Cmtm and Cmts respectively denotes the metal to metal and metal to substrate capacitance. C_{eq2} is proven to be smaller than C_{eq1} due to smaller potential difference between conducting plate.

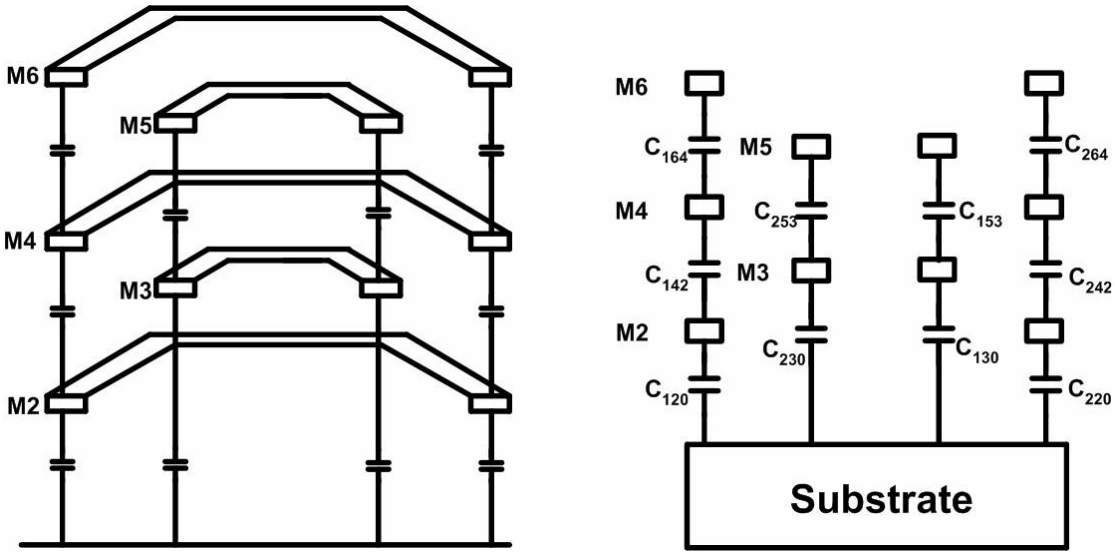
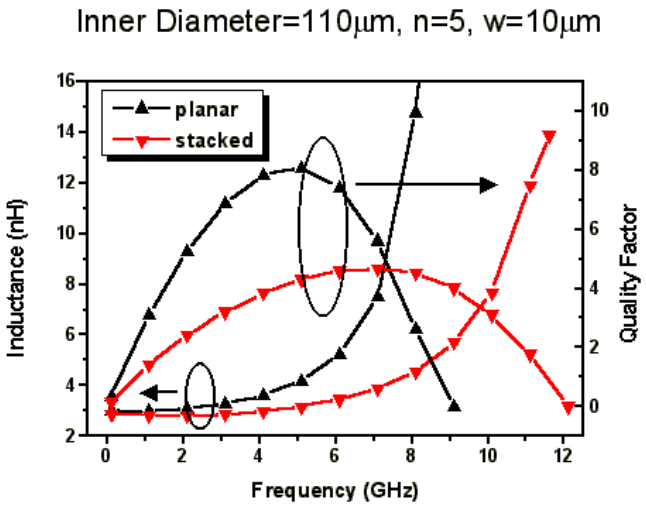


Fig. 4-4 Cross section view of 3-D symmetric transformer and potential distribution.

Figure.4-5 illustrates the simulated performance of the proposed 3-D transformer and a conventional planar counterpart. For an inductor pair with inductance of 2.85 nH in each branch, 5 turns, metal width = 10 μm, metal spacing = 1.5 μm, and inner diameter of 110 μm, the chip area of 3-D transformer is only 47% compared to that of its planar counterparts. Also it manifests higher self resonant frequency (12 GHz v.s. 9 GHz). Though its quality factor may become worse for the sake of using lower metal layer, this is not an issue for bandwidth enhancement applications.



	planar	stack
Inductance (nH)	2.98	2.86
Resonate Frequency	9 GHz	12.1 GHz
Q_{max}	8	4.7
$\frac{A_{stack}}{A_{planar}}$	-	47%

Fig. 4-5 Planar v.s. 3-D symmetric transformer performance comparison.

4.4. Circuit Design

To alleviate bandwidth degradation caused by the parasitic capacitance of photo detector and IC package, a regulated cascode (RGC) topology is adopted as the input stage. The TIA architecture is in pseudo differential configuration with shunt-feedback for better sensitivity and higher common mode noise immunity. Furthermore, an automatic gain control (AGC) loop is built in to avoid signal overload induced data jitter. The AGC is composed of an amplitude detector, a comparator, and an integrator. As TIA's output swing exceeds a preset voltage level Vref , the AGC will be activated. The comparator then generates a compensating current to charge or discharge the integrator, and the conversion gain of TIA can be adjusted by reducing the shunting resistance in the input stage.

4.4.1. Trans-impedance Amplifier Circuit Schematic

The detailed circuit schematic of the TIA is as shown in Figure.4-6(a), which is composed of a regulated cascode (RGC) input stage (M_1, M_2) followed by a common source gain stage (M_5,M_7) with shunt feedback. The right half circuit of TIA (M_3,M_4,M_6,M_8) is a replica for automatic gain control.

In the high input current state, the common source amplifiers in the second stage of TIA may be driven into deep triode region and results in overload induced data jitter. To mitigate this effects, the feedback resistors are adjusted by turning-on the shunting resistance of M_7. On the contrary, as the input current is below a predetermined threshold level, the shunting transistors are turned off for low noise operation.

4.4.2. Automatic Gain Control Circuit Schematic

The detailed circuit schematic of AGC is shown in Figure.4-6.(b), which is comprised of a peak-detector (M_1, M_2, C_1, C_2) followed by an OTA for amplitude comparison (M_3-M_8), a lossy integrator stage (M_{11}, R_1, C_3). and a low pass filter (R_2, C_4). The loop bandwidth of AGC is mainly determined by $1/R_2C_4$. Here M1 acts as the nonlinear rectifying element on the output signal of TIA. On the other hand, VTH derived from Vref at the replica of TIA core sets up the threshold voltage to turn on AGC. As the photo current exceeds a predetermined input level, the output node of TIA Vo will be driven to be lower than Vref . Thereafter, the OTA (M_3-M_{10}) would sense the voltage difference and generate the compensation current to charge or discharge the integrator, whose output V_{AGC} is utilized to control the turn on

resistance of M_7 and M_8 in the TIA core.

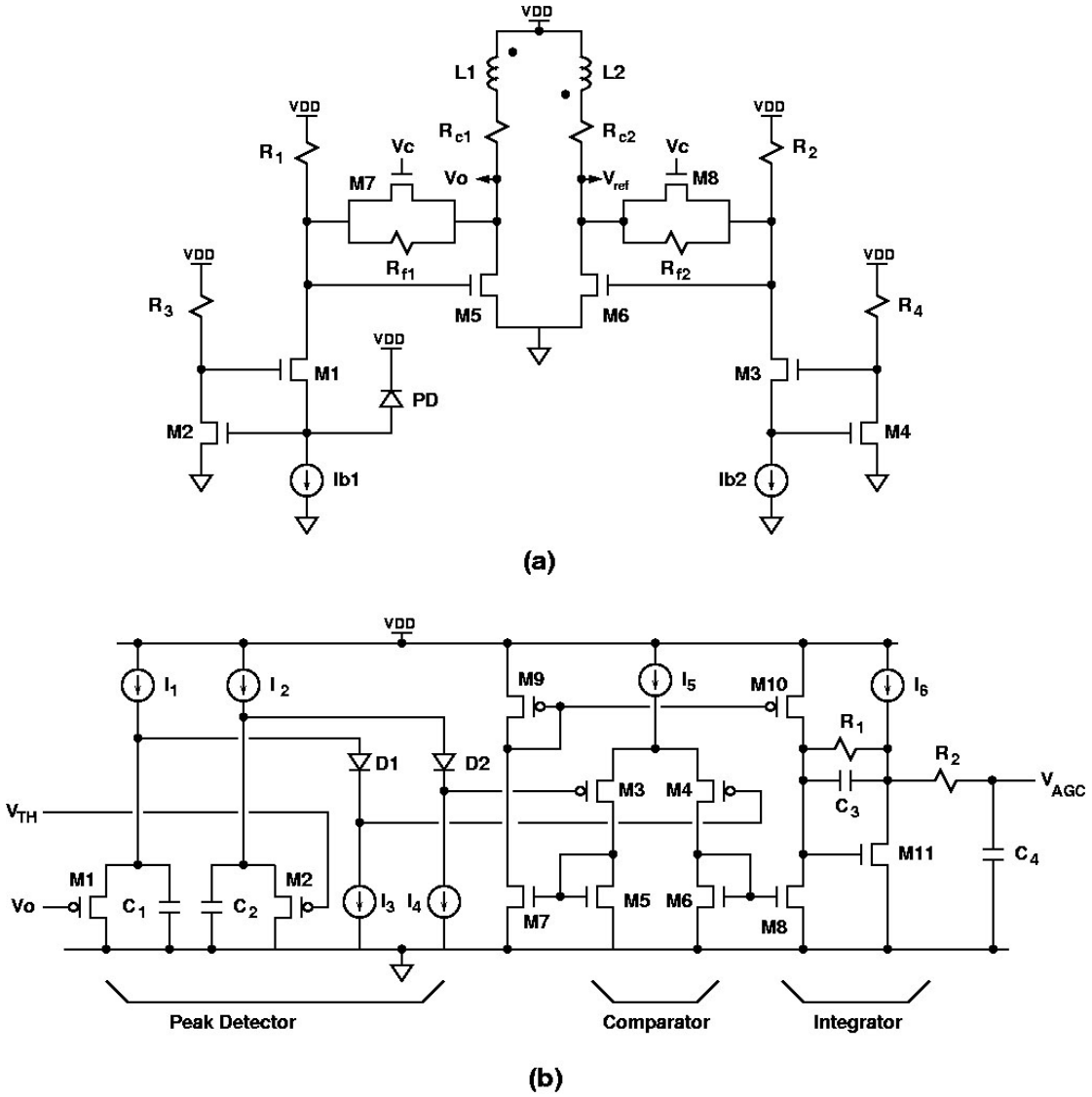


Fig. 4-6 (a) Transimpedance amplifier circuit schematic (b)Amplitude detector for AGC.

4.4.3. Limiting Amplifier Circuit Schematic

The core circuit of the voltage amplifier is shown in Figure.4-7(a), which is based on Cherry-Hooper circuit architecture with active feedback [25]. Compared to the prior art in [25], the GBW requirement in the front-stage of voltage amplifier is

relaxed and thus no peaking inductor is required to save area. Also, different from our previous work in [32] using resistive feedback, unilateral feedback avoids trade-off between feedback factor (close loop gain) and open loop gain (close loop BW) [25]. The gain cell of slicer is shown in Figure.4-7(b). Herein inductive peaking technique is utilized to accelerate voltage switch and balance rising and falling time at high voltage level.

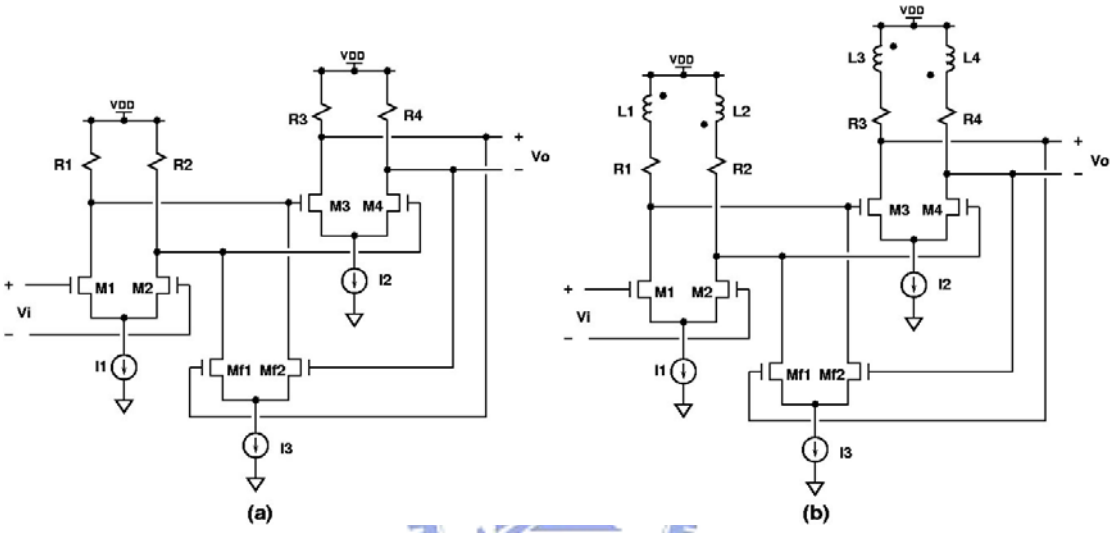


Fig. 4-7 :Gain Cell of (a) Voltage amplifier, and (b) Slicer.

4.5. Experimental Results

With Oepic-P5030A photo detctor, whose responsivity is 1 A/W, the sensitivity of the optical receiver AFE at 10 Gbps is about -13 dBm for BER less than 10^{-12}. The bit error rate performance at 10 Gbps is summarized in Figure.4-8. The tolerated power level is up to 0 dBm by the built in automatic gain control scheme. The input referred noise current (I_N) of the optical receiver is derived from its sensitivity performance. As

$$Sensitivity \approx 10\log\left[\frac{14.1I_N(r_e+1)}{2\rho(r_e+1)}1000\right]dBm$$

where ρ is the responsivity of photo detector, and re is the extinction ratio. The corresponding I_N is approximately 6.68 μA.

Figure.4-9 illustrate the corresponding 10 Gbps eye diagrams at sensitivity level with $2^{31}-1$ PRBS inputs and bit error rate less than 10^{-12}. Figure.4-10 illustrate the corresponding 10 Gbps eye diagrams at overload level of the same pattern length and bit error rate less than 10^{-12}. Operating under a 1.8V supply, the power dissipation is 199 mW, among which 35 mW is consumed by output buffer. Figure.4-11, Figure.4-12, Figure.4-13, and Figure.4-14 illustrate the corresponding eye diagram at 1.25Gbps, 5Gbps, 7Gbps, and 10Gbps with 2^{31}-1 PRBS input at a bit error rate of 10^{-12} . Figure.4-14 illustrates the chip photo. Fabricated in a 0.18μ m CMOS technology, chip size is 1300 μm × 1566 μm.

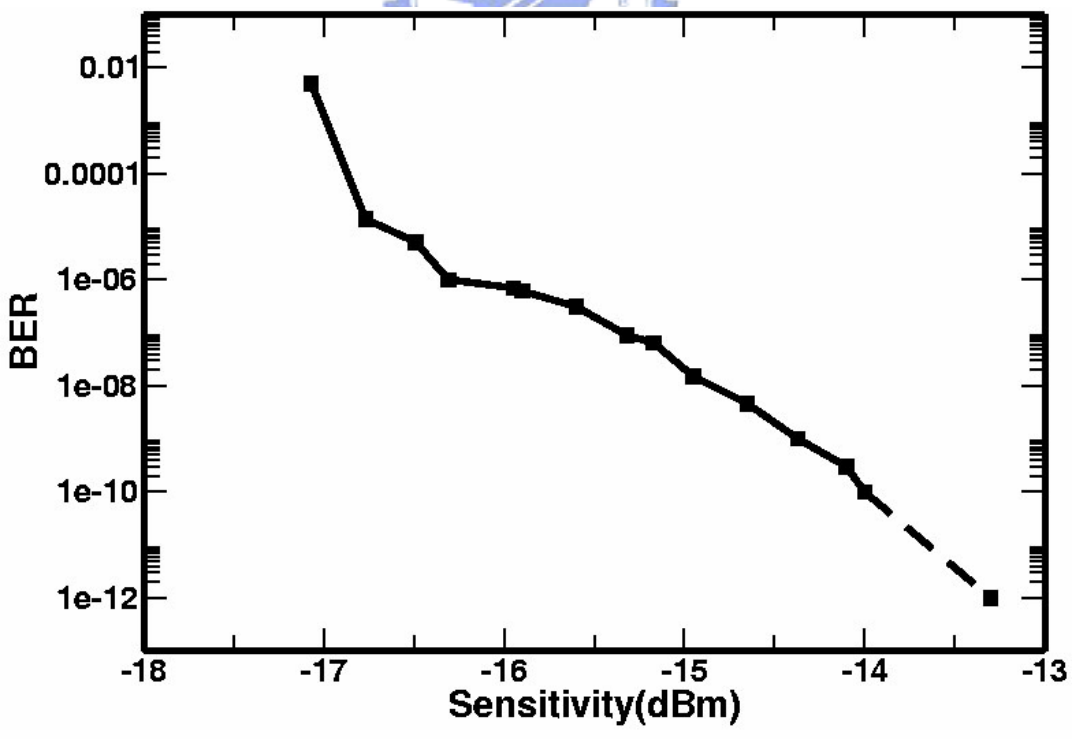


Fig. 4-8: 10Gbps bit error rate performance with 2^{31}-1 PRBS input.

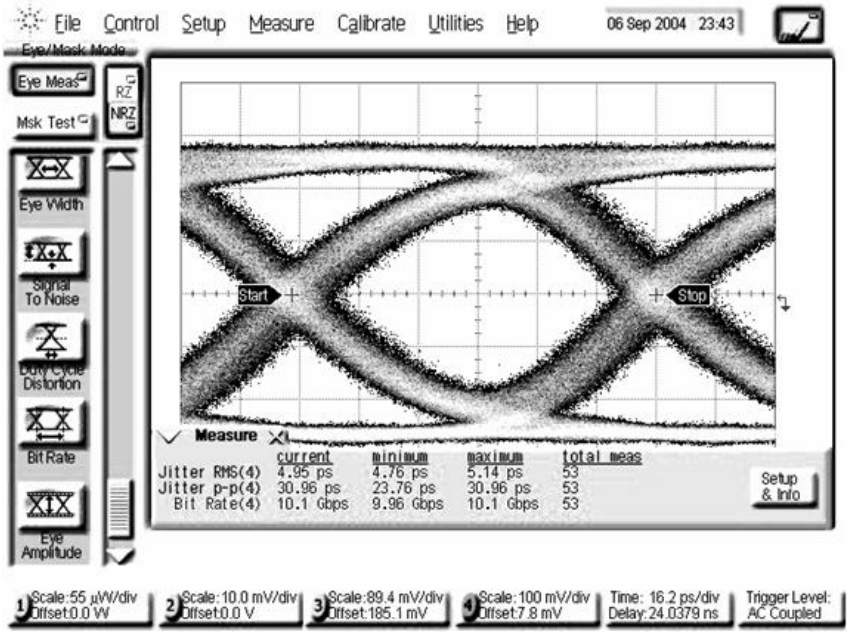


Fig. 4-9 : 10Gbps eye diagram @ -13dBm sensitivity level with 2^{31}-1 PRBS input.(X axis:16.2ps/div, Y axis: 100mV/div, Jitter(pp)=30.96ps)

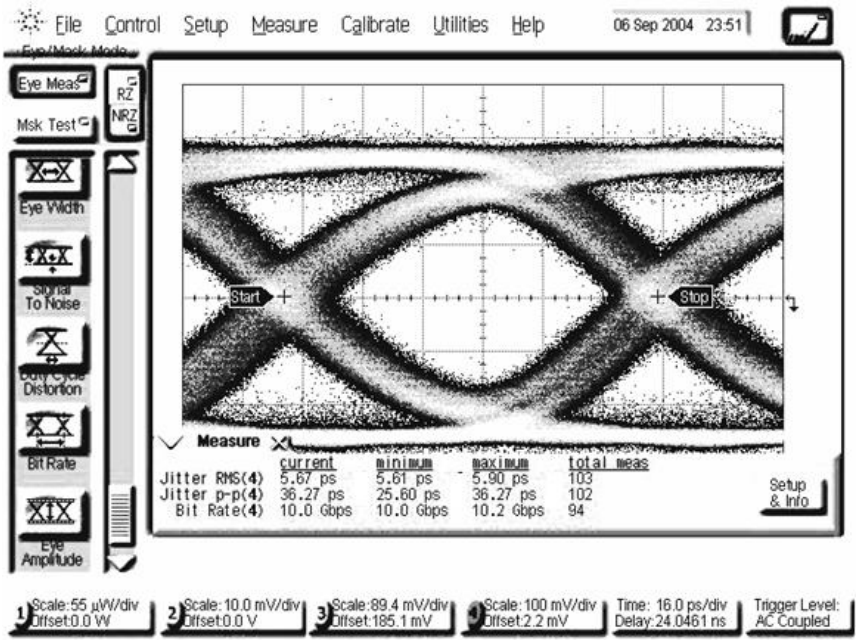


Fig. 4-10 : 10Gbps eye diagram @ 0dBm overload level with 2^{31}-1 PRBS input.(X axis:16ps/div, Y axis: 100mV/div, Jitter(pp)=36.27ps)

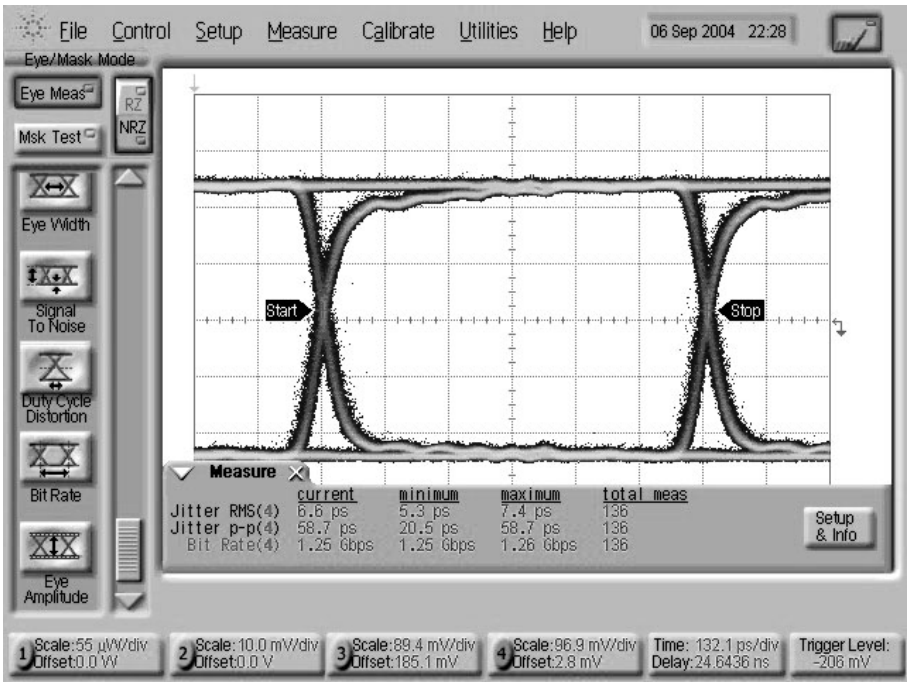


Fig. 4-11: 1.25Gbps eye diagram with 2^{31}-1 PRBS input. (X axis: 132.1ps/div, Y axis: 96.9mV/div, Jitter(pp)=58.7ps).

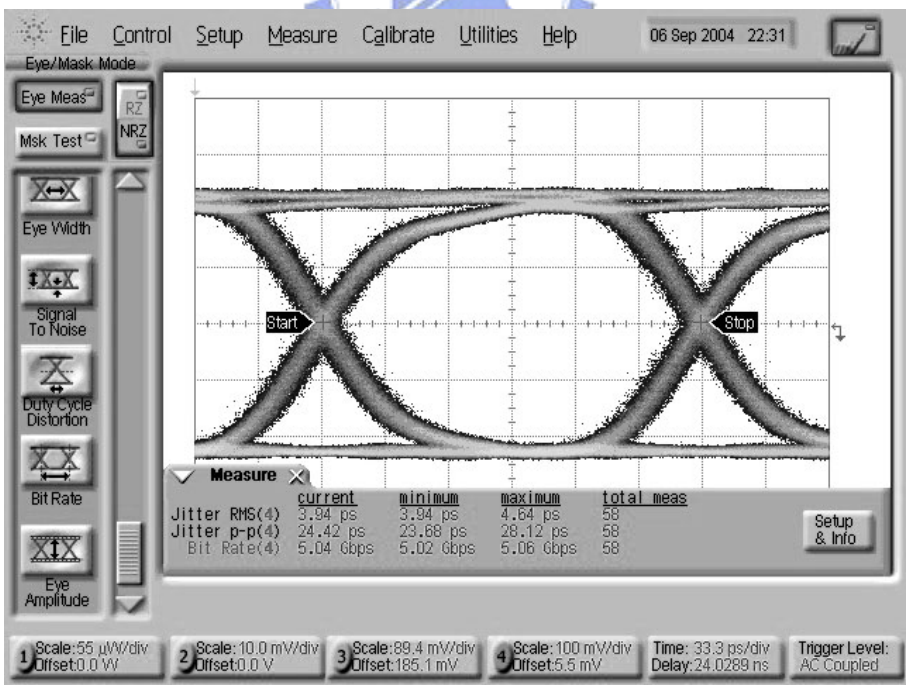


Fig. 4-12 : 5Gbps eye diagram with 2^{31}-1 PRBS input. (X axis: 33.3ps/div, Y axis: 100mV/div, Jitter(pp)=24.42ps).

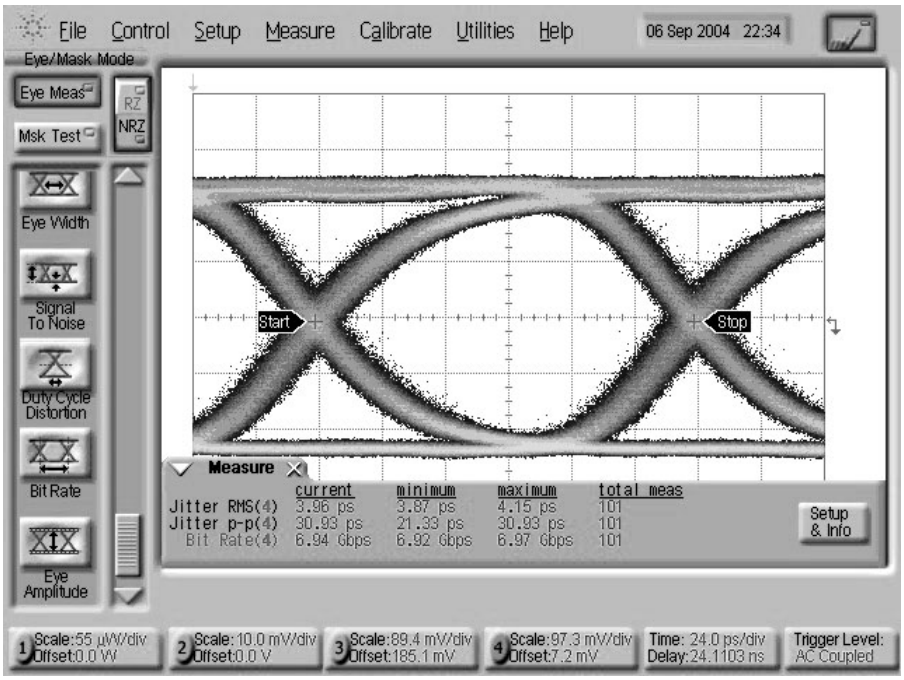


Fig. 4-13 : 7Gbps eye diagram with 2^{31}-1 PRBS input. (X axis: 24ps/div, Y axis: 97.3mV/div, Jitter(pp)=30.93ps).

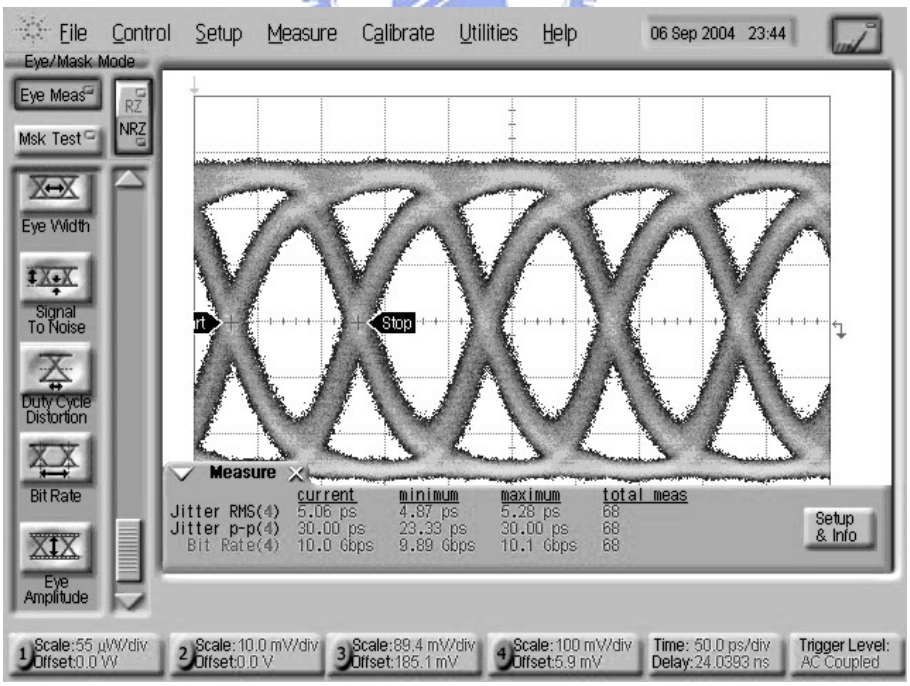


Fig. 4-14 : 10Gbps eye diagram with 2^{31}-1 PRBS input.(X axis:50ps/div, Y axis: 100mV/div, Jitter(pp)=30ps)

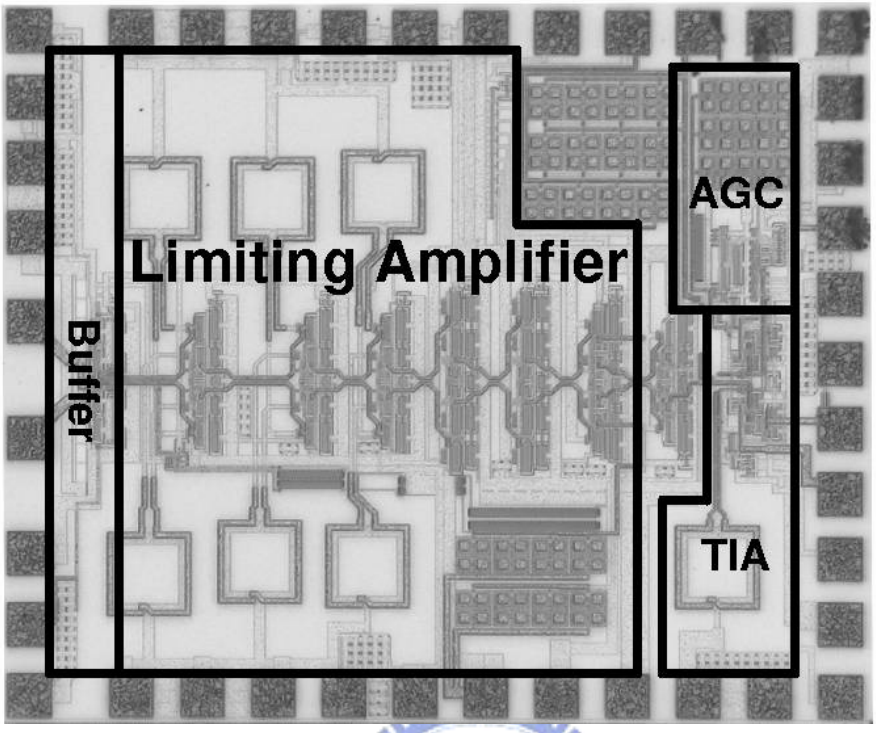


Fig. 4-15 : Optical receiver AFE chip photograph.

4.6. Conclusion

This paper describes the design of a fully-integrated 10 Gbps optical receiver analog front-end in a generic 0.18 μ m CMOS technology. The optical AFE provides a conversion gain of 90 dBΩ and -3 dB bandwidth of about 7.86 GHz, which is limited by the transimpedance amplifier. A regulated cascode input stage is utilized to decouple the loading effect at the input node, and wide bandwidth is achieved by means of shunt feedback and inductive peaking. Instead of using bulky planar inductors or two asymmertric 3-D inductors, this paper proposes a novel fully symmetric 3-D transformer for inductive peaking in each differential pair. Thus the chip area can be greatly reduced. Moreover, an AGC is built in to alleviate overload

induced data jitter. The proposed architecture is suitable for both low cost and low voltage applications.

Table I summarized the performance comparison between this work, our previous work in [32] and the prior arts in [25][30][31]. By single chip integration, gain-bandwidth requirement for individual building blocks can be rearranged and further optimized. The proposed prototype is both power and area efficient while manifesting good performance.

	This work	[25]	[30]	[31]	[32]
Function	TIA+AGC+LA Single Chip	LA	LA and TIA chip sets	TIA	TIA+AGC+LA Single Chip
Power	199mW (1.8V)	150mW(1.8V)	TIA:108mW LA:360mW (1.8V)	137mW(1.8V)	210mW(1.8V)
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Inductor Counts	7	24	N.A.	2	9
GBW	248.5 THz-Ω	2.97 THz	11.7 THz-Ω(TIA) 1.19 THz(LA)	4.6 THz-Ω	135 THz-Ω

Table 4-1 Performance comparison

Chapter 5

Conclusion

This thesis describes the design of optical receiver front-end fabricated in TSMC 0.18μm 1P6M CMOS technology. Furthermore, the design methodology and implementation techniques of optical receiver were presented. Major research results can be summarized as follows.

First, in order to accomplish a high speed circuit at low supply voltage, inductive peaking technique is adopted. An attractive feature of this technique is that the bandwidth enhancement comes with no additional power dissipation. To reduce the chip area and improve the resonate-frequency of the inductive load, an inverting type transformer with symmetric stacked configuration is proposed.

Second, a trans-impedance amplifier with automatic gain control is demonstrated. The bandwidth is enhanced by the following techniques: (i) A low input impedance TIA is implemented by regulated cascode gain stage consists of a common gate

amplifier with its gate controlled by a negative local feedback loop. (ii) the global feedback is replaced with local feedback to further increase the dominate pole. (iii) Shunt-peaking is adopted to produce an additional zero. Moreover, the gain control is realized by adjusting the gate voltage of the feedback transistor parallel with a fixed passive resistor. Implemented in a 0.18 μm digital CMOS process, the input dynamic range is from -13dBm to 0dBm.

Finally, a single chip 10Gbps optical receiver front-end is implemented in 0.18mm CMOS technology, which manifests GBW exceeds that of the state-of-the-arts reported to date. The single chip optical receiver facilitates GBW optimization, and benefits from low power consumption and small form factor.

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