低功率正反器與可重置的先進先出暫存器設計

學生：蔡志侃　　指導教授：黃威

國立交通大學電子工程學系研究所碩士班

摘　　要

本論文使用低功率電路設計技術來實現時脈驅動儲存元件設計。一個適合應用在低資料轉換率應用的低震盪電壓條件性擷取時脈邊緣觸發正反器被提出且使用 TSMC 100nm 技術設計。此單緣觸發正反器使用了低震盪電壓的時間延遲電路、條件性擷取技術和電晶體疊加技術來達到低功率設計。另外，一種條件性充電雙時脈邊緣觸發正反器被提出且使用 TSMC 100nm 技術實驗。此種使用了條件性充電技術的雙緣觸發正反器能夠在管路化系統中有效地降低一半的時脈功率消耗。

為了能夠減少時脈系統的功率消耗，一種新型的閘電路被提出。這種新型的閘電路結合了三種時脈閘技術，可應用在消除資料的短時脈衝波干擾和減少系統中多餘的功率消耗。一種結合了電路偵測功能和資料保存功能的電路操作機制在第四章中被討論。前面提出的條件性充電雙時脈邊緣觸發正反器也使用了此技術來重新設計且使用 TSMC 100nm 技術來模擬。

一個可重置的先進先出暫存器被實現且使用 TSMC 0.13um 技術設計。此先進先出暫存器可重新配置需要的儲存資料量，在使用 16 字元資料量下可減少 31.7%的功率消耗，使用 64 字元時則減少 18.3%。此先進先出暫存器可應用在通訊系統中和使用在記憶體自動配置程式之中。

Low Power Flip-Flop and Reconfigurable FIFO Design

student：Chi-Ken Tsai　　Advisors：Dr. Wei Hwang

Department of Electronics Engineering & Institute of Electronics
National Chiao Tung University

ABSTRACT

The clocked storage elements using the low power technique are realized in this paper. The low swing conditional capture edge-triggered flip-flop (LSCCFF) suitable for the low switching activity applications is proposed and simulated in TSMC 100nm technology. The single edge-triggered flip-flop uses low swing voltage delay chain, conditional capture technique and stacked technique to reduce the power consumption. A conditional precharged double edge-triggered flip-flop (CPDFF) is presented and simulated in TSMC 100nm technology. The double edge-triggered flip-flop using the conditional precharged technique could be used to reduce half of the clock power in a pipelined system efficiently.

In order to reduce the power in the clock tree, a new gating circuit is presented. This gating circuit combines three kinds of the clock gating techniques and could be used to cancel the glitch and reduce the redundant power in the system. The scan-retention mechanism is discussed in the chapter 4. The CPDFF is redesigned with the scan-retention technique and simulated in TSMC 100nm technology.

A reconfigurable first-in-first-out register file (FIFO) is proposed and simulated in TSMC 0.13um technology. The FIFO cell could reconfigure the valid storage word length and save 31.7% and 18.3 static power for 16 words and 64 words storage length. This FIFO cell could be applied to the communication systems and used in the memory compiler program.