A Charge-Based Capacitance Model of Short-Channel MOSFET's

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Abstract—**A new quasi-static two-dimensional (2-D) intrinsic capacitance model for short-channel MOSFET's has been proposed. It was derived based on a physically based charge sharing scheme and implemented using a quasi-static solution of a MOS device simulator. 2-D field-induced mobility degradation, velocity saturation, and short channel effects are included in the model. In this model, charge conservation holds and channel charge partitioning are properly treated. The simulation results clearly show the importance of 2-D field-induced effects to short-channel MOS devices. Comparison of the simulated results with reported experimentally measured data shows that the proposed model is far more reliable than the analytical model. The proposed method can be used to link a device simulator and a circuit simulator for accurate timing calculation in both digital and analog MOS integrated circuits.**

I. INTRODUCTION

WITH THE ADVENT in silicon MOS-VLSI technology and the scaling down of device size, precise characterization of small geometry MOS transistors and their associated circuit models are becoming increasingly important for predicting the performance of VLSI circuits, particularly for ac small signal or transient simulation purpose in designing DRAM and switching capacitor circuits. Two important characteristics needed for circuit simulation are the MOS dc (I–V) and ac (CV) models. Much work has been devoted to the study of dc models for small geometry VLSI devices. On the other hand, by comparing with the development of dc models, insufficient effort has been placed on the ac characterization of these devices.

The capacitances associated with a MOSFET include 1) overlap capacitances, 2) junction capacitances, and 3) intrinsic capacitances. Shown in Fig. 1 is a cross sectional view of a MOSFET with various capacitances indicated and a complete circuit model of MOSFET in SPICE2. It shows the nonlinear dc circuit model and all of the above capacitances. Among them, *overlap capacitances*, such as CGDO, CGSO, CGBO, are linear capacitances and process-dependent, and can be measured from the test-key of IC process; *junction capacitances*, such as CJ, CJSW, are also process- and geometry-dependent and can be formulated by the p-n junction theory or measured experimentally. *Intrinsic capacitances*, such as C_{GS}, C_{GD}, C_{GB}, etc., are caused by the gate induced charges in the channel region as shown in Fig. 2. They are nonlinear capacitances which are bias-dependent and so can not be easily modeled. This paper will be focused on the development of an *intrinsic capacitance model* for short-channel MOSFET's.

Meyer [1] is the first to present a capacitance model which is widely used in SPICE2. Much work [2]–[6] has been placed on the study of an improved model for solving two existing problems. Ward and Dutton [2] pointed out the *charge nonconservation problem* in Meyer's model. Another problem is the *channel charge partitioning* [4], [5]. A more recent model, derived analytically from the depletion approximation by Sheu *et al.* based on CSIM [5] (which has been replaced by a new name called BSIM in [6] and will be used hereafter in this paper), seems to be a better one in terms of simplicity and consistency since its dc I–V and ac CV characteristics are consistently derived. However, the model is not accurate enough for short-channel devices due to neglecting the 2-D field induced mobility degradation effects and the assumption of surface potential clamping at $2V_F$ (where V_F is the quasi-Fermi potential) for MOS devices operating in the strong inversion region. Until recently, Iwai *et al.* [7] proposed one way of using accurate numerical approaches, i.e., numerical simulation, in which some of the shortcomings mentioned above can be overcome. However, only the capacitances associated with the gate terminal can be computed, i.e., C_{GD}, C_{GS}, and C_{GB}. The capacitances associated with the other terminals cannot be computed directly in their method since the way of *channel charge partitioning is unavailable*.

In the characterization of small size MOSFET's, accurate models should consider 2-D or 3-D effects. In this paper, we propose for the first time a novel approach in obtaining *all of the intrinsic capacitances including the nonreciprocal components* for short- and long-channel MOSFET's through numerical simulation. The above mentioned two problems in reported literatures, *charge conservation* and *channel charge partitioning*, are properly treated. Also, since the numerical simulation involves the solution of the 2-D fields which include the field-induced mobility degradation and velocity saturation, short-channel effects in the proposed model are properly considered. The evidence of the computed re-

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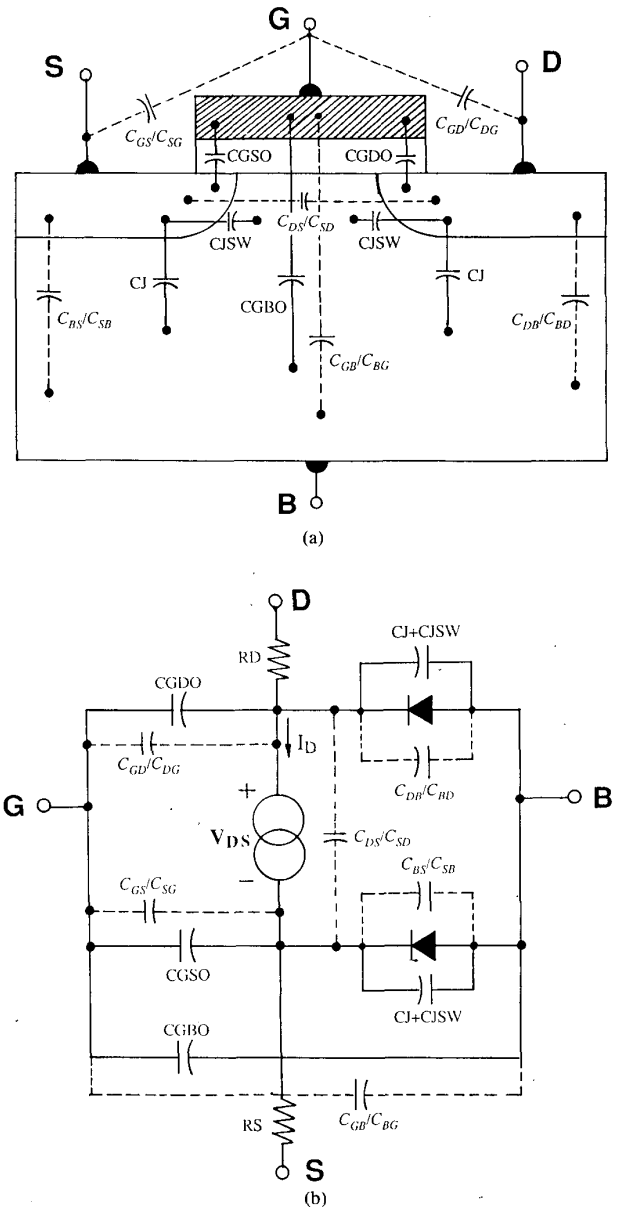

Fig. 1. (a) Cross-sectional view of a MOSFET and the associated capacitances. Intrinsic capacitances are shown in dashed lines. (b) A complete circuit-based model of MOSFET for SPICE2.

sults in this paper would show that mobility and velocity saturation effects will affect the short-channel device significantly. The motivation in developing the intrinsic capacitance is intended to link a device simulator and a circit or timing simulator (e.g., [8]) without using equivalent circuit model for capacitance calculation. A charge-based model is proposed and implemented using device simulator-MINIMOS [9] in Section II. Section III shows the simulation results and the short-channel effects on the *CV* characteristics are investigated. Comparison of the new results with reported models are given in Section IV. Finally, summary and conclusions are given in Section V.

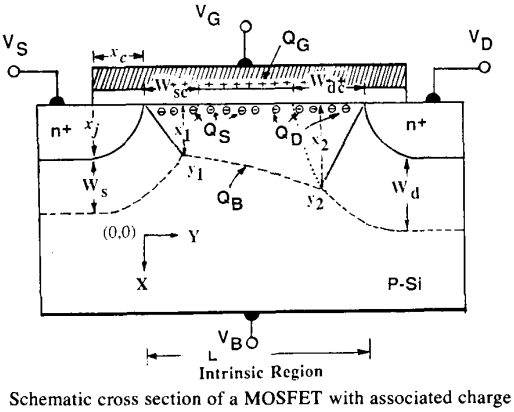

Fig. 2. Schematic cross section of a MOSFET with associated charge distributions and the boundaries of Q_B.

II. Charge-Based Model

In formulating a 2-D charge model which is suitable for short-channel MOSFET's, accurate calculation of the charge distribution in the MOS devices has been proposed based on a *physically-based* charge sharing scheme and a *reasonable* channel charge partition for Q_S and Q_D. The numerical simulation by incorporating these ideas will be discussed in this section.

For the n-channel MOSFET given in Fig. 2, there are four kinds of charges associated with the terminals of the device, in which Q_G, Q_D, Q_S, and Q_B represent the gate, drain, source, and bulk terminal charges, respectively. The channel charge in the inversion layer is called Q_C and is split with some ratio into Q_S and Q_D depending on the device operating regions. They must satisfy the charge conservation rule

$$Q_B + Q_B + Q_C = 0. \tag{1}$$

All of these charges are nonlinear functions of device terminal voltages, V_G, V_D, V_S, and V_B. The intrinsic capacitances are defined by

$$C_{ij} = -\partial Q_i / \partial V_j, \qquad \text{for } i \neq j \tag{2}$$

where i, j represents one of the four terminals, i.e., D(drain), S(source), G(gate), and B(bulk). Q_i is the charge of the i terminal and V_j is the voltage of the j terminal. For intrinsic capacitance calculation, we need to find the above charge components as functions of terminal voltages which again give various CV characteristics in the voltage range of interest.

For example, there are three gate capacitances associated with the gate

$$C_{GS} = -\partial Q_G / \partial V_S \big|_{V_{GD}, V_{GB}}$$

$$C_{GD} = -\partial Q_G / \partial V_D \big|_{V_{GS}, V_{GB}}$$

and

$$C_{GB} = -\partial Q_G / \partial V_B \big|_{V_{GS}, V_{GD}}. \tag{3}$$

For numerical simulation, C_{GD} is calculated as $-\Delta Q_G / \Delta V_D$. Q_G is computed by integrating $\epsilon_{ox} E$ along the gate electrode periphery between the source and drain

edges, i.e.,

$$Q_G = W \int_0^L q_G(y)\, dy = W \int_0^L \epsilon_{ox} \vec{E}_y \cdot \overrightarrow{dl}$$
$$= W \int_0^L \epsilon_{ox} E(x)\, dy. \quad (4a)$$

Here, $q_G(y)$ is the gate charge per unit channel length, $E(x)$ is the electric field perpendicular to the gate electrode, and W is the channel width. ΔQ_G is computed as the gate charge difference between the two simulations for V_D and $V_D + \Delta V_D$, that is

$$\Delta Q_G = W \int_0^L \epsilon_{ox}\, \Delta E(x)\, dy \quad (4b)$$

which then gives C_{GD} from (3). Similarly, C_{GS} and C_{GB} are computed in a similar manner by replacing ΔV_D by ΔV_S or ΔV_B.

In order to determine the bulk charge, Q_B, a *2-D charge sharing scheme* [10] is adopted as shown in Fig. 2 for MOS device operating in the linear region. In this scheme, the slant line at the source and drain regions are drawn to approximate the value of the bulk charges. The bulk charges outside the slanted boundaries are assumed to be the depleted charges due to the source and drain junctions, whereas that inside the slant lines are the gate induced bulk charge in the intrinsic region. In other words, Q_B is the total gate induced depletion charge bounded by the dashed trapezoidal region and has 2-D distributions in the x- and y-directions. The boundary points, (x_1, y_1) and (x_2, y_2), are determined as follows.

The drain and source regions are assumed to be a planar junction in vertical direction and a cylindrical junction in the lateral direction. In Fig. 2, x_j is the source/drain and bulk junction in the depth direction, x_c is the lateral diffusion length of the source(drain) junction, and is assumed to be 0.7 times x_j in practice. W_s and W_d are the depletion layer width of a plane junction at the source and drain side respectively. W_{sc} and W_{SD} are the depletion layer width of a cylindrical junction. The overall depletion layer around the junction can be considered to be an ellipse with center at the gate end. W_s and W_d are given by

$$W_s = \kappa \sqrt{V_{bi} - V_{BS}} \quad (5a)$$

and

$$W_d = \kappa \sqrt{(V_{bi} + V_{DS} - V_{BS})} \quad (5b)$$

where

$$\kappa = \sqrt{2\epsilon_{si}/qN_A}. \quad (6)$$

Here, V_{bi} is the built-in voltage of the source(drain)-bulk junction, V_{BS} is the back gate bias, and V_{DS} is the drain to source voltage. Once W_s and W_d are known, the lateral diffusion length across the cylindrical junction can be approximated by the ellipsoidal formula [11], i.e.,

$$W_{sc} = x_j[d_1 + d_2(W_s/x_j) - d_3(W_s/x_j)^2] \quad (7a)$$
$$W_{dc} = x_j[d_1 + d_2(W_d/x_j) - d_3(W_d/x_j)^2] \quad (7b)$$

where

$$d_1 = 0.0631353,\ d_2 = 0.8013292,$$
$$\text{and } d_3 = 0.01110777. \quad (7c)$$

The boundary point (x_1, y_1) is on the ellipse, therefore, we have

$$[x_1/(x_j + W_s)]^2 + [y_1/(W_{sc} + x_c)]^2 = 1 \quad (8)$$

which then gives

$$y_1 = (W_{sc} + x_c)\sqrt{[1 - x_1/(W_s + x_j)^2]}. \quad (9)$$

Also,

$$x_1 = \kappa \sqrt{\Phi_{s1} - V_{BS}} \quad (10)$$

where Φ_{s1} is the surface potential at $y = x_c + W_{sc}$ and can be obtained from simulation. There are two unknowns in (9) and (10), only 2 or 3 iterations are needed to determine x_1 and y_1. Similarly, x_2 and y_2 can be determined from the following two formulas.

$$y_2 = (L + 2x_c) - (W_{dc} + x_c)\sqrt{[1 - x_2/(W_d + x_j)^2]} \quad (11)$$

and

$$x_2 = \kappa \sqrt{\Phi_{s2} - V_{BS}} \quad (12)$$

where Φ_{s2} is the surface potential at $y = L + x_c - W_{dc}$.

Therefore, Q_B is calculated as

$$Q_B = -W \int_0^L q_B(y)\, dy$$
$$= -W \int_0^L \int_0^{X_d} q[p(x, y) - N_A]\, dx\, dy. \quad (13)$$

Here, $q_B(y)$ is the depleted bulk charge per unit channel length and width, p is the hole density in the x-y direction and x_d is the depletion layer width. The channel charge, Q_C, in the inversion layer, is the sum of Q_D and Q_S. In reported literatures [2], [4]-[5], channel charge partitioning, i.e., the partition between Q_S and Q_D, were presented. The ratio of Q_D and Q_S varies for devices operating in different regions based on the artifact of satisfying a specific boundary condition. However, note that there are infinite ways to do the channel charge partitioning. To overcome this problem, a physically-based channel charge partitioning method proposed by Oh *et al.* [12] was used in [5] and will be used here also. Since $q_c(y)$ is a stiff exponential function in the x-direction, it is rather difficult to compute the numerical integration of $q_c(y)$ directly. Instead of computing the direct integration of $q_c(y)$, an indirect way of using $q_c(y) = -(q_G(y) + q_B(y))$ in the numerical integration is proposed. Therefore, Q_S and Q_D

are represented by

$$Q_S = W \int_0^L (1 - y/L)[q_G(y) + q_B(y)]\, dy \quad (14)$$

and

$$Q_D = W \int_0^L (y/L)[q_G(y) + q_B(y)]\, dy \quad (15)$$

respectively. Here, $q_c(y)$ is the channel charge per unit channel length.

A 2-D device simulator-*MINIMOS* 3.0, has been adequately modified with a suitable chosen grid by increasing the grids near the source and drain regions in y-direction and increasing the grids near the depletion layer boundary in x-direction in order to keep the integration accuracy. A physically-based mobility model in [13] has also been incorporated in the simulator. By applying the above equations, the charge densities, $q_G(y)$, $q_B(y)$, and hence, the charge associated with their respective terminals can be calculated using accurate *cubic spline* numerical integration technique. Once the charge variations in the voltage range of interest are known, the intrinsic capacitances can be computed by applying (3). Note that since the simulation results from MINIMOS are obtained at steady-state, the capacitance values were developed for quasi-static operation.

III. Simulation Results

Simulations have been carried out for a set of n-channel Si-Gate MOS devices with different channel lengths (L). Device and process parameters are: device channel width, $W = 30\ \mu$m, gate oxide thickness, $t_{ox} = 450$ A, and substrate doping, $N_A = 1.2 \times 10^{15}\ \text{cm}^{-3}$. The drain and source regions are As-implanted through a thin oxide (550 A) with an energy of 150 keV and dose of $1 \times 10^{15}\ \text{cm}^{-2}$. Diffusion temperature and time are 1050°C and 30 minutes, respectively. Junction depth, x_j, is about 0.3 μm. The simulated capacitances are normalized by WLC_{ox}, where C_{ox} is the computed gate oxide capacitance per unit area.

Figs. 3 and 4 show the simulated intrinsic capacitances versus V_{GS} characteristics for 2-μm and 20-μm channel length devices, respectively, operating throughout all the regions. In order to investigate the short-channel effect on the CV characteristics, a number of $C - V_{GS}$ curves for MOS devices with $L = 1$, 2, 4, and 20 μm are also computed and compared as shown in Figs. 5–7. Several important features and the short-channel effect can be observed from the comparison of these figures.

(1) For the long-channel device (Fig. 3), C_{GS} will approach the $2/3WLC_{ox}$ value in the saturation region and decrease to a lower value in the linear region. This $2/3WLC_{ox}$ capacitance is the value that is used widely in the rather primitive Meyer's model [1]. However, for the short channel device (Fig. 4), the value of C_{GS} will be higher than that of long-channel device at saturation and approaches this value at very high gate voltage in the linear region. It is worth noting that normalized values of C_{SG} and C_{DG} will approach with each other to an approximate value of 0.5 at very high gate voltages (linear region). This is essentially the same as the channel charge partition which was widely used in reported literatures [2],

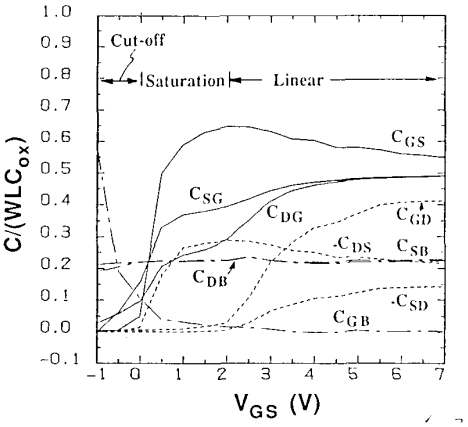

Fig. 3. Results of intrinsic capacitance simulation for $L = 20\ \mu$m at $V_{DS} = 2$ V, $V_{BS} = 0$ V.

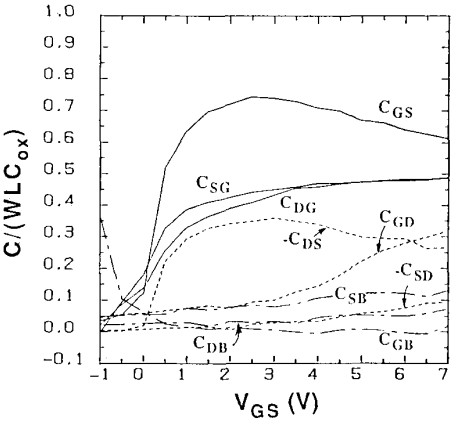

Fig. 4. Results of intrinsic capacitance simulation for $L = 2\ \mu$m at $V_{DS} = 2$ V, $V_{BS} = 0$ V.

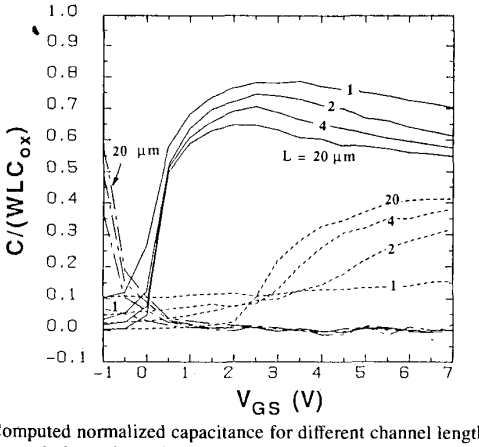

Fig. 5. Computed normalized capacitance for different channel lengths and the observed short channel effects. C_{ox} is the gate oxide capacitance. (——) C_{GS}, (- - -) C_{GD}, (— - —) C_{GB}.

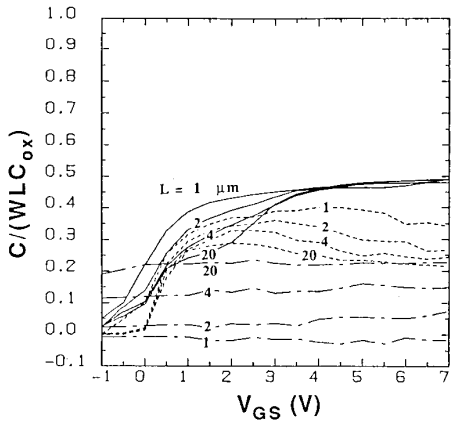

Fig. 6. C_{DG}, C_{DS}, C_{DB} versus V_{GS} for different channel lengths. (——) C_{DG}, (- - -) $-C_{DS}$, (— — —) C_{DB}.

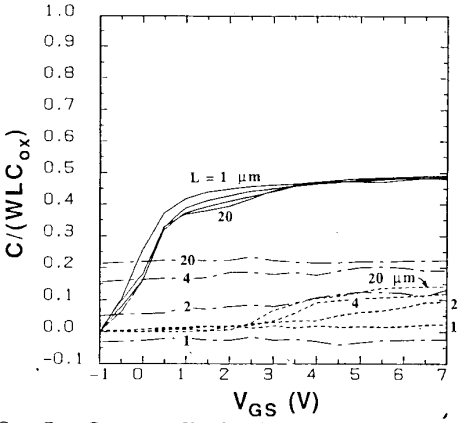

Fig. 7. C_{SG}, C_{SD}, C_{SB} versus V_{GS} for different channel lengths. (——) C_{SG}, (- - -) $-C_{SD}$, (— — —) C_{SB}.

[4–5]. One interesting result is by comparing the $C_{SG}(C_{DG})$ curves for both the 20 and 2 μm devices in Figs. 3 and 4, respectively. It is noted that in the saturation, C_{SG} or C_{DG} is more flat for the long-channel device. It is a manifestation of the less velocity saturation effect on long-channel device since the C_{SG} or C_{DG} characteristic is related to the channel charges, Q_C.

(2) One specific feature of the short-channel effect is revealed in the comparison of the C_{GD} characteristics in Fig. 5. There is a sharp transition between saturation and linear regions for long-channel device at $V_G = 2.2$ V whereas it is smoothly changed for short-channel device. These are due to the 2-D field-induced effects. The physical reasons are given as follows. Total charge at the gate is given by

$$Q_G = WC_{ox} \int_0^L [V_G - V_{FB} - V_S(y)]\, dy \qquad (16)$$

where $V_S(y)$ is the surface potential. At a given gate voltage, V_G, the change in the gate charge, ΔQ_G, due to ΔV_D can also be calculated from

$$\Delta Q_G = -WC_{ox} \int_0^L \Delta V_S(y)\, dy. \qquad (17)$$

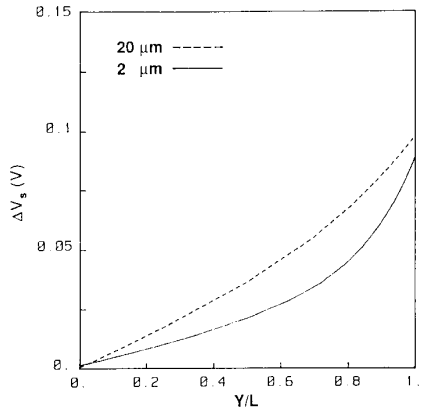

Fig. 8. Comparison of ΔV_S versus y/L for a long-channel and a short-channel devices.

We see that the value of C_{GD} or ΔQ_G is proportional to the integration of ΔV_S from source to drain at two different V_D's. The area under the ΔV_S curve is larger for higher V_G and thereby giving an increase of C_{GD} with increasing gate voltages. It is also noted that in the cutoff and saturation region for long-channel devices, the amount of induced charges on the gate through the oxide, and hence, the induced capacitance, C_{GD}, is small compared to WLC_{ox} whereas it is much more significant for short-channel devices. However, normalized value of C_{GD} decreases with decreasing channel length due to the velocity saturation in the linear region. Since velocity saturation near the drain gives rise to an increase of the channel resistance or smaller area under ΔV_S curve. For example, Fig. 8 gives the simulated ΔV_S versus y/L curves for two devices with channel length 2 μm (dashed line) and 20 μm (solid line) working in the linear region. It is apparent that 2-μm channel length device has smaller ΔV_S value due to the velocity saturation effect which results in a reduced C_{GD} for short-channel devices. It can also visualize from (17) that a short-channel with lower ΔV_S curve has smaller ΔQ_G, and hence smaller, C_{GD}.

(3) From the family of curves for C_{GS} (Fig. 5) it is seen that the C_{GS} curve of the short-channel device will rise above the cutoff region at a lower gate voltage than in the long-channel device due to a lower threshold voltage of the short-channel device. Also, from the saturation to linear region, C_{GB} is nearly zero and the total gate capacitance $C_G = C_{GS} + C_{GD} + C_{GB}$. Since short-channel device has smaller C_{GD}, its C_{GS} apparently is larger than that of long-channel device.

(4) In the cutoff region, fringe fields from the source and drain will tend to decrease the accumulation of holes, thereby giving smaller C_{GB} value for short-channel device as shown in Fig. 5.

(5) One important fact in designing VLSI circuits is that capacitances are not scaled with reducing channel length as revealed from the above figures, Figs. 5–7, and thus need further consideration in designing VLSI circuits.

Variations of capacitances with varying drain-source bias, $C - V_{DS}$, for $L = 2$ μm is also computed as shown

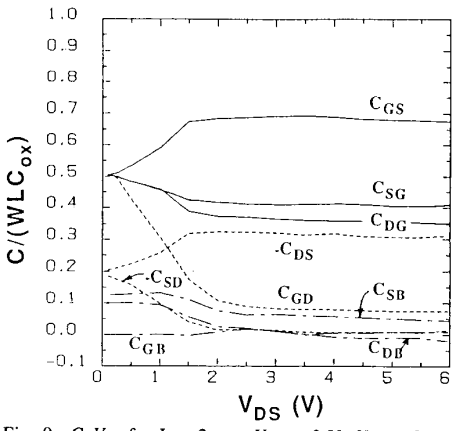

Fig. 9. C-V_{DS} for $L = 2$ μm, $V_{GS} = 2$ V, $V_{BS} = 0$ V.

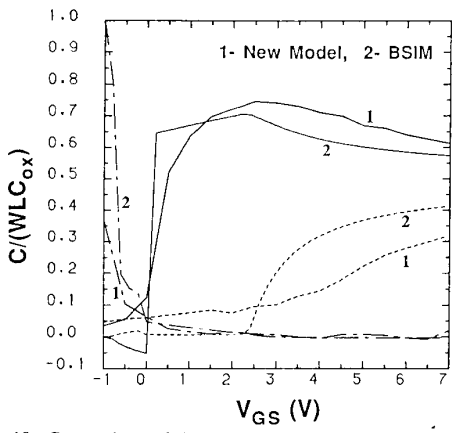

Fig. 10. Comparison of the new results with BSIM. $L = 2$ μm. (——) C_{GS}, (- - -) C_{GD}, (— - —) C_{GB}.

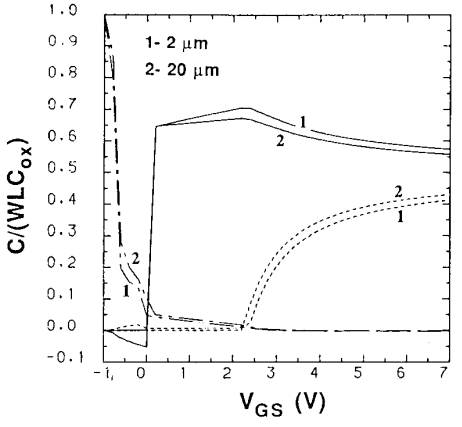

Fig. 11. Computed results from BSIM for $L = 2$ μm and $L = 20$ μm, (——) C_{GS}, (- - -) C_{GD}, (— - —) C_{GB}, respectively.

in Fig. 9. Note that at zero drain-source bias, normalized capacitances C_{SG} and C_{DG} are approximately equal to 0.5. A finite value (0.07 in the linear region) of C_{GD} is obtained for short-channel devices which puts a limit on the high frequency performance for VLSI applications.

IV. Comparison with Reported Models

Based on the numerical results as computed above, this section will deal with the discussion of the validity and the comparison of the new model with reported analytical model [5] as well as experimentally measured results [7]. As a comparison between our new results with those of BSIM [5], one typical result, $C - V_{GS}$ curve, for $L = 2$ μm is shown in Fig. 10. Two basic mechanisms responsible for the discrepancies are discussed as follows.

(1) In BSIM [5], field-induced mobility degradation and velocity saturation effects are not included in its analytical expression, therefore, capacitance values have a sharp transition between different operating regions. This is obvious from the results shown in Fig. 11 obtained by the method of BSIM. It shows that there is not much difference between long- and short-channel devices due to the improper treatment of the velocity saturation effect. In other words, this is due to the exclusion of the mobility factor in deriving CV characteristics from I-V characteristics in [5], which is equivalent to use a constant mobility in the formulation. However, there is no such problem in our new numerical model since field-induced effects are already included in the device simulator. Moreover, from a recent paper by Iwai *et al.* [7], we learned that sharp transition for C_{GD} and C_{GS} is for the case of constant mobility, i.e., without considering vertical field-induced mobility degradation and velocity saturation effect. Therefore, we conclude that C_{GS} and C_{GD} should have a smooth transistion from saturation to linear region due to the velocity saturation effect. This smooth transition of capacitance values between different regions are also consistent with the reported measuring results as shown in [14] (e.g., Fig. 1).

(2) In our model, charge conservation holds as it does for [2]–[6]. However, based on our channel charge partitioning method, Q_S/Q_D ratio changes with gate biases in the saturation region. In BSIM, the Q_S/Q_D ratio changes from 6/4 (a fixed value) in the saturation to 5/5 in the triode region (Fig. 2 in [5]). The reason is quite obvious for two reasons. One is the abandonment of the pinning of surface potential at $2V_F$ in the new model since the actual simulated value of surface potential is varied along the channel but not fixed at $2V_F$, particularly at the surface near the drain. The other one is that the velocity saturation effect will affect the surface potential significantly in short-channel devices, and hence, the CV results. Therefore, it is concluded the Q_S/Q_D ratio has its natural distribution (Figs. 3 and 4) rather than as that indicated in [5, Fig. 2].

(3) One important implication from the above comparisons is that better analytical CV model can be achieved in the future if we can find an appropriate formulation of the characteristics in short-channel MOS devices. These characteristics include accurate formulation of the mobility degradation which incorporates both vertical and lateral field-induced effects and an accurate expression of the surface potential for short-channel devices.

V. Conclusion

In this paper, a new 2-D intrinsic capacitance model for short-channel MOSFET's has been proposed based on a physically-based charge sharing scheme and a reasonable channel charge partitioning method using numerical simulation. All of the intrinsic capacitances including the nonreciprocal components in a MOS device are computed and demonstrated for the first time. Short-channel effects on the device *CV* characteristics are investigated and compared with reported models. Comparisons with reported analytical models or experimental data show that the new model is close to experimental results particularly for short-channel devices. Accuracy problem in reported analytical models has been overcome since the 2-D field-induced effect has been included in the numerical solution.

Several important features of the proposed model are that: 1) Both charge nonconservation and channel charge partitioning problems are solved in the new model. 2) It includes the vertical field-induced mobility degradation and velocity saturation effects which are both crucial to short-channel MOS device characteristics. 3) The *CV* curves are continuous and vary smoothly throughout all regions of operation. It is quite important for the convergence property in circuit simulation applications. 4) The model can be easily applied to a real transistor with complicate device structures and process parameters such as MOS devices with implanted channel, however, the analytical model is not available for implanted-channel MOS devices. 5) It bridges the gap between a device simulator and a circuit/timing simulator. The most important use of the modeled results is in establishing a table look-up *CV* characteristic (such as the method in [15]) for timing or circuit simulator and for use in timing delay estimation of MOS-VLSI circuits. Moreover, the results obtained in this paper can be used as a guideline for showing the accurate description of the *CV* characteristics.

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