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碩 士 論 文

先進材料應用於低溫複晶矽薄膜電晶體和金氧半場效電晶體之研究

A Study of Low-Temperature Polycrystalline Silicon Thin Film Transistors and MOSFETs Using Advanced Materials

研 究 生：黃耀陞

指導教授：簡昭欣　教授

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研 究 生：黃耀陞　　Student：Yao-Sheng Huang

指導教授：簡昭欣　　Advisor：Chao-Hsin Chien

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摘要 (中文)

在本論文中，我們利用了先進的高介電常數材料來製造高效能的低溫複晶矽薄膜電晶體。擁有高效能 N 型通道薄膜電晶體以不同的高介電常數介電層材料：包括二氧化鉿（HfO_2）、矽酸鉿（Hf-silicate）、氧化鋁鉿（Hf-aluminum oxide）被提出，以有機金屬高介電薄膜沉積系統沉積的高介電常數介電層在低溫環境中被製作出來，分別參雜不同比例的矽或鋁組成比作為我們互相比較的主軸，並且研究其效應與可靠度。

我們發現高介電常數材料在電性上的表現有著普遍性的改善：包括有較低的臨界電壓、較好的次臨界擺幅、較高的驅動電流；在研究中，我們發現擁有複晶結構的二氧化鉿 (HfO_2)薄膜會導致較大的漏電流；相對地，矽酸鉿 (HfSiOx)薄膜則表現出比較優異的熱穩定度，在高溫退火處理後仍維持其非晶狀態的結構。氧化鋁鉿 (HfAlOx)薄膜則隨著鋁的參雜量越多，亦可提高其結晶溫度。當然，矽酸鉿薄膜相較於二氧化鉿薄膜較低的介電常數，則為矽酸鉿薄膜的缺點。另外，具有較低介電常數的介面層自然形成於

高介電氧化層薄膜和矽基板之間，將會導致等效氧化層厚度降低的問題。

我們也研討了有關使用高介電薄膜當作閘極介電層的複晶矽薄膜電晶體所引起的嚴重漏電流現象。我們認為高介電薄膜所產生的較高電場是引發嚴重的閘極誘發汲集漏電流(GIDL)的原因，而場發射電流為其主要的漏電流機制。不同介電層的複晶矽薄膜電晶體，其中矽酸鉿在目前的測試中展現了較佳的可靠度，主要原因在於其有較高的結晶溫度、較好的薄膜品質與較少的介面狀態密度。

最後，我們嘗試將此新開發的高介電係數材料應用在金氧半場效電晶體，並且探討較薄介電質層的結構和電性。

A Study of Low-Temperature Polycrystalline Silicon Thin Film Transistors and MOSFETs Using Advanced Materials

Student: Yao-Sheng Huang Advisors: Dr. Chao-Hsin Chien

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ABSTRACT

In this thesis, advanced High-κ materials were employed to fabricate high performance low-temperature polycrystalline silicon thin film transistors (TFTs). High performance n-channel poly-Si thin film transistors (TFTs) are demonstrated using the different High-κ dielectric with hafnium dioxide (HfO_2), hafnium silicate (HfSiOx) and hafnium aluminum oxide (HfAlOx) layer are demonstrated by metal organic chemical vapor deposition system with low temperature processing. We compare with different composition ratio High-κ materials layer for our main shaft and the effect and reliability are also studied.

It is found the electrical characteristic of High-κ dielectric TFTs that improve obviously：including the lower threshold voltage, the better subthreshold swing, the higher driving current.

However, the large leakage current would be caused by the polycrystalline structure of HfO_2 film. In contrast, HfSiOx films exhibit better thermal stability and retain the amorphous

structure even after high temperature annealing. In addition, as Al content increasing of HfAlOx films that could be to raise crystalline temperature. Certainly, the lower κ compared with HfO_2 film is the disadvantage of the HfSiOx films. Besides, the native interfacial layer with lower κ value always exists between the High-κ gate dielectric and Si substrate, which defeats the purpose of EOT lowering.

Moreover, the higher leakage current of poly-Si TFTs using High-κ gate dielectric was also studied. Aggravated gate-induced drain leakage (GIDL) current was thought to arise from the higher induced electric field by the introduction of High-κ films, and field-emission current would be the dominant leakage mechanism. We found the HfSiOx dielectric TFTs have the better reliability due to it has the better interface, higher crystalline temperature and lower density of states.

Finally, we also tried to apply the newly-developed High-κ films to the Metal-oxide semiconductor field-effect transistors (MOSFETs). And the structural and electrical properties of the thinner High-κ films were discussed.

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謹以此論文，獻給所有關心我的人以及我最親愛的家人!

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Chapter1

Introduction and Motivation

Low-temperature-polycrystalline-silicon (LTPS) thin-film-transistors (TFTs) have received much attention in recent years because of their increasing applications in active matrix displays (AMLCDs) [1.1]-[1.5], active matrix organic light emitting displays (AMOLEDs) [1.6]-[1.7], and memory devices [1.8]. Because of their better grain crystallinity, compared with the amorphous counterparts, higher carrier mobility and drive current can be achieved in poly-Si TFTs. The ability of fabricating high-performance LTPS TFTs enables their use in a wide range of new applications. Therefore, further improving the performance of LTPS TFTs is an interesting and important topic.

1-1 An Overview of Low-Temperature-Polycrystalline-Silicon (LTPS) Thin Film Transistors (TFTs)

The study of polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated below a maximum temperature of 600°C commenced in the 1980s. The original motivation was to replace quartz substrate with low-cost glass for active matrix display applications. In the beginning, the a-Si:H (hydrogenated amorphous silicon) TFTs were applied as the pixel switching device in the first-generation active matrix liquid crystal displays (AMLCDs). The major advantages of a-Si:H TFT technology are low processing temperature compatible with large-area glass substrate and low leakage current due to the high off-state impedance. However, because of the lack of short range order, the low carrier field-effect mobility (typically below 1 cm^2/V-Sec) of a-Si:H TFTs limited their application to the switching elements only. Integration of driver circuits with display panel on the same substrate is very

desirable because of the cost reduction in the module and reliability improvement of the system.

More recently, poly-Si TFTs are employed extensively in active-matrix liquid crystal displays because of their superior performance. The effective carrier mobility in poly-Si is significantly higher than that in a-Si, so the devices with reasonably high drive currents can be achieved in poly-Si TFTs. The higher drive-current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Previously, poly-Si TFT technology was primarily applied on small, high-definition LCD panels for projection display systems, however, the high processing temperature made it incompatible with commercial large-area glass substrates. With the rapid development of fabrication processes which are compatible with glass substrates in recent years, the manufacture of LTPS TFTs in AMLCDs on large-are substrates attracts more attentions. Modification of process procedure for enhancing TFT performance and reducing fabrication cost become an important issue in the fabrication of LTPS TFTs on large-area glass substrates.

Compared to the ultra-large scale integration (ULSI) process technology, the processes anddevice structures of LTPS TFTs are similar with metal-oxide-semiconductor field-effect-transistors (MOSFETs). The noticeable difference between LTPS TFTs and MOSFETs is that the former has to be performed at relatively low temperatures in order to be compatible with glass substrates. Due to this feature, only a-Si or poly-Si channels can be achieved on the glass substrate and the mobilities of a-Si and poly-Si are both much lower than that of c-Si (single-crystal silicon), which is widely used in conventional MOSFETs. Therefore, how to further increase the mobility of the low-temperature TFTs is one of the most important challenges. Among various process issues, the crystallization of a-Si thin films has been considered to be the most important process for fabricating high-performance

LTPS TFTs. The crystallized poly-Si thin films always serve as active layer (i.e., channel) in the poly-Si TFTs. As a result, the quality of crystallized poly-Si films profoundly affects the performance of the poly-Si TFTs. In polycrystalline materials, most of defects are present in the grain boundaries. Enlarging grain size by various crystallization methods, such as solid phase crystallization (SPC), laser crystallization, and metal-induced crystallization (MILC), can reduce the grain boundaries and effectively promote the quality of poly-Silicon. The performance of devices can be improved through the high-quality poly-Si formed by crystallization technologies. Furthermore, other low-temperature process technologies of fabricating LTPS TFTs, such as gate dielectric formation, dopant activation, defect passivation, and device structures, are also essential for producing high-performance LTPS TFTs.

Finally, novel structure design is another approach to fabricate high-performance poly-Si TFTs. This technique focuses on the reduction of the electric field near the drain junction, and thus suppresses the device's off-state leakage current. Many structures including multiple channel structures, offset drain/source, lightly doped drain (LDD), gate-overlapped LDD, field induced drain and vertical channel have been proposed and investigated intensively.

1-2 Motivation for improving Low-Temperature-Deposited Gate Dielectric Used in LTPS TFTs

In the recently, the gate dielectric scaling down trended toward of the physical limitation (~1.0nm for SiO_2) for International Technology Roadmap for Semiconductors (ITRS) [1.9]. It extend a number of fundamental problems such high leakage current、low oxide breakdown voltage and low mobility…etc.

For TFTs, the key parameters of the LTPS TFTs are：(1) High mobility, (2) Low threshold voltage, and (3) High driving current and Low leakage current at high operate

voltage. These are for demand of that to realize system-on-panel (SOP)、integrating driving ICs on the glass substrate and drive the liquid crystal. Using a thin dielectric can improve the driving current of TFTs. Similar to MOSFETs, however, the conventional gate dielectric (i.e. SiO_2、Si_3N_4) for small dimension TFTs also need to decrease the thickness. Although thinning down the gate oxide can increase the drive current of TFTs, however, the quality of low-temperature silicon oxide is not good enough, it results in higher gate leakage current.

However, the low-temperature-deposited oxide used in LTPS TFTs always exhibits poorer physical and electrical quality, such as high interface trap density, high gate leakage and low breakdown field, compared with high-temperature thermal grown oxide used in VLSI MOSFETs. Consequently, thicker gate oxide has to be used to prevent the high gate leakage current.

1-4 Why do we use High-κ materials?

In order to preserve the physical dielectric thickness while increasing the gate capacitance, several new high-κ materials, including Al_2O_3, Ta_2O_5 were proposed [1.10]-[1.11]. Among them, Al_2O_3 TFTs improvement is not sufficient due to the κ value is not high enough. On the other hand, the Ta_2O_5 TFTs induce higher gate leakage current due to its narrow band-gap.

In thesis, we fabricated the LTPS TFTs with High-κ gate dielectrics deposited by AVD system, including HfO_2, HfSiOx and HfAlOx. Mainly, in addition to show the lower threshold voltage，we want to discuss the influence of the different composition ratios of HfSiOx and HfAlOx films and reliability. Moreover, we hope to increase the driving current, decrease the threshold voltage of High-κ device and have high gate capacitance capability compared with conventional devices. Therefore, we found the better High-κ dielectric for LTPS TFTs that will show higher mobility, alleviated V_{TH} roll-off, improved subthreshold

swing, and increased on/off current ratio for n-channel Poly-Si TFTs.

Finally, we used the advanced materials as same as the LTPS TFTs on MOSFETs for thinner films. Then, the structure and electrical properties were discussed about various composition ratios influence.

1-5 Organization of the Thesis

In this thesis, the advanced High-κ materials were employed to fabricate the high-performance low-temperature polycrystalline silicon thin film transistors and metal-oxide-semiconductor field-effect transistors.

In Chapter 2, a new AVD system was the metal-organic chemical vapor deposition (MOCVD), dedicated to the deposition of the advanced high-κ films, was introduced briefly. Afterwards, we focused on the study in which HfO_2 HfSiOx and HfAlOx films were deposited under different pulse ratios using AVD system. Both structural and electrical characterizations of the High-κ films were presented. The effects of important deposition parameters, including the deposition temperature, the chamber pressure, oxygen gas flow, deposition frequency, and the composition adjustment, on the physical properties of as-deposited thin films were examined. Then the thermal stability of the High-κ films was studied with the help of post-deposition annealing (PDA) at high temperature.

In Chapter 3, high performance and low-temperature-compatible n-channel polycrystalline-Silicon TFTs were using High-κ materials.

In Chapter 4, high performance MOSFETs was using High-κ materials.

Finally, conclusions as well as future prospects for further research were given in Chapter 5.

Chapter2

Characterizations of High-κ Films Deposited by Atomic-Vapor Deposition

2-1 Introduction

As the dimensions of complementary metal oxide semiconductor (CMOS) devices are scaled into the nanometer regime, the gate dielectric thickness must also decrease to maintain a value of capacitance to reduce short channel effects and to keep device drive current at an acceptable level. The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates that by the years 2003-2005, the equivalent oxide thickness (EOT) of the gate dielectric decreases steadily to thinner than 1nm. Its leakage current under normal operation bias falls into the direct tunneling regime. For future generations of metal-oxide-semiconductor field-effect transistors (MOSFETs), the current gate oxide layer (SiO_2 or SiOxNy) will need to be replaced with a new material possessing a higher dielectric constant ($\kappa > \kappa_{SiO2}=3.9$).

High-κ materials are employed to increase the physical thickness of the gate insulator while maintaining the same EOT and gate capacitance, thus reduces significantly the tunneling leakage current. Although many High-κ materials are proposed to replace the conventional silicon dioxide (SiO_2) as gate insulator, Hafnium dioxide (HfO_2) is the most promising candidate for its excellent advantages, such as a suitable dielectric constant (~25) [2.1], high band-gap energy (~ 5.9eV), and suitable tunneling barrier height for both electron and hole (>1eV). However, HfO_2 is easily crystallized during deposition or following annealing processes, and crystallization increases the leakage current via grain boundaries. In order to improve the relatively low crystallization temperature of around 600°C of pure HfO_2,

alloying HfO_2 with SiO_2 and Al_2O_3 has been proposed [2.2]-[2.3]. Since their silicon or aluminum binary oxides, such as HfSiOx and HfAlOx, retain an amorphous structure after high temperature treatment, these binary oxides are now the most promising candidates to become the gate dielectric for next-generation MOSFETs [2.4]-[2.5].

Recently, High-κ materials have been investigated using several deposition techniques including physical vapor deposition (PVD) [2.4], atomic layer deposition (ALD) [2.9], plasma enhanced chemical vapor deposition (PECVD) [2.10], and jet vapor deposition (JVD) [2.11]. Although physical vapor deposition (PVD) is a simple technique for depositing new materials for evaluation in an academic organization, it may cause severe plasma damage to the electrical devices and is not preferred by industries because of poor step coverage and thickness uniformity. Chemical vapor deposition (CVD) has the advantages of uniform thickness over large substrate areas and good conformal step coverage. In contrast to ALD, it is relatively easy to dope the HfO_2 using CVD, which may be necessary for future gate dielectrics.

In this chapter, we employed the new atomic vapor deposition (AVD) system to deposit the High-κ films. The AVD system would be introduced briefly in section 2-2. Afterward, we focused on a study in which HfO_2, HfSiOx and HfAlOx films were deposited under different pulse ratios using AVD system. We present both structural and electrical characterizations of the High-κ films. First of all, the deposition and evaluation of HfO_2 thin films have been performed in section 2-3. In addition, we would hope to deposit simultaneously a stack structure to suppress interfacial layer growth. For example, a stack structure deposited two different High-κ dielectrics for a top gate oxide was HfO_2 film and a under gate oxide was HfSiOx film.

In the second part, the Si atoms incorporation into HfO_2 films were investigated various composition ratios and these results of HfSiOx films were discussed in section 2-4. Finally,

the Al atoms incorporation into HfO_2 films were investigated various composition ratios and these results of HfAlOx films were discussed in section 2-5.

2-2 Overview of Atomic-Vapor Deposition (AVD) System

Figure 2-1 illustrates the schematic diagram of the AVD system. The main parts of the AVD system contain an AIXTRON horizontal reactor and a liquid-delivery TRIJET-TM vaporizer. Metal-organic precursors are used as the source of the High-κ film and kept at room temperature in liquid phase in a stainless tank. The precursor would be injected into the vaporizer via high-speed electro-mechanical valves and the injector plays the important role to control the injection amounts of the precursors. The injected amounts of the precursors can be controlled exactly by adjusting the injection numbers and opening time of individual injectors. In our experiment, the opening times of the injectors were all fixed at 0.8 msec. The injection periods and pulses can be adjusted to control the thickness and composition of the deposited films. The liquid precursor was injected to the vertical vaporizer and transferred from liquid type to gas type immediately. The temperature of vaporizer at 170℃could be introduced according to the kind of precursors. Argon gas would be used as carrier gas to carry the vaporized precursor into the reactor through the showerhead. The process gas, oxygen in our experiment, would be heated first in gas-box and then mixed with vaporized precursors in the showerhead. Finally, the mixed gases flowed to the process reactor and film deposition would take place on the hot substrate. The deposition parameters, including deposition temperature, chamber pressure, oxygen gas flow, injection frequency and pulse numbers, could be fine-tuned to obtain the adaptable films in different device applications. Among all process parameters, the substrate temperature is the key issue to affect the quality of the as-deposited films.

2-3 Structure and Electrical Characterizations of HfO_2 and HfO_2+HfSiOx-IL

2-3.1 Experiment

HfO_2 films were deposited by liquid-injection atomic-vapor deposition (AVD) system and the liquid precursor was Hafnium(Tert-Butoxy)$_2$(mmp)$_2$, (Hf[OC(CH_3)$_3$]$_2$(mmp)$_2$, mmp：OC(CH_3)$_2$$CH_2$$OCH_3$), which was dissolved in octane to make a 0.05 M solution. The evaporation temperature of vaporizer was 170℃. Argon gas was used as the carrier gas, with a flow rate of 200 sccm, and oxygen as the oxidant with a flow rate of 1300 sccm. Substrate temperatures were 500℃, and the chamber pressures were 5 mbar. Prior to the deposition, the 6-inch silicon substrates were treated with standard RCA clean. After the cleaning process, the HF-treatment was to immerse wafers into a 100:1 diluted HF solution and then spun dry without rinse in DI water. Subsequently, wafers were put immediately into MOCVD for HfO_2 and HfO_2+HfSiOx-IL films deposition to prevent the native oxide formation. The thickness of film was controlled by the injection pulse numbers. In addition, we split two cases of HfO_2 film thickness for 40 nm (Case Ⅰ) and 4 nm (Case Ⅱ). Subsequently, case Ⅰ was post deposition annealing (PDA) at 600℃ for 24h in N_2 ambient of poly-Si TFT device and case Ⅱ was rapid temperature annealing (RTA) at 900℃ for 30sec in N_2 ambient of MOSFET device. The deposition rate was extracted by measuring the thickness of thick HfO_2 film with N&K 1500 analyzer and anther thin film with an elliposmeter.

2-3.2 Material Properties Extraction

After film deposition, post deposition annealing (PDA) was performed on all samples to investigate its impact on material properties and electrical characteristics of HfO_2 films. The fundamental physical properties of these films were analyzed by many techniques, such as

x-ray photoelectron spectrum (XPS), grazing incidence x-ray diffraction spectrum (GI-XRD) and high resolution transmission electron microscopy (HRTEM).

In addition, the electrical characteristics of the HfO_2 films were extracted from the capacitors, low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) and metal-Oxide-semiconductor field-effect transistors (MOSFETs) device. For electrical analysis, a precision impedance meter (Agilent 4284) was used for C-V measurements and a semiconductor parameter analyzer (Agilent 4156C) was used for I-V measurements.

2-3.3 Structural Characterizations of HfO_2 Films by XPS Analysis

In case Ⅰ, chemical characterizations of HfO_2 and HfO_2+HfSiOx-IL films were accomplished by x-ray photoelectron spectroscopy (XPS) utilizing monochromatic and standard Al x-ray source. The results are shown in Figures 2-2. In case Ⅱ, the results are shown in Figures 2-3. Detected elements in thin films are hafnium (Hf), oxygen (O), and carbon (C). In order to avoid the undesirable carbon contamination on the sample surfaces, XPS analyses were also performed with ion milling. Negligible damage by low energy ions during depth profiling could be assumed since no significant shift of the binding energies is observed. It is found that the relative intensity of C_{1s} signals decreases drastically after sputtering.

Then, we would check Si spectra of our samples to compare with Si standard data base to correct XPS signals. This result is reasonable due to the fact that all air-exposed materials will have a thin film deposition, composed primarily of hydroxide (i.e., alcohol-type, C-OH units). After removing this thin layer, the signals originating from purer HfO_2 can be obtained. This phenomenon shows that the composition of HfO_2 good chemical binary at the case Ⅰ and Ⅱ. We calculated the atomic area of XPS data and sensitivity factor to extract the Hafnium and oxygen atomic ratio. For HfO_2 film, Hf/O composition ratio = 1/2.3 in Table 2-1.

2-3.4 Chemical Bonding and Composition of HfO_2 Films by XRD Analysis

After annealing at 600℃ for 24h in N_2 ambient. Figures 2-4 to 2-5 show the GI-XRD spectra of the HfO_2 film and HfO2+HfSiOx-IL films, more sharp peaks, which are identified to come from monoclinic polycrystalline structure, become more visible. The dominate phases of monoclinic polycrystalline structure are (110)、(-111)、(111)、(200)、(220). Among them, the intensity of (110)、(-111)、(200)、(220) phases at one layer HfO_2 film were larger than HfO_2+HfSiOx-IL stack structure. On stack structure, the plane of (111) that density is bigger than the other phases. The HfSiO-IL aids to slightly suppress the formation of monoclinic phase in HfO_2 film.

After rapid temperature annealing at 900℃ for 30sec in N_2 ambient. Case Ⅱ in Figure 2-6 shows the monoclinic phases as same as the case Ⅰ.

The disadvantages of polycrystalline thin films in the device applications are the large leakage current, device characterization lead to degrade.

2-3.5 Structural Images of HfO_2 Films by TEM analysis

Figure 2-7 shows the images of cross-sectional TEM for the HfO_2 sample deposited at 500°C and the samples with subsequent post-deposition annealing at 600℃ for 24h in N_2 ambient, respectively. The TEM samples of poly-Si TFT devices and MOSFET devices were fabricated by focus ion beam (FIB) method.

The test structures (gate-electrode/gate-dielectric/poly-Si channel) are included in the samples of TFT devices. In part Ⅰ, the lighter contrast is near the HfO_2/poly-Si channel interface. This interfacial layer is thought to be a Si-rich Hf silicate according to many previous reports, even though this speculation can be hardly identified by any compositional analysis method. The dark contrast is purer HfO_2 film. The total physical thickness, the

individual thickness of HfO_2 film and interfacial layer are 48.9nm and 1.0nm, respectively summary in Table 2-4. By the way, other problem to the upper interface between gate-electrode and HfO_2 was rough. This could be caused by contact badly and induced leakage paths.

In part Ⅱ, Figure 2-8 shows the images of cross-sectional TEM for the stack structure. A bottom layer HfSiOx film deposited100A at 500°C. Subsequently, a upper layer HfO_2 film deposited 300A at 500℃. The samples with subsequent post deposition annealing at 600℃ for 24h in N_2 ambient. The total physical thickness, the individual thickness of HfO_2 film, HfSiOx-IL and interfacial layer are 37nm, 6.5nm and 1.0nm, respectively summary in Table 2-4. Figures 2-9 , 2-11, which were identified by TEM energy-dispersive spectroscopy (EDS) in Table 2-5 lists the element ratios of Hf, Si and O in bright (Spectrum1) and dark (Spectrum2) regions separately.

Figure 2-12 shows the images of cross-sectional TEM for case Ⅱ. The light region was an interface layer between HfO_2/Si. Physical thickness of HfO_2 film and IL were 3.3nm and 2.0nm, respectively summary in Table 2-6.

2-4 Structure and Electrical Characterizations of HfSiOx Films

2-4.1 Experiment

In this section, we focus on the deposition and evaluation of HfSiOx films. HfSiOx films were deposited by liquid-injection atomic vapor deposition (AVD) and the liquid precursors were $Hf[OC(CH_3)_3]_2(mmp)_2$ and $Si[OC(CH3)_3]_2(mmp)_2$ respectively; both are dissolved in octane to make a 0.05M solution. Form the reference process parameters for HfSiOx thin films deposition (deposition temperature = 500℃, chamber pressure = 9 mbar, oxygen gas flow = 1800 sccm, Argon gas flow = 200 sccm, injection frequency = 1Hz). It is well known

that the Si precursor usually needs higher processing temperature for the film deposition.

In order to have a more detailed surveillance over the influence of stoichiometric ratio on the properties of thin films, deposition temperature 500℃, injection frequency 1 Hz, and the pulse ratios (Hf/Si pulse ratios = 1/1, 5/1, 10/1) were executed separately.

In case Ⅱ, HfSiOx thin films deposited various pulse ratios (Hf/Si pulse ratios = 1/2, 1/1, 5/1, 10/1, 20/1, 30/1) were executed separately.

2-4.2 Material Properties Extraction

After film deposition, post deposition annealing (PDA) was also performed on all samples to investigate its impact on material properties and electrical characteristics of HfSiOx films. The fundamental physical properties of thin films were analyzed by many techniques, such as x-ray photoelectron spectrum (XPS), grazing incidence x-ray diffraction spectrum (GI-XRD), and high resolution transmission electron microscopy (HRTEM). Furthermore, the electrical properties of HfSiOx films were also extracted from the capacitors with MOS structure.

For electrical analysis, a precision impedance meter of model Agilent 4284 was used for C-V measurements and a semiconductor parameter analyzer of model Agilent 4156C was used for I-V measurements.

2-4.3 Structural Characterizations of HfSiOx Films by XPS Analysis

Figures 2-13 to 2-15 show the spectra of Hf_{4f}, Si_{2p}, and O_{1s} as a function of Hf/Si pulse ratios: Hf/Si ratio= 1/1, 5/1, 10/1. From Figure 2-13 of Hf_{4f}, we found that pure hafnium oxide shows two clearly separated peaks and becomes broader as the concentration of Si increases. These broad peaks are caused by additional created-peaks when the

concentration of Si increases. The binding energy of Hf-O bond monotonically increases with increasing concentration of Si. It means that more and more Si-O bonds are formed as the Si ratio increases, so the peak shifts to the higher binding energy. The same trends have been seen in the binding energy spectra of Si_{2p} and O_{1s} states, shown in Figures 2-14 to 2-15. Typical values of the binding energy of Si_{2p} and O_{1s} states are around 103.2 eV and 532.8 eV for silicon dioxides, respectively. As the amount of Hf increases, the peaks of Hf_{4f} shift from 17.0 eV to 16.5 eV , the peaks of Si_{2p} shift from 102.0 eV to 101.7 eV and the peaks of O_{1s} shift from 531.3 eV to 530.2 eV. These shifts mean that oxygen prefers to bind with Si than Hf, so more and more Si-O bonds are formed. When Hf/Si atomic ratio in corporation to HfSiOx films increased, we found XPS spectra of Si_{2p} intensity decreased right.

Case Ⅱ in Figures 2-17 to 2-18. Figure 2-17 shows Hf_{4f} spectra, the Hf atomic intensity decreased as Si atoms incorporations were increasing. The Hf-O bond was good and spectra were not shift obviously. Figure 2-18 shows one strong peak and one weak peak located at 102.2 eV and 97.6 eV are found in Si-bulk and HfSiOx (Hf/Si=1/2, 1/1, 5/1, 10/1, 20/1, 30/1) films. These are Si peaks coming from Si substrate in XPS measurements due to the thinner films of these two samples.

This result is also consistent with our XPS spectra described above. Nevertheless, the HfSiOx films retain amorphous structure and exhibit better thermal stability than HfO_2 film after high temperature annealing, which is beneficial for device applications. We calculated the atomic area of XPS data and sensitivity factor to extract the Hafnium and silicon atomic ratio. Si atoms incorporation into HfSiOx films, the composition ratios (77%, 66%, 40%, 25%, 12%, 9% Si) taken the place of pulse ratios (Hf/Si pulse ratios = 1/2, 1/1, 5/1, 10/1, 20/1, 30/1) in Table 2-2 and 2-3.

2-4.4 Chemical Bonding and Composition of HfSiOx Films by XRD

Analysis

Figure 2-16 shows GI-XRD spectra of HfSiOx films of case Ⅰ with Hf/Si composition ratios (25%, 40%, 66% Si) deposited at 500℃ and subsequent to PDA at 600℃ for 24h in N_2 ambient. For the spectra of these measured samples, we didn't find any signal besides substrate signal. We believe that the HfSiOx films deposited with these parameters exhibit amorphous structures which were preferred from the viewpoint of suppressing leakage current and better thermal stability during device fabrications, compared with HfO_2 films.

Figure 2-19 shows GI-XRD spectra of HfSiOx films of case Ⅱ with Hf/Si composition ratios (9%, 12%, 25%, 40%, 66%, 77% Si) deposited at 500℃ and subsequent to RTA at 900 ℃ for 30sec in N_2 ambient. We found crystalline phases as less Si incorporations of 40%, the dominant phase were monoclinic and orthorhombic structures.

2-4.5 Structural Images of HfSiOx Films by TEM Analysis

Figure 2-20 shows the images of cross-sectional TEM for the as-deposited HfSiOx film with Hf/Si composition ratio (66% Si) deposited at 500℃, the sample with subsequent post deposition annealing at 600℃ for 24h in N_2 ambient, respectively. Both of top and bottom interfaces were smooth for HfSiOx film which could be better electrical properties. The individual thickness of HfSiOx films and interfacial layer are 34.6nm and 1.0nm respectively summary in Table 2-4.

Figure 2-21 shows the images of cross-sectional TEM for case Ⅱ. The light region was an interface layer between HfSiOx/Si. Physical thickness of HfSiOx film was 3.0nm and interfacial layer was 1.6nm. Summary of thickness was in Table 2-6.

2-5 Structure and Electric Characterizations of HfAlOx Films

2-5.1 Experimental

In this section, we focus on deposition and evaluation of HfAlOx films. HfAlOx films were deposited by liquid-injection atomic vapor deposition (AVD) and the liquid precursors were $Hf[OC(CH_3)_3]_2(mmp)_2$ and $Al[OCH(CH_3)_2]_3$. Both precursors were dissolved in octane to make a 0.05M solution. Form the process parameters for HfAlOx thin films deposition (deposition temperature = 500℃, chamber pressure = 5 mbar, oxygen gas flow = 1300 sccm, Argon gas flow =200 sccm, injection frequency = 1Hz). In order to have a more detailed surveillance over the influence of stoichiometric ratio on the properties of thin films, deposited pulse ratios (Hf/Al pulse ratios = 1/1, 5/1, 10/1) were executed separately. After film deposition, post deposition annealing (PDA) was also performed on all samples to investigate its impact on material properties and electrical characteristics of HfAlOx films.

In case Ⅱ, HfAlOx thin films deposited various pulse ratios (Hf/Al pulse ratios = 1/2, 1/1, 5/1, 10/1) were executed separately.

2-5.2 Material Properties Extraction

The fundamental physical properties of thin films were analyzed by many techniques, such as x-ray photoelectron spectrum (XPS), grazing incidence x-ray diffraction spectrum (GI-XRD), and high resolution transmission electron microscopy (HRTEM). Furthermore, the electrical properties of HfAlOx films were also extracted from the capacitors with MOS structure. For electrical analysis, a precision impedance meter of model Agilent 4284 was used for C-V measurements and a semiconductor parameter analyzer of model Agilent 4156C was used for I-V measurements.

2-5.3 Structural Characterizations of HfAlOx Films by XPS Analysis

Figures 2-22 to 2-24 show the spectra of Hf_{4f}, Al_{2p}, and O_{1s} as a function of Hf/Al composition ratios: Hf/Al ratio= 1/1, 5/1, 10/1. Typical values of the binding energy of Al_{2p} and O_{1s} states are around 74.4 eV and 532.8 eV for aluminum oxides, respectively. From Figures 2-22 to 2-23 show as the amount of Hf increases, the peaks of Hf_{4f} weren't shift for 16.5 eV , the peaks of Al_{2p} shift from 73.3 eV to 73.6 eV and the peaks of O_{1s} shift from 529.9 eV to 530.0 eV. As Hf/Al composition ratios in corporation to HfAlOx films increased, we found XPS spectra of Al_{2p} intensity decreased.

As same as the XPS spectra for case Ⅱ, Figures 2-26 to 2-27 show the spectra of Hf_{4f} and Al_{2p} as a function of Hf/Al composition ratios: Hf/Al ratio= 1/2, 1/1, 5/1, 10/1.

This result is also consistent with our XPS spectra described above. We calculated the atomic area of XPS data and sensitivity factor to extract the Hafnium and aluminum composition ratio, Al atoms incorporation into HfAlOx films, the composition ratios (63%, 40%, 12%, ~7% Al) taken the place of pulse ratios (Hf/Al pulse ratios = 1/2, 1/1, 5/1, 10/1) in Table 2-2 and 2-3.

2-5.4 Chemical Bonding and Composition of HfAlOx Films by XRD Analysis

Figure 2-25 shows GI-XRD spectra of HfAlOx films with Hf/Al composition ratios (~7%, 12%, 40% Al) deposited at 500℃ and subsequent to PDA 600℃ for 24h in N_2 ambient. For the spectra of these measured samples, we found crystallization phases for less Al incorporation of 40% Al into HfAlOx film. We saw that as Al atoms increased incorporation into HfAlOx films, the crystallization temperature would to be raised [2.12]. For 12% Al content into HfAlOx film, the cubic-like phase had to get data bases. For ~7% Al

content into HfAlOx film, we got the monoclinic and an amount of small cubic-like phases.

We considered two cases of the dielectric constant for HfAlOx films with Hf/Al composition ratios (~7% and 12% Al). We employ the Clausius-Mossotti relation for that analysis [2.13].

The Clausius-Mossotti relation is expressed as follows:

$$\kappa = 1 + (8\pi\alpha_m/3V_m)/(1 - 4\pi\alpha_m/3V_m) \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Here, κ, α_m and V_m are the κ-value, molar polarizability and the molar volume, respectively. In Eq. (1), α_m increase or V_m shrinkage bring about the κ-value enhancement. Although it is difficult to determine the accurate α_m value experimentally, V_m values can be evaluated from the lattice parameters determined by XRD. The α_m value concern about High-κ dielectric nature and the V_m value concern about deposition system, surface treatment, post deposition annealing temperature…etc that maybe influence phase structure.

There were two ways to raise dielectric constant (κ) for Eq. (1). The molar polarizability (α_m) could to be increased or the molar volume (V_m) might decrease. When we discussed the same dielectric, we only considered about the V_m of various conditions. We would like to discuss the κ-values impact on some of the lattices, ex. cubic, tetragonal, monoclinic, orthorhombic…etc. The highest κ-value is cubic phase and if the phase spectra are others, and the κ-value could reduce.

2-5.5 Structural Images of HfAlOx Films by TEM Analysis

Fig. 2-29 shows the images of cross-sectional TEM for the as-deposited HfAlOx film with Hf/Al composition ratio (~7% Al) deposited at 500℃, the samples with subsequent rapid temperature annealing at 900℃ for 30sec in N_2 ambient, respectively. The total physical

thickness, the individual thickness of HfAlOx films was 3.6nm and interfacial layer was 1.7nm. Summary of thickness were in Table 2-6.

Table 2-1

Recipes of HfO_2, HfSiOx and HfAlOx

in Aixtron atomic-vapor deposition (AVD) system.

Recipe	Chamber /LDS	Subsector	Pressure	O_2 Flow (sccm)	Ar Flow (sccm)
HfO_2	170℃	500℃	5 mbar	1300	200
HfSiOx	170℃	500℃	9 mbar	1800	200
HfAlOx	170℃	500℃	5 mbar	1300	200

Table 2-2

Summary of XPS extracted composition ratio of

HfO_2、HfSiOx、HfAlOx films,

Hafnium (Hf)、Silicon (Si)、Oxygen (O)、Aluminum (Al)

deposited at 500℃ and PDA at 600℃, 24 h

HK TFT 40nm condition	Pulse Ratio	Composition Ratio	Si or Al content
01.HfO_2	Hf/O = 1/2	1/2.3	—
02.HfO_2+HfSiOx	Hf/O = 1/2	1/2.3	66% (IL)
03.HfSiOx	Hf/Si = 10/1	1/0.33	25%
04.HfSiOx	Hf/Si = 5/1	1/0.67	40%
05.HfSiOx	Hf/Si = 1/1	1/2	66%
06.HfAlOx	Hf/Al = 10/1	1/0.07	~7%
07.HfAlOx	Hf/Al = 5/1	1/0.14	12%
08.HfAlOx	Hf/Al = 1/1	1/0.67	40%

Table 2-3

Summary of XPS extracted composition ratio of

HfO_2、HfSiOx、HfAlOx films,

Hafnium (Hf)、Silicon (Si)、Oxygen (O)、Aluminum (Al)

deposited at 500℃ and RTA at 900℃, 30s

OM HK 4nm Condition	Pulse Ratio	Composition Ratio	Si or Al content
01.HfO_2	Hf/O = 1/2	1/2.3	—
02.HfSiOx	Hf/Si = 30/1	1/0.10	9%
03.HfSiOx	Hf/Si = 20/1	1/0.14	12%
04.HfSiOx	Hf/Si = 10/1	1/0.33	25%
05.HfSiOx	Hf/Si = 5/1	1/0.67	40%
06.HfSiOx	Hf/Si = 1/1	1/2	66%
07.HfSiOx	Hf/Si = 1/2	1/3.3	77%
08.HfAlOx	Hf/Al = 10/1	1/0.07	~7%
09.HfAlOx	Hf/Al = 5/1	1/0.14	12%
10.HfAlOx	Hf/Al = 1/1	1/0.67	40%
11.HfAlOx	Hf/Al = 1/2	1/1.67	63%

Table 2-4

Summary of thickness for the samples

deposited at 500℃ and PDA at 600℃, 24h

HK TFT 40nm Condition	Physical thickness (A) (TEM)	Thickness of High-k/interfacial layer (A)
01.HfO_2	504	489/15
02.HfO_2+HfSiOx-IL (66% Si)	445	370/65/10
03.HfSiOx (66% Si)	356	346/10

Table 2-5

Summary of TEM-EDX composition ratio of HfO_2+HfSiOx-IL stack structure,

Hafnium (Hf)、Silicon (Si)、Oxygen (O)

deposited at 500℃ and PDA at 600℃, 24h

	Hf	Si	O	Composition Ratio
HfO_2 (Top layer)	31.58%	18.14%	50.27%	Hf/O = 1/1.6
HfSiOx-IL (66% Si) (Bottom layer)	7.93%	45.98%	46.09%	Hf/Si = 1/5.8

Table 2-6

Summary of thickness for the samples

deposited at 500℃ and rapid temperature annealing at 900℃, 30s

OM HK 4nm Condition	Physical thickness (A) (TEM)	Thickness of High-k/interfacial layer (A)
HfO_2	53	33/20
HfSiOx (25% Si)	46	30/16
HfAlOx (~7% Al)	53	36/17

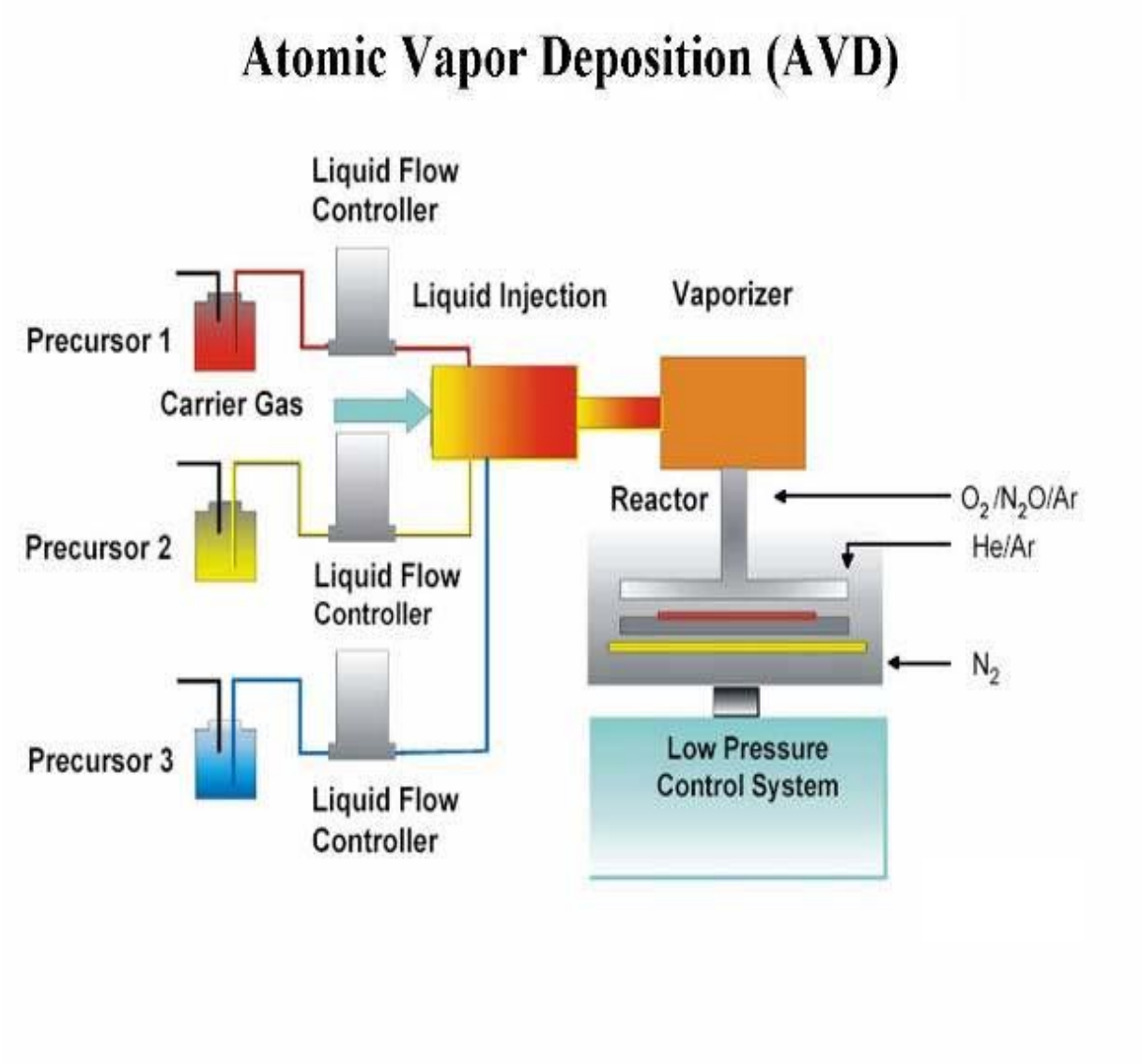
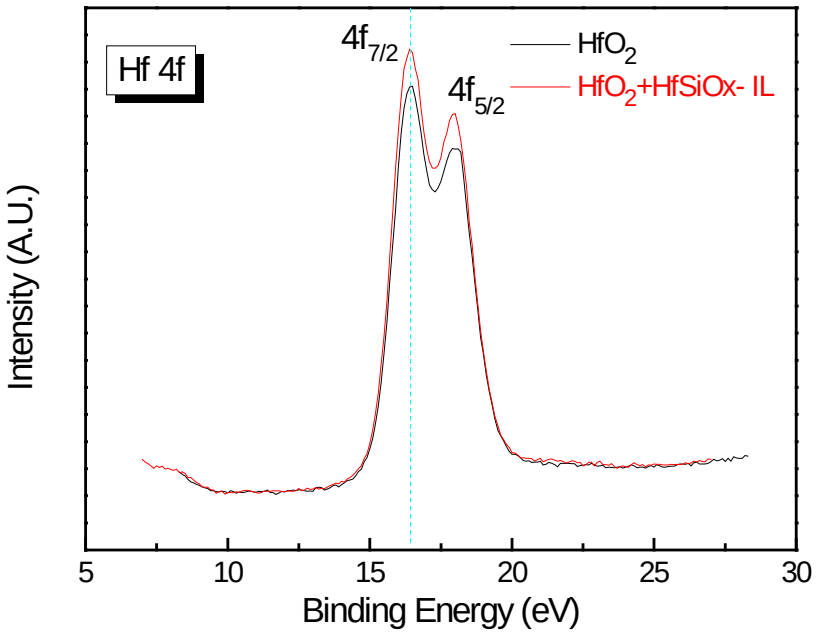
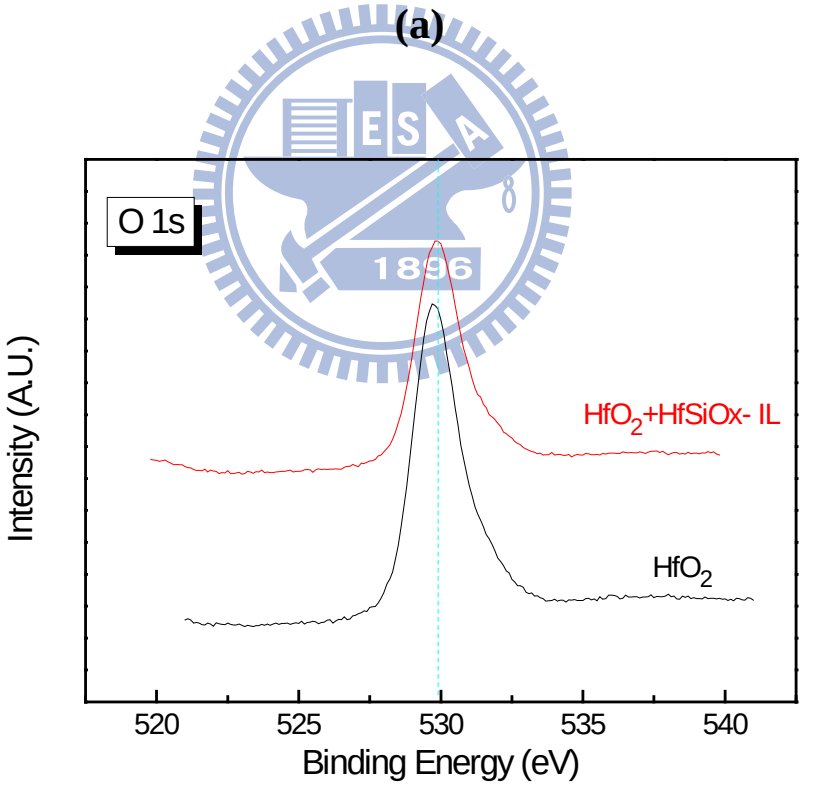


Figure 2-1 Schematic diagram of atomic-vapor deposition (AVD) system.

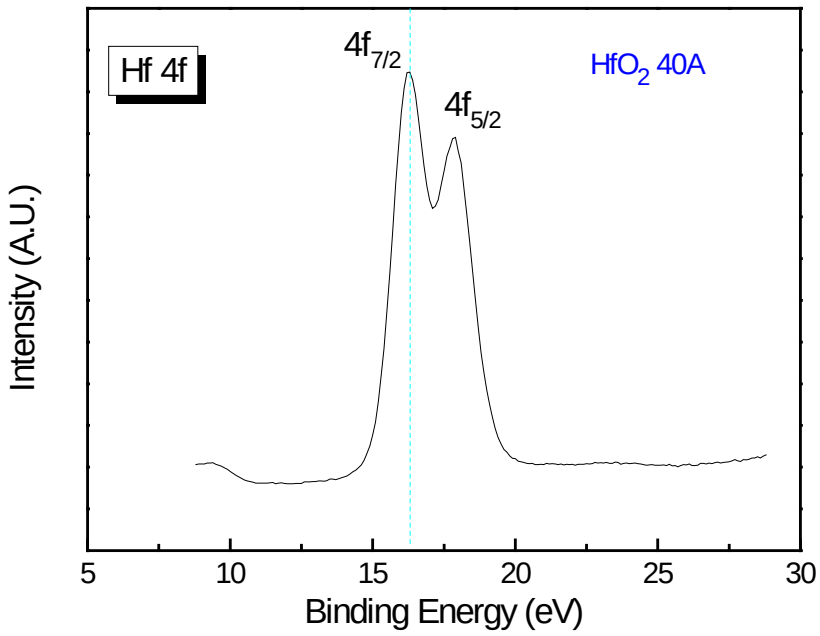


(a)

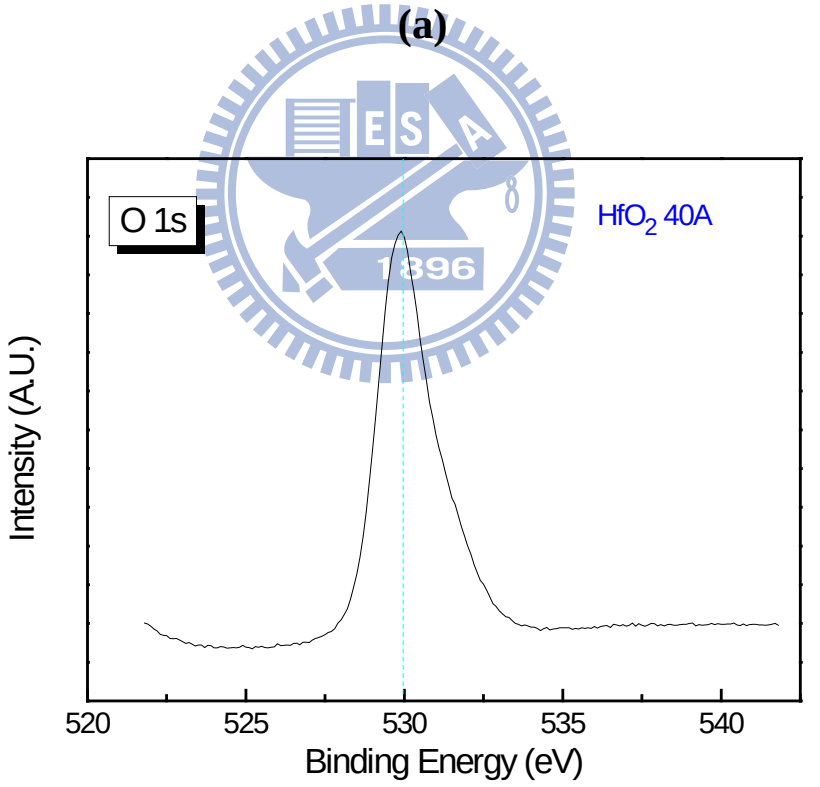


(b)

Figure 2-2 XPS data of (a)Hf_{4f} spectra, and (b)O_{1s} spectra for HfO_2 and HfO_2+HfSiOx-ILfilms deposited 400A by AVD.



(a)



(b)

Figure 2-3 XPS data of (a)Hf_{4f} spectra, and (b)O_{1s} spectra for HfO_2 film deposited 40A by AVD.

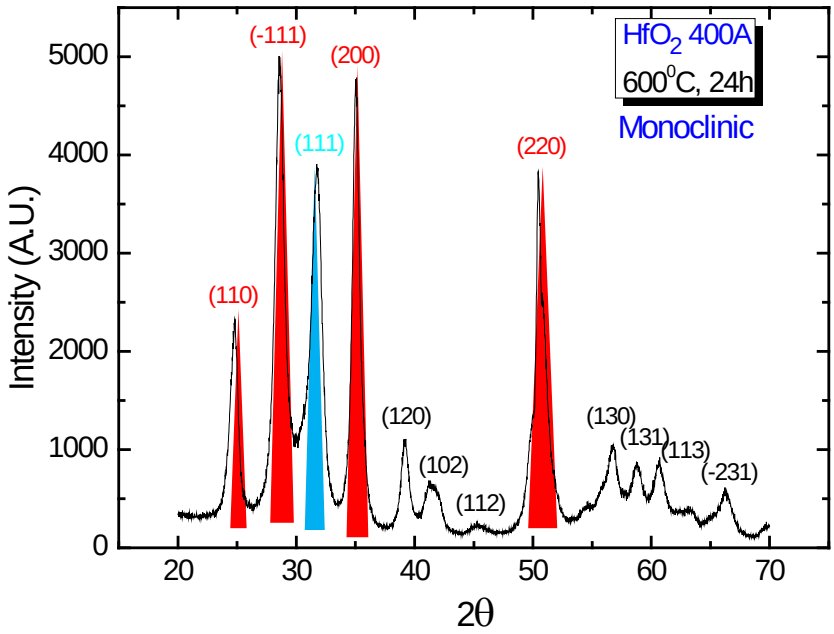


Figure 2-4 XRD spectra of HfO_2 film deposited 400A by AVD. PDA 600℃ and 24h in N_2 ambient.

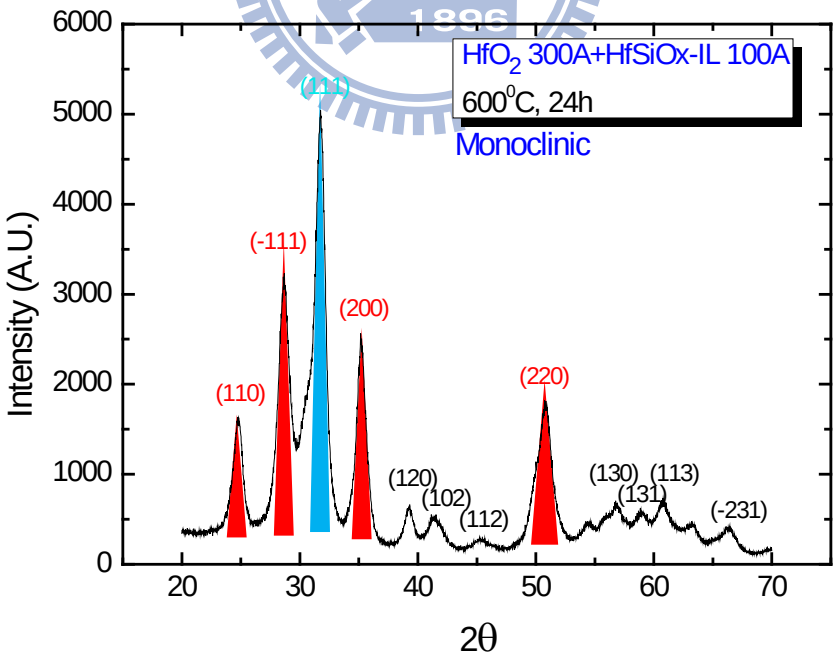


Figure 2-5 XRD spectra of HfO_2+HfSiOx-IL films deposited 300A and 100A by AVD. PDA 600℃ and 24h in N_2 ambient.

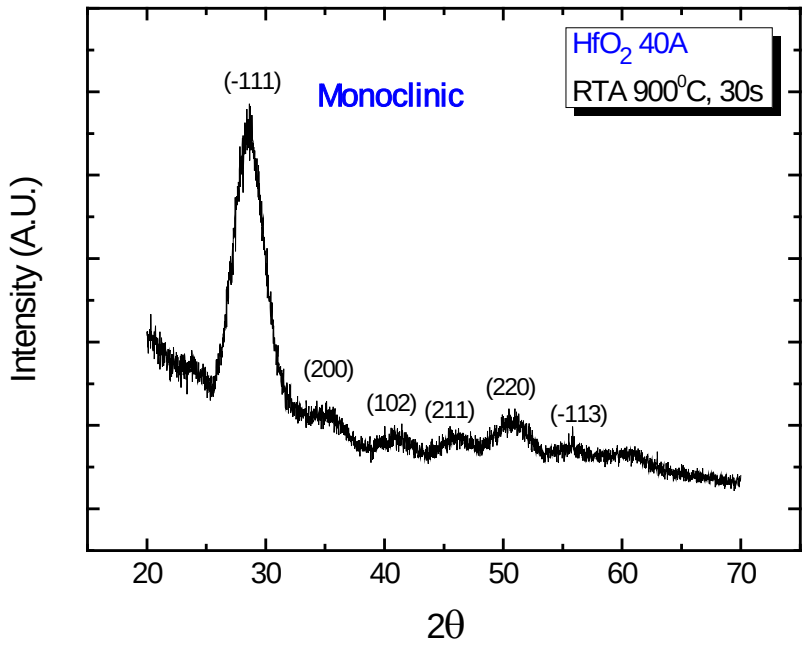


Figure 2-6 XRD spectra of HfO_2 film deposited 40A by AVD. RTA 900℃ and 30s in N_2 ambient.

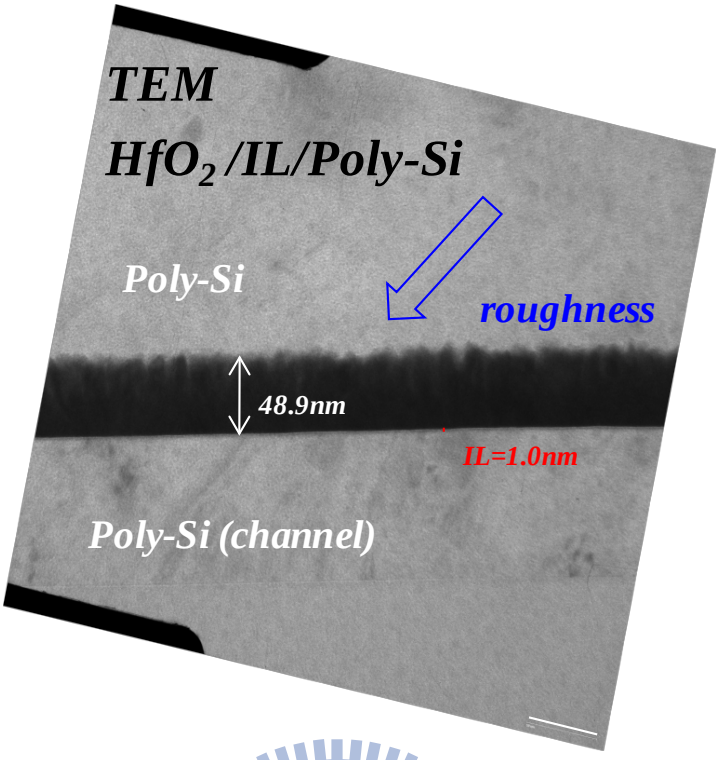


Figure 2-7 Cross-sectional TEM images of TFTs incorporating HfO_2 dielectric. The thickness of HfO_2 and IL are around 48.9nm and 1.5nm, respectively.

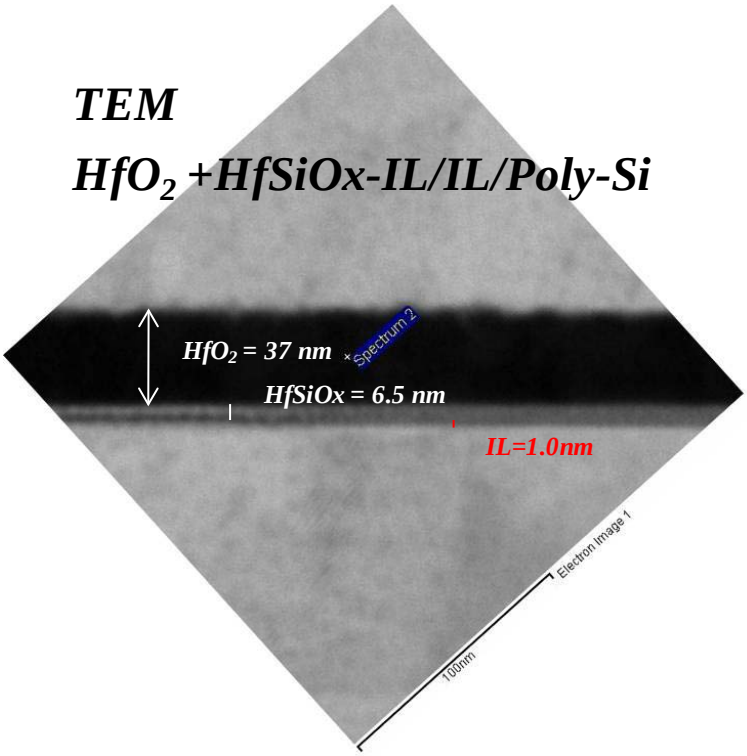


Figure 2-8 Cross-sectional TEM images of TFTs incorporating two dielectrics of HfO_2+HfSiOx-IL. The thickness of HfO_2, HfSiOx-IL and IL are around 37nm, 6.5nm and 1.0nm, respectively. (Spectrum 2)

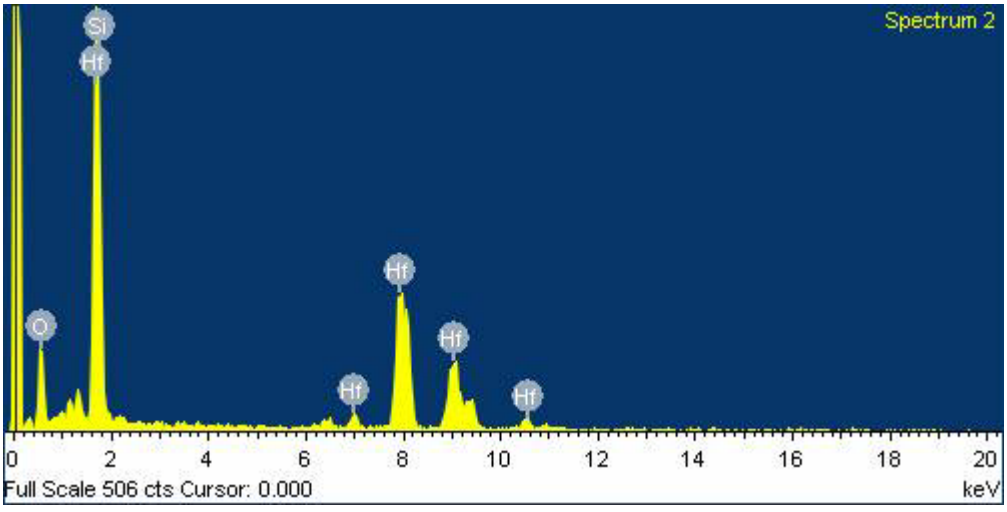


Figure 2-9 TEM-EDX for composition ratios of Hf and Si from HfO_2 dielectric on top structure of Spectrum 2.

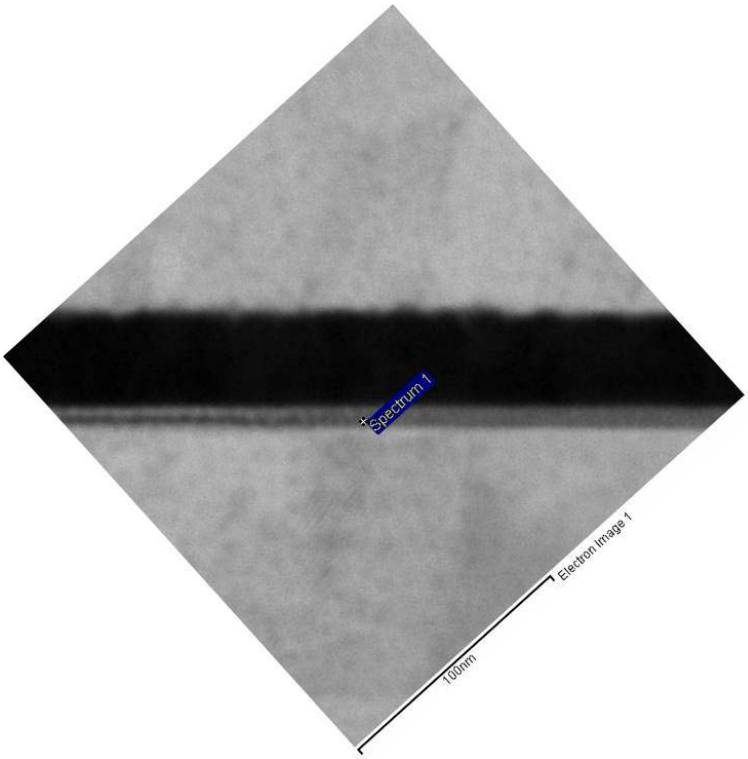


Figure 2-10 Cross-sectional TEM images of TFTs incorporating two dielectric of HfO_2+HfSiOx-IL film. The thickness of HfO_2, HfSiOx-IL and IL are around 37nm, 6.5nm and 1.0nm, respectively. (Spectrum 1)

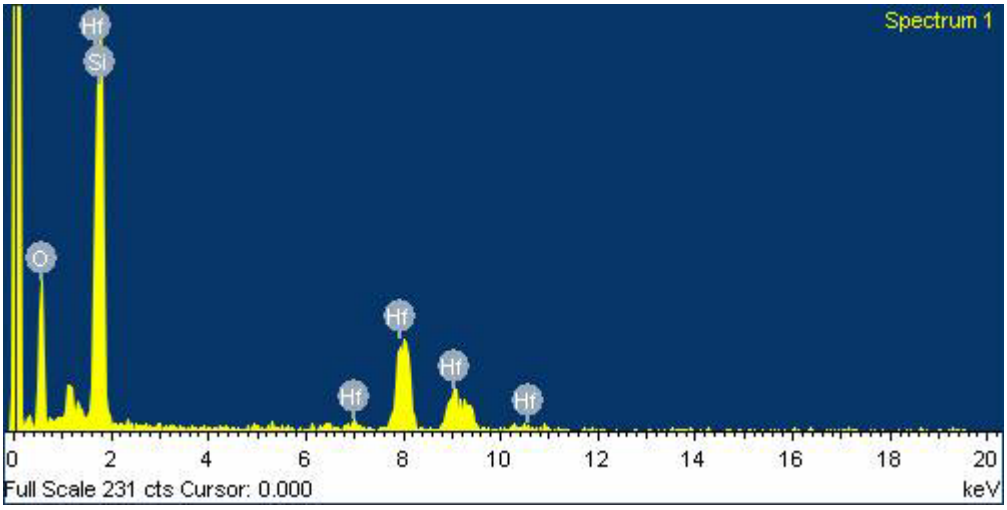


Figure 2-11 TEM-EDX for composition ratios of Hf and Si from HfSiOx-IL dielectric on bottom structure of Spectrum1

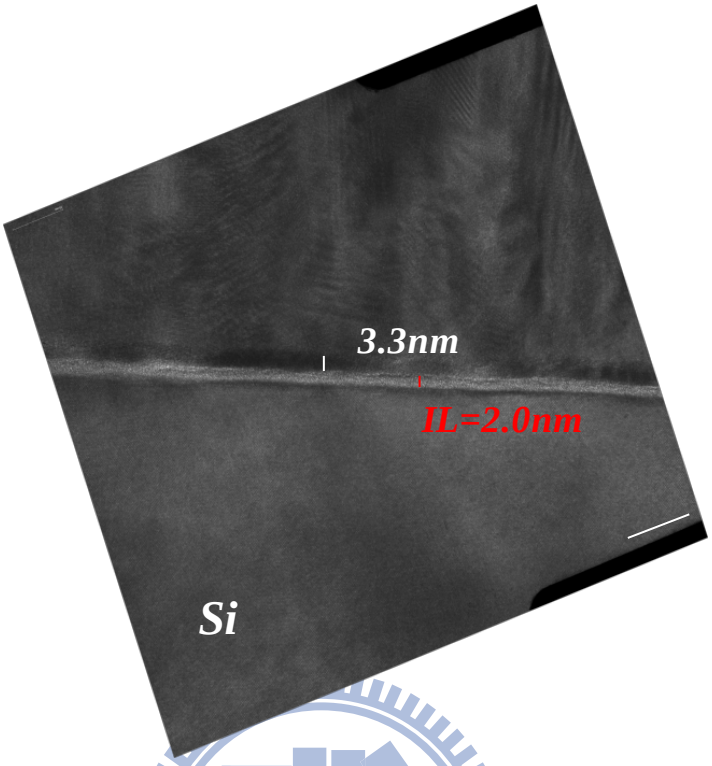


Figure 2-12 Cross-sectional TEM images of TFTs incorporating HfO_2 dielectric. The thickness of HfO_2 and IL are around 3.3nm and 2.0nm, respectively.

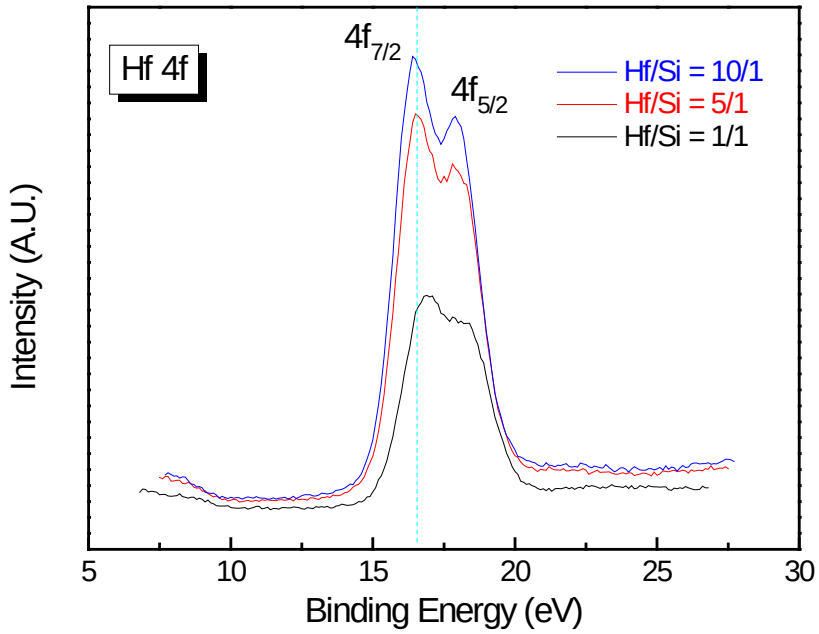


Figure 2-13 XPS spectra of Hf_{4f} for HfSiOx films deposited by AVD at various Hf/Si composition ratios on Si (100).

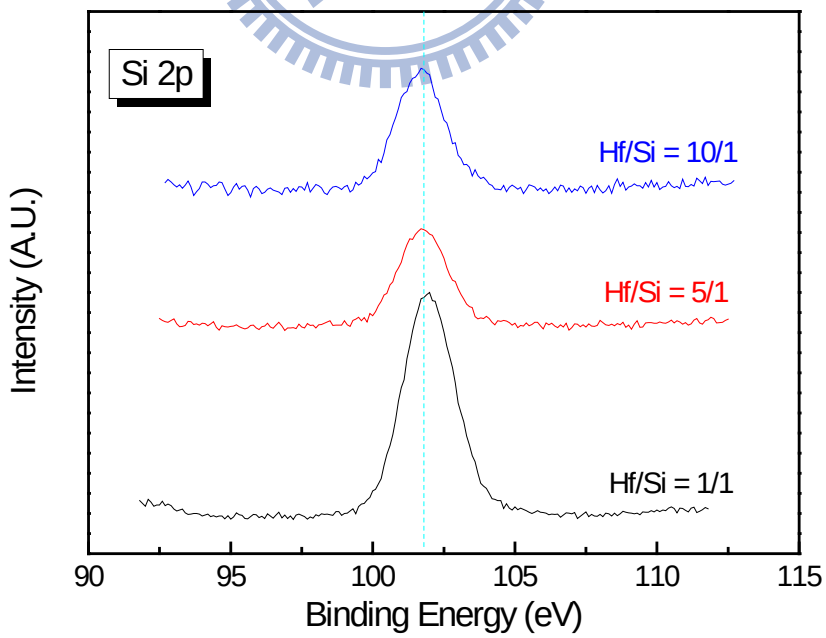


Figure 2-14 XPS spectra of Si_{2p} for HfSiOx films deposited by AVD at various Hf/Si composition ratios on Si (100).

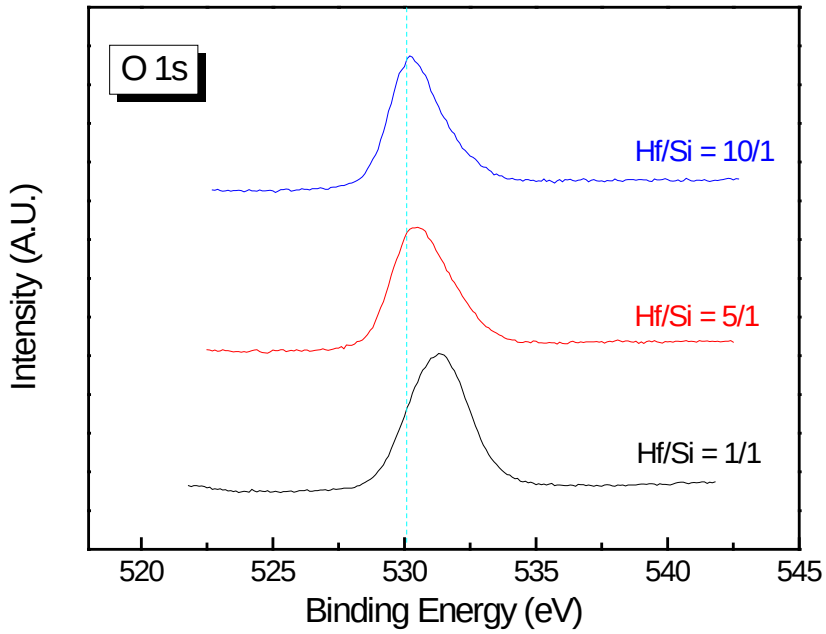


Figure 2-15 XPS spectra of O_{1s} for HfSiOx films deposited by AVD at various Hf/Si composition ratios on Si (100).

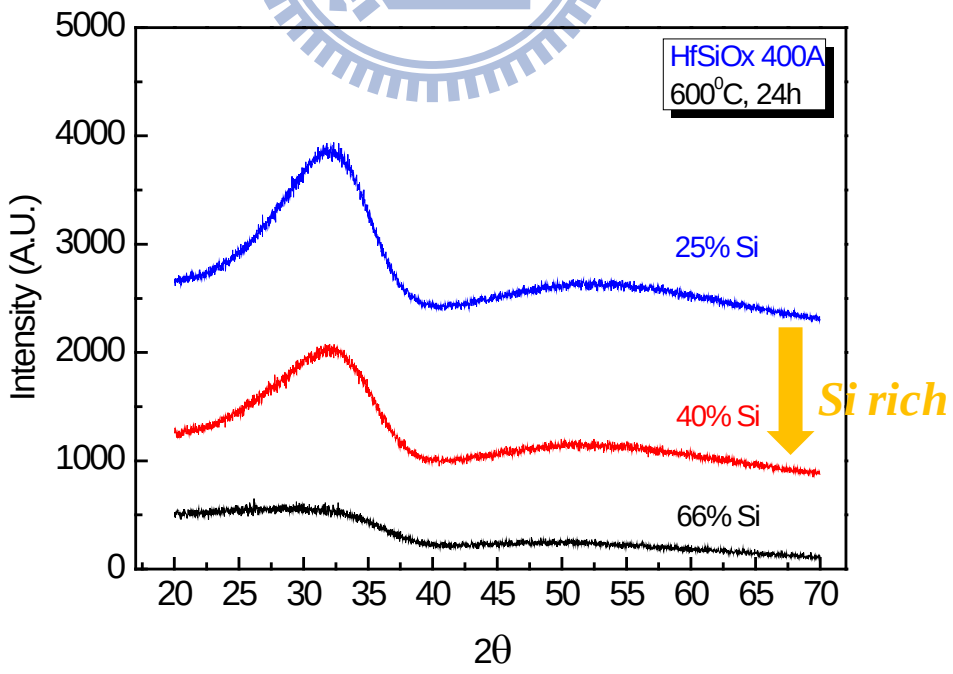


Figure 2-16 XRD spectra of HfSiOx films deposited by AVD. PDA 600℃ and 24h in N_2 ambient.

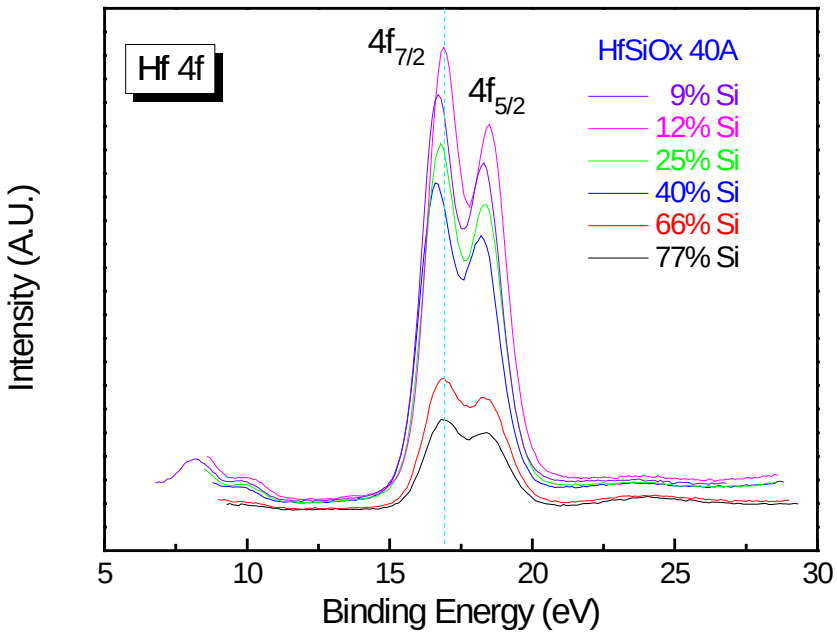


Figure 2-17 XPS spectra of Hf_{4f} for HfSiOx films deposited 40A by AVD at various Hf/Si composition ratios on Si (100).

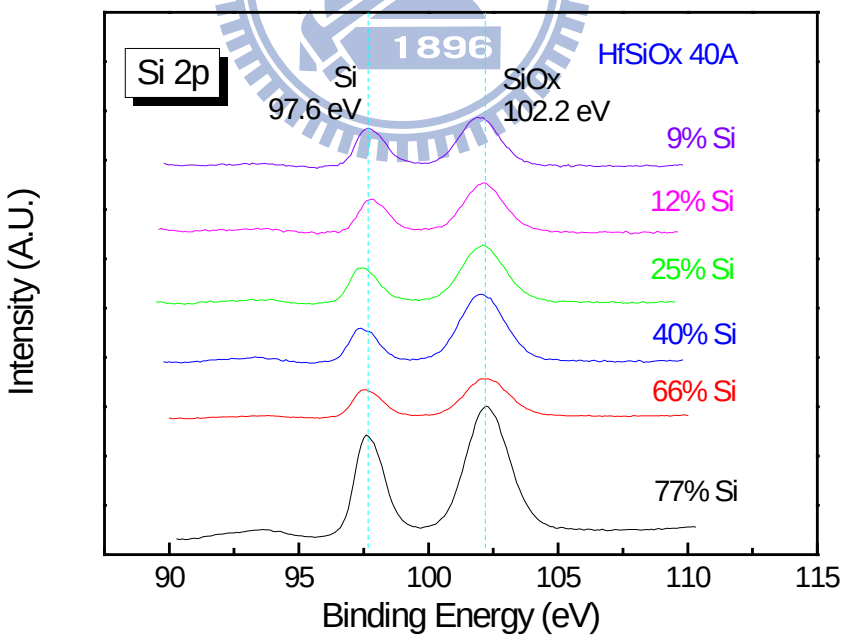


Figure 2-18 XPS spectra of Si_{2p} for HfSiOx films deposited 40A by AVD at various Hf/Si composition ratios on Si (100).

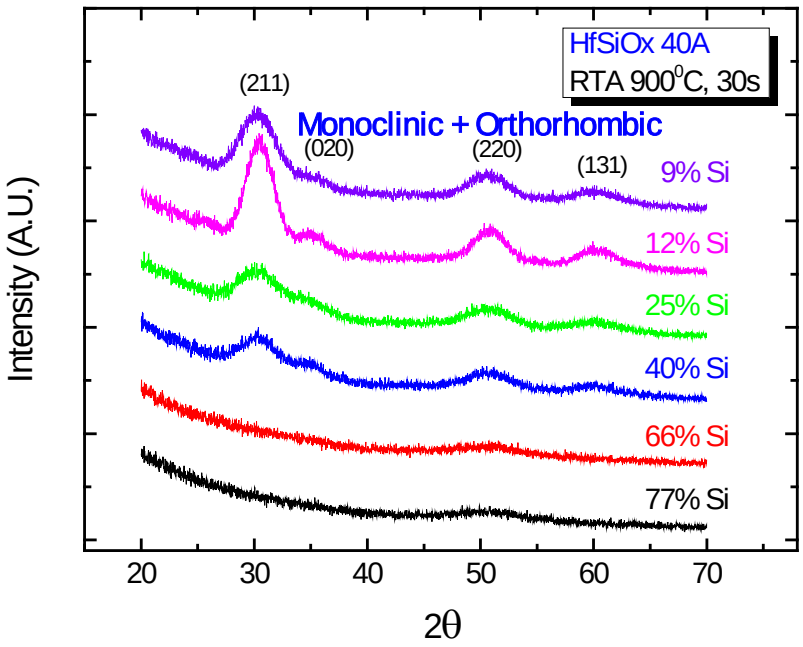


Figure 2-19 XRD spectra of HfSiOx films deposited 40A by AVD. RTA 900℃ and 30sec in N_2 ambient.

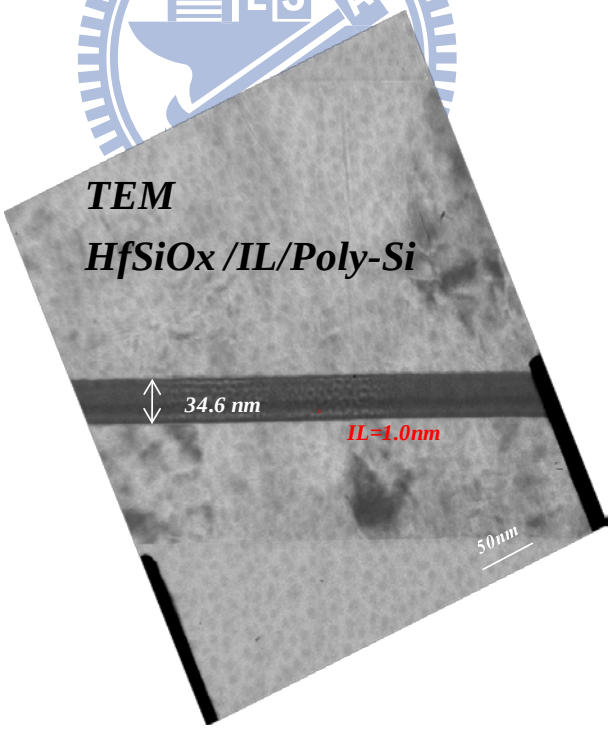


Figure 2-20 Cross-sectional TEM images of TFTs incorporating HfSiOx dielectric. The thickness of HfSiOx and IL are around 34.6nm and 1.0nm, respectively.

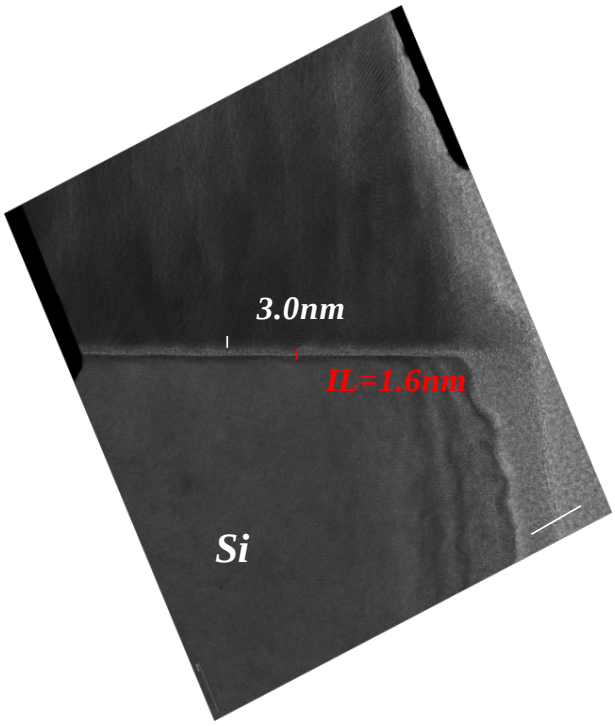


Figure 2-21 Cross-sectional TEM images of TFTs incorporating HfSiOx dielectric. The thickness of HfSiOx and IL are around 3.0nm and 1.6nm, respectively.

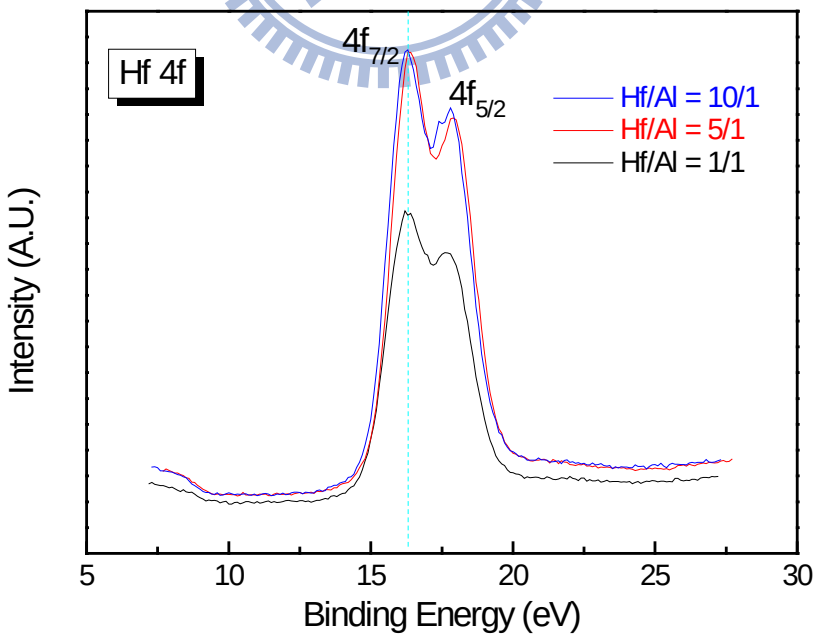


Figure 2-22 XPS spectra of Hf_{4f} for HfAlOx films deposited by AVD at various Hf/Al composition ratios on Si (100).

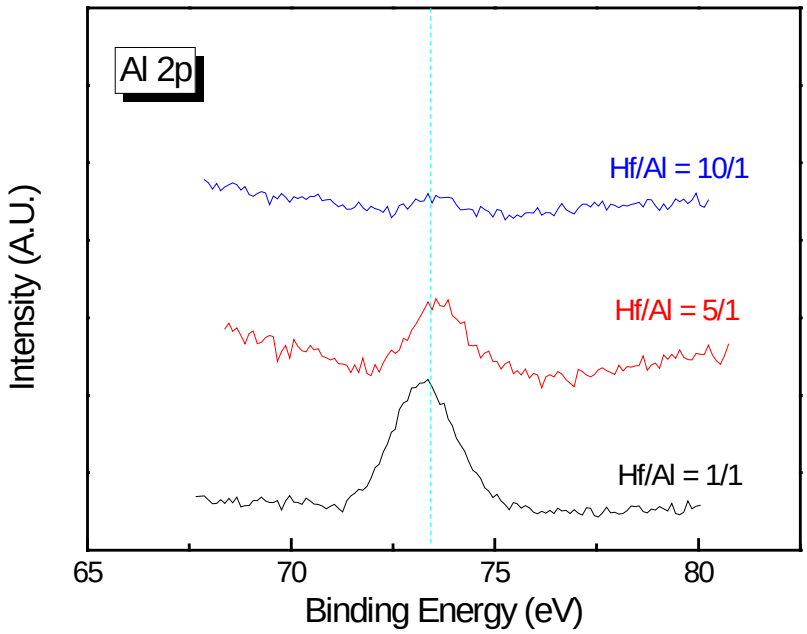


Figure 2-23 XPS spectra of Al_{2p} for HfAlOx films deposited by AVD at various Hf/Al composition ratios on Si (100).

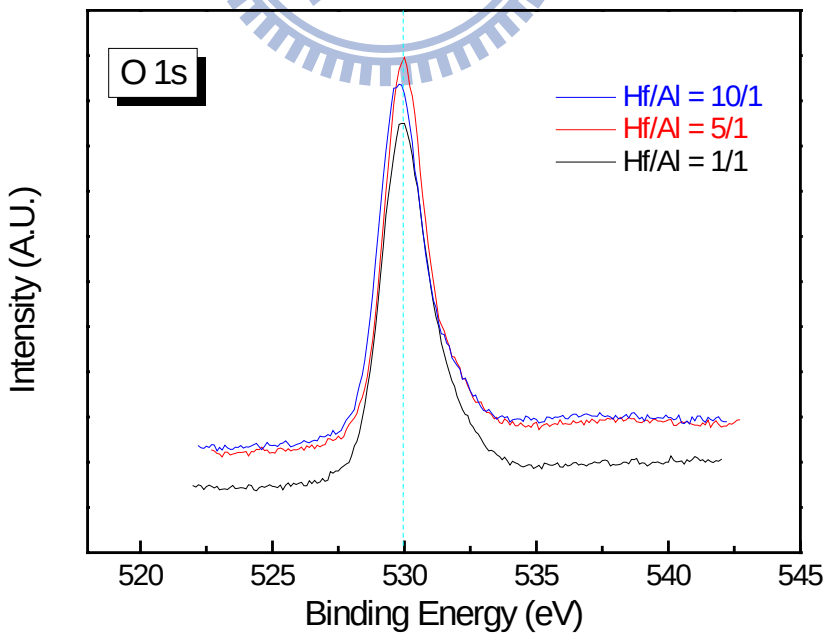


Figure 2-24 XPS spectra of O_{1s} for HfAlOx films deposited by AVD at various Hf/Al composition ratios on Si (100).

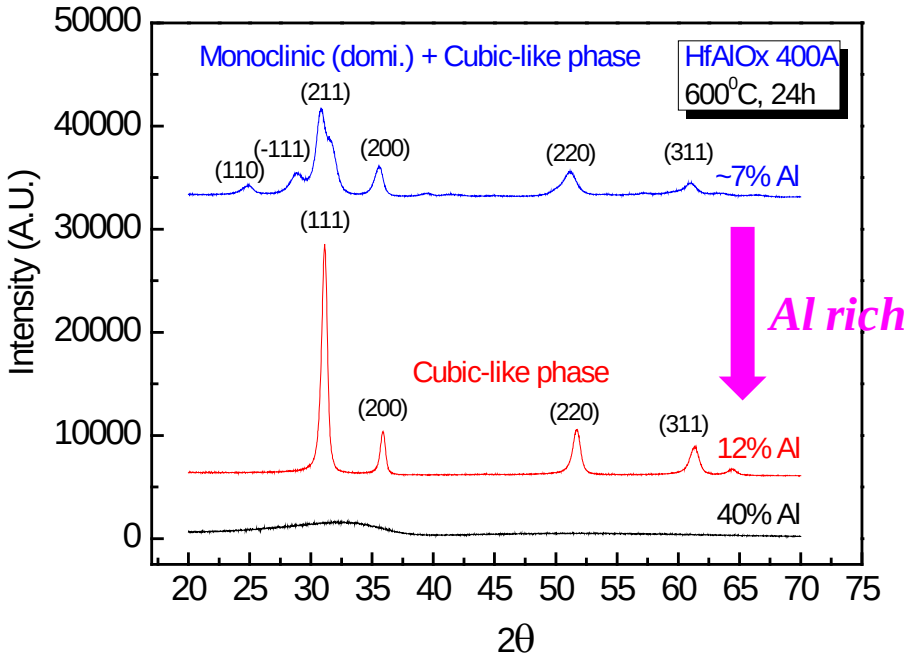


Figure 2-25 XRD spectra of HfAlOx films deposited by AVD. PDA 600℃ and 24h in N_2 ambient.

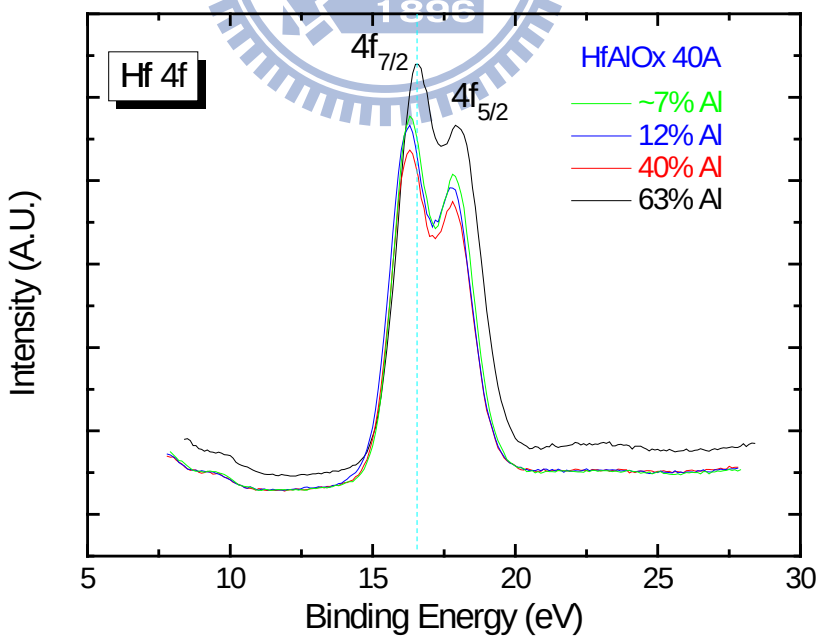


Figure 2-26 XPS spectra of Hf_{4f} for HfAlOx films deposited 40A by AVD at various Hf/Al composition ratios on Si (100).

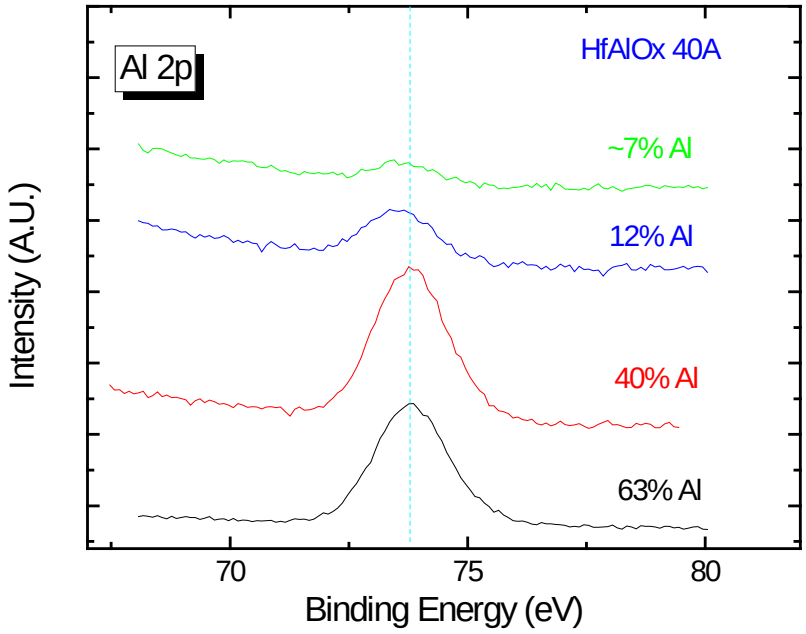


Figure 2-27 XPS spectra of Al_{2p} for HfAlOx films deposited 40A by AVD at various Hf/Al composition ratios on Si (100).

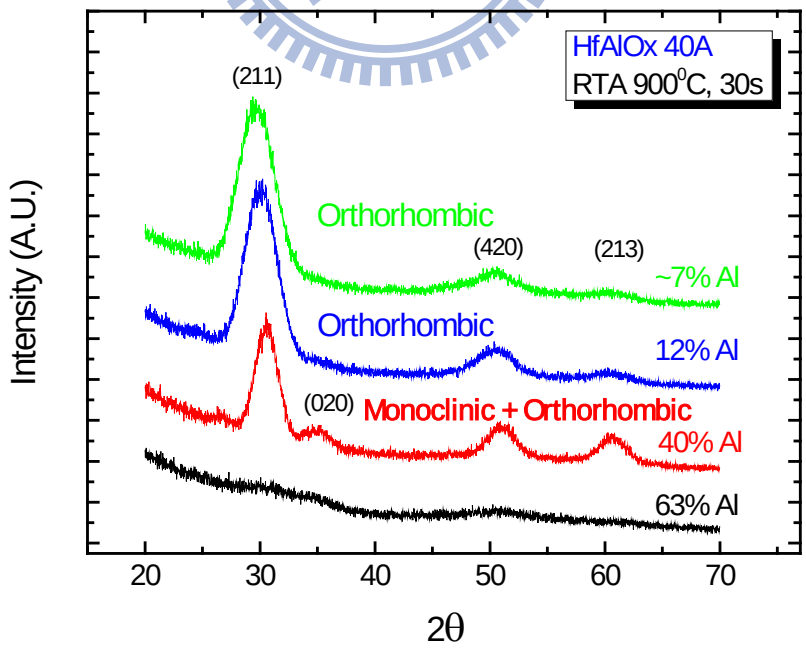


Figure 2-28 XRD spectra of HfAlOx films deposited 40A by AVD. RTA 900℃ and 30sec in N_2 ambient.

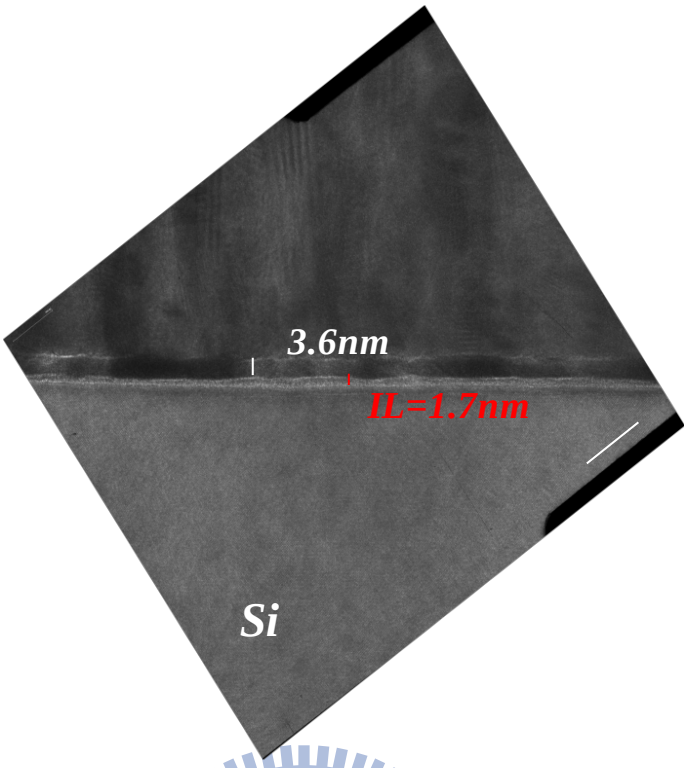


Figure 2-29 Cross-sectional TEM images of TFTs incorporating HfAlOx dielectric. The thickness of HfAlOx and IL are around 3.6nm and 1.7nm, respectively.

Chapter3

High-Performance and Low-Temperature-Compatible N-Channel Polycrystalline-Silicon TFTs Using High-κ Material

3-1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are employed extensively in active-matrix liquid crystal displays because of their superior performance [3.1]. Recently, the practicability of integrating the entire system on the panel (SOP) has been investigated vigorously [3.2]. This goal requires that the display driving circuits contain high performance TFTs capable of operating at lower voltages while delivering higher driving currents. Although scaling down the gate oxide can increase the driving current of a TFT, it leads inevitably to a higher gate leakage current because of the decreased quality of the low-temperature-deposited gate dielectrics [3.3]. To maintain the physical dielectric thickness while increasing the gate capacitance, several new High-κ materials have been proposed, including Al_2O_3, Ta_2O_5, and HfO_2 dielectrics[3.4]–[3.6]. Because Al_2O_3 films exhibit relatively low values of κ (~ 9) and excess fixed charge, the TFT performance is not improved sufficiently for application [3.7]. The narrow band gap of Ta_2O_5 dielectric implies that a thicker film is necessary to reduce the gate leakage current of TFTs [3.8], which limits the increase in gate capacitance. Recently, hafnium dioxide (HfO_2) has been applied to TFTs because of its higher value of κ (14~20) and sufficiently wide band gap [3.6]. Although poly-Si TFTs incorporating HfO_2 as the gate dielectric exhibit superior performance in many respects, several issues remain problematic: e.g., the higher gate leakage current arising from

poly-crystalline HfO_2 films and the degraded mobility arising from additional scattering.

In this chapter, we focus on the depositions of thicker High-κ films (~40nm) and present both structural and electrical characterization of these High-κ films. And then, we describe a systematic study of the electrical properties of low-temperature-compatible p-channel poly-Si thin-film transistors (TFTs) using HfO_2, HfSiOx and HfAlOx High-κ gate dielectrics. We found that the transistors containing HfSiOx gate dielectric exhibit higher values of Ion/Ioff ratio and μ_{FE} and smaller values of subthreshold swing (S.S.) and V_{TH}, which compared with deposited-HfO_2 dielectric.

Then, due to some of better benefits of HfSiOx gate dielectric, ex. lower gate leakage current density (Jg), higher I_{on}/I_{off} current ratio…etc. We tried to stack two different dielectrics that discussed electrical properties with others High-κ materials. We would choose 66% Si incorporation into HfSiOx film as bottom layer and HfO_2 film top of HfSiOx film.

3-2 High-κ Films Deposition and Device Fabrications

Firstly, the thicker High-κ films (~40nm) were deposited through atomic vapor deposition (AVD) system. From the experience of thin High-κ film deposition, we use the substrate temperature as 500℃ and oxygen gas flow as 1300 sccm for HfO_2 and HfAlOx films. Another, we use the substrate temperature as 500℃ and oxygen gas flow as 1800 sccm for HfSiOx film. The $Hf[OC(CH_3)_3]_2(mmp)_2$ precursor, $Si[OC(CH_3)_3]_2(mmp)_2$ precursor, $Al[OCH(CH3)_2]_3$ precursor and oxygen gas were employed as Hf, Si, and O sources, respectively. The structural characterizations of these films would be analyzed by various measurements, such as, x-ray photoelectron spectrum (XPS), x-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM). And then, self-aligned top-gate n-channel poly-Si TFTs were fabricated and the procedure flow was illustrated in Figure 3-1.

First of all, a 550nm-thick thermal oxide was grown on Si wafers in a furnace to simulate the glass substrate. Next, a 100nm-thick amorphous silicon layer was deposited through the dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 hour in N_2 ambient to induce the crystallization of poly silicon. Individual active regions were then patterned by lithography and defined by dry etching. After RCA cleaning, various gate dielectrics (with thickness of 40nm) were deposited. Specifically, HfO_2, HfSiOx and HfAlOx films were deposited through atomic vapor deposition (AVD) using an AIXTRON Tricent system at a substrate temperature of 500°C. All of the wafers were then subjected to deposition of a 25nm-thick amorphous silicon layer, which served as the gate electrode, through LPCVD at 550°C. The gate electrodes were patterned and the source, drain, and gate regions were doped through self-aligned phosphorous ion implantation (dosage: 5×10^{15} ions/cm^2; energy: 36 keV). After formation of the source and drain, the dopant was activated at 600°C for 24 hour in N_2 ambient. Finally, contact holes were opened and 550nm Ai-Si-Cu alloy was deposited and defined. Wafers were then sintered at 400℃ for 30 min in forming gas to complete the fabrication.

Capacitors containing High-κ dielectrics were fabricated simultaneously through the use of a shadow mask to allow measurement of dielectric constants and leakage current densities. The MOSCAP process flow is illustrated in Figure 3-2.

3-3 Device Electrical Parameters Extraction

In this section, device of proposed poly-Si TFTs measurements were performed using an Agilent 4156C precision semiconductor parameter analyzer, and an Agilent 4284A precision LCR meter. Moreover, the methods of parameter extraction used in this study are described. These parameters include threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), subthreshold

swing (S.S.), On current (I_{on}), Off current (I_{off}), On/Off current ratio (I_{on}/I_{off}).

The threshold voltage was defined as the gate voltage at which the drain current reached a normalized drain–current (I_D) equal to (W/L) × 10^{-8} A at a value of V_{DS} of 0.1 V, where W is the drawn channel width and L is the drawn channel length. The field-effect mobility, which was extracted from the maximum transconductance6 (G_m), and the subthreshold swing (S.S.) were measured at a value of V_{DS} of 0.1 V. The value of the S.S. was extracted from the maximum slope of the I_{DS}−V_{GS} characteristics.

3-4 Structural Characterization of High-κ Films

For further analysis, we used XPS analysis to decide composition ratios for HfO_2, HfSiOx and HfAlOx films in Table 2-2. Then, we used XRD measurements to investigate the crystallinity of HfO_2, HfSiOx and HfAlOx films. After annealing at 600°C for 24h in N_2 ambient, HfO_2 films clearly exhibit polycrystalline monoclinic structure, whereas HfSiOx films remain in amorphous structure. But HfAlOx films could be crystallized as Hf-rich (~7%, 12% Al content) after annealing in our experiment. Figures 2-7, 2-8, 2-20 display cross-sectional transmission electron microscopy (TEM) images at different magnifications of the HfO_2, HfO_2+HfSiOx-IL and HfSiOx films, with physical thicknesses of 48.9, 37+6.5, 34.6 nm and interfacial layer of 1.0, 1.0, 1.0 nm, respectively. These TEM samples of poly-TFTs devices were fabricated by focus ion beam (FIB) method and the test structures (poly-Si gate-electrode/gate-dielectric/poly-Si channel) are included in all samples. Samples with HfSiOx films possess amorphous structures, which are conducive to forming smoother surfaces at both the top and bottom interfaces, whereas the device with HfO_2 gate dielectric depicts polycrystalline structure and displays rough top interface.

It was important to reduce the interfacial layer growth; we had test structure of gate oxide stack sample. Because we found as Si incorporation into HfO_2 film that had lower

interface density state and good smooth surface in TEM images. We thought about some better properties of HfSiOx films as bottom layer of stack structure and then discussed in next section.

3-5 Capacitance-Voltage characteristic of High-κ Thick Films

First of all, Figures 3-3 (a) to (d) provide plots of the capacitance density versus gate voltage for the High-κ dielectrics. Figure 3-3 (e) displays plot of the hysteresis for the High-κ dielectrics.

Figure 3-3 (a) extracts value of κ for the HfO_2 film is around 14.2, which is significantly lower than that of bulk HfO_2 (κ = 20~25), possibly because of (i) the thicker interfacial layer with lower κ value in Figure 2-7 or (ii) the presence of excess oxygen atoms in the HfO_2 film [3.8] , and (iii) the fact that effective charges associated with the softest modes are relatively weak when the HfO_2 film possesses its most-stable monoclinic structure [3.9]-[3.10].

The hysteresis decreased with accumulation of Si contents in Figure 3-3 (e). In other words, the hysteresis widths were 1.59V to 0.27V correspond to 25% to 66% Si contents in Figure 3-3 (c). Then, we utilize HfSiOx-IL (66% Si) film as interface layer of HfO_2 film, which the hysteresis was 0.11V that lower than HfO_2 and HfSiOx (66% Si) in Figure 3-3 (b). By the way, the dielectric constant of HfSiOx-IL film is 11.4, which is between HfO_2 and HfSiOx (66% Si). Summary dielectric constant for High-κ materials were in Figure 3-4. Figure 3-3 (a) shows three kinds of materials which are HfO_2, HfSiOx (66% Si) and HfAlOx (40% Al). We found some of Si or Al atoms doped into HfO_2 film that suppress effectively the hysteresis effect from 3.79V to 0.27V. Figure 3-3 (d) shows the hysteresis for three various Al contents of HfAlOx films.

The dielectric constant extracts from Capacitance and summary in Figure 3-4. On the other hand, the value of κ for HfSiOx film is around 6.53, which is also lower than expected.

The Hf/Si composition ratio calculated from this value of κ (66% Si) is for XPS analysis. The values of κ for other HfSiOx films (Si incorporation =40%, 25%) were 10.32 and 12, respectively. This result indicates that Si atoms are more reactive toward oxygen atoms than are Hf atoms under our process conditions, which is consistent with the results in Chapter 2.

The value of κ for HfAlOx film is around 13.33, which is higher than HfSiOx film, obviously. Because the κ-value for aluminum oxide (κ_{Al2O3}～9) is higher than silicon dioxide (κ_{SiO2}～3.9). So, the κ-value increasing as we utilize silicon (Si) or aluminum (Al) atoms to incorporate with HfO_2. The Si atoms incorporation calculated from HfSiOx films (66%, 40%, 25%) and the Al atoms incorporation calculated from HfAlOx films (40%, 12%, ~7%) are for XPS analysis. This result indicates that Si atoms are more reactive toward oxygen atoms than are Hf atoms under our process conditions, which is consistent with the results in Chapter 2.

We would be got exactly physical thickness in Table 3-1, that subtracted thickness of interfacial layer from total thickness by TEM and measured correct dielectric constant in Figure 3-4.

The HfSiOx films also exhibit smaller frequency dispersion (~3.5%) than the HfO_2 films (~6%) and the HfAlOx films (~6.6%) on the C-V curves measured at 100K and 1MHz, as shown in Figures 3-5 to 3-7.

Using HfSiOx or HfSiOx-IL can improve Jg-CET characteristic in Figure 3-8 and doped Si or Al atoms incorporation into HfO_2 had higher breakdown field and lower gate leakage current density (Jg) in Figure 3-9.

The lower dielectric constant of the HfSiOx films is therefore due to their being Si-rich. In terms of the current–voltage characteristics, the HfSiOx films exhibit superior performance-smaller leakage current (2.65×10^{-10} A/cm^2 at V_{GS} = -2 V) and larger breakdown field (-6MV/cm), compared with the HfO_2 films (4.78×10^{-9} A/cm^2 and -4.6 MV/cm, respectively), presumably because of the amorphous nature of HfSiOx film after processing.

In terms of the current-voltage characteristics, the HfAlOx films for Hf/Al composition ratio = 40% exhibit superior performance-larger leakage current (6.12×10^{-9} A/cm^2 at V_{GS} = -2 V) and larger breakdown field (-6.2 MV/cm), compared with the HfO_2 films (4.78×10^{-9} A/cm^2 and -4.6 MV/cm, respectively).

3-6 Electrical Properties of High-κ Thick Films

Figure 3-10 shows the plot of I_D-V_G for High-κ materials. Due to Si atoms incorporation into HfO_2 film could be improved interface roughness that reduced DIBL effect. Aggravated gate-induced drain leakage (GIDL) current was thought to arise from the higher induced electric field by the introduction High-κ films, and field-emission current would be the dominant leakage mechanism. Furthermore, HfSiOx films were smaller gate leakage than HfO_2 and HfSiOx-IL films in Figure 3-11.

Figures 3-12 to 3-13 show summary of threshold voltage and I_{on}/I_{off} ratio; HfSiOx and HfSiOx-IL could improve to receive lower V_{TH}, higher I_{on}/I_{off} ratio at lower operating voltage.

We used the conductance method [3.11] to extract interface density of states (D_{it}) for High-κ materials and summary of plot in Figure 3-14. We extracted Subthreshold swing from I_D-V_G characteristic in Figure 3-15 at V_{DS}=0.1V for High-κ materials to compare with the conductance method. And then getting a trend as same as together. The interface density of states (D_{it}) was smaller to receive better Subthreshold swing.

Figure 3-16 displays the relationship between the field-effect mobility (μ_{FE}) and the gate voltage of poly-Si TFTs with different gate dielectrics. Obviously, HfSiOx-TFT depicts much higher μ_{FE} than HfO_2-TFT. By the way, HfSiOx-IL-TFT decice got the better mobility than only HfO_2 film. The device with gate dielectric depicts slowly rising mobility and lower peak of μ_{FE} related to the thicker equivalent oxide thickness (EOT) and inferior gate oxide quality. Grain-boundary scattering and Coulomb charge scattering would be main mobility

degradation mechanisms for this device. For poly-Si TFTs using High-κ gate dielectrics, the mobility should be improved due to the thinner EOT and superior film quality, such as in the case of HfSiOx-TFTs. The poly-Si channels were prepared and crystallized by LPCVD system at the same time, so we thought the grain boundary scattering should be nearly the same among all samples.

3-7 Characteristics of Low-Temperature-Polycrystalline Silicon (LTPS) TFTs Using High-κ Gate Dielectric

Although the values of the S.S. and Ion/Ioff current ratio of TFTs containing HfSiOx are slightly worse than those of the TFTs incorporating HfO_2, we believe that HfSiOx is a better choice for use as the gate dielectric in future poly-Si TFTs for the following reasons: First, TFTs containing HfSiOx films exhibit smaller leakage current and larger breakdown field strength than TFTs containing HfO_2 because of the amorphous nature of the HfSiOx films after processing. Second, the hole mobility of TFTs containing HfSiOx is around 2 times better than that of the TFTs incorporating the HfO_2 dielectric, whereas it is worse for the TFTs containing the HfO_2 gate dielectric. According to previous reports, we speculate that the degraded mobility of the TFTs containing the HfO_2 dielectric is due to additional Coulomb scattering caused by the charges in the HfO2 dielectric. In contrast, HfSiOx films prevent this additional scattering and exhibit improved mobility because of their higher thermal stability. Third, the removal of HfSiOx through etching is much easier than that of HfO_2. This feature is rather important for device fabrication.

3-8 Summary

In this chapter, high performance n-channel poly-Si TFTs using hafnium silicate

(HfSiOx) gate dielectric is demonstrated using low-temperature processing. Higher I_{on}/I_{off} current ratio, smaller subthreshold swing, lower threshold voltage and higher mobility than deposited-HfO_2 gate dielectric are achieved at lower operation voltages. Our results suggest that HfSiOx dielectric is a potential candidate for the gate-dielectric material of future high-performance poly-Si TFTs. Summary MOSCAP and device benefits were in Table 3-2 to 3-3.

Furthermore, the gate oxide stack structure utilizing HfSiOx-IL structure (66% Si) as bottom layer to suppress interface defects and then could be enhanced high performance LTPS TFTs.

Table 3-1

Summary of thickness, physical thickness, thickness deviation

for Low-Temperature Polycrystalline Silicon TFTs.

HK TFT 40nm Condition	N&K $T_{N,K}$ (nm)	TEM $T_{high\text{-}k}+T_{IL}$ (nm)	Thickness Deviation (%)
1.HfO_2	47.9	50.4 (48.9+1.5)	4.9
2.HfO_2+HfSiOx-IL (66% Si)	43.3	44.5 (37+6.5+1.0)	2.7
3.HfSiOx (66% Si)	33.5	35.6 (34.6+1.0)	5.8

Table 3-2

MOSCAP parameters vs. Device parameters

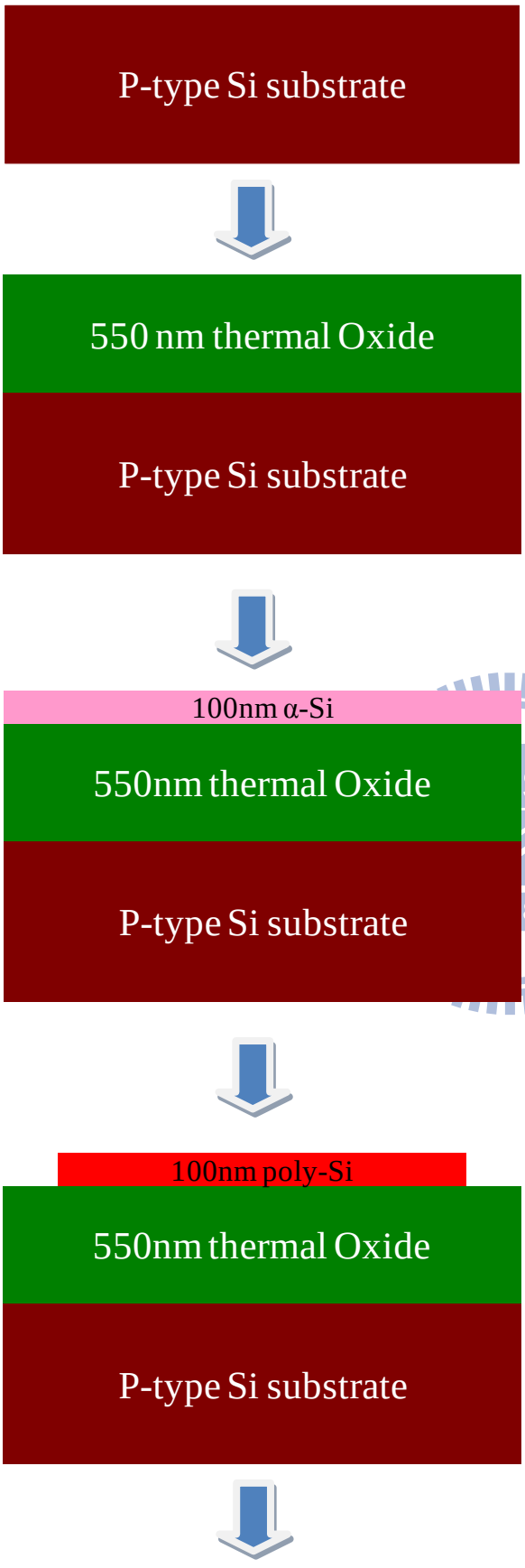
Gate dielectric	Crystalline	C-V Hysteresis (V)	Jg-CET	E_{BD} (MV/cm)	D_{it} (cm^{-2}/eV^{-1})		Note
HfO_2 ($T_{N,K}$=47.9nm)	Yes	3.79	4.75E-5 13.3 nm	-4.55	1.27E11		
HfO_2+HfSiOx-IL ($T_{N,K}$ =43.3nm)	Yes	0.11	6E-8 14.6 nm	-5.38	9.23E10		☆☆☆
HfSiOx (66% Si) ($T_{N,K}$ =33.5nm)	No	0.27	2.16E-8 18.9 nm	-6.0	1.77E11		☆☆☆☆
HfAlOx (40% Al) ($T_{N,K}$ =50.1nm)	No	1.08	1.85E-7 13.9 nm	-6.19	1.99E11		☆☆

Table 3-3

Device parameters of Low-Temperature N-Channel Polycrystalline Silicon TFTs.

(W/L = 10μm/1μm) incorporating various dielectrics at V_{DS} of 0.2V

W/L = 10μm/1μm Gate dielectric	I_{on}/I_{off} ratio (@VDS=2V)	S.S. (V/Dec)	V_{TH} (V)	DIBL (mV/V)	GIDL	μ_{EF} (cm^2/V-sec)	
HfO_2 ($T_{physical}$=48.9nm)	4.5E6	0.50	4.87	4.87	160	5.05	☆
HfO_2+HfSiOx-IL ($T_{physical}$=43.5nm)	1.2E7	0.46	4.32	4.32	42	18.47	☆☆☆☆☆
HfSiOx (66% Si) ($T_{physical}$=34.6nm)	9.5E6	0.61	3.72	3.72	53	7.88	☆☆☆
HfAlOx (40% Al) ($T_{physical}$=50.1nm)	1.05E7	0.63	4.30	4.30	50	8.11	☆



1. Si substrate

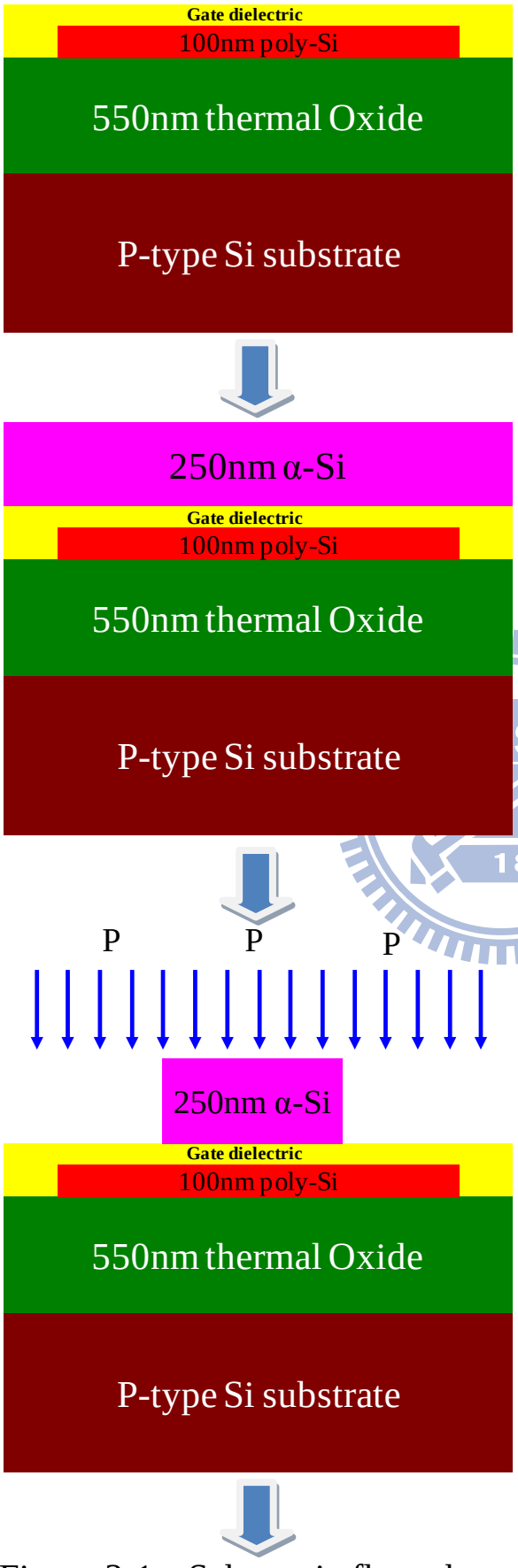
2. Thick oxide layer to simulate glass plate

3. Amorphous-Si deposition by LPCVD system at 550℃, in SiH_4 ambient.

4. Re-crystallization (600℃, N_2, 24 h)

5. Active region definition (Mask 1)

Figure 3-1 Schematic flow charts for the fabrication of poly-Si TFTs.



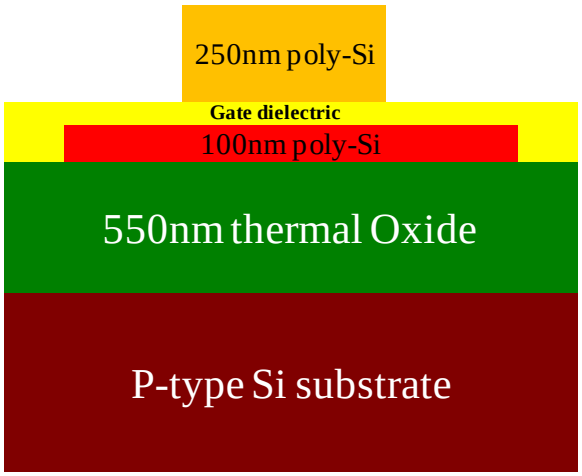
6. 40nm Gate dielectrics deposition by AVD.

7. 250nm amorphous-Si deposition by LPCVD system.

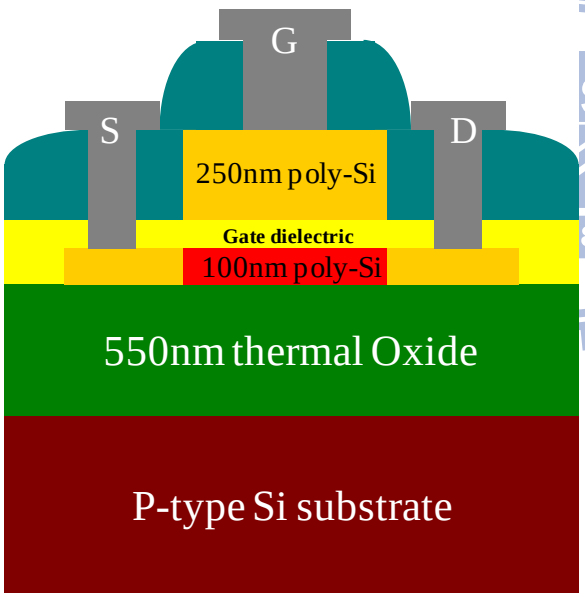
8. Amorphous-Si gate definition (Mask 2).

9. P^+ ion implantation to gate and channel.

Figure 3-1 Schematic flow charts for the fabrication of poly-Si TFTs.

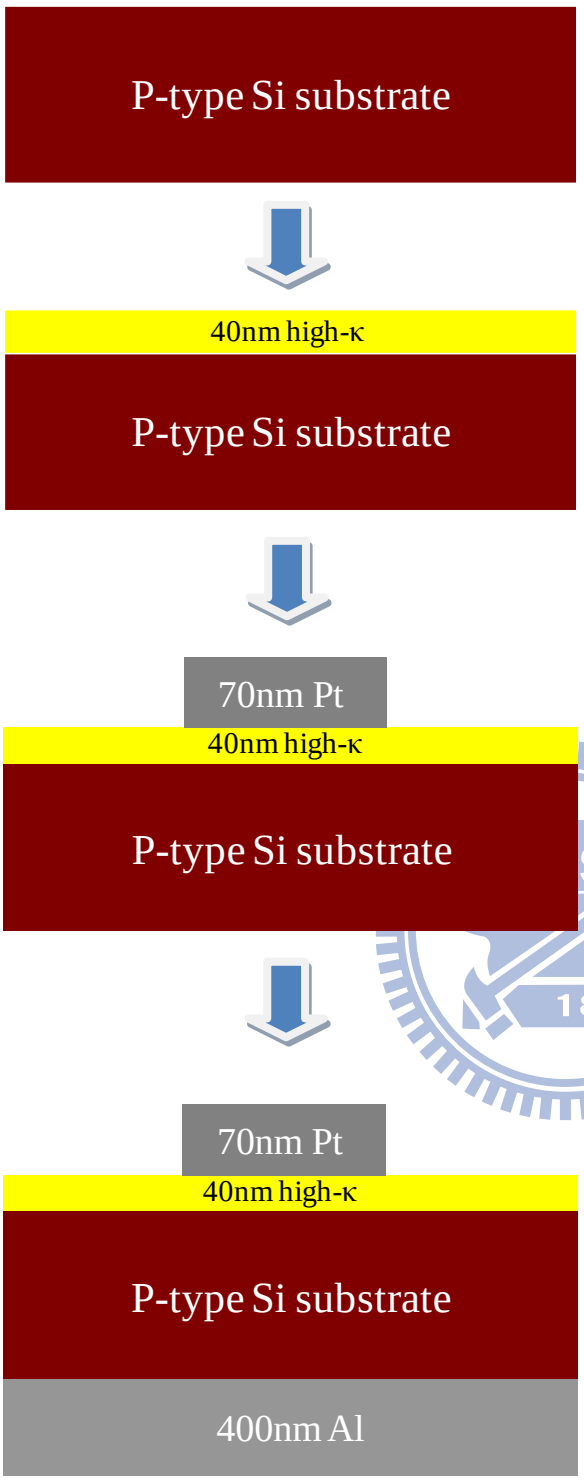


10. Amorphous-Si gate re-crystallization and dopant activation (600℃, N_2, 24 hr)



11. Passivation layer deposition by PECVD system and contact hole definition (Mask 3).
12. 500nm Al-Si-Cu deposition by PVD system and metal-pad definition (Mask 4).
13. Forming gas sintering (400℃, 30 min)

Figure 3-1 Schematic flow charts for the fabrication of poly-Si TFTs.



1. Si substrate

2. 40nm gate dielectrics deposition by AVD
3. Annealing by LPCVD system at 600°C, 24h, in N_2 ambient.

4. Top Pt (70nm) electrode deposition by sputter system through shadow mask.

5. Backside Al (400nm) electrode deposition by thermal coater system.

Figure 3-2 Schematic flow charts for the fabrication of capacitors.

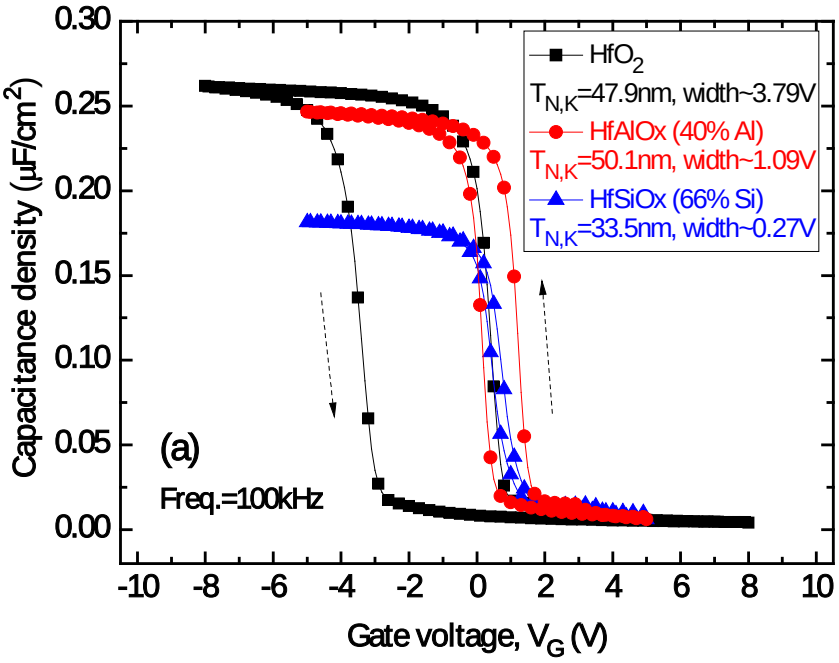


Figure 3-3 Plots of capacitance density versus gate voltage.

(a) HfO_2, HfSiOx and HfAlOx

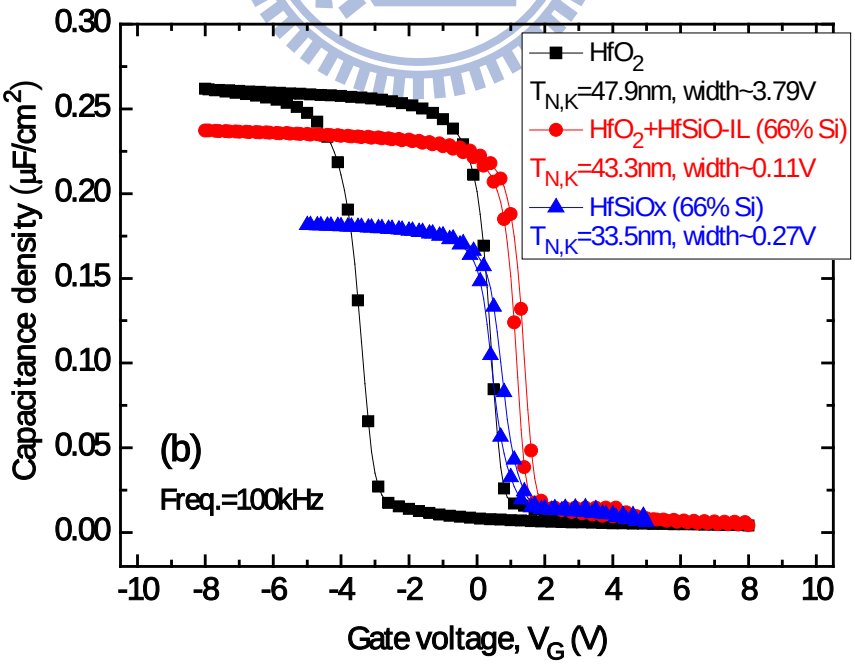


Figure 3-3 Plots of capacitance density versus gate voltage.

(b) HfO_2, HfO_2+HfSiOx-IL and HfSiOx (66% Si)

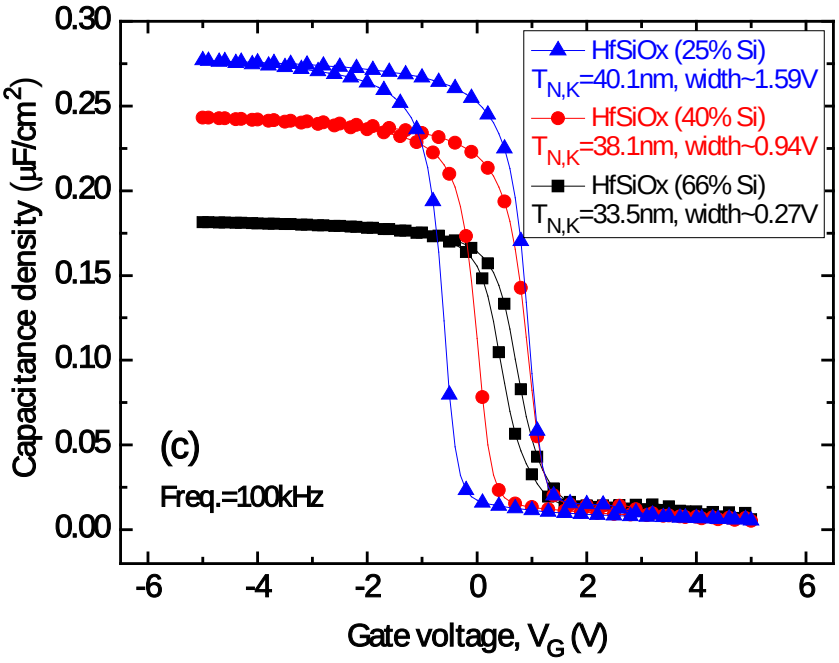


Figure 3-3 Plots of capacitance density versus gate voltage.

(c) HfSiOx incorporation of 25%, 40% and 66% Si

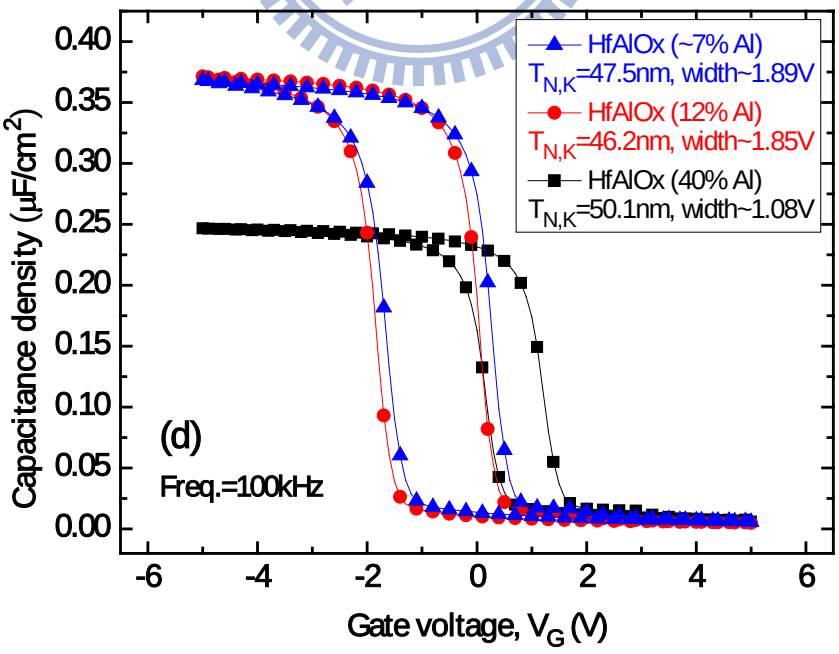


Figure 3-3 Plots of capacitance density versus gate voltage.

(d) HfAlOx incorporation of ~7%, 12% and 40% Al

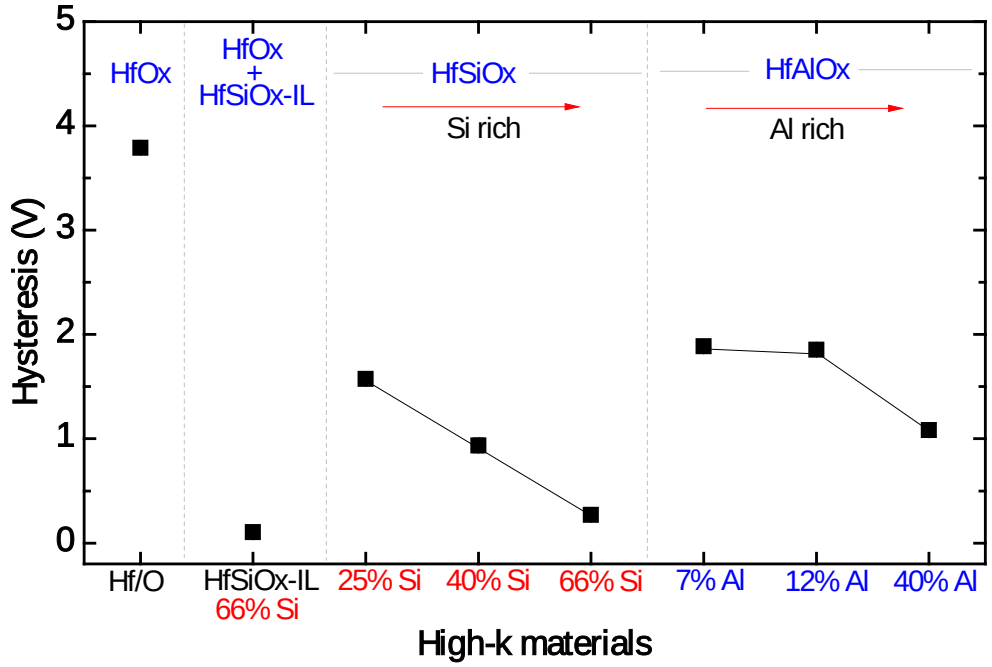


Figure 3-3 Summary of hysteresis for High-κ materials.

(e) HfO_2, HfSiOx-IL, HfSiOx and HfAlOx

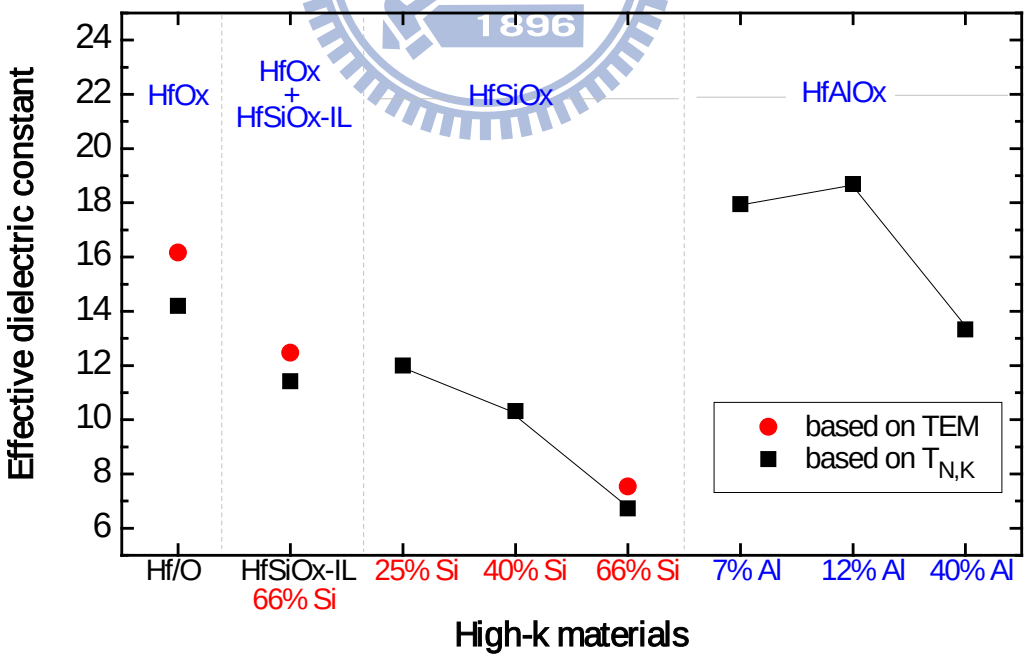
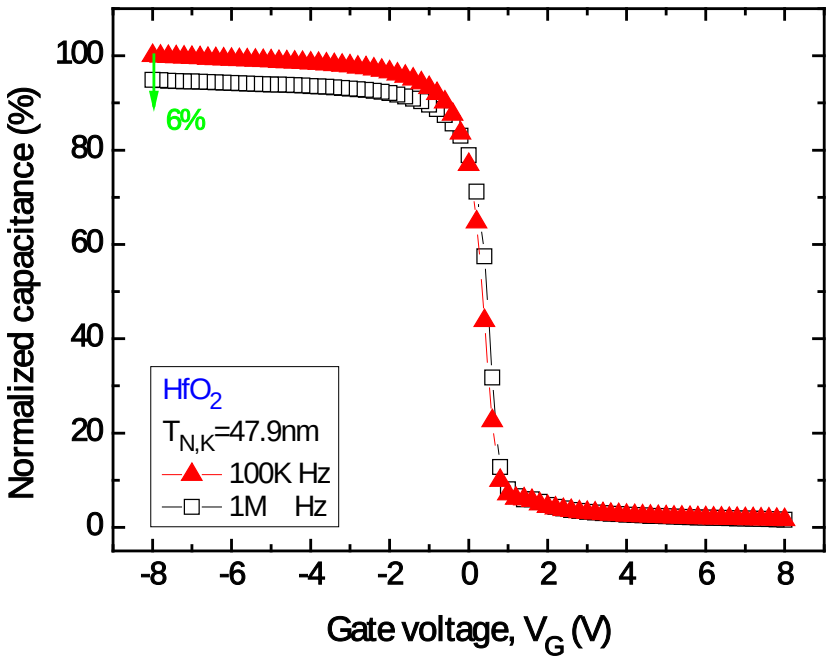
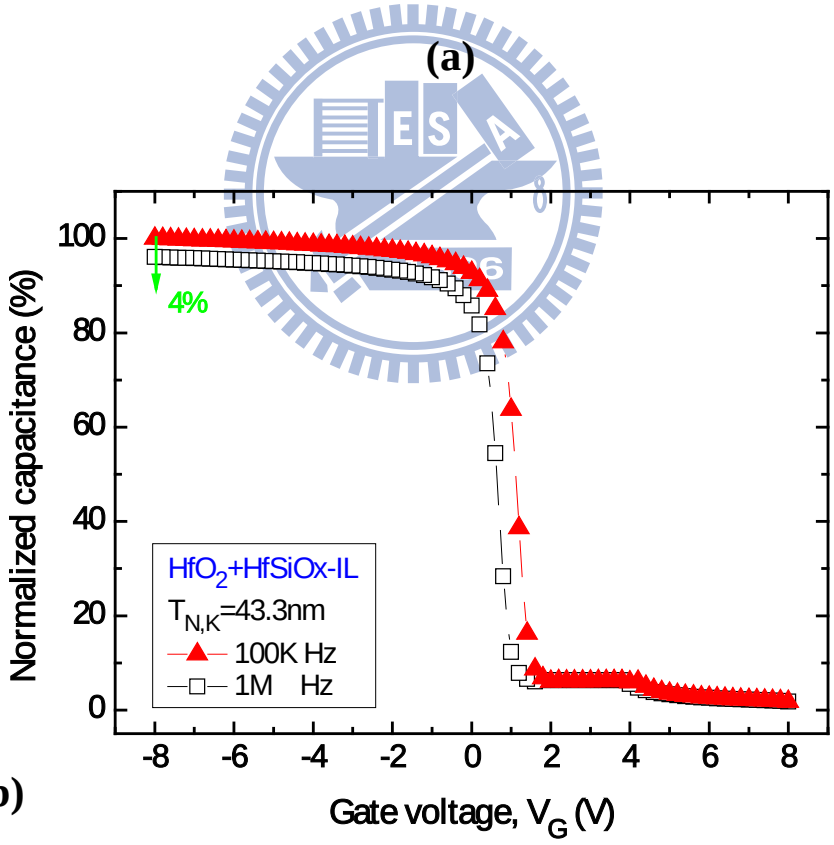


Figure 3-4 Summary of effective dielectric constant for High-κ materials.



(a)



(b)

Figure 3-5 Frequency dispersion of normalized capacitance versus gate voltage for (a)HfO_2 (b)HfO_2+HfSiOx-IL films after annealing at 600℃, 24h in N_2 ambient.

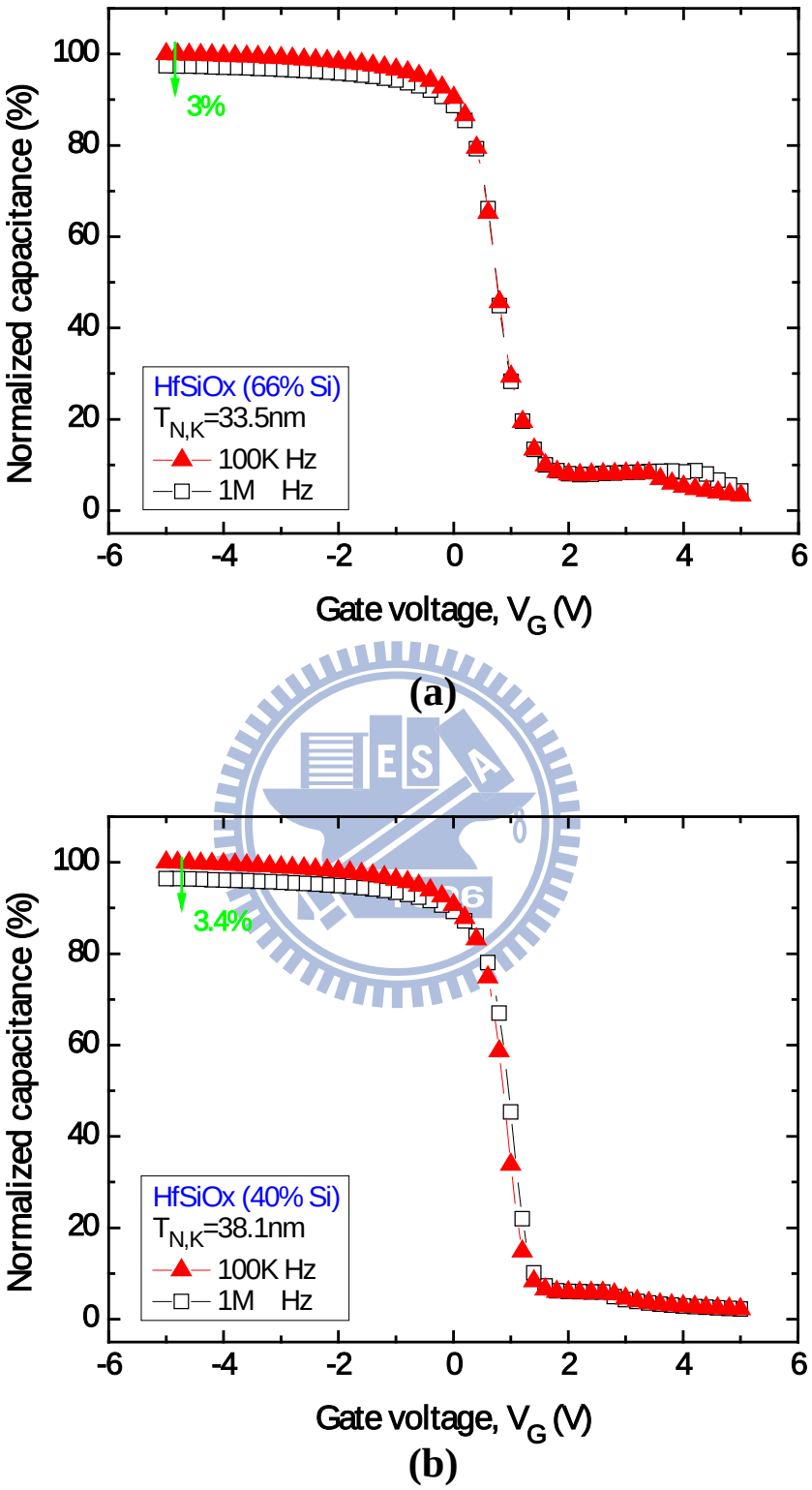
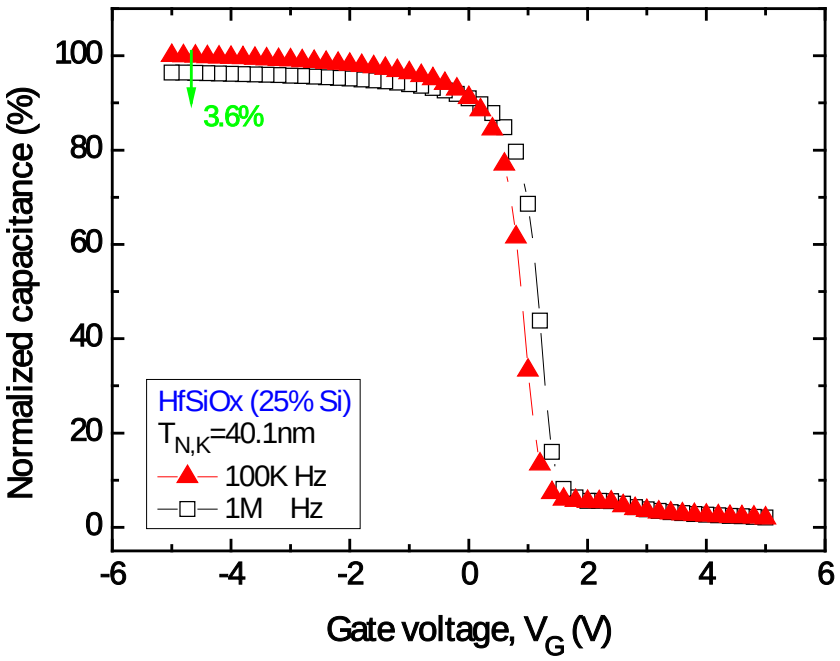
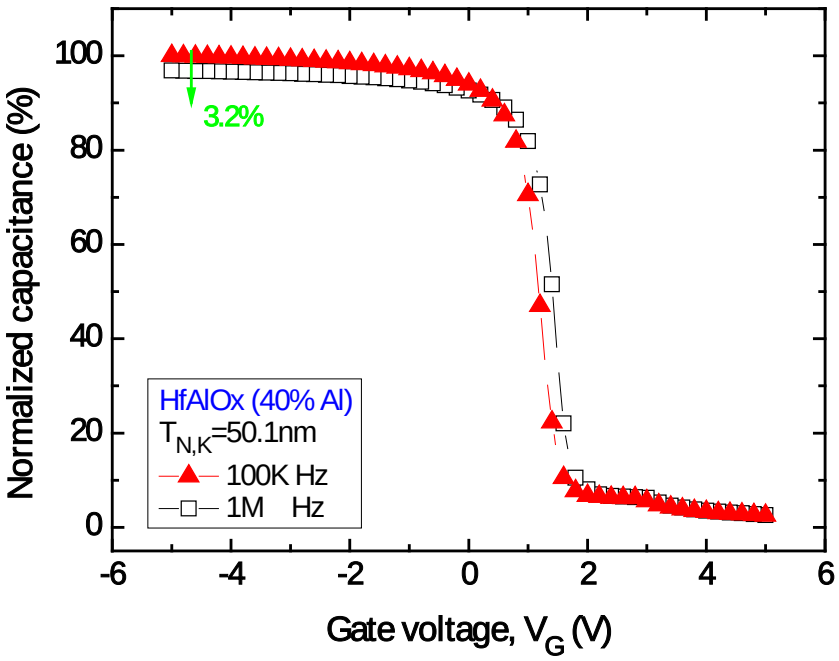


Figure 3-6 Frequency dispersion of normalized capacitance versus gate voltage for HfSiOx incorporation of (a)66%, (b)40%, (c)25% Si after PDA at 600℃, 24h in N_2.

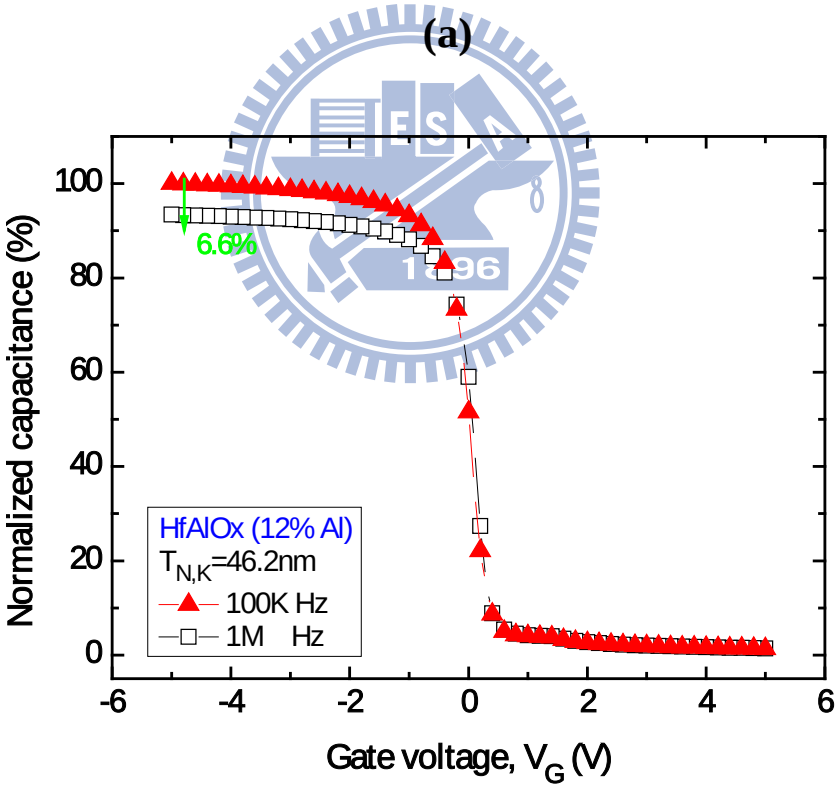


(c)

Figure 3-6 Frequency dispersion of normalized capacitance versus gate voltage for HfSiOx incorporation of (a)66%, (b)40%, (c)25% Si after PDA at 600℃, 24h in N_2.

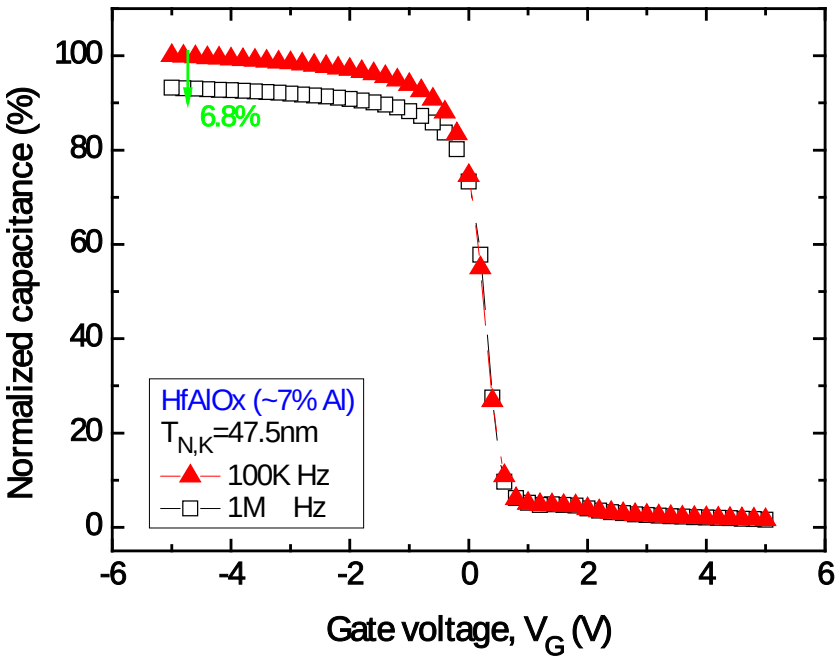


(a)



(b)

Figure 3-7 Frequency dispersion of normalized capacitance versus gate voltage for HfAlOx incorporation of (a)40%, (b)12%, (c)~7% Al after PDA at 600℃, 24h in N_2.



(c)

Figure 3-7 Frequency dispersion of normalized capacitance versus gate voltage for HfAlOx incorporation of (a)40%, (b)12%, (c)~7% Al after PDA at 600℃, 24h in N_2.

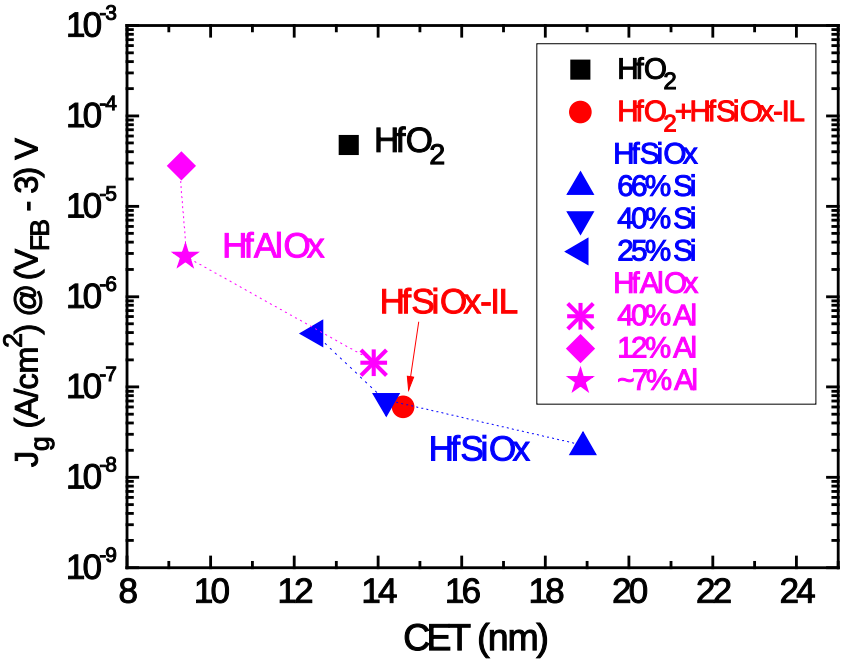


Figure 3-8 Leakage current density versus capacitance equivalent thickness for High-κ materials after PDA at 600℃, 24h in N_2 ambient.

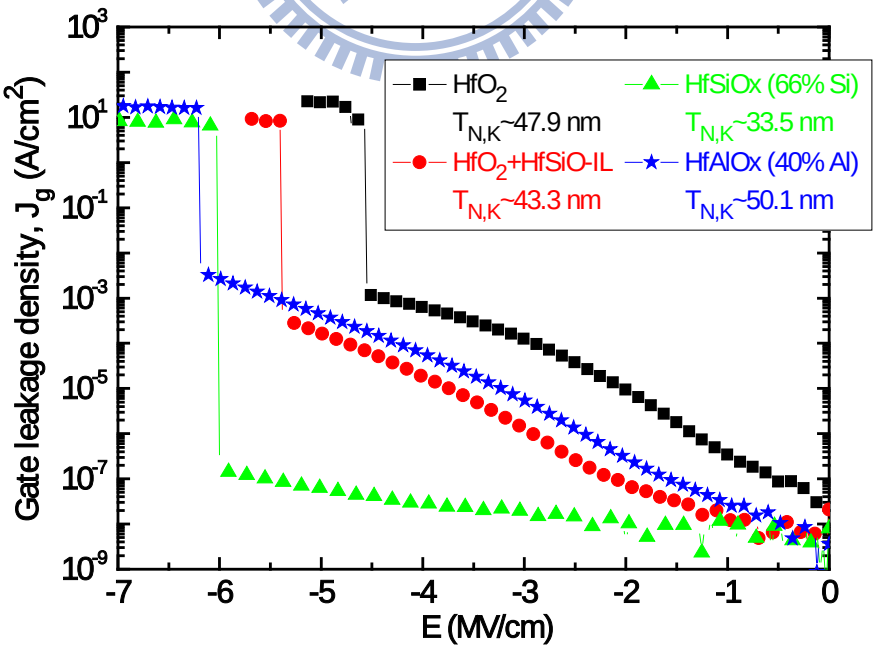


Figure 3-9 Leakage current density versus electrical filed for High-κ materials.

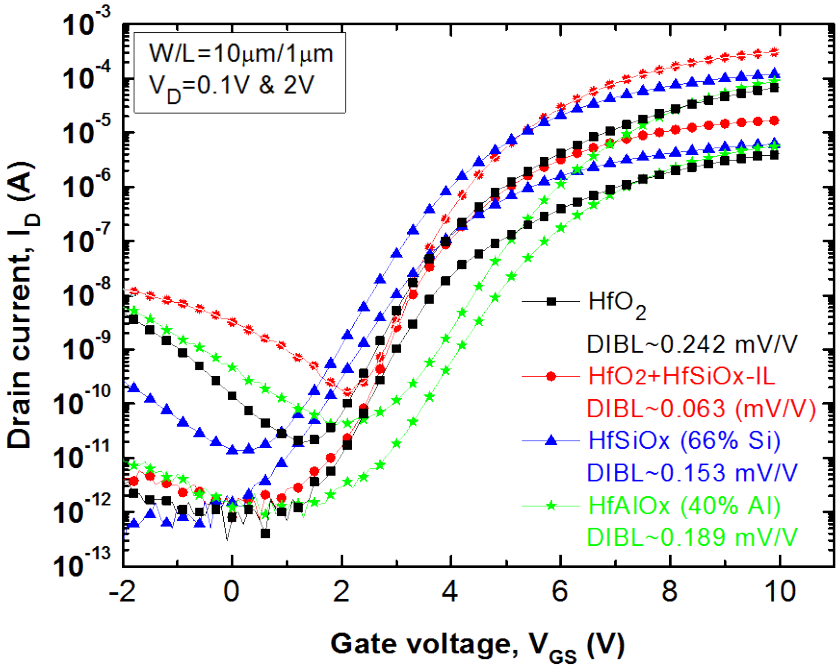


Figure 3-10 The plot of I_D-V_G for HfO2, HfSiOx-IL (66% Si), HfSiOx (66% Si) and HfAlOx (40% Al).

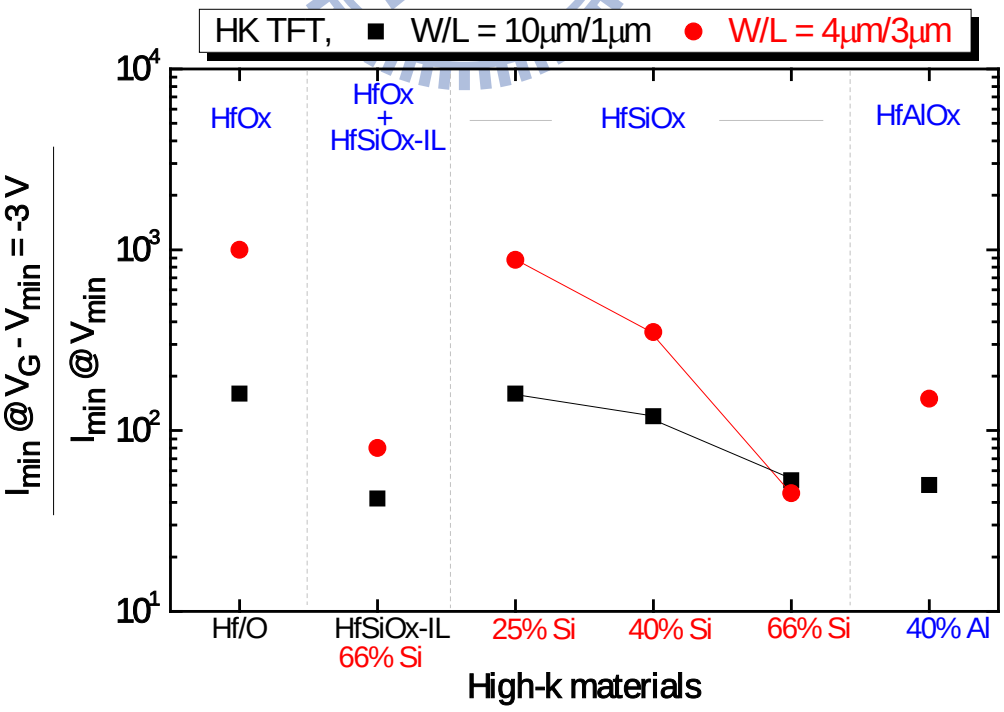


Figure 3-11 Summary of GIDL effect for High-κ materials.

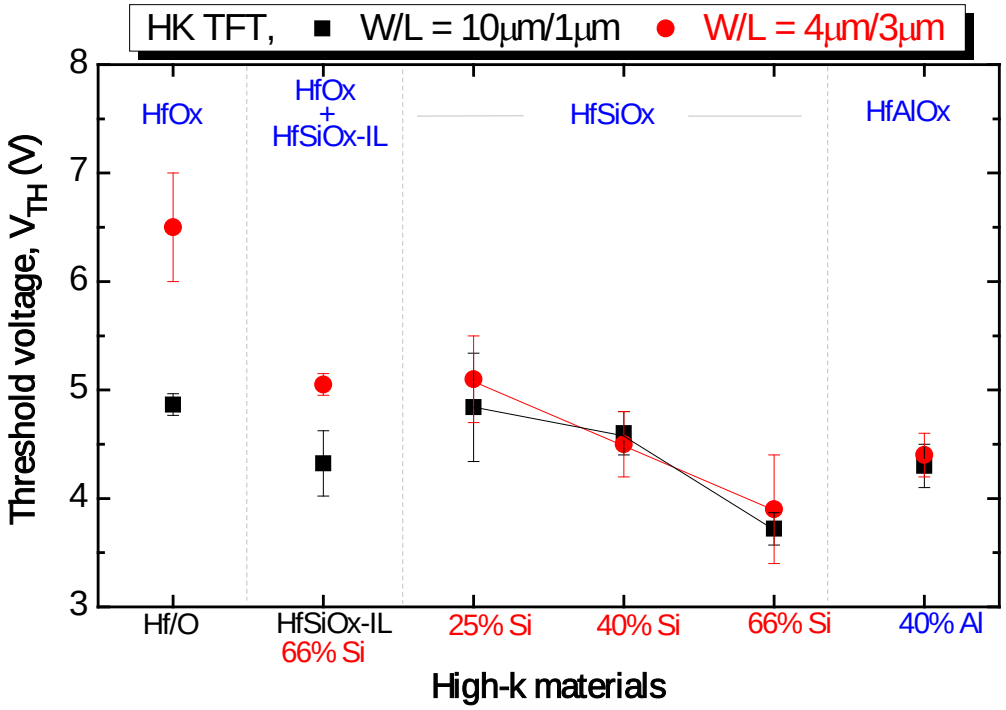


Figure 3-12 Summary of threshold voltage for High-κ materials.

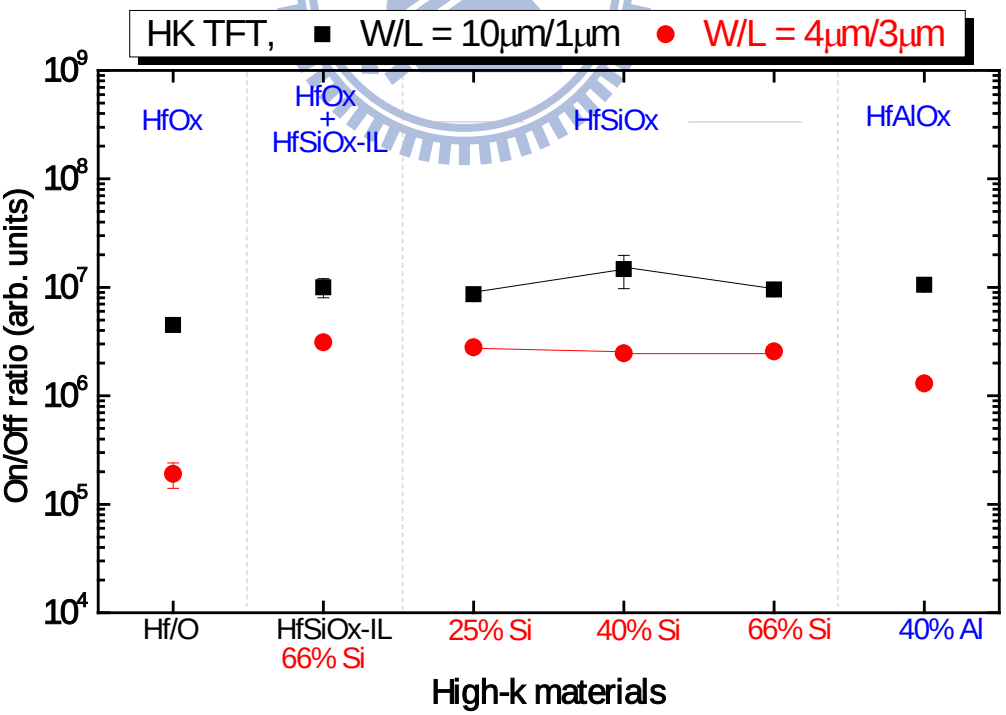


Figure 3-13 Summary of On/Off current for High-κ materials.

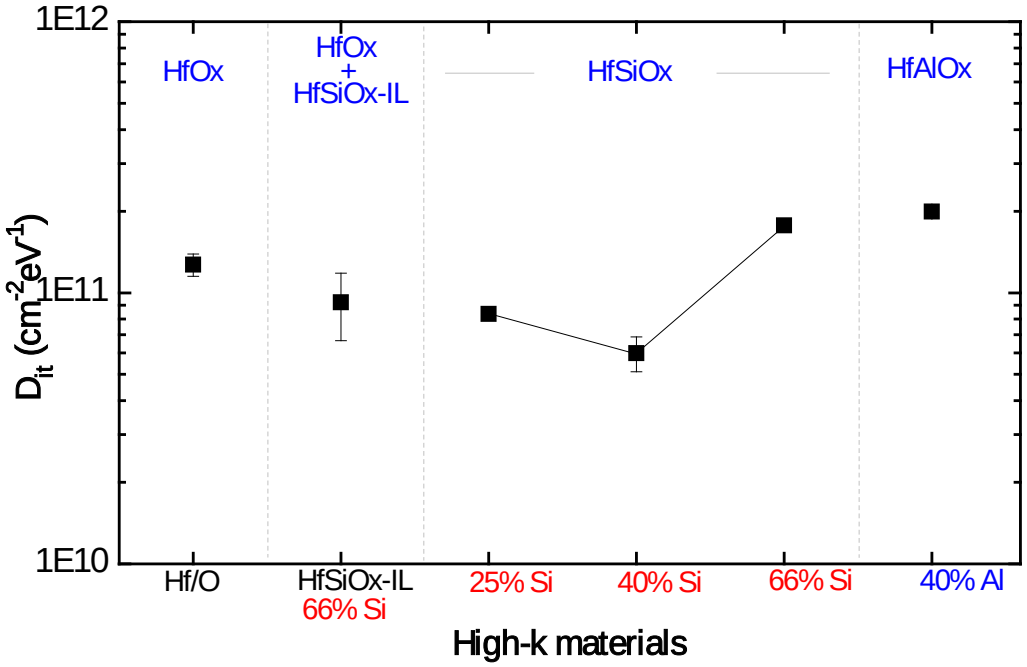


Figure 3-14 Summary of interface density of state for High-κ materials.

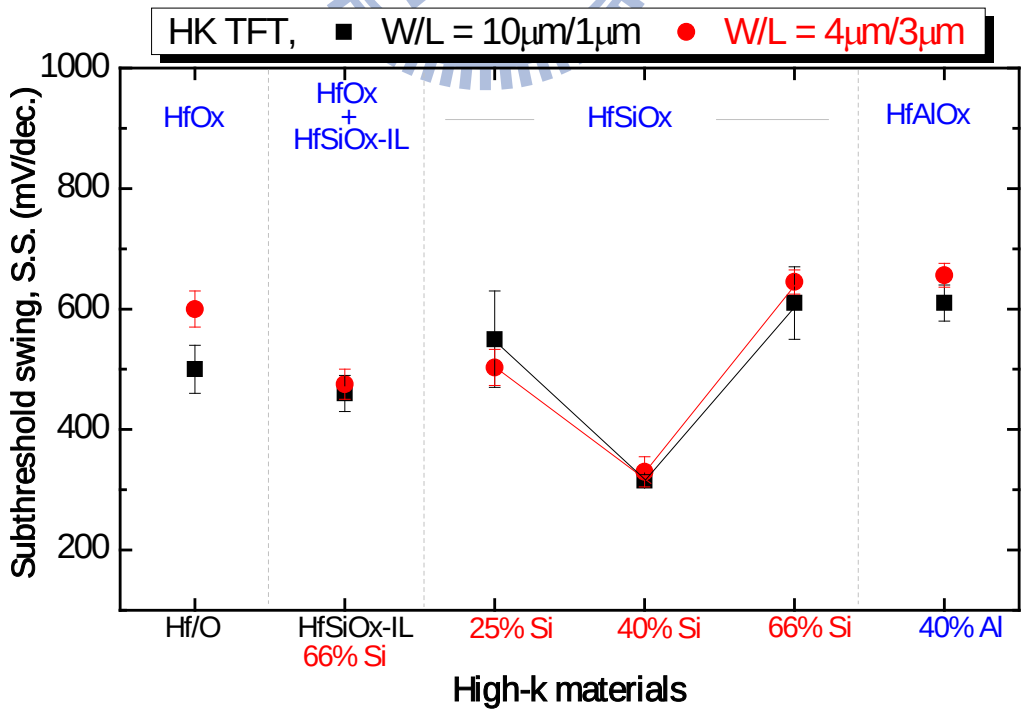


Figure 3-15 Summary of subthreshold swing for High-κ materials.

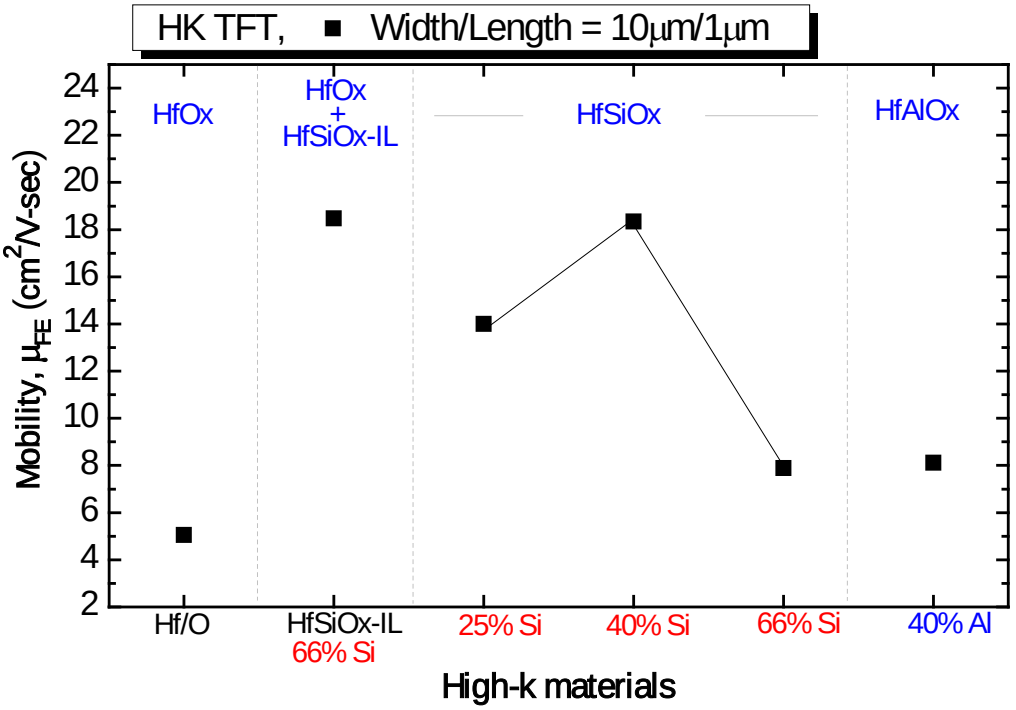


Figure 3-16 Summary of field-effect mobility for High-κ materials.

Chapter4

High-Performance and MOSFETs Using High-κ Material

4-1 Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important device for forefront high-density integrated circuits such as microprocessors and semiconductor memories. The basic MOSFET structure using this SiO_2/Si system was proposed by Atalla [4-1]. In this chapter, we prepare to fabricate 1's mask structure and modify for various High-κ materials that replace the gate oxide of the conventional deposited-SiO_2 MOSFETs devices.

4-2 High-κ Films Deposition and Device Fabrications

Firstly, the thinner High-κ films (~4nm) were deposited through atomic vapor deposition (AVD) system. From the experience of thin High-κ film deposition, we use the substrate temperature as 500℃ and oxygen gas flow as 1300 sccm for HfO_2 and HfAlOx films. Another, we use the substrate temperature as 500℃ and oxygen gas flow as 1800 sccm for HfSiOx film. The $Hf[OC(CH_3)_3]_2(mmp)_2$ precursor, $Si[OC(CH3)_3]_2(mmp)_2$ precursor, $Al[OCH(CH_3)_2]_3$ precursor and oxygen gas were employed as Hf, Si, and O sources, respectively. The structural characterizations of these films would be analyzed by various measurements, such as, x-ray photoelectron spectrum (XPS), x-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM). And then, self-aligned top-gate n-channel 1's mask MOSFETs were fabricated and the procedure flow was

illustrated in Figure 4-1.

First of all, the silicon-wafers were standard RCA cleaning. Subsequently, rapid thermal oxidation (RTO) at 600℃ for 10 sec and spike at 900℃. This fabrication would be suppressed interfacial layer to grow. Then, the various gate dielectrics (with thickness of 4nm) were deposited. Specifically, HfO_2, HfSiOx and HfAlOx films were deposited through atomic vapor deposition (AVD) using an AIXTRON Tricent system at a substrate temperature of 500°C. All of the wafers were then subjected to anneal at 900℃ for 30 sec in N_2 ambient. Subsequently, deposition of a 250nm-thick TiN layer was through FSE-PVD, which served as the gate electrode. The gate electrodes were patterned and the source, drain, and gate regions were doped through self-aligned arsenic ion implantation (dosage: 5×10^{15} ions/cm^2; energy: 30 keV). After formation of the source and drain, the dopant was activated at 600°C for 120 sec in N_2 ambient. Finally, all of the wafers were subjected to anneal at 700℃ for 60 sec in N_2 ambient again. Figure 4-2 displays the plan-view schematic for the fabrication of MOSFETs.

Capacitors containing high-κ dielectrics were fabricated simultaneously through the use of a shadow mask to allow measurement of dielectric constants and leakage current densities (the process flow is illustrated in Figure 4-3).

4-3 Device Electrical Parameters Extraction

In this section, device of proposed MOSFETs measurements were performed using an Agilent 4156C precision semiconductor parameter analyzer, and an Agilent 4284A precision LCR meter. Moreover, the methods of parameter extraction used in this study are described. These parameters include threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), subthreshold swing (S.S.), On current (I_{on}), Off current (I_{off}), On/Off current ratio (I_{on}/I_{off}).

The threshold voltage was extracted drain–current (I_D) in the linear region at a value of V_{DS} of 0.2 V at the V_G axis is equal to $V_{TH}+1/2V_D$. The field-effect mobility, which was

extracted from the maximum transconductance (G_m), and the subthreshold swing (S.S.) were measured at a value of V_{DS} of 0.2 V. The value of the S.S. was extracted from the maximum slope of the I_{DS}-V_{GS} characteristics.

4-4 Structural Characterization of High-κ Films

For further analysis, we used XPS analysis to decide atomic ratios for HfO_2, HfSiOx and HfAlOx films in Table 2-3. Then, we used XRD measurements to investigate the crystallinity of HfO_2, HfSiOx and HfAlOx films. After annealing at 900°C for 30 sec in a N_2 ambient, HfO_2 films clearly exhibit polycrystalline monoclinic structure as same as thicker films in Figure 2-6, and HfSiOx films exhibit monoclinic and amount of small orthorhombic structure in Figure 2-19. This behavior suggests that the HfSiOx film has better thermal stability than the HfO_2 film. Figures 2-12, 2-21, 2-29 display cross-sectional transmission electron microscopy (TEM) images at different magnifications of the HfO_2, HfSiOx and HfAlOx films, physical thicknesses were 3.3, 3.0, and 3.6 nm, respectively. These TEM samples of MOSFET devices were fabricated by focus ion beam (FIB) method and the test structures (gate-electrode/gate-dielectric/silicon) are included in all samples. In addition, as discussed in Chapter 2, the interfacial layer between High-κ/Si interface was grew during the film deposition and became thicker (~1.5nm) after 900℃ for 30 sec annealing, as shown in Table 2-6.

4-5 Characteristics of MOSFETs Using High-κ Gate Dielectric

First of all, Figures 4-4 to 4-5 show I_D-V_G plot and subthreshold swing for various Si contents of HfSiOx films. Figure 4-5 shows subthreshold swing and channel length relation, the subthreshold swing decreased with accumulation of Si contents for any channel length conditions from 2um to 30um. Then, we chose the minimum and maximum Si content cases

for channel length of 30um to compare with together in Figure 4-4. The GIDL effect could be suppressed slightly of 77% Si content HfSiOx device.

Secondly, we compared HfAlOx films with S.S. and various Al content samples relation in Figure 4-7. The characteristic of S.S. would be enhanced as same as the HfSiOx dielectrics. Figure 4-6 shows I_D-V_G plot, we found the V_{TH} shift as accumulation of Al contents. The results were discussed in section 4-6.

Finally, we discussed characteristic of I_D-V_G and subthreshold swing with HfO_2, HfSiOx (12% Si) and HfAlOx (12% Al) dielectrics. Figures 4-8 shows the GIDL effect, HfSiOx and HfAlOx MOSFET devices were got better performance than HfO_2-device. And subthreshold swing was enhanced obviously as utilizing Si or Al atoms incorporated into HfO_2 film in Figure 4-8.

4-6 Electrical Properties of MOSFETs by Source/Drain Series Resistance Correction

There had some problems in the device and processes due to the MOSFETs device were only one lithograph. The source/drain regions were without metal contact. First of all, we extracted the source/drain series resistance (R_{SD}) of HfSiOx (66% Si) device. We utilized V_G-V_{TH}=1.0V and V_G-V_{TH}=1.25V cases to extract the series resistance and we got two regions at channel length equal to zero in Figure 4-10. We obtained series resistance value from 850 to 1000 ohm for cross region of two cases at channel length equal to zero. To avoid correction was lager deviation and unbelievable, we chosen worse case of series resistance value for 1000 ohm to correct. We utilized series resistance correction method for various channel lengths to calculate threshold voltage (V_{TH}), transconductance (Gm), On/Off current ratio…etc. Firstly, we check threshold voltage (V_{TH}) and change back correction data which receive 1.2 times from channel length comparison 30um with 3um in Figure 4-11. Then, we

check transconductance (Gm) and change back correction data which receive 10 times from channel length comparison 30um with 3um in Figure 4-12. Finally, On/Off current ratio were 15 times between 30um and 3um in Figure 4-13. Therefore, we avoided correction deviation too huge and we would be discussed the case of channel length equal to 30um for MOSFET devices.

Although source/drain series resistance correction method [4.1] was expressed as follows:

$$\mathbf{V_{GSi} = V_{GS,max} - I_{D,max}/g_{m,max}} \quad \ldots\ldots \text{(1)}$$

$$\mathbf{g_{m,max} = kV_{DS}/[1 + kR_{SD}(V_{GS,max} - V_{TH} - V_{DS}/2)]^2 \text{ , } k = C_{ox}\mu W/L} \quad \ldots \text{(2)}$$

$$\mathbf{V_{TH0} = V_{GS,max} - V_{DS}/2 + [1 - (1 + 4kR_{SD}(V_{GS,max} - V_{GSi}))^{1/2}]/2kR_{SD}} \ldots \text{(3)}$$

Here, in Eq. (1), V_{GSi} is cross of the tangent line and x-axis in linear region. $g_{m,max}$, $V_{GS,max}$, and $I_{D,max}$ are the maximum value of I_D-V_G differential, the point of $V_{GS,max}$ and $I_{D,max}$ at V_D of 0.2V are correspond to $g_{m,max}$'s gate voltage as same, respectively. In Eq. (2) and (3), the V_{TH} and V_{TH0} is threshold voltages correspond to pre-correction and post-correction.

We got exactly values for our parameters of MOSFET device in Figures 4-14, 4-17 to 4-20. Summary of V_{TH} correction was in Figure 4-14. There was obvious V_{TH} shift issue as Al contents more than 40% incorporation. The V_{TH} shift increased with accumulation of Al contents in HfAlOx films in Figure 4-15. The result of V_{TH} shift was the negative fix charges [4.2]-[4.4]. The negative fix charge was extracted from capacitance and voltage, which value was around 1E12 cm^{-2}.

Figure 4-18 shows the off current, HfSiOx and HfAlOx materials were better than HfO_2 dielectric. Due to HfSiOx and HfAlOx films were smaller off current, we would be obtained superior I_{on}/I_{off} current ratio in Figure 4-19.

Finally, Figures 4-20 to 4-21 displays plot of transconductance correction and mobility, respectively. All High-κ MOSFETs have the close values of G_m, which is dependent on C_{ox}

and mobility. We attempt to extract C_{ox} to estimate the mobility further, but it seems exhibit the irregular tendency. Summary of electrical characteristics on MOSFETs were in Table 4-1.

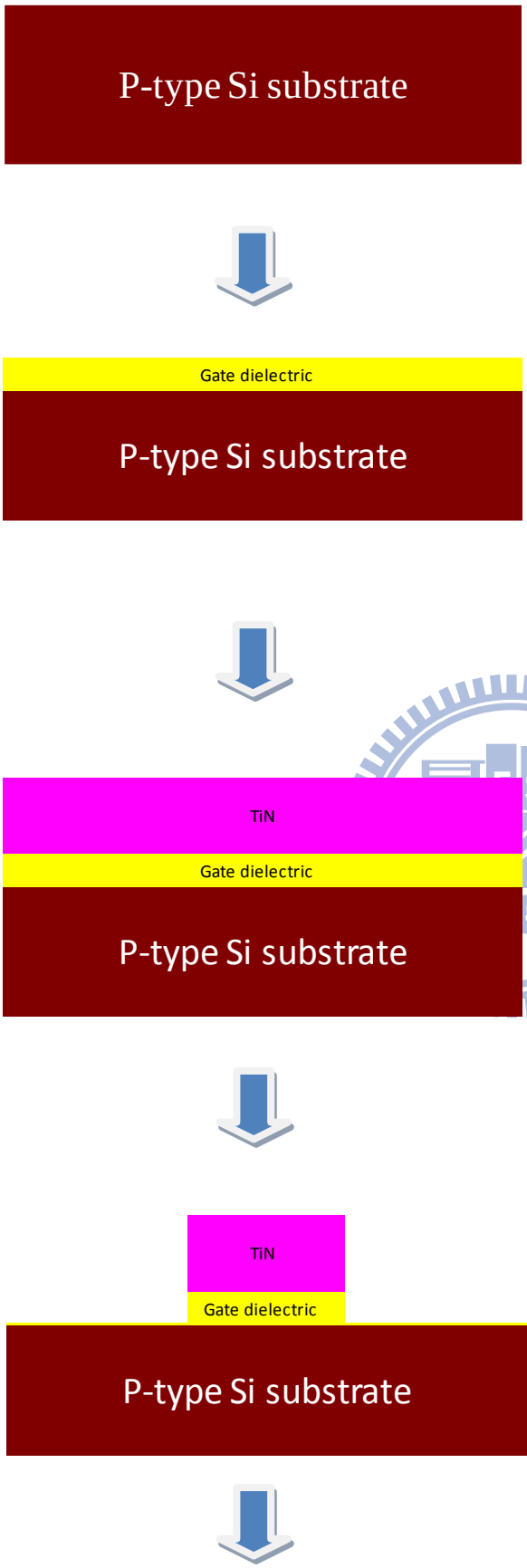
4-7 Summary

1's mask MOSFETs process was very fast to finish and it would be cost down. But series resistance problems were first of all to be solved. Because source and drain regions were without metal contact that caused series resistance increased. If series resistance problems would to be solved, their performance could discuss remarkably.

Table 4-1

Summary of I_{on0}/I_{off} ratio, S.S. and V_{TH0} on MOSFETs.

W/L 150um/30um Gate dielectric	I_{on0}/I_{off} ratio (@V_{DS}=1.2V)	S.S. (mV/Dec)	V_{TH0} (V)
01.HfO_2	4.59E6	94.5	0.58
02.HfSiOx (9% Si)	9.59E6	94	0.65
03.HfSiOx (12% Si)	1.92E7	91.5	0.67
04.HfSiOx (25% Si)	2.09E7	88	0.63
05.HfSiOx (40% Si)	1.17E7	84	0.59
06.HfSiOx (66% Si)	2.98E7	83	0.62
07.HfSiOx (77% Si)	4.42E7	80	0.63
08.HfAlOx (~7% Al)	9.34E6	89	0.62
09.HfAlOx (12% Al)	1.21E7	85.5	0.67
10.HfAlOx (40% Al)	1.21E7	82.5	1.11
11.HfAlOx (63% Al)	1.52E7	79.6	1.05



1. Si substrate

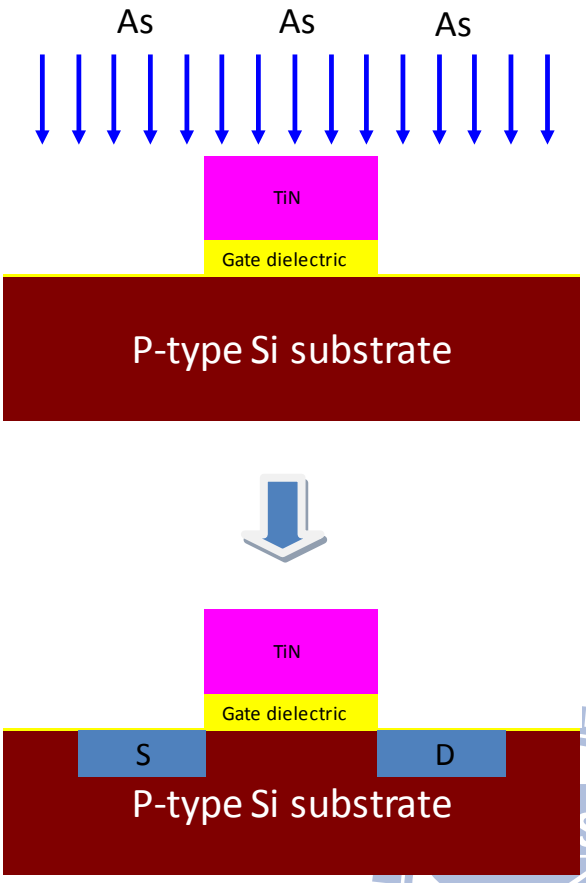
2. RTO 600℃, 10s+Spike 900℃
3. 4nm Gate dielectrics deposition by AVD
4. RTA 900℃, 30s

5. PVD TiN 250nm

6. Etching TiN

7. Etching gate oxide

Figure 4-1 Schematic flow charts for the fabrication of MOSFETs.



8. As ion implantation

9. Activation
(RTA 600℃,120s + 700℃,60s)

Figure 4-1 Schematic flow charts for the fabrication of MOSFET.

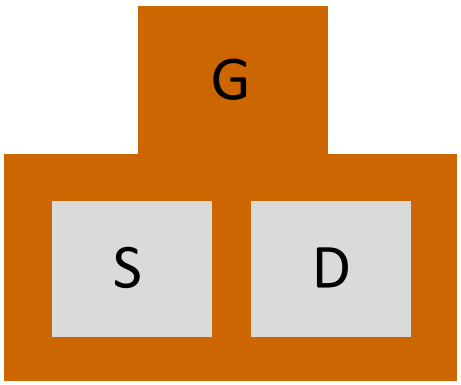
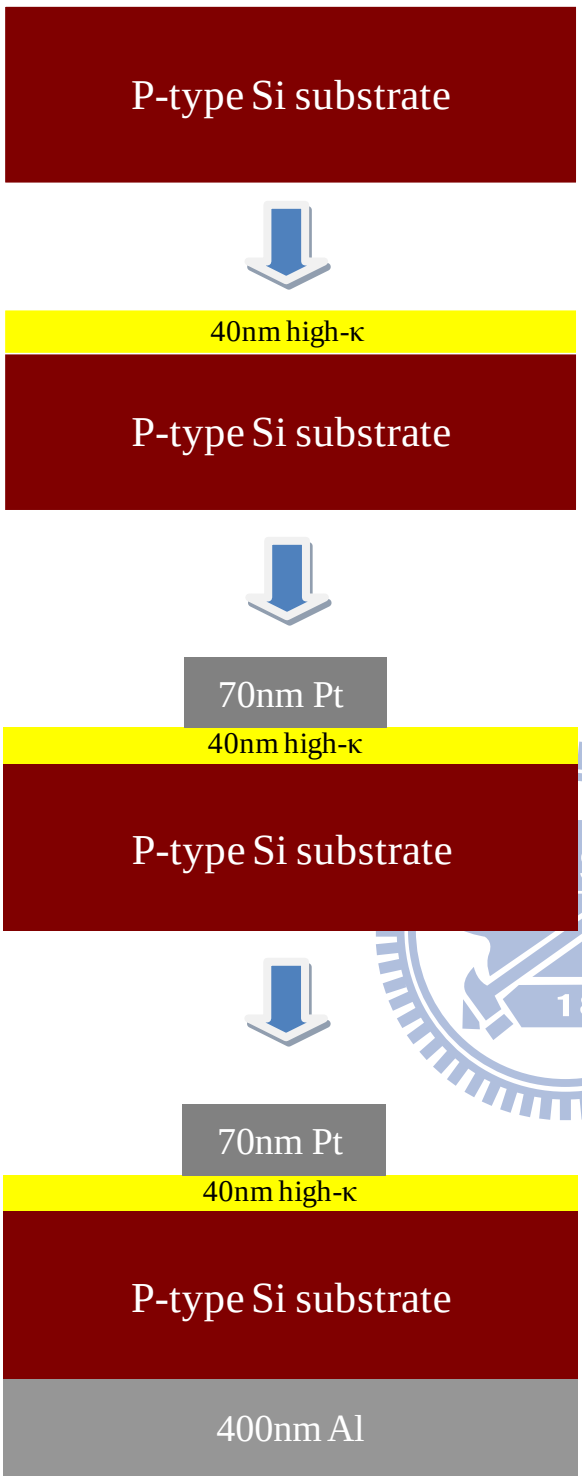


Figure 4-2 The plan-view Schematic for the fabrication of MOSFETs.



1. Si substrate

2. 40nm gate dielectrics deposition by AVD
3. Annealing by LPCVD system at 600°C, 24hr, in N_2 ambient.

4. Top Pt (70nm) electrode deposition by sputter system through shadow mask.

5. Backside Al (400nm) electrode deposition by thermal coater system.

Figure 4-3 Schematic flow charts for the fabrication of capacitors.

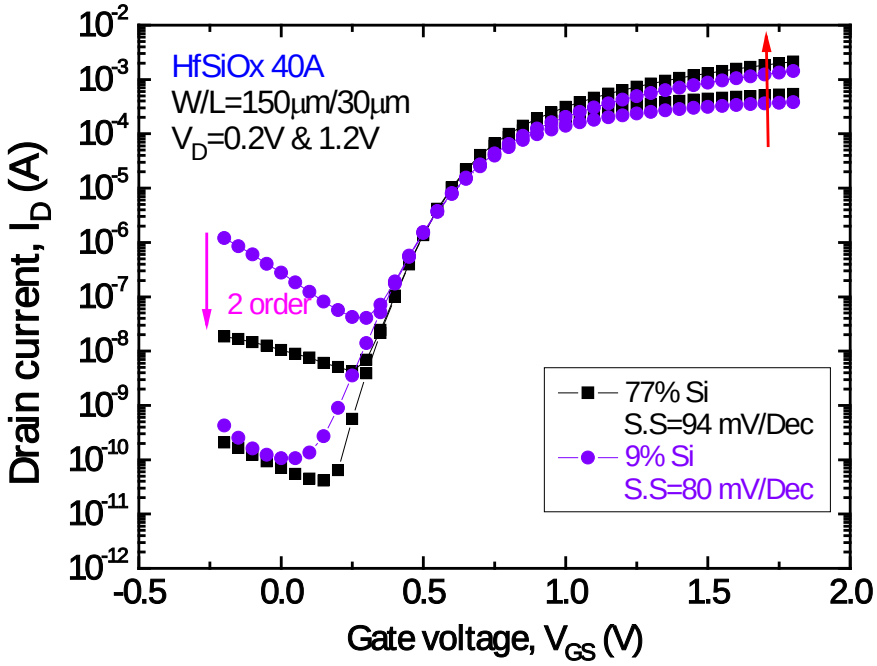


Figure 4-4 Comparisons of transfer characteristics at V_{DS} of 0.2 and 1.2V between HfSiOx incorporation of 9% and 77% Si.

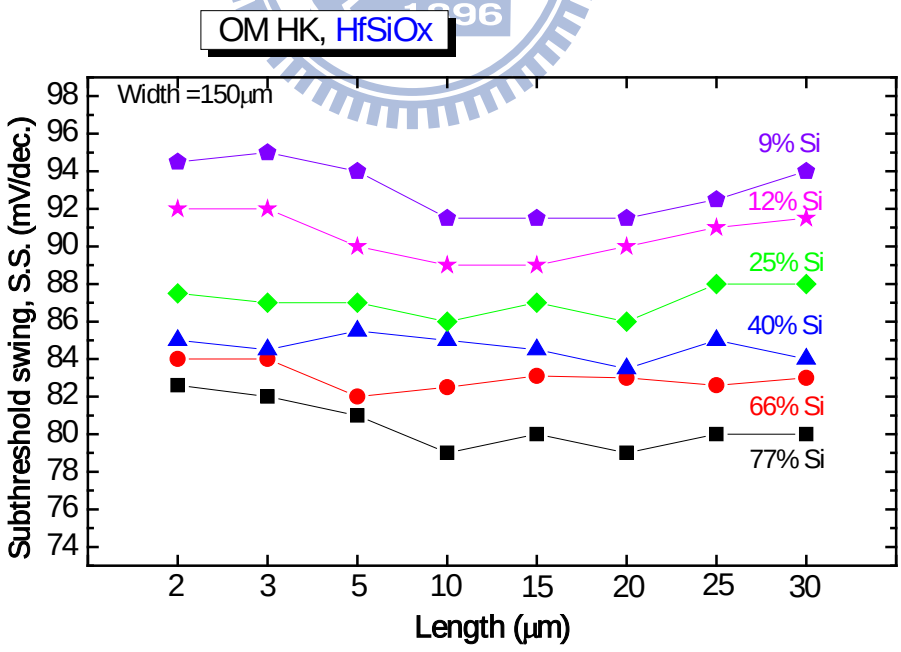


Figure 4-5 Comparisons with various composition ratios of HfSiOx for subthreshold swing.

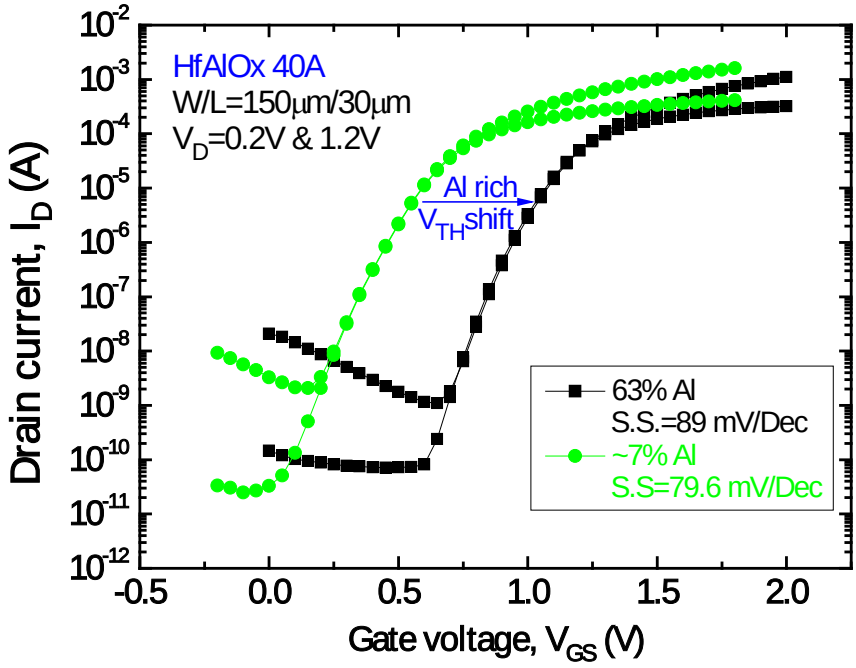


Figure 4-6 Comparisons of transfer characteristics at V_{DS} of 0.2 and 1.2V between HfAlOx incorporation of ~7% and 63% Al.

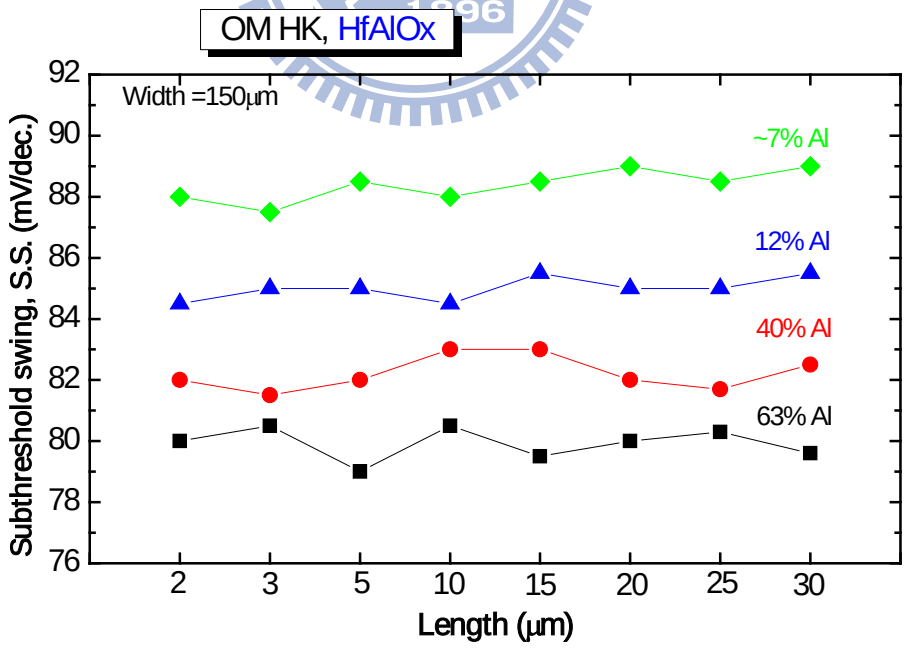


Figure 4-7 Comparisons with various composition ratios of HfAlOx for subthreshold swing.

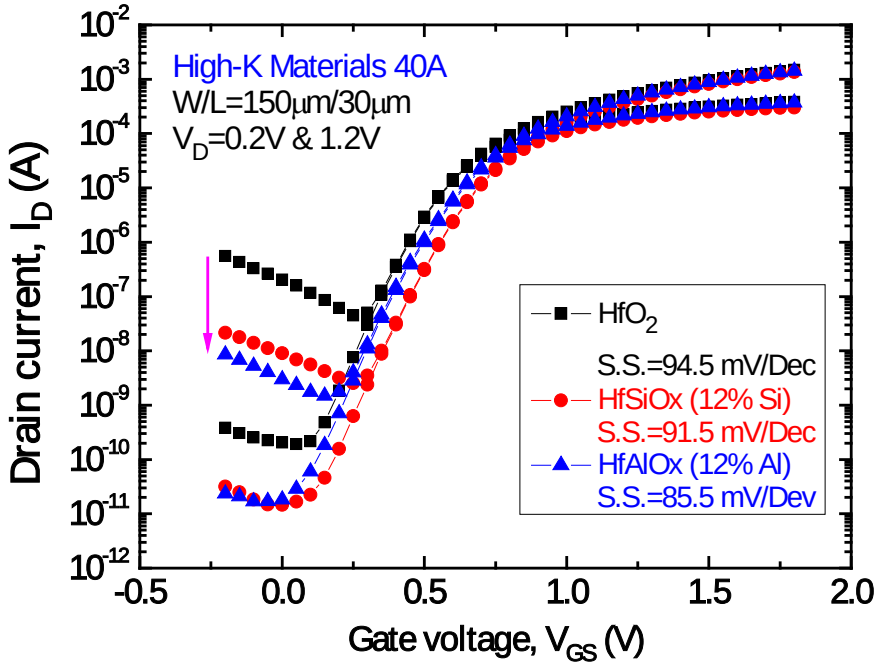


Figure 4-8 Comparisons with various High-κ materials for transfer characteristics at V_{DS} of 0.2 and 1.2V.

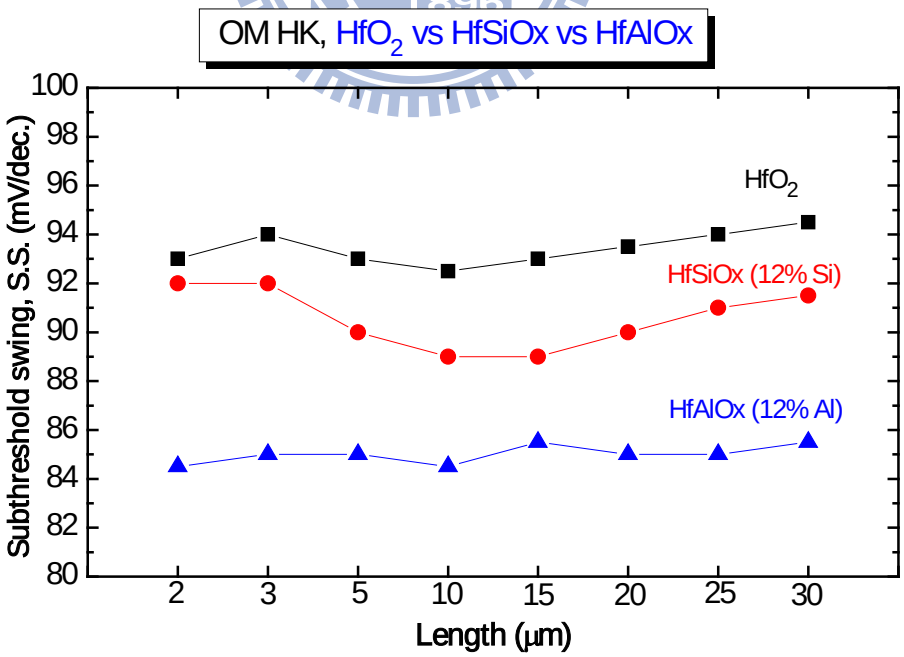


Figure 4-9 Comparisons with HfO_2, HfSiOx (12% Si) and HfAlOx (12% Al) for subthreshold swing.

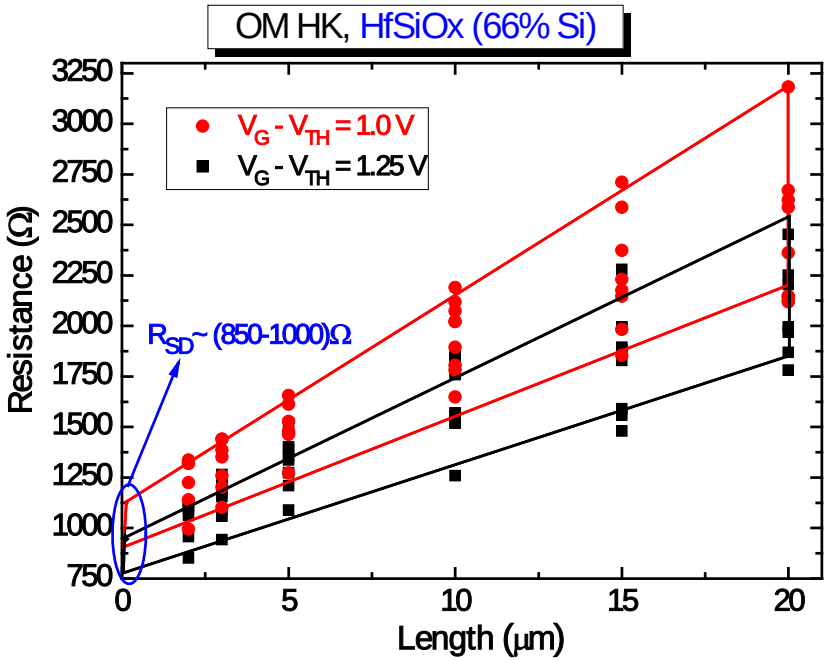


Figure 4-10 Schematic for source/drain series resistance of HfSiOx (66% Si) on MOSFETs.

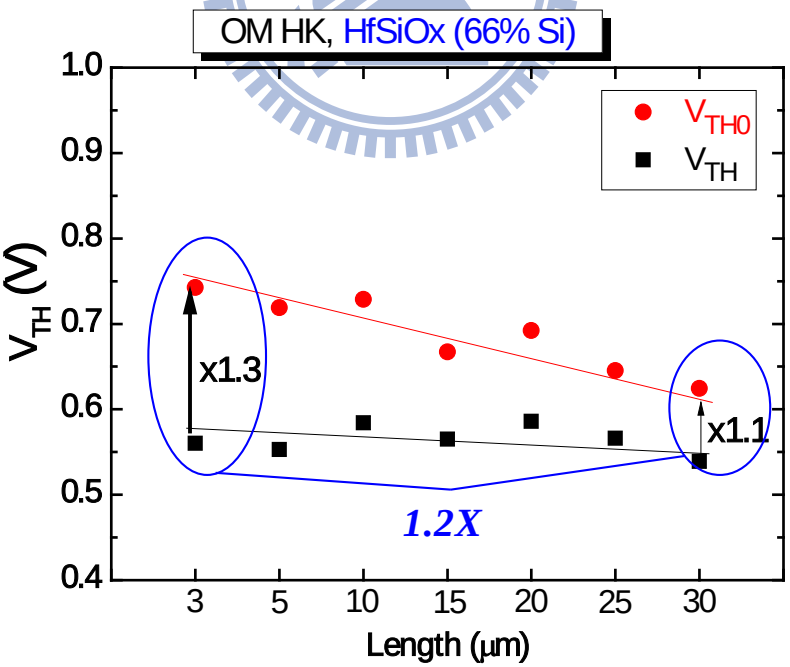


Figure 4-11 Comparison with threshold voltage correction between before and after condition on MOSFETs.

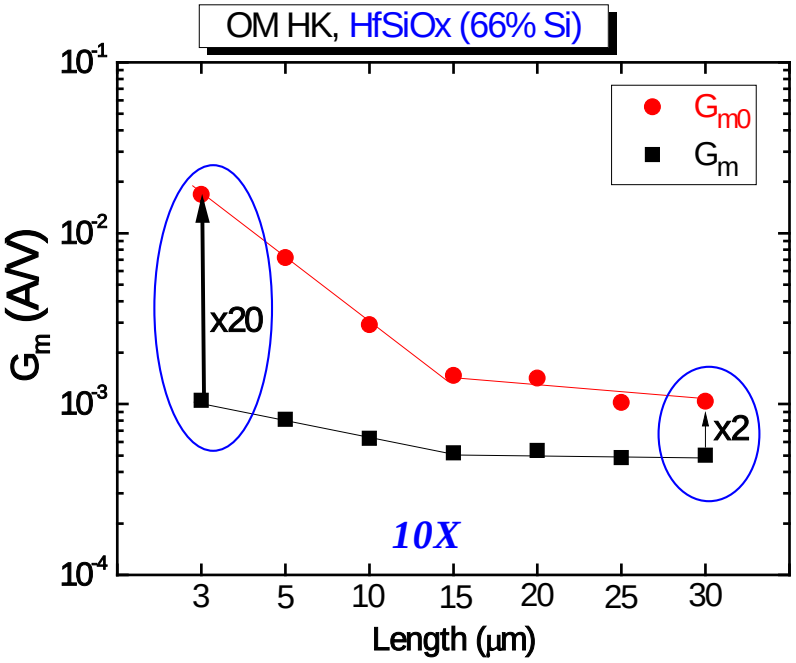


Figure 4-12 Comparison with conductance correction between before and after condition on MOSFETs.

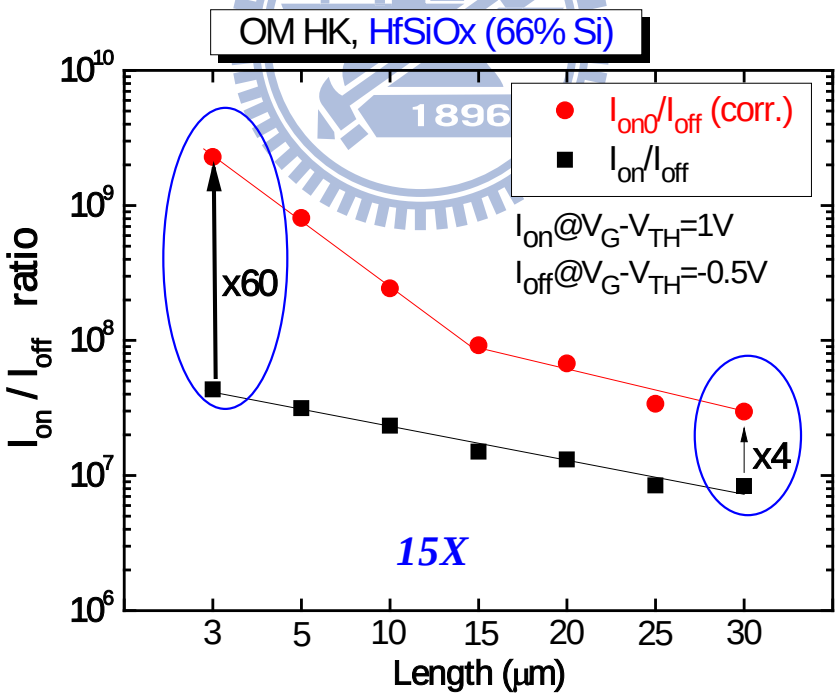


Figure 4-13 Comparison with on/off current ratio correction between before and after condition on MOSFETs.

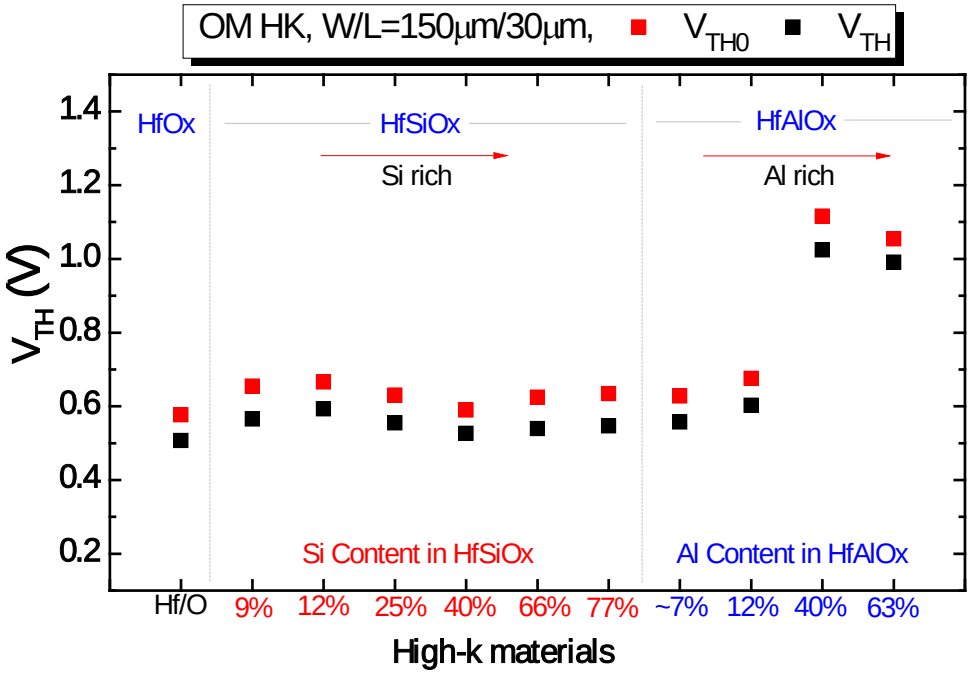


Figure 4-14 Summary of V_{TH} correction at V_{DS} of 0.2V for HfO_2, HfSiOx and HfAlOx films by R_{SD} correction method.

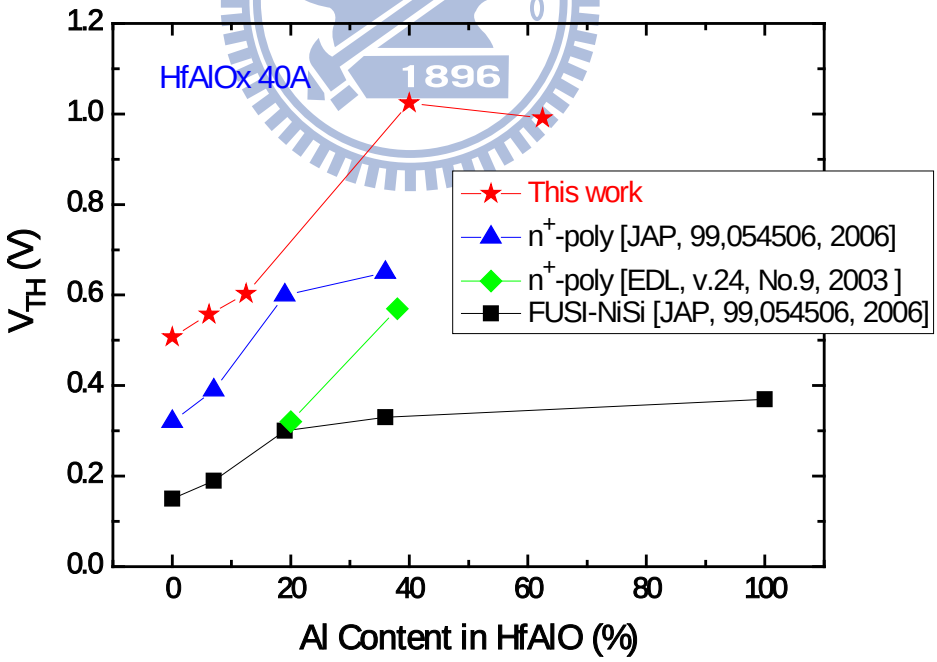


Figure 4-15 Comparison with various Al content in HfAlOx.

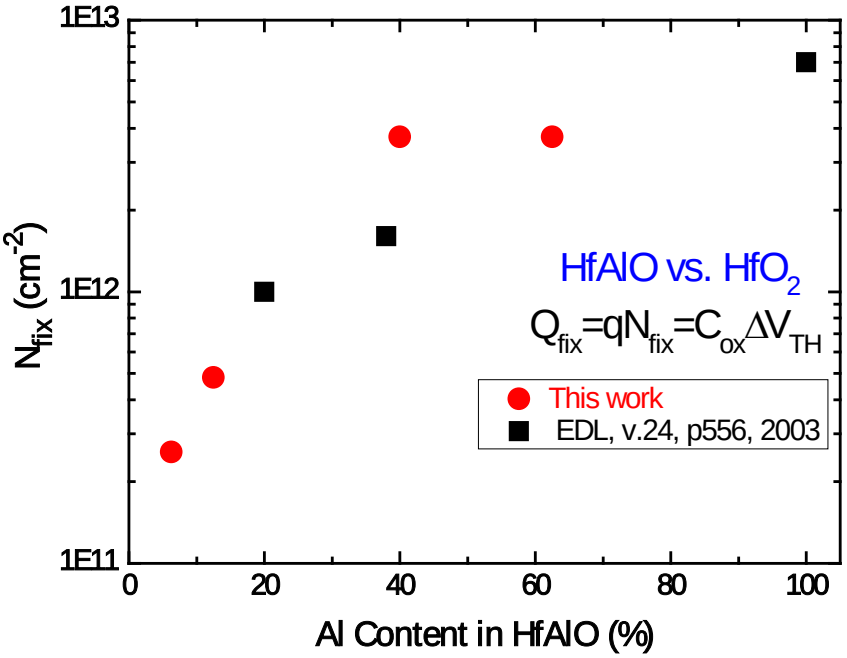


Figure 4-16 Calculated fix charge with various Al content in HfAlOx.

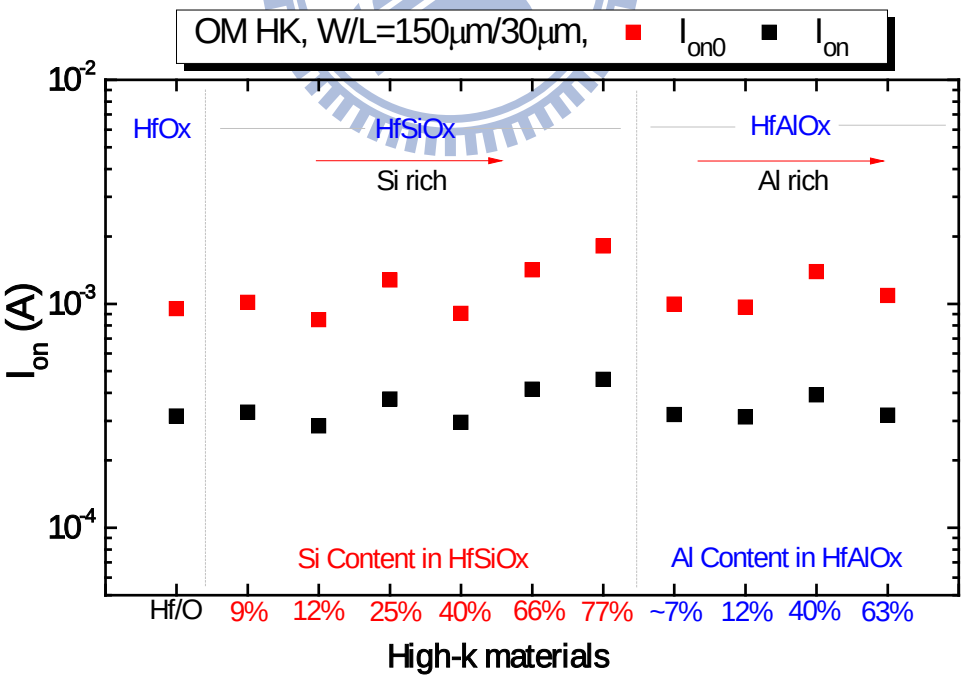


Figure 4-17 Summary of I_{on} correction at V_{DS}=0.2V for HfO_2, HfSiOx and HfAlOx films by R_{SD} correction method.

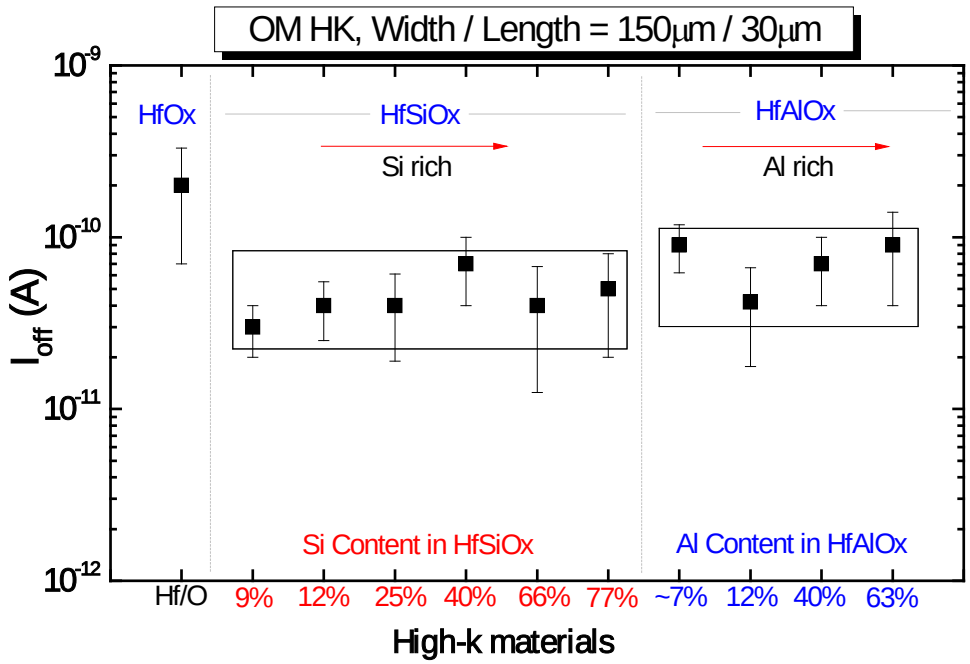


Figure 4-18 Summary of I_{off} correction at V_{DS}=0.2V for HfO_2, HfSiOx and HfAlOx films by R_{SD} correction method.

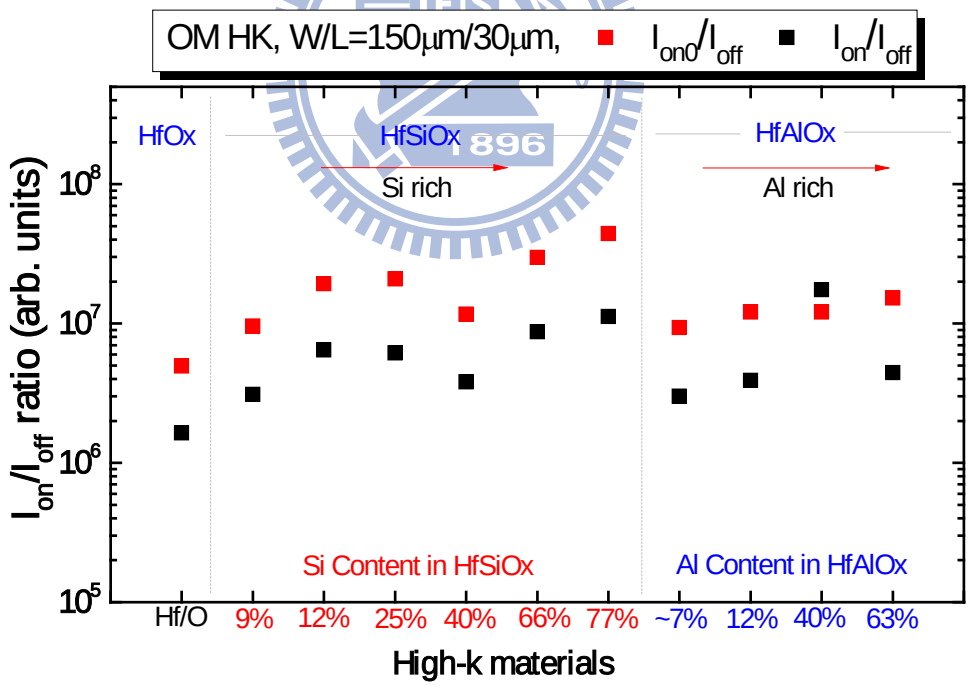


Figure 4-19 Summary of I_{on}/ I_{off} ratio correction at V_{DS}=0.2V for HfO_2, HfSiOx and HfAlOx films by R_{SD} correction method.

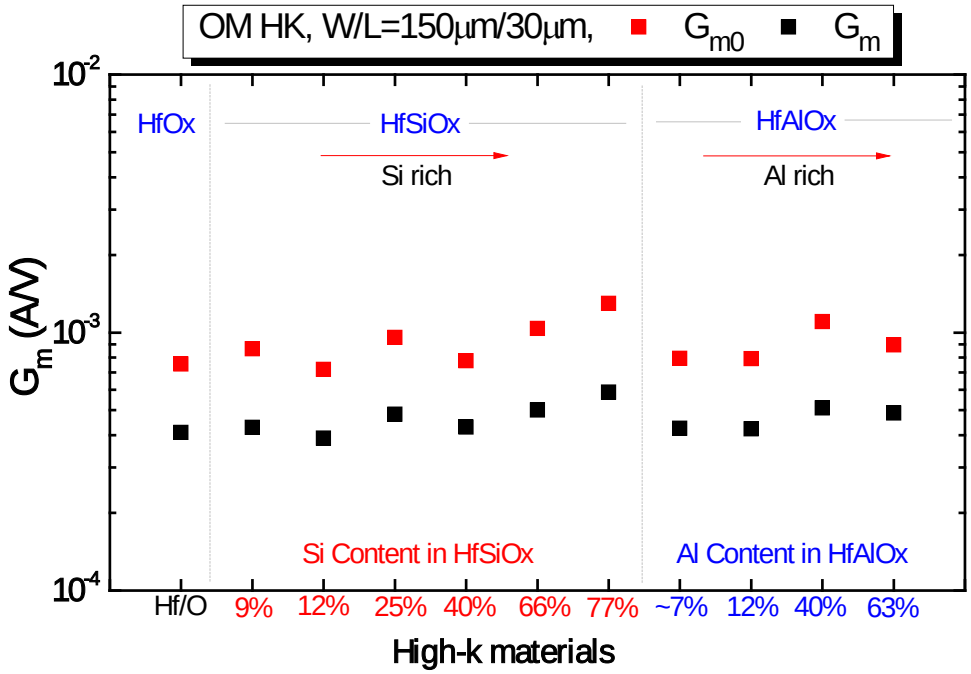


Figure 4-20 Summary of thansconductance correction for HfO_2, HfSiOx and HfAlOx films by R_{SD} correction method.

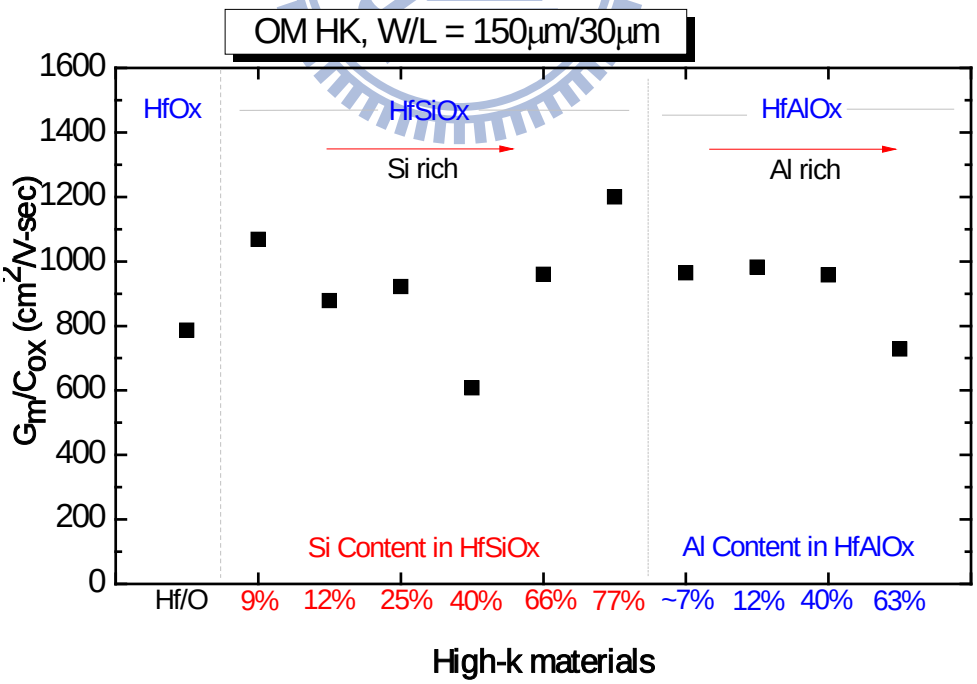


Figure 4-21 Summary of mobility correction for HfO_2, HfSiOx and HfAlOx films by R_{SD} correction method.

Chapter5

Conclusions and Future Prospects

5-1 Conclusion

In this thesis, we have employed advanced High-κ materials to fabricate high performance low-temperature thin film transistors.

Firstly, the deposition parameters of the newly-developed High-κ materials prepared by atomic-vapor deposition (AVD) system were investigated in chapter 2. However, the large leakage current would be caused by the polycrystalline structure of HfO_2 films. In contrast, the HfSiOx films exhibit better thermal stability and still keep the amorphous structure after temperature annealing. Moreover, the presence of unwanted interfacial layer with lower κ-value always exists between the thin High-κ gate dielectric and Si substrate.

Furthermore, we applied these High-κ materials to replace the conventional SiO_2 gate dielectric of LTPS TFTs and studied newly materials on the performance in chapter 3. High performance n-channel poly-Si TFTs using hafnium base High-κ dielectric including hafnium oxide (HfO2), hafnium silicate (HfSiOx) and hafnium aluminum oxide (HfAlOx) are demonstrated using low-temperature processing. Finally, the mechanisms of mobility degradation and leakage current of poly-Si TFTs incorporating High-κ gate dielectrics were investigated in chapter 3. The gate oxide stack structure was utilizing HfSiOx-IL film (66% Si) as bottom layer to suppress interface defects and smooth surface that obtained some of better electrical characteristics. However, using HfSiOx films can significantly eliminate these additional scatterings and achieve better mobility because of the thermal stability and better inherent properties. Nevertheless, High-κ gate dielectrics would lead higher electric field and induce severe GIDL current of poly-Si TFTs.

For the advanced MOSFETs application, deliberate surface treatments have to be done to suppress the interfacial layer growth in an effort to achieve lower EOT value by using these High-κ films in chapter 4.

The results and discussions are concluded and summarized as follows. We found that higher performance n-channel poly-Si TFTs and MOSFETs using hafnium-silicate gate dielectric was obtained with low-temperature-compatible processing. Higher I_{on}/I_{off} current ratio, smaller subthreshold swing, lower threshold voltage and higher mobility than deposited-HfO_2 gate dielectric were achieved at lower operation voltages. Our results suggest that HfSiOx is a potential candidate for the gate-dielectric material of future.

First successful correction of source/drain series resistance for 1's mask MOSFETs were deposited successfully advanced materials onto Si substrates using AVD system. It is an importance problem without metal contact on source/drain and we must to be solved or changed fabrication processes.

5-2 Future Prospects

Although many aspects and topics have been covered in our study, there are still several interesting works that could be organized and executed.

(1) The optimization of LTPS TFTs using High-κ gate dielectrics:

The High-κ TFTs were fabricated successfully in our study and exhibited better performance that replace of the sample with conventional deposited-SiO_2 gate dielectric. However, the characteristics of High-κ TFTs can be optimized by using more advanced methods and new structures. For example, better quality of poly-Si channel could be achieved by excimer laser annealing, which has been widely used in mass-production. As expected, enhancing the quality of deposited poly-Si films by laser annealing can bring about superior performance of High-κ TFTs. Also, as mentioned in the literature, High-κ

gate dielectrics would lead higher electric field and induce severe GIDL current of poly-Si TFTs. The adoption of lightly doped drain (LDD), multi-gate, and offset structures, which can reduce the electrical field between the drain and the channel of the TFTs, can be applied to suppress the deterioration of the off-state current when high-dielectrics are employed as gate dielectrics. Furthermore, High-κ materials with thermally-stable amorphous structure and higher κ value or the High-κ stack films also could be utilized to decrease the EOT and enhance the device performance. In addition, using different High-κ materials to improve interface quality and enhance superior performance poly-Si TFTs, Ex. stack structure, various Si or Al atoms incorporation into HfO_2 films as bottom layer on stack structure…etc. Finally, to accomplish the entire processing of the poly-Si TFTs in low-temperature, the metal gate and low-temperature activation methods have to be employed to achieve the goal.

(2) The fabrication of MOSFETs:

First successful correction of source/drain series resistance for 1's mask MOSFETs were deposited successfully advanced materials onto Si substrates using AVD system. Several key issues have to be overcome in the process of 1's mask MOSFETs in future. Firstly, the crystallinity of temperature to be modified by advanced materials, such as lower annealing temperature to avoid polycrystalline structure. And then, reducing source/drain series resistance was an important to enhance the device performance.

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Vita

姓　　名 ： 黃耀陞　　Yao-Sheng Huang

性　　別 ： 男

出生日期 ： 西元　1984　年　3　月　8　日

出 生 地 ： 高雄市

地　　址 ： 高雄市三民區義德路25號

學　　歷 ： 私立逢甲大學電子工程學系

（西元 2002 年 9 月 ~ 西元 2006 年 6 月）

國立交通大學微電子奈米科技產業碩士專班

（西元 2007 年 9 月 ~ 西元 2009 年 9 月）

碩士論文題目 ：

先進材料應用於低溫複晶矽薄膜電晶體和金氧半場效電晶體之研究

A Study of Low-Temperature Polycrystalline Silicon Thin Film Transistors and MOSFETs Using Advanced Materials