國立交通大學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

新式多晶矽奈米線 SONOS 元件製作與特性分析

Fabrication and Characterization of Novel Poly-Si Nanowire SONOS Devices

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中 華 民 國 九 十 八 年 八 月

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A Thesis

Submitted to College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of Master

in

Industrial Technology R & D Master Program on

Microelectronics and Nano Sciences

August 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年八月

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摘 要

在本篇論文中，我們發展一種新的製程方法，製作與分析多閘極結構的多晶矽奈米線 SONOS 元件。這些方法無須借助先進與昂貴的製程設備，即能形成極小尺吋的奈米線；同時經由製程步驟上的修改，共有三種不同閘極組態的元件，分別命名為 SG、ΩG 與 GAA，可以完成與比較，有助於我們探討多閘極對於奈米線的基本電性。我們的實驗數據顯示，在三種不同閘極組態的元件當中，由於奈米線具有較佳的閘極控制能力，使得 GAA 展現出更好的特性，因此具有較大的導通電流、抑制短通道效應、較好的次臨界幅擺(subthreshold swing)。

此外，在 SONOS 特性上，相較於其他兩種元件，近圓形的 GAA 奈米線通道展現出更好的寫入和抹除特性；在可靠度議題方面，GAA 奈米線也擁有最佳的的電荷儲存能力(retention)和耐操度(endurance)，它可以承受超過 10000 次的重複寫入/抹除，並且在室溫下十年後仍可維持大於 0.5V 的記憶窗(memory window)。

Fabrication and Characterization of Novel Poly-Si Nanowire SONOS Devices

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ABSTRACT

In this thesis, poly-Si nanowire (NW) SONOS devices with various multiple-gated (MG) configurations were fabricated by utilizing a simple and low-cost technique. With a slight modification in the fabrication procedure, three different types of MG configuration, namely, SG, ΩG, and gate-all-around (GAA), were realized in the fabricated devices. It thus allows us to unambiguously investigate the impacts of different MG configurations on the basic electrical characteristics. The experimental results show that much improved device characteristics with GAA devices are achieved as compared with the other types of devices, owing to the superior gate controllability over NW channel with the GAA structure, which results in a higher ON-current, suppressed short channel effects, and steeper sub-threshold swing (SS) for NWs.

For SONOS characterization, we confirmed that the round-shape GAA NW channel exhibits the best performance in P/E characteristics among all splits. For reliability issues, the GAA devices also exhibit good data retention and endurance characteristics. The memory window can be larger than 0.5 V after 10 years for a device after subjecting to 10^4 times of P/E cycles at room temperature.

Acknowledgment

兩年的時間過的好快，首先要感謝的是我的兩位指導教授，黃調元博士與林鴻志博士，不論是再做人處事、亦或是在學業指導都給予了我很大的協助。很慶幸當初有這個機會可以加入這麼棒的研究團隊，謝謝你們這兩年來提供我那麼好的學習機會與環境，讓我從中學習到許多寶貴的經驗，接下來也要感謝實驗室的其他同學們這兩年來給我的協助。首先非常感謝徐行徽博士以及蘇俊榮博士的照顧，沒有你們帶領我做實驗與經驗傳承，當然就不會有今天的我；也要謝謝陳威臣學長在我實驗遇到瓶頸時給我指點迷津、還有總是帶給實驗室歡樂的蔡子儀學長，在我正要開始跑實驗時 wafer 被打破的第一時間趕來救我；以及幾位畢業的學長姊們：大雄、大偉、Ally、漢仲、樟樟等，謝謝你們在課業上與實驗上的指教，也非常懷念我碩一那年的實驗室出遊，能和你們在同個實驗室真的是非常快樂。還有第一個認識的毛毛、格倫、君帆、阿嘎、政建、桀桀、濤濤和佑寧，每個都很優秀能跟你們互學習與成長真的很開心，謝謝你們!另外，實驗室裡的小碩一還有禹伶學妹總是把實驗室整理的乾乾淨淨，讓大家有個舒適的研究環境，感謝大家。

接下來要感謝身旁的朋友們。謝謝 CSD LAB 的黑妞、羅衡哥、凱凱哥、Pola、進哥，因為有你們讓我的碩士生涯增添不少樂趣，現在我要畢業了，你們也要繼續加油拿到博士學位，土地公會保佑你們的。另外，還要謝謝詠儒，有你的陪伴讓我在準備畢業的階段可以順利的完成。

最後要感謝最重要的家人。感謝我最愛的媽咪，謝謝妳提供我無虞的生活條件，讓我可以專注地安心學習，以及感謝在清大動機念博班的哥哥沒有你的遠見，我就不會在交大了，希望我的表現會讓你們感到驕傲，等我以後賺大錢一定會好好回報你們的

由衷的感謝以上每一個人，謝謝你們給我的幫助，希望大家永遠身體健康、幸福快樂。

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CHAPTER 1

Introduction

1-1 Overview of Nanowire Technology

Field-Effect Transistors (FETs) built on Si nanowire (NW) channels have recently received lots of attention. When the diameter or feature size of a stripe-structured material is smaller than 100 nm, it is called nanowire (NW). Nanowires (NWs) possess high surface-to-volume ratio, making it attractive for a variety of applications, including nano-scale CMOS[1], memory devices[2], NW thin-film transistors (TFTs) [3], light-emitting diodes (LEDs) [4], and sensors for detecting biological or chemical species [5]. Among theses applications, the NWs are typically prepared by either top-down or bottom-up methods [6]. The top-down method usually employs advanced optical or e-beam lithography tools and expensive materials to generate the NW patterns [7]. This technique is suitable for mass production with the capability of precise positioning and good reproducibility. On the other hand, the bottom-up method usually employs metal-catalytic growth for preparation of NWs [8][9]. Although bottom-up methods are significantly cheaper than top-down methods and more flexible for experimental purpose, they have their own imperfection. Namely, they suffer seriously from the difficulty in precisely positioning, alignment, and exact structure parameter of the NWs. For metal-catalyzed growth, metal contamination is a potential concern. In brief, the formation of NWs usually needs more complicated process flow and/or costly advanced tools and becomes an obstacle to their further evolution. To cope with this issue, we have recently developed a simple and

low-cost method to fabricate the multiple-gated (MG) NWs, which is different from the conventional top-down or bottom-up methods. In our approach, neither costly nor advanced equipment is required to form NWs patterns. Moreover, the NW is free from metal contamination which may incur in metal-catalytic grown NWs.

1-2 Multiple-Gated Structure

For IC technology, scaling is not simply shrinking device dimensions into nano-scale, but also increasing the gate controllability in order to suppress short channel effects (SCEs). [10] To deal with this issue, two methods for increasing the gate controllability are feasible, one is the use of high-κ materials as gate insulator, and the other is the adoption of multiple-gated (MG) structure. In recent years, a number of MG silicon-on-insulator (SOI) devices and fin-like structures have been investigated and proposed, which can effectively prevent the electric field originating from the drain side from penetrating into the channel.

Several types of MG structures have been published, such as double-gate [11], FinFET [12], tri-gate [13], Ω-gate [14], and gate-all-around (GAA) MOSFETs [15]. Among these configurations the last one is the most ideal MG structure but also the most difficult to fabricate. Channel potential of these devices is more effectively controlled by the MG structure as compared with the conventional planar structure, resulting in much better gate controllability and greatly enhanced device performance. In this work a modified process has been developed to fabricate MG NW devices, and details of the process flow will be described in Chapter 2.

1-3 Overview of SONOS Flash Memory

Scaling of NAND-type Flash memory has been aggressively pursued in recent years [16]. Low power consumption, low cost, and large storage capacity have triggered its

application in numerous new consumer products, such as ipod, digital cameras, MP3 players, personal digital assistants (PDAs), and other storage medium for personal appliances. Therefore, the industry of nonvolatile memory (NVM) is stimulated profoundly. NVM device retains the stored data even if the power is switched off. It is more convenient for data access and ideally suitable for portable electronic products. Furthermore, according to the International Technology Roadmap for Semiconductors (ITRS) [17], the technology node of flash memory has become an official index in recent years. Therefore, flash memory plays an important role not only in our daily life but also for semiconductor industry.

Up to now, floating-gate device is the mainstream of flash memory technology. However, high density and low cost are the basic requirements for flash memory, the conventional floating-gate structure has been facing several challenges in device scaling. Since the storage layer of floating-gate device is made of conducting poly-silicon, as the spacing between two neighboring cells is shortened, coupling interference may cause undesirable threshold voltage shift [18]. Thinning of tunnel oxide thickness for reducing the programming/erasing operation voltages is necessary for lowering the power consumption, however, floating-gate device also suffers from the large stress-induced leakage current (SILC) as tunneling oxide is thinner than 8 nm, which would degrade the reliability of memory device [19][20]. With these limits, it is difficult to further reduce the size of floating-gate flash memory.

Nowadays, silicon-oxide-nitride-oxide-silicon (SONOS) is widely viewed as the most potential candidate for succeeding floating-gate flash memory [21][22]. Instead of using a poly-silicon storage layer in floating-gate devices, the storage layer of SONOS devices is a nitride trapping layer. Since the charges are discretely stored in the ultra-thin nitride, the height of the devices is effectively reduced. More importantly, the issues of coupling effect and interference between neighboring cells are cleverly solved. Finally, the SILC pertaining

to the floating-gate flash memory lose its effectiveness in degrading the retention of the devices, since the charges are stored in the discrete traps of the nitride layer. Therefore, SONOS-type memory has been viewed as a potential candidate for the post-FG flash memory.

Today, many studies have devoted to the extension of SONOS structure to thin film transistor (TFT) for the purpose of system-on-chip (SOC) or system-on-panel (SOP) integration [23]. The TFT-SONOS memory with 3D vertical stacked configuration can not only increase the device density, but also reduce the power consumption [24].

1-4 Motivation of this Study

It's important that SONOS-type memory devices possess low programming/erasing (P/E) operation voltage, high P/E speed, and excellent reliability. Based on the background information stated in previous sections, NW SONOS represents a potential candidate for next-generation flash memory application. This stimulates us to carry out this study in which we investigate the related issues with our fabricated NW structures with three types of MG configurations. Because of good gate controllability of NWs, it is believed that performance improvements such as faster P/E efficiency can be achieved. Moreover, the impacts of different MG configurations are compared and discussed. The information should be helpful to understand how it affects the operation of NW devices and circuits.

1-5 Organization of the Thesis

This thesis is divided into four chapters. In Chapter 1, the related backgrounds and motivation of this study are described briefly. Detailed device structures and process flows for different types of MG NW devices characterized in this thesis are depicted and described in Chapter 2. Basic fundamental, P/E, and reliability characteristics of NW

SONOS memory are then presented and discussed in Chapter 3. Finally, we summarize all findings and results in this study and suggest the directions of future work in Chapter 4.

CHAPTER 2

Device Fabrication and Basic Operation Principles of SONOS Memory Devices

NW structures have been shown to be beneficial for enhancing the device performance, as introduced in the first chapter. However, the conventional NW formation processes, either top-down or bottom-up approaches, are cumbersome and costly. To alleviate this problem, we have recently developed a simple and low-cost method to fabricate NW devices with multiple-gate (MG) configurations [25]~[27]. In this chapter, we describe a modified scheme based one a previous one [28] to fabricate NW SONOS devices with various MG configurations. The new scheme has been employed to fabricate the devices characterized in this work.

2-1 Device Fabrication and Process Flow

A top-view of the device is shown in Fig. 2-1(a). Cross-sectional views of the device at different steps along Line $\overline{AB}$ in Fig. 2-1(a) are shown in Figs. 2-1(b) to 2-1(g). All devices in this work were fabricated on bare silicon substrate capped with a 200nm-thick wet oxide. First, a 50nm bottom nitride/50nm TEOS /30nm dummy nitride stacked layer was deposited sequentially by low pressure chemical vapor deposition (LPCVD) on the thermal oxide layer [Fig. 2-1(b)]. Then, the dummy nitride/TEOS stack was patterned by anisotropic plasma etching [Fig. 2-1(c)]. DHF etching was carried out in the subsequent step to remove

the TEOS layer with high selectivity to the top and underlying nitrides, and rectangular encroached cavities were formed at the two sides of the dummy patterns [Fig. 2-1(d)]. Next, a 100nm undoped amorphous silicon (a-Si) was deposited [Fig .2-1(e)]. By taking advantage of the excellent filling capacity of LPCVD process, the cavities formed in last step could be refilled by the deposited a-Si. Subsequently, an annealing step was performed at 600^{o}C in N_2 ambient for 24 hours to transform the a-Si into polycrystalline phase. Afterwards, source/drain (S/D) implant was carried out by P^+ implantation with an energy of 25 keV and a dose of $1x10^{15}$ cm^{-2}, followed by the definition of S/D photoresist patterns by a standard I-line lithography step. The main split conditions of this work were determined by the following steps. For the first type of structure, denoted as side-gate (SG), an anisotropic plasma etching was performed to remove the poly-Si not protected by the nitride. Poly-Si films that filled the previously-existing cavities would be left intact since they were protected by the nitride in the dry etching step. Hence, nanowire channels were simultaneously formed at this step in a self-aligned manner. Note that for the SG devices, the nitride layer was kept after the etching step, so that only one side of the NW channel is modulated by the gate, as shown in Fig. 2-1(f-1). For the second type of structure, the remaining nitride hard mask was subsequently removed by hot H_3PO_4. By continuously etching TEOS by a diluted HF (DHF) solution with controlled etching time, it's worth noting that the profile of NW channel is omega-shaped so it was denoted as omega-gate (ΩG) [Fig. 2-1(f-2)]. The third type of structure denoted as gate-all-around (GAA) was formed by continuously removing the bottom nitride by means of hot H_3PO_4 [Fig. 2-1(f-3)]. Finally, all structures were combined and capped with the ONO layer consisting of a 5nm-thick TEOS oxide as the tunneling oxide, a 8.5nm-thick nitride as the charge storage layer, and a 10nm-thick TEOS oxide as the blocking oxide. Then a 150nm in-situ doped n^+ poly-Si gate was deposited and patterned to serve as the gate electrode [Fig. 2-1(g-1) to (g-3)]. All devices were then covered with 250nm-thick oxide passivation layer. It is worth

noting that the resultant ΩG and GAA devices have semicircular and circular cross-sectional shapes, respectively. Also notice that no additional S/D dopant activation step was necessary. This is because the depositions of passivation TEOS film were performed at temperatures higher than 700^{o}C and the process time ~3.5hours was sufficiently long to for dopant activation purpose. Then contact holes and test pads were formed by standard metallization steps.

Figures 2-2 and 2-3 show the cross-sectional TEM picture of ΩG and GAA NW SONOS-devices along Line $\overline{AB}$, respectively. It can be seen that the shape of NWs is nearly circular while the dimensions and shapes of ΩG and GAA are similar to each other even though different etch steps were performed to them. The channel width of SG or the gated vertical edge of the NW, is about 20nm for each NW channel, as shown in Fig. 2-4. For ΩG and GAA devices, the channel width is increased to 50 and 60nm, respectively, owing to the fact that additional NW edges are incorporated as the conductive channel. Furthermore, there are two NWs in one device, the effective channel width is doubled to 40, 100, 120nm for SG, ΩG, and GAA, respectively.

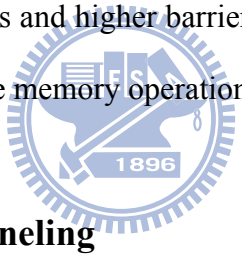
2-2 Program/Erase Mechanisms of SONOS Flash Memory

Before introducing the SONOS flash memory device, we present the operation mode about programming and erasing in memory cells. Several program/erase mechanisms have been widely studied for flash memory operation, including channel hot electrons injection (CHEI), Fowler-Nordheim tunneling (FN tunneling), and band-to-band tunneling (BTBT). These mechanisms will be discussed in the following sections.

2-2.1 Channel Hot Electrons Injection

The hot-carrier-effect (HCE) on MOSFETs had been discovered since 1970s [29]. The

scheme of HCE is shown in Fig. 2-5. It occurs because of strong lateral electrical field in the pinch-off region of the channel while a transistor is biased under a sufficiently high gate voltage (V_G) and a high drain voltage (V_D). Under the situation as $V_D \geqq V_{DSAT}$, a pinch-off point occurs near the drain side and major voltage drop along the channel occurs in the region between the pinch-off point and the drain junction. The channel electrons will be accelerated in this region. Some will gain sufficient energy and become "hot carriers", known as channel hot electrons (CHEs). Then, parts of the high energy carriers may cause the impact-ionization near the drain region which will create new electron-hole pairs. Through scattering, some of these electrons can keep enough energy to overcome the barrier height and inject into the gate dielectric, as is described by the well-known "lucky electron model" [30]. On the other hand, the injection for holes is much more difficult than electrons owing to the heavier effective mass and higher barrier height. As a result, hot-hole injection is seldom employed in non-volatile memory operation.



2-2.2 Fowler-Nordheim Tunneling

According to classical theory, tunneling of electrons in the channel region through gate dielectrics to the gate terminal is forbidden, when electron energy is lower than the barrier height. This is not true as quantum mechanic is considered, especially when gate oxide thickness becomes very thin. Based on the strength of electric field across the insulator, the tunneling mechanism can be categorized into two types. The first type occurs when the electric field built up across tunneling oxide (Eox=$\frac{V_{OX}}{t_{OX}}$) is higher than $\frac{\Delta V_C}{t_{OX}}$, where ΔV_C is the conduction barrier height at oxide/Si interface, hence electrons in Si channel may tunnel into the conduction band of oxide. Such process is illustrated in Fig. 2-6(b) and is called F-N tunneling [31]. The other type is direct tunneling (DT) [32] occurring when Eox is lower than $\frac{\Delta V_C}{t_{OX}}$, where electrons pass through oxide and inject directly into the gate

electrode, as shown in Fig. 2-6(c). DT process dominates only as the oxide is sufficiently thin, say, 43 nm or thinner. Comparing the F-N tunneling and DT in flash memory application, DT mechanism may cause leakage issue which degrades the retention and reliability properties of the devices.

2-2.3 Band-to-Band Tunneling

Gate induced drain leakage (GIDL) is a major issue in controlling the off-state leakage current for nano-scale MOSFETs. GIDL is induced by the band-to-band-tunneling (BTBT) process in the overlapped region of n^+ drain and gate [33]. When a highly negative voltage relative to n^+ drain region is applied to the gate, the strong electric field results in deep-depletion within the n^+ region adjacent to the oxide interface and drain junction, as illustrated in Fig. 2-7 (a), and the energy band diagram shown in Fig. 2-7 (b).Due to the high electric field or assistance by traps in the gap, electrons may tunnel from the valance band into the conduction band, thus named BTBT. At the same time, portions of the holes left in the valence band may gain enough energy in depletion region and surmount the oxide barrier height into the storage nitride layer. However, the depletion region will accelerate excess holes to flow into substrate. Some of these hot holes would overcome the barrier high of tunneling oxide to inject into nitride trapping layer and recombine with the electrics. Such process can be used to erase the electrics stored in the nitride layer, named as BTBT Hot-Hole erase.

2-3 Devices Measurement and Operation Principles

2-3.1 Electrical Characterization and Measurement Setup

In this study the electrical characteristics of the fabricated devices are all characterized by a measurement system constructed by an HP4156 semiconductor parameter analyzer and

Interactive Characterization Software (ICS) program, an Agilent-E5250A switch, and an Agilent-8810A pulse generator.

2-3.2 Basic Program/Erase Operation Principles

There are several approaches for P/E operation in flash memory device just as mentioned in previous chapter. Since the existence of potential barriers caused by the defects presenting in the grain boundaries of the poly-Si NW channel would hinder the acceleration of the electrons from source to drain, the CHEI method is not appropriate for programming operation of poly-Si NW SONOS device. Therefore, in this study we employ FN tunneling mechanism for P/E operations of the fabricated NW devices. For programming operation, both source and drain are grounded, and a positive voltage is applied to the gate in order to cause a strong electric field and the tunneling of electrons induced in the channel through the thin tunnel oxide layer and captured by the trapping centers in the storage nitride layer. For erasing operation, both source and drain are also grounded, and a negative voltage is applied to the gate in order to de-trap the electrons stored in the nitride layer.

2-4 Reliability of SONOS Flash Memory

Nonvolatile flash memory has become a necessary part in modern portable storage products. For practical application, the NVM need to conform to some reliability requirements, such as data retention capability and program/erase (P/E) cycling endurance. It is important that two main characteristics to estimate the practicability and reliability of memory in determining the life-time of digital products.

2-4.1 Retention

The retention of NVM refers to the ability of the memory cell to keep the trapped

charge over a period of time to retain the stored data information. In general, the threshold voltage of the programmed (erased) state usually decreases (increases) with retention time after P/E cycles result in memory window shrinkage [34]. All possible charge loss paths are illustrated schematically in Fig. 2-8. Generally speaking, the charge escaping path from nitride trapping layer could be categorized into two types, one is Frenkel-Poole (FP) emission mechanism [35], and the other is tunneling mechanism through either tunneling oxide or blocking oxide. The combination of FP emission and field-enhanced thermal excitation (TE) can be explained by the movement of trapped charges from site to site within the bandgap, especially when an electric field is applied. The other data loss mechanism is tunneling effect, the trapped electrons in the nitride layer could tunnel back to the conduction band of Si-substrate (trap-to-band tunneling, T-B), or inject into the interface trap between Si-substrate and tunneling oxide (trap-to-trap tunneling, T-T). In addition, holes from Si valence band may tunnel into the nitride trapping center under the influence of the internal electric field (band-to-trap tunneling, B-T) [36].

For commercial products, the standard retention time is 10 years with the memory window larger than 0.5V [37]. The tunneling oxide thickness and quality in NW SONOS devices has evident effect on data retention. Thinner tunneling oxide will lead to faster P/E efficiency, but charge storage capacity will become worst due to the shorter tunneling length. If there exist a lot of defects in the tunneling oxide and the interface, which may speed up the charge lost rate by trap-assisted tunneling. What mentioned above are all the challenges that SONOS type memory needs to face.

2-4.2 Endurance

Endurance refers to a reliability concern of a NVM device, which is defined by the number of P/E cycles that can still retain acceptable P/E window on device without failure. However, P/E operations of flash memory are applied with a very high voltage hence the

energetic carriers would degrade the tunneling oxide and nitride trapping layer. More and more defects like oxide traps and interface trap states would act as trap-assisted-tunneling sites for data lost paths, resulting in the degeneration of the device performance. For SONOS-type memory, electrons are stored in discrete traps in the nitride layer rather than the floating-gate in a conventional Flash device, hence theses electrons will not lose entirely as the aforementioned defects are generated. It is one of the reasons why SONOS is viewed as an important role for next-generation flash memory. Today, most commercially available NVM products endurance standard are at least 10^4 P/E cycles [38]. For reducing stress-induced damage in the tunneling oxide, operation voltage must be reduced. Even though, there is a dilemma between applied voltage and P/E speed. We have to optimize all related parameters, for example, the thickness of etch ONO stack layer, operation time, and modes, etc.

CHAPTER 3

Characteristics of Nanowire SONOS Memory Devices

3-1 Basic Transfer Characteristics of Nanowire SONOS Memory Devices

Figure 3-1 shows the I_D-V_G curves of the three types of NW SONOS devices stated in previous chapter. In the figure all measured devices have channel length of 0.4μm and equivalent gate oxide thickness of 20nm. It can be seen that the GAA device depicts better subthreshold swing (SS) and lower threshold voltage (Vth) than ΩG and SG devices. The DIBL phenomenon is negligible for the GAA devices, which can be attributed to the ultra-thin channel body and much improved gate controllability. These observations are expected since among the three types of NW devices, the GAA split has its NW channels surrounded by the gate while the SG split which has only one of the NW surface under gate modulation has the worst SS and the lowest on-current. The improvement of SS for the GAA device can be attributed to the improved (gated)-surface-to-volume ratio with such configuration. GAA device also has the highest on-current. The on-current difference among the splits cannot be explained by the difference in effective channel width alone, since the ratios of on-current of the splits differ significantly than the ratios of effective width. Volume inversion effect [39] is postulated to occur in the tiny NW and affect the device performance.

Figures 3-2 to 3-4 show the transfer characteristics of the three types of NW SONOS devices with different channel length. The I_D-V_G curves of SG devices shift as channel length varies, indicating that V_{TH}, SS, and on/off current are strongly related to the channel length. This condition is different for GAA device as shown in Fig. 3-4 in which the on-current significantly increases with reduced channel length. The drain induced barrier lowing (DIBL) is obvious for ΩG and SG device with channel length of both 0.4μm and 1.0μm, which means the effect in the short channel is profound. The situation is improved with the GAA structure. The I_D-V_G characteristics of GAA devices with 5μm channel length shown in Fig. 3-5 indicate that the devices are obviously nonfunctional. The current is below the detection limit of the measurement system. One possible origin for this observation is that the NW channels have been broken during the removal of the sacrificial dielectrics. In Fig. 3-6, as the channel length of the NW increases, the tiny NW body is harder to sustain the stress as the channel is suspended, and leads to the collapse. Once the NW collapses, disastrous failure referred to as "stiction" or "static friction" occurs [40].

In Fig. 3-7 the measured V_{TH} versus channel length of 0.4, 0.7, 1, and 2μm are plotted for GAA, and 0.4, 2, and 5μm are plotted for ΩG and SG. Note that the symbol represents the mean value and the error bar spans the range of measured V_{TH}. Moreover, the V_{TH} roll-off seems less obvious for GAA NW devices. Note that full depletion of the channel is expected because of the sufficiently small dimension of our NWs. Figures 2-2 and 2-3 show that the three types of NW devices almost possess the same cross-sectional dimensions in the channel region, hence SG with only one side of its NW channels gated has the thickest effective depletion width. On the other hand, the GAA device nominally has a gate-all-around configuration, thus has the thinnest effective depletion width. Therefore, the GAA device has the smallest V_{TH} among the three types of NW SONOS devices, as shown in Fig. 3-8. However, our TEM analysis shows that the "GAA" devices with channel length equals to or larger than 2μm, the central portion of the NW channel actually touches the

bottom of the substrate. An example of TEM image is given in Fig. 3-9. This means those devices with channel length $\geqq$ 2 μm are no longer with GAA configuration, while the effective channel width is diminished. This would certainly degrade the current drive, as shown in Fig. 3-4.

3-2 Program/Erase Characteristics of Nanowire SONOS Memory Devices

As mentioned in Sec. 2-2, the SONOS devices in this work are programmed and erased by F-N tunneling. As shown in Fig. 3-10(a), the I_D-V_G curve of a programmed GAA NW device is nearly parallel to that of fresh state. Figure 3-10(b) shows the V_{TH} shift versus programming time of GAA NW device with gate bias of 10V, 11V, and 12V. For simplicity, the V_{TH} is defined as the gate voltage at drain current of 1 nA. For a fixed period, the V_{TH} shift increases with increasing gate bias. It can be seen that memory window of 2.2V can be achieved within 10 microsecond (μs) with applied voltage of 11V. We utilize this operation condition to program fresh devices for investigation of erasing characteristics. Figure 3-10(c) is the result of V_{TH} shift as a function of erasing time with gate bias of -9V, -10V, -11V, respectively. The V_{TH} shift increases with increasing gate voltage and/or operation time. It can be seen that the rate of V_{TH} shift slows down when erasing time is longer than 1ms with gate bias of -11V. Similar situation also happens for the other two erase conditions (-10V and -9V) shown in the figure, although the erase time for saturation to occur is longer. Moreover, the saturation (absolute) value of V_{TH} shift is smaller for gate bias of -11V than that of -10V. Basically the trend is similar to what observed and reported previously and can be explained by the tunneling of electrons from the gate through the blocking oxide to the nitride [41], which tends to balance the erasing mechanism by FN hole injection from the

channel and results in the V_{TH} saturation phenomenon mentioned above. Fig. 3-10(d) shows energy band diagram of the SONOS-device with n^+ poly-Si gate. Owing to the relatively low barrier height of n^+ poly-Si gate for electrons, the electron tunneling mechanism from the gate is preponderant which may seriously limit the erasing voltage as well as the window size. To relieve this concern, a new gate material with higher work-function, such as p^+ poly or TaN [41], would be helpful.

Fig. 3-11(a) shows the I_D-V_G curves of a programmed ΩG NW device before and after programming. A memory window of 1.2V can be achieved within 50 microsecond (μs) with applied voltage of 11V. Figure 3-11(b) is the V_{TH} shift versus programming time of ΩG NW device with gate bias of 10V, 11V, and 12V, respectively. Figure 3-11(c) is the result of V_{TH} shift as a function of erasing time with gate bias of -8V, -9V, -10V, respectively. The I_D-V_G curves of a SG NW device before and after programming is shown in Fig. 3-12(a). A memory window of 1.5V can be achieved within 0.1 millisecond (ms) with applied voltage of 11V. Figure 3-12(b) is the V_{TH} shift versus programming time of SG NW device with gate bias of 9V, 10V, and 11V, respectively. Figure 3-12(c) is the result of V_{TH} shift as a function of erasing time with gate bias of -8V, -9V, -10V, respectively.

The above results indicate that the GAA devices have the largest program window and the fast P/E speed among the three types of devices, which is attributed to the advanced GAA structure, leading to superior gate controllability. The explanation about the impact of different gate structure on the P/E characteristics is given in the next section.

3-3 Reliability Characteristics of Nanowire SONOS Memory Devices

3-3.1 Retention Characteristics

Figure 3-13 depicts the retention characteristics of GAA NW SONOS-devices under

two different P/E conditions. All electrodes are grounded during the period of retention measurement. As can be seen in the figure, as the devices receive P/E gate bias of 11V(10μs)/-10V(10ms) and 10V(10μs)/-9V(10ms), the memory window can be maintained at about 0.9V and 0.5V, respectively, after 10 years at room temperature. Figure 3-14 shows the results for the ΩG NW device programmed by gate bias of 11V for 50μs, and -9V with 50ms for erasing. The memory window is nearly 0.4V after 10 years at room temperature. Figure 3-15 shows the results for the SG NW device programmed by gate bias of 11V for 0.1s, and -9V for 1s for erasing, the memory window can be larger than 0.5V after 10 years at room temperature. It is worth noting that the tunneling oxide was fabricated by LPCVD TEOS, and a lot of defects may exist in the channel/tunnel oxide interface, as mentioned in last section, which may speed up the charge lost rate by trap-assisted tunneling. Therefore, field-enhanced trap-assisted tunneling and F-P emission through oxide trap are considered to be the two major charge loss mechanisms in our NW SONOS-devices. For erased state, the V_{TH} value is relatively stable after 10^4 seconds as compared with the programmed state, especially for the GAA split.

3-3.2 Endurance Characteristics

There are two P/E specifications applied to the GAA SONOS devices for endurance tests with P/E conditions of 11V(10μs)/-10V(10ms) and 10V(10μs)/-9V(10ms), and the results are shown in Figs. 3-16 (a), (b). The memory windows in the beginning are about 2.3V and 3.2V for the two P/E conditions. As stressing cycles increase, the windows decrease from 2.3V and 3.2V for the two cases to 1.7 and 2.7V, respectively. The results show that the stressing cycles can be more than 10^4 with acceptable memory window. As cycle number increases, the threshold voltages for both programmed and erased states are observed to move upward while the memory window narrows due to the larger shift in erased state, as shown in Fig. 3-16(a). The decreased subthreshold swing is ascribed to the

degradation of tunneling oxide with additional interface states generated, and the memory window closure is attributed to the degradation of the nitride layer, as shown in Fig. 3-16 (b). In the figures the solid lines represent the fresh P/E states, and the dashed lines are the transfer characteristics after 10^4 P/E cycles. It is clear that the subthreshold swing degradation is one of the factors responsible for the V_{TH} increase. However, the programmed and erased curves after 10^4 P/E cycles appear to be parallel to each other, implying the amount of electrons "erased" from the storage nitride decreases with increasing P/E cycles, although the reason is not clear yet.

Next, we measured the data retention characteristics again to inspect the quality of tunneling oxide. Figs.3-17(a) and (b) show the retention characteristics of GAA SONOS-devices before and after 10^4 P/E cycles with two P/E specifications. Compared with fresh devices, the V_{TH} of stressed devices does not show obvious change in the rate of V_{TH} lowering in programmed state in Figs. 3-17(a) and (b). For erased state, the erased device after 10^4 P/E cycles shows somewhat more increase in V_{TH}. According to a previous study [42], this might be caused by the de-trapping of holes contained in the tunneling oxide. Figure 3-18 shows the I_D-V_G characteristics of a device after 10^4 P/E cycles with P/E specifications of 11V10 μs/-10V10ms. The dashed lines were measured right after the P/E operation, while the solid lines were measured 10^4 sec after the P/E operation. It is obvious that the memory window shrinks from 2.2V to 1.7V. For the erased state, de-trapping of holes is evidenced with the positive shift of threshold voltage.

Figures 3-19 (a) and (b) show the endurance characteristics and I_D-V_G characteristics before and after 10^4 P/E cycles of ΩG NW SONOS devices. From Fig.3-19(b) it is clear that the subthreshold swing worsens after 10^4 P/E cycles, while the memory window is kept at about 1.5V. Because we define V_{TH} at I_D=1nA, the V_{TH} shift in both programmed/erased state comes mainly from SS degradation.

Next, we use the MAXWELL SV simulation software [43] to analyze the electric field

of GAA devices and ΩG devices, and the results are shown in Figs. 3-20(a) and (b). In the simulation analysis, as the two structures are compared, we can clearly see that GAA NW SONOS has symmetric profile and uniform electric field. This explains why the GAA split exhibits the best performance in all regards among the fabricated samples. Moreover, crossing of the two subthreshold curves of the erased state before and after 10^4 cycles is observed in Fig.3-19(b). Such phenomenon is postulated to be caused by the non-uniform electron trapping in the nitride layer due to the non-uniform field distribution (Fig. 3-20(b)).

To sum up, the superior basic transfer and memory characteristics evidence the potential of the GAA NW SONOS-devices for future flash memory applications.

CHAPTER 4

Conclusion and Future Work

4-1 Conclusion

Multiple-gate (MG) configuration promotes gate controllability and the tiny NW structure reduces the impact of defects in the channel. In this thesis, we propose and demonstrate a simple and flexible way to fabricate novel MG poly-Si NW SONOS devices without resorting to advanced lithographical tools like e-beam direct writers. With a slight modification in fabrication procedure, three different types of MG configuration, namely, SG, ΩG, and gate-all-around (GAA), were implemented in the fabricated devices.

As compared with ΩG and SG devices, the improvements in device characteristics with GAA devices is achieved, owing to the enhanced gate controllability over NW channel which results in a higher ON-current, suppressed short channel effects, and steeper sub-threshold swing (SS) for NWs, as verified in our experimental results. These excellent characteristics can retain even with shrunk channel length.

For SONOS characterization, the GAA split not only exhibits the best device characteristics as mentioned above, but also the best performance in P/E characteristics. This is attributed to the increase in strength of the electric field at the NW-tunnel oxide interface as well as the reduced electric field strength in the blocking oxide, as evidenced from the simulation results presented in last chapter. Hence it possesses the most prominent performance among the different types of device characterized in this work. The retention measurements show that the memory window can be larger than 0.5 V after 10 years at

room temperature. For endurance test, the devices can sustain P/E cycles for more than 10^4 times while maintaining acceptable memory window in retention test. By optimizing the ONO composition and thickness, further improvement is possible.

4-2 Future Work

The development and characterization of MG poly-Si NW SONOS have been studied in this thesis. For the purpose of further improving device performance, some valuable studies for the future work are suggested as follows:

For GAA NW devices the NW's cross-sectional shape plays a key role. The round-shape is most preferred, while other shapes may suffer from the existence of sharp corners and/or irregular shape which may result in non-uniform field distribution [43]. In this work we've found the formed NWs have a shape close to circle, but details about the results are still not clear. Further effort is needed to understand the factors that determine the NW shape.

Next, the O/N/O stack composition and thickness should be optimized to further reduce the operation voltage and/or to increase the P/E speed. In addition to improving the quality of TEOS oxide, replacement with another high-*k* dielectric is also viable. Regarding the nitride storage layer, nitride profile engineering in the layer is also a viable approach.

In this study, we have demonstrated many important and interesting results about NW SONOS characteristics. The experimental results show decent electrical characteristics and acceptable memory window with the GAA structure. Nevertheless, it is a pity that we don't have a complete model to explain the characteristics of the NW SONOS devices. Therefore, performing more simulation work to justify our findings is another urgent work in the future.

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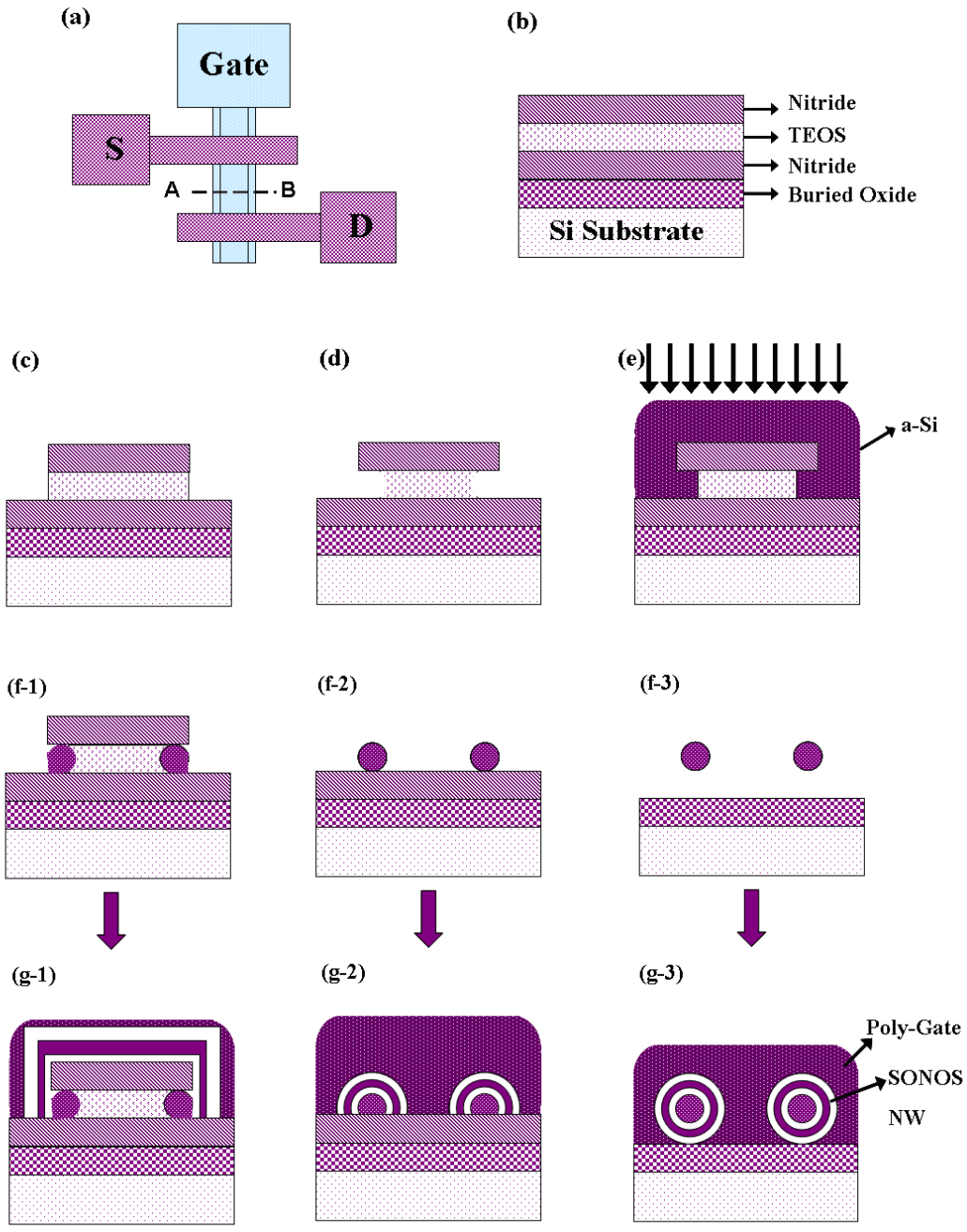
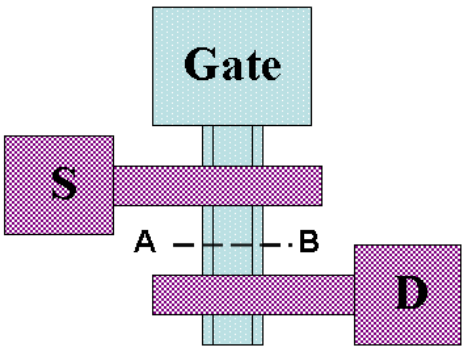


Fig. 2-1 (a)Top-view of the NW device, and cross-sectional view (along Line AB in (a)) of NW SONOS-devices at different steps: (b) Bottom Nitride, TEOS and Nitride formed on Si-substrate capped with a buried oxide. (c) Nitride and TEOS patterned by anisotropic reactive plasma etching. (d) Recessed cavities formed by DHF wet etching. (e) a-Si deposition and annealing, and S/D implant. (f-1) Si removal with anisotropic dry etching. (f-2) Nitride removal with hot H_3PO_4 and TEOS removed by DHF. (f-3) Bottom Nitride removal with hot H_3PO_4. (g-1 to g-3) ONO stacked layer and poly gate deposition.



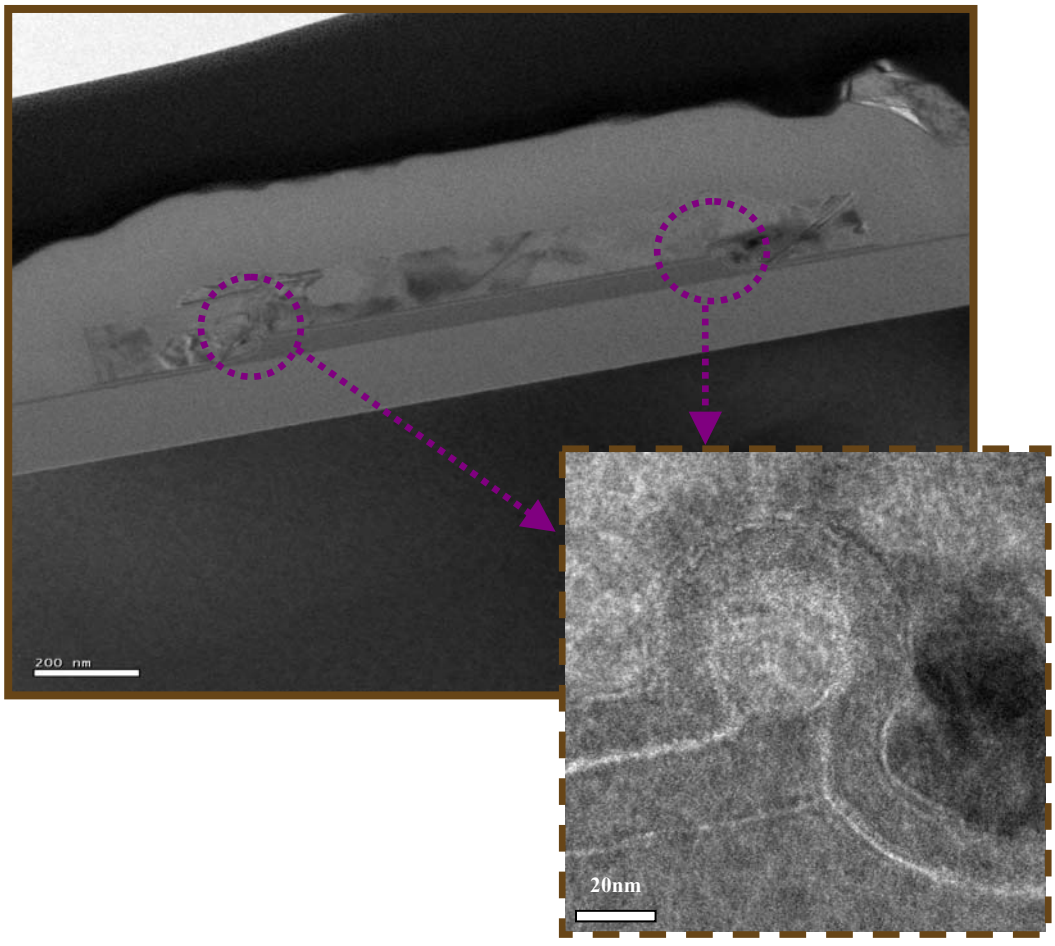
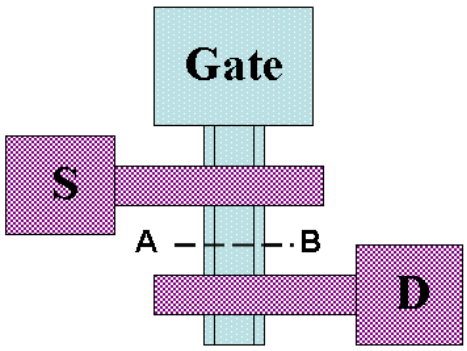


Fig. 2-2 Cross-sectional TEM picture of an NW SONOS-device with omega-gate along Line $\overline{AB}$ of the top layout.



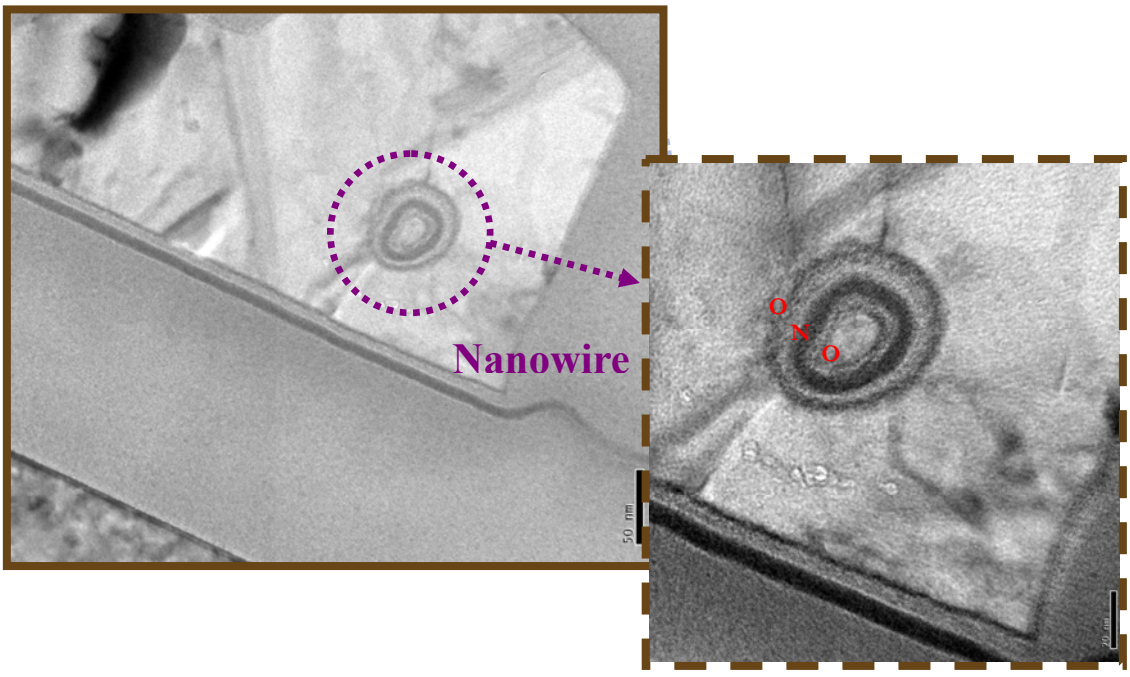


Fig. 2-3 Cross-sectional TEM picture of NW SONOS-device with gate-all-around (GAA) along Line $\overline{AB}$ of the top layout with channel length of 1μm.

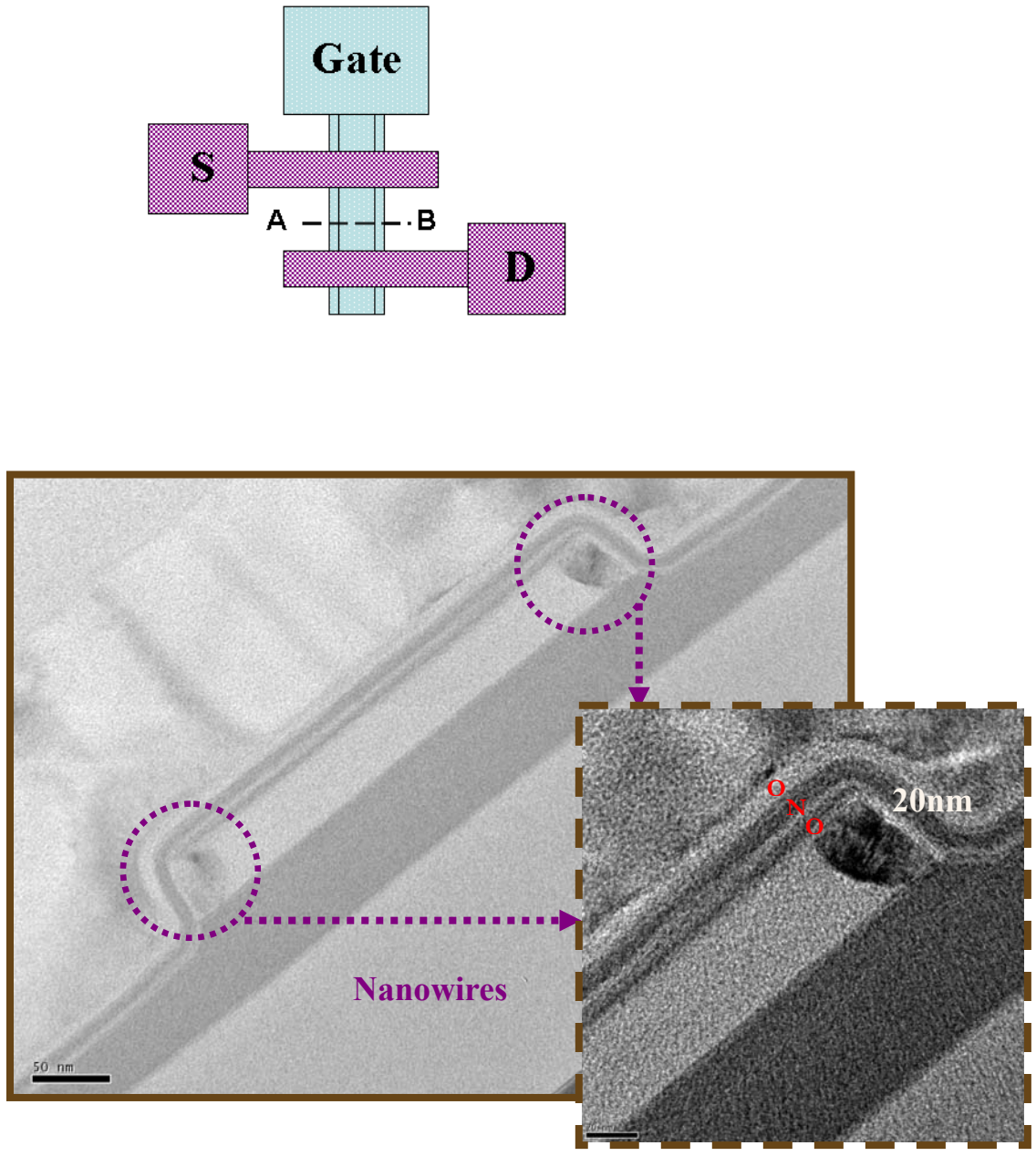


Fig. 2-4 Cross-sectional TEM picture of NW-SONOS device with side-gate (SG) along Line $\overline{AB}$ of the top layout.

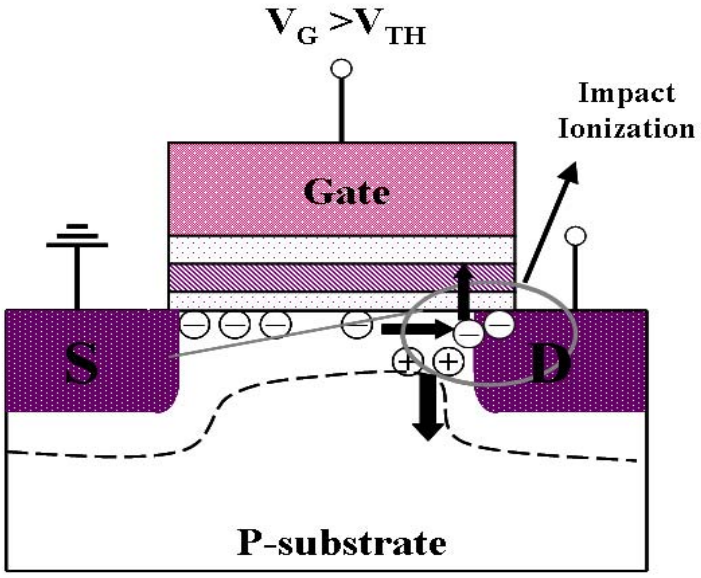


Fig. 2-5 Channel Hot Electron Injection (CHEI). Channel hot electrons (CHEs) are produced by the strong lateral electrical field in the pinch-off region, and lead to the generation of extra electron-hole pairs. Portions of hot electrons may inject into the gate dielectric and get trapped in the storage nitride layer.

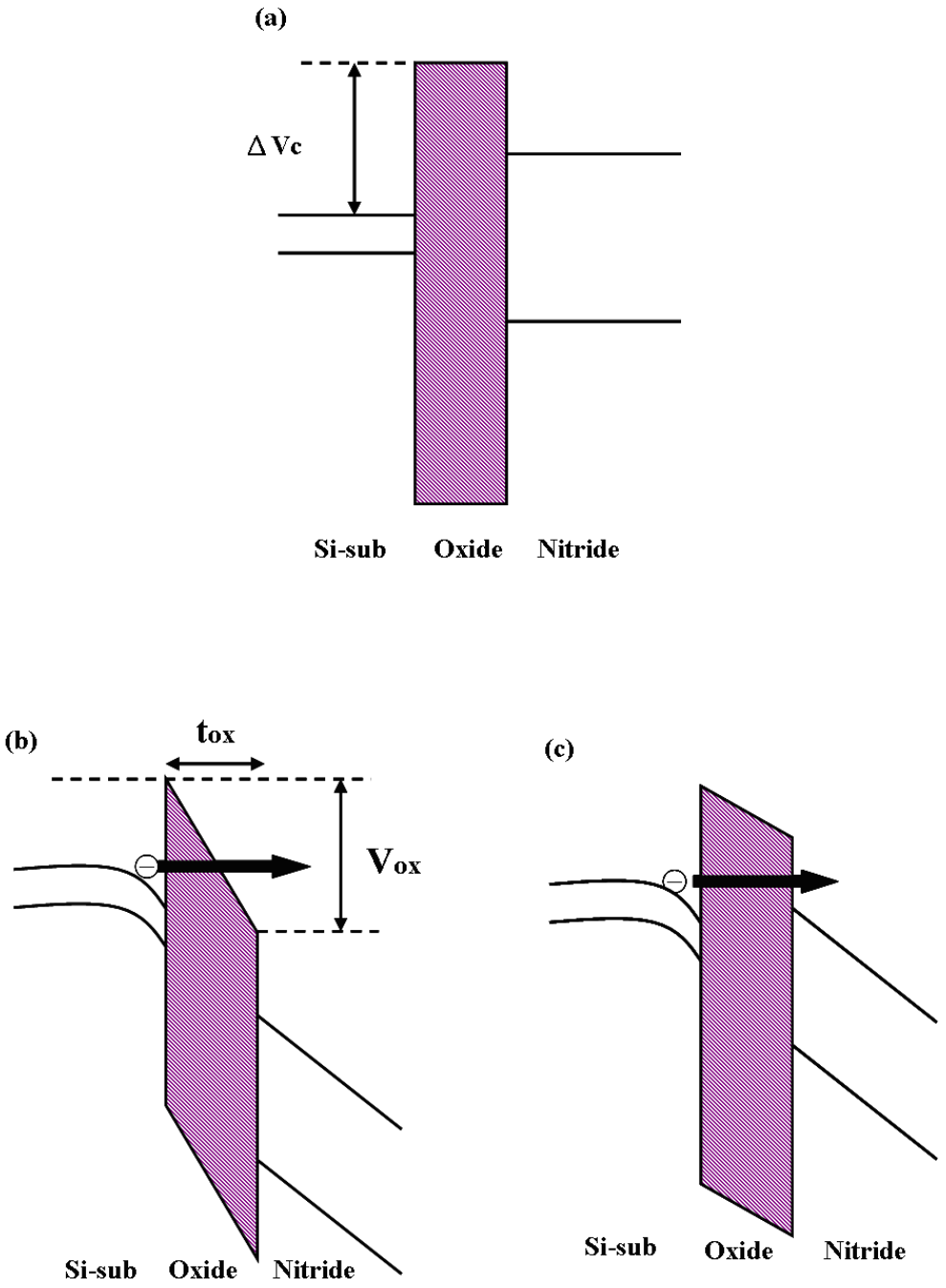


Fig. 2-6 (a)Energy band diagram of SONOS structure in flat-band condition. (b)Fowler-Nordheim tunneling occurs when Eox is higher than $\frac{\Delta V_C}{t_{OX}}$. (c)Direct tunneling occurs when oxide is thin enough and Eox is lower than $\frac{\Delta V_C}{t_{OX}}$.

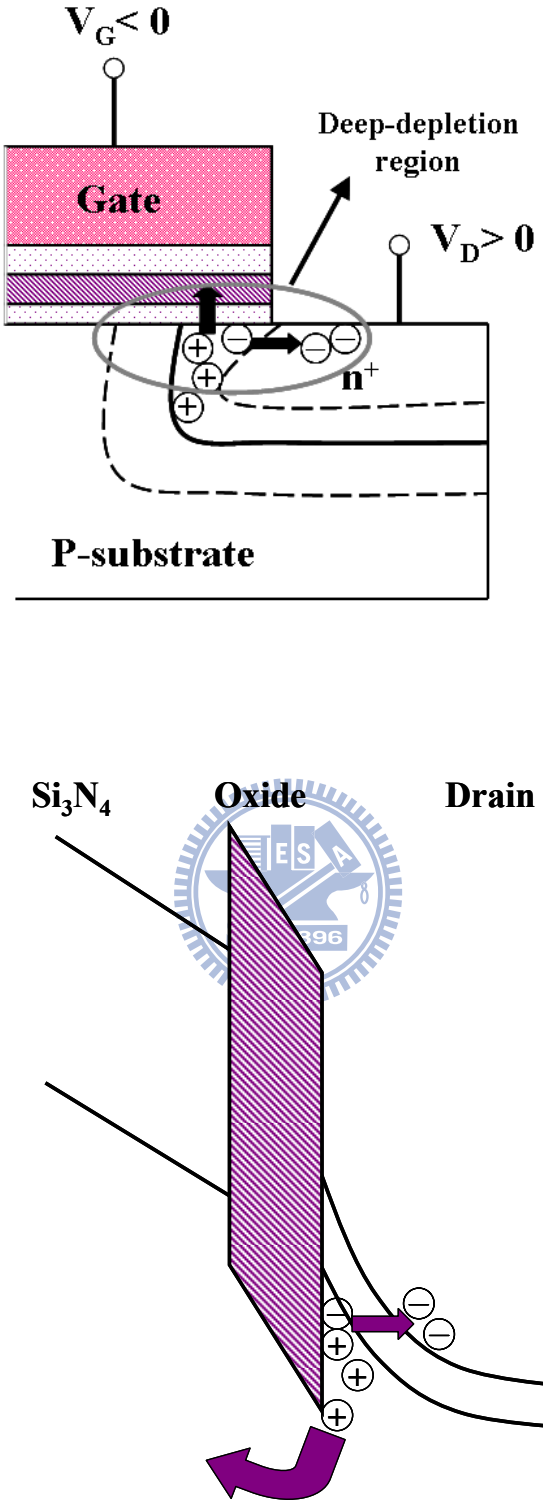


Fig. 2-7 Band-to-Band Tunneling (BTBT). (a) When biasing a negative voltage on gate electrode, a deep-depletion appears in n^+ drain region adjacent to the oxide interface. (b) Portions of the hot-holes generated in the GIDL may surmount the oxide barrier and inject into the storage nitride layer.

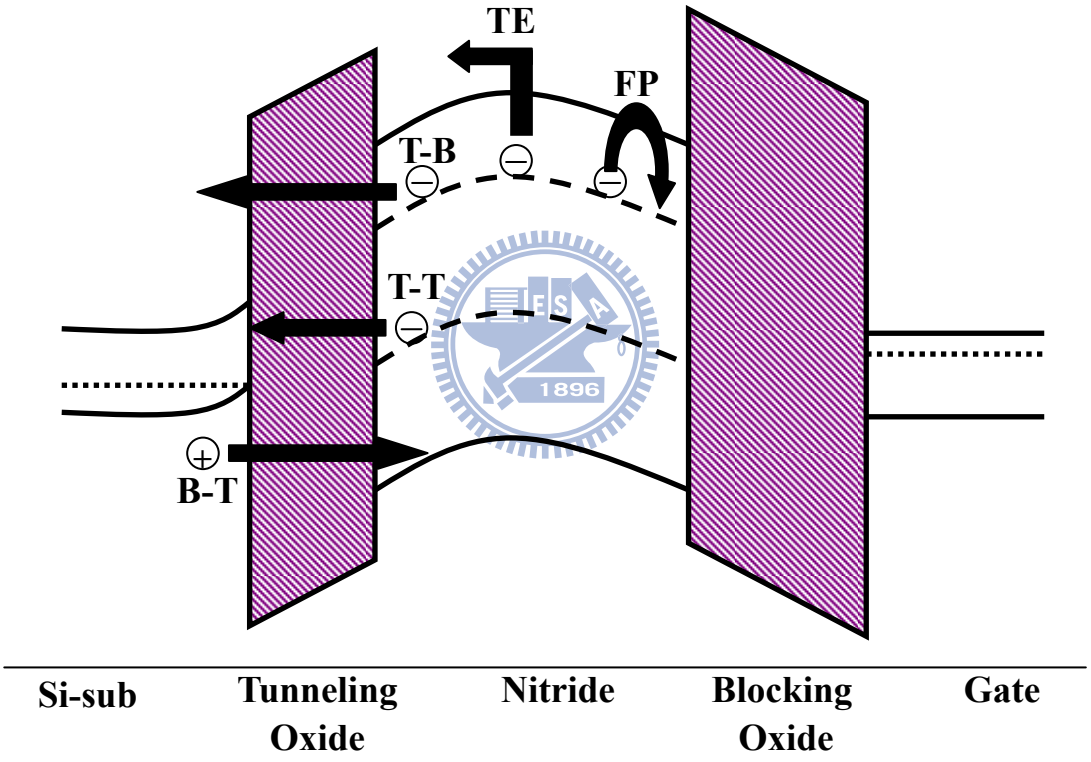


Fig. 2-8 Data lost paths in SONOS flash memory

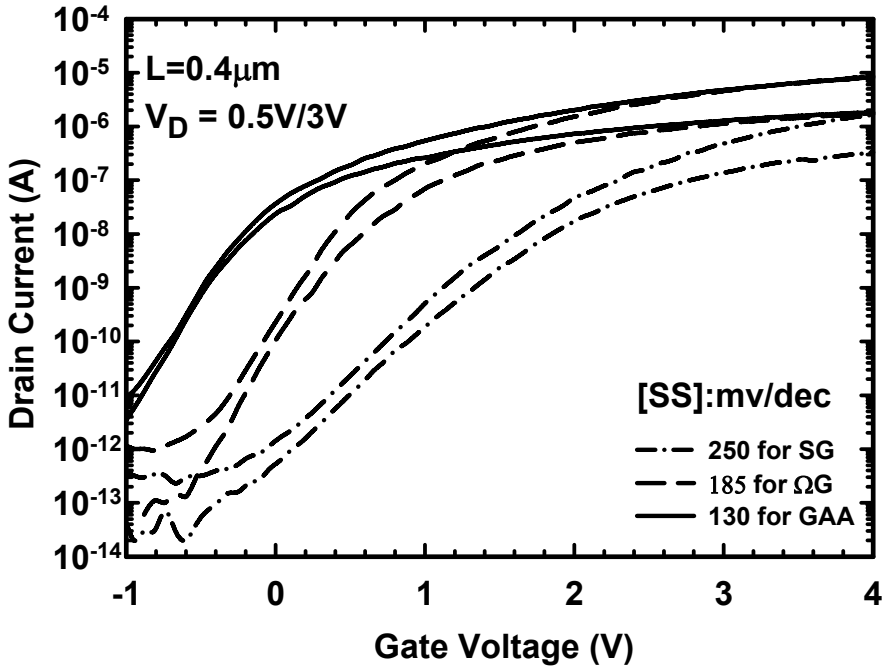


Fig. 3-1 Transfer characteristics of the three types of NW SONOS-devices with channel length of 0.4μm.

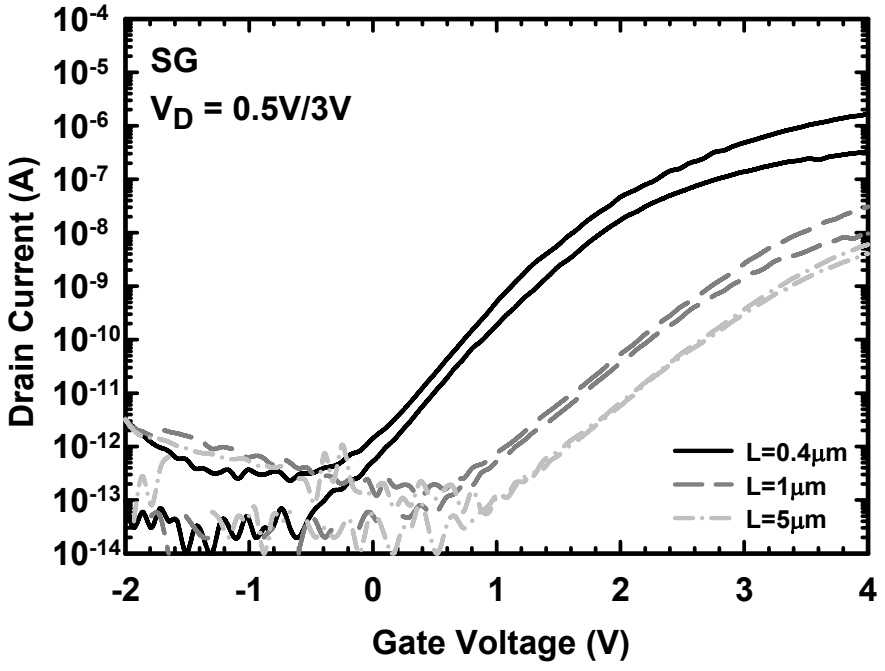


Fig. 3-2 Transfer characteristics of SG devices with different channel length.

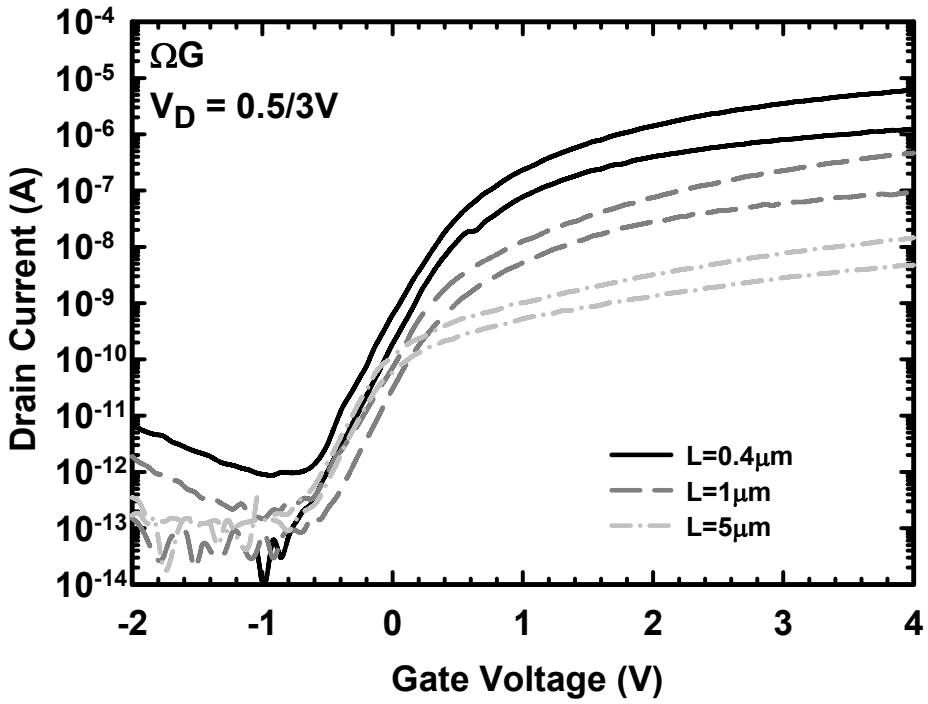


Fig. 3-3 Transfer characteristics of ΩG devices with different channel length.

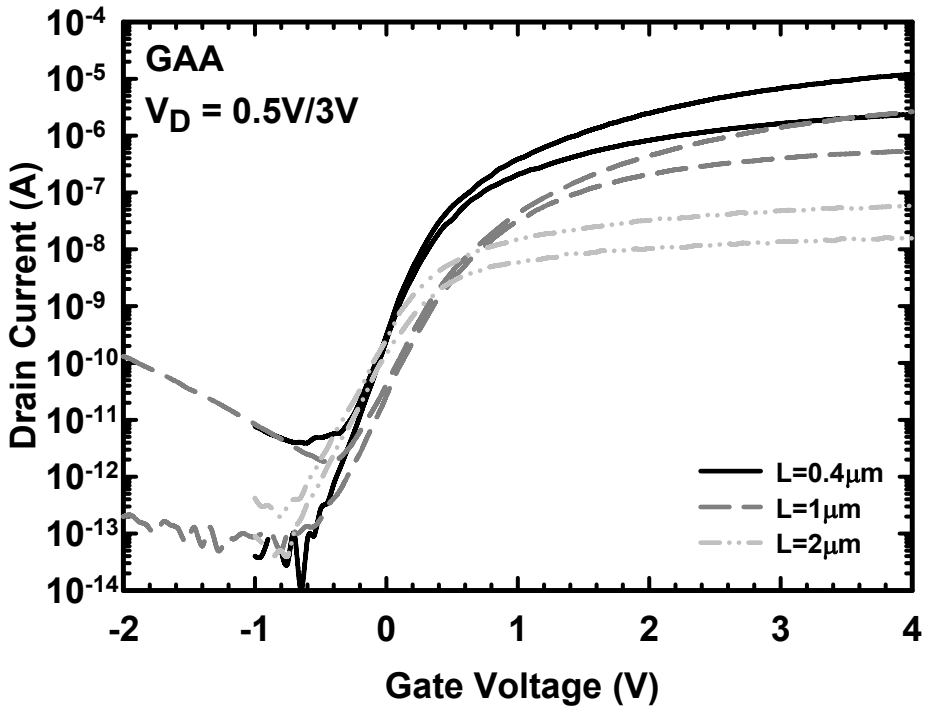


Fig. 3-4 Transfer characteristics of GAA devices with different channel length.

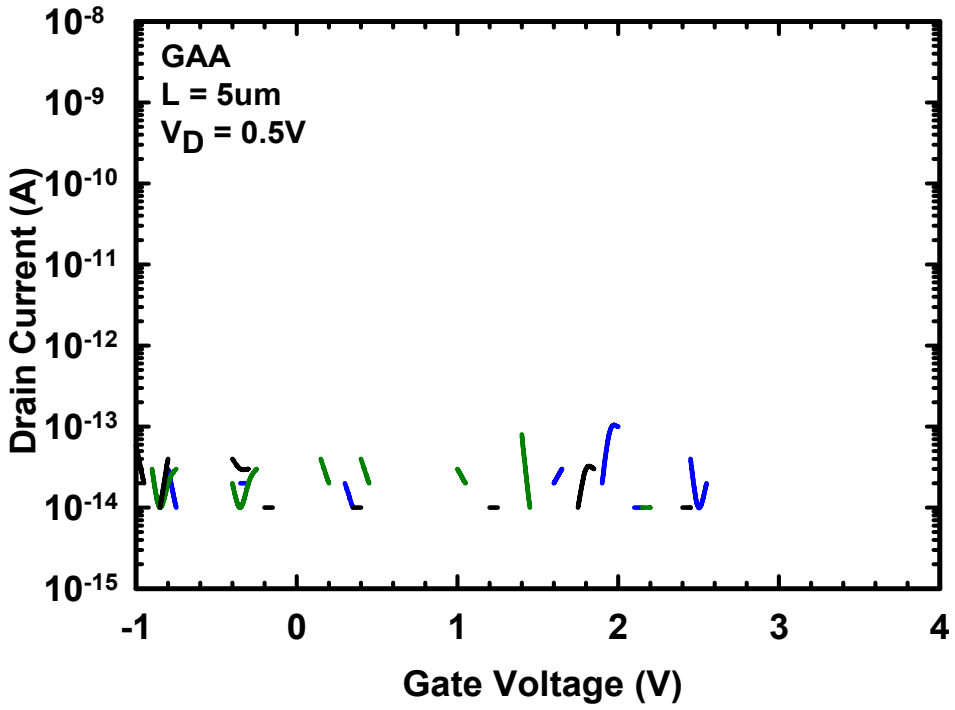


Fig. 3-5 Transfer characteristics of GAA devices with channel length = 5μm.

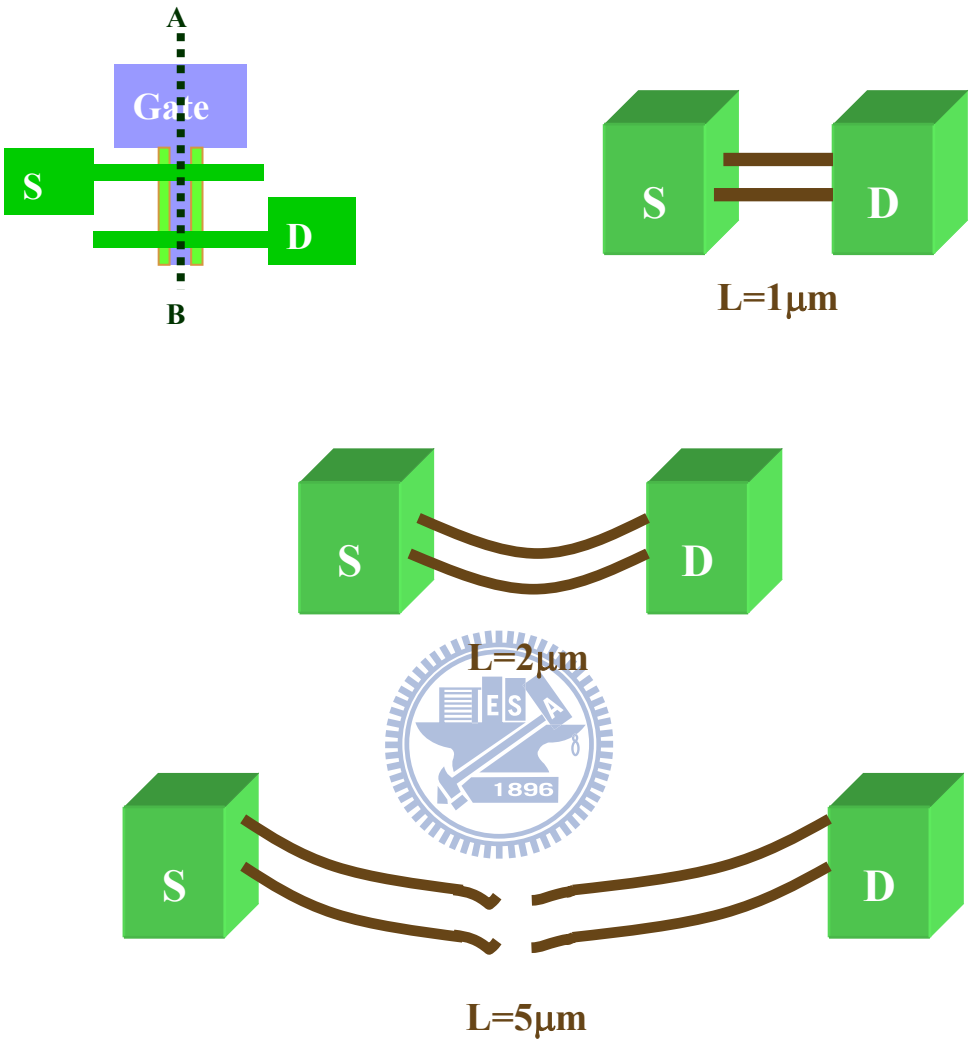


Fig. 3-6 A lateral view of GAA devices along line $\overline{AB}$ versus channel length of 1, 2, and 5μm.

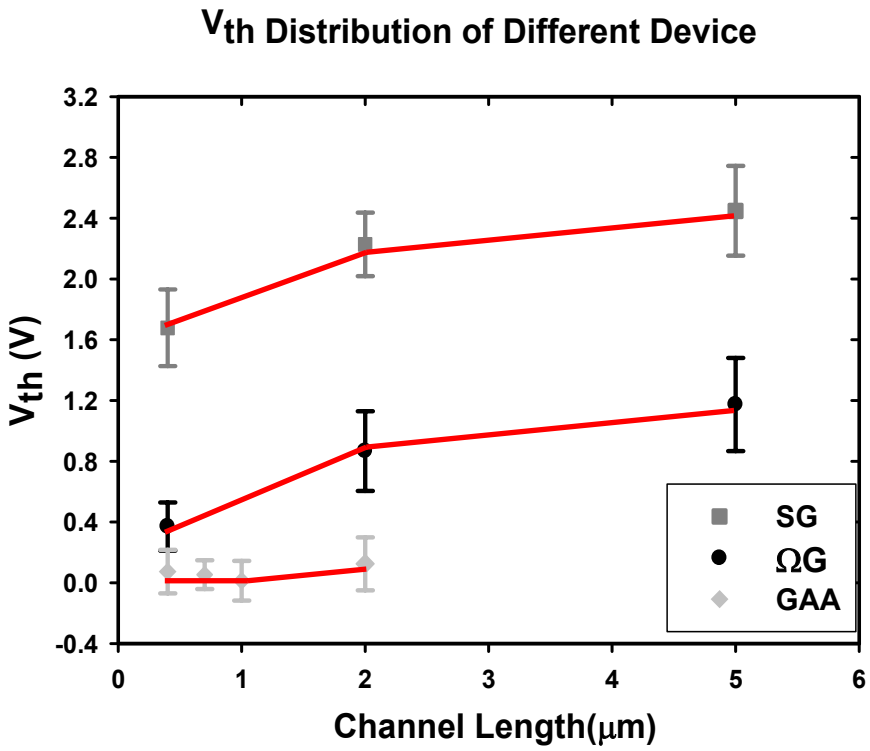


Fig. 3-7 Mean value of V_{TH} versus channel length for various structures.

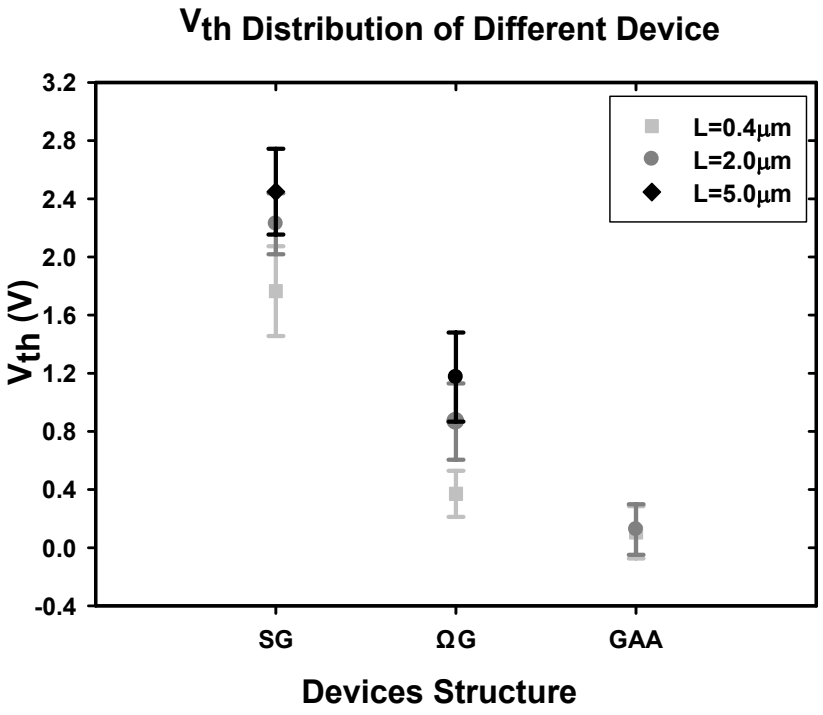


Fig. 3-8 Mean value of V_{TH} for various structures.

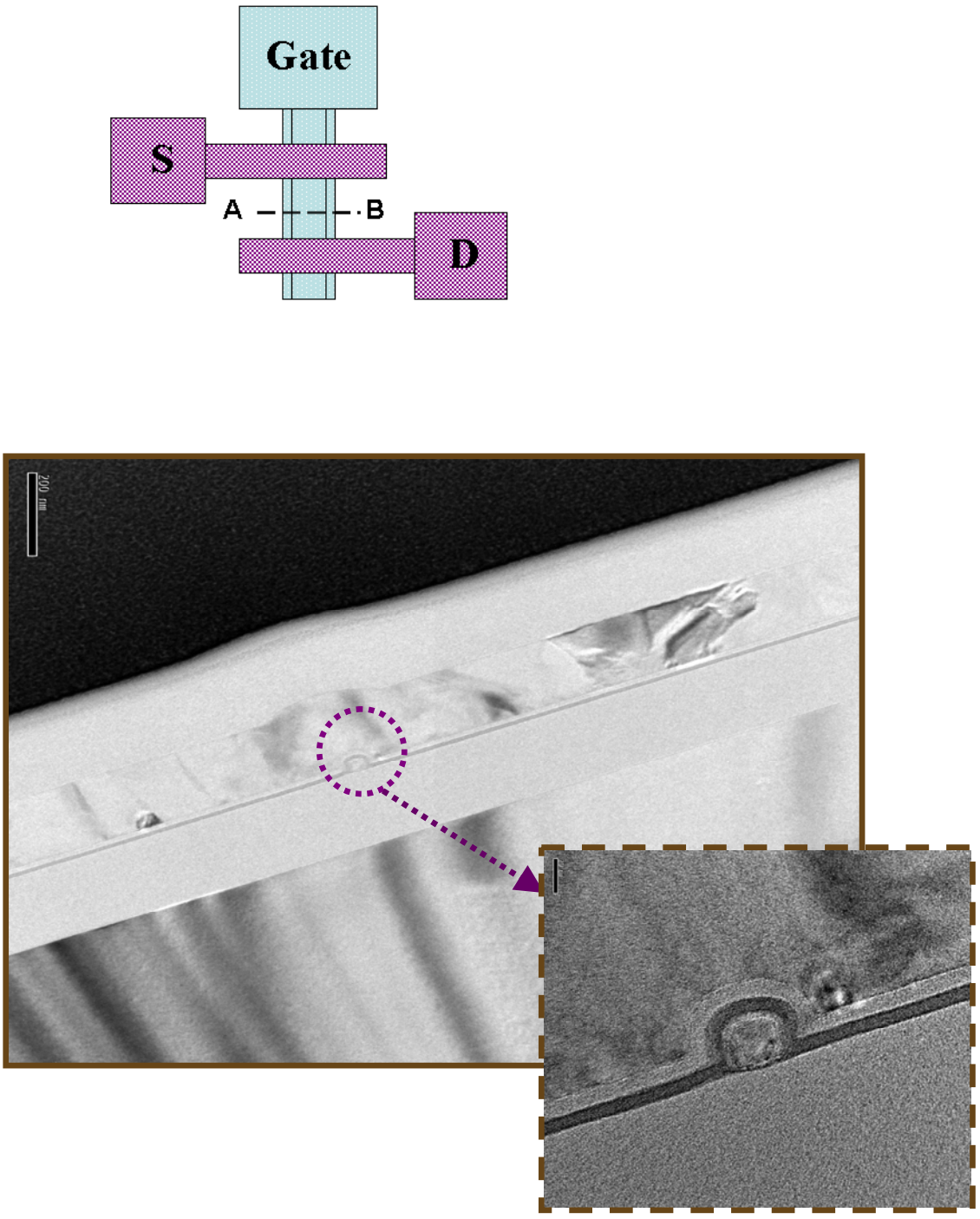


Fig. 3-9 Cross-sectional TEM image of a NW SONOS-device with channel length of 2μm along Line $\overline{AB}$ of the top layout..

(a)

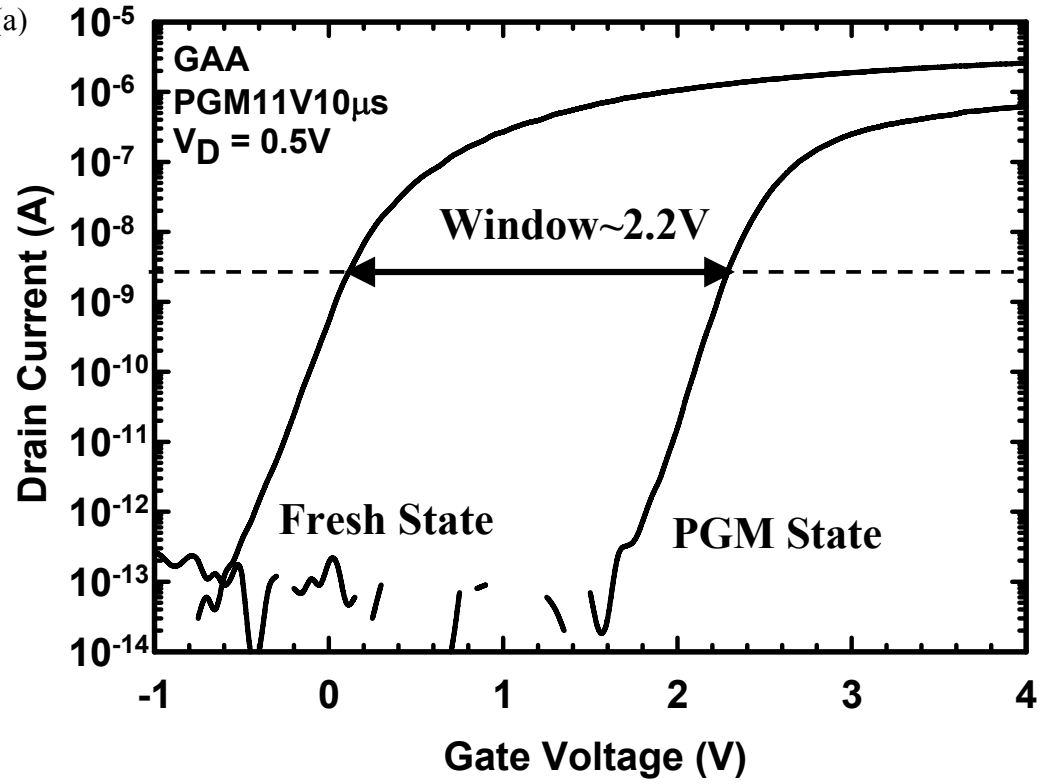


Fig. 3-10 (a)Transfer characteristics of a GAA SONOS-device before and after programming operation with gate voltage of 11V for 10μs. A V_{TH} shift of 2.2V is achieved.

(b)

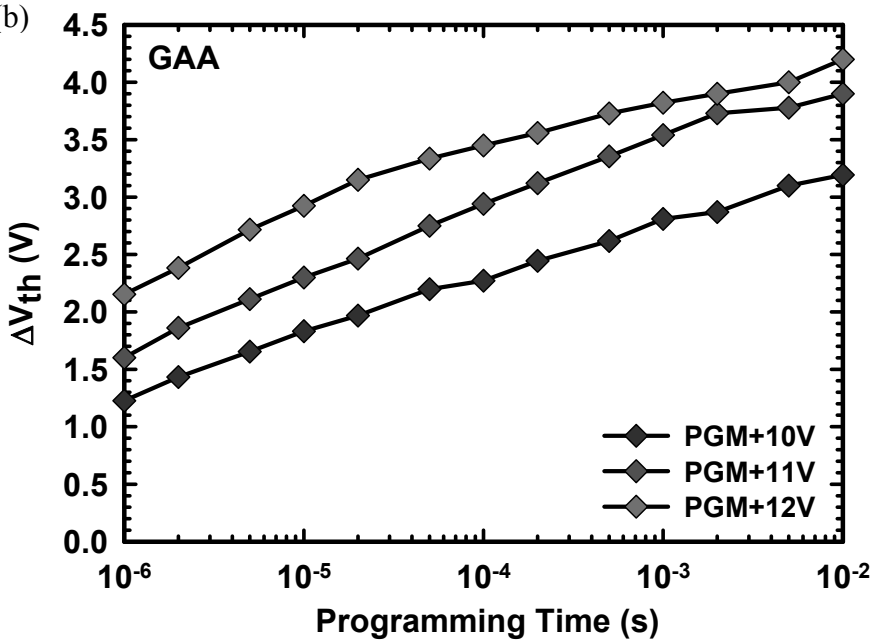


Fig. 3-10 (b)Programming characteristics of GAA SONOS-devices.

(c)

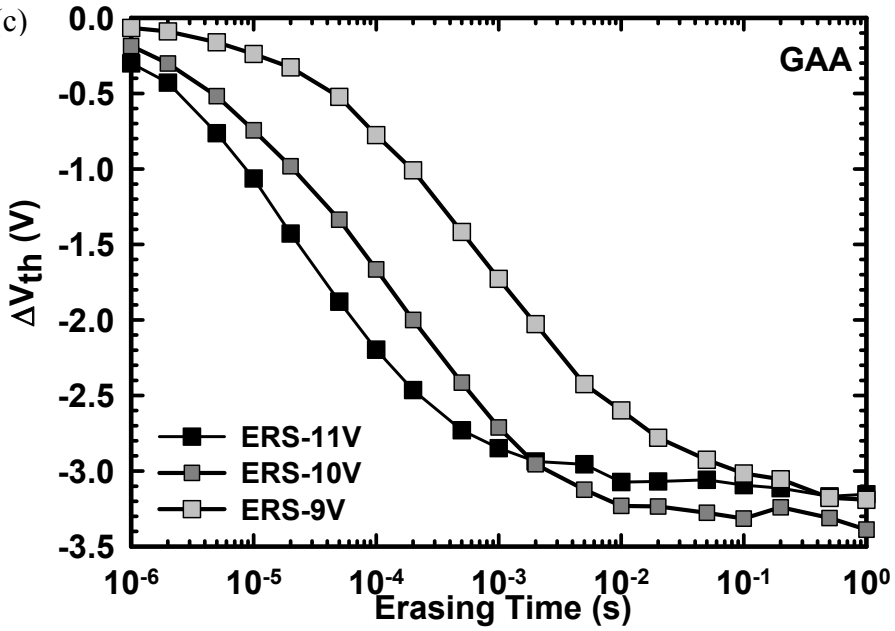


Fig. 3-10 (c)Erasing characteristics of GAA NW SONOS-devices.

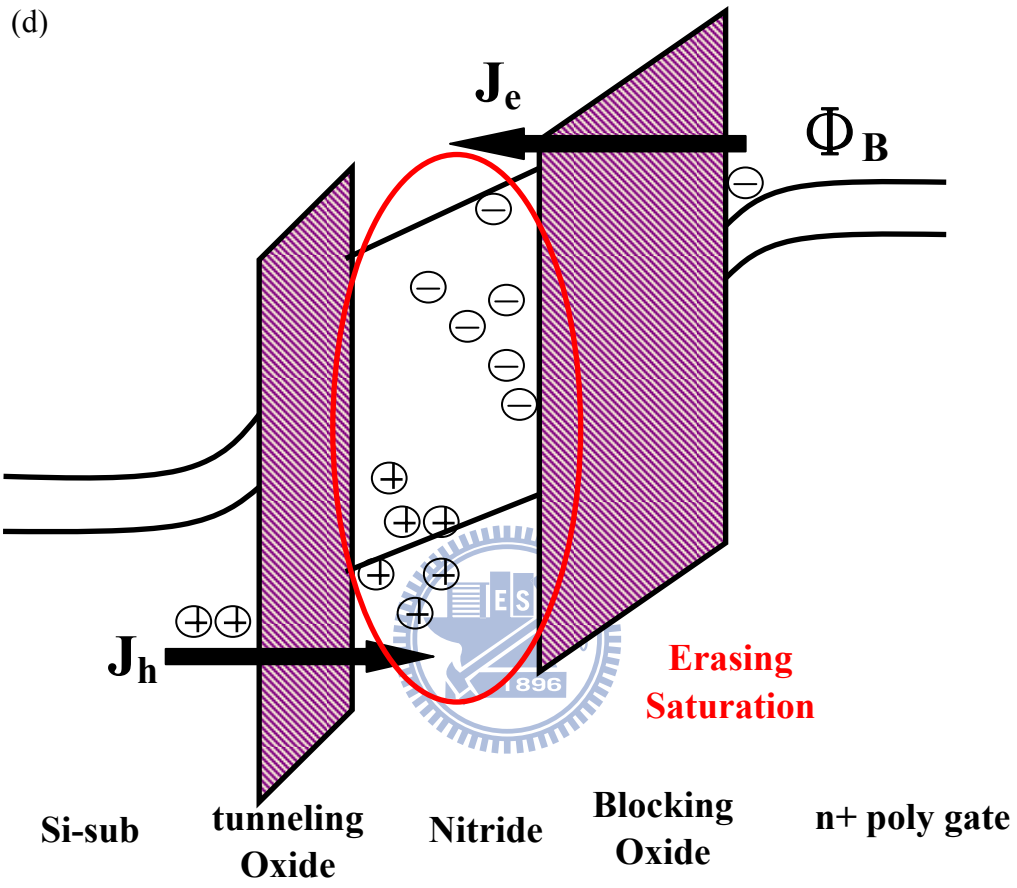


Fig. 3-10 (d)Energy band diagram of the SONOS-device with n^+ poly-Si gate under erasing operation.

(a)

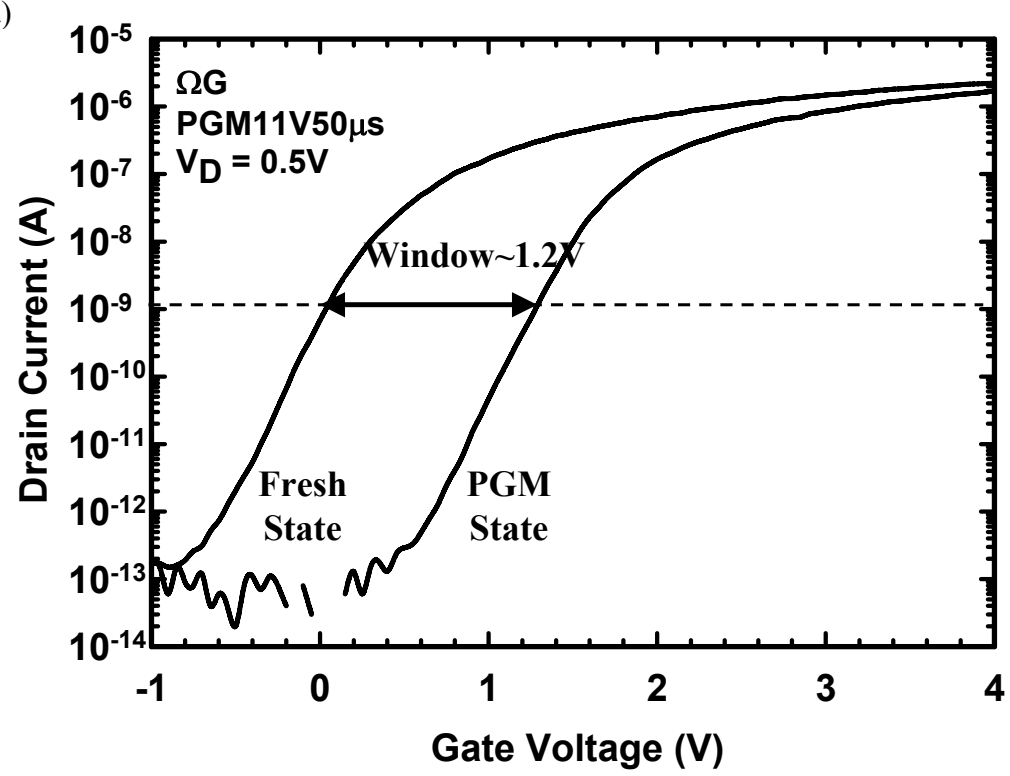


Fig. 3-11 (a)Transfer characteristics of an ΩG SONOS-device before and after programming operation with gate voltage of 11V for 50μs. A V_{TH} shift of 1.2V is achieved.

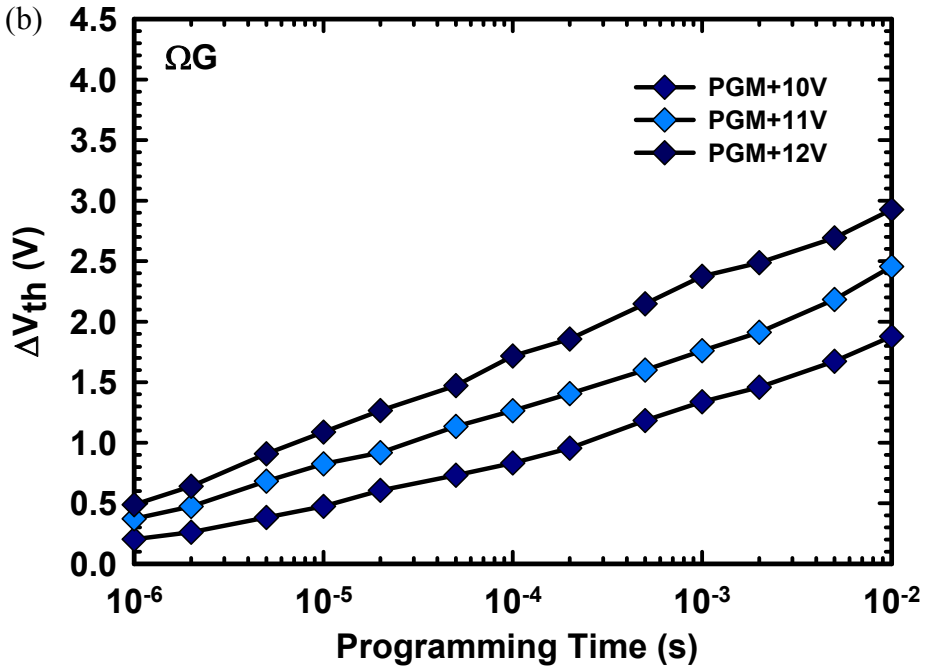


Fig. 3-11 (b)Programming characteristics of ΩG SONOS-devices.

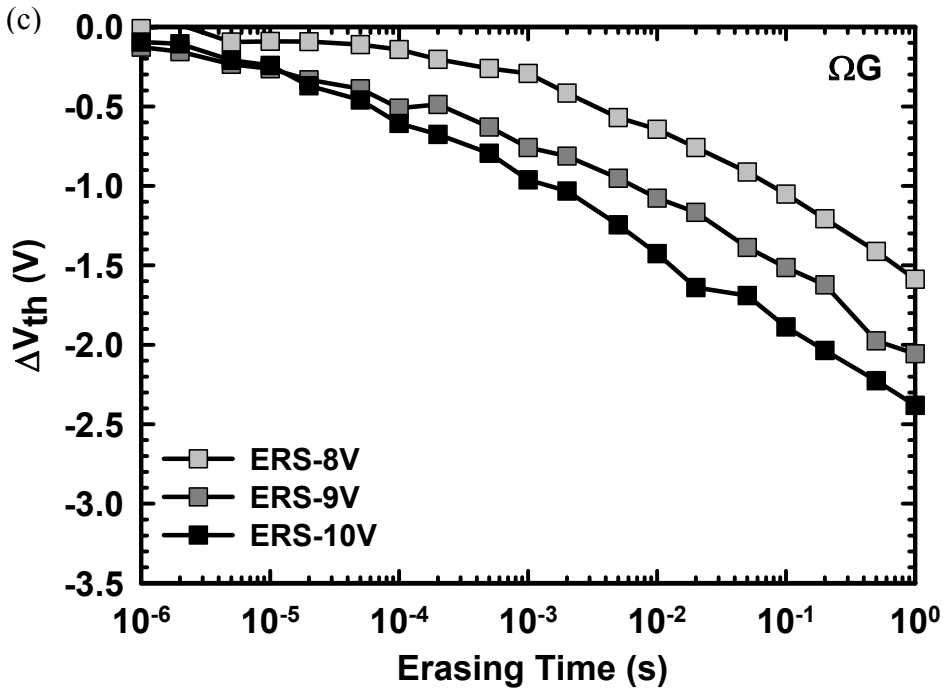


Fig. 3-11 (c)Erasing characteristics of ΩG NW SONOS-devices.

(a)

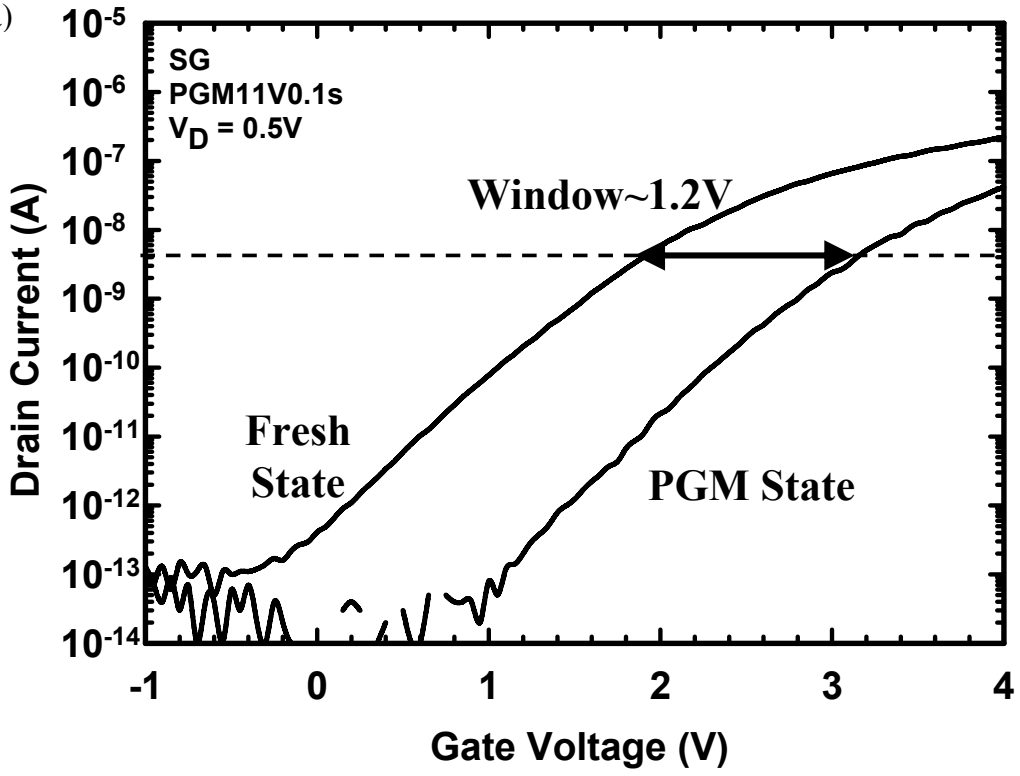


Fig. 3-12 (a)Transfer characteristics of an SG SONOS-device before and after programming operation with gate voltage of 11V for 0.1s. A V_{TH} shift of 1.2V is achieved.

(b)

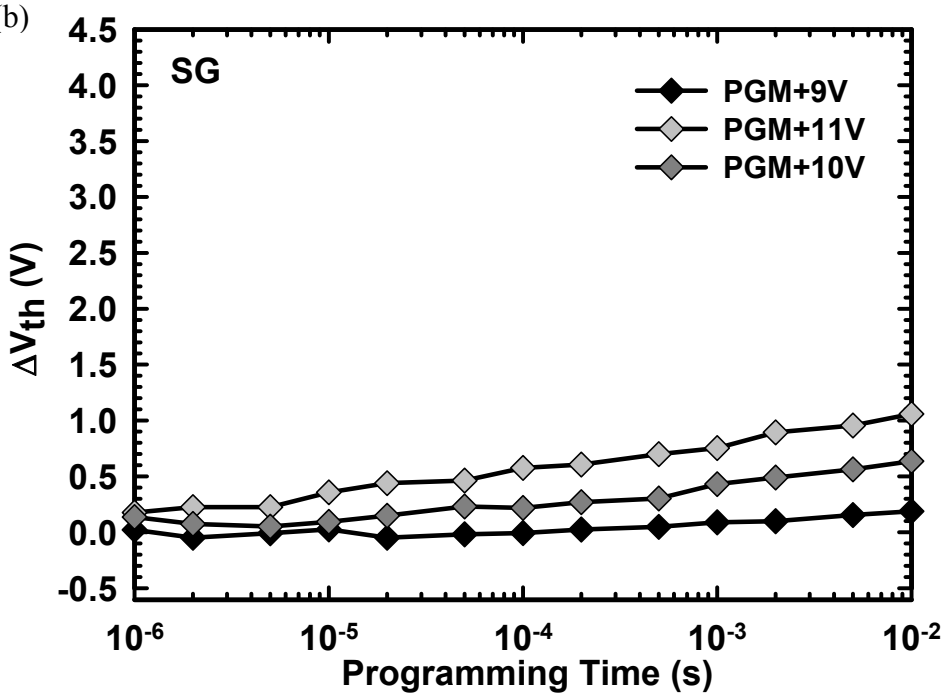


Fig. 3-12 (b)Programming characteristics of SG SONOS-devices.

(c)

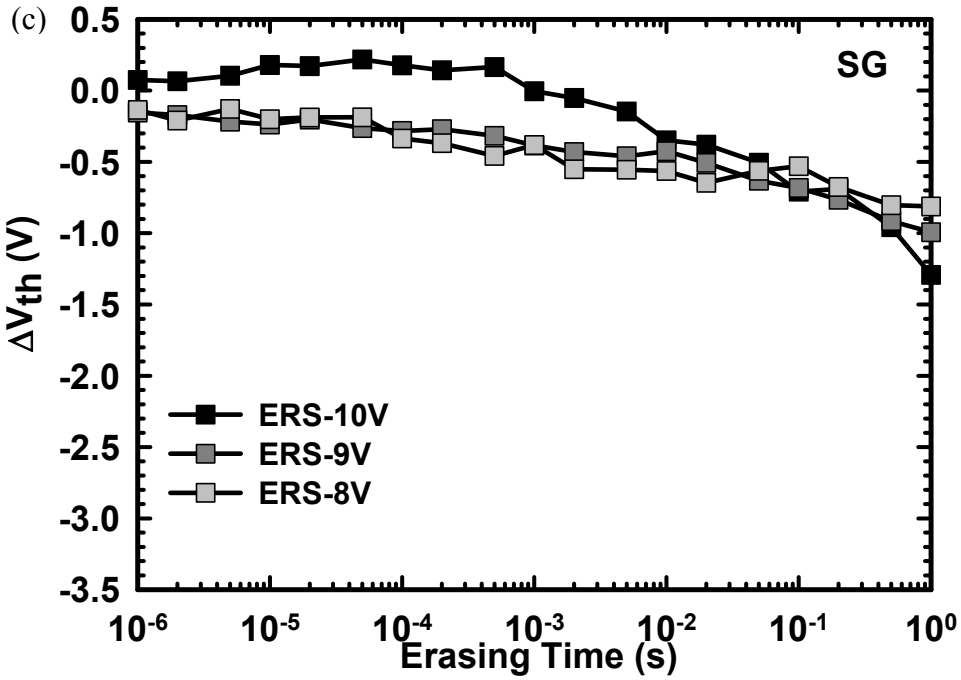


Fig. 3-12 (c)Erasing characteristics of SG NW SONOS-devices.

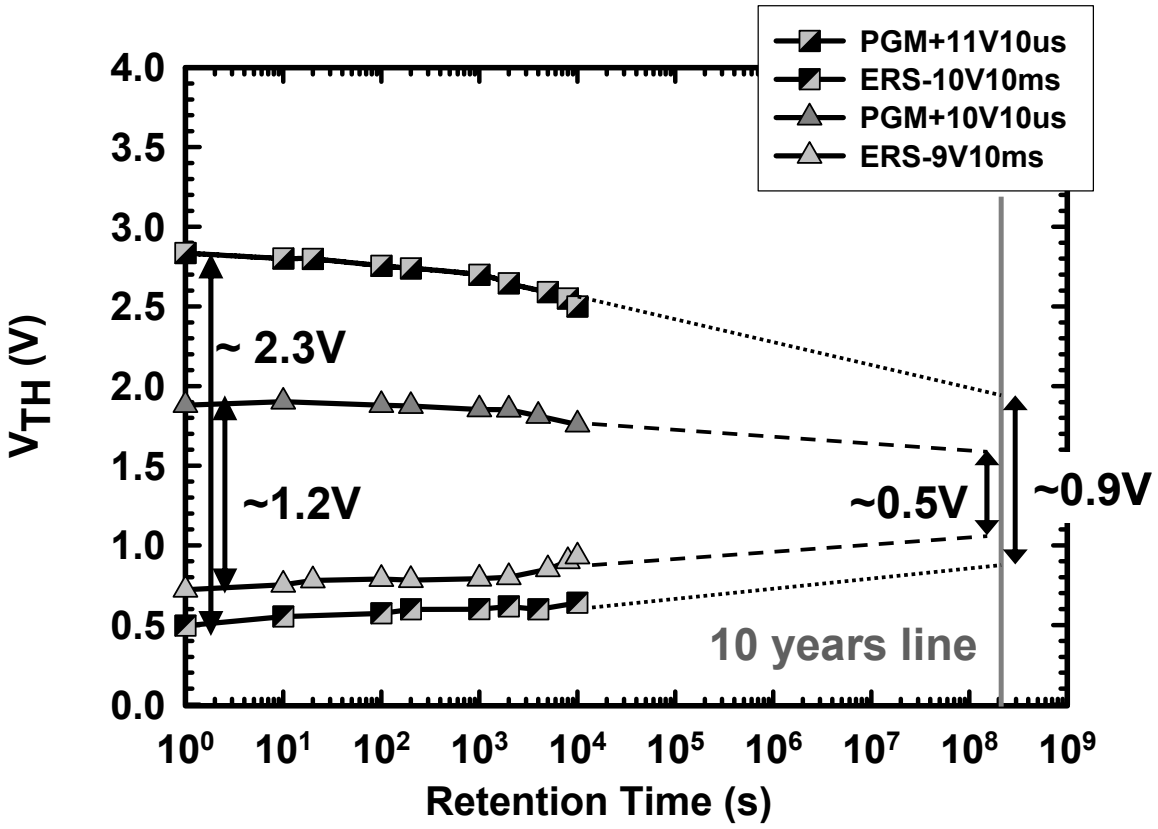


Fig. 3-13 Retention characteristics of GAA devices at room temperature.

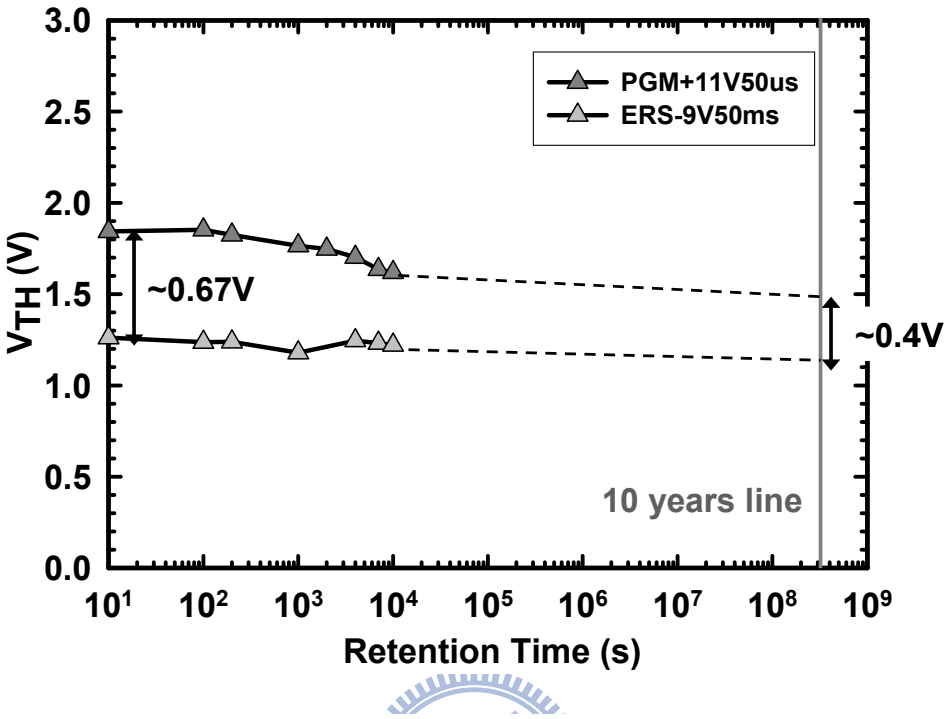


Fig. 3-14 Retention characteristics of ΩG devices at room temperature.

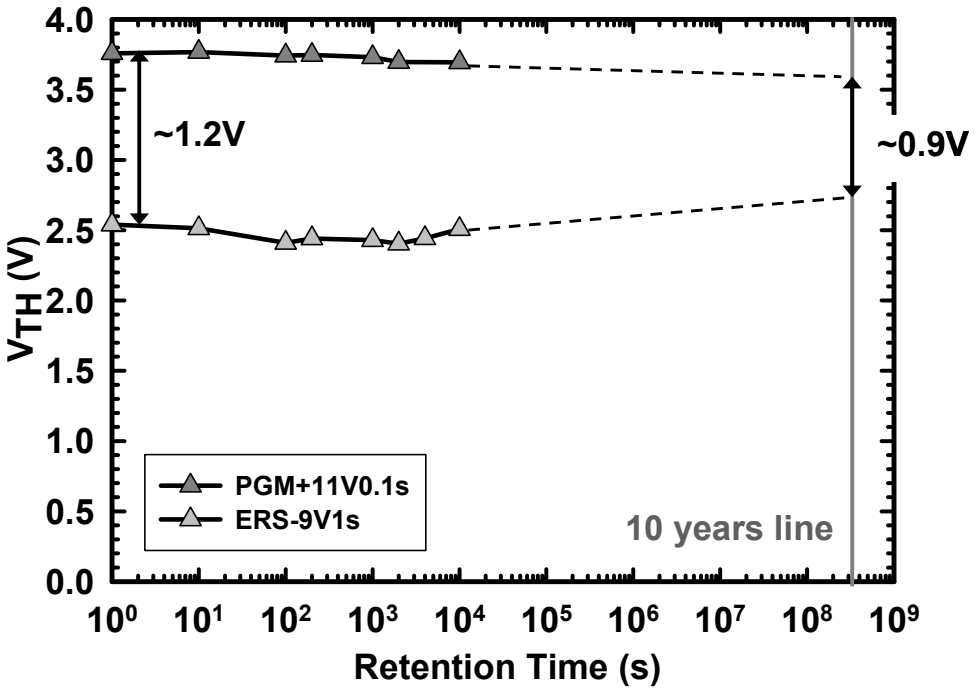


Fig. 3-15 Retention characteristics of SG devices at room temperature.

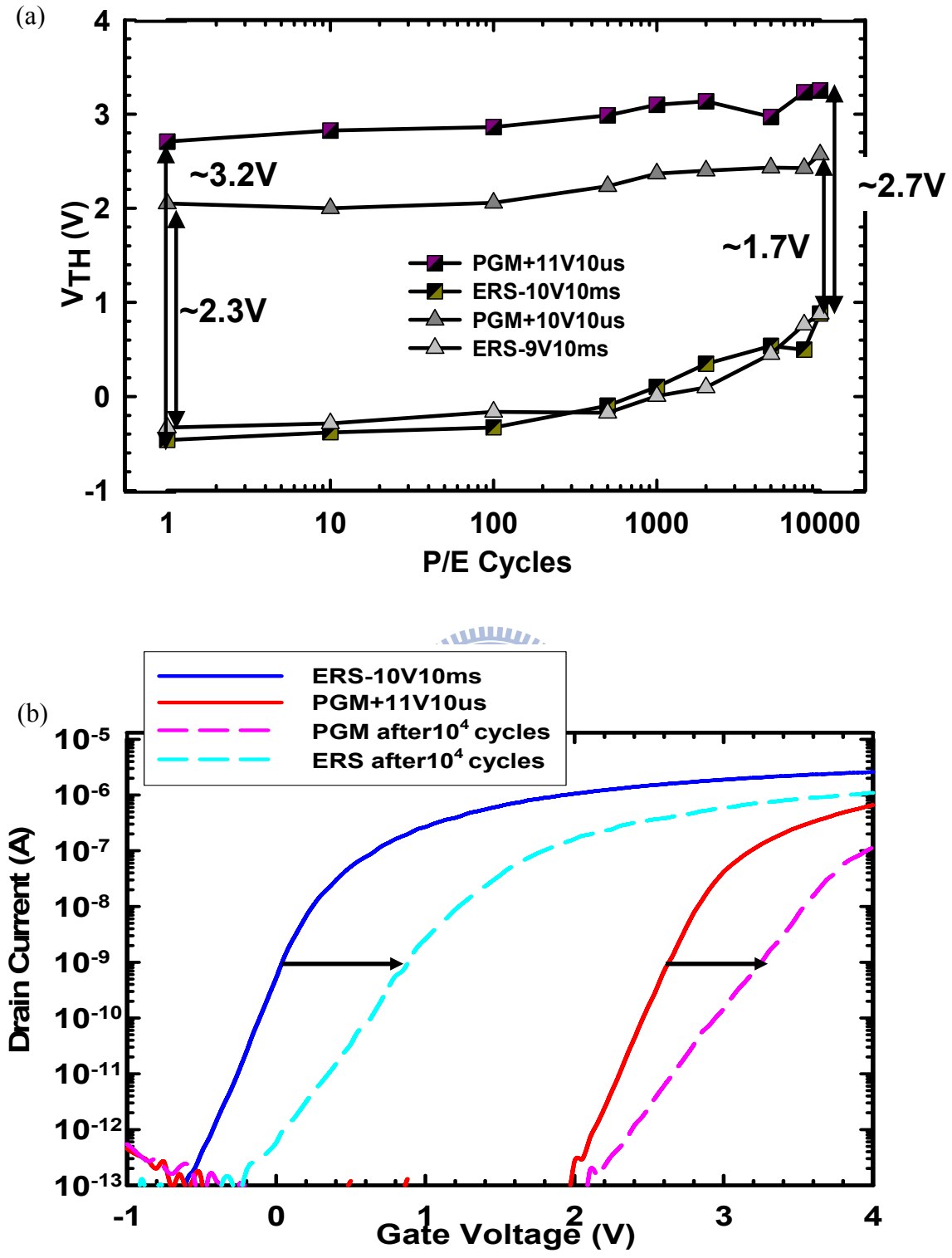


Fig. 3-16 (a)Endurance characteristics of GAA SONOS-devices. (b)I_D-V_G characteristics before and after P/E cycles with different P/E specifications.

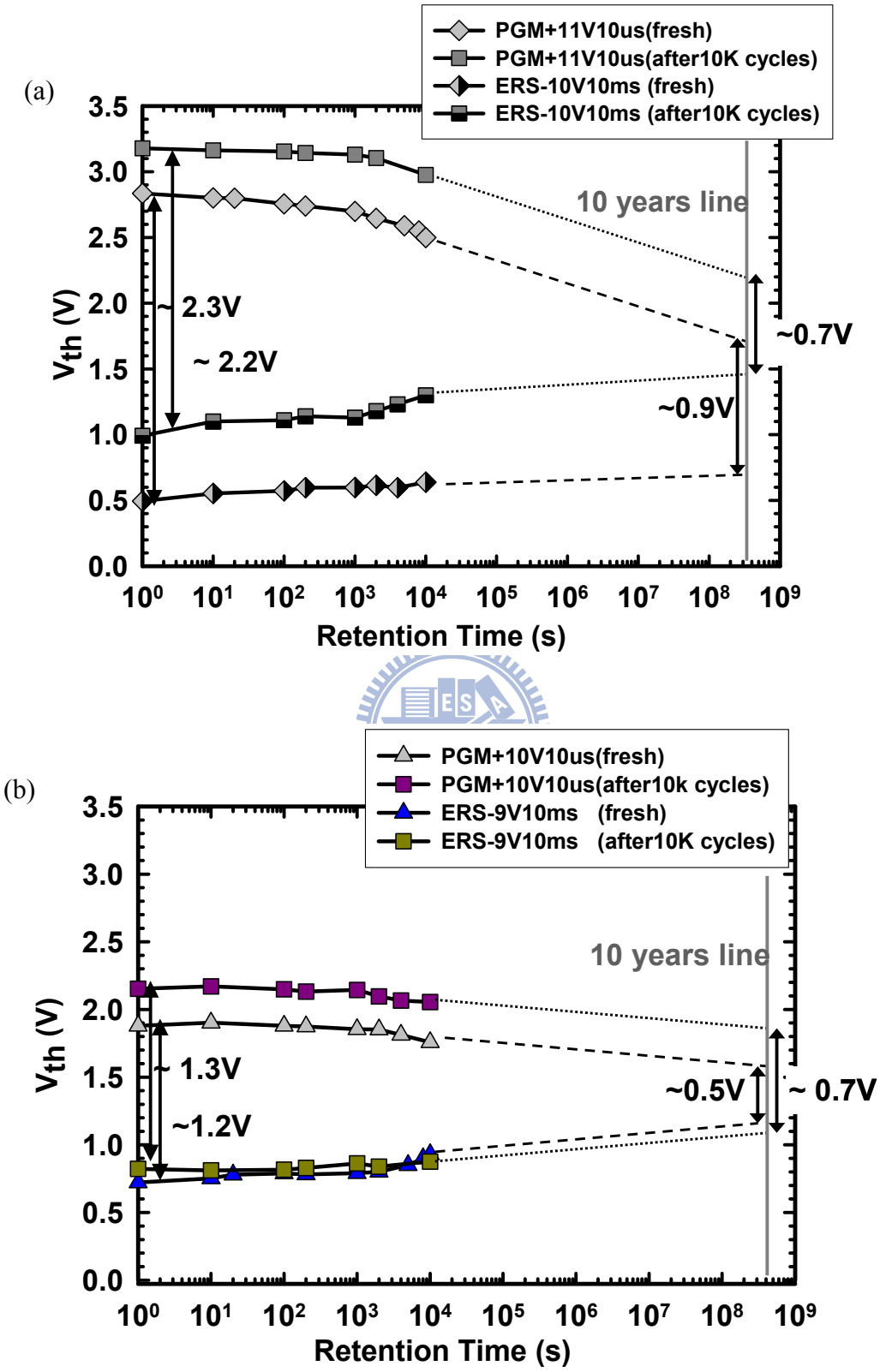


Fig. 3-17 Retention characteristics of GAA SONOS-devices before and after stressing with P/E specification of (a) 11 V:10 s/-10 V:10ms and (b)10V:10s/-9V:10ms.

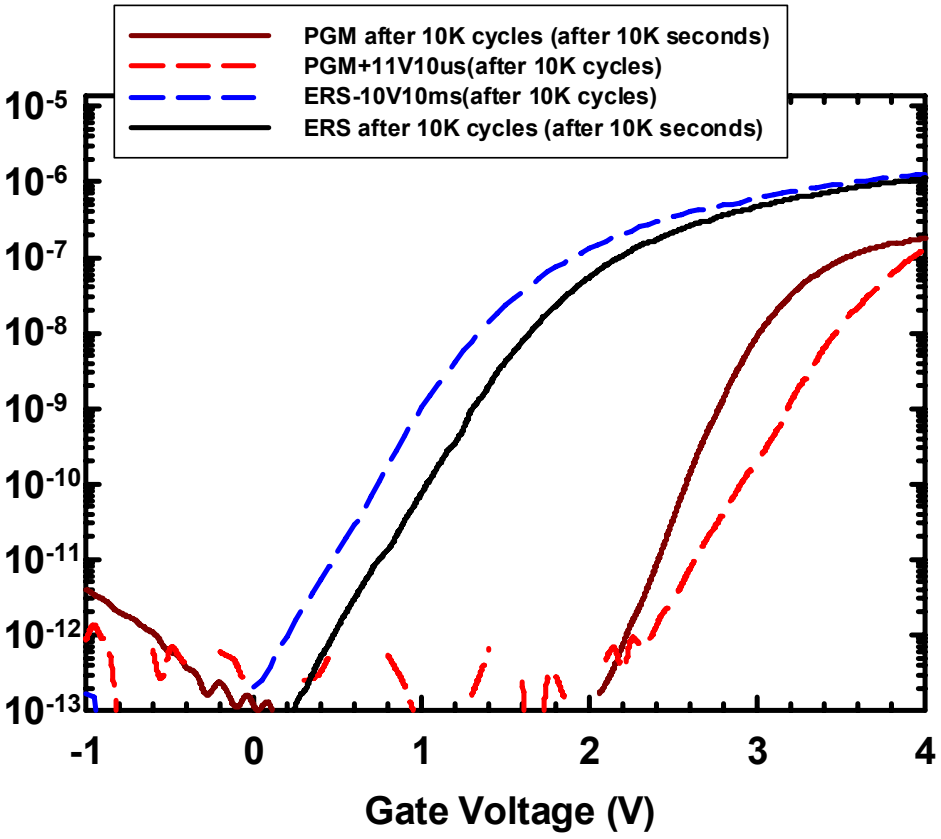


Fig. 3-18 I_D-V_G characteristics immediately after 10K P/E cycles and then after 10^4 seconds retention test with P/E specifications of 11 V:10 μ s/-10V:10ms.

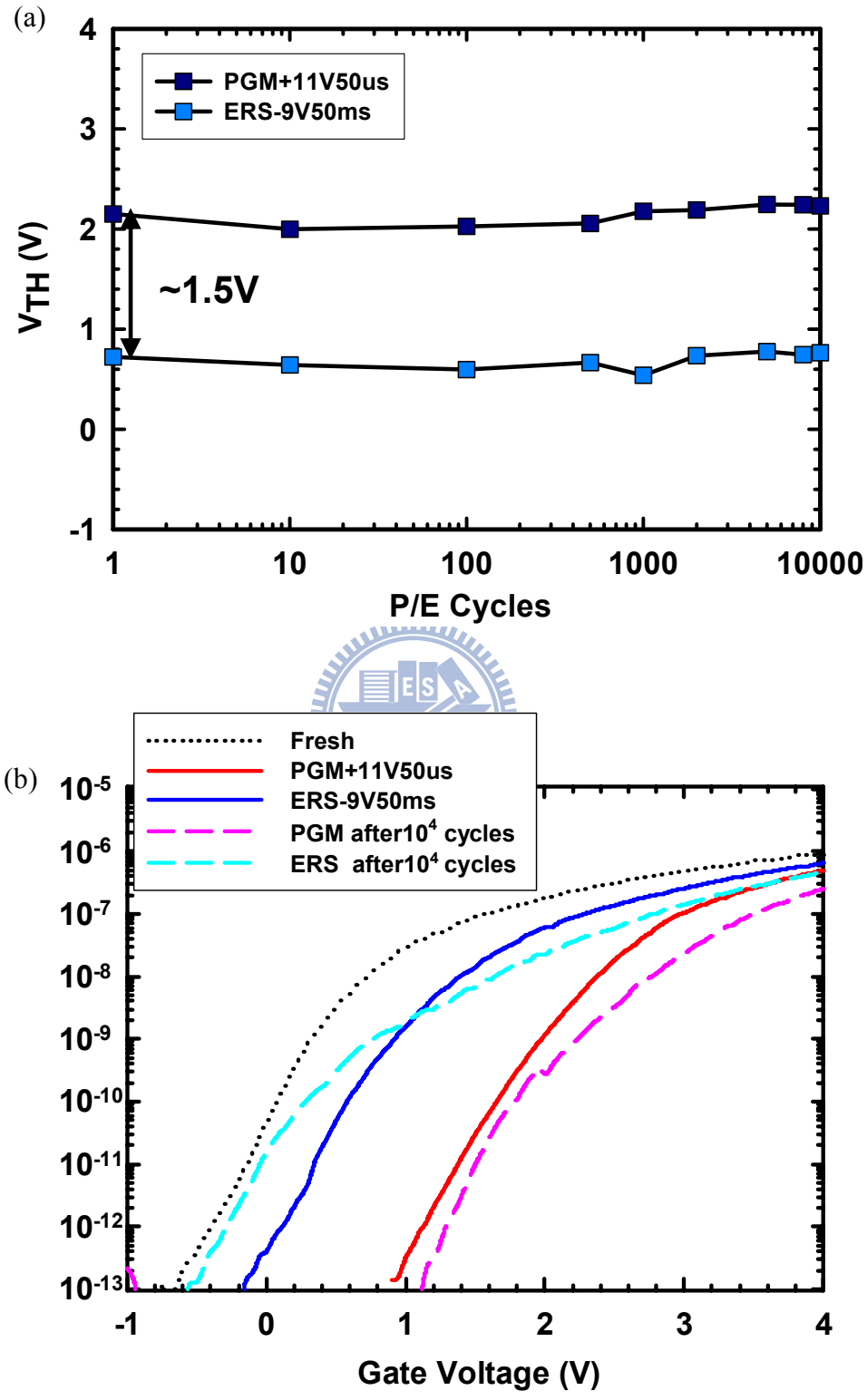
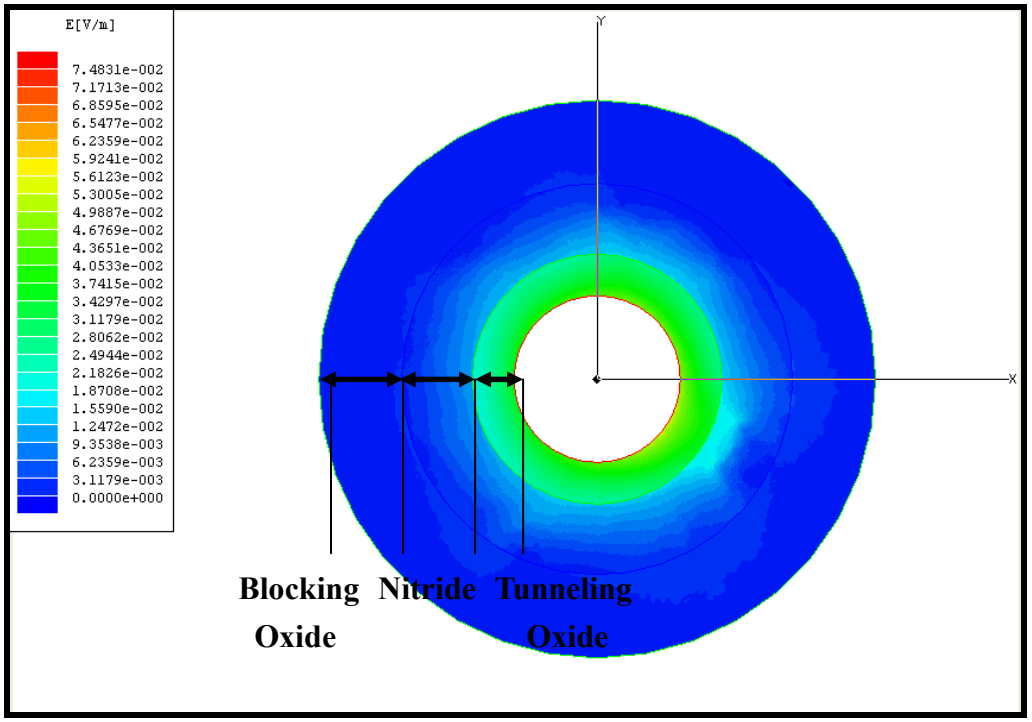


Fig. 3-19 (a)Endurance characteristics of ΩG SONOS-devices. (b)I_D-V_G characteristics before and after P/E cycles with P/E specifications of 11V:50 μs/-9V:50ms.

(a)



(b)

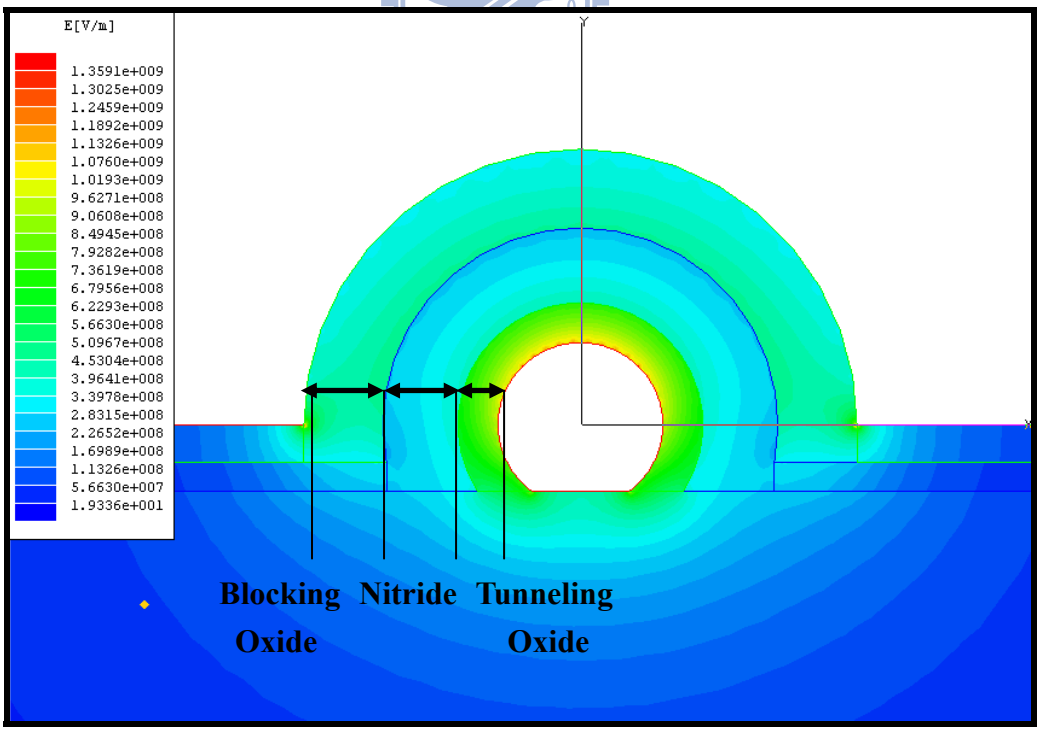


Fig. 3-20 MAXWELL SV simulation of electric field for (a) GAA SONOS-devices (b) ΩG SONOS-devices.

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論文題目:新式多晶矽奈米線 SONOS 元件製作與特性分析

Fabrication and Characterization of Novel Poly-Si Nanowire SONOS Devices