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以奈米壓印技術製作大面積次微米孔洞陣列

Development of a nano imprint process for fabricating submicron dot array in large area

研究生: 周智超

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指導教授：崔秉鉞　博士　　　　Advisor： Dr. Bing-Yue Tsui

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摘　　要

薄膜太陽能電池是值得期待的下世代太陽能電池之一，理因其低廉的價格和多方面的基板應用。多年研究下已研發出許多方法可以製作薄膜太陽能電池，empty-space in silicon (ESS) 是其中可期待的方法之一。 ESS 的優勢在於製程上的低花費並能提供了良好的能量轉換率。然而，如果能夠導入奈米壓印技術取代原本的深紫外線的微影製程會是一個更大的突破。

”軟性”奈米壓印改良自原本的奈米壓印，以軟性的圖章取代傳統的硬式材質，因此有更好的延展和耐用性並能達到高解析度和良好的均勻度。除此之外，軟性奈米壓印並有機會在高低落差較大的試片上展現良好的性能。軟性奈米壓印可以解析為下列三種步驟：(1)製作軟性圖章 (2)壓印步驟 (3)圖形轉換。首先為了證明此技術在量產上有其優勢，我們比較了此技術和目前主要的下世代微影技術，並以 cost of ownership (CoO)模型來證明軟性奈米壓印的可行性。

在製作軟性圖章上，一個適合的硬質罩幕層是影響表現的重要條件之一。不理想的幕層設計會導致圖形的變形和崩解。在此，我們考慮了變形的模型進而設計出一個適當的結構，並在測試中證明此結構的穩定及可利用性。另外在壓印的步

驟中，抗黏層的塗佈有相對性的重大影響。實驗的過程中，我們並發現要達到均勻的表面並能保持較高的光阻高度差必須考量到適當的光阻塗佈厚度。由於奈米壓印的基本原理來自於光阻的流動和空洞的填補。在此概念下，成功發展出一個簡易的計算求出最恰當的光阻塗佈厚度，並且藉此達到良好的壓印成果。

在壓印的圖形上會有一層多餘的光阻層需要去除以達到後續良好的蝕刻圖形，在此我們以氧氣電漿蝕刻的方法與之去除，此法不僅簡單更有顯著的效果。而後續矽的蝕刻則以SF_6 混合O_2來進行研究。本文中討論了蝕刻製程中幾個重要的條件，例如壓力，氣體流量和能量功率。在氧氣的濃度增加的情況下，側壁的保護相對的提高但也因此減弱了蝕刻的能力。研究中也顯示在低功率和高壓力下，蝕刻的表現是較好的，無論是在側壁保護或是相對的蝕刻率上。

但也由於製程上的限制，單純以 SF_6 混合 O_2 進行的蝕刻無法達到 ESS 對孔洞深度的要求。因此，我們刻意蝕刻出倒金字塔形狀的孔洞結合陽極氧化的步驟達到極深的孔洞。但又考量到此條件下的孔洞，其直徑的變異太大可能會增加 ESS 的困難度。因此，我們在矽晶片上沉積了一百奈米的二氧化矽當作額外的硬質罩幕層，而成功的製作出符合 ESS 要求的周期性孔洞。最後，實驗的結果客觀地顯示出軟性奈米壓印有著其多樣的發展性，且能在低花費且快速的情況下完成。

Development of a nano imprint process for fabricating submicron dot array in large area

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Abstract

Thin-film solar cells are one of the promising approaches for the next generation of solar cells among various approaches due to their low price and wide applications of different substrates. There are many techniques to achieve thin-film solar cells. A layer-transfer process based on the empty-space in silicon (ESS) technique has a promising opportunity, because it presents potentially a better tradeoff between energy conversion efficiency and cost than other techniques. However, its biggest challenge is to reach competitive prices. The development of nano imprint lithography (NIL) as an alternative to optical lithography such as deep-ultra-violet (DUV) lithography is an important aspect of decreasing the cost.

Soft-NIL is an improved technique providing a high-resolution and good uniformity patterns by using a soft stamp instead of a rigid stamp. The soft-NIL process is briefly composed of the following three steps: (1) Fabrication of soft stamp, (2) imprint process and (3) pattern transfer. Here, we compare soft-NIL with other possible next generation lithography, and use the model called cost of ownership (CoO) to prove the feasibility of soft-NIL.

For the fabrication of the soft stamp, a suitable hard mask as a mold for soft stamp is the most important factor that affects the performance. Inappropriate design of the hard mask will result in deformations such as buckling, lateral collapse, and roof

collapse. After considering deformation models, we fabricate soft stamps avoiding the above deformations. Besides, the soft stamp is proved sufficiently stable and reusable even over ten times imprint.

Concerning the imprint process, an anti stick layer coating strongly affect the performances, and the findings for imprinting a uniform structure and high resist contrast over a large area by calculating a suitable polymer thickness are demonstrated. Based on the optimized concerns including squeeze flow and cavity-filling mechanisms, we successfully imprint uniform structures with very thin residual layers over a large area.

Oxygen plasma is used to remove the residual layer, and anisotropic etching of silicon is performed by SF_6 and O_2 plasma. We prove the importance of accurately removing residual layers, and the essential of uniform imprinted structures. We report detailed discussions of the link between the etching profiles and etch parameters such as power, pressure, and gas flow. When higher O_2 concentrations are added, it causes a better sidewall passivation but also decreases the etching rate of silicon. Therefore, improvements of the anisotropic etching are shown by applying low power density and high pressure since low power density strongly decreases the lateral etching and high pressure increases the silicon-etching rate.

Extremely deep pores achieved are achieved owning to a combination between dry-etch and anodization, because the soft-NIL patterning process allows to make regular pores. A better control of anodization is performed by an inverted-pyramid-shaped cavity intentionally etched providing specific points to etch. Based on this thought, we take advantage on a negative effect existing in dry etching process, which results in slopped sidewalls.

In the end, we deposit 100 nm silicon oxides before coating the thermal resist, and use this oxide as mask to etch silicon for the desired structures. The imprinted structures show the same property when imprinting above silicon oxide. Therefore, we could fabricate desire structures based on proper etching conditions in this process, and the results show many possibilities of soft-NIL.

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List of abbreviations

DUV deep-ultra-violet

PV photovoltaic

TFSC thin-film solar cells

ESS empty-space in silicon

NIL nano imprint lithography

FDTS 1H,1H,2H,2H ferfluorodecyltrichlorosilane

EBL electron beam lithography

AFML atomic force microscope lithography

PDMS polydimethylsiloxane

Soft-NIL soft nano imprint lithography

CoO Cost of Ownership

WPH wafers per hour

WPM wafers per mask

ARC antireflective coating

UV ultraviolet

PMMA polymethylmethacrylate

Tg glass transition temperature

SCR space charge region

SEM scanning electron microscope

AFM atomic force microscope

Chapter 1: Introduction

Thin-film solar cells are one of the promising candidates for the next generation of solar cells among various approaches. There are many techniques to achieve thin-film solar cells, and layer-transfer processes have a promising opportunity. An epi-free method combined with reorganization of macro pores is one of these layer-transfer methods. However, the epi-free process involves optical lithography, which is still an expensive and time-consuming step. If we can replace this step by another advanced lithography process, it will save a significant amount of energy and cost. Various alternative lithography techniques are under development and, among the various approaches, nano imprint lithography reveals a higher potential than others to replace the conventional optical lithography. The different points will be discussed in this introduction chapter.

1.1 Solar cells

Developing green energies, which come from natural resources such as sunlight, rain, wind, tides and geothermal heat, is one of the best ways making the environment better. Compared to conventional energies, green energies are cleaner, and renewable unlike fossil fuels which keep harming ther world. Moreover, oil prices reach records year by year, and will definitely not depreciate in the future. In other words, we need to focus on sustainable energies to replace fossil fuels. All of the above issues push scientists into developing a new energy, which can be inexhaustible, and affordable.

Solar cells are a promising candidate for green energy, because their energy is directly derived from the sun, which is a long lasting source of energy, available almost everywhere. Utilization of solar energy creates no pollution except in the production and maintenance of solar cells lead to some amount of pollution, and this is the most important advantage that makes it more practical than conventional energy like oil, which will release greenhouses gases into our air when it burns.

The mechanism of solar cells can be simply expressed as following. Photons from the sunlight hit the photovoltaic (PV) cells and are absorbed. Then, electrons are released from their atoms, allowing them to flow through the cell to produce electricity. Different cells are connected together in series and encapsulated into modules. Later, these modules can be constructed into an array to provide a larger current and voltage. There are many different types of solar cells, and (multi-)crystalline silicon solar cells are current industry leader. The main reason is that crystalline silicon solar cell can offer higher conversion efficiency, but the high cost of fabricating them is a main issue. As a result, scientists keep focus on researching new kinds of solar cells offering more affordable price. Based on the tradeoff between cost and efficiency, thin-film solar cells are gaining interest.

1.1.1 Thin-film solar cells (TFSC)

Thin-film solar cells (TFSC) are a promising approach to achieve a low price, and can be applied on variety of different substrates. TFSC cover a wide range of technologies, and we will focus on the issue of thin-film crystalline silicon. Except the silicon based TFSC, other two-component (binary) materials attractive for thin-film solar cells are: GaAs, CdTe, Cu_2S, Cu_2O, InP, Zn_3P_2, etc, but the scarcity of these components and even their toxicity limit their developments [1-1,1-2]. The other thin film technologies, organics and dye-sensitised cells present immense impact on the TFSC industry in the future due to their inexpensive processing and flexible applications [1-3, 1-4]. However, silicon based solar cells have their irreplaceable advantages over the other thin film technologies on its abundance of material, non-toxicity and great connection with the current semiconductor industry. Unfortunately, the thickness of this thin crystalline layer cannot easily be obtained from current wafer techniques.

Hence, there are two ways to make a thin crystalline film; one is to directly deposit a crystalline layer on a substrate, and another is to transfer a thin crystalline layer from a thick wafer to a foreign. The first method requires the use of the epitaxy [1-5] that refers to the method of depositing single-crystalline film on a single-crystalline

substrate. Although epitaxy is capable of producing high-quality layers, it is low-throughput and high temperature requirements for high-quality layers represent a bottleneck for industrial processes. The latter method, on the other hand, does not require epitaxial deposition and therefore presents potentially a better tradeoff between energy conversion efficiency and cost than the other techniques. A layer transfer process based on the empty-space in silicon (ESS) technique [1-6] would form a high-quality crystalline layer without the step of epitaxy. Therefore, we call this process "Epi-free" method. A plate-shaped ESS below the surface of the silicon can be fabricated by connecting the spherical empty spaces (Figure 1.1-(c)), which are formed by surface migration of Si on the patterned Si substrate upon annealing, and this surface layer above the empty-space is potentially detachable.

1.1.2 Decreasing the cost of the epi-free method

The whole solar-cell process based on the epi-free techniques is composed of the following steps (Figure 1.2). (1): Formation of regular macropores by deep-ultra-violet (DUV) lithography combined a dry etching process. (2): Annealing of these pores for formation of a detachable and singlecrystalline thin film. (3): Solar-cell processing of the first side of the film. (4): Bonding and detachment. (5): Processing of the second side.

Avoiding an expensive process like optical lithography with DUV light as source for forming regular nanostructures is the main idea of this thesis, because the cost of lithography equipment constitutes 25% to 35% of the cost of all semiconductor fabrication equipment [1-8]. DUV lithography equipment costs over $ 10 million, and the cost of lithography equipment has increased at a nearly exponential rate over the past 30 years [1-9]. The limited throughput of DUV lithography is another major disadvantage of this process. If we want to replace it, we need to solve uniformity, resolution and throughput issues. Therefore, I will discuss some possible solutions which are considered as low-cost lithography in the next section (1.2).

1.2 Possible solutions for low-cost lithography

Suitable unconventional lithography should meet the epi-free process requirements together with other important issues, so to estimate the feasibility of these possible solutions we base ourselves on the following points. First, the whole process has to be more affordable than the optical lithography like I-line and DUV module, with an acceptable yield. Second, it should have a reliable throughput. Third, it has to meet the requirements on the porous structures that are needed for the epi-free method. The requirements on the porous structures are that these pores can be reorganized to form a thin film. In detail, the important parameters (Figure 1.3) that control the empty-space in silicon are pore diameter (d), pore wall thickness (w), aspect ratio, and length (l). Transformation into a single sphere requires the aspect ratio (l/d) follow the empirical rule between 3 and 9.5, and pore wall thickness should be equal or smaller than the pore diameter [1-10, 1-11, 1-12]. In our expectation, we want to make structure of around 500 nm diameter, and the depth have to be higher than 1.5 μm.

The following section introduces some possible unconventional lithography, and compares them. In the end (1.3), the most appropriate method among them is described.

1.2.1 Self-assembly process

With methods based on self-assembly, disordered components automatically form organized structures from local interactions, without external force like physical contact and optical lithography. Block copolymers, colloidal lithography, and porous alumina are three of those methods of self-assembly that may let us pre-pattern our wafers.

Block copolymers is a technique that uses self-assembling diblock copolymers as nano lithographic masks to create nanostructures [1-13]. In this reference, for example, diblock copolymer micelles were generated in a toluene solution. These micelles were loaded by a noble-metal salt. After dipping a substrate into this solution, a monolayer of ordered micelles is generated, covering almost the complete surface. After treatment in

hydrogen plasma, all of the organic components are removed and only crystalline metal clusters of few nanometer sizes remain. This metal cluster mask can be used directly in a chlorine dry etching process. The unsuitable aspect of this process is that it is not possible to achieve deep pores from the very thin resulting mask, and this process only can fabricate around 30 nm deep pores [1-13].

In colloidal lithography, particles can assemble into organized structures in a liquid [1-14]. The hexagonal close-packed motif they form acts as an evaporation mask; with this method planar arrays of diverse nanostructures have been accomplished. Nevertheless, this technology cannot be applicable to cm-large area, and the structure size cannot easily be changed, since it simply mimics the size of the hexagonal close-packed motif [1-15].

Unlike colloidal lithography, porous alumina may be applied to a large area. With this method, ordered pores are used as a template on silicon. In a first step, a layer of aluminum is anodized into porous alumina on the silicon substrate, and etching away the alumina. The next step is to anodize the surface again on certain condition, and the surface will be organized into hexagonal packed arrays. Again, these hexagonal packed can be used as mask to form a structure. [1-16] However, this method is limit by the narrow windows and pitch of the alumina mask.

1.2.2 Nano imprint lithography (NIL)

Nano imprint lithography is a high throughput, low cost, nonconventional lithographic method. It has been listed by MIT's Technology Review as one of ten emerging technologies [1-17], and the international Technology Roadmap for semiconductor announced the inclusion of NIL on their roadmap as a candidate technology to replace optical lithography [1-18]. The concept of NIL is use a mold with nanostructures to imprint the negative structure on a thin resist on a substrate [1-19].

NIL has demonstrated 25 nm feature size, 100 nm pitch, vertical and smooth sidewalls, and excellent uniformity [1-20], and its applications of 150 mm diameter wafers is also achieved [1-21]. The ultimate resolution of nano imprint can be sub-10

nm from further experiment, and paper study [1-22]. Besides, it is also feasible to imprint over a non-flat surface [1-23]. Another advantage of this technique is that the mold is durable, so the imprint process is repeatable. The master mold can be reused multiple times, and as a consequence, the mold itself can be fabricated by a more expensive or more time consuming fabrication method. In addition, the size uniformity area is acceptable if the imprint condition is optimized. Finally, NIL has been successfully in fabricating some nano scale products, and all these advantages push us to research this process as an alternative lithography.

1.3 Overview and the competitiveness of NIL

NIL is a promising method to replace optical lithography in the epi-free method. This section gives an overview of NIL. We will introduce the concept of NIL in 1.3.1, discuss an improved NIL process which is called "soft" nano imprint in 1.3.2, and compare it with conventional fine feature lithography including the calculations of cost of ownership in 1.3.3 and 1.3.4.

The complete process of NIL is composed into following steps (Figure 1.4): (1) Fabrication of the hard mask composed of regular pores by conventional lithography. Pressing this hard mask into the resist which was spin coated on the substrate. (2) Demolding of the hard mask, to duplicate the negative nano structures in the resist. (3) Dry etching to remove the residual layer of resist and etch the substrate. (4) Removal of the remaining resist on the surface.

1.3.1 The concept of NIL

NIL was mentioned for the first time in 1995 in an article by Chou et al. [1-19]. NIL is based on the deformation of a thermoplastic resist coated on the substrate by using a rigid stamp. The work presented in the first article started activities on NIL all around the world. NIL acts as a potential cost-efficient nanofabrication technique and as a way to realize simple devices in a patterning step. Besides, NIL is a promising technique, which allows us to obtain nanometer scale on large size wafers.

A stamp (hard mask) with the desired nanometer features is needed. This is usually fabricated by, for example, optical lithography or electron-beam lithography combined with dry etching. The resist to be printed, a printable polymer, is spun onto a solid substrate. The stamp and the substrate are placed on parallel stages. These are heated up to the printing temperature, which is above the glass temperature of the polymer to be molded and a certain amount of time is allowed for the thermal equilibrium to be reached. Then, the stamp and resist are brought into physical contact and pressure is applied, followed by subsequent cooling and then demolding. In Figure 1.5, temperature and pressure cycle of NIL is shown. The next step is the pattern transfer where an anisotropic etching process, is used to remove the residual resist and silicon etching in the compressed area.

The estimated imprint cycle for NIL is a few minutes. The imprint time mainly depends on three things the viscosity of the thermoplastic polymer, the stamp protrusion size, and of course the heating and cooling time provided by the NIL machines. It can be concluded that by optimizing the imprint time NIL can become a fast nano lithography tool compared to other lithographies. By patterning a single master stamp for NIL by time expensive lithography techniques and then replicating the master stamp by the NIL technique, NIL becomes a rather fast technique for patterning of features in the nanometer range. An obvious use of the technique would be to make optical devices since these often tend to have some periodicity in the structures, and typically demand sub-wavelength patterns in the order of a few hundred nanometers with a resolution in the order of a few tens of nanometers.

Adhesion is a very important issue in NIL. Consequently, the use of anti stick treatment for stamps containing sub-100 nm features is reported [1-24]. Ideally, the resist should stick to the substrate but not to the stamp, so that the stamp can be safely removed safely after the imprint. For a perfect separation, the substrate should have a large surface energy so that the resist may adhere well to it, while the stamp should have a low surface energy. Specifically when the stamp feature size gets smaller the sticking tendency between polymer and stamp is enhanced, demanding an anti stick layer. Appling anti stick coatings can reduce the adhesion between the two surfaces.

Using 1H,1H,2H,2H perfluorodecyltrichlorosilane (FDTS) as anti stick layer to obtain a very low surface energy is presented [1-25]. The resulting silane layer prevents adhesion of the stamp to the surface resist of silicon substrate. Moreover, a low surface energy released layer on the stamp surface not only helps to improve imprint qualities, it also significantly increases the stamp lifetime by preventing surface contamination.

1.3.2 Improved NIL: Soft nano imprint lithography (soft-NIL)

NIL involves applying a high pressure for the imprinting of the patterns into an underlying polymer, and high temperature, which has to be above Tg of the substrate polymer for several minutes. In such conditions, the hard mask like bare silicon or chrome mask supported on a glass plate has a high risk of brittle failure for the mask and the substrate. Therefore, some apparent limitations inherent in the NIL make it somewhat unsuitable for forming high resolution and complex structures, and it is even worse for leading to no pattern formation by using a hard mask [1-28]. Another disadvantage is that this technique is unsuitable in conforming to non-uniform large areas [1-34].

A solution to these problems is the usage of a soft, bendable stamp. This soft material typically is polydimethylsiloxane (PDMS) which has been considered highly effective based on its characteristic of ***low*** elastic modulus and low surface energy [1-35]. These properties allow a PDMS stamp to produce consistent nano-scale imprints on the surface of resists, over large contact areas regardless of a substrate's topographic uniformity by conforming to the surface during contact and yielding during release [1-36]. Moreover, the pressure induced by local irregularities as dust particles will be distributed over the mold, reducing the chance of breaking the substrate [1-37]. Extra care for this technique is to avoid difficulties during the separation of the hard mask from the patterned substrate, but this problem can be solved by coating anti stick layer on the surfaces. Because of these advantages, we developed a soft nano imprint process in this work.

1.3.3 General comparisons with conventional fine feature lithography

To appreciate the potential of NIL, an overview of different modern techniques to produce very fine features discussed in this section: Photolithography, electron beam lithography (EBL), and atomic force microscope lithography (AFML).

Photolithography is based on a projection-printing system in which the image is projected onto a thin film of photoresist that is spin-coated on a wafer through a high numerical aperture lens system. The resolution of the system is subject to the limitations set by optical diffraction according to the Rayleigh Equation [1-26], Resolution=$k_1\lambda$/NA, where λ is the wavelength of the illuminating light, NA the numerical aperture of the lens system, and k_1 a constant that depends on the photoresist. As a result, illuminating sources with shorter wavelengths are progressively introduced into photolithography to generate structures with smaller feature sizes. It is plausible that features as small as 100 nm can be manufactured optically by employing advanced mask resist technologies and DUV radiation, and extreme Ultra-Violet (EUV) lithography is being developed for next generation integrated circuits [1-27]. The sizes of the features fabricated by photolithography are limited to optical diffraction, and the high-energy radiation needed for small features requires complex facilities and technologies [1-28]. As structures become increasingly small, they also become increasingly difficult and expensive to produce. These techniques are capable of generating very small features, but the development into practical commercial methods for low-cost processing still requires great ingenuity [1-29].

EBL refers to lithographic process is the practice of scanning a focused electron beam of to form patterns across a surface covered with resists, and of selectively removing either exposed or non-exposed regions of the resist. The primary advantage of EBL is that it can overcome the diffraction limit and the cost of mask fabrication; thus, it allows a small diameter electron beam to be scanned over a surface. However, it takes a very long time including moving the beam across the surface to expose. The writing speed of an electron beam system in wafers can be estimated by considering the total beam current incident on the wafer and the sensitivity of the resist [1-30]. In a contact-printing mode, EBL can reach a writing speed of 0.02 cm^2/sec, but its exposure systems are rather complex and expensive [1-31].

AFML uses an AFM to oxidize a surface by applying a voltage difference between the tip and the surface [1-32]. The oxidized pattern can subsequently be used as an etch mask to transfer the pattern into the substrate. Applying an AFM it is possible to achieve line widths down to 10 nm and a typical scan speed of the AFM is in the order of 5 μm/sec [1-33]. In the following table, throughput, cost, and resolution of EBL, AFML and photolithography are compared to those of NIL. We can clearly learn the throughput is NIL's strength compared to other process. More importantly, the low cost consumption of NIL is the driven force to push this process into mass production.

Table 1. 1: NIL compared with EBL, AFML, and photolithography.

	Throughput	Cost	Resolution
NIL	High	Low	High
EBL	Low	High	High
AFML	Low	Middle	High
Photolithography	High	High	High

1.3.4 The calculations of cost of ownership (CoO)

Although the optical lithography is still the mainstream process today, scientists are still searching for replacements that have lower cost with fine features. During the development of such new processes, the cost of ownership (CoO) is a possible analysis for users to estimate the practicability of new processes and understand what modifications are necessary. CoO represents the cost of lithography per wafer level and it is widely used to compare lithography costs of various technology options. An integral CoO of lithography is modeled by International SEMATECH to compare the competing lithography technologies in an unbiased way [1-39].

The basic CoO model which is shown in formula {a} assumes that the cost per wafer level is the sum of process, mask, and tool costs [1-39, 40]. The calculations of this

model are determined from the following parameters. Process cost is assigned to the cost of resist and etching process, and this parameter is assumed to be constant as $7 in each calculation [1-41]. Here, we have to notice that this assumption is relatively conservative due to the low resist costs of soft-NIL, and the etch costs are expected to be comparable to that of optical lithography. Besides, there is extra cost of the PDMS (soft stamp), but this material reveals a quite affordable price. Mask usage describes the whole lifetime of single mask during the exposedness. Mask cost is defined as the cost of fabricating the mask including the material and process. The calculations of CoO are predictably reduced in high mask usage and low mask cost. Another key parameter of CoO is the capital equipment cost, which affect the results in a determined way due to its extremely high price in extra-advanced machine. The throughput of the exposure system closely influences the tool cost since the cost of the capital equipment will be reduced over more wafers. Besides, other parameters are assumed constant in all the calculations. First, Lithography equipment annual maintenance costs is always assigned as certain percentage as 5% of capital equipment, and all the equipments will depreciate in 5 years [1-41]. Second, the utilization of the equipment is 70 % no matter of optical lithography or NIL equipment.

$$CoO = P_w + \frac{M_0}{M_L} + \frac{E_0 + (D)(E_M)}{(D)(T)(U)(365)(24)} \qquad \{a\}$$

Here, P_w = Process cost per wafer level (resist and etch costs).

M_0 = Mask cost in $.

M_L = Mask usage in number of wafer levels.

E_0 = Capital equipment costs in $.

E_M = Lithography equipment annual maintenance costs in $.

D = Equipment depreciation in years.

U = Utilization of equipment.

T = Throughput in wafer levels per hour.

.

The strategy of soft-NIL is not as the same as optical lithography, and we can understand the ideas form Fig. 1.6. We use master silicon as hard masks to duplicate numerous PDMS (soft stamp), and use each stamp fabricating imprinted structures. Therefore, we should slightly transform the original formula into a new one which is

suitable for soft-NIL. In the formula {b}, CoO' is also the sum of process, mask, and tool costs. It is noticeable that the difference is the mask costs compared to basic CoO, and it comes from the strategy mentioned before. Each master silicon which is fabricated from optical lithography can duplicate numerous imprinted structures. Therefore, the hard mask cost is derived from the CoO in optical lithography and extra etching cost [1-42]. Besides, the mask usage depends on how many imprinted structures can be obtained.

$$CoO' = P_w + \frac{CoO + Ce}{M_L} + \frac{E_0 + (D)(E_M)}{(D)(T)(U)(365)(24)} \qquad \{b\}$$

Here, P_W = Process cost per wafer level (resist and etch costs)

CoO = Hard mask cost in $

Ce= Etching cost in $

M_L = Hard mask usage in number of wafer levels

E_0 = Capital equipment costs in $

E_M = Capital equipment annual maintenance costs in $

D = Equipment depreciation in years

U = Utilization of equipment

T = Throughput in wafer levels per hour

Given the statistics below, the cost per wafer can be calculated based on the formula. First, the mask costs are simplified as the volume selected for the mask shop is 100 masks per week, but are necessary for comparative modeling. Besides, the results indicate the change in mask cost is very small when mask line with run rates of greater than 100 masks per week [1-43, 1-44]. In DUV lithography, the mask cost around $ 28K. Regarding the mask usage, it tends to have higher mask usage in semiconductor industry. For this reason, the mask usage has the range from 500 wafers per mask (WPM) to 8000 WPM [1-41]. Here, we suppose it to be their average as 4250 WPM. For the soft-NIL, the M_L can be identified based on our experiment. We can fabricate more than ten soft stamps per hard mask, and each soft stamp could imprint more than ten samples. Therefore, the M_L in process is over the product of ten and ten in soft-NIL. As mentioned before, the cost of optical exposure equipment is exponentially increasing, and it is believed that the increase will become more serious.

DUV exposure systems cost over $11 million [1-45]. In general, vendors claim "nano-imprint" tools can process chips at a lower cost than conventional optical equipment. This cost-effective alternative like nano-imprint lithography is sold less than $2 million per unit [1-46]. In the aspect of throughput, SEMATECH assumes an exposure tool-limited throughput and uses technology-specific modeling to predict the throughput. For DUV optical lithography, the throughput is 39 wafers per hour (WPH) optimized with the tradeoff between resist sensitivity and available dose [1-44]. In soft-NIL, the throughput is limited to 12 WPH due to the imprint process cycle of the resist.

The results of the CoO analyses are presented in Table 1.2, and this analysis presents a comparison of the Cost of Ownership (CoO) between the soft-NIL technology and the DUV lithography.. We can see there are two main reasons make soft-NIL be more affordable. First, the major advantage of soft-NIL is associated with the low cost of NIL machines. Besides, the parameter of mask costs in wafer levels is much less than the masks from which they are made through the mask replication strategy. This comparison is believed to provide a low cost procedure in choosing soft-NIL as an alternative process.

Table 1.2: The CoO comparison of soft-NIL and DUV lithography. (Pw=$7, D=5 years, EM= 5% of E0 and U= 70 %)

Technology	Mask cost	ML (WPM)	E0	T (WPH)	CoO (or CoO')
Soft-NIL	$ 25.1+4.48	100	$2 M	12	$ 14
DUV	$ 28K	4250	$11M	39	$ 25.1

1.4 Thesis outline

The final objective of the thesis is to prove whether NIL can be integrated into the epi-free process as a replacement of optical lithography. The epi-free process is in fact based on the reorganization of macro pores to form a thin film layer and require a low-cost and high-throughput lithography technique. The experimental process of

soft-NIL is presented in Chapter 2, and the results of the experiments will be described and discussed in Chapter 3. In Chapter 4, we conclude all findings, and have perspectives for future works.

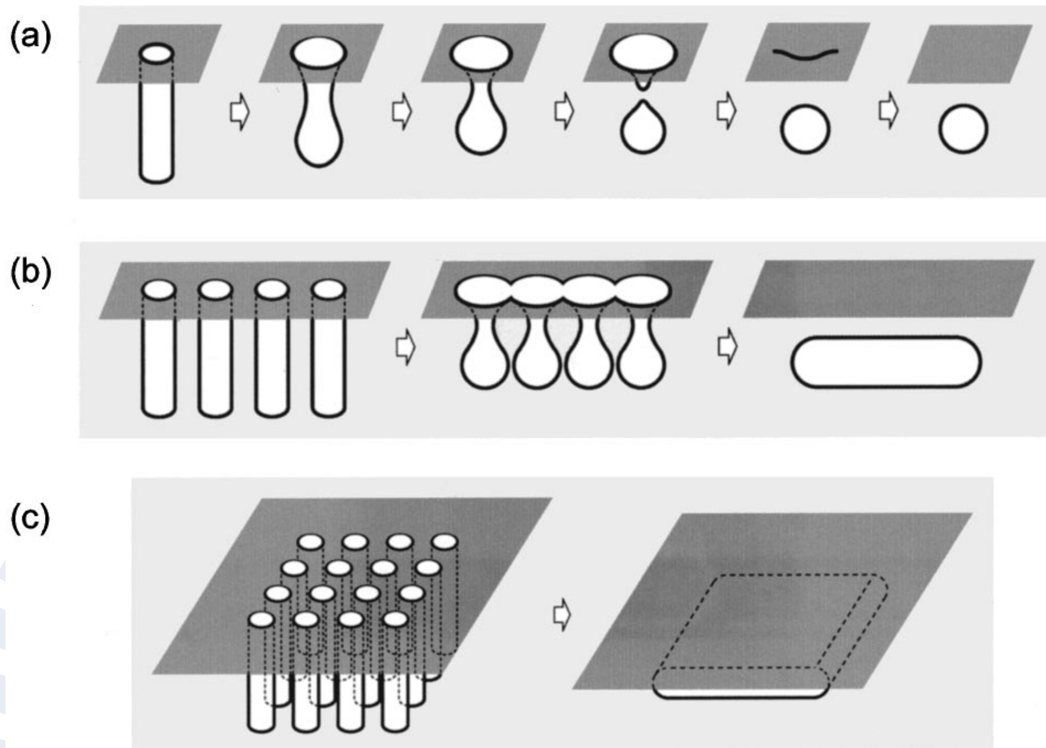


Figure 1. 1: Schematic illustration of self-organizing sequences for the formation of ESS having three typical structures: (a) sphere, (b) pipe, and (c) plate. The surface layer (c) above the empty-space is potentially detachable [1-6].

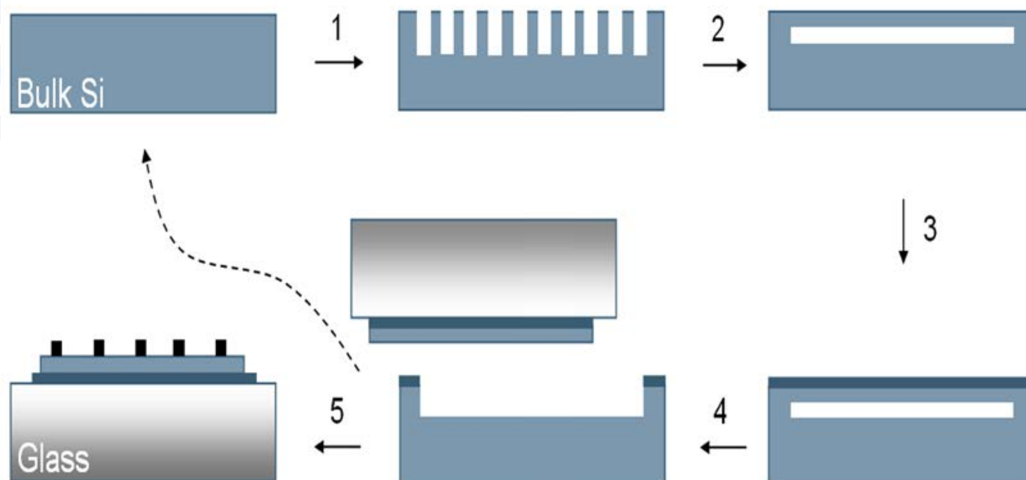


Figure 1. 2: Process flow of epi-free technique [1-7]. (1): Formation of regular macropores by DUV lithography combined with a dry etching process. (2): Annealing of these pores for formation of a detachable and singlecrystalline thin film. (3): Solar-cell processing of the first side of the film. (4): Bonding and detachment. (5): Processing of the second side.

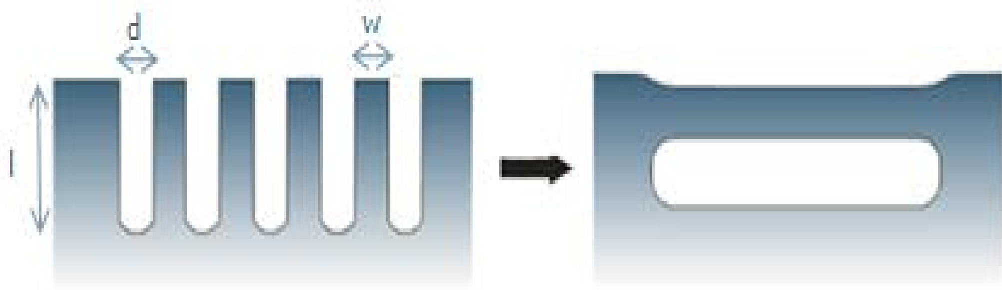


Figure 1. 3: Parameters in porous structure are pore diameter (d), pore wall thickness (w), aspect ratio, and length (l) [1-7].

Figure 1. 4: Process flow of nano imprint lithography.

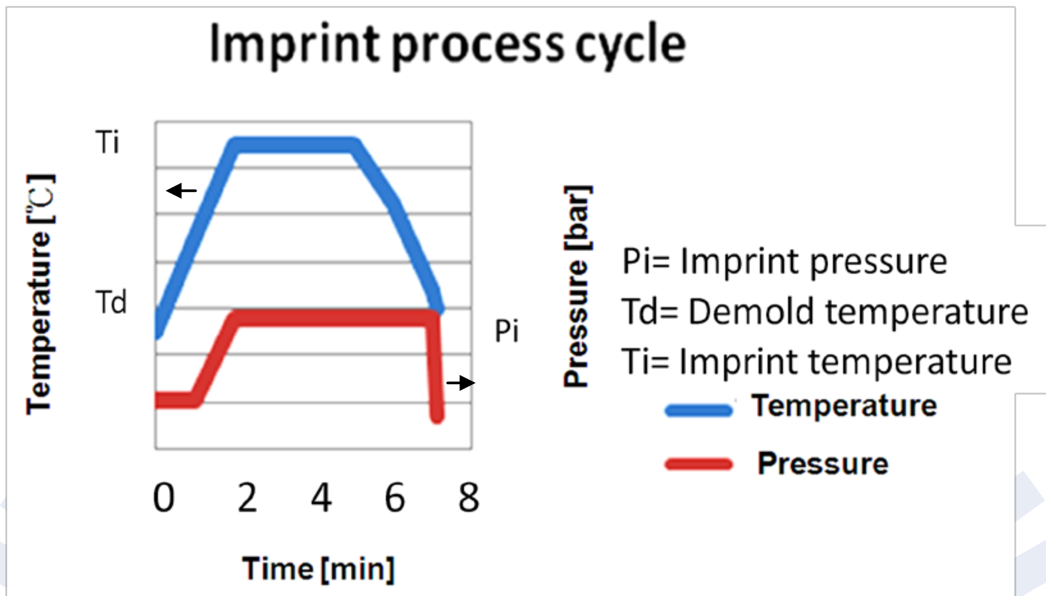


Figure 1.5: Temperature and pressure cycle of NIL.

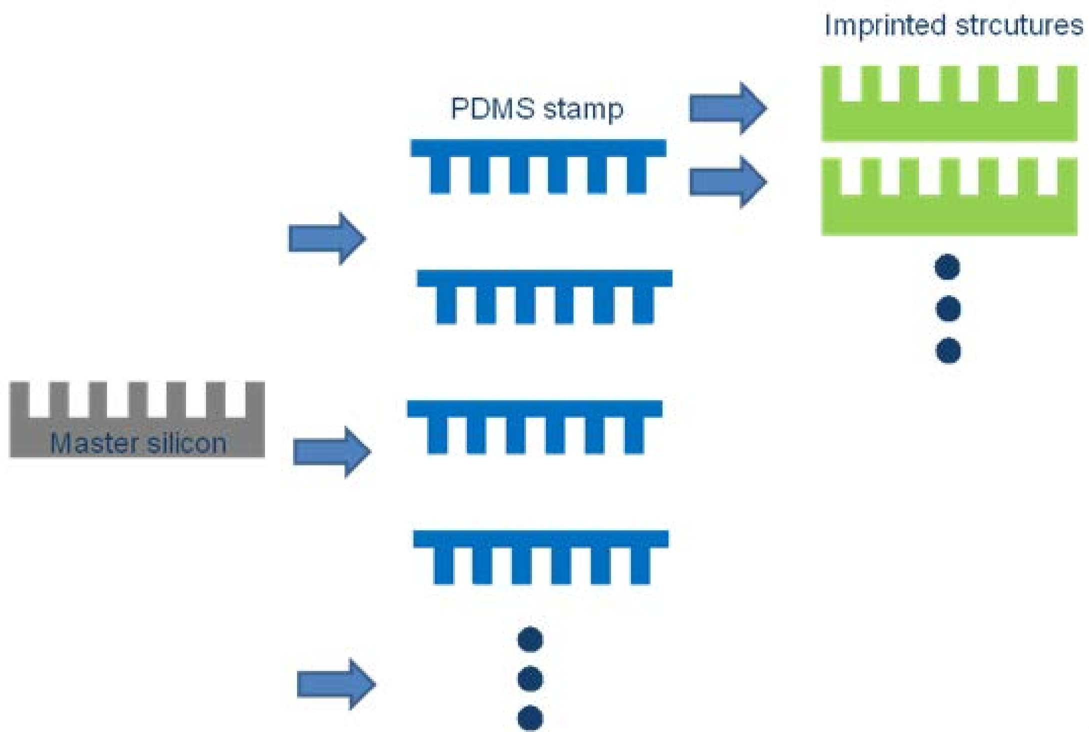
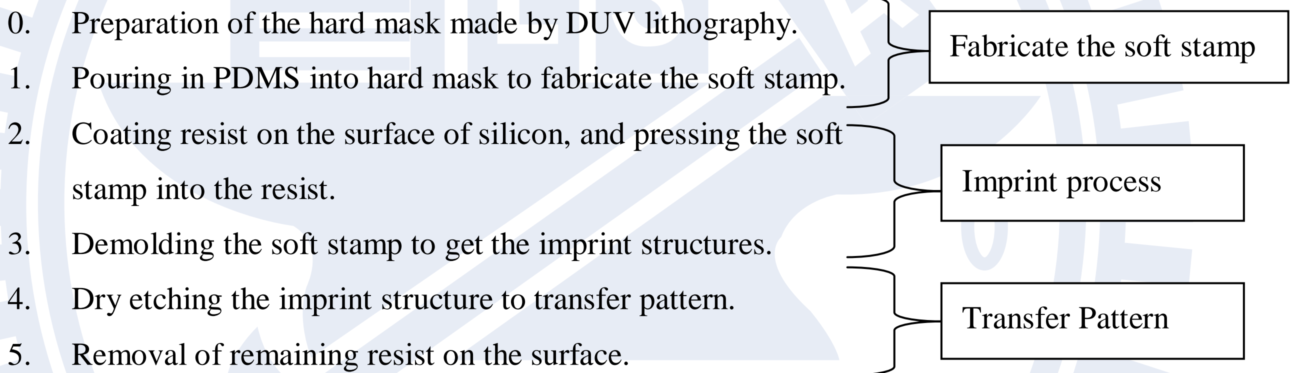


Figure 1.6: Master silicon can be replicated hundreds of times using a soft stamp to imprint.

Chapter 2: Soft Nano imprint lithography

As seen from the comparison of unconventional lithographies in the last chapter, soft nano imprint is very promising to replace the process of DUV lithography in the epi-free method. The complete experimental flow of soft nano imprint lithography (soft-NIL) will be explained in detail in this chapter.

This chapter will be divided into three parts, and the content sequentially follows the experimental steps. We will specify how to make the soft stamp (Section 2.1), the imprint (2.2), and the pattern transfer (2.3). The experimental flow of soft nano imprint is illustrated in the figure below:



2.1 Fabrication of soft stamp

Fabrication of soft stamp is the first step of the previous figure. The process of making hard mask will be presented in 2.1.1. In the following section (2.1.2), we will discuss the fabrication of soft stamps. In the end (2.1.3), characterization of the soft stamp will be discussed.

2.1.1 Hard mask

The hard mask is composed of regular pores which should meet the requirements of the epi-free method. Fabrication of porous structure (Figure 2.2) is processed by DUV lithography of silicon wafers, which are 200 mm in diameter, (100)-oriented and phosphorus doped with a resistivity of approximately 10 Ω cm. The fabrication is accomplished through the following steps.

1. A full RCA cleaning.
2. Growing a 500 nm oxide at 975 ˚C in a H_2O and O_2 atmosphere, and a 50 nm SiON antireflective coating (ARC) was deposited on top of it to improve the resolution by avoiding light reflections.
3. A 650 nm thick photo resist was spun, exposed under 248-nm light and developed.
3. Dry etching the dielectric ARC and the silicon oxide in a parallel-plate etcher by CF_4 plasma. The resist was afterwards removed, first in O_2 plasma, then by a wet etch to remove residues.
4. The wafer was first dipped in phosphoric acid to remove the dielectric ARC and other nitride compounds. Then, silicon were etched in a transformer coupled plasma system in a SF_6 and O_2 mixture. The oxide mask was removed afterwards by a wet cleaning.
5. The wafer received an HF dip and a full RCA cleaning.

Two hard masks (Figure 2.3), which are patterned with circles of around 440, and 460 nm diameters with two different pore depths, are served as soft stamp's mold. The first mask set has pores with 700 nm deep features, while the second one has only 200 nm deep pores. On the other hand, deep pores provide a thicker sacrificial resist layer to be consumed during the dry etch process. Nevertheless, pillars of the soft stamp will become fragile and the adhesion between soft stamp and resist will increase for very high aspect ratios. On the one hand, shallow pores are easier to process but provide a thinner mask, and therefore do not allow etching of high aspect ratio pores. Deeper pores can however be accomplished by an anodization process (This process will be explained in 2.3.3).

We also fabricate the hard mask with shallow pores in different process, and the reason of re-fabricating the hard mask is caused from changing the process

environment. This hard mask is processed by using I-line stepper applied to the silicon, which is 150 mm in diameter, (100)-oriented and phosphorus doped. The fabrication is accomplished through the following steps

1. SC-1 clean the sample for 20 minutes.
2. A 830 nm photo resist was spun, exposed under 365-nm light and developed.
3. Dry etching the silicon in TCP-9400 with Cl_2 and HBr plasma.
4. The wafer was first cleaned in O_2 plasma. Then, SPM clean is performed to remove the remaining photo resist.
5. The wafer received a SC-1 clean.

The depth of the pores is measured through P-10 after etching, and the result is 220 nm which meets our requirements. Besides, the in-line SEM measurement of top view is shown in the Fig. 2.4, and we successfully fabricate the similar hard mask as before.

Before using this hard mask to mold the soft stamp, we clean these samples by the following three steps.

1: Immersion in acetone in an ultrasonic bath for 10 min.
2: Immersion in isopropanol in an ultrasonic bath for 10 min.
3: Ultraviolet (UV) light and Ozone treatment for 15 min.

After cleaning, the hard masks is heated in a small furnace tube of 140 $^{\circ}C$ for 30 minutes, and is coated an anti stick layer which is composed of FDTS to prevent the soft stamp from adhering to the pores' walls.

2.1.2 Soft stamp (PDMS)

The soft stamp is composed of polydimethylsiloxane (PDMS) from Dow corning, named Sylgard 184. The whole process of making soft stamp is as follows.
1: Mix of pre-polymer (base) and cross-linker (curing agent) components. (Default ratio is 10:1).

2: Pour in the above mixture onto the hard mask in a Teflon container. The container's shape is a hollow cube (Figure 2.5) with section of 2*2 cm^2. The container is put into a stainless steel mold (Figure 2.5), and this mold is used to fix the container onto the hard mask.

3: Air bubbles are usually trapped during mixing, so the mold is put into a vacuum oven to degas.

4: Curing soft stamp at a temperature of 110 ˚C for 45 min in an oven, and taking it out at normal temperature until it cools down.

The soft stamp is peeled from the hard mask, and preserved in DI water. Because PDMS is hydrophobic [2-1] and does not react with water, it will remain its property while DI water will prevent dirt to stick on the mold.

2.2 Imprint process

After making the soft stamp from the hard mask, we use this soft stamp to imprint the structure on a resist. Imprint process is the second and third step of the Figure 2.1, and we will specify this process in this section. The process of coating resist on silicon will be presented in 2.1.1. In 2.1.2, we will discuss the imprint process from the soft stamp. Furthermore, some more specific topics like residual layer and uniformity issues about imprint will be discussed in Chapter 3.

2.2.1 Spin coating of the resist

Before spinning resist on the silicon substrate, we clean this bare silicon substrate by the following three steps.

1: Immersion in acetone in an ultrasonic bath for 10 min.

2: Immersion in isopropanol in an ultrasonic bath for 10 min.

3: Ultraviolet (UV) light and Ozone treatment for 15 min.

This kind of clean process plays an important role, because the imprint process is accomplished by physical contact. The pattern will not be transferred where particles are presented or, even worse, wafers mat break due to uneven forces

We use the polymethylmethacrylate (PMMA) based polymer (mr-I 7010E) from Micro Resist Technology as our resist, which is a thermoplastic polymer suitable for nano imprint. The process of coating resist can be divided into three parts. 1: Spinning with a certain speed for 30 sec. 2: Baking wafers for 2 min in 140 ˚C to remove a fraction of the residual solvent. 3: Uniformity and thickness are measured by ellipsometery (The refractive index of this resist is 1.406.). In our experiment we use three kind of thickness resist by 1000, 2000, and 3000 rpm in 30 sec, and they are 160, 120, 95 nm respectively (Table 2.1). Besides, there are some samples are grown 100 nm silicon oxide in H_2O and O_2 atmosphere before coating the resist.

Table 2. 1: The relation table between resist thickness and spin speed.

Spin speed	1000 rpm	2000 rpm	3000 rpm
Thickness of resist	160 nm	120 nm	95 nm

2.2.2 Imprint

The imprint process is based on the property of the thermoplastic polymer mentioned in the previous section. Characteristic of thermoplastic polymer is based on its glass transition temperature, Tg, in the order of 50 ˚C-120 ˚C dependent on its molecular weight. In the work presented here, PMMA with a molecular weight of 35 kg/mol and a glass transition temperature of 60 ˚C is used [2-2]. When resist is heated to temperatures above 60˚C it behaves as a purely viscous liquid, and when the stamp is pressed into a resist film at this temperature the resist responds with a squeeze flow. After pressing the stamp into the polymer and substrates are cooled while keeping the applied pressure in order to release any stress and to prevent the polymer from flowing back. When the stamp and substrate are cooled to a temperature below the glass transition temperature the stamp is removed and the pattern from the stamp is

inversely replicated into the polymer, and there is a thin residual layer of resist left underneath the mold protrusions.

In the process cycle, PMMA is heated to 130˚C, and the soft stamp with nanometer-scale patterns is pressed into the films with a pressure of 30 bar for several minutes, during which the polymer can flow to fill in the volume delimited by the surface topology of the stamp for imprinting the pattern. After cooling to a temperature below 60 ˚C, the stamp is detached from the printed substrate. In Figure 2.6, the schematic of imprint is shown with its characteristic temperature and pressure cycle. Before imprinting, the soft stamp is heated in a small furnace tube of 140˚C for 30 minutes, and is coated with an anti stick layer which is composed of FDTS to prevent the resist from adhering to the pores' walls in soft stamp.

2.3 Pattern transfer

After imprinting structures into the resist, the next process is to use this imprinted structures as a mask to transfer patterns by dry-etch. The residual layer of PMMA is etched first, to open a silicon window. In a next step, the silicon is etched by reactive ion etching in a ML200RF. The figure below (Figure 2.7) illustrates the process flow of pattern transfer. Etching residual layers to open silicon windows will be discussed in 2.3.1, and we will discuss of etching of silicon into deep holes in 2.3.2. The purpose and theory of anodization process will be presented in 2.3.3.

2.3.1 Residual layer remove

After imprinting, there is a thin residual layer of polymeric material left underneath the mold protrusions. For most applications, this residual layer is removed by an anisotropic O_2 plasma-etching process to complete the pattern definition. Since the residual polymer layer is only several nanometers thick, the oxygen plasma etching process can be relatively short, thus minimizing the damage of the imprinted patterns during etching.

In our experiment, we try two different O_2 recipes to etch the residual layer and open the silicon window. The first etching carries out a high etching rate. However, since the residual layer is only a few nanometers, only one second of etching is needed in this case, which is too short for a good reproducibility and control. Therefore, we developed new O_2 recipes with a lower etch rate. After adjusting the condition, a new O_2 etching results in a reasonable etching time based on our etching thickness. The condition of these two O_2 recipes in Table 2.2 and etching rate is presented in Figure 2.8.

Table 2. 2: The condition of these two O_2 recipes

	Power	Gas pressure	Gas flow of O_2
O_2 recipes	200 W	200 mTorr	200 sccm
New O_2 recipes	50 W	50 mTorr	50 sccm

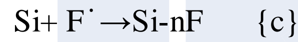
2.3.2 Silicon etch

The process of etching silicon for desired features of cylinder-shaped pores is the main goal of etching silicon. Any deviation from the pattern results from different gas reactivity, pressure, power, etc. In general, etching can be divided into wet and dry etching, and either method can induce isotropic or anisotropic etching. Isotropic etching etches in all directions equally, and leading to mask undercutting with a rounded etching profile (Figure 2.9). Anisotropic etching is directional and is either chemically or physically (Figure 2.9). In our application, anisotropic etching has more opportunity to achieve high aspect ratio of cylinder-shaped pores. Selection between two different methods in anisotropic etching, the dry etching has better selective than the wet etching towards PMMA and silicon.

The aim of pattern transfer is to find a complementary set of materials and etchants, thus allowing good selective and desired patterns. Thus, deep anisotropic dry etching in silicon has become an important task for development of regular deep pores. Several approaches can be used to inhibit lateral etching during the process and thereby

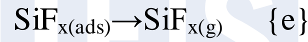
maximize the anisotropy, and a wide range of chemistries allow suitable sidewall passivation to be formed during the etch [2-4]. Here the passivation layer directly results from the chemical reaction between the dissociated precursor gas and the silicon, possibly also with mask material contribution.

The silicon etch cycle uses SF_6 to proceed [2-5], and F can proceed with silicon etching by absorption followed by product formation and desorption as a gas ($_g$) illustrated in equation {c}, {d}, and {e} where ($_{ads}$) means adsorption onto the surface (2-6).



$$Si + F^{\cdot} \rightarrow Si\text{-}nF \quad \{c\}$$

$$Si\text{-}nF \rightarrow SiF_{x(ads)} \quad \{d\}$$

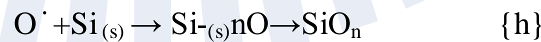


$$SiF_{x(ads)} \rightarrow SiF_{x(g)} \quad \{e\}$$

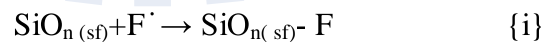
In the silicon passivation cycle, we use SF_6 combined with O_2 as dry etch process to fulfill anisotropy. Considering a simple model of this mix gas [2-6], equation {f} and {g} illustrate the formation of ion and radical species by electron impact dissociation, and the role of O is primarily seen as that of passivating the silicon surface by reacting with the silicon to absorb on the surface to form an oxide, illustrated in equation {h} where ($_s$) and ($_{sf}$) indices denote surface and surface film respectively. The surface passivation layer (silicon oxide) will be removed by the F adsorbs onto the surface (equation {i}) and the ion bombardment plays the critical role in the removal of the passivation film by enhancing the adsorption, reaction and desorption illustrated in equation {j}.

$$SF_6 + e^- \rightarrow S_xF_y^{+} + S_xF_y^{\cdot} + F^{\cdot} + e^- \quad \{f\}$$

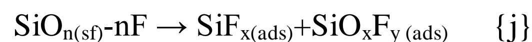
$$O_2 + e^- \rightarrow O + O^{\cdot} + e^- \quad \{g\}$$



$$O^{\cdot} + Si_{(s)} \rightarrow Si\text{-}_{(s)}nO \rightarrow SiO_n \quad \{h\}$$



$$SiO_{n\,(sf)} + F^{\cdot} \rightarrow SiO_{n(sf)}\text{-}\,F \quad \{i\}$$



$$SiO_{n(sf)}\text{-}nF \rightarrow SiF_{x(ads)} + SiO_xF_{y\,(ads)} \quad \{j\}$$

In short, the vertical etching rate is sustained by ion bombardment at high fluorine content while lateral etching is reduced by oxygen sidewall passivation. For our

experiments, four different silicon plasma etching processes are tested, and the first one is merely silicon etching without any passivation.

1) Etching in SF_6 (100%) at a pressure of 100 mTorr, a flow rate of 100 sccm SF_6, and a power of 100 W.
2) Etching in SF_6 / 10% O_2 mixtures (SF_6/ O_2 = 100 sccm/ 10 sccm) at a pressure of 100 mTorr and a power of 100 W.
3) Etching in SF_6 / 30% O_2 mixtures (SF_6/ O_2 = 100 sccm/ 30 sccm) at a pressure of 100 mTorr and a power of 100 W.
4) Etching in SF_6 / 40% O_2 mixtures (SF_6/ O_2 = 100 sccm/ 40 sccm) at a pressure of 100 mTorr and a power of 100 W.

The etching rates of resist in Figure 2.10 for these four different etching conditions. We can see that the etching rate increases when the oxygen content increases. A trade –off between anisotropy and resist consumption will have to be found.

After pattern transfer, the remaining resist is removed and the substrate cleaned by the following two steps. (1) Immersion in acetone in ultrasonic bath for 5 min. (2) Immersion in IPA in ultrasonic bath for 5 min.

2.3.3 Anodization for deeper pores

Because of the limitations of our experiment, we cannot fabricate high aspect ratio pores only by dry etching, which merely use a single layer of PMMA as mask, but anodizing the "pre-patterned" structure is a possible way to fabricate deep and regular pores. Hence, combining soft-NIL with the anodization process fabricates deeper pores which can meet the requirements of the epi-free method.

The most prominent feature of anodization of silicon is the formation of porous silicon (PSi), which was discovered by Uhlir of Bell Labs in the late 1950s [2-7]. This technique has been studied intensively because of its potential in producing porous silicon in an affordable and simple process, and there are variety of discussions on different models and mechanisms [2-8]. Here we focus on the model discussed below.

Theoretically, anodic dissolution of Si requires the presence of positive carriers (h+) at the Si and electrolyte interface. When a silicon wafer is immersed into an electrolyte, a space charge region (SCR), which is an energy barrier, is generated [2-9]. The silicon-electrolyte interface then behaves like a diode, because the SCR creates Schottky barrier that the holes must cross for the silicon to be etched. However, the SCR is not homogeneous over the whole surface. If some pores exist on a silicon-electrolyte interface, the SCR is thinner and the electric field is larger at sharp edges of the pores compared with the other flat areas. Holes (h+) thus gathered around the pores tips result in preferential electrochemical etching at the tips. Besides, the passivation of the pore walls is ascribed to the depletion of holes, so the SCR passivates the pore walls against dissolution [2-9]. This mechanism results in formation of deep pores at pre-patterned sites. Hence, a better control of the porous structures is obtained by intentionally pre-etching inverted-pyramid-shaped cavities providing specific points for pore nucleation. In addition, these pre-patterned sites can be fabricated by soft-NIL.

Here we anodized n-type silicon under front side illumination in hydrofluoric acid (HF) based electrolytes. For n-type silicon, the dissolution reaction requires illumination since the dissolution reaction involves holes at the semiconductor electrolyte interface, which are minority carriers in n-type Si. In the anodization experiment, we imprinted our soft stamp into 5 cm x 5 cm one-side polished (100)-oriented n-type silicon wafers, phosphorus-doped, with resistivity of 0.2-0.3 Ω cm. After imprinting and suitable dry etching, samples are cleaned in the following four steps (1) $1H_2O_2:4H_2SO_4$ for 10 min at 80 ˚C, (2) Water rinse, (3) HF-dip and (4) Water rinse. The sample's front side is exposed to electrolyte which is composed of HF and ethanol with a ratio of 1:5 (9 wt% HF), and illuminating the front side of silicon wafer to generate electron-hole pairs (Figure 2.11) [1-7]. The lamp is a 50 W tungsten-bulb halogen lamp, and quartz-glass beaker acts as a lamp protection, which play a role of screen against HF vapours.

2.4 Characterizations of the soft stamp

Since the characteristics of PDMS are transparent, soft and nanometer structures, there exists a need for characterizations. In this section, all the characterization techniques that we tested will be presented, and it will be divided into the visual inspection and the topography measurement.

2.4.1 Visual inspections

Concerning the measurement of soft stamp which is transparent, and the features of our sample are just few hundred nanometer. Hence, it is hard to measure by normal optical microscope. However, optical microscope is a simple way to measure samples compared to other tools, because it is easy to operate and a time saving measurement. A high-resolution microscopy is introduced here. We use HIROX (KH7700) high-resolution microscopy to measure our sample. In addition, it can magnify objects 7000 times with a nice resolution, in other words, we can see 400 nm by eye. Although we can use this equipment to measure our samples, we still need another equipment to measure the cross section and higher resolution topography.

2.4.2 Topography measurements

The optical profilometer (NT-3300) which is a product from company Veeco was the first equipment we test. Optical profilometer brings white light interferometry to acquire data, and analyzing to perform surface topography. We measure the results on soft stamp (PDMS), and hard mask (Silicon). Each pixel, when measured with the largest magnification (100x), is only 0.08 to 0.1μm wide. This means that only 7 - 8 pixels cover one period, not enough to see the depth accurately (Figure 2.12). However, the problem regarding our samples is the structure is too small to be measured accurately with this optical profilometer. Even if the results of hard mask are some regular circles, we cannot acquire better resolution than this. In addition, the same kind of image can be measured with optical microscope. Besides, we cannot clearly analyze the results of soft stamp, because PDMS cannot reflect enough light to produce good image.

Dektak Stylus Profiler is additional equipment we use, and it is an instrument, which provides profile data of a sample detecting the vertical detection of a stylus in contact with the sample which is moved horizontally across the sample surface. The vertical movements of the stylus is measured and recorded simultaneously during the scanning, which reveals the topographical structure of the surface. However, the tip we use is micrometer scale, and it is too large for our structure. Therefore, it cannot sense our patterns when measuring.

We also use Scanning electron microscope (SEM) to measure soft stamp. There a problem exists, because PDMS is not conductive. Hence, we have to coat a conductive layer on the surface. We coat gold on PDMS at first time, but the adhesion between each other is not good. Therefore, there is no result from this sample. After literature survey [1-38], Cr has a better adhesion property with PDMS. However, coating Cr makes this measurement complicated, so we find another method to acquire structure from PDMS. The most suitable measurement of soft stamp is atomic force microscope (AFM). We can acquire a good resolution of topography and measuring the depth profile. Besides, using rigid tips instead of soft tips to measure can allow a better resolution of PDMS. Because PDMS will slightly adhere to soft tips, rigid tips do not stick to PDMS so much.

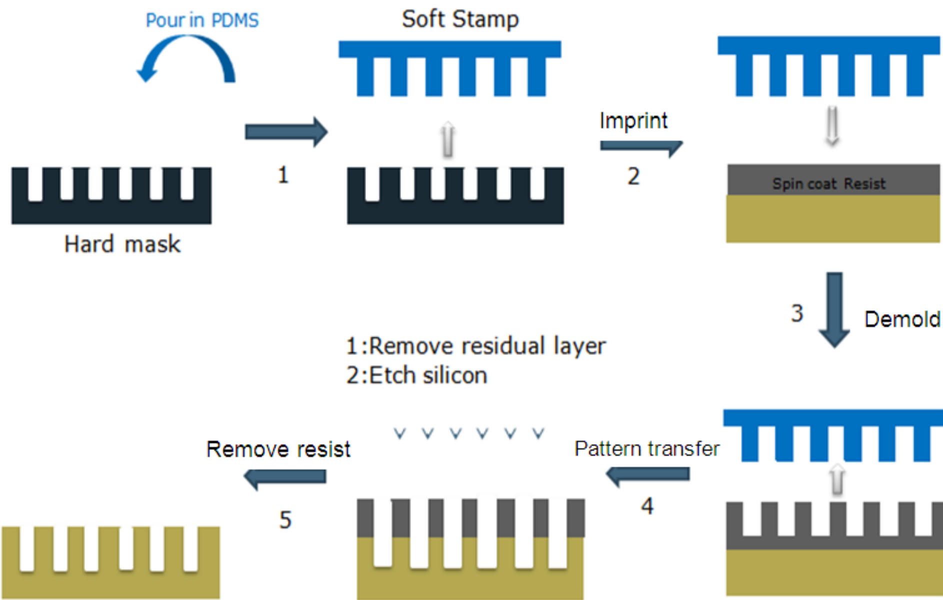


Figure 2.1: Experimental flow of soft-NIL, which is composed of soft stamp fabrication in the step 1, imprint process in the step 2 and 3, and the pattern transfer in the step 4 and 5.

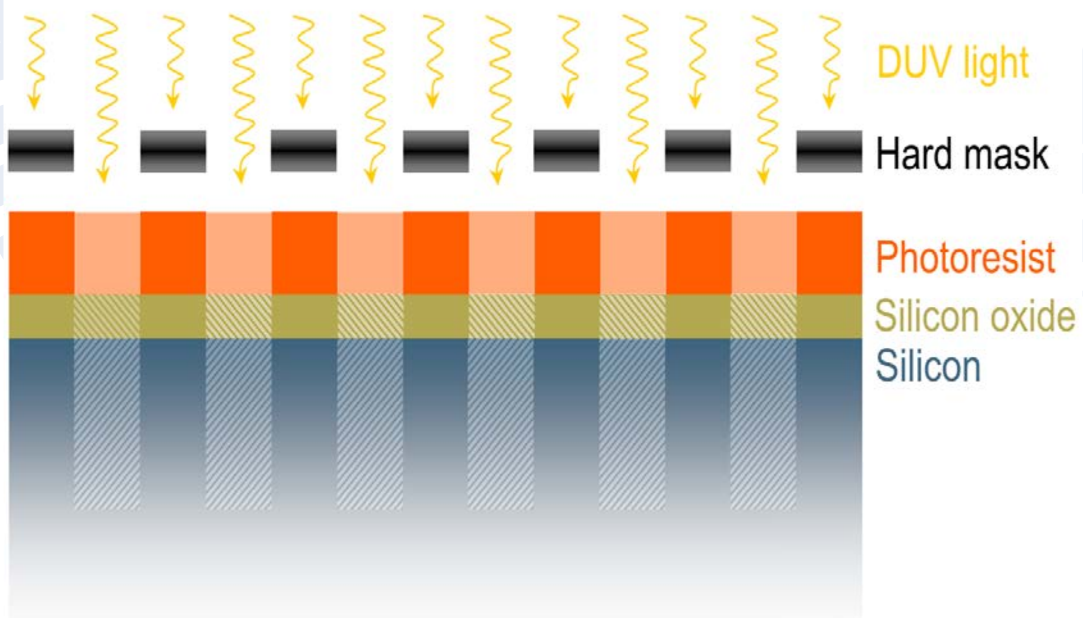


Figure 2 2: The fabrication of the porous structure by DUV lithography and dry etching [1-7].

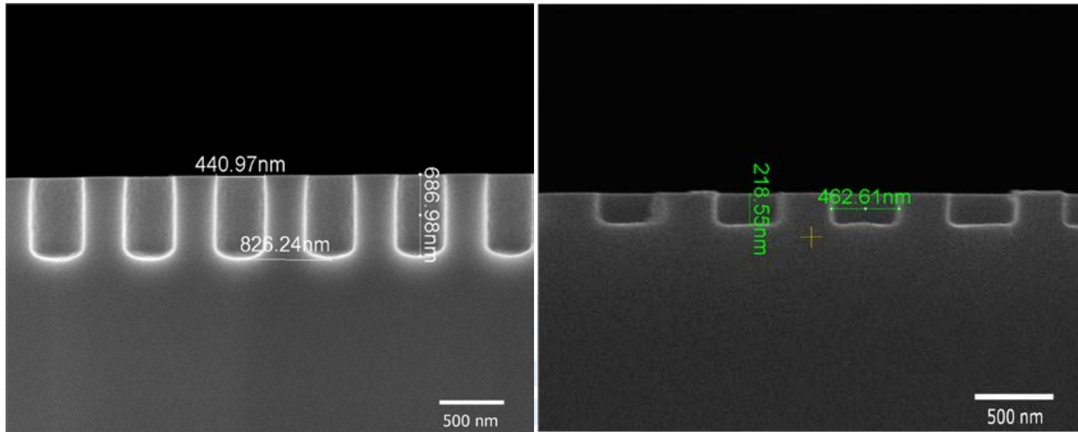


Figure 2. 3: Two silicon structures used as hard masks. The left one is composed of 440 nm diameter and 700 nm deep pores. The right one is composed of 460 nm diameter and 220 nm deep pores.

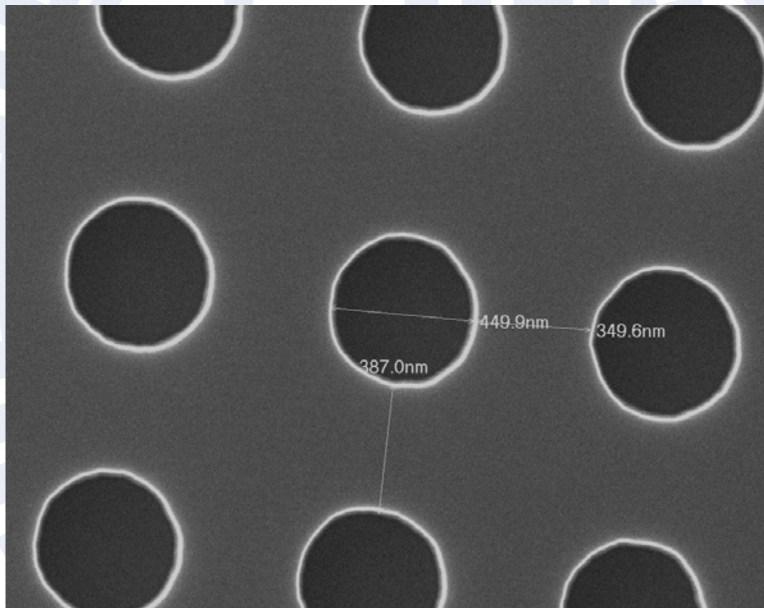


Figure 2.4: SEM image of samples which is acted as hard mask, and the circles are composed of 450 nm diameter.

Figure 2. 5Teflon container (left) and stainless steel mold (right) used to fabricate the soft stamp.

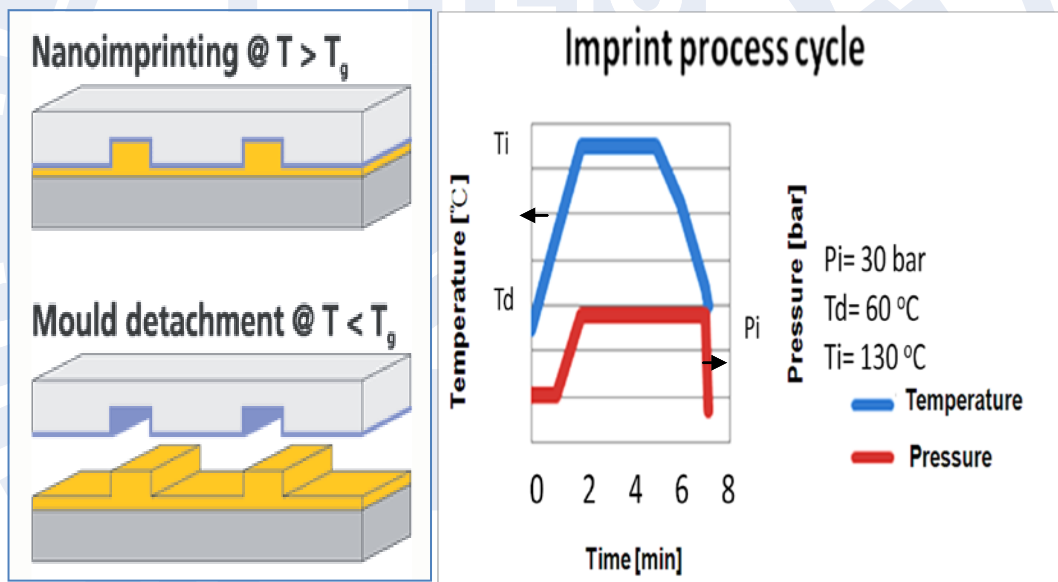


Figure 2.6: Schematics of the imprint process (left) [2-2] and the temperature/pressure cycle (right).

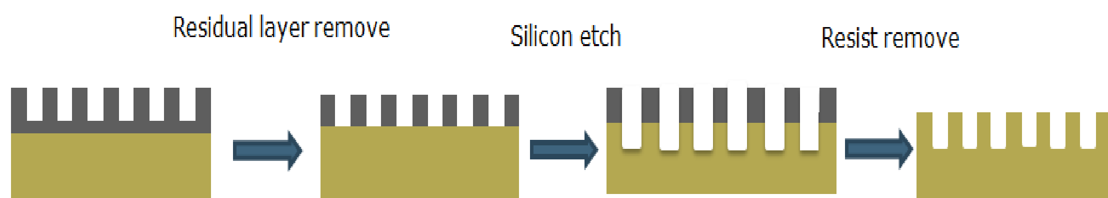


Figure 2. 7: Process flow of pattern transfer.

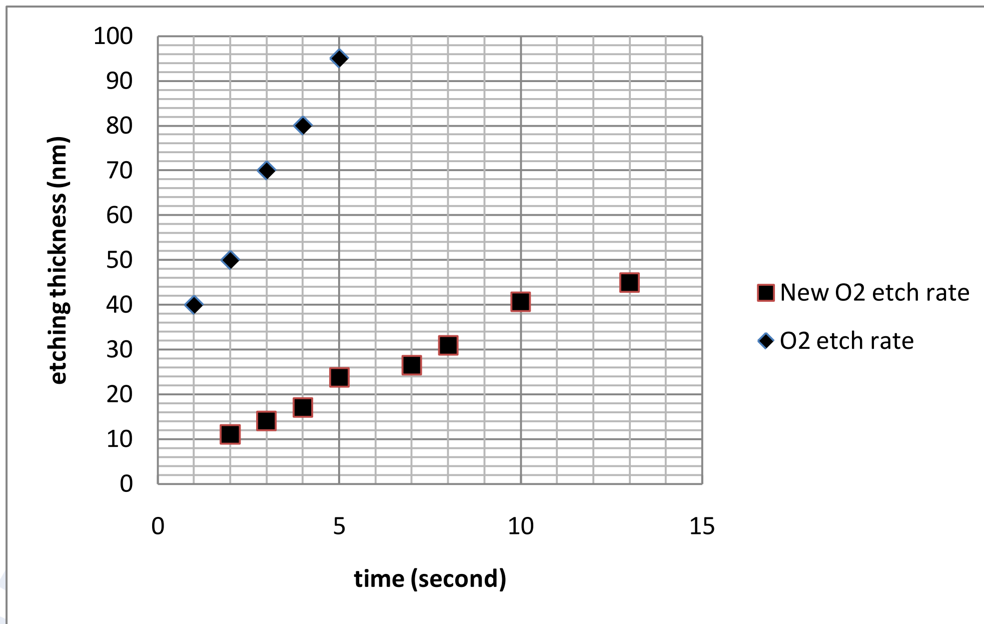


Figure 2. 8: The etching rate of PMMA with two different dry etch conditions. The first etching carries out a high etching rate. (The etching rate is calculated from the different thickness of resist during etching and measured by ellipsometery.)

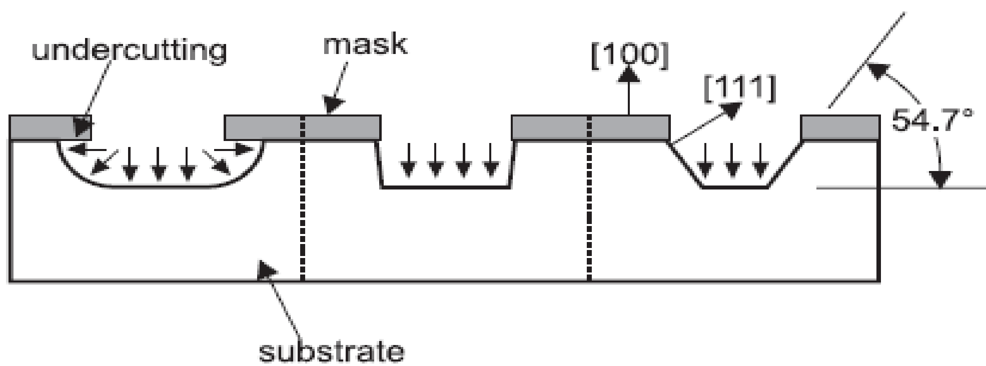


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Figure 2. 9: Overview of (left) isotropic and (middle, right) anisotropic etching. Anisotropic etching by (middle) dry etching or by (right) wet anisotropic etching [2-3].

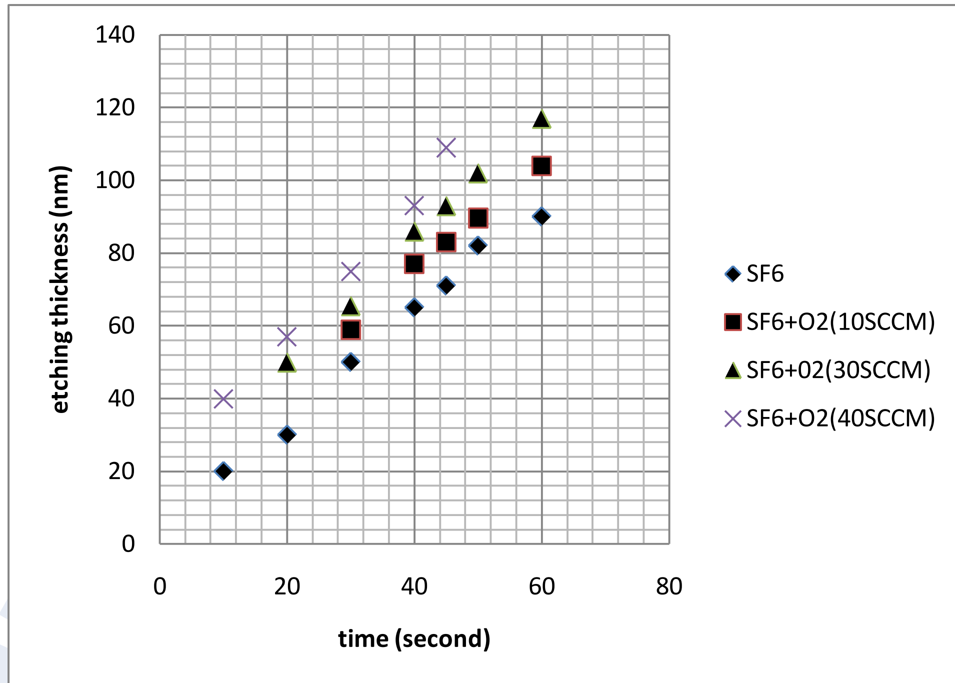


Figure 2. 10: The etching rate of PMMA with four different SF_6 and O_2 mixture. Etching rate of resist increases when the oxygen content increases.

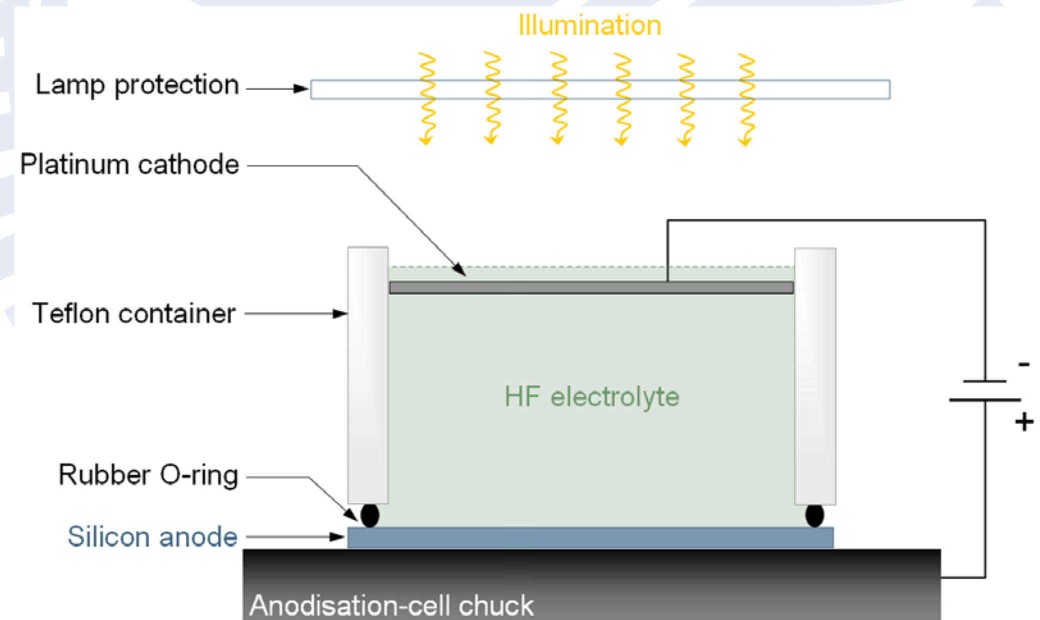
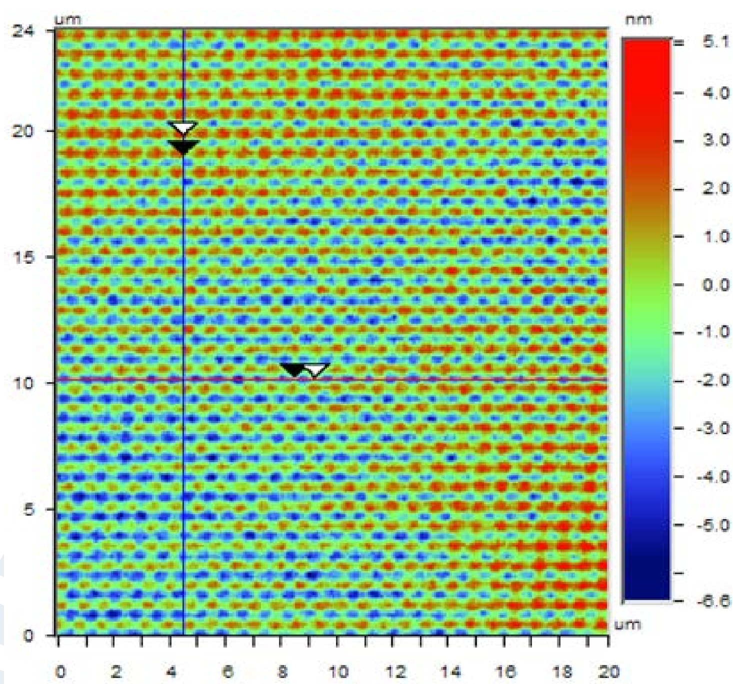


Figure 2. 11: Schematic illustration of an open O-ring anodisation cell. The lamp is a 50-W tungsten-bulb halogen lamp, and the lamp protection is a quartz-glass beaker that protects the lamp from HF vapors [1-7].



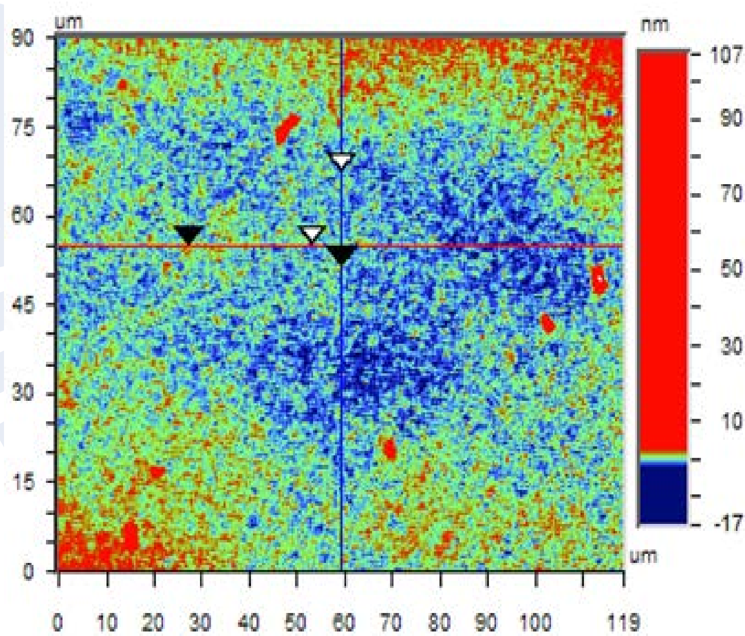


Figure 2. 12: Left is the result of hard mask from optical profilometer, and we can see a low resolution result. Right is the result of soft stamp from optical profilometer, and we cannot clearly see structures on the surface.

Chapter 3: Results and discussion

Experimental results are presented and discussed sequentially following the progress of soft-NIL, such as fabricating a suitable soft stamp, proper imprint conditions, and an accurate pattern transfer. In this chapter, explanations of material properties in terms of adhesion characteristic, deformation model, and viscous flow of polymer will be discussed, too.

In our experiments, we use two different kind of hard masks, which were presented in 2.1.1, and we will introduce the soft-NIL application of the first hard mask that has deeper pores in 3.1. In the following, the results of another hard mask, which has shallow pores, will be discussed in 3.2. We also investigate the suitable pattern transfer with specific dry etch conditions that lead to sidewall passivation, to duplicate the mask structure. This dry-etch steps is combined with an anodization process to fabricate deeper structures for achieving the aspect ratio requirements of the epi-free method. In the end, a better control of suitable aspect ratio for these pores is realized by an extra silicon oxide deposition which acts as hard mask instead of single resist to etch silicon.

3.1 Imprint from hard mask composed of deep pores

The first set of hard mask is composed of 440 nm diameter and 700 nm deep pores, and we fabricate a soft stamp to imprint structures with an anti-stick FDTS coating as shown in 3.1.1. In 3.1.2, we intentionally do the same process as above but without FDTS coating, and test different mix ratios of PDMS for imprinting in 3.1.3. In the end (3.1.4), we discuss a model of three different soft-stamp deformation modes including buckling, lateral collapse, and roof collapse to calculate an ideal hard mask more suitable for our process.

3.1.1 Process with coating anti stick layer

After fabricating the soft stamp from the mould of silicon with FDTS-coating, we imprint the stamp into 95-nm-thick resist. Figure 3.1 shows an AFM image of the stamp before imprinting, and the depth profile of the features. From the depth profile, the height of the pillar is 400 nm, and the height of soft stamp is lower than the hard mask probably comes from the limitations of AFM. We observe the surface of the soft stamp has a line defect before imprinting, and this is not a coincidence because it is visible on every sample. This suggests the flow of PDMS is not in an even dispersion and it probably comes from the fact that PDMS flow is limited when the mold has too deep pores. Figure 3.2 shows an AFM image of the soft stamp after imprint, with, on average, 800 nm pitch and 500 nm depth along line 1. Note that after imprinting, we cannot observe individual pillars but pillars collapsed against each other.

Figure 3.3 and Figure 3.4 show AFM and SEM images of the imprinted resist. In AFM image, there are 350 nm depth holes, and each hole is formed as elliptical shape instead of round shape. Measured from the depth profile, the depth of the patterns is around 500 nm. SEM images from top view show these structures have 750 nm pitch and 700 nm diameter, and confirm that etch pillar is closely attached to the adjacent one. Compared to Figure 3.3, the depth profile of AFM is matched to the SEM measurements.

From the results above, we can confirm that the stamp features are deformed upon imprinting, and we can suppose that the main problem is that the aspect ratio of the stamp is too high, and we will explore what are the limitations of the hard mask by applying mechanical models in 3.1.4.

3.1.2 Process without coating anti stick layer

For fabricating of a low aspect ratio structure, we intentionally not coat FDTS on the hard mask when the soft stamp is fabricated, to avoid PDMS getting deep into the pores. Therefore, soft stamps with decreased pillars' height can be fabricated, and these short pillars have a better mechanical property avoid bending when imprinting. Figure 3.5 shows atomic force microscopy (AFM) images of the stamp made from the hard mask. Measuring the stamp features, pillars have 500 nm diameter and only 50 nm depth.

In Figure 3.6, the AFM image shows the patterns of resist which is 95-nm-thick on silicon after imprinting. Holes having 500 nm diameter and 50 nm depth were obtained from the depth profile, showing a good correspondence with the soft stamp. In figure 3.7, images obtained from high-resolution microscopy reveal a bad uniformity of this sample. This likely comes from resist adhered to the stamp when imprinting without FDTS coating.

Since PDMS is an elastomer with a low Young's modulus, a limited pressure can introduce a large deformation of the imprinted areas. However, such a low toughness PDMS stamp cannot guarantee an overall mechanical stability of high-resolution patterns. For this material, a higher Young's modulus can be obtained by using a higher curing temperature or a higher ratio of PDMS mixture [3-1, 3-2]. In this experiment, we tested different ratios of mixture (1:5 and 1:15) to improve the uniformity. In Figure 3.8, the Topography of 3-D image shows the patterns which imprinted by soft stamp composed of 1:5, 1:15 and 1:10 mixture ratio. Higher or lower ratios of PDMS mixture lead to degrading of other mechanic properties of the stamps, such as fragility and overall toughness. Therefore, the optimal mixture ratio is 1:10.

Comparing the different results between with and without anti-stick layer, we observe that regular pores only exist in without-coating results. Regular pores will be better for the subsequent pattern transfer. However, we need to concern its bad uniformity and the low resist contrast, which is not sufficient for etching. Therefore, we discuss a model of three different soft-stamp deformation modes including buckling, lateral collapse, and roof collapse to calculate an ideal hard mask more suitable for our process.

3.1.3 Modeling the imprint Deformations

As pointed out by Delamarche et al. [3-3], one obvious limitation of imprint approaches results from the material properties typical for an elastomer. The PDMS has a low Young's modulus of ~ 1 MPa, but this low modulus poses limitations to the obtainable stamp feature sizes. Thus, the mechanical characteristics of the imprint

process are critical to the replication of features and the generation of patterns with high fidelity. There are two main methods to avoid deformation when imprinting.

The first method is mentioned by Schmid et al. [3-4] who use composite stamps of PDMS. They formulate a polymeric composite based on vinyl and hydrosilane end-linked polymers herein referred to as hard-PDMS, which has a high Young's modulus (~9 Mpa). Their design uses a multilayer stamp including a thin layer of hard-PDMS on a slab of 184-PDMS, which is the same as in our experiment. They combine advantages of soft stamps with hard stamps, and extend the capabilities of soft lithography to sub-100-nm features. A disadvantage of using this multilayer stamp is the complicated preparation of the hard-PDMS layer, which requires three steps rather than one. The difficulty in cleaning the surface of the stamp is also a problem because the hard-PDMS layer cracks easily.

Another method is to design an appropriate structure preventing stamp deformation, as mentioned in [3-5]. With an optimal design of hard mask, the fabricated soft stamp will have a better mechanical property to prevent deforming. Here, we consider the stamp with the features of Figure 3.9, where 2a, 2w, and h are the dimensions of the features' width, spacing, and height, respectively. There are three undesirable consequences of stamp deformation: 1) buckling 2) lateral collapse and 3) roof collapse, and the geometry of these three failure modes is drawn in Figure 3.10.

The mechanism of deformation is mentioned in detail by Hui et al [3-6]. To prevent the three failure modes mentioned above, the stamp conditions must satisfy the following conditions:

$$\frac{-1.47\sigma_{\infty}h^2}{\pi^2 E^* a^2} < \frac{1}{1+(w/a)} \qquad \{k\}$$

(Buckling)

$$\frac{h}{2a}\left[\frac{4\gamma_s}{3E^* a}\right]^{1/4} < \sqrt{w/a} \qquad \{l\}$$

(Lateral collapse)

$$\frac{-4\sigma_{\infty}W}{\pi E^{*}h}\left(1+\frac{a}{w}\right)\cosh^{-1}\left[\sec\left(\frac{w\pi}{2(w+a)}\right)\right]<1 \qquad \{m\}$$

(Roof collapse)

Here, σ_{∞} is the uniform stress applied to the top of the stamp and $E^{*} = E/(1-v^{2})$ is the plane strain of the stamp material, where E is the Young's modulus and v is the Poisson's ratio. In the case of PDMS, the Poisson ratio is around 0.5, for incompressive elastomers, and the Young's modulus is about 1 MPa [3-7]. The Young's modulus of PDMS depends on the mix ratio and the thickness of sample. For our soft stamp, the value of 1 Mpa is more suitable according to the experimental process. The surface energy of the material (γ_s), and it can be calculated by measuring the detachment length of a fixed-end cantilever beam. According to [3-8], PDMS has a γ_s of 0.3 N/m.

Regarding buckling, it mainly results from a high aspect ratio (h/2a). Pillars can collapse when loaded or even under their own weight. When the inequality in equation {k} is not satisfied, it will cause this kind of deformation. Concerning lateral collapse, when the applied forces are sufficiently large to bend the pillars, the pillars might make contact between each other. Once contact occurs, pillars may adhere to each other due to surface adhesive forces. Therefore, lateral collapse of neighboring pillars will happen. To establish a criterion for lateral stability, inequality in equation {l} is considered. Regarding roof collapse, it results from low aspect ratio which causes insufficient relief exists on the surface, and the stamp has to withstand this compressive force. To avoid the roof collapse, the conditions should satisfy formula {m}.

In the case of the first hard mask, both conditions of buckling and lateral collapse are not satisfied. From the above formulas, the depth of pore should be below 400 nm for the desired diameter of 450 nm. Therefore, we fabricate a new hard mask which has a lower aspect ratio avoiding these three deformation problems. The results of this new hard mask's application will be shown in the next section.

3.2 Imprint from hard mask composed of shallow pore

After considering the deformation problems mentioned above, a hard mask composed of 460 nm diameter and 230 nm depth is applied to soft-NIL. A soft stamp is fabricated from this new hard mask, and Figure 3.11 shows the results of AFM as well as its depth profile. By comparing the soft stamp to the hard mask (Right image of Figure 2.3), we can confirm that the stamp is perfectly duplicated. Besides, in this series of experiment, all patterns are FDTS-coated, because it will improve the quality of imprinted structures. Without FDTS, the structures will have a non-uniform surface.

3.2.1 The performance of different thickness of resist

The thickness of resist is an important factor which influences the performance of imprint structure. Ideally, we want to completely duplicate the structures into the resist from the stamp, and to obtain a maximum thickness contrast providing a thicker sacrificial resist layer consumed during the subsequent dry-etch process. Therefore, we tested different thicknesses of resist imprinted by the same stamp, and observed the differences in pore diameter and depth from AFM.

Figure 3.12 shows the AFM measurement of imprinted structures in 95-nm-thick resist, as well as the extracted profile. In this case, the imprinted structure has a depth of 150 nm, a diameter of 450 nm, and a pitch of 800 nm. Compared to the original hard mask, the thickness contrast is lower. Imprint structures of 120-nm-thick resist are shown in Figure 3.13 from AFM results. The thickness contrast obtained under this condition is 180 nm and the circle size is equal to that of the hard mask. When we use 160-nm-thick resist, results successfully lead to a structure nearly identical to the hard mask. AFM image shows structures with 230 nm depth, and 460 nm diameter (Figure 3.14).

These results clearly demonstrate the fidelity of imprint structures obtained by applying a different thickness of resist, and that this thickness change only affects the thickness contrast and not the size of the circles. In addition, the soft stamp is reusable and reliable. In our test, the soft stamp could be used more than ten times, with similar results for the different experiments.

From the above results, we can learn that a different thickness contrast can be obtained from different thicknesses of resist. In addition, there is a simple calculation regarding to the connections between filling percentage and thickness contrast. For given diameter, pitch and height of the soft stamp (Figure 3.15), we can calculate the cavity coverage of the soft stamp as shown in equation {l}, considering different thicknesses of resist. The filling percentage can be obtained from the above information as shown in equation {m}. In this case, the soft stamp has a cavity coverage of 0.75 and 230-nm height pillars. Imprints were done into substrates with film thickness of 95, 120, and 160 nm corresponding roughly to the three situations of 60 %, 75%, and 100% filling, respectively.

$$\text{Cavity coverrage} = \frac{\pi \times (\text{diameter})^2}{(\text{pitch})^2} \qquad \{l\}$$

$$\text{Filling percentage} = \frac{\text{Resist thickness}}{\text{Cavity coverage} \times \text{Height}} \qquad \{m\}$$

We can conclude that if the imprint is used for lithographic purposes, the situation where the initial resist thickness corresponds to a 100% filling situation could be an advantage. However, thickness contrast is not the only issue of NIL, and there are other concerns, which will be discussed in next section.

3.2.2 Optimizations of the soft-NIL process

Optimization of the soft-NIL process consists of fabricating a high thickness contrast, a uniform surface and the thinnest possible residual layer.

Before discussing these optimizations, the discussion of the pattern formations presented by Schift et al. is presented [3-9]. There are different pattern formation mechanisms like self-assembly and explosive expansion of air, and intended fine filling of the stamp cavities is discussed here. The filling mechanism of a stamp cavity is shown schematically in Figure 3.16. The polymer is squeezed under the protruding features of the stamp when imprinting, and this squeeze flow starts to fill all cavities. Here it can be seen that the capillary effects, causing the polymer to flow up the

cavity walls. The flow will be restricted when the polymer reaches the bottom of the cavity and then start to fill the cavity.

Ideally, the polymer melt flows into the cavity until it is fully filled, as it can be seen in the depth profiles of Figure 3.14. However, in Figures 3.12 and 3.13, it can be seen that the polymer flows up the cavity walls from the boundary, but the protrusions along the wall are apparent. We conclude that a sufficient amount of polymer melt can reach a better uniformity, and the squeeze flow will lead to imperfect patterns when the resist is not sufficient (< 100% filling) to fill the whole cavity.

Another advantage of 100% filling is that it is the best way to keep a good uniformity in terms of area. When the initial thickness is too high (> 100% filling) it will cause a bad uniformity over the sample. Images of high-resolution microscope in Figure 3.17(a) can prove that the uniformity is bad when we apply a very thick resist of 250 nm. In this high filling condition, resist not only fills all cavities, but the extra resist remains on certain areas, creating non-uniformities. This extra coverage results in the appearance of artifacts as shown in Figure 3.17(a). The result of 160 nm and 95 nm resist are shown in Figure 3.17 (b) and (c). In combination with the results from the previous section, it is clearly that the application of 160 nm resist shows the best result.

Furthermore, Scheer et al. have looked into the polymer flow by looking at imprints done with a stamp containing both negative and positive pattern [3-10]. Scheer et al. conclude that inadequate material transport and varying polymer flow distances are the reasons for unsuccessfully and inhomogeneous imprints. When large differences in pattern size or pattern group size have to be imprinted, the material transport inherent to this technique will limit the imprint quality. Another research mentions that the polymer flows faster in the high-density area. Therefore, a different polymer flow occurs despite the uniform pressure applied on the backside of the stamp. This difference induces a non-uniform residual thickness between areas of different densities [3-11]. Therefore, small and periodical patterns are replicated most easily. In our experiment, this inherent advantage comes out, because of the simple periodical pore pattern presented in our structures.

Besides the uniform patterns discussed above, a thin residual layer is also a critical factor in NIL. Cavity filling is primarily responsible for the residual layer height obtainable in an imprint process. When suitable cavity filling is applied by adjusting the initial polymer layer height, the final residual layer height only depends on the imprint time. With the optimal of cavity filling, thin and uniform residual layers are achieved [3-12]. As expected by these cavity-filling arguments, the residual layer thickness should be directly proportional to the initial film thickness [3-14]. For our application, although a minimum residual layer can be achieved with a thin resist, it will result in a low thickness contrast. In our experiment, we achieved a highest thickness contrast and a very thin residual layer from a suitable soft stamp and resist thickness, and this thin residual layer provide us a good control of pattern transfer. In Figure 3.18 are shown SEM images of imprint structures in 160 nm thickness of resist. There is a uniform topography, and a very thin and uniform residual layer. This layer is too thin to be accurately measured by SEM, but an upper limit of 20 nm can be given.

3.3 The results of Pattern transfer

The concept of pattern transfer is using the imprinted structures as the mask for the subsequent dry-etching process. We furthermore combine a dry-etching process with an anodization technique to fabricate deeper pores.

3.3.1 Etching silicon without sidewall passivation

Isotropic etching is etching the material without sidewall passivation, and this mechanism may be not suitable for providing deep pores. However, it is likely we can observe some basic results in the first test. In this section, all samples are composed of 500 nm diameter and 50 nm resist contrast (Figure 3.6), which is fabricated from deep-pores hard mask without FDTS coating.

The first experiment does not involve removal of the residual layer by O_2 plasma, and we use one-step of SF_6 plasma to transfer patterns. Figure 3.19 presents the results of different etching times under this condition (described in Section 2.3.1). The area of the structures becomes larger with increased etching time. Since the silicon window is not open when SF_6 etch the silicon, there are many un-patterned areas on the sample. Therefore, in the next experiment, the samples are first etched by a high etching rate of O_2 plasma in one second (described in Section 2.3.1), and then the silicon etched by SF_6 in 10 to 30 seconds as shown in Figure 3.20. It is found that the silicon etching is more effective after this residual layer etch than previously. Besides, SEM image shown in Figure 3.21 shows the sample etched in 30 seconds. The isotropic etching clearly results in the square, and the reaction of isotropic etching with silicon is the main factor responsible for this. From the right image in Figure 3.21, the large various heights of structures come from the bad uniformity of the imprinted structures.

We conclude that the removal of residual layer plays an important role in pattern transfer uniformity, and an inappropriate SF_6 etching leads to a small area of structures. Besides, the uniformity of the imprinted-resist pattern directly affects the performance of pattern transfer.

3.3.2 Optimization of the residual layer removed by O_2 plasma

Before performing the anisotropic etching, we test the accurate conditions of O_2 plasma to remove the residual layers. Figure 3.22 shows three samples patterned with three different etching times at a low etching rate of O_2 plasma (described in Section 2.3.1), indicating that 5 seconds is the most appropriate in our experiment. The blur patterns visible in the 3-second etching time and 8-second etching time result in a smaller resist contrast proven by the depth profile in AFM measurement, and therefore in a thinner resist to be consumed for silicon etching.

Based on the above results, all samples are etched by the low etch-rate O_2 plasma in 5 seconds prior to the silicon etching in the following dry-etching experiments.

3.3.3 Etching Silicon with sidewall passivation

Silicon etching with sidewall passivation is required for the desired high aspect ratios, and we use an anisotropic etching by SF_6 and O_2 to perform this process. All experiments carried out in this section are composed of 460-nm-diameter pores and 230-nm-resist contrast (Figure 3.14), which is imprinted from the soft stamps composed of shallow pillars (220 nm) with FDTS coating.

The sample etched with SF_6 with 10% O_2 for 40 second is shown in the Figure 3.23. The effect of adding O_2 is not apparent, because the lateral etching is still large. There is also creation of silicon oxide, which looks like white whiskers, on the corners of the mesh, and it points out that the O_2 concentration is not high enough to form a steady and sufficient passivation layer when performing the etching. In Figure 3.24, the etching time increases to 60 second, and the edges start to contact each other, resulting in the disappearance of the structures, because of the insufficient sidewall passivation.

An effective anisotropic etching can be controlled by a proper concentration of O_2 addition to the plasma. An increase of the O_2 content in plasma enhances the sidewall passivation and therefore reduces lateral etching [3-14]. Figure 3.25 shows the results of different O_2 concentrations. The lateral etching can be significantly reduced with higher oxygen concentration. However, the silicon surface is more oxidized from the high oxygen content, which strongly reduces the etch rates of silicon. The high oxygen concentration also causes an increase in the etching rate of resist, and therefore to an undesirable faster disappearance of the etch mask.

These initial results are satisfactory, confirming that the higher oxygen concentration leads to a better sidewall passivation. In a next step, we tested a longer etching time to obtain deeper pores. Figure 3.26 shows the results of different etching times with the same O_2 concentration. The pores depth increase when the etching time increases, but the diameter of pores also increases. It is likely that the reaction start to etch the edges of the mask. We only reached aspect ratio around 0.7 in this test.

Therefore, the limitation of aspect ratio now appears. It has not been possible to reach higher aspect ratio only by adjusting the oxygen flow.

3.3.4 Influence of different dry-etch parameters

In the mechanism of silicon dry-etching, pressure and power also play an important role. In the next experiment, silicon substrates are etched in SF_6 plasma at different pressures and energies of incident ions. The increased pressure increases the probability of SF_6 molecules to get in contact with the target material, and higher power increases the probability of dissociation of the SF_6 molecules [3-15]. The etching rate of silicon increases with the increase of pressure in the reactor and power. Therefore, it is possible to reach higher aspect ratios. However, problems occur with the increase of power and pressure. In Figure 3.27, samples are etched in a 150 W power and 150 mTorr pressure with different O_2 concentration. The sizes of each pore strongly vary. This phenomenon comes from an uneven electron density distribution in the reactor and the resulting uneven species concentration across the electrode leads to a poor uniformity of the etch process. The high power worsens this phenomenon. Besides, the etching rate of resist tremendously increases when the power increases, because the polymer mask is easier consumed. The sample in Figure 3.28 was etched at a pressure of 200 mTorr and power of 100 W. Although the etching rate increased, the lateral etching rate also increase, which results from the increase of mask consumption. Therefore, the undefined edges appear.

From another point of view, etching silicon at a slow rate with good sidewall passivation instead of seeking a high etching rate without proper sidewall passivation may be a better approach to obtain deeper pores. It is well known that lower power decreases the ion energy. Therefore, a decrease of bias voltage reduces the etching rate, including the lateral etching rate, and is hence a possible way to reach our requirements [3-16]. The pores with a depth of 450 nm and a diameter of 450 nm in the condition of low power are shown in Figure 3.29. We can reach aspect ratio of 1 in the low power condition, but this might be the limitation of SF_6-based dry etching. The ion bombardment is too low when the power decreases, and it will cause a low

silicon-etching rate. In addition, the resist mask thickness is not enough and is consumed at an early stage.

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3.3.5 Fabricate inverted pyramid pre-patterned structures by dry etching

Due to the infeasibility of fabricating deep pores merely by SF_6-based dry etching with a PMMA resist, a combination between dry etching and electrochemical etching, anodization, is a possible method to fabricate deeper pores. In fact, anodization of a properly pre-patterned silicon wafer can form regular pores. In particular, inverted pyramid pre-pattern structures are optimal to be anodized uniform pores. Based on this thought, we take advantage on a negative effect occurring in some dry etching processes that result in slopped sidewalls. Slopped sidewalls are caused by the angular dispersion of ions due to the collisions within the sheath ion interactions and the sidewalls. The etching rate depends on the angle of ion incidence. Therefore, extra lateral etching along the higher part of the sidewall occurs. Besides, the resist erosion that results from the ion bombardment of the surface enhances this mechanism. Therefore, adding high concentration of O_2 to the SF_6 based dry-etch with a long etching time. The collisions are enhanced by a long etching time, and a high concentration of O_2 increases the resist erosions. A slopped profile resulting from a varying etching rate along the sidewall is shown in Figure 3.3. The resulting sharp pore tip should lead to a better control of anodization.

3.3.6 Anodization process

Anodization of pre-patterned structures is performed for fabricating deeper pores. In a first set of experiments, the non-optimal pre-patterned structures were used. These samples (etched in 40% O_2 for 20 seconds (Figure 3.25 (c))) were anodized with a current density of 8 mA/cm^2 for 300 seconds shown in Figure 3.31. The difference between pre-patterned and bare silicon is obvious and shown in Figure 3.31 (a). However, the pre-patterned pores present some defects. First, pores become branched at high-current density, and this degeneration in the horizontal direction results in not much difference in pore cross section with the un-patterned area (comparing between Figure 3.31 (b) and (c)). A point worth noting is that the

branches only exist at high current density. In fact, for anodized samples with high current density, more electronic holes are offered at the sample surface to be consumed at the tip. The holes start to penetrate into the walls between the pores and promote dissolution by HF there. If the hole current is increased further, the wall thickness eventually becomes zero and the branches get worse [3.17].

The same sample is anodized with a lower current density of 4 mA/cm^2 for 240 seconds and shown in Figure 3.32. The sample has regular structures, and the diameter is only slightly dependent on the artificial variations of current density (shown in Figure 3.32 (b)). Besides, the difference between pre-patterned and bare silicon is clearer (comparing between Figure 3.32 (b) and (c)), because we obtain more uniform pores in diameter, length and pitch in pre-patterned silicon. Interestingly, there is more than one sub-pore beneath one pre-patterned etch-pit in some areas (shown in Figure 3.32 (a), and this phenomenon might be accounted for the shape of etch-pits. The unsmooth bottoms of etch pits result in more than one preferential etching route. Therefore, good controls of pre-patterned samples are required for an optimized anodization process.

In order to define the starting position of etching exactly at the etch-pits' tips, inverted-pyramids have been formed on the front side of the samples as shown in Figure 3.30. The resulting structures shown in Figure 3.33 demonstrate that pre-patterning sample successfully provides ordered and deep pores (~8 μm). Next to branching and the presence of multiple pores per etch-pit, another defect is the non-uniformity of the pore's diameter in depth. A possible explanation for it is the irregular current density that is delivered to the sample by the generator, as can be seen in Figure 3.34. Therefore, to improve the electrical contact between the sample and the anodization cell, the backside doping of the sample was increased by performing phosphorus diffusion. The results of Figure 3.35 show an improved diameter uniformity in depth but a layer variation from pore to pore, sometimes even to the dying of small pores. Therefore, we cannot properly judge the pore size because the visible size is not necessarily the actual size from cross section. The dark dots in the circular etch-pits as shown in Figure 3.35, indicate deeper and larger pores, and it can be seen that the deep pores do not exist in every etch pit. The irregular current

feed is still observed in these samples, and the reason is still unknown. The large difference between pores resulting from it is not acdeptable for our application and future work have to improve the anodization conditions.

3.4 Suitable depth control of the Pattern transfer

Using silicon oxide as mask instead of single resist is a possible method for fabricating deeper pores, since the low etching rate of silicon oxide compared to the resist. In figure 3.36, the experimental flow of soft-NIL applied above silicon oxide is shown.

Before growing, suitable thickness of silicon oxide is chosen by each material's etching rate. If the silicon oxide still remains above the bottom after opening silicon window, the silicon etching cannot well perform. If the silicon oxide is too thin, the silicon cannot etch that deep. The etching selectivity of Si films and SiO_2 films at 550W powers and CF_4 gas flow rates and CHF_3 gas flow rates of 40 and 20 sccm, respectively with constant O_2 and Ar is 19.6. The etching selectivity of SiO_2 films and resist at 200W powers and HBr gas flow rates and Cl_2 gas flow rates of 30 and 40 sccm, respectively is over one. Therefore, 100 nm silicon oxide is enough to ensure etching 1.35 μm silicon, and 220 nm resist is also enough to open silicon window. The depth is calculated from the object of aspect ratio is three. The pattern transfer process is shown in Fig. 3.37.

3.4.1 Open silicon window

The imprinted structure above the silicon oxide is achieved by the same process as normal imprint. The left image of Figure 3.38 is shown SEM image of imprint structures in 160 nm thickness of resist above silicon oxide. There is a uniform topography over a large area. Besides, accurate conditions of O_2 plasma of removing the residual layers is performed, and the cross section after etching is shown in the right image of Fig. 3.38.

Etching of silicon oxide mainly depends on F density and ion bombardment. The process conditions for a high etch selectivity are a 40 sccm CF_4 and 20 sccm CHF_3 flow at a 550 W power with constant O_2 and Ar in our experiment. High power etching with adding CF_4 can improve the etching uniformity [3-20]. We test two different process times which are 40 and 60 seconds; then we remove the remaining silicon oxide by immersion in acetone of an ultrasonic bath for 10 min. In Fig 3.39 (b), we can see the structures shows better etching profile than another one which shown in Fig 3. 39 (a) is etched for shorter time. Besides, the bottom of the holes is smooth, and we can easily tell the color of light dark is silicon oxide. Nevertheless, the surface is not smooth in both samples, and it shows the acetone is not enough to remove the resist which is after ion bombardment.

3.4.2 Etch silicon into desired features

In the case of silicon etching, HBr mixed with Cl can enhance the etching profile due to the reduced spontaneous chemical reaction of HBr with silicon [3-21, 3-22]. We test two different etching times which are seven and night minutes, and the etching profiles are separately shown in figure 3.40. In Fig. 3.40 (b), the SEM image shows the silicon is etched over 1.2μm in the condition of night minutes. In addition, the silicon oxide should remain on the surface after the etching according to the etching tests before, so the etching time could be longer for obtaining deeper pores. However, a silk-like residue contained by silicon polymer is remaining on the surface after silicon etching. Therefore, proper clean process is necessary. Therefore, we will use of SPM (H_2SO_4+H_2O_2) cleaning to remove these organic materials after HF dip [3-23] in the following experiments.

In the Fig. 3.41 (a), the sample is etched by CF_4 with 4% O_2 for 60 seconds, and we clean the sample by SPM instead of only acetone immersion. We can see the surface is smoother than the results shown in Fig 3.40. For obtaining deeper holes of silicon, the sample is etched by HBr with Cl_2 and HBr with O_2 at a 220 W power and 160 W for 11 and 1 minute after opening silicon window. In the clean process, we use of SPM (H_2SO_4+H_2O_2) cleaning to remove the organic materials after HF dip. We have

the results in the Fig. 3.41 (b), and the aspect ratio of these holes is over three which meet our requirements. Besides, the surface is smooth without remaining polymers as shown in the Fig. 3.41 (c) which is the top view of this sample.

In the case of silicon etching, the selectivity between silicon oxide and silicon is lower than we test on purely bulk silicon. However, the holes etch profile shows a nearly vertical sidewall possibly due to the less spontaneous reactivity of the Br radical with silicon compared to the Cl radical on the sidewall. The defects on the bottom appear to the related to the penetration of hydrogen ions through the sheath voltage [3-24]. Moreover, we also process the same etching condition for 13 minutes in order to obtain deeper holes. The results show in Fig. 3.42, and the rough surface indicates the silicon is over etched. Therefore, if we want to have deeper pores, the thicker silicon oxide is a possible solution.

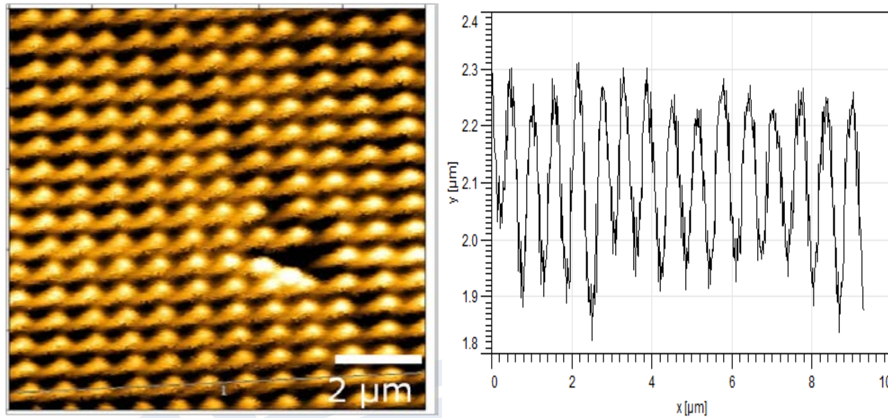


Figure 3.1: AFM image and depth profile of soft stamp before imprinting with anti-stick layer coating. On average, 400-nm height pillars along line 1.

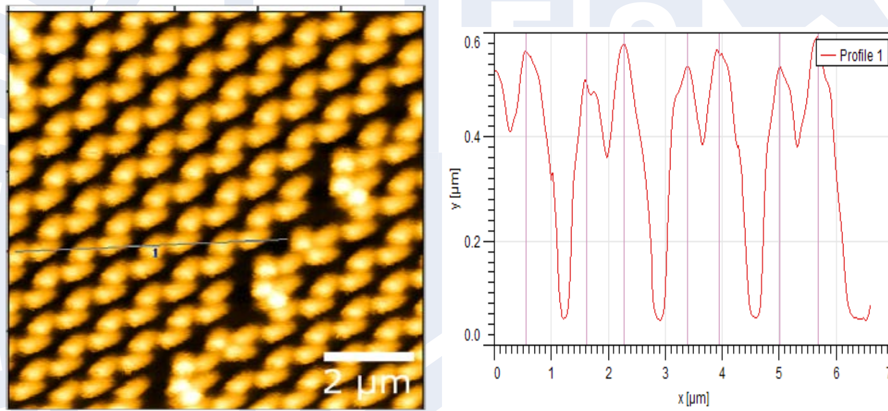


Figure 3.2: AFM image and depth profile of soft stamp after imprinting with anti-stick layer coating. On average, 800-nm pitch and 500-nm height pillars along line 1.

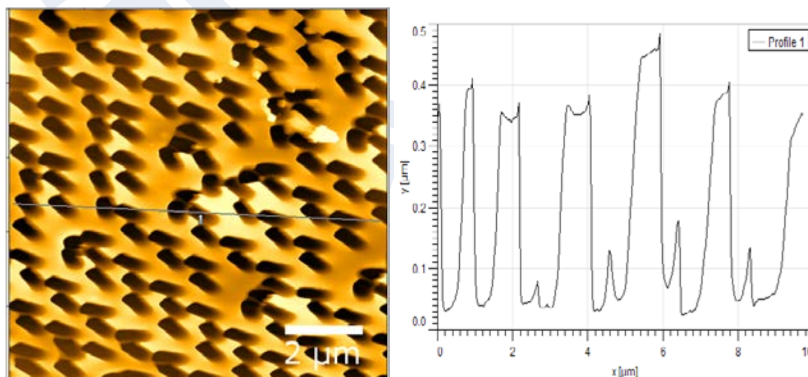


Figure 3.3: AFM image and depth profile of the soft stamp imprinted into 95-nm resist on silicon. On average, 800-nm pitch and 400-nm depth pores along line 1.

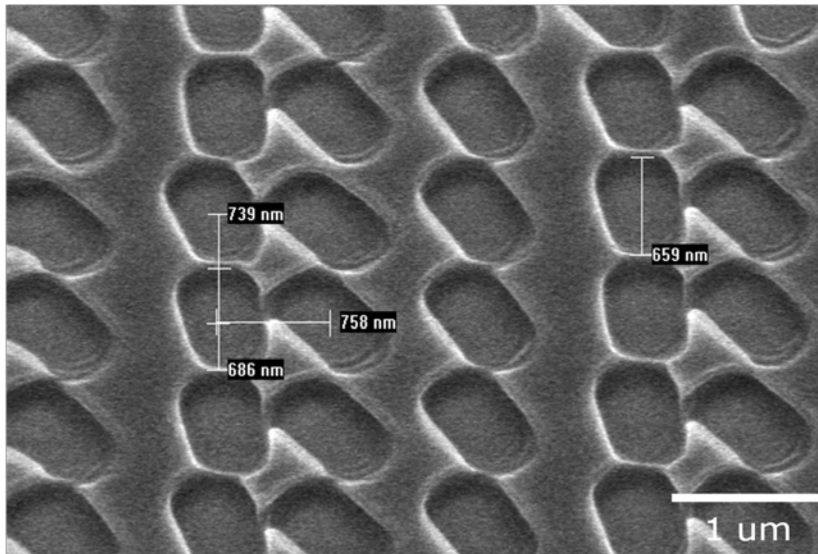


Figure 3.4: SEM image of the soft stamp imprinted into 95-nm-thick resist on silicon. Confirm that etch pillar is closely attached to the adjacent one.

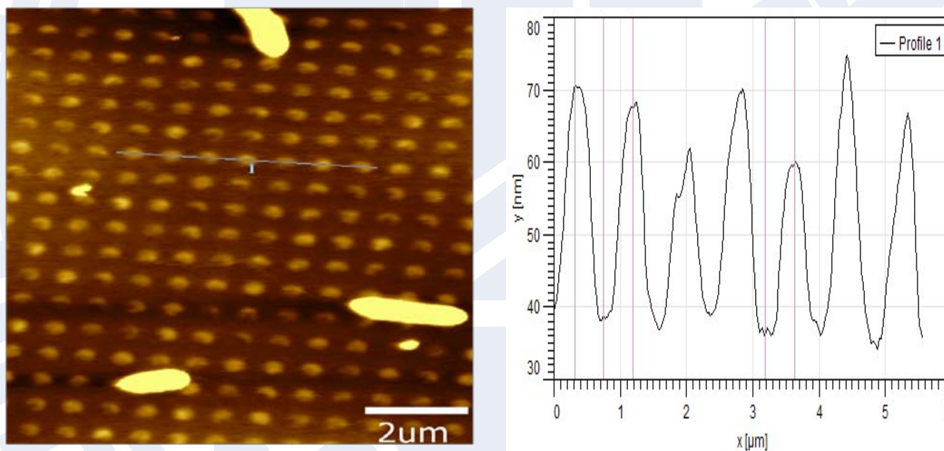


Figure 3.5: AFM image and depth profile of soft stamp after imprinting without anti-stick layer coating. On average, 500-nm diameter and 50-nm depth along line 1, and it shows that the pillars do not deform anymore. (The bright spots of the AFM image come from an artificial effect that indicates dirt on the surface of stamp. These particles probably originate from the operating environment.)

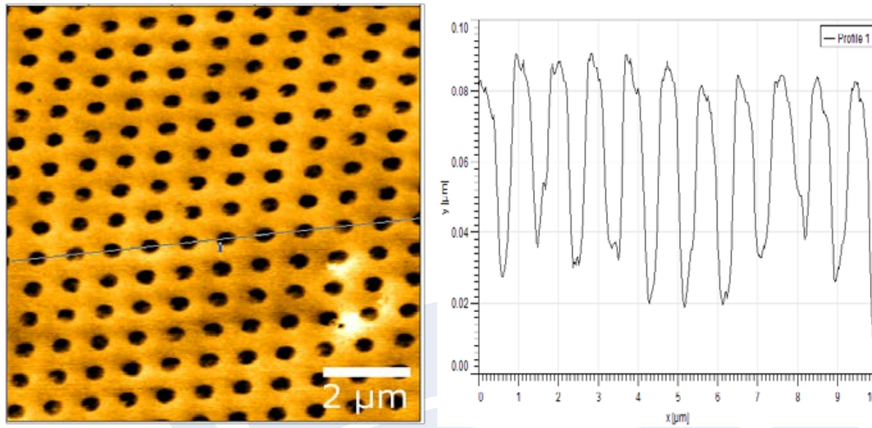


Figure 3.6: AFM image and depth profile of the soft stamp imprinted into 95-nm resist on silicon. On average, 500-nm diameter and 50-nm depth along line 1.

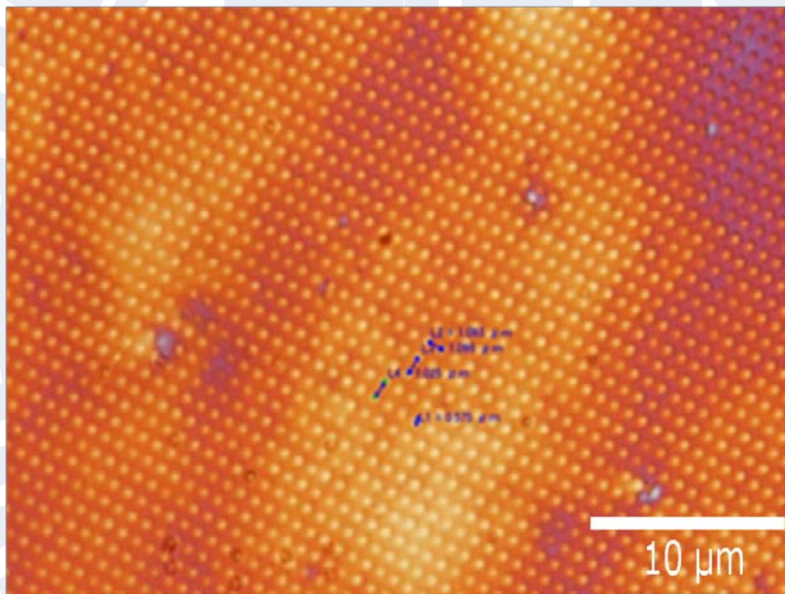


Figure 3.7: High-resolution Microscopy image of the soft stamp imprinted into 95-nm-thick resist on silicon, and it shows a bad uniformity of this sample.

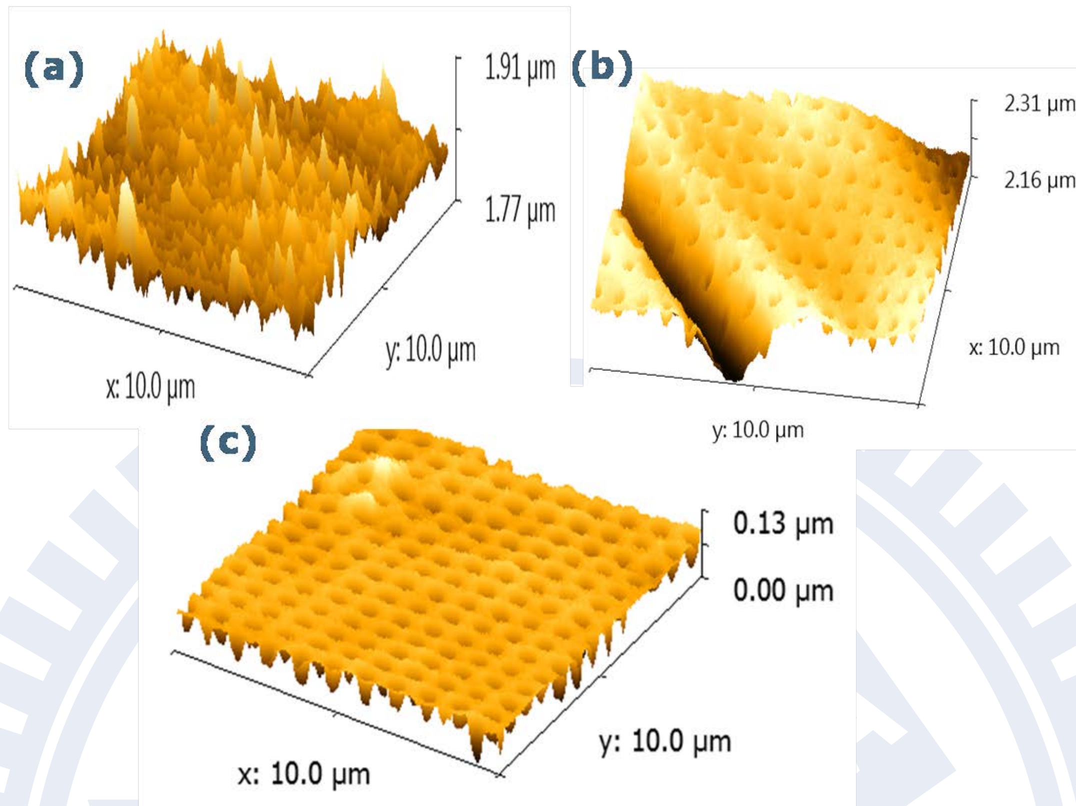


Figure 3.8: Topography of 3-D image shows the patterns imprinted with a soft stamp composed of (a) 1:5, (b) 1:15 and (c) 1:10 mixture ratio.

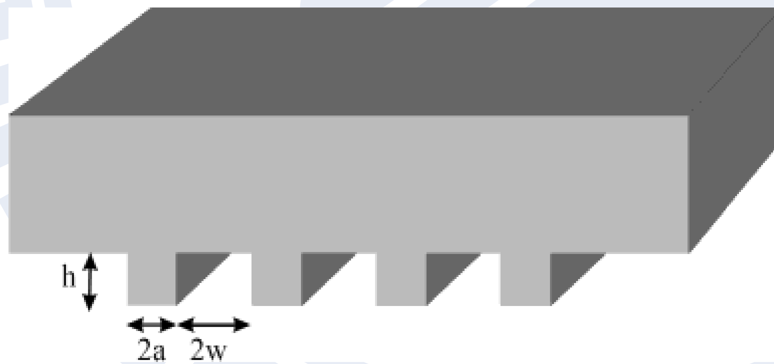


Figure 3.9: Schematic of stamp with width of 2a, height of h, and pitch of 2w [3-5].

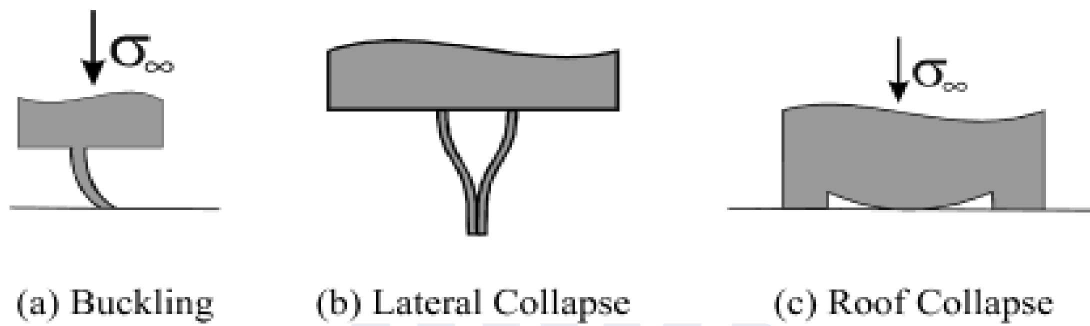


Figure 3.10: Three failure modes of stamp deformation. (a) buckling (b) lateral collapse (c) roof collapse [3-5].

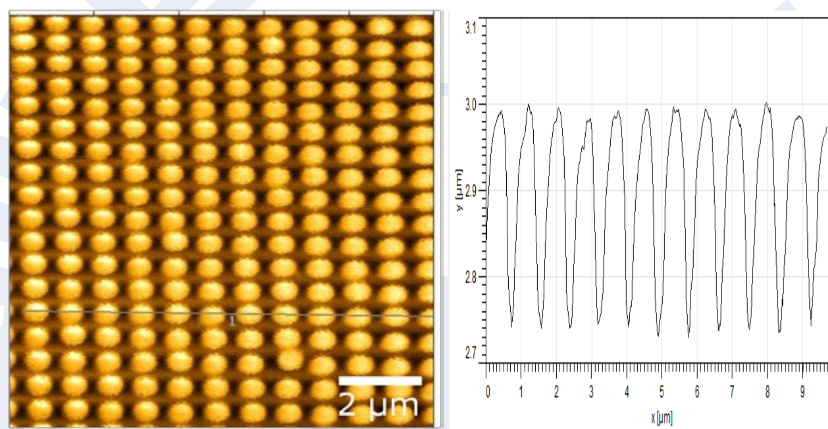


Figure 3.11: AFM image and depth profile of soft stamp composed of 500-nm diameter and 230-nm height pillars, and it shows that stamp is perfectly duplicated from the hard mask (Right image of Figure 2.3).

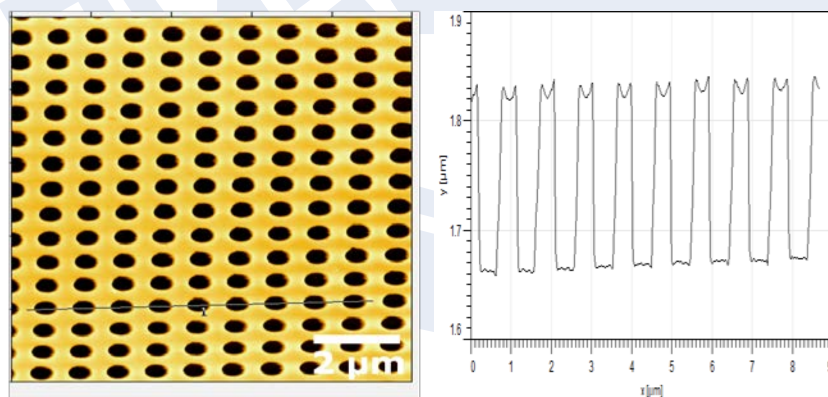


Figure 3.12: AFM image and depth profile of imprinted structures in 95-nm-thick resist, and the pores are composed of 450-nm diameter and 150-nm depth.

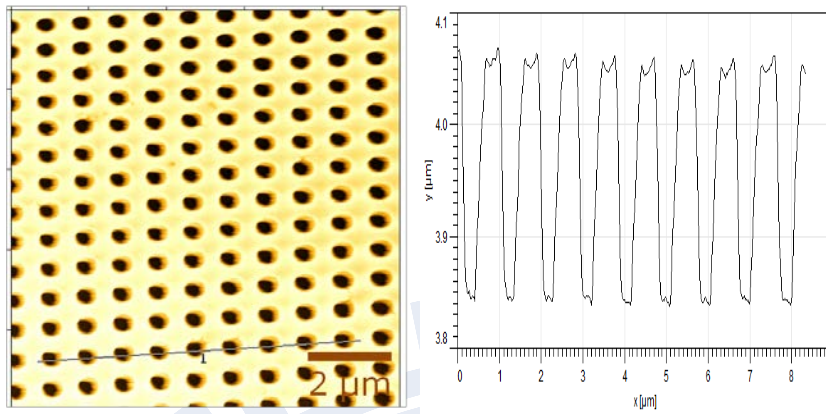


Figure 3.13: AFM image and depth profile of imprinted structures in 120-nm-thick resist, and the pores are composed of 450-nm diameter and 180-nm depth.

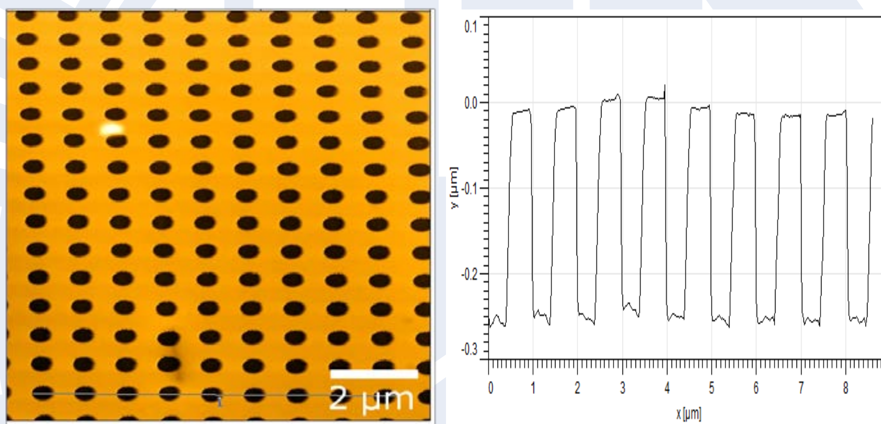


Figure 3.14: AFM image and depth profile of imprinted structures in 160-nm-thick resist, and the pores are composed of 460-nm diameter and 230-nm depth.

Figure 3.15: Schematic illustration of the soft stamp.

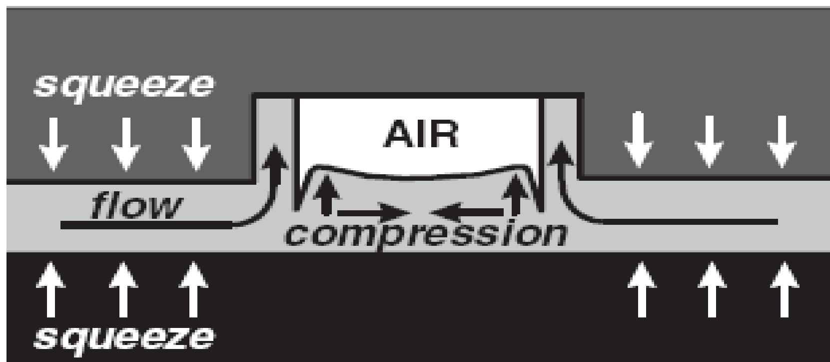


Figure 3.16: A schematic representation of squeeze flow of a polymer into a stamp cavity [3-9].

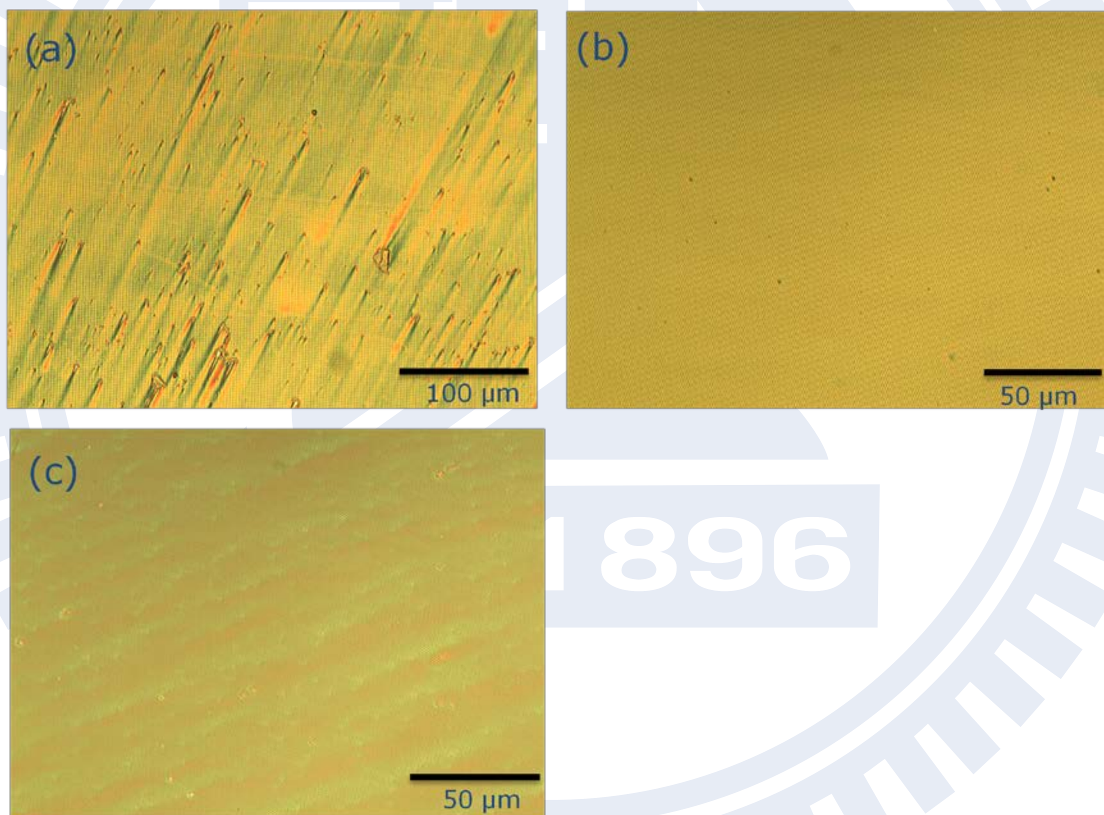


Figure 3.17: Optical microscope image of imprint structure in (a) 250 nm, (b) 160 nm and (c) 95 nm thickness of resist. The best uniformity is obtained in (b) with a 100% cavity fill.

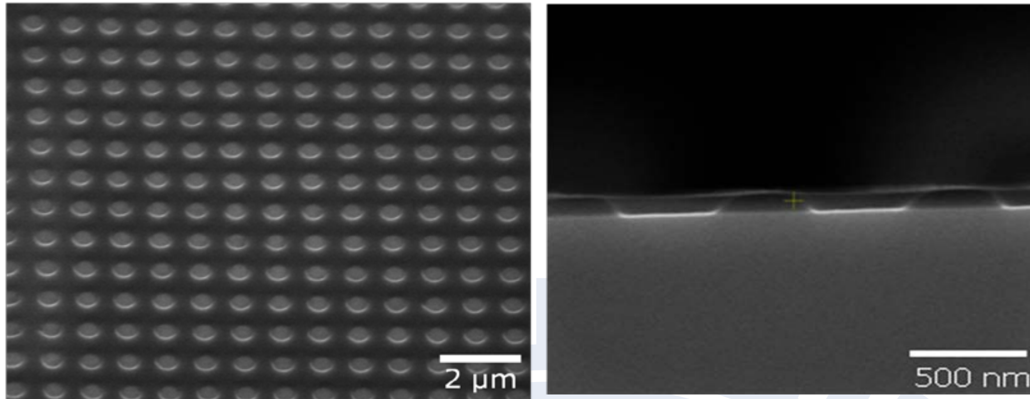


Figure 3.18: SEM images, from tilted top view and cross section, of an imprinted structure in 160-nm thickness of resist. There is a uniform topography (left) and a very thin residual layer (right).

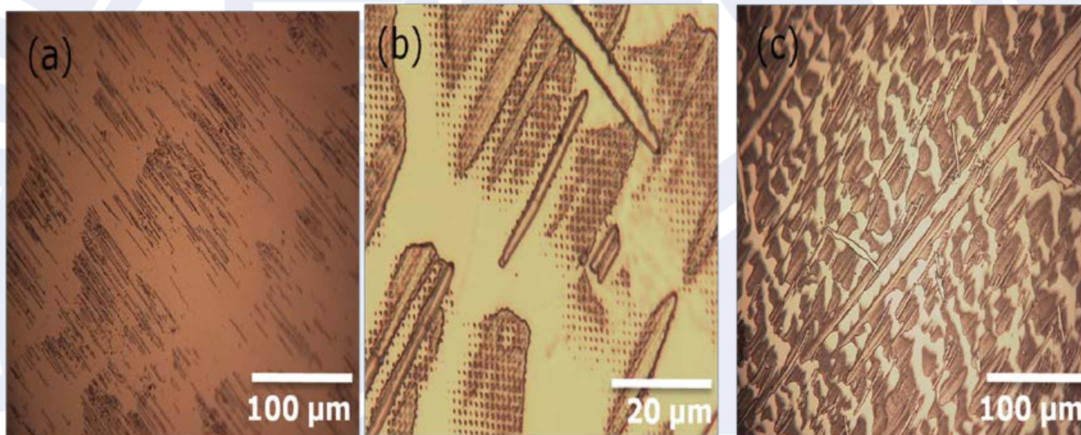


Figure 3.19: High-resolution microscopy images of imprinted silicon etched for (a) 10, (b) 30, and (c) 40 sec by SF_6. The area of the structures becomes larger with increased etching time.

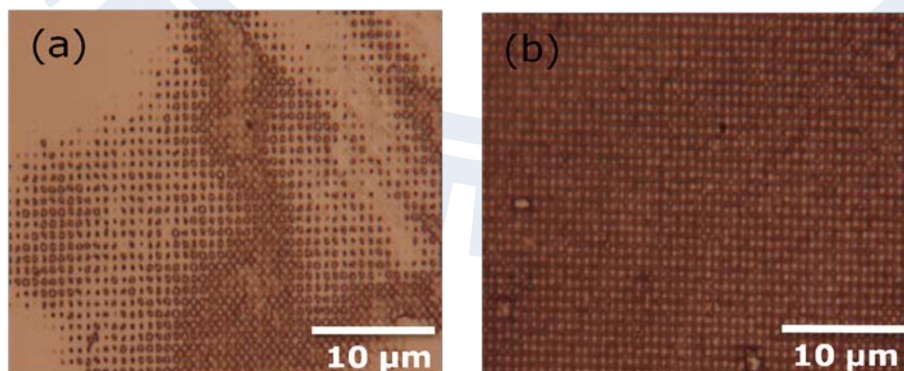


Figure 3.20: High-resolution microscopy images of imprinted silicon are first etched by a high etching rate of O_2 plasma in one second, and then the silicon etched by SF_6

for (a) 10 and (b) 30 seconds. Here, the silicon etching is more effective than without removing residual layer.

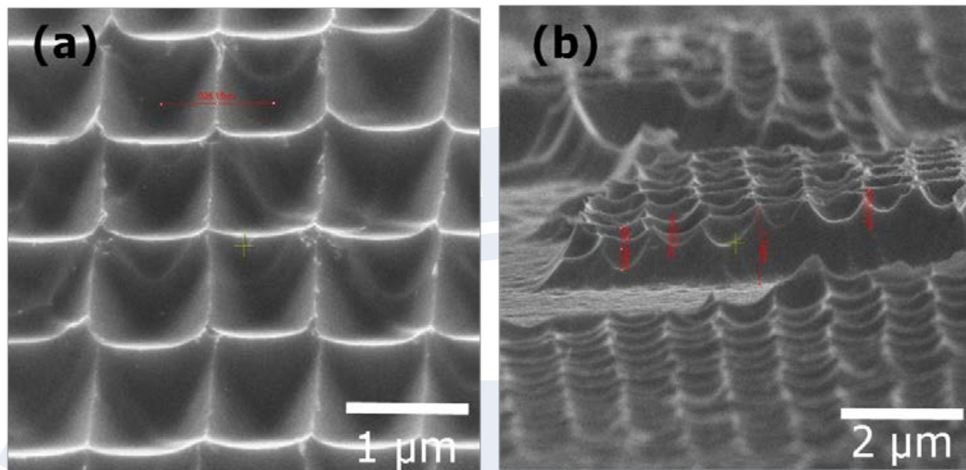


Figure 3.21: SEM images of samples etched by O_2 for 1 second and SF_6 30 for seconds. (a) The isotropic etching clearly results in the topography and (b) the large various heights of structures come from the bad uniformity of the imprinted structures.

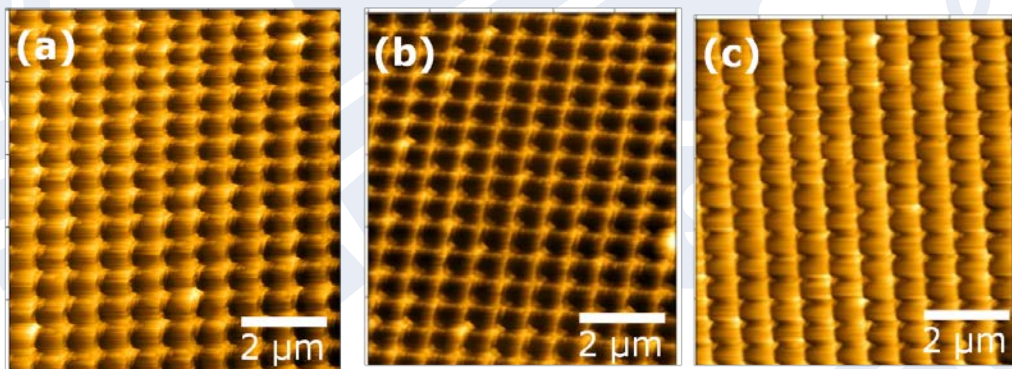


Figure 3.22: AFM images of samples etched by O_2 for (a) 3, (b) 5 and (c) 8 seconds and SF_6 with 10% O_2 for 40 seconds. Showing that 5 seconds is the most appropriate in our experiment.

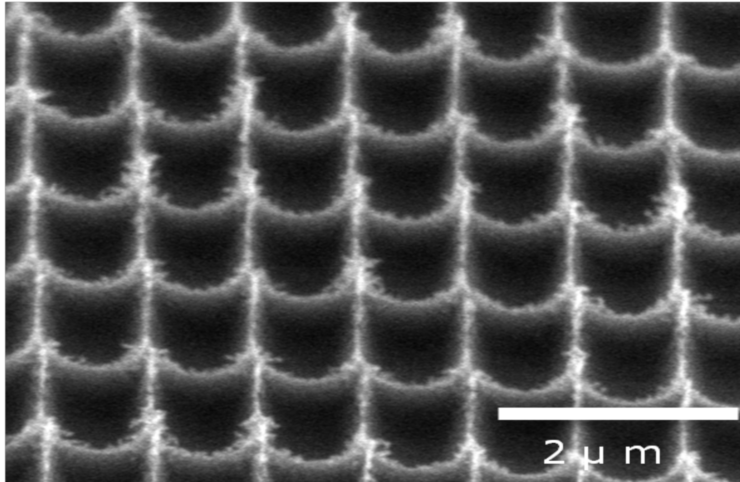


Figure 3.23: SEM image of samples etched by O_2 for 5 seconds and SF_6 with 10% O2 for 40 seconds. Silicon oxide is created on the corners of mesh.

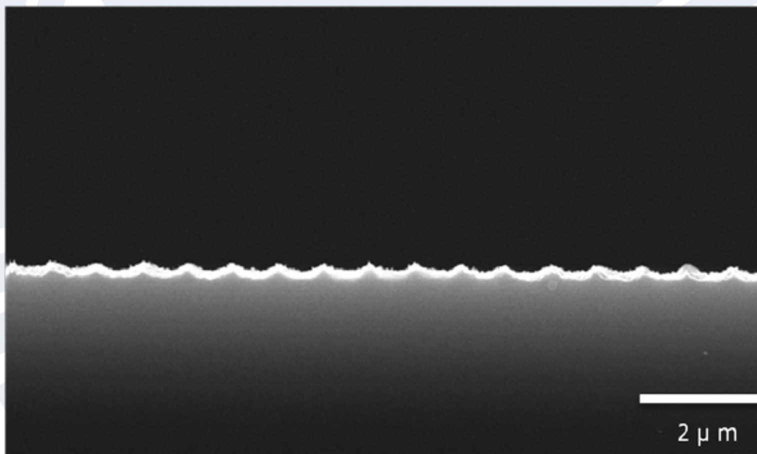


Figure 3.24: SEM image of samples which is etched by O_2 for 5 second and SF_6 with 10% O_2 for 60 seconds. Disappearance of the structures results from insufficient sidewall passivation.

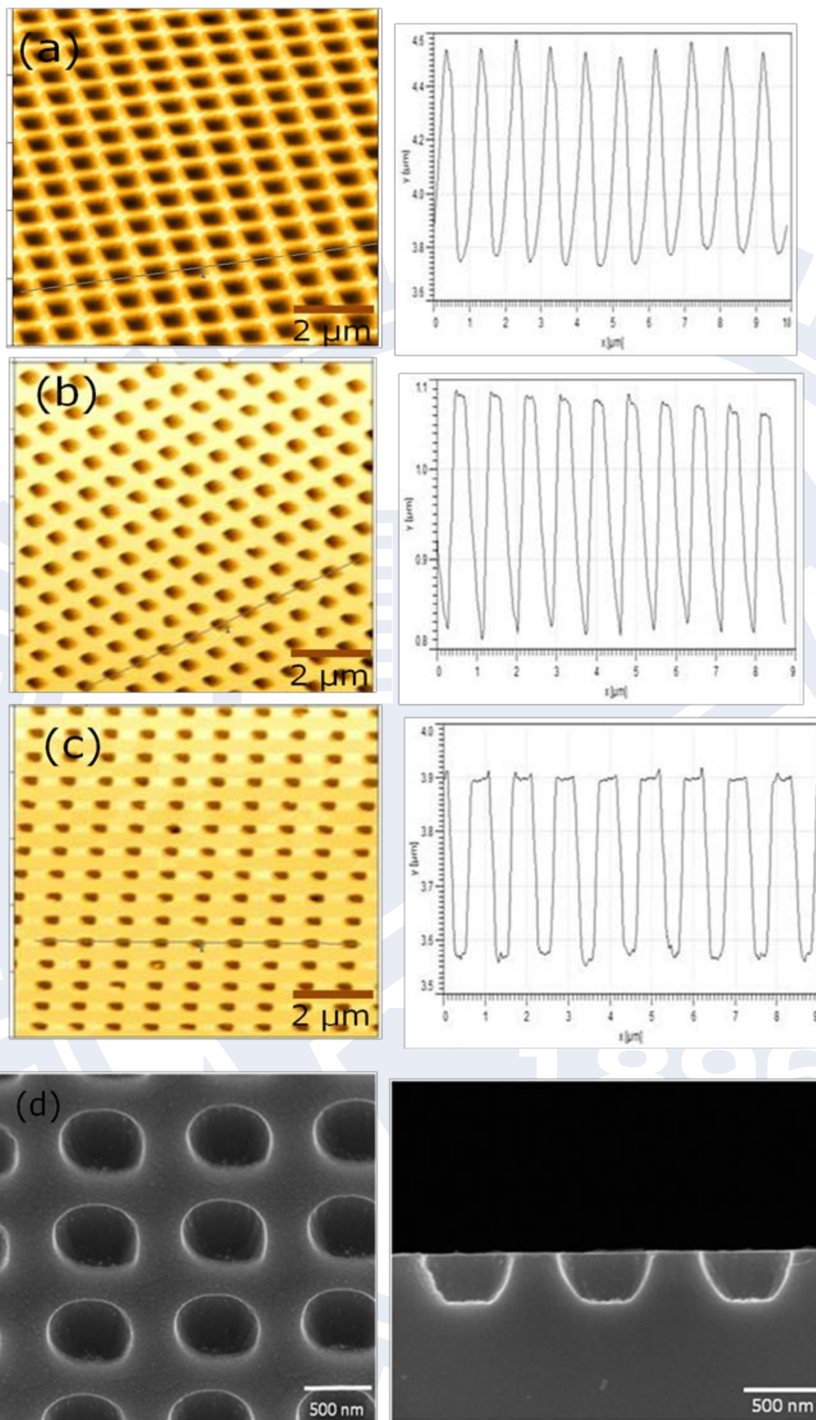


Figure 3.25: AFM measurement and SEM images of samples etched by O_2 in 5 second and (a) SF_6 with 20% O_2 for 30 second, (b) 30% O_2 for 30 second, (c) 40% O_2 for 20 second and (d) 60% O_2 for 60 second.

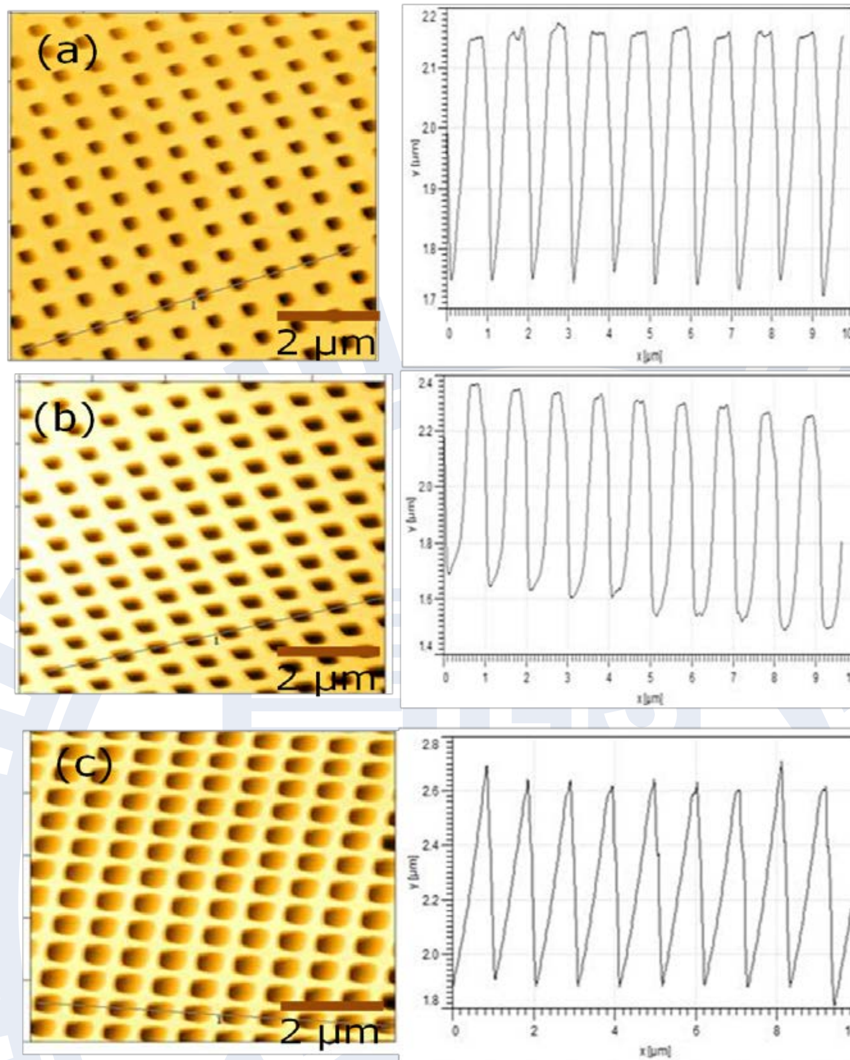


Figure 3.26: AFM and depth profile of samples etched by O_2 in 5 seconds and by SF_6 with 40% O_2 for (a) 30 seconds, (b) 40 seconds and (c) 70 seconds.

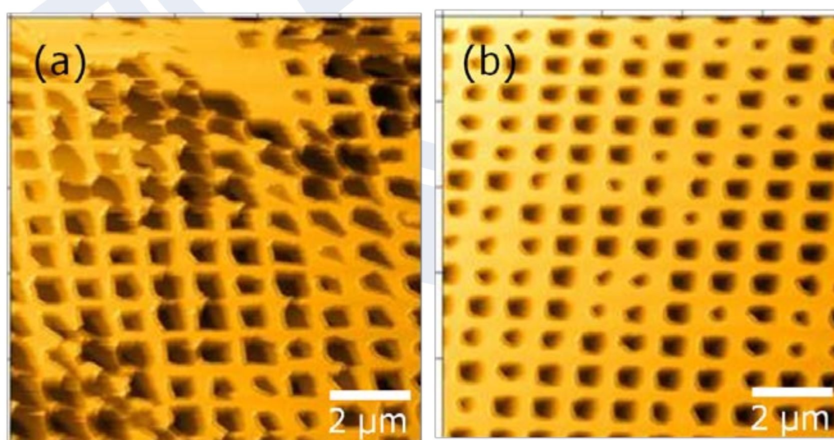


Figure 3.27: AFM images of samples etched by O_2 for 5 seconds and SF_6 with (a) 10% O_2 and (b) 30 % O_2 with pressure of 150 mTorr, power of 150 W for 15 seconds.

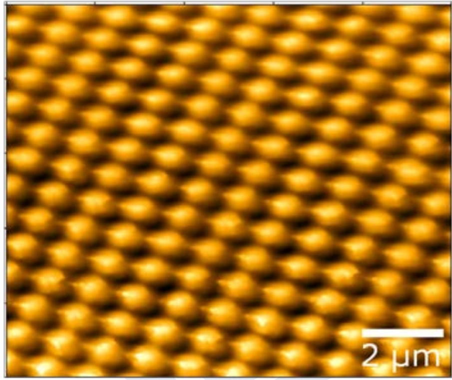


Figure 3.28: AFM images of the sample etched by O_2 for 5 seconds and SF_6 with 40% O_2 with pressure of 200 mTorr, power of 100 W for 60 seconds.

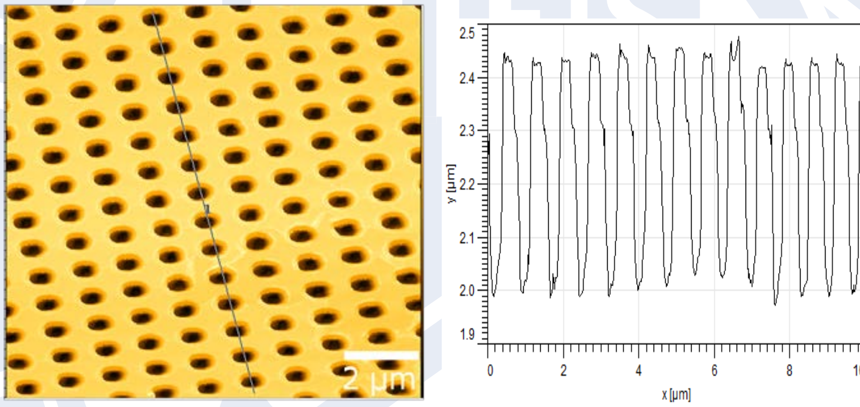


Figure 3.29: AFM images and depth profile of the sample etched by O_2 for 5 seconds and SF_6 with 40% O_2 with pressure of 300 mTorr, power of 50 W for 180 seconds. The pores with a depth of 450 nm and a diameter of 450 nm.

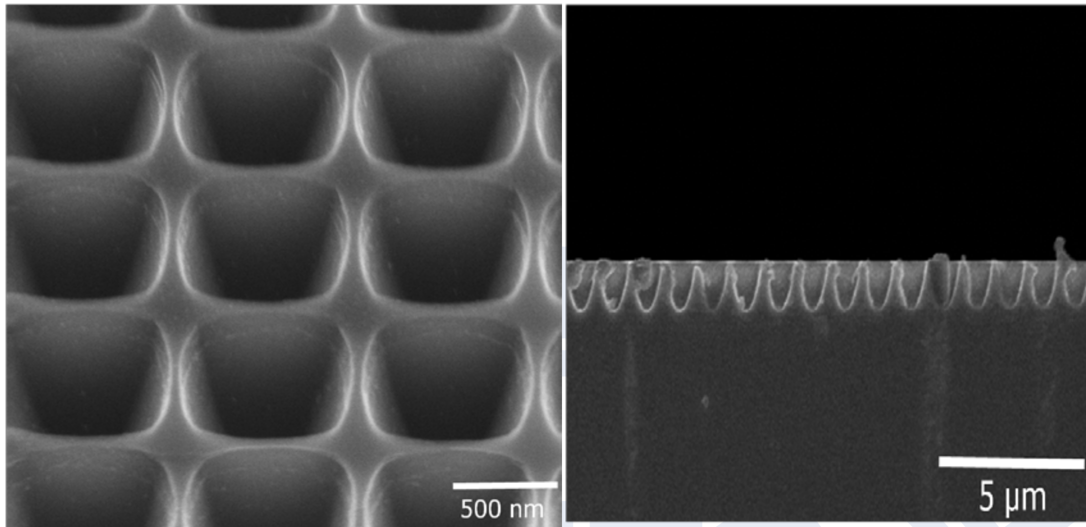


Figure 3.30: SEM images of samples etched by O_2 for 5 seconds and SF_6 with 40% O_2 for 70 seconds. (a) Top view of pre-pattern structures and (b) cross sectional view of inverted pyramid pre-pattern structures.

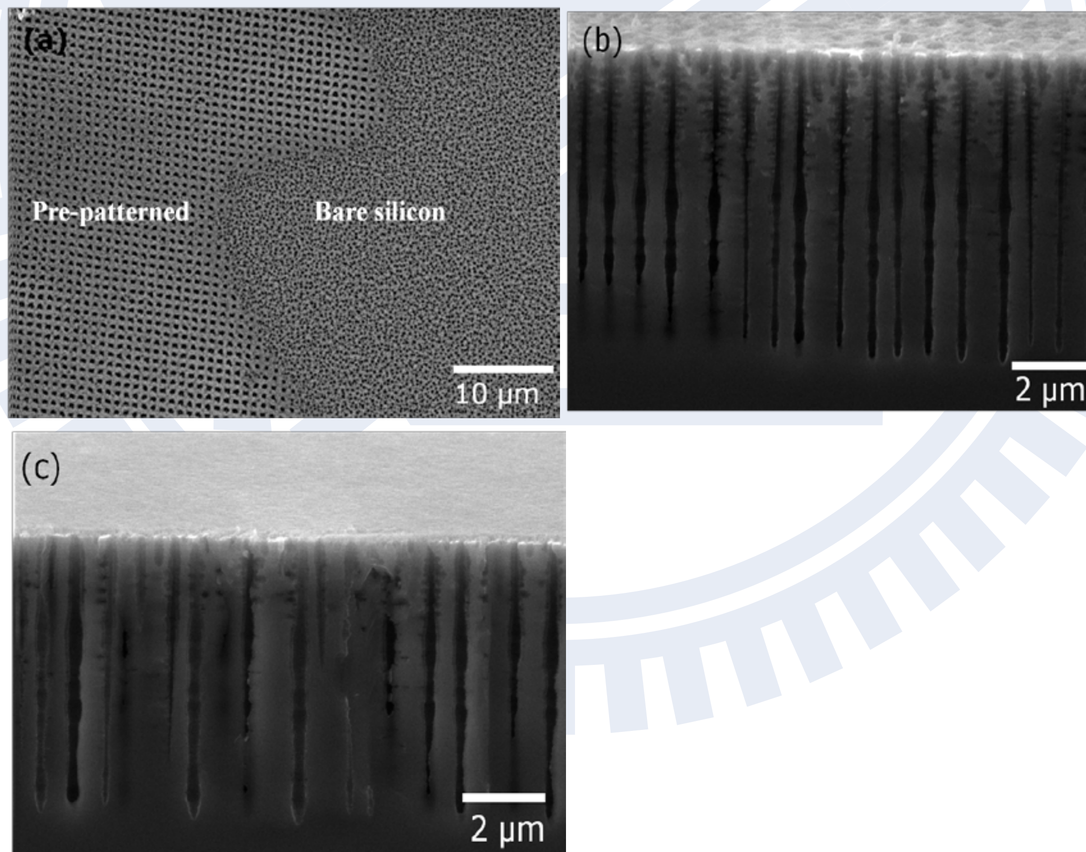
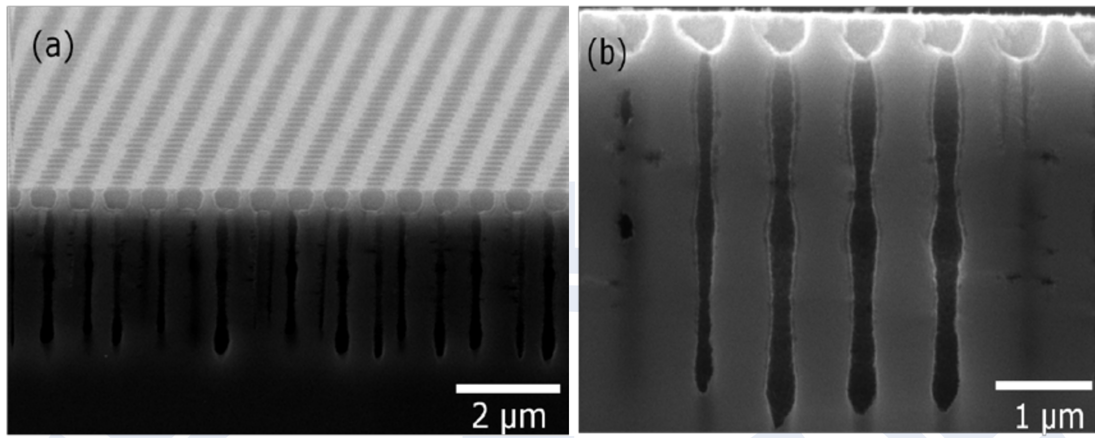


Figure 3.31: SEM image of anodized pores with a current density of 8 mA/cm2 for 300 seconds. (a) Comparison between pre-patterned and bare silicon, (b) cross-sectional view of pre-patterned area and (c) flat area.



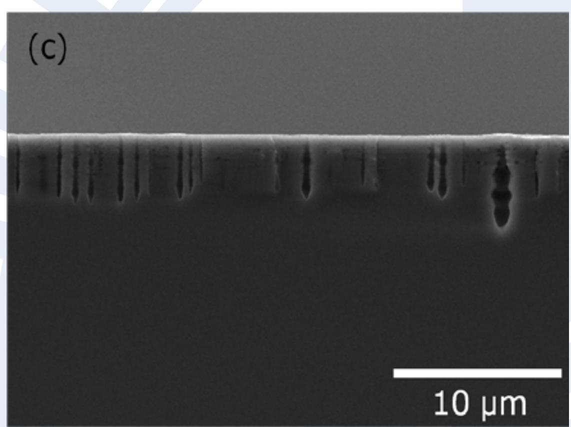


Figure 3.32: SEM image of anodized pores with a current density of 4 mA/cm2 for 240 seconds. (a) Tilted view of pre-patterned area, (b) cross-sectional view of pre-patterned area and (c) cross-sectional view of bare silicon area.

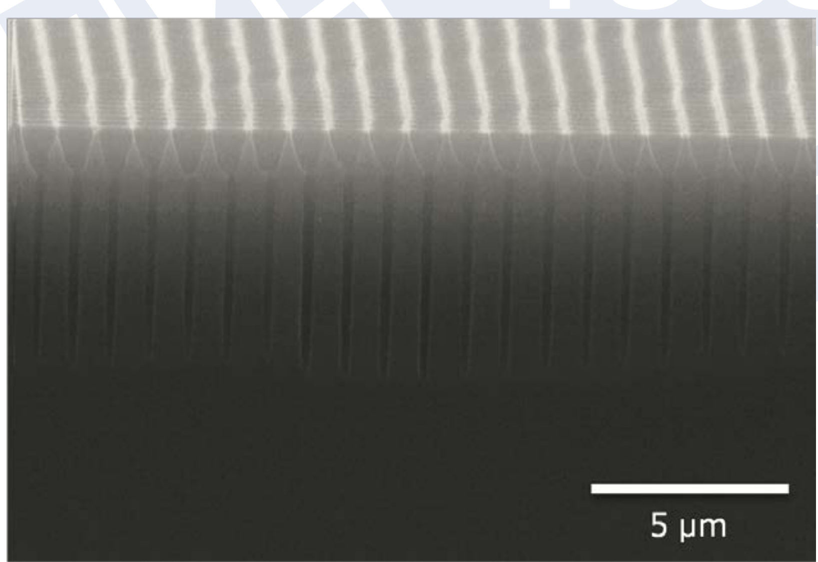


Figure 3.33: SEM view of anodized pores formed with a current density of 4 mA/cm2 for 240 seconds, from a sample pre-etched with inverted-pyrampids.

Evolution of current during anodization.

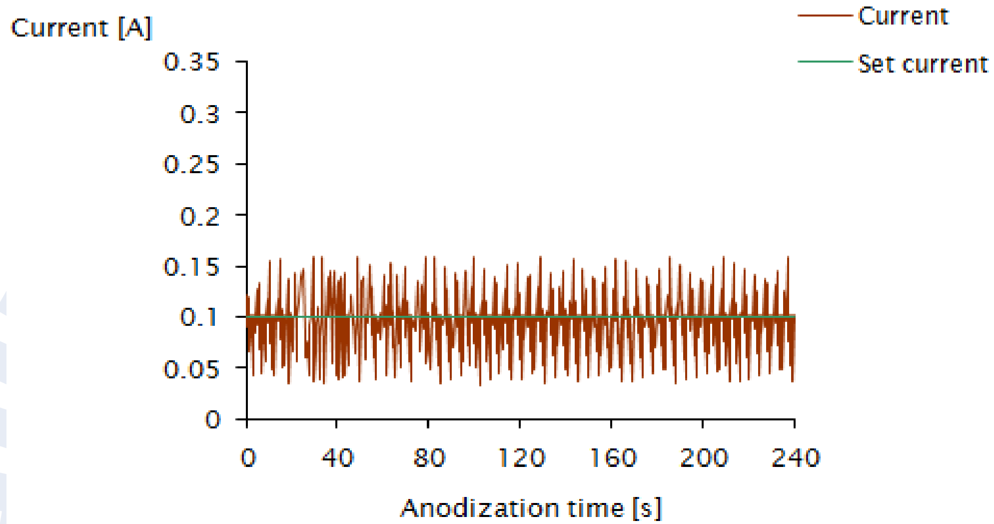


Figure 3.34: Evolution of current during anodization. The set current is 0.1 A, but the irregular current density that is delivered by the generator.

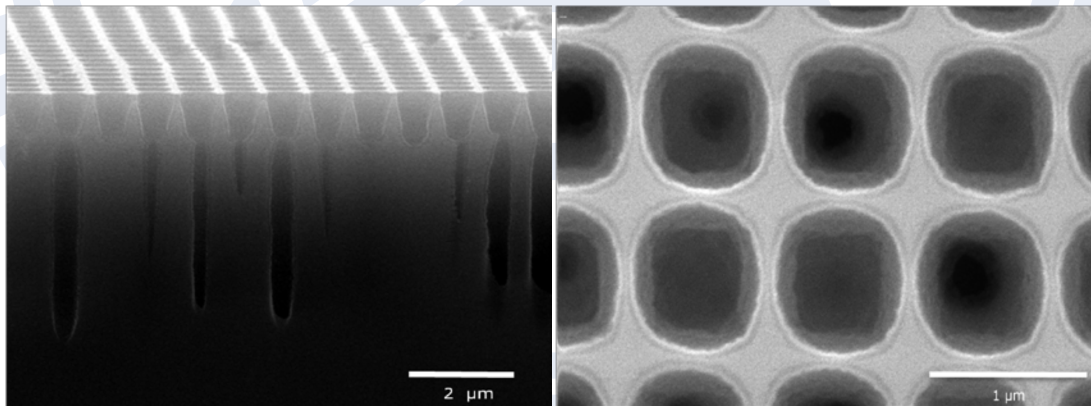


Figure 3.35: SEM view of pores formed from a sample with inverted-pyramids etched pits anodized with the etching condition of 4 mA/cm2 currnet density for 240 seconds. The backside of the sample was highly doped to obtain a better backside contact.

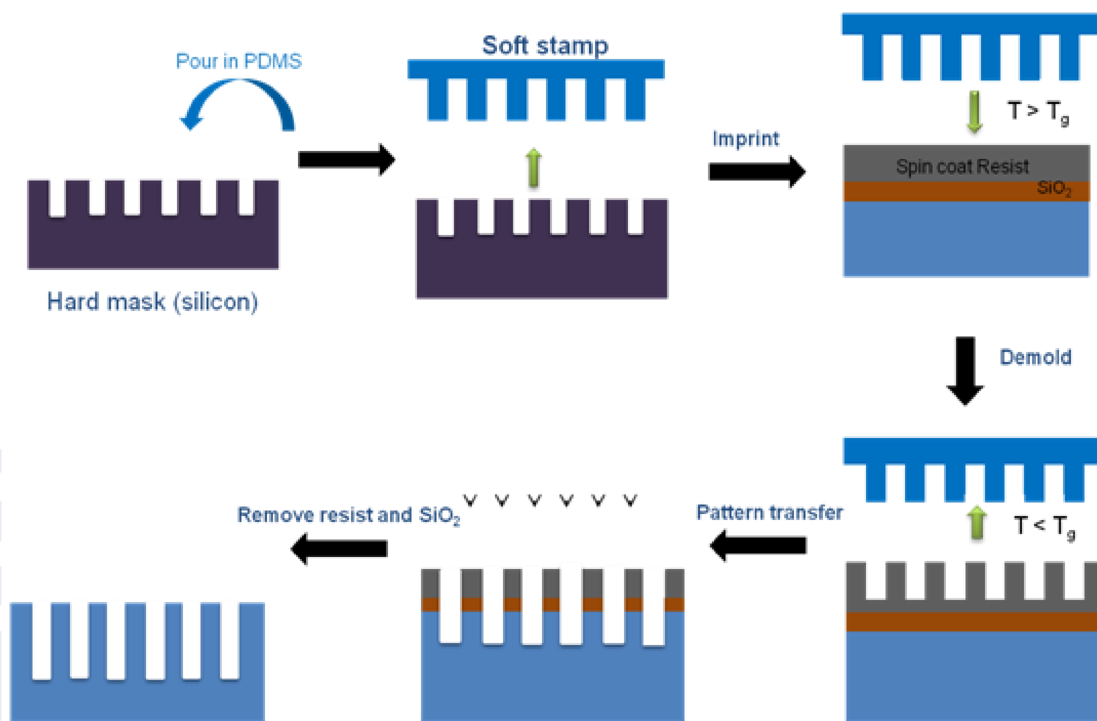


Figure 3.36: Experimental flow of soft-NIL, which is composed of soft stamp fabrication in the step 1, imprint process in the step 2 and 3, the pattern transfer in the step 4 and 5.

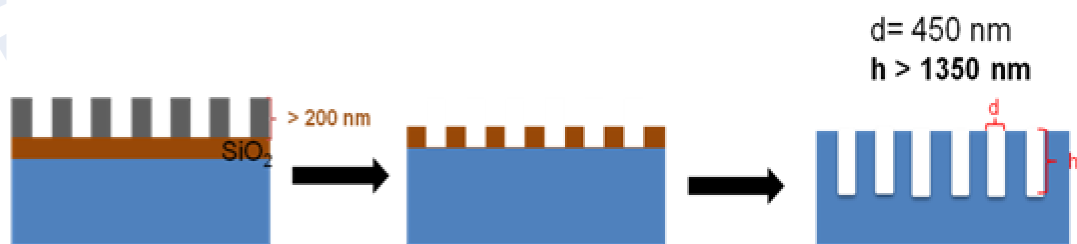


Figure 3.37: Experimental flow of the pattern transfer. In the first step, use resist as mask to open silicon window, and use silicon oxide as mask to etch silicon in the second step.

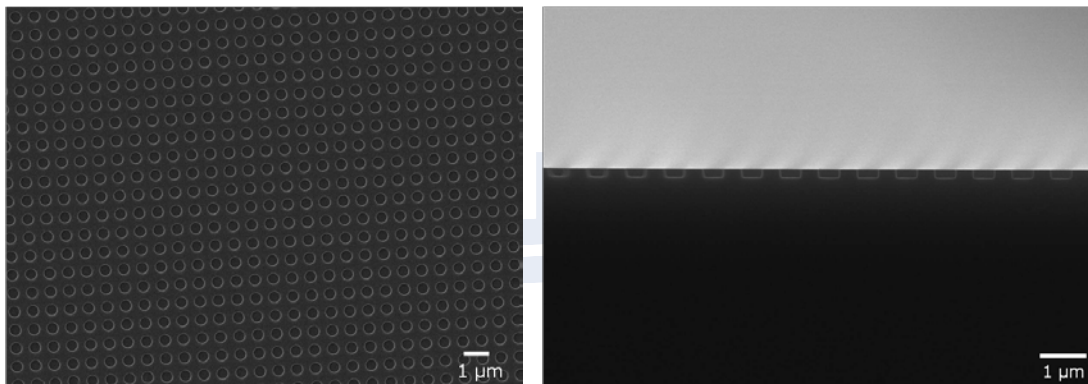


Figure 3.38: SEM image from top view of imprinted structure (left). SEM image from cross section of imprinted structure after removing residual layer (right).

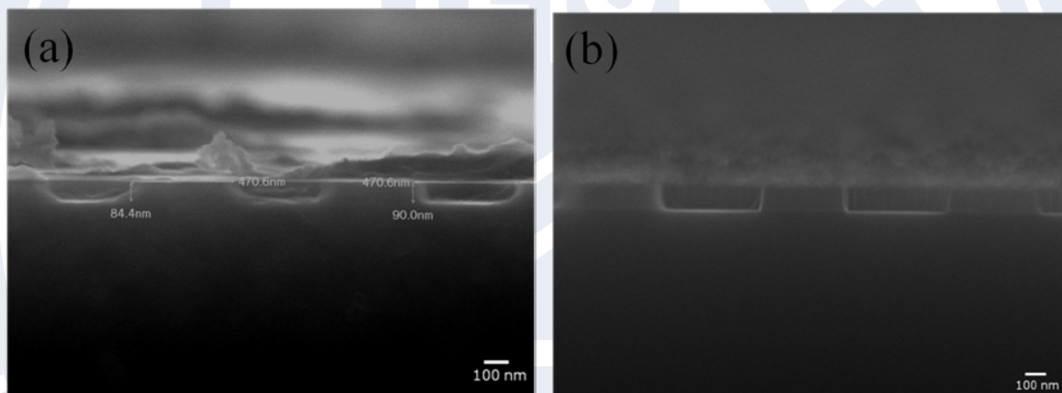


Figure 3.39: SEM images of samples etched by CHF_3 and CF_4 with 4 % O_2 for open silicon window. (a) The sample is etched for 40 seconds, and the silicon oxides still appear on the bottom. (b) The sample is etched for 60 seconds, and the silicon window is open.

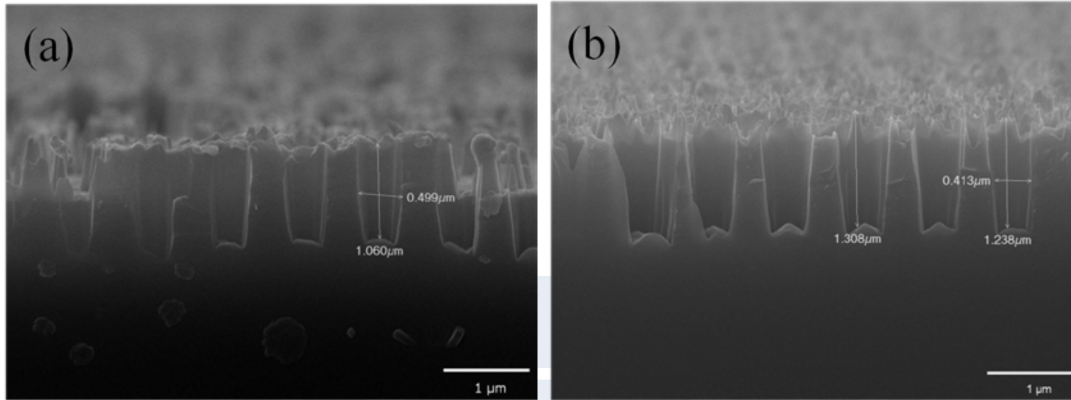


Figure 3.40: SEM images of samples etched by HBr with Cl_2 and HBr with O_2. (a) The sample is etched for 7 and 1 minutes, and the silicon is etched over 1μm. (b) The sample is etched for 9 and 1 minutes, and the silicon is etched over 1.2μm.

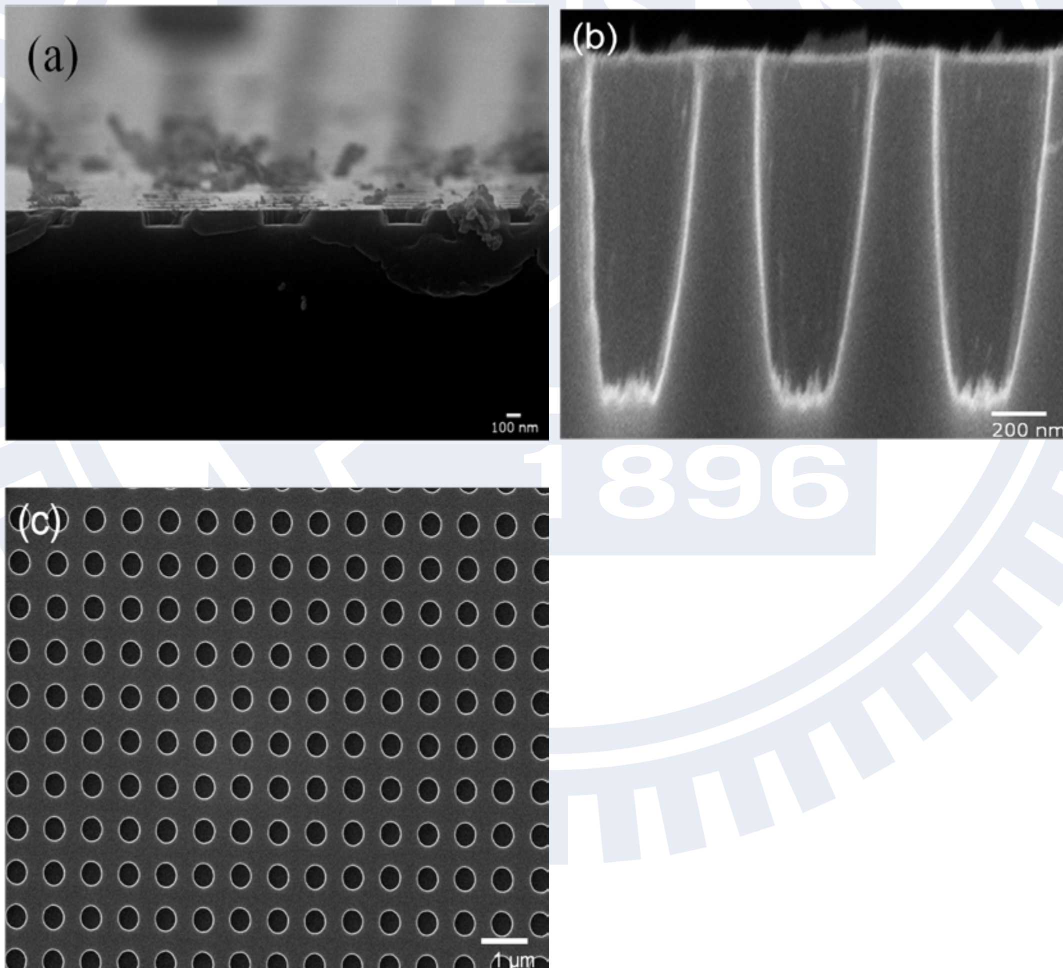


Figure 3.41: SEM images of samples. (a) The sample etched with CF_4 and 4 % O_2 for 60 seconds. (b) The cross section of sample etched by HBr with Cl_2 and HBr with O_2

for 11 and 1 minutes after opening silicon window. (c) The top view f sample etched by HBr with Cl_2 and HBr with O_2 for 11 and 1 minutes after opening silicon window.

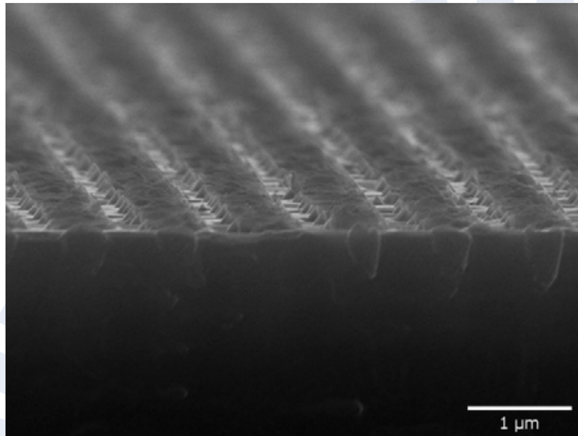


Figure 3.42: SEM images of the sample which is etched by HBr with Cl_2 and HBr with O_2 for 13 and 1 minutes, and the silicon oxide is not enough to protect the surface, which appears so rough.

Chapter 4: Conclusion and Perspectives

The soft-NIL process is briefly composed of the following three steps: (1) fabrication of soft stamp, (2) imprint process and (3) pattern transfer. Each step has its own challenges that need to be solved.

4.1 Conclusion

For the fabrication of soft stamp, inappropriate design of the soft stamp will result in deformation and causes an unexpected imprinted structure. If the aspect ratio is too large, buckling and lateral collapse will occur during imprinting. After considering deformation models, we fabricate soft stamps avoiding the above deformations and successfully imprint desired features.

Concerning the imprint results, the filling percentage strongly affects the performances. The best method to keep a good uniformity over a large area is to keep 100% filling by adapting the resist thickness to 160 nm. The filling percentage can be calculated from the thicknesses of the resist divided by the cavity coverage and the height of soft stamp. Intended fine filling can also perform perfect features concerning the squeeze flow during imprint. In addition to uniformity, a thin residual layer is another key aspect for the imprinted structure. We achieve a very thin residual layer and keep a highest resist contrast in our experiment. The imprint process is proved sufficiently repeatable and stable over ten times imprint.

Concerning the pattern transfer, this step plays a critical role in performing desired features. We prove the importance of accurately removing residual layers, and the essential of uniform imprinted structures. To reach a good pattern transfer, the links between the etching profiles and etch parameters such as power, pressure, and gas flow are discussed. When higher O_2 concentrations are added, it results in a better sidewall passivation but also decreases the etching rate of silicon. Therefore, improvements of the anisotropic etching are shown by applying a low power density

and high pressure, since low power density strongly decreases the lateral etching and high pressure increases the silicon etching rate.

Extremely deep pores are achieved owing to a combination between dry-etch and anodization, because the soft-NIL patterning process allows to make regular pores. A better control of anodization is performed by an inverted-pyramid-shaped cavity intentionally etched providing specific points to etch. Based on this thought, we take advantage on a negative effect existing in dry etching process, which results in slopped sidewalls. After anodizing with an optimized etching condition, the resulting structures demonstrate that inverted-pyramid-shaped pre-patterning successfully provides ordered and deep pores (~8 μm). Nevertheless, large difference between pores resulting from irregular current feed may be unacceptable in ESS process.

Therefore, we deposit 100 nm silicon oxides before coating the thermal resist, and use this oxide as mask to etch silicon for the desired structures. The imprinted structures show the same property as above bare silicon, and we could achieve pores with aspect ratio over three. Besides, the etching profile is still smooth and has a nearly vertical sidewall.

Finally, the applications of soft-NIL are broad since the imprinted structures are feasible for many etching processes. For instance, some of the structures achieved in this work are ideal for light trapping and the sub wavelength passive optics components of PV. Besides, our study indicates that soft-NIL, as an alternative lithography, can potentially replace conventional lithography in some applications like pre-patterning for controlled anodization.

4.2 Perspectives

In the extension of this thesis, the main task is to prove the feasibility of TFSC based on soft-NIL process. A successful thin-film formation not only depends on an appropriate porous array, but also on appropriate annealing conditions. For now, the achievement for ESS application is still unclear, so different annealing will be treated for the anodized deep-pores samples.

The theory behind forming defect-free single-crystalline thin films from porous silicon is based on the surface diffusion. Therefore, appropriate annealing conditions like hydrogen, argon were proven appropriate, but, conversely, nitrogen may block reorganization by forming silicon nitrides [4-1]. These different conditions and the properties of the results are the object for further experiments and studies.

Another challenge that arises will be to find an optimal anodization process that creates an equal pore diameter, because the difference on pore diameter may not be acceptable for our application. A possible explanation for the irregular diameter is the irregular current density that is delivered to the sample by the generator. We try to improve the electrical contact between the sample and the anodization cell by the backside doping of the sample. However, the irregular current feed is still observed in these samples. This difference between pores may be optimized by further experiments like using rear-side illumination instead of front-side.

Although the development of deep pores is achieved by depositing silicon oxide as hard mask instead of single resist, this extra deposition is a factor increasing the process cost. Therefore, this concern may be improved by two aspects of treatments under investigated.

(1) Imprint in more stable "sol-gel" films has been investigated [4-2]. Under appropriate annealing, these sol-gel films allow to obtain a highly resistant coating compared to PMMA [4-3]. Besides, patterning sol-gel films by soft-NIL has the advantage that soft stamp is compliant to the surface which minimize the pressure to obtain contact with the substrate and allow imprinting curved and irregular surfaces.

(2) Applying different dry-etch mechanisms. In our experiment, the control of sidewall passivation becomes the main limitation as the depth increases. Fluorine molecules do result in increased etching rate, but at the expense of increased lateral etching as the sidewall passivation is attacked by high fluorine concentrations. One method of utilizing high fluorine concentrations is to work at low substrate temperatures. This "cryogenic" temperature etching does enhance the sidewall

passivation [4-4]. Another technique is based on the mechanism invented by Lärmer and Schilp [4-5]. They use a variant of the sidewall passivation technique. Rather than the sidewall protection being an integral part of the process, the passivation is deliberately segregated by using sequentially alternating etching and deposition steps in this mechanism. A sidewall passivation polymer is deposited and subsequently the polymer and silicon are etched from the bottom, to allow the etching to proceed directionally. In this cyclic way, the etching and deposition can be balanced to provide accurate control of the anisotropy.

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