國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

使用 I-Line 雙重曝光技術實現非對稱 0.1μm P 型金氧半場效電晶體與相關可靠度問題之研究

A Study of Double-Patterning Technique with i-line Stepper to accomplish 0.1μm PMOSFETs and Its Related Reliability Issues

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中華民國九十九年九月

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摘要

本篇論文使用i-line光學步進機，應用雙重微影成像法之技術，製作出遠優於i-line光學步進機解析度極限(~0.3μm) 的次0.1微米的閘極圖形;並搭配新設計的光罩，改進先前研究遭遇到元件過度蝕刻造成缺陷的問題[1]。這技術包含了兩次光學微影以及後續蝕刻製程。此技術可應用在非對稱金氧半場效電晶體的結構設計與製作，其電晶體可以比傳統的對稱結構有更大的最佳化空間。本研究調變了汲極延伸區域的接面深度與源極/汲極邊緣的局部摻雜（halo implant），來驗證其對於驅動電流、短通道效應的影響，最後再進行元件負偏壓溫度不穩定性的分析研究。

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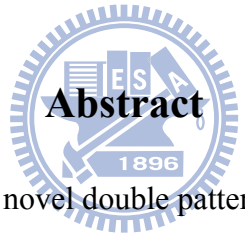

Abstract

In this thesis, we developed a novel double patterning technique, which consists of two exposures with an i-line stepper and two etch steps, to define poly-Si gates with line width down to sub-100nm regime, far beyond the resolution limit of the conventional i-line lithographic method (~0.3 μm). The double patterning process has also been employed in fabrication of sub-100 nm p-channel devices. During the course, we addressed an unexpected etch-induced recess phenomenon encountered in the study of our group in previous year [1] with ingenious modification in the mask design. We've also demonstrated the capability of the developed double patterning method in fabricating MOSFETs with asymmetrical S/D. The basic electrical

characteristics of the PMOSFET devices with symmetrical and asymmetrical S/D were measured and compared. The results confirm the enhancement of immunity to the short-channel effects with asymmetrical S/D design. Finally, we also explored the negative-bias-temperature-instability (NBTI) of the fabricated devices.

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Chapter 1 Introduction

1-1 Background

With the first commercial Si transistor announced by Texas Instruments (TI) in 1954 [2], Si quickly replaced Ge as the most important semiconductor for manufacturing. In 1970s, the "Si-based" technology had been well established. To increase the device density and reduce the fabrication cost, the IC industry had concentrated on scaling down the devices' dimensions and enlarging the wafer size since the early 1960s. Today, the mainstream of wafer diameter has been shifted from 8 inch (200 mm) to 12 inch (300 mm), and the microprocessor unit (MPU) physical gate length of device has scaled down to nano era (< 29 nm) according to the International Technology Roadmap for Semiconductors (ITRS) 2009 (Table. 1-1) [3]. Moreover, the physical gate length of device is scaling down to 22 nm for the requirements of high-performance logic technology in 2012 [3].

Major purposes of shrinking the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) dimension are to enhance the driving capability and increase the device density. However, as the MOSFET dimensions are reduced, there are many issues obstructing the progress of the semiconductor device. The most well known issue is the occurrence of short channel effects (SCE) that cause the threshold voltage

(V_{th}) roll-off, drain-induced barrier lowing (DIBL), and bulk punch-through, etc [4]-[16]. These effects become more difficult to suppress as the channel length decreases continuously.

Another issue is related to the lithography techniques for generating the fine patterns. Current 45 and 32 nm nodes of manufacturing need water-based 193nm immersion (193i) lithography to generate the most critical patterns. However, the cost of 193i lithography machine is above 60 million U.S. dollars [17] which is too high and not affordable for most academic organizations. Concurrently, although e-beam exposure technique is feasible to scale device gate length down to 0.1 μm, it suffers from the low throughput. To relieve these concerns, recently our group proposed the use of double patterning technique (DPT) with an i-line stepper to realize the fabrication of sub-0.1 μm devices [1] which could take advantage of much reduced cost as compared to the 193i techniques and much faster throughput as compared to the e-beam counterparts.

To alleviate the SCEs and other degradation effects caused by scaling, many researchers have devoted themselves to inventing new device structures to enhance the device performance. For example, devices with lightly-doped drain (LDD) [18] structures were utilized to decrease the hot-carrier effects (HCEs). Even with the scaled supply voltage nowadays, LDD structures are still important in input/output

(I/O) devices. Other devices with double implanted LDD (DI-LDD) [18] structures, which are also called “halo implant” structures [10]. Such structures are added with an oppositely type of dopants located near the channel and underneath the source and drain junctions to meliorate the SCEs. Thanks to the development of those structures, great advancement in semiconductor technology has been achieved and the progress is still going.

Furthermore, in order to lower process cost and simplify device fabrication, standard manufacture schemes are devised with the symmetric structure. That is, the source and drain doping profiles are the same. However, theoretically symmetric structures are not ideal for device performance, and, with an appropriate design, asymmetric structures should outperform the symmetrical counterparts.

1-2 Double Patterning Technique

As mentioned above, 193i lithography is being used for 45 nm and 32 nm nodes of manufacturing [3]. The Rayleigh equation applicable for immersion lithography can be written as

$$HP = \frac{K\lambda}{N_{IF} NA}, \tag{1-1}$$

where HP is the minimum printable half pitch feature size, N_{IF} is the immersion fluid index of refraction at the lithographic wavelength, NA is the numerical aperture of the

stepper lens, λ is the lithographic wavelength, and K is a measure of the lithographic process capability. Since the N_{IF} of a liquid (e.g., water) is much larger than that of air, the resolution can be improved with the wet lithographic techniques.

However, it's very difficult for 193i to push further into 22 nm node and beyond, so finding a succeeding technique is urgent. One of the possible solutions is extreme ultra-violet (EUV) method which uses a much shorter wavelength of 13.4 nm with an NA of ~0.25. Another way is the 3rd generation immersion 193 nm system which has ~1.55 NA requiring higher refractive index (RI) (RI > 1.8) fluids, lens and photo-resists materials. Nevertheless, none of these techniques are ready for production yet to this date [20].

Double patterning (DP) is a resolution improvement technique that can potentially cut the pitch of patterns in half [21]. Double patterning lithography (DPL) has already shown its feasibility to the 22nm node [22]. Consequently, DP is viewed as a bridge to EUV lithography technology, which is not expected to be available for volume production until approximately 2011 or later.

1-3 Halo Implantation and Source/drain Extension Structure

For the purposes of performance enhancement and cost reduction, MOSFET scaling is inevitable. Certainly there are a number of critical problems lying ahead that

need to be carefully addressed [23]-[24].

Nowaday the most general method to restrain the SCE-induced drain-induced barrier lowing (DIBL), Vth roll-off, and bulk punch-through, is to perform the halo implantation (also called the pocket implantation) [19], which was first presented in 1985 and also called DI-LDD [18].

Halo implantation structure is formed using a titled angle implantation to form the high counter doping regions at the drain/substrate and source/substrate junctions and below the channel. The dopant type is the same as that of the substrate. Because of the relatively high doping concentration, the depletion regions of both source and drain extensions can be suppressed efficiently, resulting in a significant reduction in the subthreshold leakage current and the bulk punch-through, hence alleviating the SCE-induced degradations.

LDD structure [18] is used to improve HCE for devices working under a high operation voltage (e.g., I/O devices). As the applied drain voltage is sufficiently high that the maximum electric field along the channel exceeds a certain value, significant impact ionization may occur near the drain side. Fortunately, we can utilize the LDD structures to relieve the concern somewhat by decreasing the peak electric field in the channel of the MOSFET [25]. Actually LDD structures [18] have been commonly used to improve hot-carrier reliability [26]-[28] for MOSFETs operated under a high

voltage.

However, when MOS devices are scaled to nano-scale regime, the LDD regions will contribute more parasitic resistance and result in drain current degradations. Moreover, operation voltage of the core devices in most advanced chips has been lowered to around 1V. This means the HCEs is no longer a major concern for these devices. Therefore the doping concentration of the regions is increased to a level comparable to that in the deep source/drain S/D regions for reducing the parasitic resistance but the junction depth is retained ultra-shallow for good control of the SCEs. In those nano-scale devices the previous "LDD" regions are renamed as "extension" since they are no longer "lightly doped." Furthermore, the use of asymmetric source/drain (S/D) extension (i.e., the two extensions have different doping concentration and/or junction depth) structures can be adopted for optimizing the current-drive capability, SCE control, and hot-carrier reliability [26]-[28].

1-4 Motivation and Objectives of this Thesis

As mentioned in Sec. 1-2, our group proposed the implementation of double patterning technique (DPT) into the i-line photolithographic process to realize the fabrication of nano-scale devices [1]. Basically the concept has been proved to be useful and feasible for generating patterns with critical dimension (CD) down to 0.1

μm. However, most of the devices fabricated in the previous work were found to be with poor performance and leaky. Origins for such outcome are found to be related to the etch-induced recess occurring at one side of the gate during the second gate etch step. An example is shown in Fig. 1-1. Occurrence of such phenomenon is due to the failure of end point detection during the second gate etch step. This issue has been addressed [1] and is expected to be solvable with a modified mask design. In this study, we examine the feasibility of the DP process with aforementioned modification in mask layout design and aim at fabrication and characterization of p-channel devices with channel length down to 0.1 μm and even shorter.

1-5 Organization of This Thesis

This thesis is divided into four chapters and each chapter is introduced briefly as below.

In Chapter 1, we show a brief overview of the background and the motivation.

In Chapter 2, we describe and evaluate the DP process developed in this work, and then we describe the DP technique for device fabrication. Finally, we present the measurement setup and characterization scheme.

In Chapter 3, we present the experimental results on characterizing the fabricated PMOSFET devices. Transfer and output current-voltage (I-V), and

capacitance-voltage (C-V) characteristics are examined and discussed. We also explore the effects of the halo-implant, symmetric and asymmetric extension structures on the device characteristics, device reliability issue like NBTI performance.

Finally, in Chapter 4, we conclude the results and suggest the future work.

Table 1.1 Lithographic-Field and Wafer Size Trends [3]

Year of Production	2009	2010	2011	2012	2013	2014	2015
Flash ½ Pitch (nm) (un-contacted Poly)(f)	38	32	28	25	23	20	18
DRAM ½ Pitch (nm) (contacted)	52	45	40	36	32	28	25
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	45	38	32	27	24	21
MPU Printed Gate Length (GLpr) (nm) ††	47	41	35	31	28	25	22
MPU Physical Gate Length (GLph) (nm)	29	27	24	22	20	18	17
Lithography Field Size							
Maximum Lithography Field Size—area (mm^2)	858	858	858	858	858	858	858
Maximum Lithography Field Size—length (mm)	33	33	33	33	33	33	33
Maximum Lithography Field Size—width (mm)	26	26	26	26	26	26	26
Maximum Substrate Diameter (mm)—High-volume Production (>20K parts starts per month)							
Bulk or epitaxial or SOI wafer	300	300	300	300	300	450	450

Chapter 2 Device Structure, Process Flow and Measurement Setup

All the device fabrications mentioned in this thesis were accomplished at the National Nano Device Laboratories (NDL).

2-1 Device Fabrication and Process Flow

In this chapter, we take the asymmetric PMOSFET with drain-side only halo as an example to illustrate the process flow in Fig. 2.1.

The devices were fabricated on 6-inch n-type bare Si wafers with resistivity of 15~25 ohm-cm. N-type well was formed by phosphorus ion (P^+) implantation (at 120 keV, $7.5E^{12}$ cm^{-2}), Vth was adjusted by arsenic ion (As^+) implantation (at 80 keV, $1E^{13}$ cm^{-2}), anti-punchthrough implantation was formed by P^+ implant (at 120 keV, $4E^{12}$ cm^{-2}), and channel stop implantation for local oxidation of silicon (LOCOS) isolation was done by As^+ implant (at 120 keV, $3E^{12}$ cm^{-2}).

After the above standard MOSFET LOCOS and n-well processes, thermal gate oxide with a thickness of 3 nm was grown in N_2O ambient, followed by a 170 nm-thick undoped polycrystalline silicon (poly-Si) deposition performed in a vertical furnace by low-pressure chemical vapor deposition (LPCVD). Subsequently, undoped

poly-Si was implanted with boron-fluoride ion (BF_2^+) at 15 KeV, $5E^{15}$ cm^{-2}. Then a 50 nm-thick LPCVD TEOS oxide was deposited as a hard mask layer.

The DP technique uses two masks denoted as G1 and G2, respectively, as shown in Fig. 2.2 to define the gate. During fabrication the gate etching steps were done with a Lam-TCP9400 operated with end point detection mode. An annealing was employed using rapid thermal anneal (RTA) at 900°C for 10 second (s) after the G1 formation process. Then asymmetric source and drain extensions were formed separately after G1 and G2 definitions, respectively. Meanwhile, according to the demand of experimental conditions, the 45° tilted angle halo-implantation was done with As^+ (at 15 to 30 keV, $5E^{12}$ cm^{-2}) at drain side only, as shown in Fig. 2.1. For the split with source-side-only halo, such implant was done immediately after the source-side extension implant. Additional split with symmetrical halo structure was also fabricated. For that split and control samples which was with symmetric S/D extension and no halo implemented, the S/D extension and halo (optional) implants were done together after G2 gate definition.

After halo implantation, 100 nm sidewall spacer was formed with LPCVD TEOS oxide, followed by deep S/D implant with BF_2^+ (at 40 keV, $5E^{15}$ cm^{-2}). Afterwards, the regions of substrate windows were formed and implanted with P^+ (at 40 keV, $5E^{15}$ cm^{-2}). Then the wafers were annealed using spike rapid thermal anneal

(SRTA) at 1000°C to activate the dopants in the preceding implantation processes. Finally, standard backend flow was executed to complete the fabrication.

The major split conditions explored in this work are listed in Table 2.1. Other implant conditions, including well implantation, threshold voltage adjustment implantations, channel stop implantation, and anti punch-through implantation are shown in Table 2.2.

2-2 Feasibility of the Double Patterning Technique

After finishing the G1 and G2 gate etching steps, we employed in-line scanning electron microscope (SEM), and focused ion-beam (FIB) SEM imaging techniques to check the test structures as well as the practical gate electrodes which were formed by either DP or single patterning technique. For all lithographic steps, we used an I-line stepper to generate the photoresist (PR) patterns, and the design of the DP masks is shown in Fig. 2.2. In this figure, the G1 mask covers the right side of the active region which is capped with the poly-Si as the gate material, and then the G2 mask covers the left side of the active region. After the two-step gate mask processes, the overlapped region of the G1 and G2 masks defines the gated region, and the gate length can be smaller than the resolution limit of single patterning technique (~0.35 μm) with conventional I-line steppers.

Figure 2.3 shows the gate length images which were formed by conventional single patterning technique. In the pictures, in order to evaluate the gate length error caused by the process and instrumental factors, we compare the difference between the designed or nominal length (L_{mask}) on mask and the practical physical length (L_{gate}) of the etched poly-Si gate measured by the in-line SEM.:

$$Error = L_{mask} - L_{gate}\,, \tag{2-1}$$

$$Error\ \% = \frac{|\,L_{mask} - L_{gate}\,|}{L_{mask}} \times 100\%\,. \tag{2-2}$$

In Fig. 2.3, it is observed that the error of gate length formed with conventional I-line scheme is less than 10 %. Nonetheless, the feature size of the line is larger than 0.3 μm. Figure 2.4 shows that the shortest gate length is around 32 nm with designed length of 50 nm. Figures 2.5 ~ 2.12 show the in-line SEM images of the etched poly-Si gates formed with the DP method with L_{mask} ranging from 60 to 300 nm. From these figures it is confirmed that the DP can significantly shrink the feature size of the poly-Si gate down to sub-100 nm regime. Generally, the error percentage increases with decreasing L_{mask}. Such trend is reasonable as far as the overlay accuracy of the i-line stepper is concerned. As shown in Table 3, the overlay accuracy is larger than 45 nm. This implies that the gate length designed below 80 nm is out of control and difficult to reproduce. Anyway, the present DP method is useful for generation of line patterns down to 80 nm with reliable control of critical dimensions, as shown in Fig.

2.13.

2-3 Electrical Measurement Setup

In this study, the electrical characteristics of the fabricated devices were evaluated by using a precision semiconductor parameter analyzer HP 4156A for I-V measurements and an LCR meter HP 4284 for C-V measurements. The device characteristics were measured on the 6 inch probe station at various gate voltages (V_g = 1 ~-2V) and drain voltages (V_d = 0 ~ -2V). Fig. 2.14 shows the measurement setup used in this experiment.

In addition to basic electrical measurements, we also analyze the device degradation and reliability, including test on static negative-bias-temperature instability. Details about the test conditions are given in the thesis as the results are presented.

Table 2.1 Split conditions of the PMOSFETs fabricated with the DP process.

	Symmetric Extension BF_2^+		
Type A	Without Halo Implantation	S/D Extension	5 x10^{14}cm^{-2}, 10 keV
Type C	With Drain Halo Implantation As^+ / Title 45° Twist 27°	S/D Extension	5 x10^{14}cm^{-2}, 10 keV
		Drain halo implantation	5 x10^{12}cm^{-2}, 30 keV
Type D	With S/D Halo Implantation As^+ / Title 45° Twist 27°	S/D Extension	5 x10^{14}cm^{-2}, 10 keV
		S/D halo implantation	5 x10^{12}cm^{-2}, 30 keV

	Asymmetric S/D Extension BF_2^+	
Type B	without halo implantation	
	Source Extension	5 x10^{14}cm^{-2}, 10 keV
	Drain Extension	5 x10^{14}cm^{-2}, 5 keV

Table 2.2 Other major implantation conditions used in the PMOSFET fabrication.

	Ion	Energy (kev)	Dose (cm^{-2})
N-Well	P^+	120	7.5 x10^{12}
Vth	As^+	80	1 x10^{13}
Channel Stop	As^+	120	3 x10^{12}
Anti-Punchthrough	P^+	120	4 x10^{12}

Table 2.3 Specifications of Canon FPA-3000i5+ Stepper.

(Data are courtesy of NDL)

Resolution	0.35 micron (dense lines)
NA	0.63 – 0.45 (automatically variable)
Reticle Size	5-inch
Reduction Ratio	5:1
Field Size	20 mm x 20 mm
Overlay Accuracy	Mean + 3 sigma ≦ 45 nm
Throughput	100 wph (200 mm)

Chapter 3 Results and Discussion

3-1 Nano-Scale Device Performance and End-Point-Detection Issue

Figure 3.1 shows the cross-sectional view of a poly-Si gate with L_{mask} of 0.1 μm. The figure shows that the practical gate length L_{gate} is measured to be 85 nm. Figure 3.2 shows the characteristics of electrical measurements performed on this device. The device was fabricated with source extension formed with BF_2^+ implant (at 10 keV, $5E^{14}$ cm^{-2}), drain extension formed with BF_2^+ implant (at 5 keV, $5E^{14}$ cm^{-2}), and drain-side-only halo formed with As^+ implant (at 30 keV, $5E^{12}$ cm^{-2}, 45 degree).

With the aid of the proposed DP method, well-behaved characteristics are demonstrated in the nano-scale device.

One issue encountered in our previous work [1] is illustrated in Fig. 3.3(a), which schematically shows the layout of original device design regarding G1 and G2 masks mentioned in Chap. 2. Figure 3.4 shows the cross-sectional view of a device taken in the prior study [1]. In the figure we can observe the substrate recess at the right side of the poly-Si gate. Such a phenomenon was induced during the second poly-Si etching step (with G2 mask) and had been identified to be caused by the ineffectiveness of end-point detection (EPD) technique. In the original mask design

shown in Fig. 3(a), most of the poly-Si film area will be removed during the first etching step. Therefore the EDP signal is too weak to be detected in the second etching step. The mismatch in etched profile results in high series resistance and low driving current [1]. To address this issue, in this work we modify the G1 mask by adding additional dummy regions, as shown in Fig. 3.3(b), so the total area of the poly-Si film present during the second etching step is sufficiently large for effective EPD. As the new scheme in mask design is implemented, the above issue is well resolved as evidenced in Fig. 3.1.

3-2 Basic Electrical Characteristics

Basic electrical characterization was performed on four types of devices fabricated with the DP process, as shown in Figs. 3.5 and 3.6 and denoted as Types A, B, C, and D, respectively. Details about the implant conditions of extension and halo for the four splits of devices are listed in Table 2.1. In brief, Type A has symmetrical S/D extensions, Type B has asymmetrical S/D extensions, Types C and D both have the same symmetrical S/D extensions as that of Type A, but Type C has on-side-only halo while Type D has symmetrical halo.

Figure 3.7 shows the CV curves of the PMOSFET measured at 100 kHz. The electrical effective oxide thickness (EOT) is 4.2 nm as estimated from the inversion

capacitance, in good agreement with the physical thickness of 3.5 nm. The result also indicates that the poly depletion effect is negligible.

3-2-1 Electrical Characteristics of P-channel MOSFETs with Asymmetric S/D Extension

In this section, we analyze and compare the electrical characteristics of Type A and Type B shown in Figs. 3.5 (a) and (b), respectively.

As transistors are made smaller, the junctions that form the source and drain regions of the transistor must be made shallower in order to improve performance and provide adequate breakdown characteristics. In particular, the region known as the drain extension must be extremely shallow to suppress the short-channel effects. Figures 3.8(a) and (b) show and compare the transfer and output characteristics, respectively, of Type A and Type B devices with channel length of 0.1 μm and width of 10 μm. With a shallower drain extension in the Type-B device, we can see in Fig. 3.8(a) that subthreshold swing of this device is slightly improved as compared with the Type-A sample. Nonetheless, the shallower drain also introduces additional resistance, resulting in degraded drive current performance illustrated in Fig. 3.8(b). Impact of the increased series resistance also reflects on the transconductance (gm) performance, as shown in Fig. 3.9.

We also inspect threshold voltage (V_{th}) as a function of channel length with the results shown in Fig. 3.10. V_{th} is defined as the gate voltage at drain current of

(W/L) · 10nA, where L is the channel length and W is the channel width. The figure shows that one of the familiar short-channel effects, the V_{th} roll-off phenomenon, owing to the charge sharing at source and drain junctions [25]. While the drain extension becomes shallower for the Type B split as compared with the Type A, the roll-off is improved due to the decreased depletion region which reduces the charge sharing effect.

Figure 3.11 shows the extracted external S/D resistance of the two types of devices. Extraction of the parameter is based on the method proposed and developed previously [25]. From the results, we confirm that the shallower junction indeed results in a larger parasitic resistance,.

3-2-2 Electrical Characteristics of P-channel MOSFETs with Halo-implant

In this section, we compare and analyze the electrical characteristics of Type A, Type C, and Type D devices shown in the Fig. 3.5(a), Fig. 3.6(a), and Fig. 3.6(b), respectively. Major differences among those types of devices are the implementation of halo.

Figures 3.12, 3.13, 3.14 show the transfer characteristics of Types A, C, and D devices, respectively, with various channel length ranging from 80 nm to 10 μm. When the channel length scales down to 80 nm, although the use of halo implemented in Types C and D is useful, the flow of bulk punchthrough current

becomes obvious and results in degradation of subthreshold characteristics in the devices This indicates the S/D extension condition used in the fabrication of these types of devices needs further optimization. The device characterized in Fig. 3.2 was fabricated with a shallower drain extension as compared with the Types, A, C, and D devices, and drain-side-only halo. As a result, the bulk punchthrough is dramatically suppressed.

Figure 3.15 shows and compares the V_{th} roll-off characteristics of the three splits of devices with channel length ranging from 0.1 to 10 μm. We can observe that devices with halo shows improved control over short-channel effect, especially for the Type D devices which have symmetrical halo. This is reasonable since halo increases the substrate doping locally near the edge of the channel. Figure 3.16 shows the DIBL effects. While a high drain bias is applied to the short-channel device, the depletion region of the drain junction further penetrates into the channel, leading to lowering of potential barrier height at channel surface [25]. In the figure it is clearly seen that the implementation of halo can reduce DIBL significantly, especially for the Type-D split. Nonetheless, the halo may degrade the drain current due to degradation carrier mobility in the channel [25]. Figure 3.17 shows that the on-current of devices as a function of the channel length. It can be seen that the Type D and Type A devices have the lowest and the

highest current, respectively. With one-side-only halo, Type C devices show improved performance as compared with the Type D ones.

3-3 Negative Bias Temperature Instability Characteristics

Negative Bias Temperature Instability (NBTI) in PMOS transistors has become a significant reliability concern in present day digital circuit design, because of the use of ultra-thin gate oxides as well as the rise in operation temperature.

In general, the standard reaction-diffusion (R-D) model [29] is used to explain NBTI phenomenon. The physical model is based on modification in structure of the SiO_2/Si interface due to electrochemical reactions during the stress, as schematically depicted in Fig. 3.18. The mechanism of NBTI electrochemical reactions is given as follows:

$$Si_3 \equiv SiH + p^+ \leftrightarrow Si_3 \equiv Si^* + H^+, \tag{3-1}$$

$$O_3 \equiv SiH + p^+ \leftrightarrow O_3 \equiv Si^+ + H, \tag{3-2}$$

where $\equiv SiH$ is a hydrogenated trivalent silicon, p^+ is a hole at the silicon surface, and $Si_3 \equiv Si^*$ is an interface trivalent silicon atom (Nit) with an unsaturated (unpaired) valence electron (a dangling bond) at the Si–SiO_2 interface, H^+ is a positively charged interstitial hydrogen ion, and $O_3 \equiv Si^+$ is a positive fixed oxide charge (N_{ox}) in the oxide. Therefore, Equation (3-1) is used to explain for Nit generation while Equation

(3-2) for N_{ox} generation. It should be noted here that (3-1) and (3-2) are reversible. NBTI effect damages the PMOSFETs by causing the shift of V_{th}, and the degradation of saturation current and transconductance. V_{th} shifts during NBT stress are modeled by considering the generation of interface defects [30] and the generation of positive charges relating to the diffusion of released hydrogen into the gate dielectric [31], induced by the injection of holes presenting at the interface. NBT stress causes a negative shift of V_{th} (ΔV_{th}) that shows a power-law dependence on stress time:

$$\Delta V_{th} = A * t^{n}, \tag{3-3}$$

where A is a constant and t is the stress time. The exponential value, n, of the power-law equitation is around 0.25 when diffusion-controlled electrochemical reactions are considered [32, 33].

In this thesis we also investigate the static NBTI of the fabricated p-MOS devices. Figure 3.19 shows and compares the V_{th} shift-versus-stress time curves at 125°C for Type A devices with various channel length of 0.14 μm, 1μm and 10 μm. We can observe that, at a fixed stress time, the Vth shift is larger for the device with a longer length. For the above channel length-dependent NBTI phenomenon, fluorine atom incorporation may play a role. Note that, in these devices, gate and S/D were doped with BF_2^+ implant. It has been shown previously that improvement in interfacial stability can be achieved with F incorporation, attributing to relaxation of the strain at

the interface or replacement of the Si–H bonds with the more robust Si–F bonds [34]. Moreover, additional fluorine atoms diffusing from the gate-S/D extension overlap regions to the channel region alleviate the distortion of the strained Si–O–Si or Si–N–Si bonds and reduce the interface states and fixed oxide charges in the fabrication process [35]. Consequently, the short-channel devices may have more Si-F bonds at Si/SiO_2 interface in the channel as compared with the long-channel ones, as indicated in Fig 3.20, because of the shorter distance between the channel center and the S/D extension. Figure 3.21 shows that subthrehold characteristics for Type A devices with channel length of 0.14 μm and 10 μm measured at 125°C, 25°C, before and after stress under gate voltage -3.3 V for 5000 seconds. As shown in Fig. 3.21, we can see that the SS is slightly smaller for the short-channel device before stress, while the difference becomes even larger after stress. This evidences the effect of fluorine atoms from S/D extension in reducing the interface states and improving the NBTI immunity for the short-channel device as compared with the long-channel one. As a result, long-channel devices have more interface states, which the distance between the channel center and the S/D extension of device is too long to generate more Si-F bonds at Si/SiO_2 interface in the channel, exhibit a larger value of ΔV_{th} under NBTI stressing.

Figure 3.22 shows and compares the ΔV_{th} -versus-stress time curves for Type A

device with channel length of 0.14 μm stressed at 25°C, 75°C and 125°C. Figure 3.23 shows and compares the Vth shift-versus-stress time curves for Type A device at 125°C and channel length 0.14 μm with various stress gate voltage -2.3V, -2.8V, and -3.3V. We can observe that a higher temperature or gate voltage shows higher V_{th} shift. While NBT stress at higher temperature, it may accelerate the release of hydrogen from the interface by breaking the Si-H bonds and form H^+ (see (3-1)) [29]). It may also accelerate the hydrogen ions diffusion away from the interface into the oxide bulk where some are trapped, causing more V_{th} shift. Figure 3.24 shows and compares the ΔV_{th}-versus-stress time curves for Type A and Type D devices with channel length of 0.14 μm at 25°C, 75°C and 125°C. Figure 3.25 shows and compares the ΔV_{th}-versus-stress time curves for Type A and Type D devices at 125°C and channel length of 0.14 μm with various stress gate voltage -2.3V, -2.8V, and -3.3V. Basically the difference between the two splits of devices is small, indicating that the implementation of the halo in the devices would not results in a great impact.

Chapter4 Conclusion and Future Work

4-1 Conclusions

In this thesis, we have successfully fabricated and studied p-channel MOSFETs with channel length down to 85 nm with an I-line double patterning process. Evaluation and comparison of device characteristics among different splits of devices having symmetric or asymmetric S/D extension and halo structures have also been done. Several results are summarized as follows:

1. Capability of the developed double patterning process in forming asymmetrical S/D structure is demonstrated. Devices with a shallower extension depth can help alleviate the short-channel effects such as V_{th} roll-off and bulk punchthough. Nonetheless, it may also introduce additional resistance, resulting in degraded drive current performance.

2. Devices with halo-implanted structures can improve DIBL effect as well as bulk punchthough. This is reasonable since halo increases the substrate doping locally near the edge of the channel to suppress the depletion region of the drain junction and thus prevent further penetration of electric field into the channel. However, the halo may degrade the drain current due to degraded carrier

mobility in the channel.

3. PMOSFETs' NBTI results show that NBT stress aggravates characteristics of devices. While stress at a higher temperature, it may accelerate the release of hydrogen from the interface by breaking the Si-H bonds. It may also accelerate the hydrogen ions diffusion away from the interface into the SiO_2 where some are trapped, causing more V_{th} shift. However, as compared with the long-channel devices, the short-channel devices show less ΔV_{th} under NBTI stressing. This is attributed to the formation of more Si-F bonds at Si/SiO_2 interface in the channel due to the diffusion of fluorine atoms from the S/D extension, thus reducing the interface states and improving the NBTI immunity. Because of a much shorter distance for the above diffusion process, the short-channel devices exhibit a much improved immunity than the long-channel ones. Furthermore, a comparison has been made between the devices with and without halo implemented. The results indicate that the implementation of the halo in the devices would not result in a great impact as long as NBTI stressing is concerned.

4-2 Future Work

There are some important and interesting topics that are valuable for the future study regarding PMOSFETs with double patterning technique:

1. In order to reduce the bulk punchthrough and DIBL effects, it is important to optimize the conditions of halo implantation and S/D junction regions by using TCAD simulation.

2. To raise the output current, we can use silicide to decrease junction resistance.

3. Beside NBTI, we can measure channel hot carrier (CHC) and drain avalanche hot carrier (DAHC) to analyze devices characteristics.

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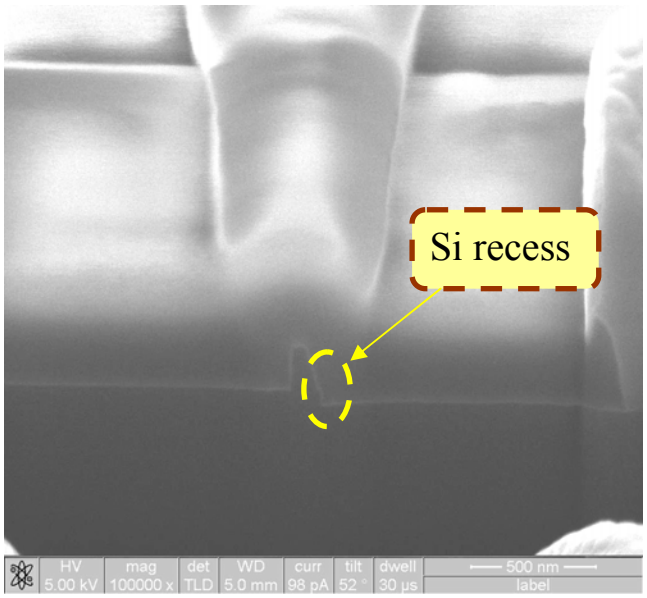
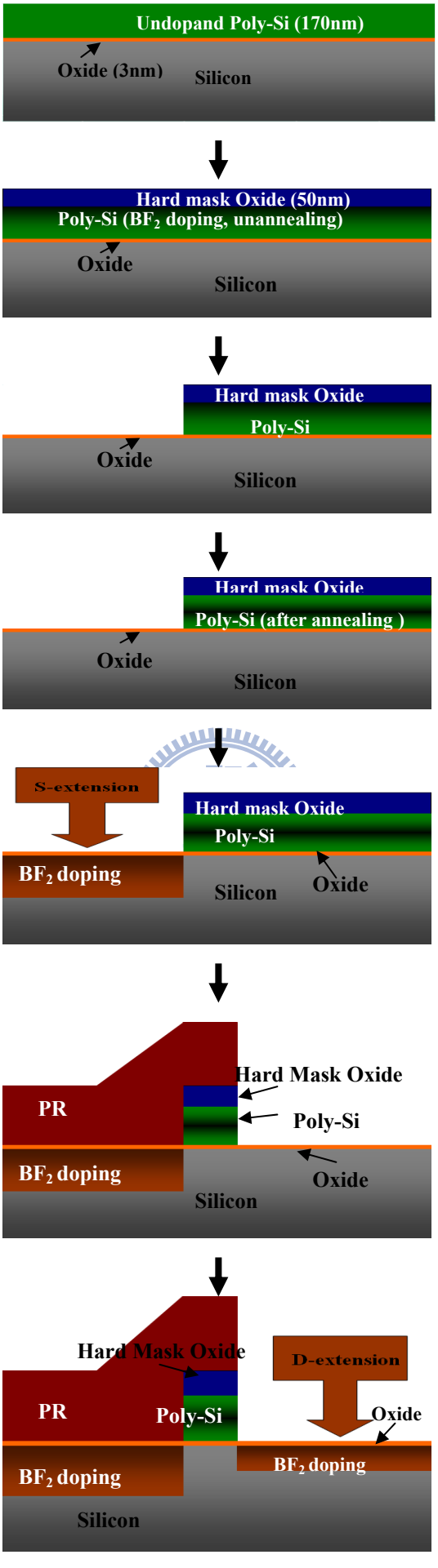


Fig.1.1. Cross sectional view of a device with nominal gate length (L_{mask}) of 0.2 μ*m* fabricated with I-line DP process developed by our group in previous year [1]. Si recess resulted in the 2nd poly etch step was found at one side of the gate.


Undopand Poly-Si (170nm)
Oxide (3nm)
Silicon
Hard mask Oxide (50nm)
Poly-Si (BF_2 doping, unannealing)
Oxide
Silicon
Hard mask Oxide
Poly-Si
Oxide
Silicon
Hard mask Oxide
Poly-Si (after annealing)
Oxide
Silicon
S-extension
Hard mask Oxide
Poly-Si
BF_2 doping
Silicon
Oxide
Hard Mask Oxide
PR
Poly-Si
BF_2 doping
Oxide
Silicon
Hard Mask Oxide
D-extension
PR
Poly-Si
Oxide
BF_2 doping
BF_2 doping
Silicon

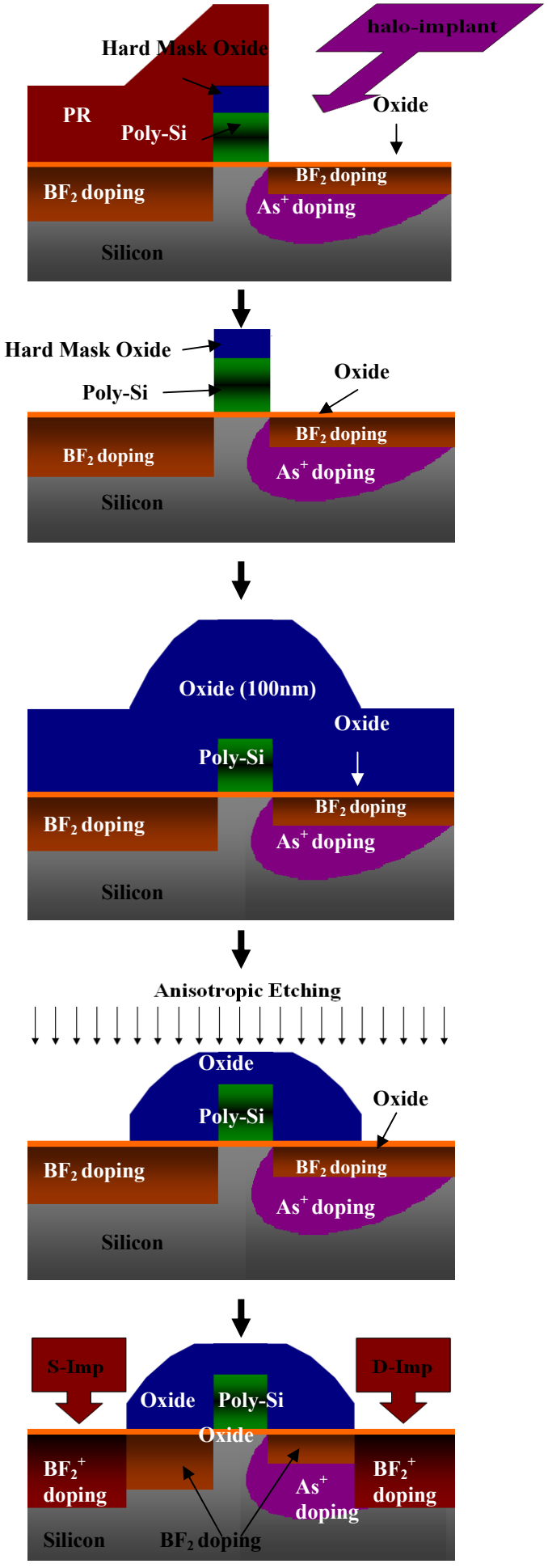
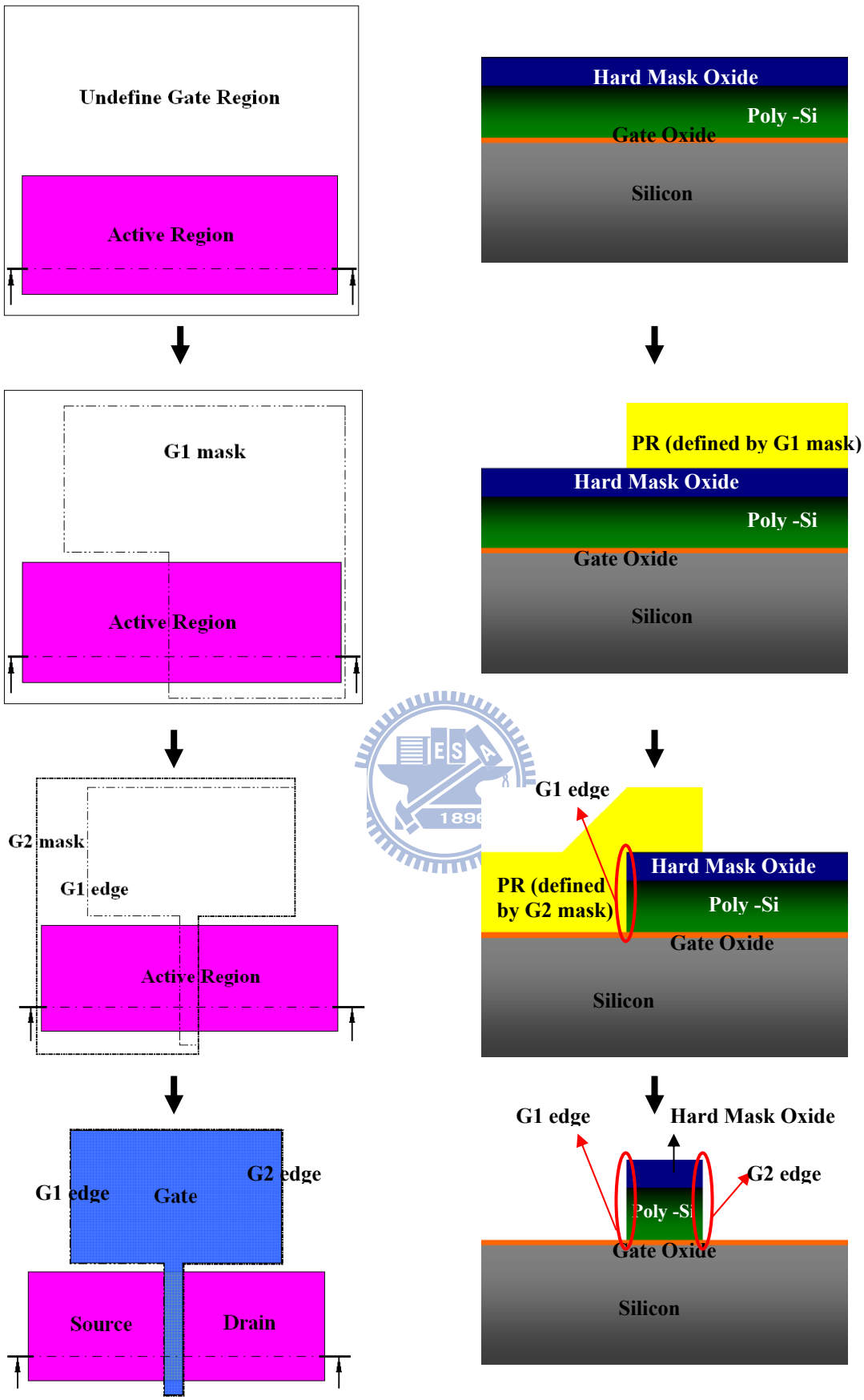
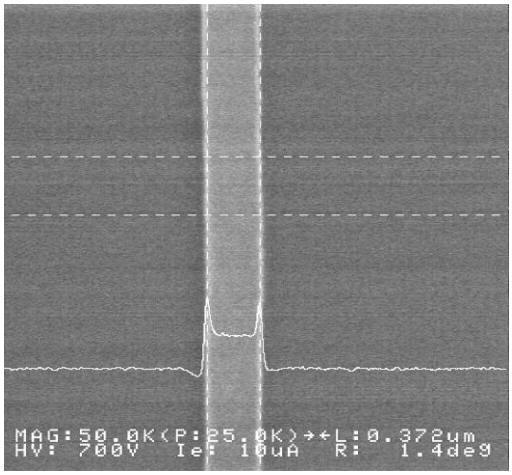


Fig. 2.1. Process flow of asymmetric extension PMOSFETs with drain-side halo-implantation.



(a) Top view (b) Cross-section view

Fig.2.2. Design of the double-patterning masks, (a) Top view and (b) Cross-sectional view.



Type: Single Patterning

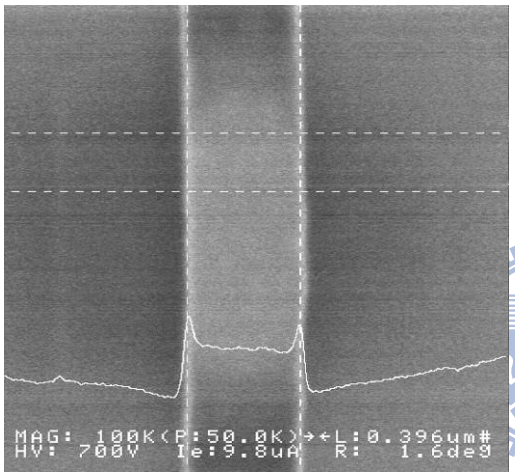
$L_{mask} = 0.35\,\mu m$

$L_{gate} = 0.372\,\mu m$

$Error = -0.022\,\mu m$

$Error\ \% = 6.286\,\%$

(a)



Type: Single Patterning

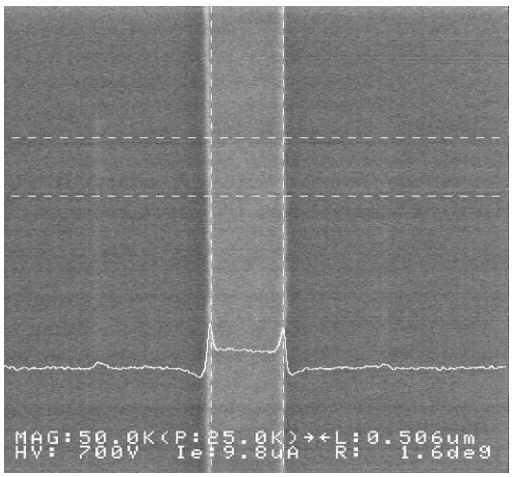
$L_{mask} = 0.40\,\mu m$

$L_{gate} = 0.396\,\mu m$

$Error = 0.004\,\mu m$

$Error\ \% = 1\,\%$

(b)



Type: Single Patterning

$L_{mask} = 0.50\,\mu m$

$L_{gate} = 0.506\,\mu m$

$Error = -0.006\,\mu m$

$Error\ \% = 1.2\,\%$

(c)

Fig. 2.3. Top-view SEM images of poly-Si gates formed by single patterning process.

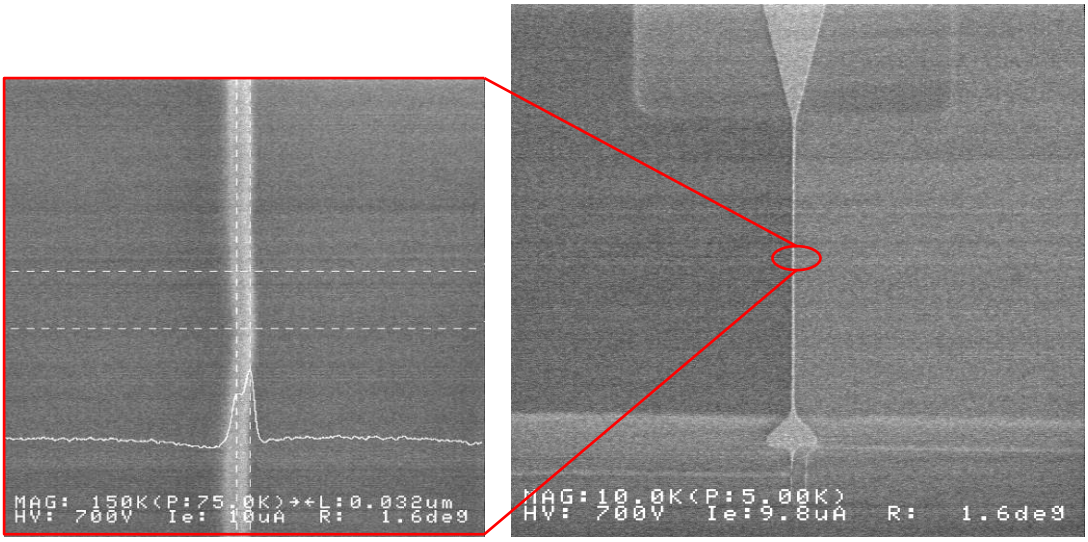
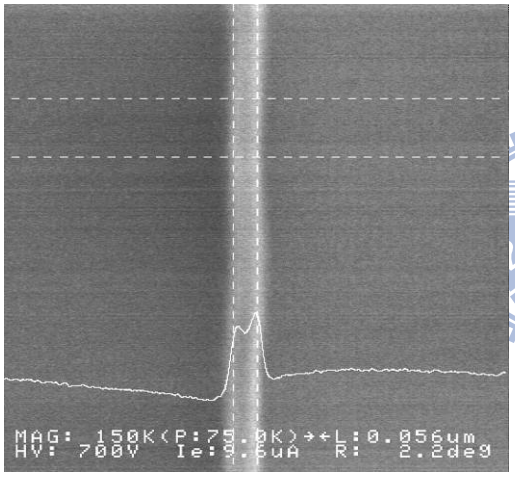


Fig 2.4. SEM image of a poly-Si gate with 32 nm in line width, formed by DP process with designed line width of 50 nm.



Type: Double Patterning

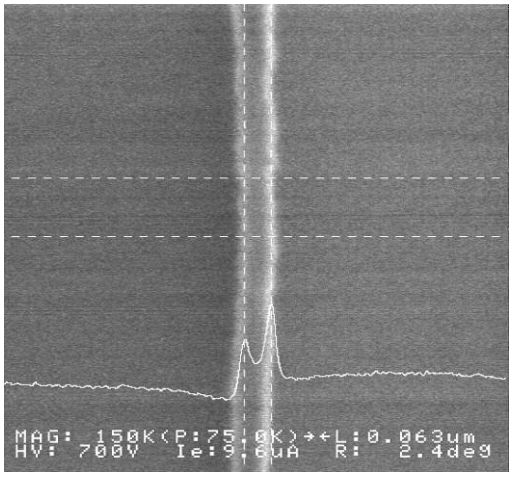
$L_{mask} = 0.05\,\mu m$

$L_{gate} = 0.056\,\mu m$

$Error = -0.006\,\mu m$

$Error\ \% = 12\,\%$

Fig. 2.5. Top-view SEM image of a poly-Si gate with designed line width of 50 nm formed by double patterning process.



Type: Double Patterning

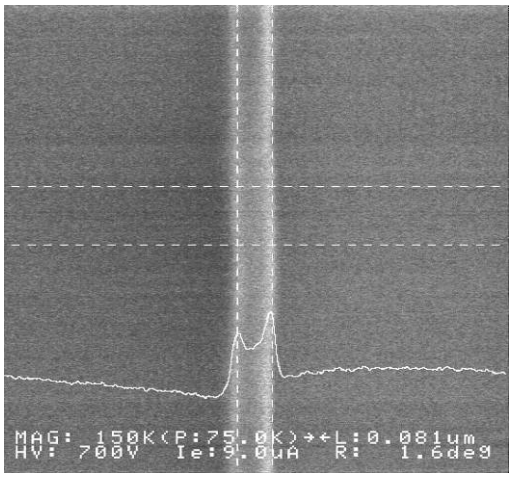
$L_{mask} = 0.06\,\mu m$

$L_{gate} = 0.063\,\mu m$

$Error = -0.003\,\mu m$

$Error\ \% = 5\,\%$

Fig. 2.6. Top-view SEM image of a poly-Si gate with designed line width of 60 nm formed by double patterning process.



Type: Double Patterning

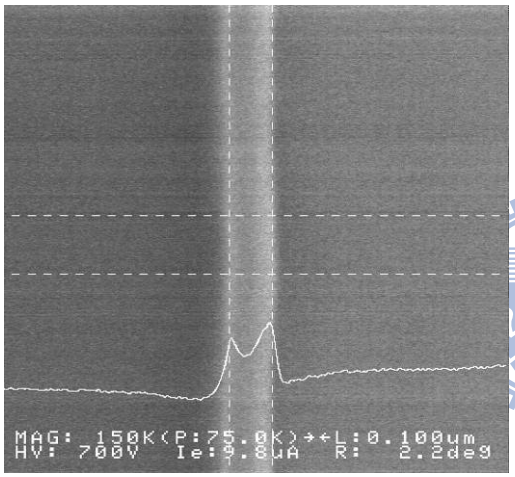
$L_{mask} = 0.08\,\mu m$

$L_{gate} = 0.081\,\mu m$

$Error = -0.001\,\mu m$

$Error\ \% = 1.25\,\%$

Fig. 2.7. Top-view SEM image of a poly-Si gate with designed line width of 80 nm formed by double patterning process.



Type: Doble Patterning

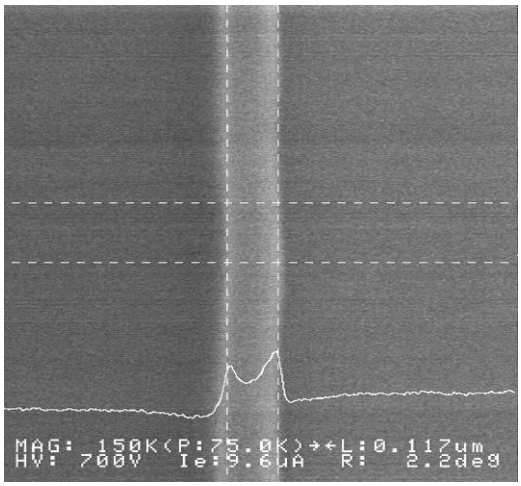
$L_{mask} = 0.10\,\mu m$

$L_{gate} = 0.10\,\mu m$

$Error = 0\,\mu m$

$Error\ \% = 0\,\%$

Fig. 2.8. Top-view SEM image of a poly-Si gate with designed line width of 0.1 μm formed by double patterning process.



Type: Double Patterning

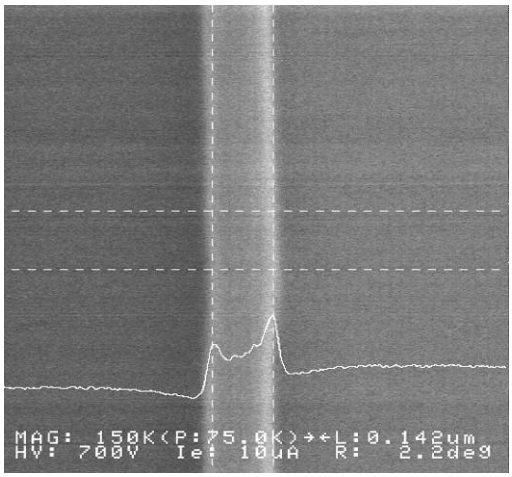
$L_{mask} = 0.12\,\mu m$

$L_{gate} = 0.117\,\mu m$

$Error = 0.003\,\mu m$

$Error\ \% = 2.5\,\%$

Fig. 2.9. Top-view SEM image of a poly-Si gate with designed line width of 0.12 μm formed by double patterning process.



Type: Double Patterning

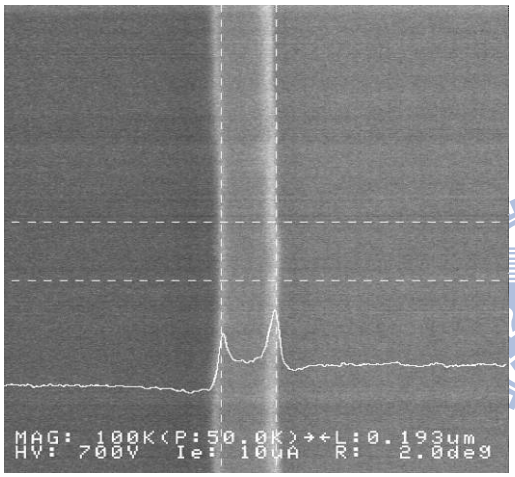
$L_{mask} = 0.14\ \mu m$

$L_{gate} = 0.142\ \mu m$

$Error = -0.002\ \mu m$

$Error\ \% = 1.428\ \%$

Fig. 2.10. Top-view SEM image of a poly-Si gate with designed line width of 0.14 μm formed by double patterning process.



Type: Double Patterning

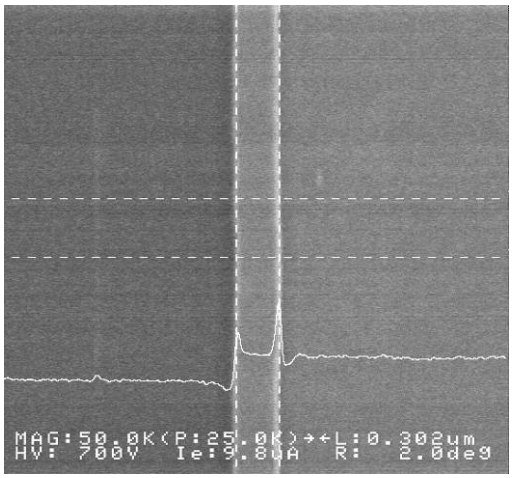
$L_{mask} = 0.20\ \mu m$

$L_{gate} = 0.193\ \mu m$

$Error = 0.007\ \mu m$

$Error\ \% = 3.5\ \%$

Fig. 2.11. Top-view SEM image of a poly-Si gate with designed line width of 0.2 μm formed by double patterning process.



Type: Double Patterning

$L_{mask} = 0.30\ \mu m$

$L_{gate} = 0.302\ \mu m$

$Error = -0.002\ \mu m$

$Error\ \% = 0.667\ \%$

Fig. 2.12. Top-view SEM image of a poly-Si gate with designed line width of 0.3 μm formed by double patterning process.

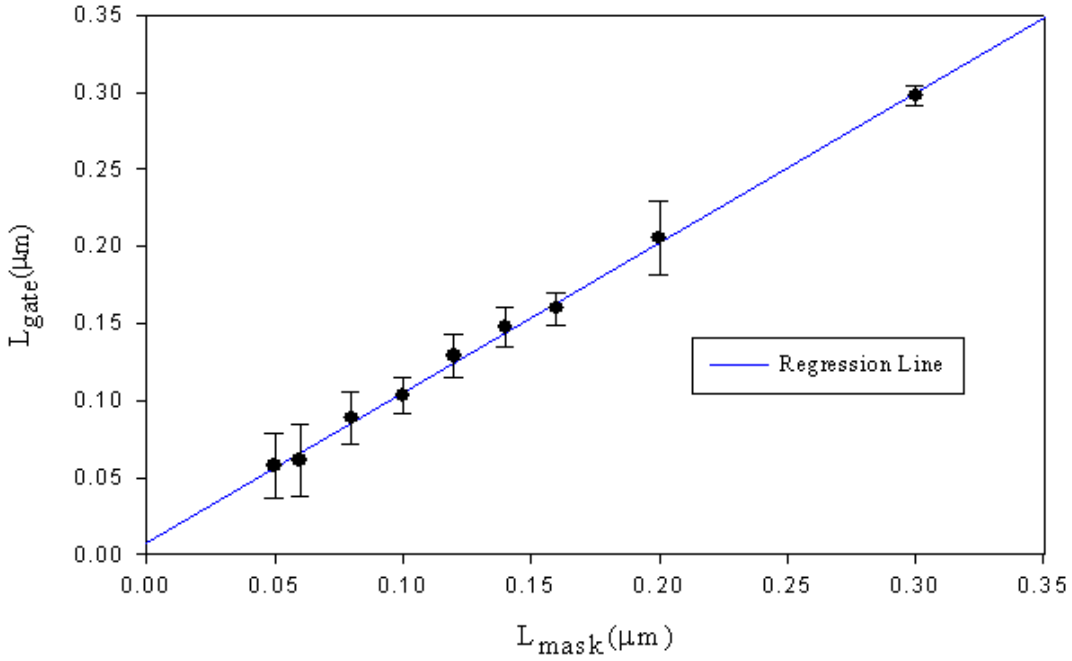


Fig. 2.13. Practical gate length (L_{gate}) extracted by top-view SEM images versus the designed gate length (L_{mask}). The error bar indicates the standard deviation (1-σ) of the measured data.

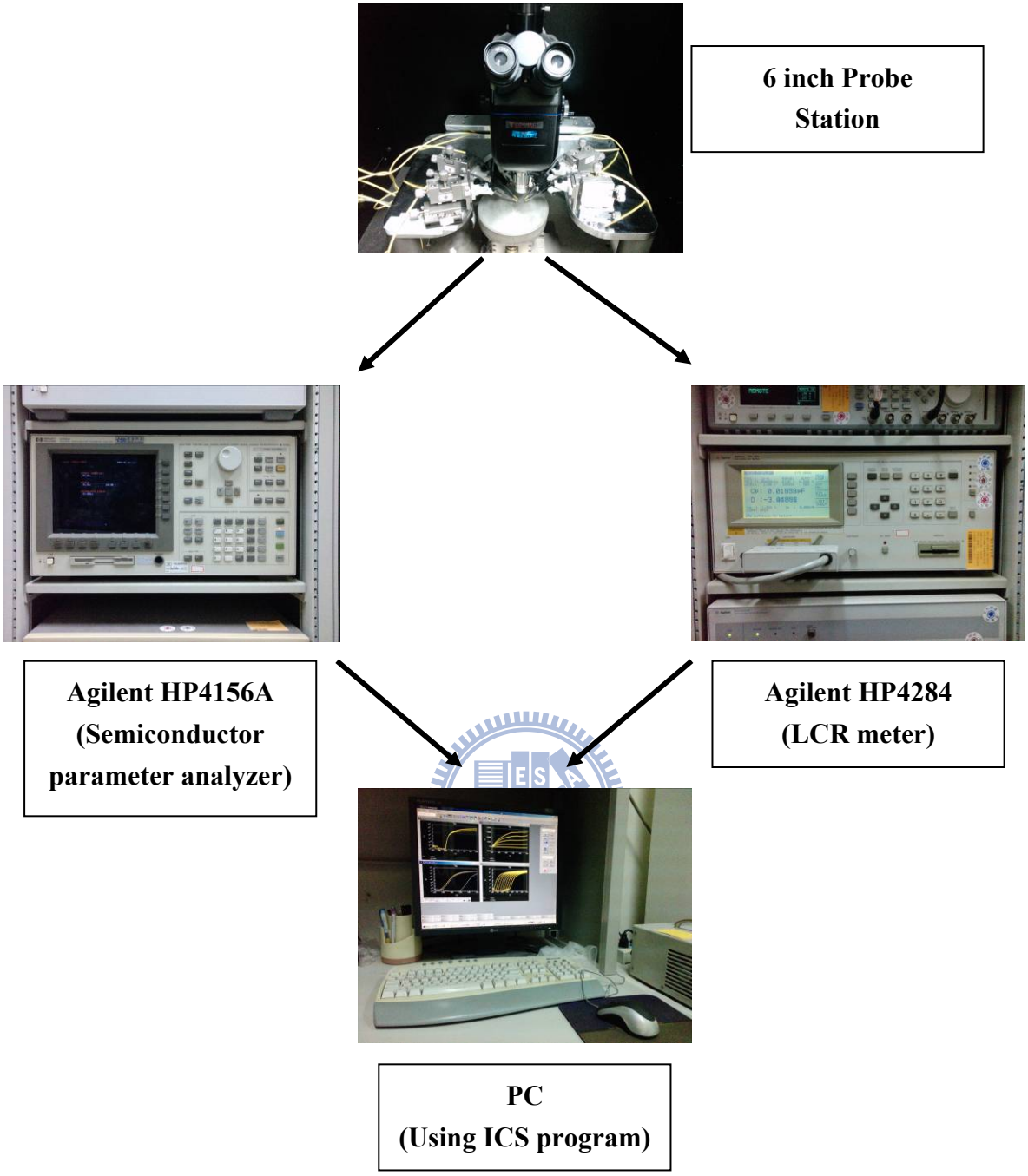


Fig. 2.14 Measurement setup.

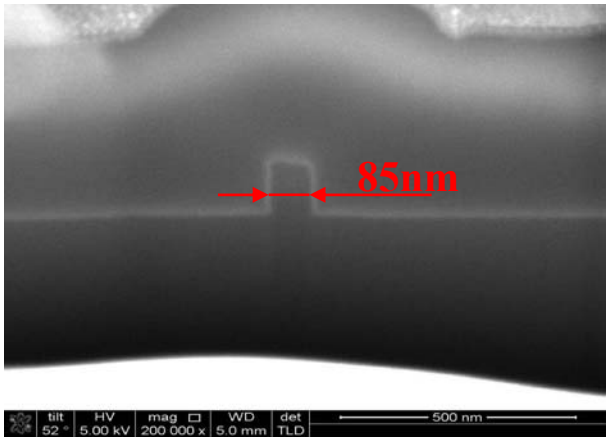
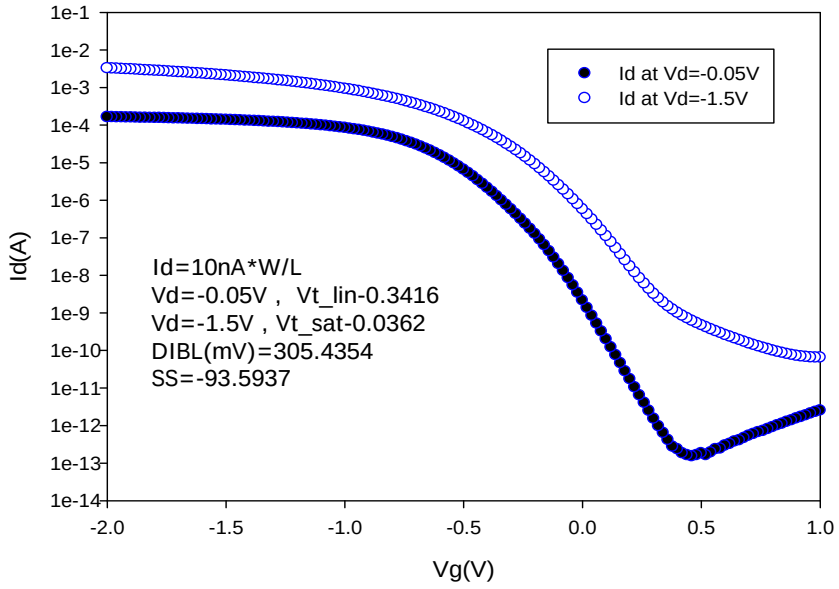
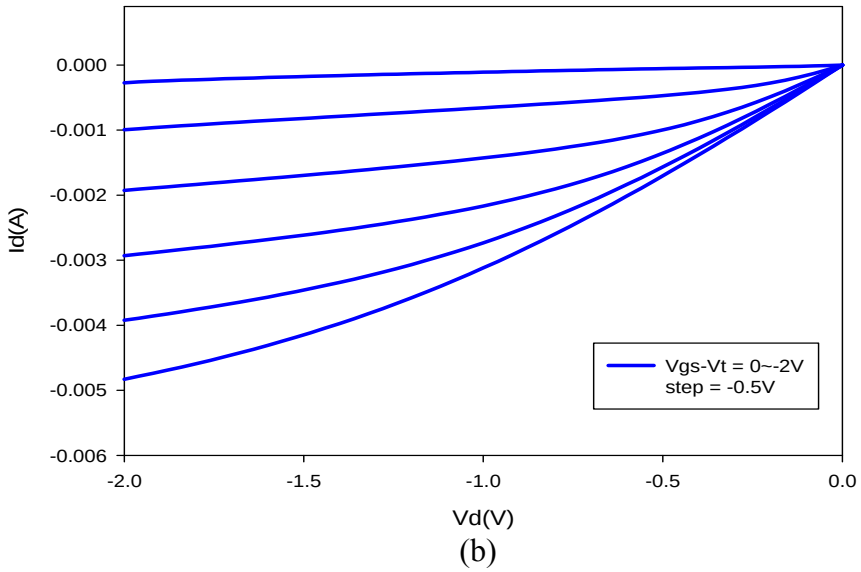


Fig.3.1. Cross sectional view of the DP gate with designed gate length L_{mask} = 0.1 μm.



(a)



(b)

Fig.3.2. Transfer characteristics of (a) I_d-V_g and (b) I_d-V_d with practical gate length of 85 nm and width of 10 μm.

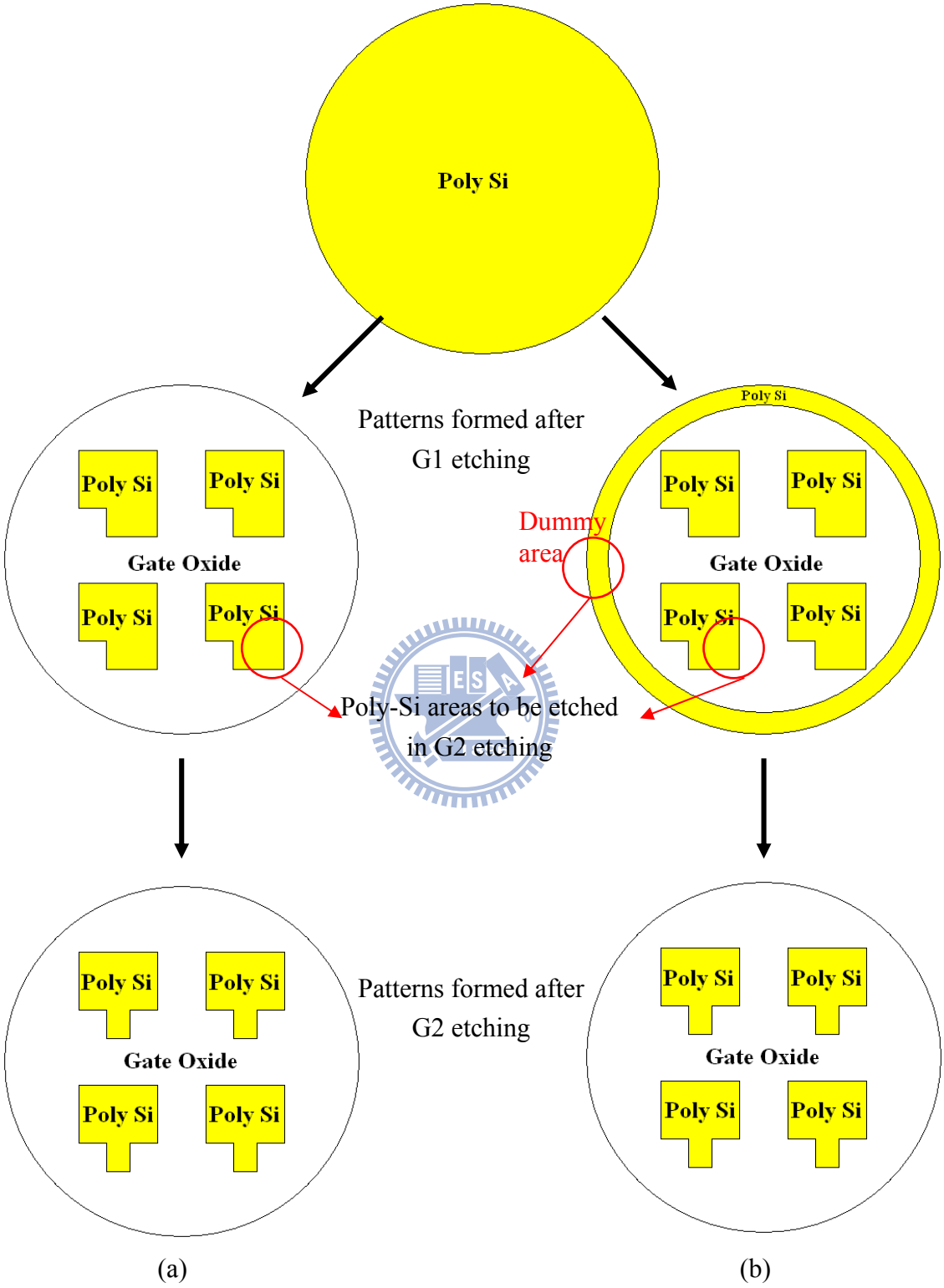


Fig. 3.3. Schematic illustrations of the DP gate patterns formed after G1 and G2 etching steps with (a) old and (b) new G1 mask design.

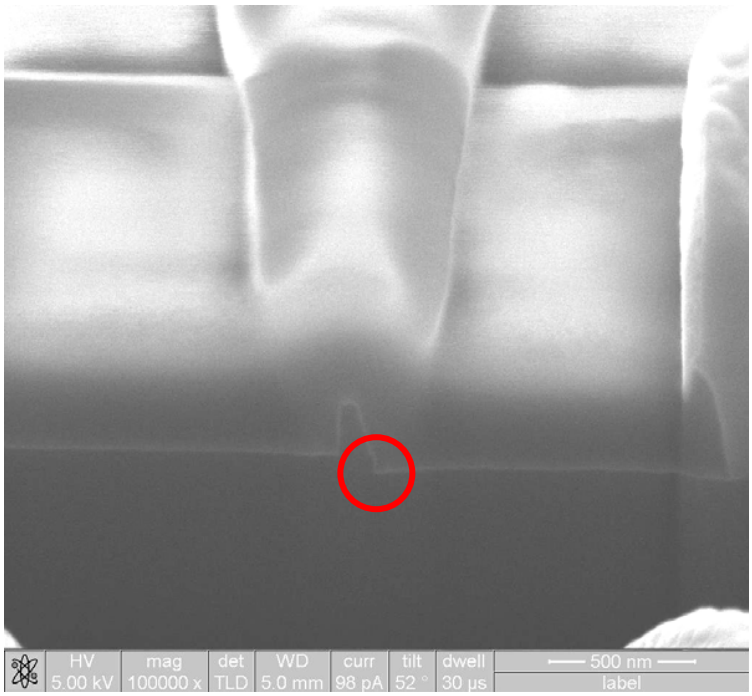
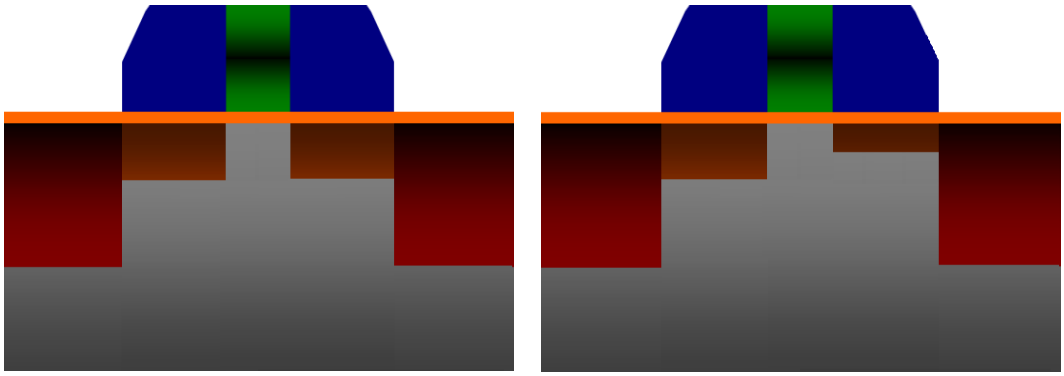
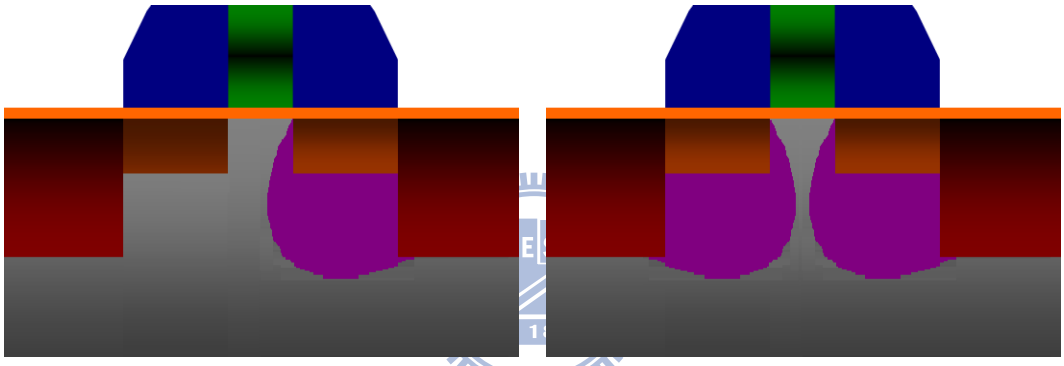


Fig. 3.4. Cross-sectional view of the fabricated MOSFET showing the damaged region caused by the second (G2) etching. [1].



(a) Type A (b) Type B

Fig. 3.5. (a) Type A device serves as the control samples with symmetric S/D. (b) Type B device with shallower drain extension.



(a) Type C (b) Type D

Fig. 3.6. (a) Type C device with drain-side-only halo. (b) Type D device with symmetrical halo.

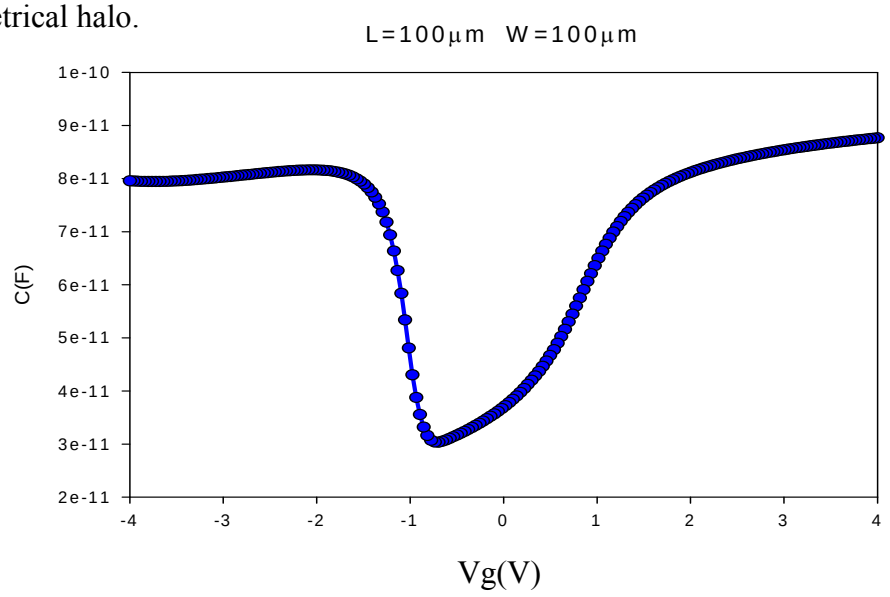
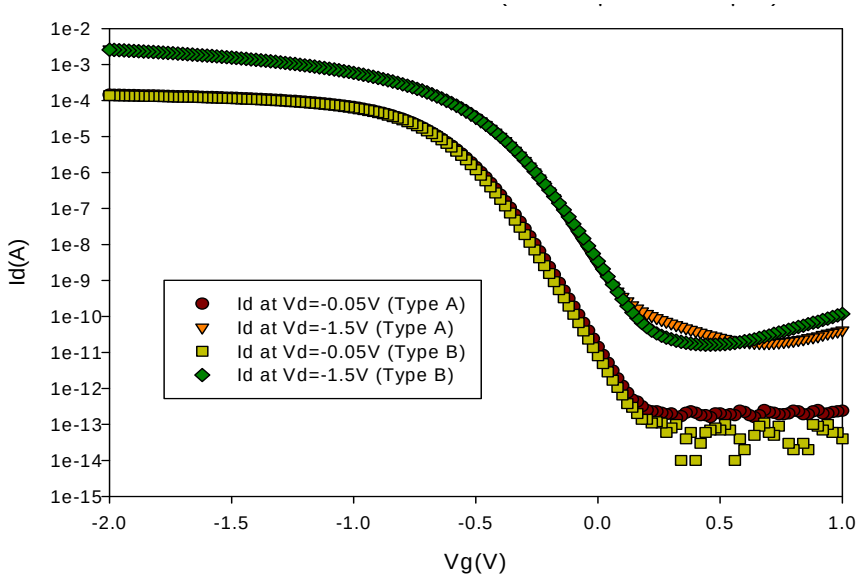
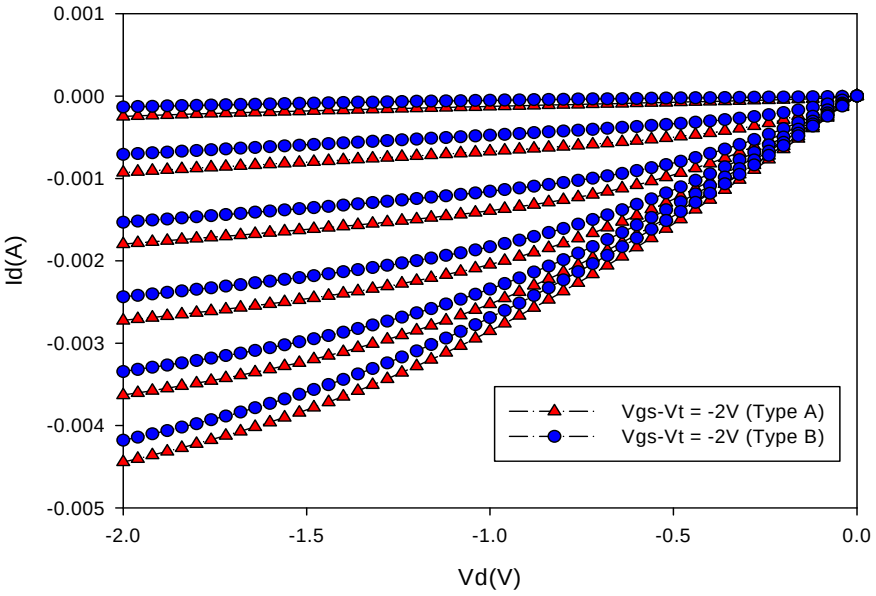


Fig. 3.7. The CV curve of an asymmetric PMOSFET with DP process. The measurement frequency is 100 kHz.



(a)



(b)

Fig. 3.8. (a) Typical transfer and (b) output characteristics of Type A and Type B devices with channel length of 0.1 μm and channel width of 10 μm.

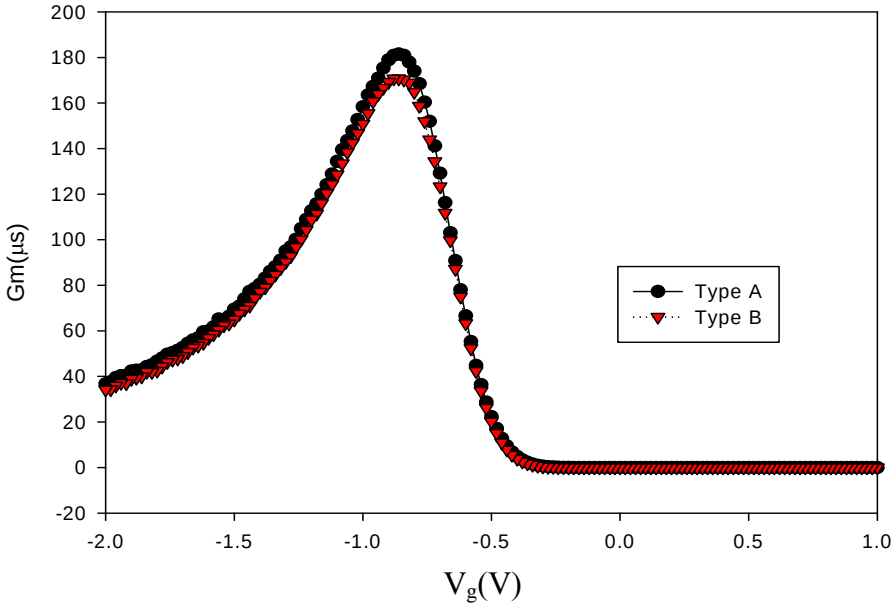


Fig. 3.9. Transconductance (Gm) of Type A and Type B devices with channel length of 0.1 μm and channel width of 10 μm.

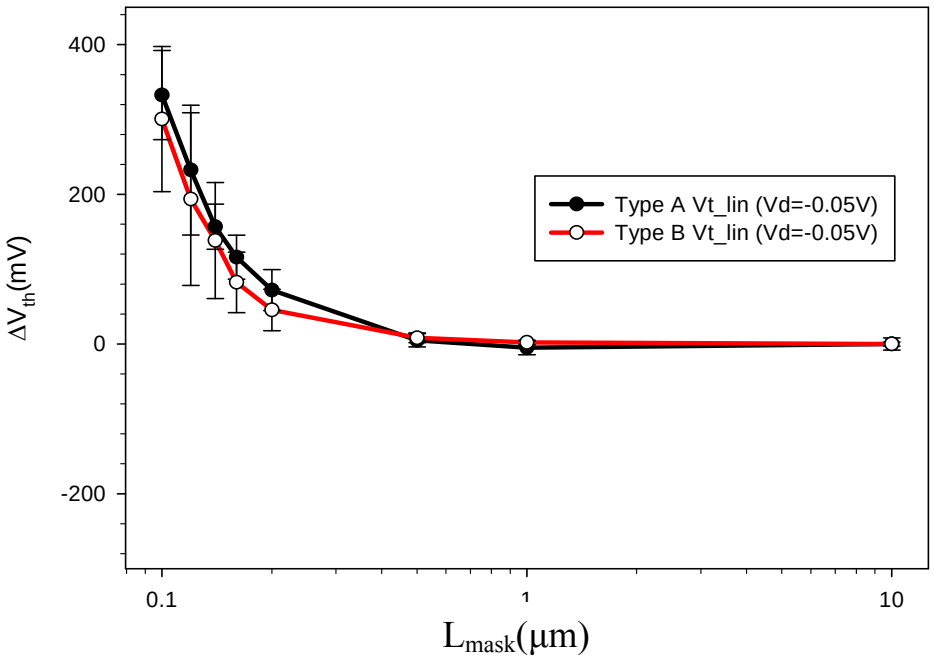
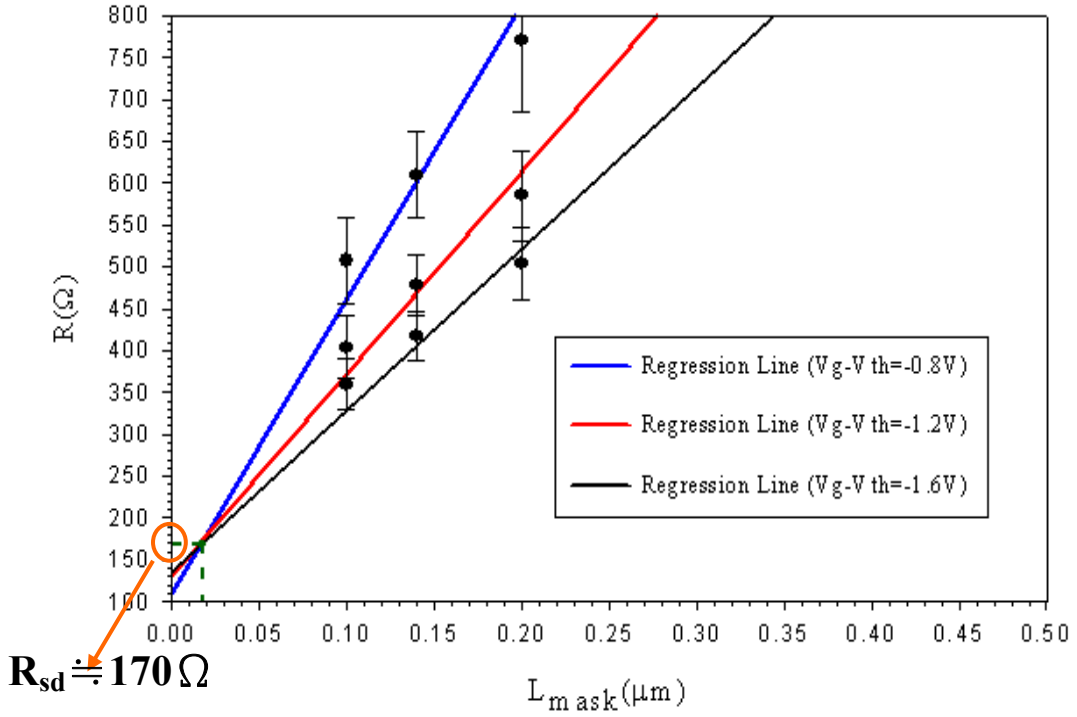
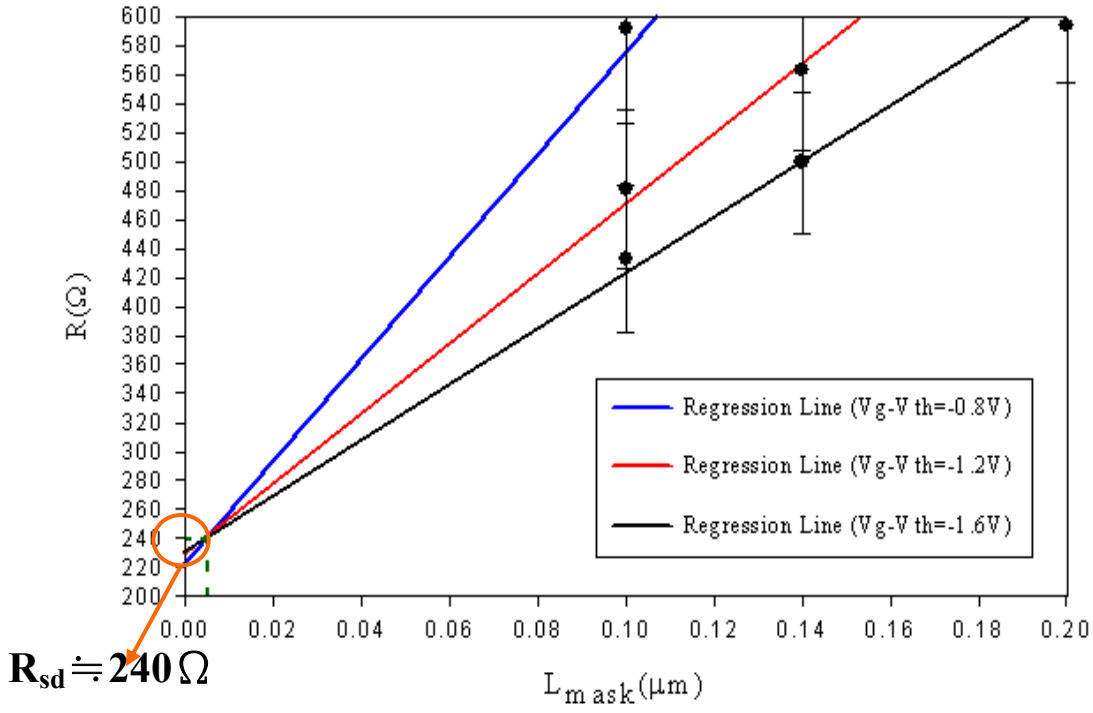


Fig. 3.10. Threshold voltage of Type A and Type B devices as a function of channel length.

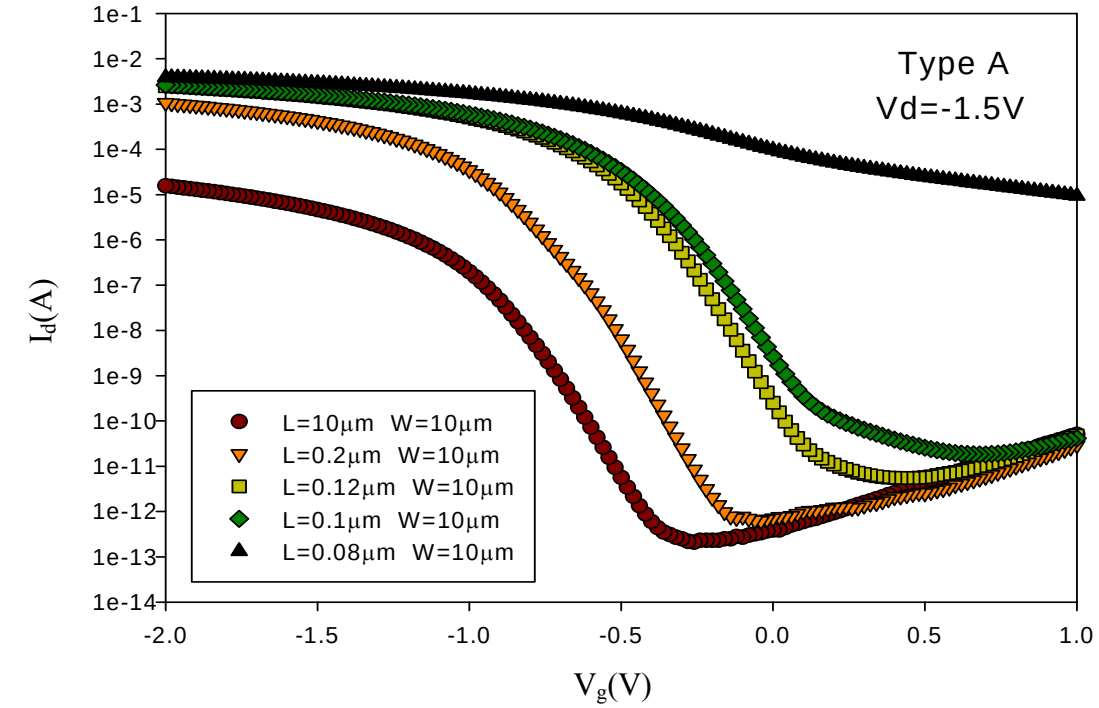


(a)

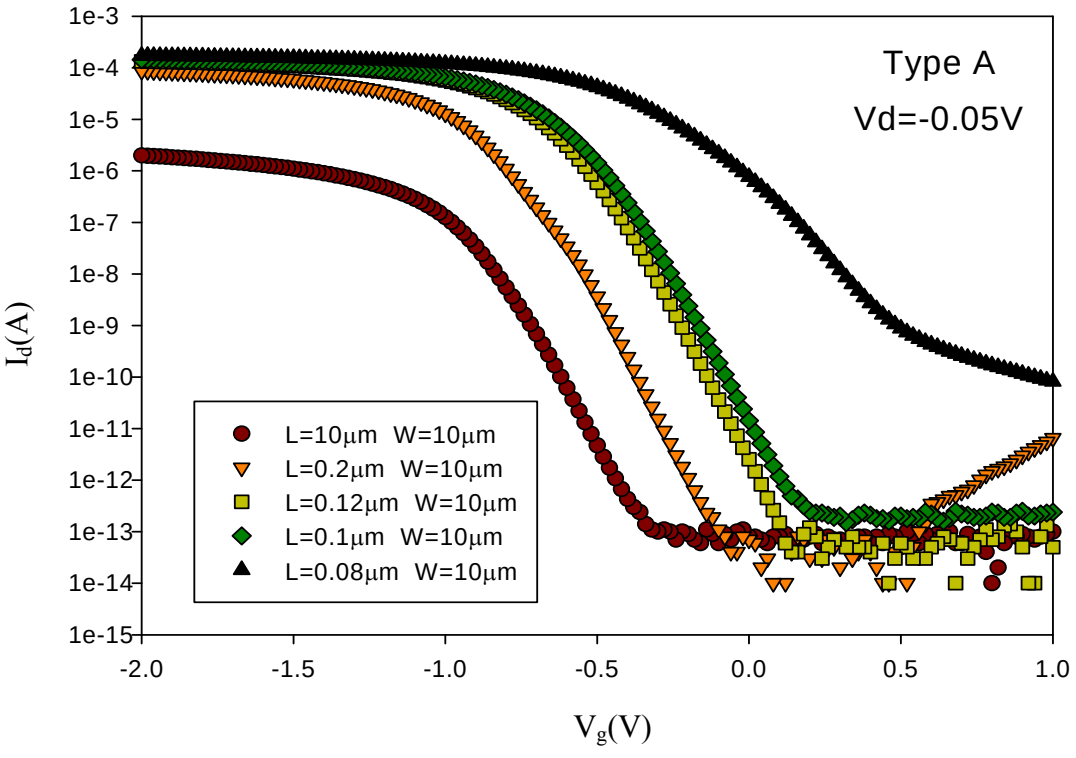


(b)

Fig. 3.11. Extracted values of external S/D resistance of (a) Type A and (b) Type B devices are 170 Ω and 240 Ω, respectively.

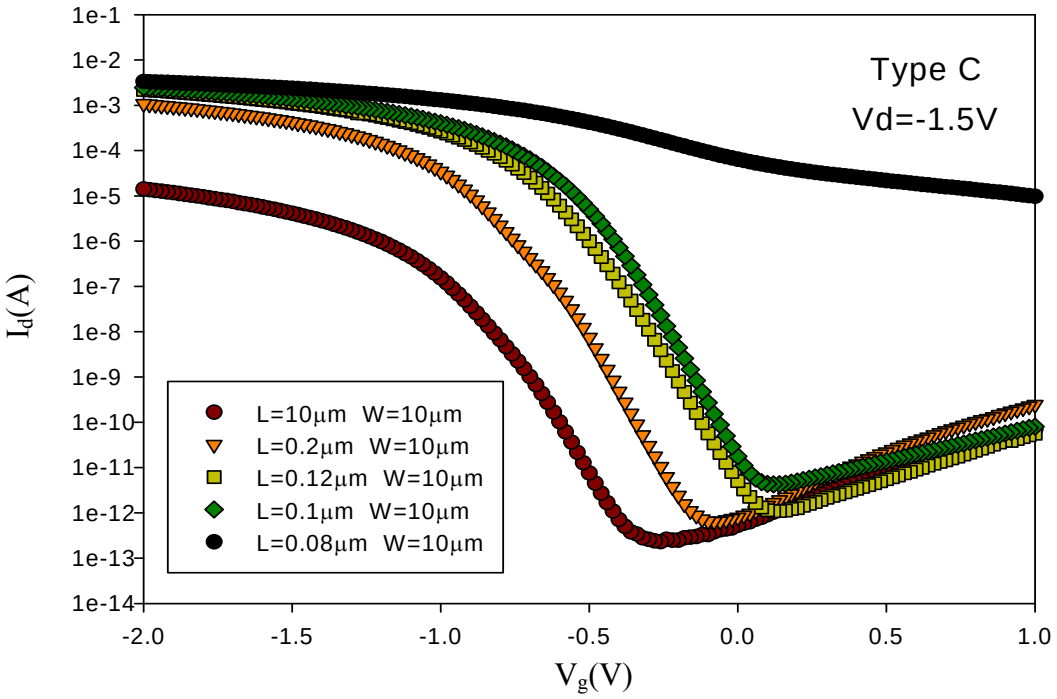


(a)

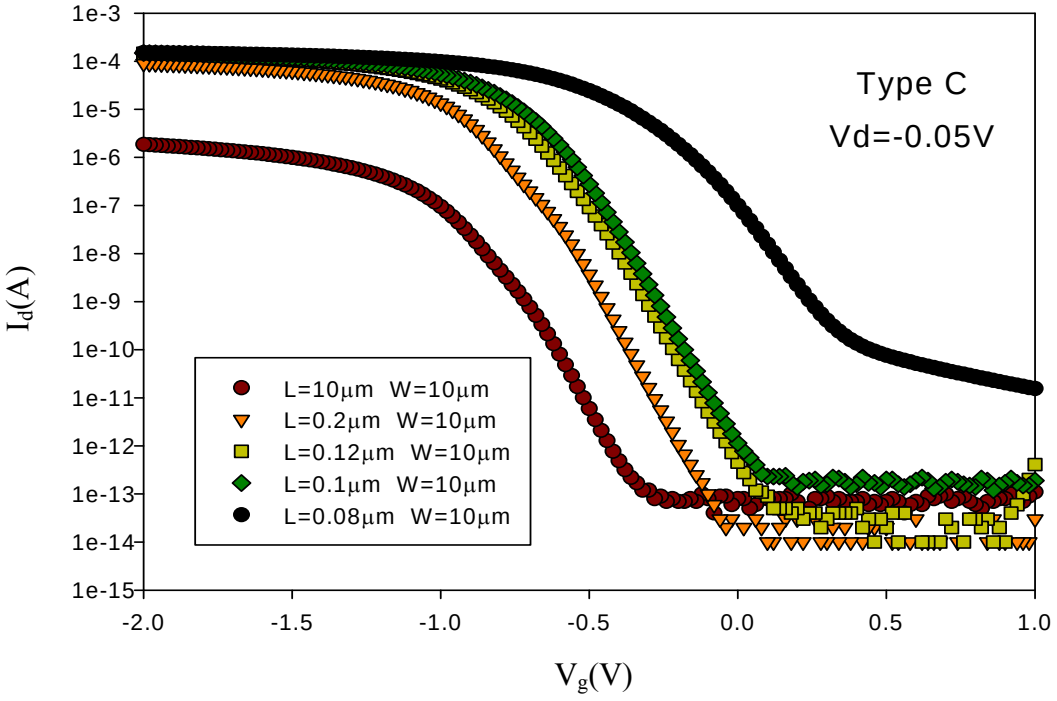


(b)

Fig. 3.12. Transfer characteistics of Type A devices with various channel length ranging from 0.08 to 10 μm. All devices have the same width of 10 μm. (a) V_d =-1.5 V. (b) V_d = -0.05 V.

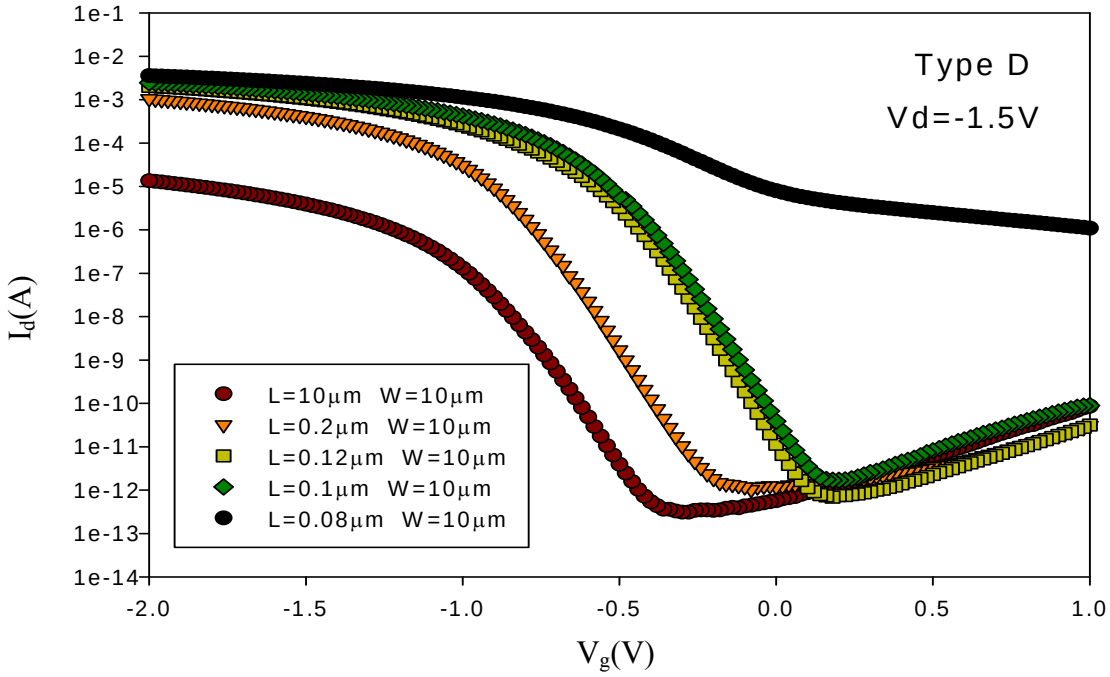


(a)

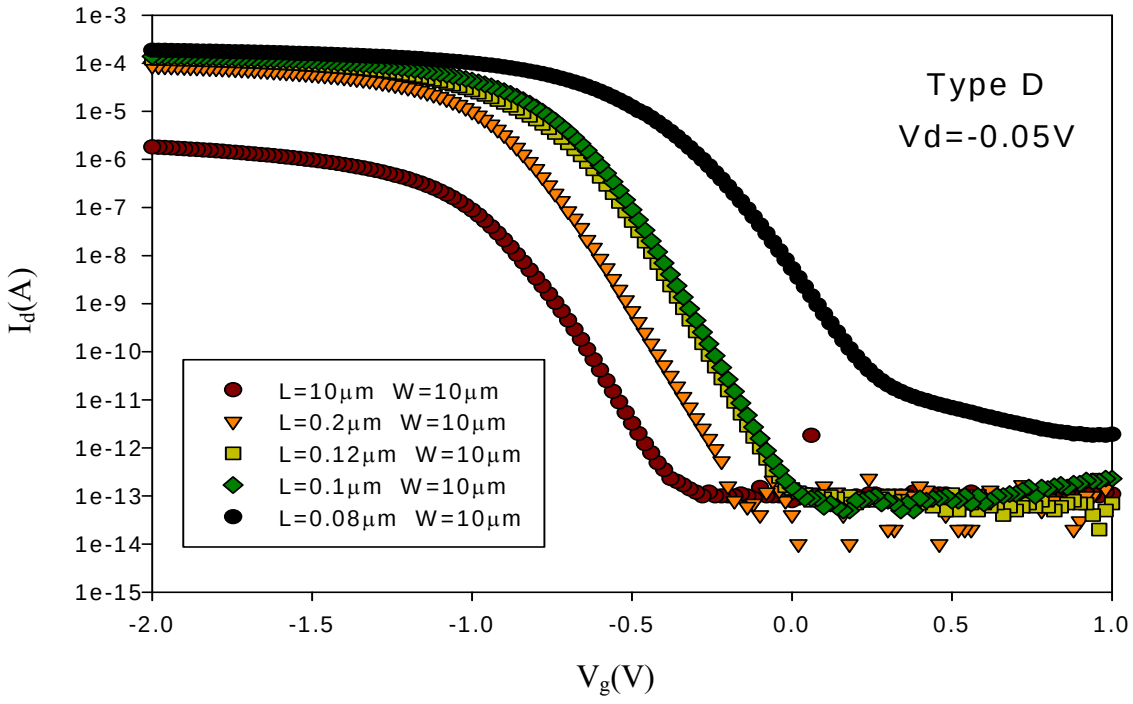


(b)

Fig. 3.13. Transfer characteristics of Type C devices with various channel length ranging from 0.08 to 10 μm. All devices have the same width of 10 μm. (a) V_d =-1.5 V (b) V_d = -0.05 V.



(a)



(b)

Fig. 3.14. Transfer characteristics of Type D devices with various channel length ranging from 0.08 to 10 μm. All devices have the same width of 10 μm. (a) V_d =-1.5 V (b) V_d = -0.05 V.

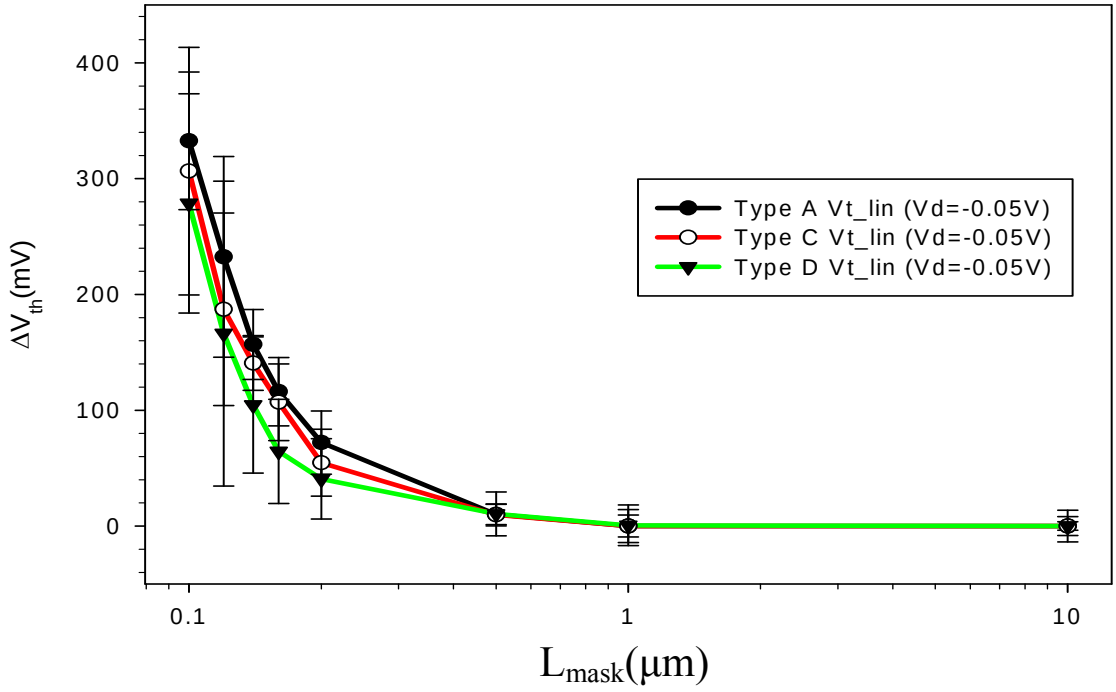


Fig. 3.15. Threshold voltage shift as a function of channel length for Types A, C, and D samples.

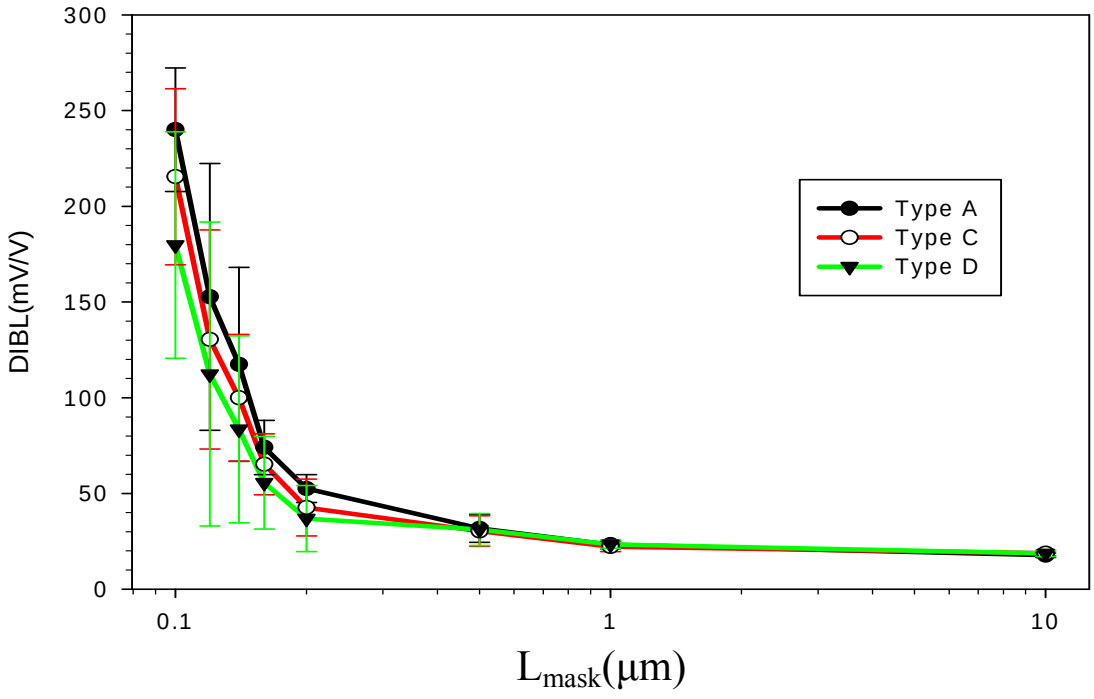


Fig. 3.16. DIBL as a function of channel length for Types A, C, and D samples.

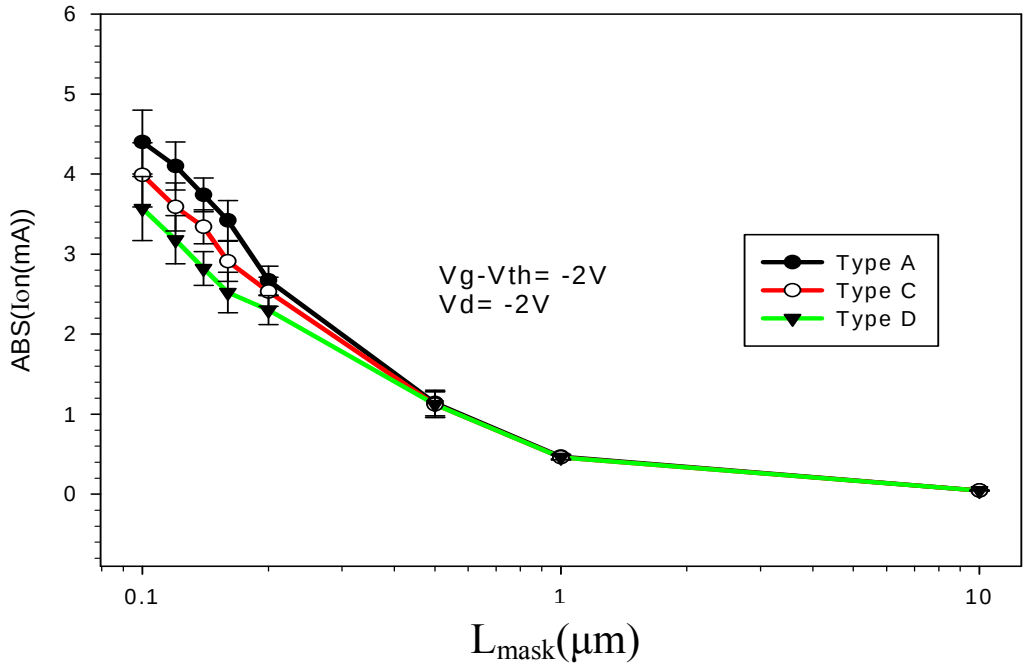


Fig. 3.17. On-current at V_g-V_{th} = -2V as a function of channel length for Types A, C, and D samples.

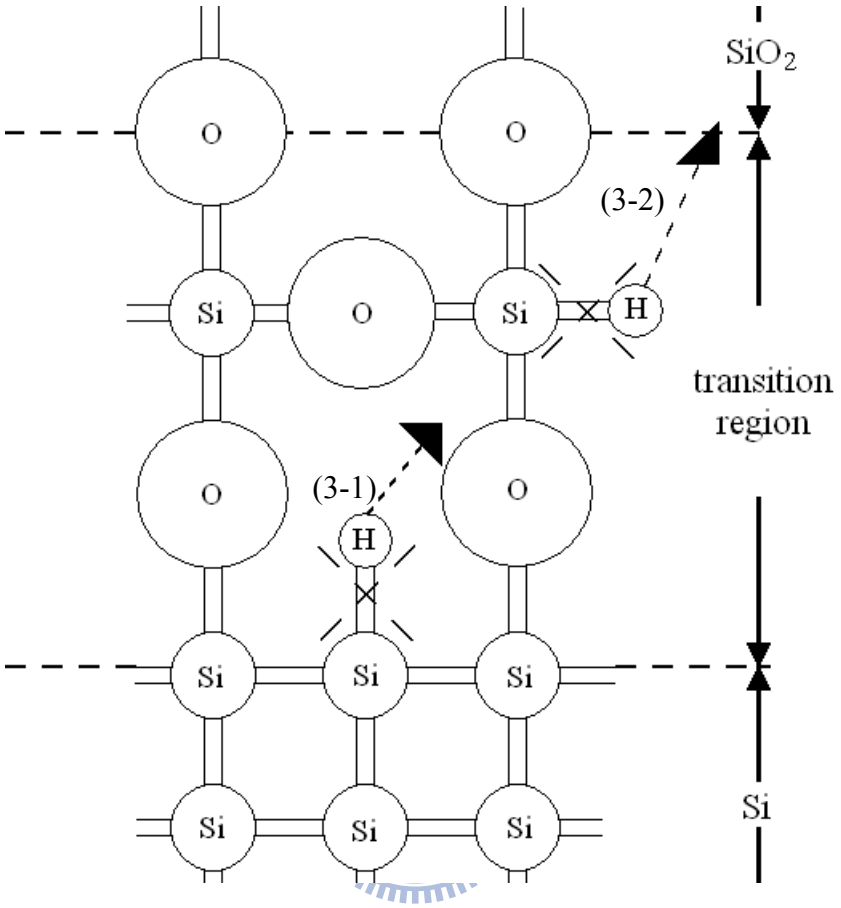


Fig. 3.18. Schematic structure of the SiO_2/Si interface [29].

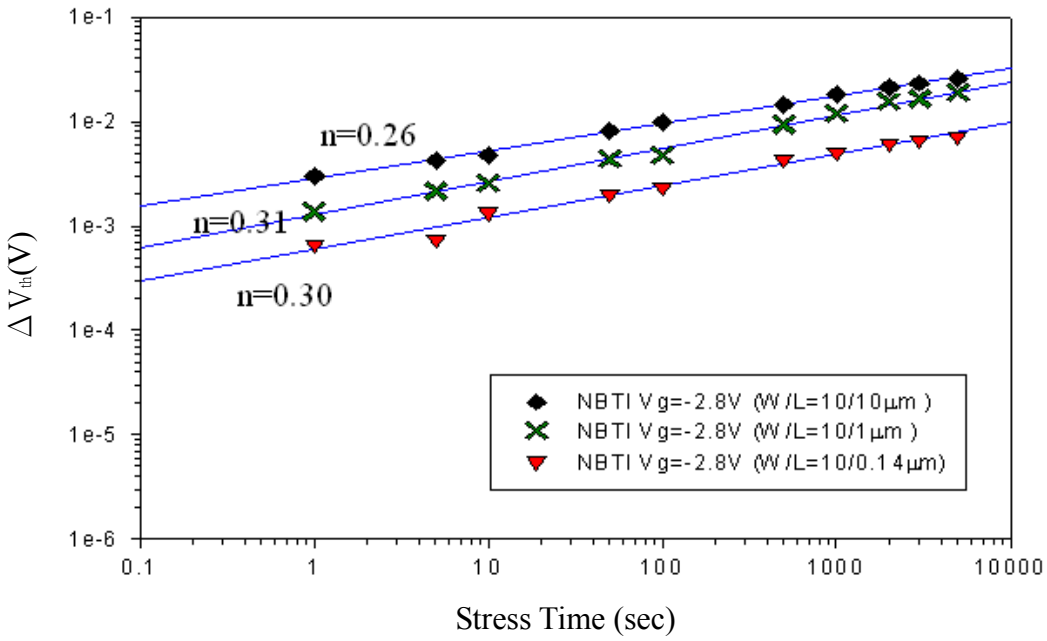
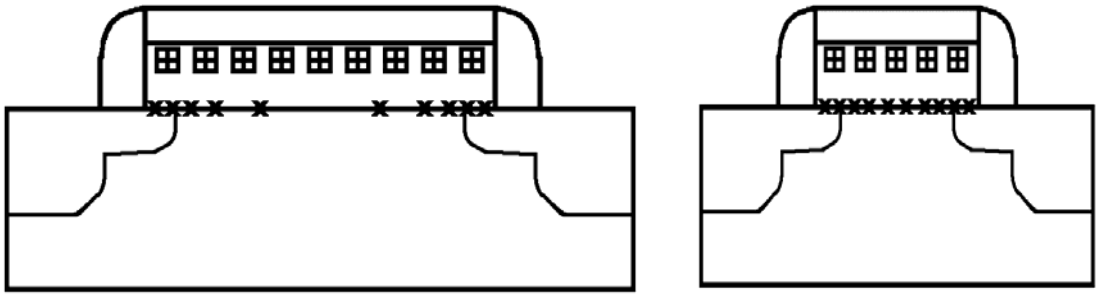


Fig. 3.19. V_{th} shift-versus-stress time curves for Type A devices with various channel length 0.14 μm, 1 μm and 10 μm at 125°C.



(a) (b)

x: Si–F bonds formed by the fabrication process

⊞: fixed-positive oxide charge

Fig. 3.20. A proposed scheme for passivation of interface states with F from the S/D extension of PMOSFET devices with (a) long-channel length and (b) short-channel length.

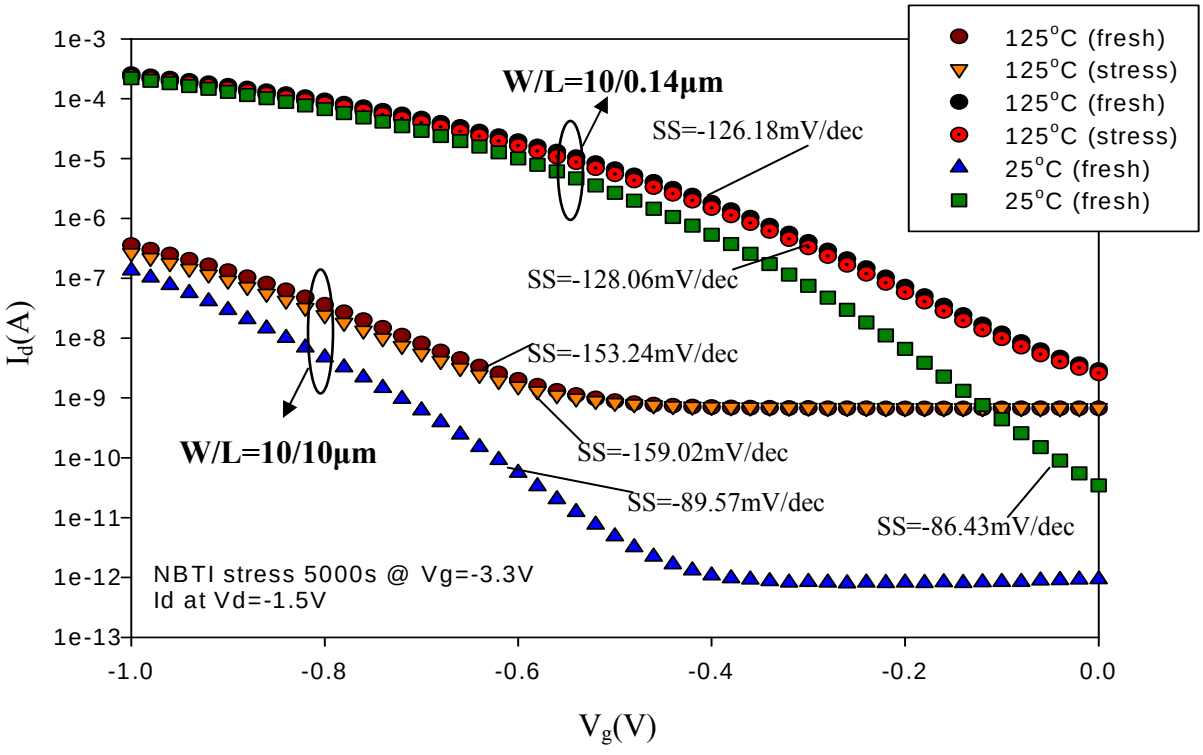


Fig. 3.21. Subthrehold characteristics measured and 25 or 125 °C for Type A devices with channel length of 0.14 µm and 10 µm before and after NBTI stress with gate voltage of -3.3 V.

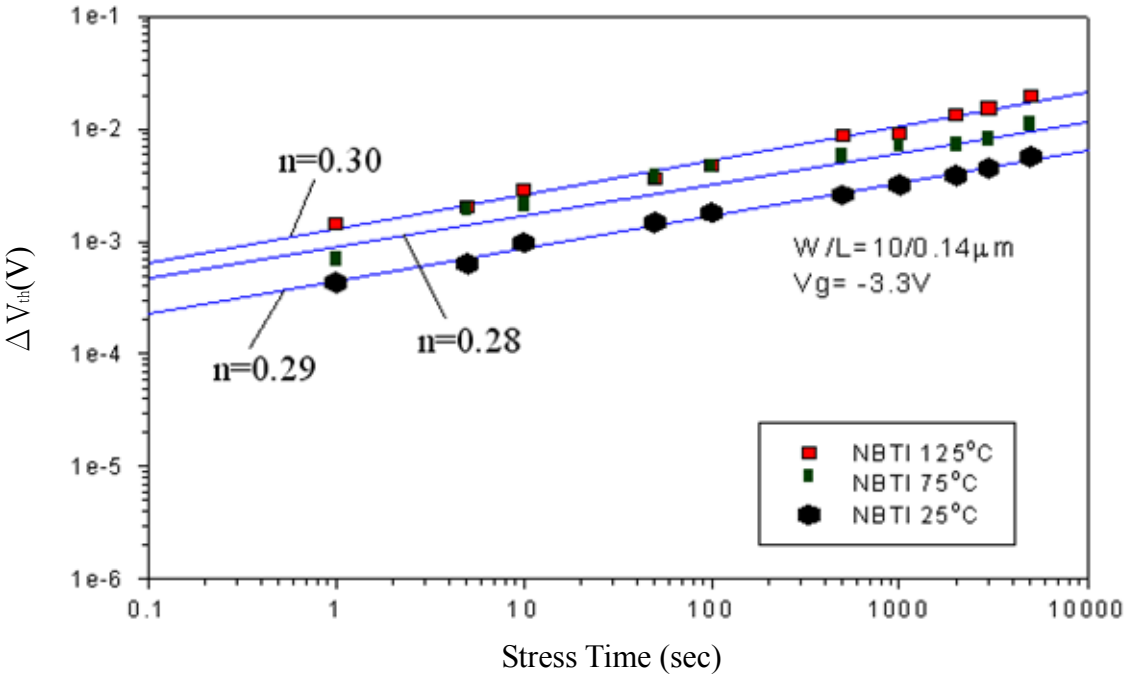


Fig. 3.22. V_{th} shift-versus-stress time curves for Type A device with channel length 0.14 μm at 25°C, 75°C and 125°C.

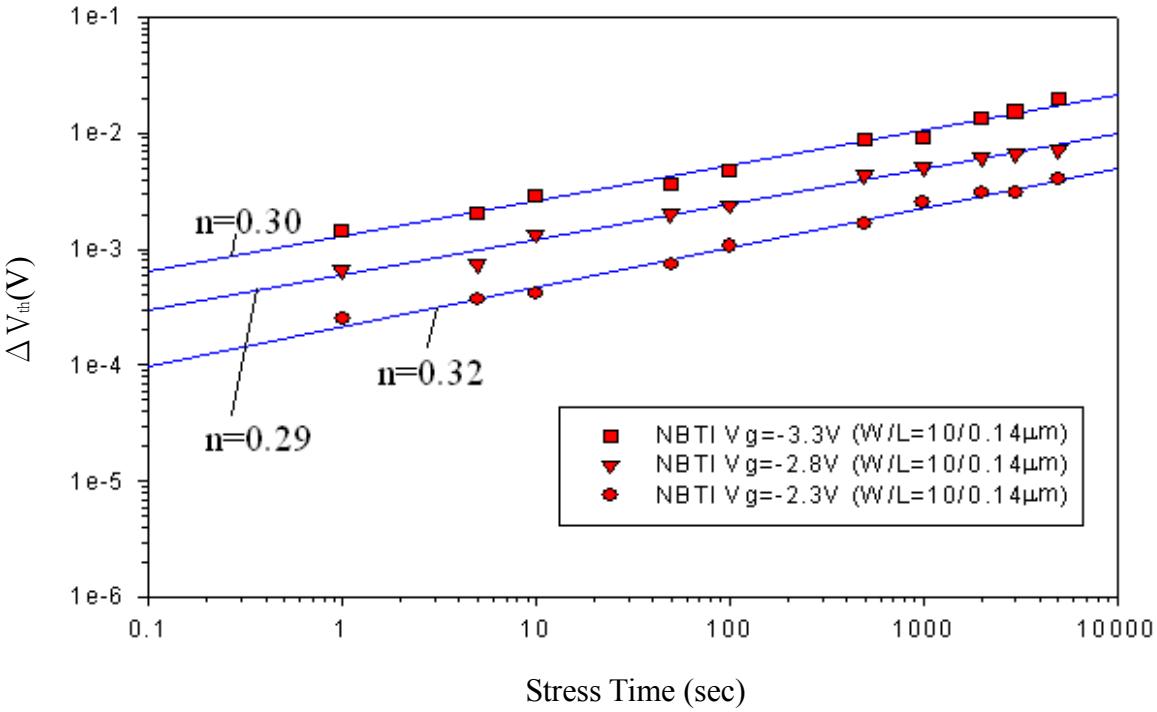


Fig. 3.23. V_{th} shift-versus-stress time curves for Type A device channel length 0.14 μm at 125°C and with various stress gate voltage -2.3 V, -2.8 V, and -3.3 V.

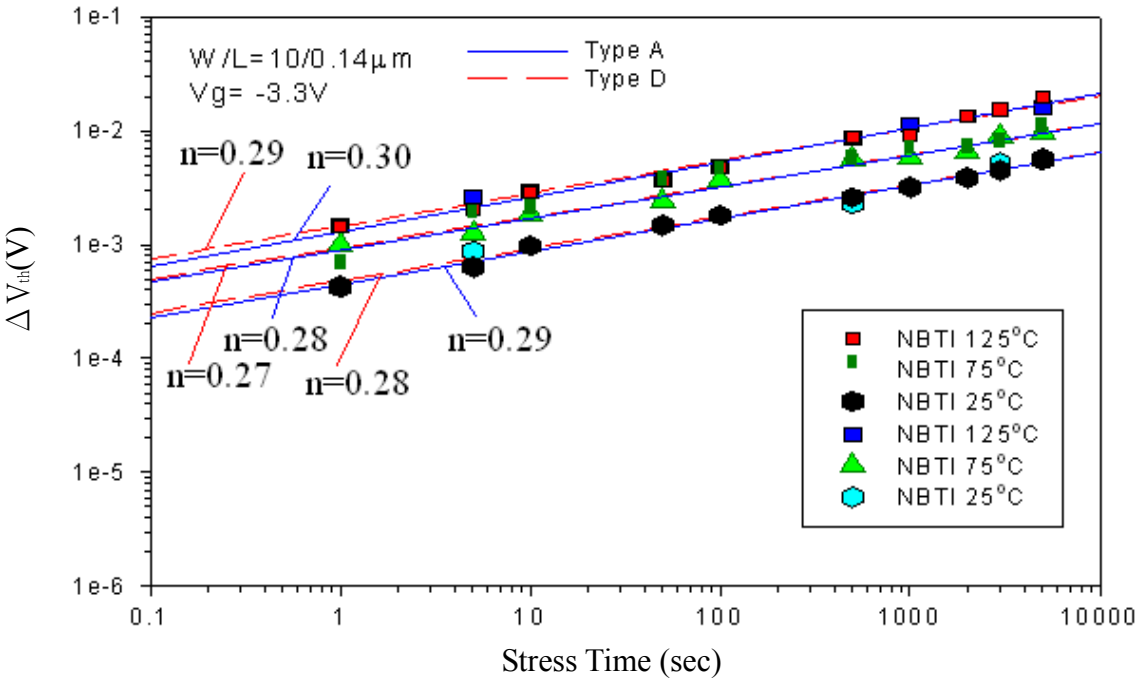


Fig. 3.24. V_{th} shift-versus-stress time curves for Type A and Type D devices with channel length 0.14 μm at 25°C, 75°C and 125°C.

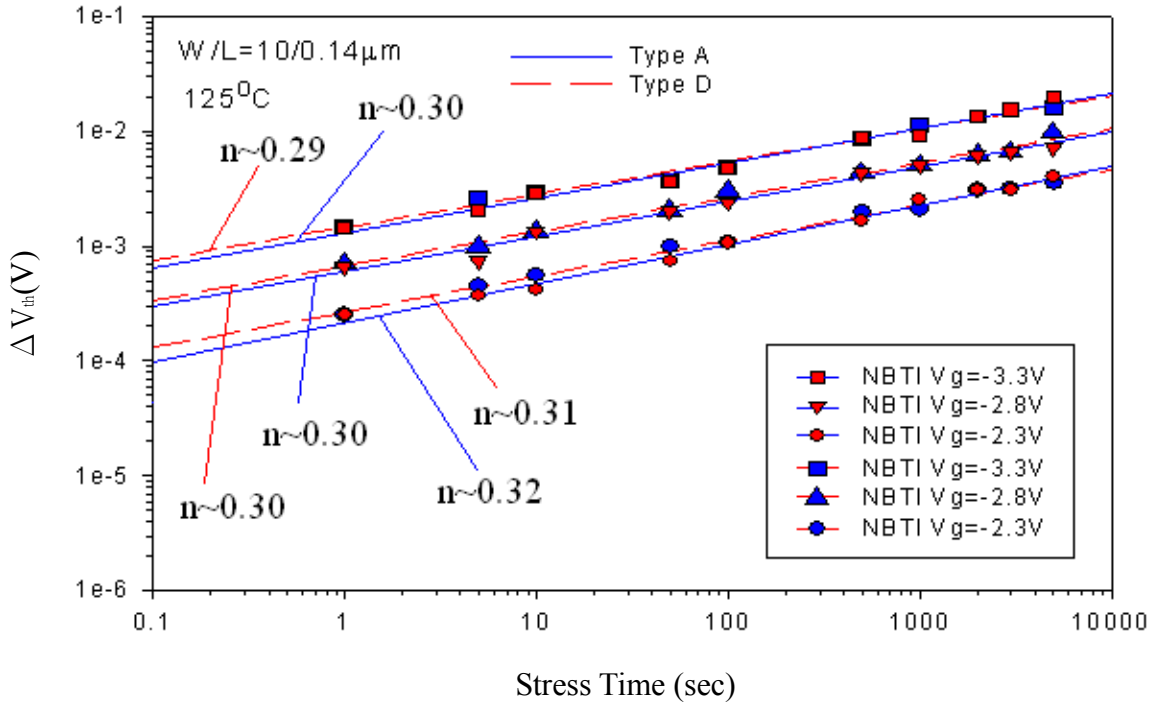


Fig. 3.25. V_{th} shift-versus-stress time curves for Type A and Type D devices at 125°C and channel length 0.14 μm with various stress gate voltage -2.3 V, -2.8 V, and -3.3 V.

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碩士論文題目：

使用 I-Line 雙重曝光技術實現非對稱 0.1μm P 型金氧半場效電晶體與相關可靠度問題之研究

A Study of Double-Patterning Technique with i-line Stepper to accomplish 0.1 μm PMOSFETs and Its Related Reliability Issues