國 立 交 通 大 學

電子工程學系電子研究所

碩 士 論 文

極紫外光輻射對於高介電常數介質之影響研究

Effect of Extreme Ultra-Violet Radiation on High Dielectric Constant Dielectrics

研 究 生：李勃學

指導教授：崔 秉 鉞 教授

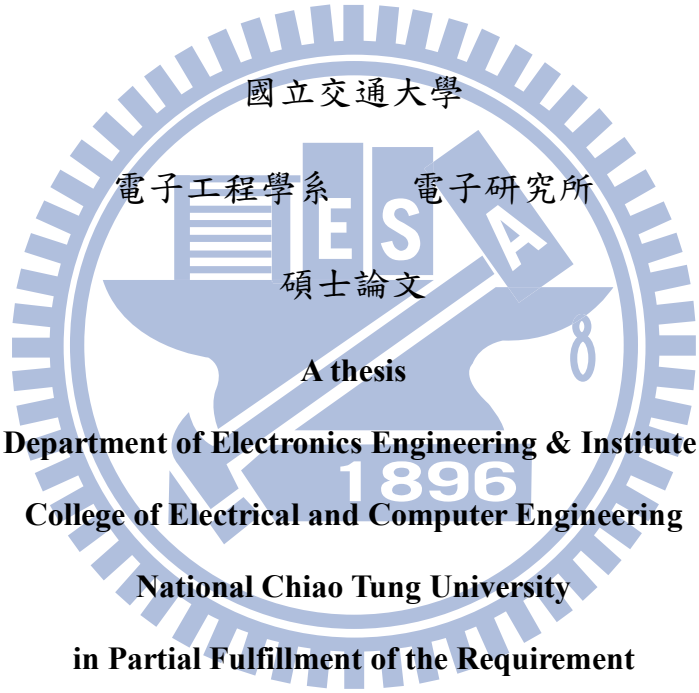
中華民國 九十九 年 七 月

極紫外光輻射對於高介電常數介質之影響研究

Effect of Extreme Ultra-Violet Radiation on High Dielectric Constant Dielectrics

研究生:李勃學　　Student: Po-Hsueh Li

指導教授:崔秉鉞　　Advisor: Bing-Yue Tsui



國立交通大學

電子工程學系　電子研究所

碩士論文

A thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirement

for the Degree of Master

in

Electronic Engineering

2010

Hsinchu, Taiwan, Republic of China

中華民國九十九年七月

極紫外光對於高介電常數薄膜之影響與其特性之研究

研究生：李勃學　　指導教授：崔秉鉞

國立交通大學電子工程學系　電子研究所碩士班

摘要

本論文探討極紫外光輻射對金屬閘極/高介電常數介電層的影響。選用氮化鈦為金屬閘極材料，並選用五種介電層，分別為二氧化矽、金屬有機化學沉積之氧化鋁、氧化鋁鈐、氧化矽鈐以及原子層沉積之氧化鋁，製作成金氧半(MOS)電容器，另外也使用二氧化矽、氧化鋁兩種介電質製作了金氧半場效電晶體(MOSFET)來驗證極紫外光對電晶體的影響。

以此五種介電質製作成的電容器經極紫外光照射後有明顯的電容-電壓特性變化，包括平帶電壓飄移，電容-電壓曲線變形，也有遲滯現象的劣化。平帶電壓飄移表示有淨正電荷產生，電容-電壓曲線變形表示介面能態增加，遲滯現象劣化則表示邊界陷阱增加。綜合所有結果顯示二氧化矽抗極紫外光能力最佳。在高介電常數介電質方面，氧化鋁呈現了最差之抗輻射能力。其中以金屬有機化學沉積之氧化鋁有最大的平帶電壓飄移，原子層沉積之氧化鋁則顯現出較多的介面能態以及遲滯現象增加。氧化矽鈐之能帶下半部經及紫外光照射後產生較多之介面能態。氧化鋁鈐也對及紫外光有敏感的反應。以二氧化矽及氧化鋁作為介電質的電晶體經極紫外光照射後，電晶體特性也和電容器一樣有臨界電壓漂移，此現象可以呼應電容器電容-電壓曲線的漂移，顯示在介電層中一樣有電洞的捕捉。

另外電晶體在關閉下的漏電流，經過元件的汲極、源極接面量測結果，我們可以確定這是由源極以及汲極的 n^+-p 接面漏電所導致的結果。可能是因為場氧化層(Field oxide)與矽基板介面經過極紫外光照射後，增加的介面能態導致激發電流增加所致。

本論文也討論到經過極紫外光影響後的元件是否可以有自我修復的現象。元件經由長時間儲存於一般室溫環境之下，電容器以及電晶體中因為極紫外光產生的傷害會逐漸減少，並且有一定程度的改善，但是並無法回復到未照射前的性能。因此極紫外光微影製程的設計必須與元件性能整體考慮，如何修復極紫外光照射所產生的損傷也是企待進一步研究的課題。

Effect of Extreme Ultra-Violet Radiation on High Dielectric Constant Dielectrics

Student: Po-Hsueh Li Advisor: Bing-Yue Tsui

Department of Electronics Engineering

Institute of Electronics

National Chiao Tung University

Abstract

In this thesis, EUV radiation damage on high dielectric constant (high-k) dielectric with metal gate is evaluated. TiN is selected as the metal gate electrode. Five kinds of high-k dielectric are evaluated. They are SiO_2, , MOCVD Al_2O_3, HfAlO, HfSiO and ALD Al_2O_3. Simple metal-oxide-Si (MOS) capacitor structure was fabricated. We also use SiO_2 and Al_2O_3 as gate dielectrics fabricate Metal-Oxide-Silicon-Field-Effect-Transistor (MOSFET) in order to demonstrate EUV effect on MOSFET.

Before and after EUV irradiation, the C-V curves of these five dielectrics have significant change. There are flatband voltage shift, C-V curve distortion and hysteresis increases. Among these five kinds of dielectrics, SiO_2 exhibits the best EUV resistance. In high-k materials, Al_2O_3 suffered the worst radiation tolerance. The MOCVD have the biggest flat band voltage shift and ALD Al_2O_3 exhibits more interface state and hysteresis increasing. After EUV irradiation the HfSiO generate

more interface state in lower Si band gap. The HfAlO also has sensitive EUV irradiation response. The radiation hardness of all dielectrics may be related to hole traps in the dielectric and the EUV absorbing rate. Positive charges (hole traps) and border traps were also generated during EUV exposure.

The I_d-V_g curve shows that there are V_{th} shift in both SiO_2 and Al_2O_3 samples which can respond to C-V curve shift with the positive charges be trapped in gate dielectric. We also observed when MOSFETs are in the off-state, the leakage current will raise after EUV irradiation. Measuring the n^+-p junction I-V characteristic we find out the leakage current is also affected by EUV. We infer that the edge of S/D region under isolation generated leakage path after EUV irradiation which cause the leakage current when MOSFETs are in off-state.

In this thesis we also discuses that weather the device can have self-annealing behavior after EUV irradiation. After storage the samples at room temperature for a long time, the decreasing of radiation induced damages is observed. How to fixed the radiation damage is still under researched.

誌謝

碩士的生涯很快的已經進入了結束的階段，一路上隨著波折不斷的實驗，也讓我從懵懂無知漸漸的蛻變並且茁壯堅強。在這短短的兩年之中我得到了許多人的協助以及鼓勵。謹以此文來表達我無限的感謝。

首先我必須感謝我的指導老師 崔秉鉞老師。老師有著豐富的學識、一絲不苟的處事態度、正直的品格、以及在教學上的熱誠。這些不凡的氣質，讓我對老師有著由衷的欽佩。在老師的指導下，嚴謹的思考模式、扎實的訓練讓我的碩士旅程得到比別人更多的收穫。在論文方面老師不厭其煩的一次一次、一字一字的幫我修改眾多的錯誤，也讓我相當的慚愧。爾今以後我將會謹遵老師的諄諄教誨前往未來的旅程。

再來實驗室的博班學長謝志民、盧季霈也時常的給我實驗的討論以及建議；還有李振銘學長在機台訓練、實驗進行、結果討論都給予大力且無私的協助讓我相當感動。李振欽學長、張孝瑜學姊也是提供了不少的實驗經驗。還有上一屆的學長賴瑞堯、王俊凱、余昆武以及蔡依成也是在機台訓練上出了不少的力，並且在平凡無奇的研究日子中帶來了很多的樂趣。實驗室的同學顏志展也和我一起做著我們前無古人的研究，並且度過一次又一次漫長又難熬的實驗時程，同甘且共苦。室友兼實驗室同學的羅子歆還有風趣幽默的周智超也在學業方面互相的砥礪精進。鄭嶸健、王培宇、陳璽允、蘇婷婷、張克勤等學弟妹們也為我帶來了許多的歡笑。另外國家同步輻射中心的許博淵博士、傅皇文先生還有彭均婷小姐也在實驗儀器的架設提供了相當多的協助；奈米中心的技術員們也相當熱心的幫助我完成我的實驗。

最後我必須感謝的是我最親愛的家人。父親 李其祐先生以及母親 石楣榕女士提供了我一個安詳穩定的環境，讓我在這無後顧之憂這環境之中求學、成長。感謝哥哥以及弟弟兄弟間的關照，更讓我覺得溫暖。

最後我將此文獻給一路上伴隨我、鼓勵我、協助我的大家。

Contents

Table Captions

Chapter 3

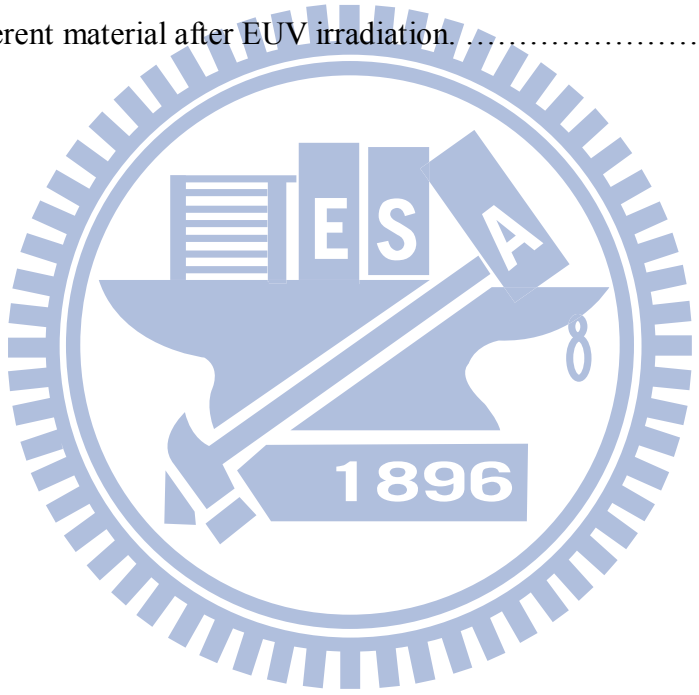


Figure Captions

Chapter1

Chapter2

Chapter3

Chapter1
Introduction

1-1 The Evolution of Lithography

VLSI technology has been developed since 1970s, the technology becomes more and more complex and hard to follow Moore' law. There are many issues limiting VLSI technology such as gate oxide quality, source/drain resistance, short channel effect, and so on. But in the latest decade, lithography system has dominated the scaling down speed. If there had any chance to make more delicate pattern, VLSI technology could progress much easier. From the first contact Aligner machine to G-line stepper, I-line stepper, 248-nm stepper, and 193-nm stepper/scanner, every change of exposure wavelength pushed the CMOS technology. However the 157-nm wavelength machine is so expensive and does not improve too much in line width and pitch, every company and fundamental research has turn to build 193-nm immersion machine. According to the 2009 ITRS [1], the 193-nm immersion machine with water can fabricate 45 nm pitch, and many company has made it into commercial production. Furthermore, the 193-nm immersion machine with double or even multiple pattern technique may be the next generation technology in 22 nm technology node, however it has not been proven that the 193-nm optical solutions are available beyond the 22 nm node. There must be a new method, a powerful method to deal with future technology nodes.

There are three potential solutions have been considered: Extreme Ultraviolet Lithography (EUVL), maskless lithography, and Imprint Lithography. All of these

technologies have huge difference comparing with the traditional lithography technology so they all have their own problems and advantages. Imprint Lithography is a technology makes template press on a thin film or on resist to make pattern, as shown in Fig. 1-1. In the previous work, imprint lithography can reach 14 nm pitch or even 5 nm linewidth [2]. However, how to make infrastructure for the 1X technology templates and a totally defect-free imprint templates are big problems. Maskless Lithography has been developed since 1980's. It use electron or molecule beam to make resister been exposed, as shown in Fig. 1-2. Electron and molecule is not a light, as long as one can make the beam smaller, it could make smaller pitch and line width. But the major problem of the Maskless Lithography is the wafer throughput. The commercial wafer throughput should be 200-300 wafers/hr, but e-beam lithography is far away from this requirement. Maybe Multi-beam systems could solve this problem in the future.

Comparing EUVL with the above two method, EUVL is also a promising lithography system and have ability to be the next generation system. The Netherlands company ASML had presented the EUV alpha-demo machine and AMD, IBM, and Toshiba used this machine to fabric 22nm node device successfully [3]. EUVL use 13.5nm wavelength as the light source, the light even close to X-ray, it also been called soft X-ray. The wavelength in this section has very high absorption rate in most materials, so the system needs to be operated in high vacuum. All optical systems should use defect-free reflective lens which reflect light by means of interference, and using reflection mask, as shown in Fig. 1-3. Because the EUVL has many differences compared to the 193-nm immersion system, there are some problems waiting for solving such as source power>180W, zero printing defect mask blanks, and some resist issues. All of these problems have been researched for a lone time. It is believed that these problems will soon be solved and the EUVL would be ready to go.

Although it is expected that EUVL will be used in the next generation, the EUV damage on advanced devices is a potential concern. It should be notice that the energy of EUV is 91.85 eV, which is several times of the SiO_2 band gap. The high energy photons may induce electron-hole pairs in the gate dielectric, and results in threshold voltage shift and device variation as well as reliability issue. Radiation damage should be taken into serious consideration. All of these problems are not so obvious in previous technology nodes because the energy of the 193-nm wavelength is only 6.42eV. As we introduce EUVL into fabricate process, radiation damage should be considered caerfully.

1-2 Radiation Damage

The original motive of radiation damage can trace back to the malfunction of *Telstar I communication satellite* in 1962, however, radiation damage was fully studied science 1970's. As the semiconductor devices were used from 1970' in the field of outer space, airplane, national defense industry, nuclear weapon, and high energy physics, the reliability of semiconductor devices in such harsh environment was noticed and we should take it much more carefully. Today, in the semiconductor process, there are many radiation damage sources those we also should be care of.

1-2-1 Radiation Induce Charge Generation and Transport

Radiation damage is caused by high energy ions or high energy photons which will generate mobile electrons and holes in both the silicon substrate and the insulator in MOS devices and cause some kinds of damages in the devices. The most sensitive part of MOS devices is the gate dielectric. Fig. 1-4 shows the effect of radiation on gate dielectric. When ionizing radiation passes through the gate oxide, the energy may

generate electron-hole pairs (e-h pairs) in the oxide. Most of the e-h pairs will recombine in several picoseconds. The other fraction of electrons and holes will be swept by the electric field. The electrons generated by radiation are much more mobile than the holes, it will be transferred away from oxide. The holes also been transferred by electric field toward the dielectric/Si substrate interface. However, the immobile holes undergo a rather dispersive hopping through the oxide. Eventually, some of the holes will be captured by hole-traps, and results in negative threshold voltage shift which can persist from hours to years. Interface states can be generated by radiation. There are many models have been proposed to describe the action, the most widely used model are hydrogen model, injection model, and stress model [4-10], but none of them can describe all phenomena. In the previous stage of radiation damage studies, most of them focused on the damages in SiO_2 which is the gate dielectric of traditional MOSFETs. In recent years, high dielectric constant (high-k) dielectric and metal gate have been employed since the 45 nm technology node and the radiation damage in high-k material should also be evaluated. High-k materials have been proved that they have much severe charge trapping problem then SiO_2 due to the high density of intrinsic defects [11-14]. There is increasing interest of radiation hardness of high-k materials as it replaces SiO_2 as the gate dielectric.

1-2-2 Radiation Effects on MOS Devices and Circuits

After irradiation, most characteristics of MOSFETs will be changed. These degradations such as threshold voltage shift, leakage current increase, swing degradation, DIBL degradation, and GIDL increase [15] make designer hard to have characteristics in hand. Even worse, all of these characteristics will change with time. When designer design the circuits, they have to make some trade-off on performance and work margin to make sure circuits will not malfunction. Radiation effects on

MOSFETs not only relate to materials but also relate to the device geometry, substrate type, method of fabrication, and structure. Besides, LOCOS isolation, shallow trench isolation, P-N junction, parasitic BJT, or even parasitic MOSFET [16-18] which around MOS devices would also be affected by radiation and have side effects on integrated circuits.

1-3 Metal Gate and High-κ Dielectric

1-3-1 From poly-Si Gate to Metal Gate

Metal gate MOSFETs was used at the beginning of the semiconductor industry. In that stage the gate electrode of MOSFETs was mad of Al. However, Al metal gate has a major disadvantage: the low melting point (660℃). Due to the low melting point, Al could not sustain high temperature process such as activation annealing of source/drain (S/D) dopants. Therefore, S/D must be formed before gate patterning. To make sure there is sufficient overlap between gate and S/D, the design rule of gate to S/D overlap can not scale down which results in high gate to S/D overlap capacitance. Gradually, Al gate was replaced by poly-silicon gate. Poly-Si gate was chose because it could be used in self-aligned process. Moreover, high melting point, low thermal stress, and fewer interface state in oxide/silicon also make the process much easier to be implemented and controlled.

However poly-Si gate encounters some problems. In order to reduce RC delay, the sheet resistance of poly-Si gate must be reduced, but the solid-state solubility of dopant in silicon has its limitation that makes sheet resistance could not be reduce easily. Fortunately, the salicide and polycide technology can solve the problem, but when the device scales down, we can't ensure the problem will not appear again. The

other problem is that boron may penetrate to channel from p^+ poly-Si gate. When the process temperature exceed 800℃ [19] , the dopants in the p^+ poly-Si gate diffuse into the substrate and cause fixed charge in the gate oxide. Moreover, the penetrated boron will change the substrate concentration. All of these side effects make the threshold voltage shift and difficult to be controlled. Although this problem can be relaxed by using amorphous Si gate, SiGe gate, or incorporating nitrogen in gate oxide, they could not totally be solved.

The major problem which make poly-Si gate been ruled out is the depletion region in the poly-Si gate. This is also cause by the limitation of solid solubility in the Si [20]. In fact, the active dopant concentration must be higher than 1.87×10^{20} cm^{-3}, at 25-nm gate length technology [21]. However, this presents great difficulty science the activated dopant concentration in poly-Si saturate at 6×10^{19} cm^{-3} and 1.0×10^{20} cm^{-3} for boron and phosphorus [22]. The depletion region in the gate electrode will degrade the channel potential, as illustrate in Fig. 1-5 [23]. This situation will make the equivalent gate oxide Thickness (EOT) could not continually scale down, even if there is already high quality thin gate oxide.

In order to make up for the shortcoming of poly-Si gate, metal gate seems to be a promising candidate for device under 45nm CMOS technology node. Metal gate provides low resistivity, high transconductance, improving mobility when high-k gate dielectric has been used [24, 25] to avoid boron penetration and gate depletion. Avoiding gate depletion could improve the gate controllability and reduce EOT. With all of these advantages, metal gate also have to deal with many old problems, high temperature in process, different gate work function on pMOS and nMOS, material stability, process compatibility, and reliability. By the time these problems have been solved and the poly-Si gate has been replaced.

1-3-2 From SiO_2 to High-κ material

Gate controllability is a subject which we always want to improve. As the technology going forward, the industry demands higher performance device and higher device density, yet we could easily reach these goals by scaling down the thickness of gate dielectric. Increasing the gate capacitance C_{ox} is the reason why we want to scaling down the gate dielectric. From the simple model for MOSFET, the drive current could be written as

$$I_d = \frac{W}{L}\mu C_{ox}(V_G - V_T - \frac{V_D}{2})V_D \quad (1)$$

, where W is the channel width, L is the channel length, μ is the channel carrier mobility, C_{ox} is the capacitance density of gate underlying channel is in the inverted state, V_G is the gate bias, and V_D is the drain bias. When the device is working in the saturation region, $V_D = V_G - V_T$ and equation (1) could be written as

$$I_{d,sat} = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_G - V_T)^2 \quad (2)$$

Logic device's performance depends on the $I_{d,sat}$, and C_{ox} could be promoted by decreasing oxide thickness, for the reason

$$C_{ox} = \frac{k\varepsilon_0}{t_{ox}} \quad (3)$$

, where k is the dielectric constant, ε_0 is permittivity of free space, and t_{ox} is the thickness of oxide. However t_{ox} could not shrink forever. In the 2009 ITRS, it is pointed out that the EOT of the high-performance logic device should reached 1.1 nm in 25nm technology node [26][27]. The ultra thin oxynitride will not competent for the job as the gate dielectric [28]. We can see clearly in Fig. 1-6., the leakage current couldn't be suppressed to desired level. The direct tunneling current will increase exponentially with decreasing gate oxide thickness. There are also significant reliability concerns for SiO_2 in this thickness regime [29].

In order to solve the above problems, there must be a material that has good gate controllability, low leakage current, and good reliability. Therefore, high-k material was introduced. We can understand the advantage of high-k material from equation (3). The high dielectric constant, which is higher than SiO_2 (k=3.9), can reach the same C_{ox} level with thicker physical thickness. High-k material with thick physical thickness can not only reduce direct leakage current but also have better reliability compared with ultrathin oxide. Many high-k materials have been proposed. Ta_2O_5 [30][31], $SrTiO_3$[32][33][34], and Al_2O_3[35][36] were been nominate for its have applied in the DRAM memory capacitor for many years and the high dielectric constant from 10-80. However, Ta_2O_5 and $SrTiO_3$ materials are not thermodynamically stable in direct contact to Si [16][37][38][39]. The dielectric constant of Al_2O_3 is not high enough which will make the EOT hard to scale down. Comparing with Ta_2O_5, $SrTiO_3$, and Al_2O_3, group IVB metal oxides show much promise in all kinds of material. TiO_2 [40][41], ZrO_2[42][43] and HfO_2[44][45] are wildly study in this field because of their's thermal stability, low interface state, suitable band offset and Gate compatibility [46]. Among these high-k materials, Hf-based dielectric has been used in the high performance logic device in Intel's 45 nm technology [47][48].

As mentioned at the end of Section 1-2-1, the radiation damage on Al_2O_3 was noticed science 1990's [49] [50]. Using high energy X-ray, these researches are focus on the electrical degradation instead of using Al_2O_3 to replace SiO_2 on VLSI technology. Until 2000's, the Hf-based dielectrics were mentioned and wildly researched for it's potential to replace SiO_2. J. A. Felix and D. M. Fleetwood et al. study many radiation reactions on the Hf-based dielectrics, and Al_2O_3. The basic experiments of these studies followed the radiation damage on SiO_2 researches and they all show high-k films are much easier to be affected by radiation compare with

SiO_2. Because EUV is a high energy source, when EUVL is introduced into mass production, the radiation hardness of these high-k materials should be reconsidered again.

1-4 Thesis Organization

In the first chapter of this thesis, we have briefly described the evolution of lithography system and also understand the EUV would be one of the most promising light source beyond 22 nm technology node. Since high-k and metal gate structure has been used in CMOS technology, EUV irradiation damage on high-k material should be concerned. Literatures regarding to ionized radiation damages on high-k material are also reviewed in this chapter.

In chapter 2, the fabrication process of MOS capacitor with various high-k dielectrics using TiN as gate electrode and traditional MOSFET will be described in detail. We also describe how to build up the experimental chamber and environment which we used in the National Synchrotron Radiation Research Center (NSRC). At the end of chapter 2, the method which is used to analyze the interface density is explained.

In chapter 3, the basic character of MOS capacitance will be shown. It is demonstrated that after EUV illumination the device suffers from some damages and degradations. Traditional MOSFET and MOSFET with high-k/metal gate are compared. It is also observed that EUV also damages the isolation region and cause higher S/D junction leakage current. .

At the end of this thesis, conclusions, future works, and some advices will be addressed.

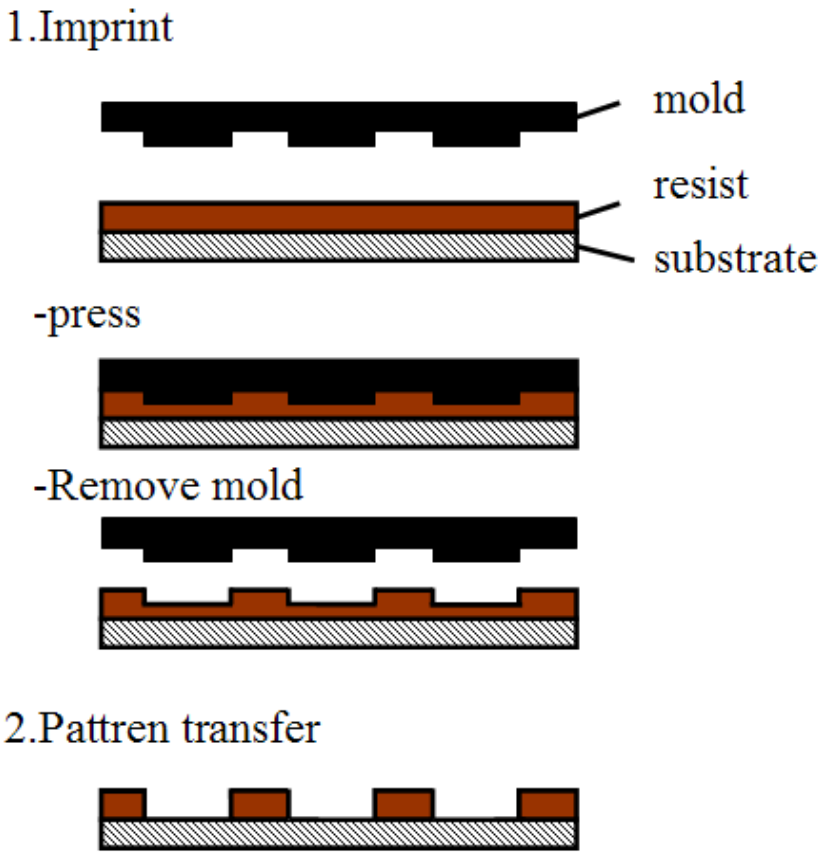


Fig. 1.1 Basic concept of imprint lithography

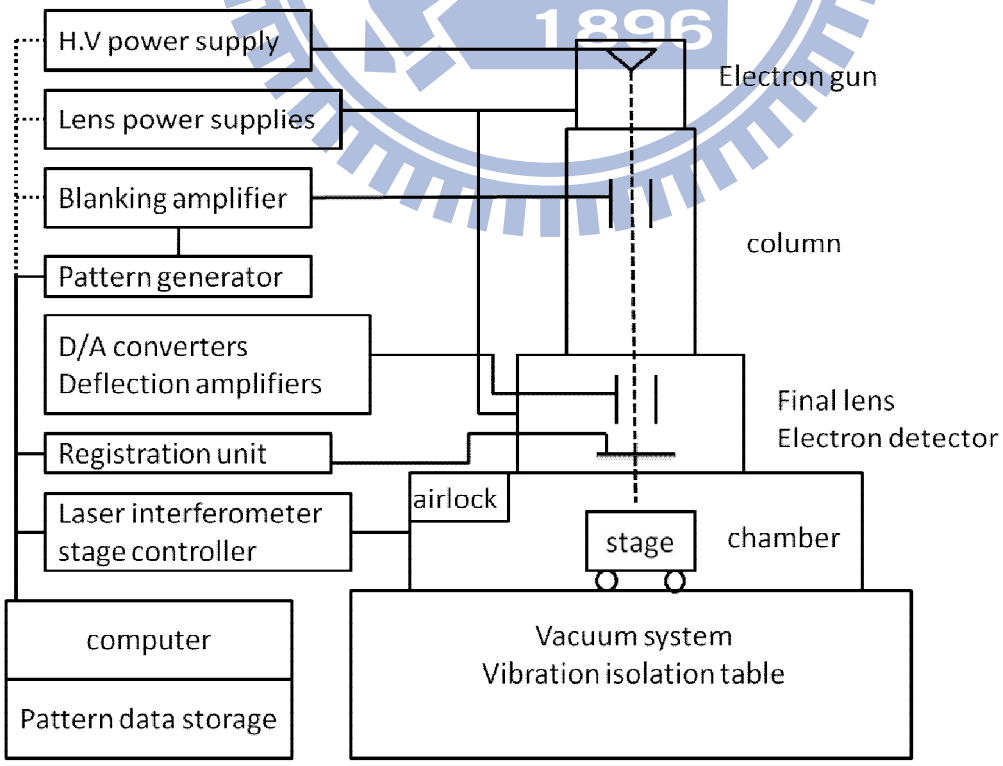


Fig. 1.2 Outlook of maskless lithography system

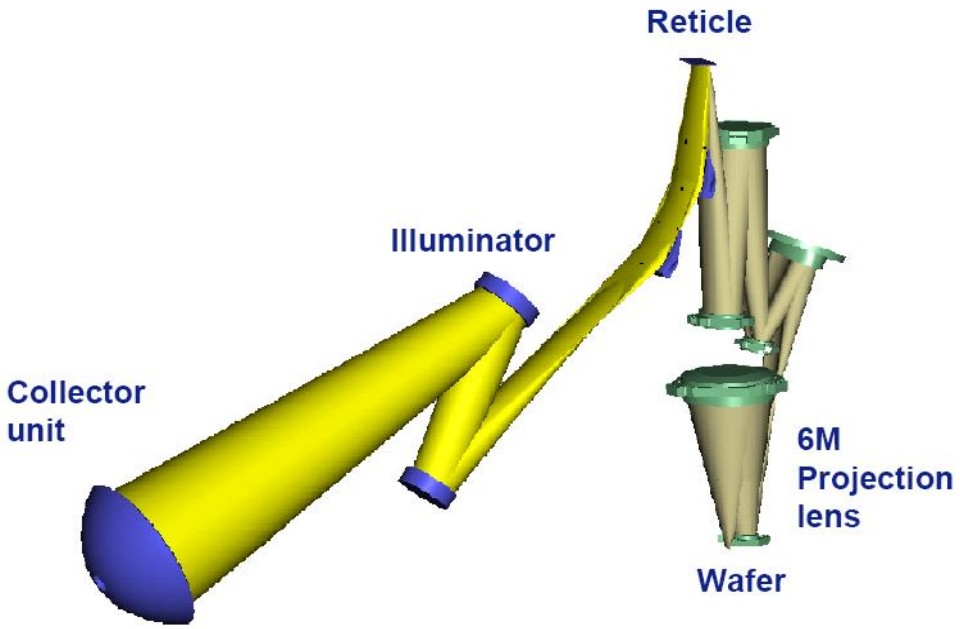


Fig. 1-3 Basic concept of EUVL which are placed in ultra-high vacuum chamber.

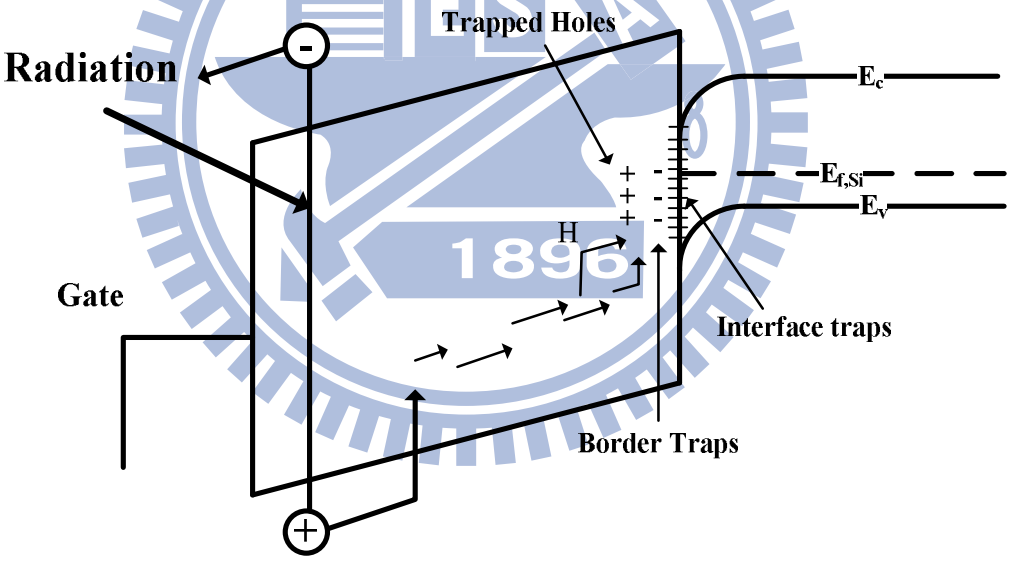


Fig. 1-4 Band diagram of gate oxide which is effected by radiation. Charge trapping on the gate dielectrics and some defect traps are generation.

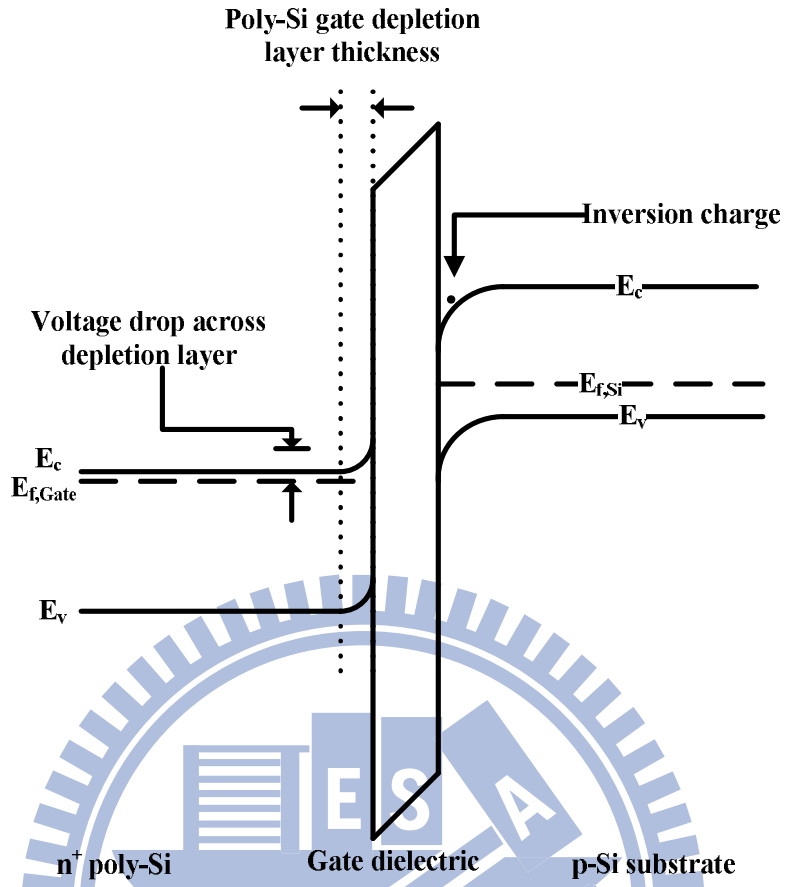


Fig 1-5 Band diagram of poly-si gate depletion.

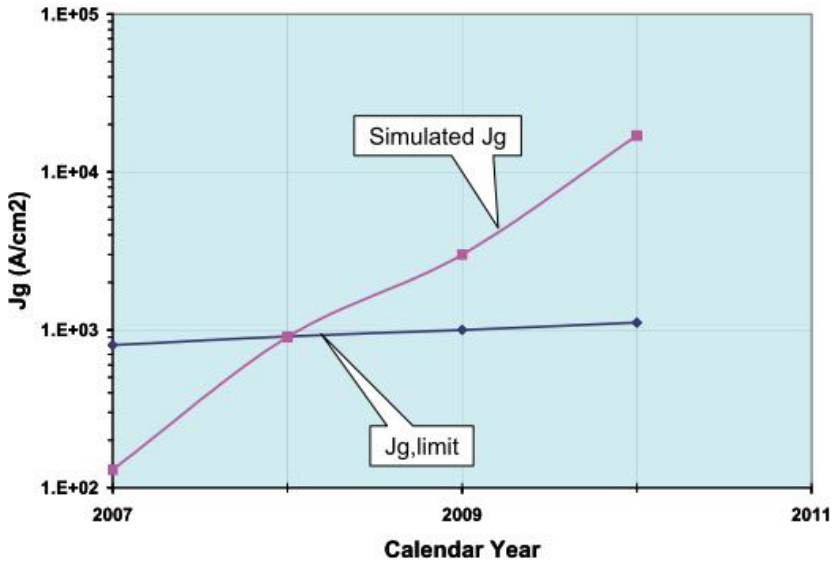


Fig.1-6 High-Performance Logic: The simulated gate leakage current versus limit gate leakage current for SiON (ITRS 2007 PROCESS INTEGRATION, DEVICES, AND STRUCTURES page.13)

Chapter2
Experimental Procedure

In this thesis we have prepared two kinds of samples for our experiment: high-k/metal gate MIS capacitors and high-k/poly-Si gate MOSFETs. The ideal work function of MOSFETs should be near the Si conduction band for NMOS and valence band for PMOS. For high-k/metal gate MIS capacitors, we choose TiN as the gate electrode because it is a midgap metal and is suit for adjusting PMOS and NMOS threshold voltage. TiN also have the good ability to screen low-energy surface optical phonon which was reported for mobility degradation under channel inversion condition [24][25]. HfSiO, HfAlO and Al_2O_3 are used as the gate dielectric and SiO_2 is used as reference. A 40-nm-thick TiN is designed for EUV to penetrate into gate dielectric. In order to have appropriate radiation damage that can be detected easily, the thickness of gate dielectric is chosen as 15 nm. The MOSFETs use poly-Si/SiO_2 and poly-Si/Al_2O_3 as gate stacks. We also prepared TiN/Al_2O_3 capacitor as the in-situ measurement sample which could measure directly during EUV illumination.

2-1 High-k Metal gate MIS Capacitor Fabrication

Fig. 2.1 shows the structure of the high-k/metal gate MIS capacitor. The devices were fabricated on 6-inch p-type Si wafer with resistivity of 1~10 Ω-cm. The wafers were first marked by a laser-marker system and then were cleaned in SC1 for 10 min to remove particles. Then the wafers were cleaned using the stander RCA cleaning process. MOCVD system was used to deposit three kinds of high-k dielectric as the gate dielectric. They are HfSiO, HfAlO and Al_2O_3. Using $Hf(O^tbu)_2(mmp)_2$,

$Si(O^tbu)_2(mmp)_2$, and Al(isopropoxide)$_3$ as precursors and Ar as carrier gas in O_2 gas surround, the high-k dielectric were deposited at 500°C. The pressure during deposition was 5 mbar and the thicknesses were about 15 nm. There was also a 15-nm-thick SiO_2 growing thermally by a furnace system at 900°C as the control sample. The 40nm TiN metal gate was deposited by a sputtering system and was patterned by RIE etching. The samples were then sputtered Al on back side by an e-gun system as the backside contact. After a 300°C /30min annealing process, the capacitor samples were finished.

2-2 MOSFET Fabrication

Fig. 2.2 shows the main process flow of the n-channel MOSFET. The devices were fabricated on 4-inch p-type Si wafers with resistivity of 1~10 Ω-cm. Wafers were cleaned by standard RCA cleaning process first and then a 500-nm-thick SiO_2 was thermally grown at 1000°C by a furnace system. We used I-line stepper to define the active region and used buffered oxide etchant (BOE) to open the active region as shown in Fig. 2.2(a). After removing the photo-resist by SPM (H_2SO_4 : H_2O_2 = 3 : 1), a SiO_2 film was thermally grown at 900°C by dry oxide to 15-nm-thick as a sacrificial layer. B_{11}^+ ion implantation at 145 keV to a dose of $1x10^{13}$ cm^{-2} was performed to enhance the field SiO_2 isolation as shown in Fig 2.2(b). Then, the sacrificial layer was remove by DHF (HF:H_2O=1:100). There are two kinds of gate dielectrics : SiO_2 and Al_2O_3. The SiO_2 was thermally grown at 900°C by dry oxidation to 15 nm and the Al_2O_3 was deposit by an atomic layer deposition (ALD) system using $Al(CH_3)_3$ (TMA) and H_2O as precursors. The Al_2O_3 was deposited at 300°C and the thickness is also 15 nm. The following step was deposition of 150-nm-thick undoped poly-Si film by a low pressure chemical vapor deposition (LPCVD) system. The temperature of

LPCVD was 620°C and the pressure was 100mtorr. And then the poly-Si gate electrode was patterned by I-line stepper. The gate etching used a high density plasma reactive ion etching (HDP RIE) system and the etching stopped at the dielectric film as shown in Fig 2.2 (c). After forming the SiO_2 spacer as shown in Fig 2.2(d), P_{31}^{+} was implanted at 35 keV to a dose of $5x10^{15}$ cm^{-2}. Gate and source/drain dopant activation was performed by rapid thermal annealing (RTA) at 900°C for 20 seconds in nitrogen gas ambient. After Al deposition by E-gun on the wafer back side, the device fabrication was finished as shown in Fig 2.2(e).

2-2-1In-situ Measurement Setup

In order to set up the in-situ measured system the sample should connect with outer PVC circuit board by Au wire. The Au wire bonding point cannot bond directly on the gate because the gate oxide would be damage by the bond machine. The bonding position should be on the field oxide region.

The main process of the in-situ measurement sample is shown in Fig. 2-3. In-situ measurement samples were fabricated on 4-inch p-type Si wafers with resistivity of 1~10 Ω-cm. A 500-nm-thick SiO_2 was thermally grown at 1000℃ by furnace to be field oxide. After patterning the active region, Al_2O_3 were deposited on the wafers by an ALD system with the precursor $Al(CH_3)_3$ (TMA) and H_2O at 250℃. Then, TiN was deposited for 400Å thickness by sputter (Fig. 2-3(a)). The gate was patterned by I-line stepper and etched by HDP-RIE (Fig. 2-3(b)). Al pad was formed by lifted-off method as shown in Fig. 2-3(c). Finally the sample was deposited with Al on the back side and annealed at 300℃ for 30min.

The top view of finalized in-situ measurement sample is shown in Fig 2-4.The sample was attached to a glass substrate by conductive copper foil which acts as the back electrode. A circuit board attached to the glass substrate above the sample. Then

sample and circuit board are bonded together by Au wire. The circuit board will contact to the pin as the top electrode.

2-3 EUV Source and End Station Setup

There are many ways to produce EUV such as discharge produced plasma (DPP), laser produced plasma (LPP) and synchrotron radiation [52]. Compared to DPP and LPP, synchrotron light source have some benefits for our study. The synchrotron light is a pure light which means that it has no contamination issue and the light also has extreme narrow band width of about 0.01 % which suits ultra thin film measurement and EUV multilayer optical component test. However synchrotron light is not fit mass production for its power is only 0.5 W which is far away from mass production power of 180W. The main reason for commercial machine needs 180W source power is that many optical components decay the source power inside the system. As EUV reach wafer surface, the power of EUV would be less than 1 % of the source power. There is no so much decay in the synchrotron system so that the synchrotron system can have lower power. In this thesis, we use synchrotron radiation generated EUV source provided by the National Synchrotron Radiation Research Center, Taiwan (NSRRC) and the beam line numbers are BL08A and BL21B.

The end station we used in this experiment consists of two parts: main chamber and differential chamber. These two chambers are separated by a valve. Both chambers should be pumped down to a pressure about 10^{-8}~10^{-7} torr during the experiment. The main chamber is the place where we put the sample in and the differential chamber allows that the pressure of main chamber doesn't keep at such a high vacuum. The EUV light is generated by synchrotron radiation and be focused by the beam line. Then the light passes through the differential chamber and finally

reaches the main chamber and irradiates on the sample. The outlook of the whole system is shown in Fig.2-5 and Fig 2-6. Fig. 2-5 shows the module of the whole experiment system. Turbo pump 1 and turbo pump 2 provide the high vacuum environment at main chamber and differential chamber, respectively. Rough pumping is done by scroll pump .Fig. 2-5(a) is the photo of our system and Fig2-5 (b) shows the output port position, through which the in-situ measurement sample can be connected to the measure instruments.

The shape of the beam is a smiling shape (Fig 2-7) and the size is 0.016 cm^2. Using photo diode we can transfer the photocurrent into EUV flux. The structure of sample rod is shown in Fig. 2-8. Sample can be directly stuck on the rod by copper foil or carbon foil. In this thesis, it is found that there still have some damages on the devices even if the devices are not directly irradiated by EUV. To avoid this issue, sample can be stuck behind a steal plat with a small window. Through the window, only the devices to be tested would be irradiated. The following is the stander steps of changing samples :

1. Check all the valve (V1 ,V2 and V3) and turbo pump 1 and 2 are close (The user should wait for 20-30 min after turn off the turbo pump to let the turbo pump slow down).
2. Vent the main chamber from the back turbo pump 1 with N_2 gas purge.
3. Open the sample rod and take it out.
4. Stick the sample on the sample rod.
5. Load the sample rod into the main chamber and lock it off.
6. Open V_2, the scroll will pump down the pressure of main chamber to $5x10^{-2}$ torr then open V3 valve and wait for 1min.
7. Start turbo 1 and turbo 2.
8. Open V1.

As the pressure of the main chamber is pumped down to $1x10^{-7}$ ~ $5x10^{-8}$ torr, sample is ready to expose to EUV. The EUV is invisible, so we use white light to help us to find the light position. The main irradiation processes are as follows :

1. Set the synchrotron light to white light.
2. Open beam line valve and make the white light to pass through differential chamber and incident in the main chamber
3. Using telescope to observe white light spot and set the telescope cross line on the light spot site.
4. Open beam line valve to block the white light and set light into EUV.
5. Move the sample to the telescope cross line (If one wants to observe the EUV directly, he can make the EUV spot on the fluorescent plate which is on the top of sample rod.)
6. Open beam line valve then EUV incidents on the sample and count down the expose time.
7. Turn off beam line valve to block EUV.
8. Go to Step 5 if there are other samples on the sample rod.

After the irradiation process is over, user can follow the changing sample steps to change the sample or finish the experiment.

2-4 D_{it} and Oxide Trap Measurement

High energy radiation will generate oxide charges and interface states. These damages may cause C-V curve shift and distortion. In this thesis we estimate these interface density and oxide charge density by two methods: high-frequency C-V method (Terman method) [53] and V_{fb} and V_{mid} method. The theoretical C-V curve is generated according to the following equations assuming there are no interface state and oxide

charges [54]:

$$\frac{1}{C}=\frac{1}{C_{ox}}+\frac{1}{C_d} \qquad \text{.....Eq.2.1}$$

where

$$C_d \equiv \frac{dQ_s}{d\varphi_s}=\frac{\varepsilon_s}{\sqrt{2}L_D}\frac{1-\exp(-\beta\varphi_s)+(n_{p0}/p_{p0})[\exp(\beta\varphi_s)-1]}{F(\beta\varphi_s, n_{p0}/p_{p0})}$$

$$F(\beta\varphi_s, n_{p0}/p_{p0})=\sqrt{[\exp(-\beta\varphi_p)+\beta\varphi_p-1]+\frac{n_{p0}}{p_{p0}}[\exp(\beta\varphi_p)-\beta\varphi_p-1]}\geq 0$$

$$\beta \equiv \frac{q}{KT}$$

$$L_D \equiv \sqrt{\frac{kT\varepsilon_s}{p_{p0}q^2}} \equiv \sqrt{\frac{\varepsilon_s}{qp_{p0}\beta}}$$

The C_{ox} can obtain from the C-V curve measurement in accumulation mode. The substrate concentration also can get from the following equation:

$$N_{sub}=-2\left[q\varepsilon_{si}\frac{\partial\left(\frac{1}{C^2}\right)}{\partial V_G}\right]^{-1} \qquad \text{.....Eq. 2.2}$$

After shift the ideal C-V curve by V_{fb} which is extracted from the measured C-V curve, the D_{it} can be calculated by comparing the measure C-V curve with the theoretical C-V curve.

$$D_{it}=\frac{C_{ox}}{q}\frac{d(\Delta V_G)}{d\varphi_s} \qquad \text{..... Eq. 2.3}$$

, where ΔV_G is the V_G different between ideal C-V curve and measured C-V curve under same capacitance and φ_s is the surface potential.

When the device is damage by radiation, we care about the change of oxide trap density (ΔN_{ot}) and interface state density (ΔN_{it}) which are related to the charges and interface states generated by radiation. In other word we don't have to calculate the total oxide traps and total interface states instead we can use ΔV_{mg} (mid gate voltage difference before and after irradiation) and ΔV_{fb} (flat band voltage difference before

and after irradiation). The extraction of ΔN_{ot} and ΔN_{it} is much easier. The basic assumption is that interface states in the upper half of the Si bandgap are predominantly acceptor-like, while those in the lower half of the bandgap are predominately donor-like [48].

$$\Delta V_{mg} \equiv V_{mg_1} - V_{mg_2} \quad \text{..... Eq. 2.4}$$

$$\Delta V_{fb} \equiv V_{fb1} - V_{fb2} \quad \text{..... Eq. 2.5}$$

, where V_{mg1} and V_{mg2} stand for the mid gate voltage before and after radiation damage, respectively, V_{fb1} and V_{fb2} are the mid gate voltage and flat band voltage before and after radiation damage, respectively. Then the ΔN_{ot} and ΔN_{it} can be easily extracted by the following equations.

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \quad \text{..... Eq. 2.6}$$

$$\Delta N_{it} = -\frac{C_{ox}(\Delta V_{fb} - \Delta V_{mg})}{qA} \quad \text{..... Eq. 2.7}$$

The reason could be easily explained by Fig.2.9 (a) and Fig2.9 (b). As the gate voltage is at V_{mg}, only the ΔN_{ot} affects V_{mg} because the interface states are charge neutrality by donor-like interface states and acceptor-like interface states. The ΔV_{fb} is affect by ΔN_{it} and ΔN_{ot}. By excluding the ΔN_{ot} by Eq. 2.6, the ΔN_{it} can be calculated by Eq.2.7.

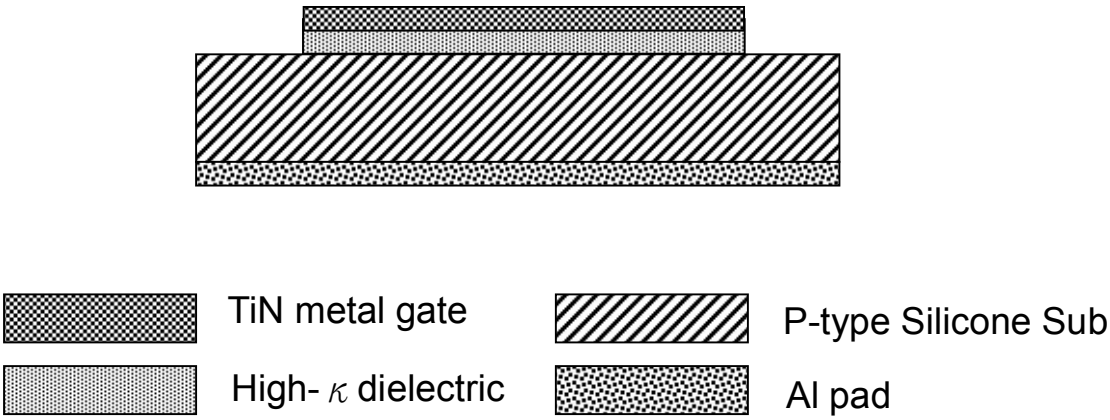


Fig. 2-1 Structure of High-k metal gate capacitance.

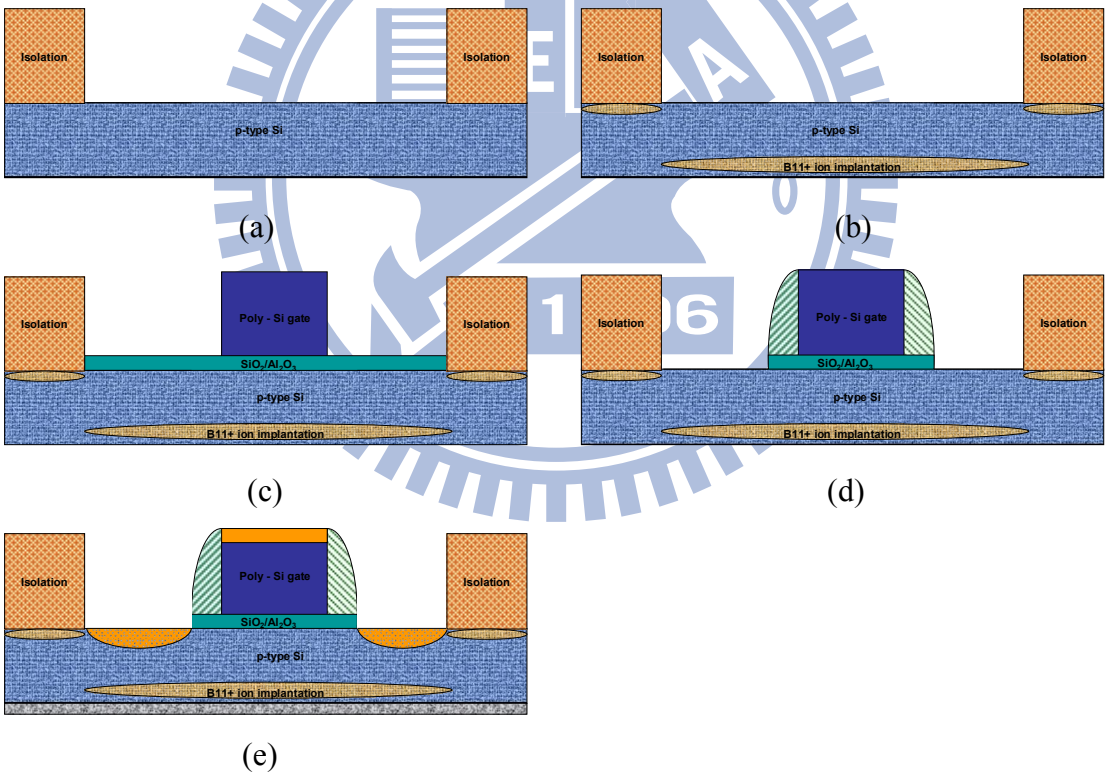
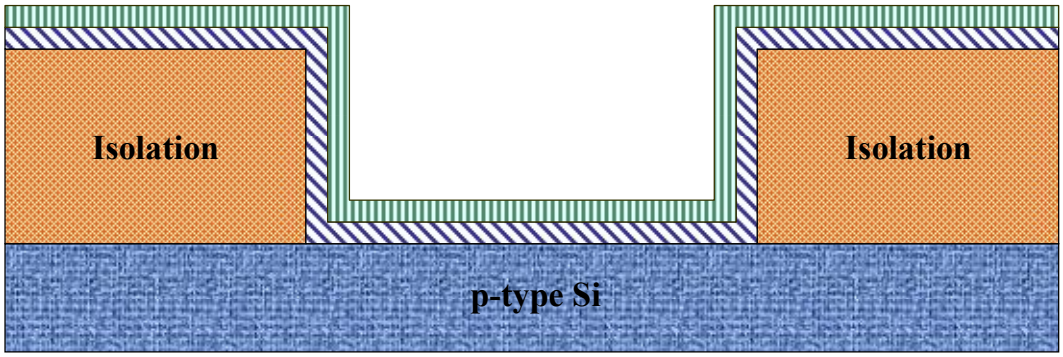
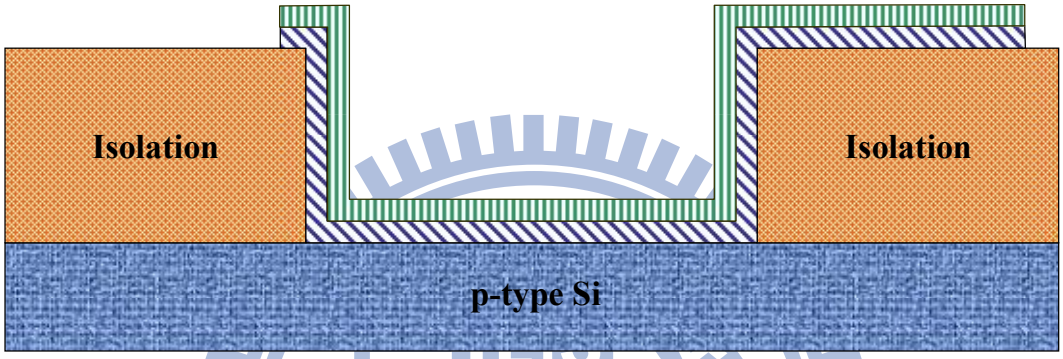


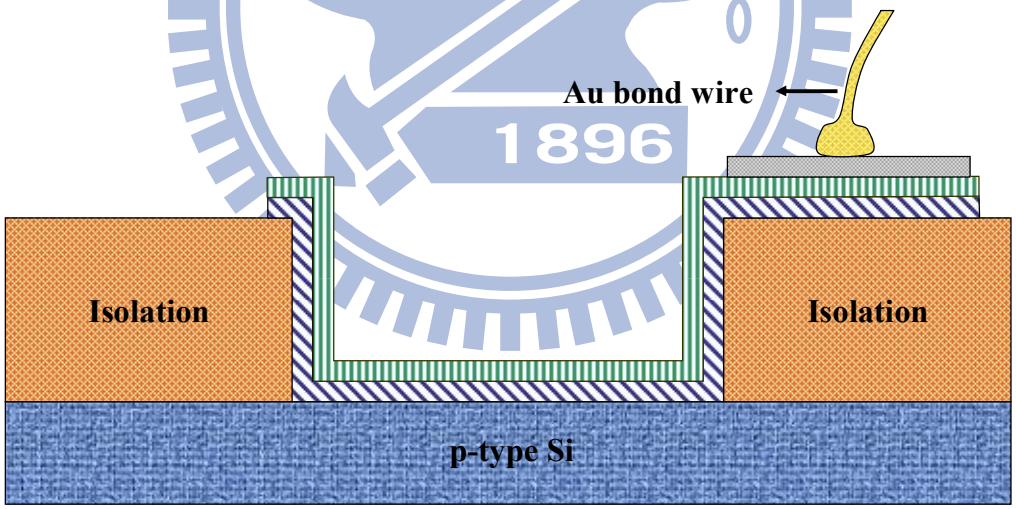
Fig. 2-2 Cross section view of the device after main process. (a) Isolation oxide formation (b) B_{11}^{+} ion implantation (c) Poly-Si gate pattern (d) Spacer forming (e) Source/Drain forming and Al deposition



(a)



(b)



(c)

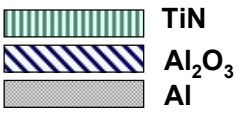


Fig. 2-3 Process of in-situ measure sample. (a)Al_2O_3 (15nm) and TiN (40nm) deposition (b) capacitance region etching (c) Bonding Al pad formation.

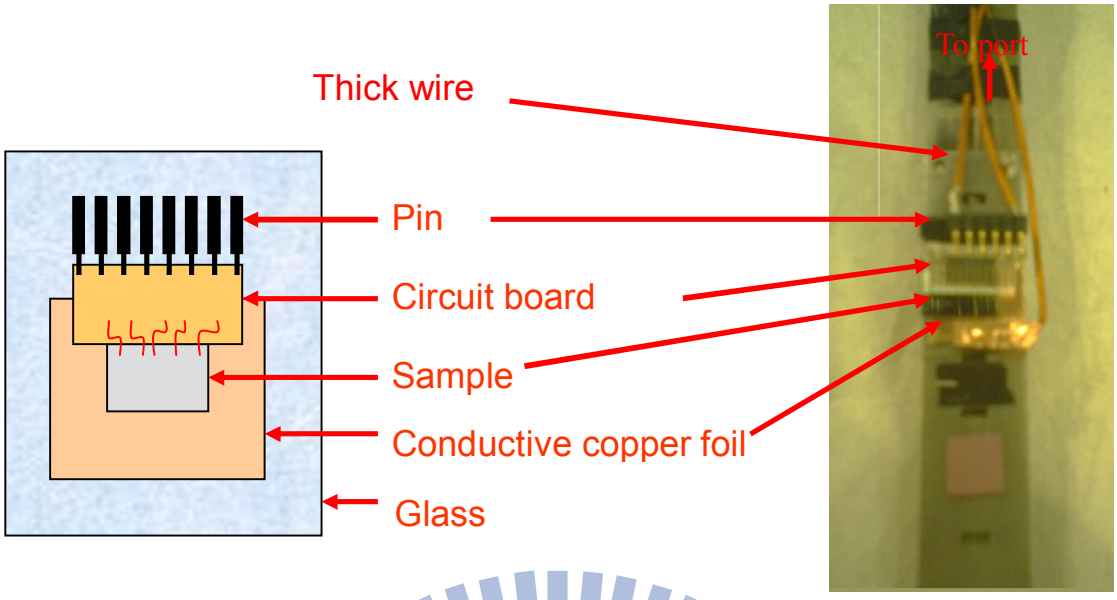


Fig. 2-4 Top view of in-situ measure sample.

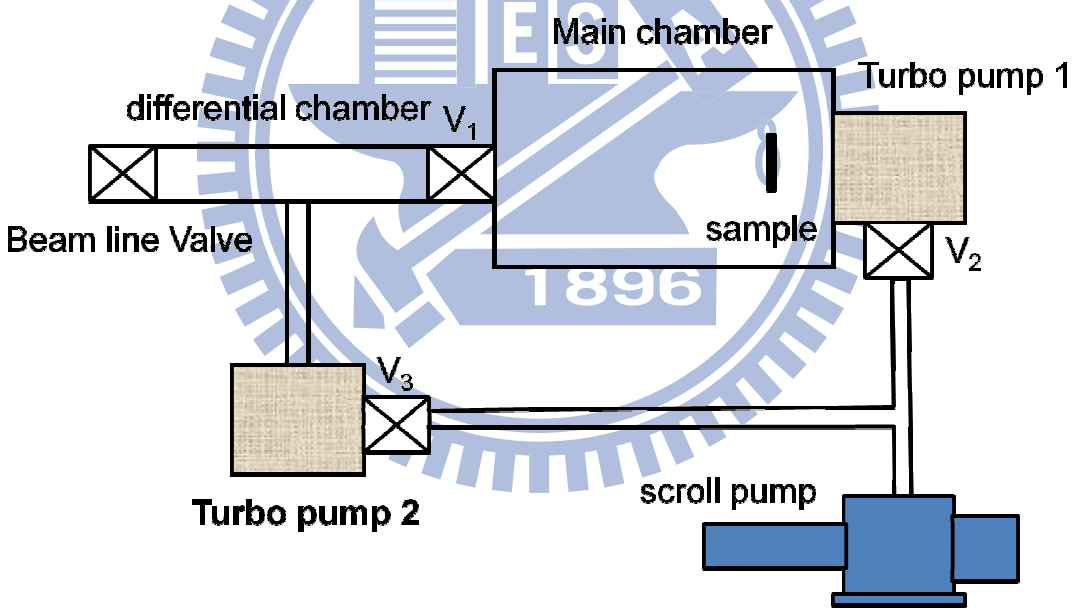


Fig. 2-5 The system module of the experiment chamber

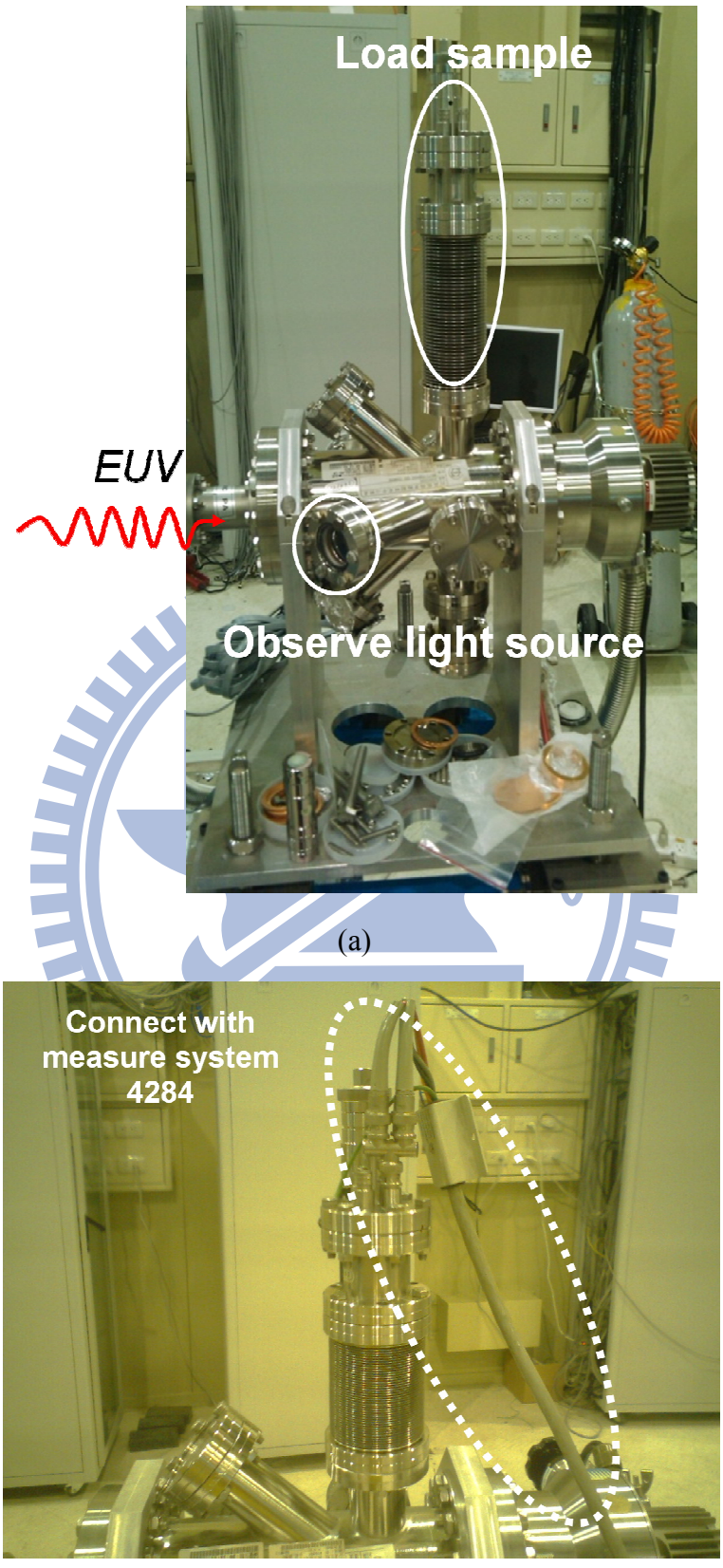


Fig. 2-6 (a) Photo of the experiment champer. (b) The output port position connect with measure system 4284b.

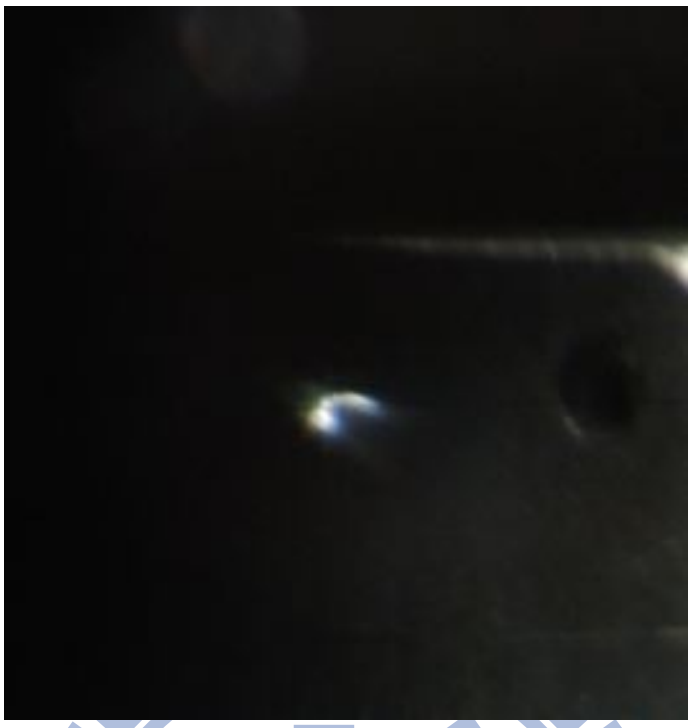


Fig. 2-7 Smiling shape of bean line and the size is 0.016 cm^2

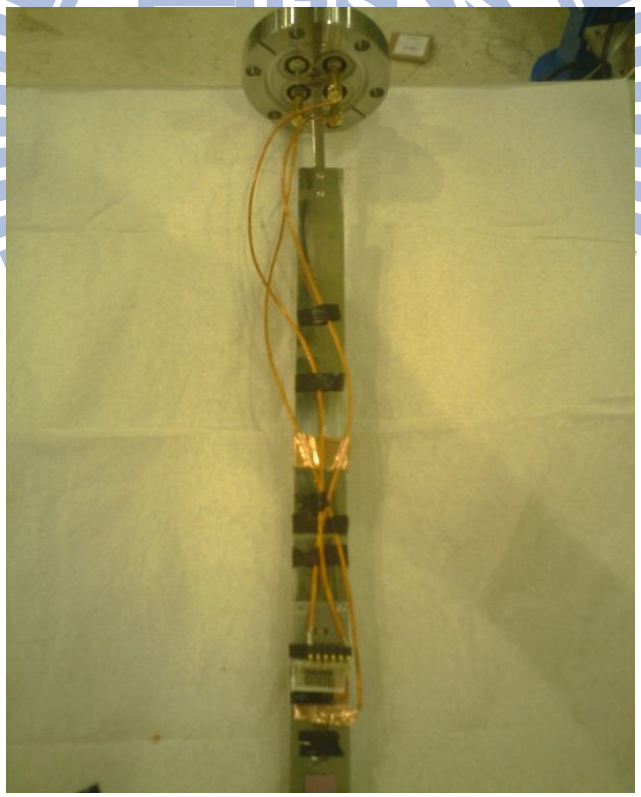


Fig. 2-8 Outlook of sample rod which is connect to the in-situ measure sample.

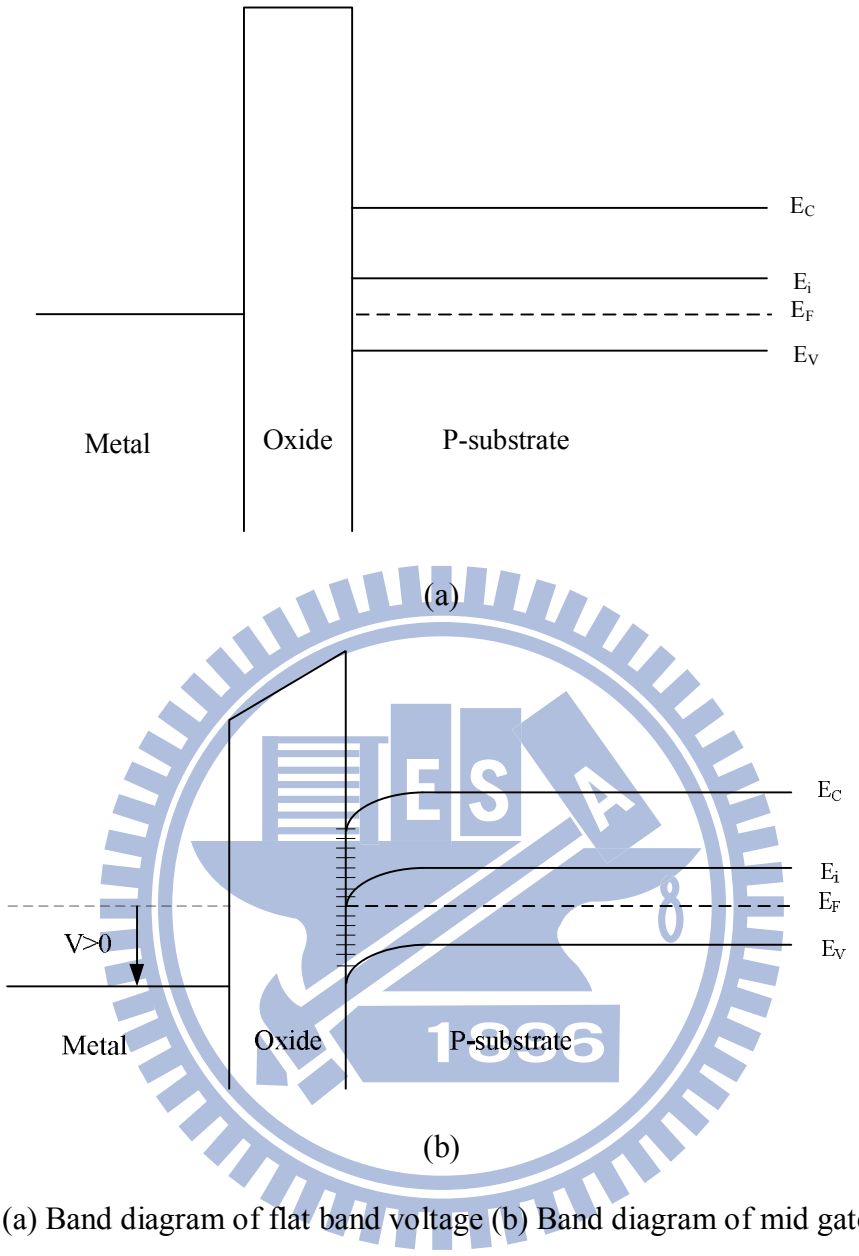


Fig.2.9 (a) Band diagram of flat band voltage (b) Band diagram of mid gate voltage.

Chapter 3

Results and Discussion

3-1 Introduction

In this chapter, the characteristics of the MIS capacitors and MOSFETs with various gate dielectrics before and after EUV irradiation are investigated. From the C-V characteristics, the MIS capacitors with five kinds of dielectric are analyzed and discussed. The main process of these capacitors has been mentioned in the previous chapter. Table 3-1 lists the dielectrics used in this thesis and the processess how they were deposited. The radiation hardness on each dielectric by various doses, the magnitude of flatband voltage shift (ΔV_{fb}) and mid-gap voltage shift (ΔV_{mg}), recovering with time, and leakage current are evaluated.

MOSFETs with two difference gate dielectrics are also examined in this chapter. As we know, the performance of MOSFETs mostly depends on the gate dielectric quality. Nevertheless, while irradiating by EUV, gate dielectric is the easiest part to be damaged. The every degradations of capacitor causing by EUV irradiation are also observed on MOSFETs. It is observed that the V_{th} shift and subthreshold swing degradation are all correlated to the damages in gate dielectric. The difference of gate leakage current and off-state current between pre-EUV irradiation and post-EUV irradiation is observed.

3-2 EUV Irradiation on MIS capacitors

3-2-1 Basic Electrical Characteristics

The radius of the capacitors, except the ALD Al_2O_3 sample, is 13.75 μm so the

capacitor area is $5.93x10^{-4}$ cm^2. For the ALD Al_2O_3 sample, the capacitor area is $4x10^{-4}$ cm^2. All of the C-V curves are measured by a precision LCR meter of model Agilent 4284B, the frequency of the small signal is set at 100 kHz and the magnitude is 25 mV.

The initial C-V characteristics of the MIS capacitors with five different gate dielectrics are shown in Fig. 3-1 to Fig. 3-5. The flat band voltages of the SiO_2, MOCVD Al_2O_3, HfSiO, HfAlO and ALD Al_2O_3 samples are -0.26 V, +1.17 V, -0.09 V, +0.66 V and +0.18V in sequence.

Hysteresis of C–V curve is commonly observed on high-k materials and it is also an important parameter to determine whether the high-k material can be used in MOSFET or not, so hysteresis needs to be minimized. Our SiO_2 and MOCVD Al_2O_3 samples exhibit almost negligible hysteresis. However, on the HfSiO, HfAlO and ALD Al_2O_3 samples, significant hysteresis are observed. The magnitudes of hysteresis are 0.09 V, 0.06 V and 0.124 V, respectively. Fig. 3-6 and Fig. 3-7 shows the TEM micrographs of the MOCVD Al_2O_3 and the ALD Al_2O_3, respectively. A 5-nm-thick interfacial layer (IL) is observed on the MOCVD sample. This is because the deposition temperature of MOCVD is 500 ^oC. At this temperature, the high-k material can interact with the Si substrate. The composition of the IL is SiO_x. Although the IL quality is not good, it provides a better interface between high-k dielectric and Si substrate. The ALD Al_2O_3 sample suffers from the worst hysteresis, because there is no IL at the interface. In fact, the hysteresis phenomenon could be reduced by RTA or another thermal process. Fig. 3-8 compares the C-V curves of the ALD Al_2O_3 sample before and after annealing in high vacuum at 300 ^oC for 30 min. The hysteresis is reduced obviously after annealing. Therefore, all high-k samples discussed in the following are annealed at 300 ^oC for 30 min in high vacuum.

Dielectric constants are listed in Table 3-1. HfAlO has the highest dielectric

constant of 13.04, and follows by HfSiO, ALD Al_2O_3, MOCVD Al_2O_3 and SiO_2. The samples deposited by MOCVD have smaller dielectric constant then the theoretic value.

In Fig 3-6, it is obvious that the MOCVD Al_2O_3 sample have a rougher TiN/Al_2O_3 interface then the ALD Al_2O_3 sample. The MOCVD Al_2O_3 sample also has a thick IL at the Al_2O_3/Si interface which makes the MOCVD Al_2O_3 sample has a large effective oxide thickness (EOT) and a lower dielectric constant.

3-2-2 Dose Effect

The exposure energy of EUV photo resist is suggested to be 10~20 mJ/cm^2. The flux of the beam line 08A1 at NSRRC is about $1x10^{12}$ photons/sec and the EUV energy is 91.85eV. Thus, the energy flux is $1x10^{12}$ x 91.85 x $1.6x10^{-19}$=0.0147 mJ/sec. The area of the EUV spot is about 0.016 cm^2, so the irradiation dose rate is 0.918 mJ/cm^2/sec[1]. In order to easily observe the irradiation damage, the EUV irradiation time is set to 60s and 300s which equals to 55.12 mJ/cm^2 and 275 mJ/cm^2, respectively. The SiO_2 sample used beam line 21B2 and the flux of 21B2 is 1 mJ/cm^2/sec.

The EUV beam spot are not so uniform. Fig. 3-9 (a) shows the 3 devices (on the same wafer) received EUV irradiation to a dose of 55.12 mJ/cm^2 and the 4 devices (on the other sample) received EUV irradiation to a dose of 275 mJ/cm^2. The C-V curves after EUV irradiation may distribute in a wide range due to the smiling shape EUV light spot shown in Fig. 3-9 (b). Therefore, the device with the most serious damage is selected to perform further analysis. In order to relax this problem for the future work, smaller capacitor area and higher device density to let device fit the beam spot are recommended.

As has been mentioned in chapter 1, EUV is a high energy light source. The e-h pairs would be generated when the EUV incidents dielectric and the C-V curve will shift due to the trapped charges and distort due to the increase of interface states. Fig. 3-10 to Fig. 3-14 show the effect of EUV irradiation on various dielectrics. When the samples are irradiated by EUV, the C-V curves of all samples shift toward negative voltage direction, this means net positive charges are produced in the dielectrics. When the irradiation time is longer, the C-V curves shift more negatively. C-V curve distortion is also observed when the samples receive high dose irradiation.

As the dose increases, we can find an interesting phenomenon: hysteresis gets worse. Not only the high-k samples but also the SiO_2 sample has this hysteresis phenomenon. This phenomenon suggests that EUV irradiation may generate some slow traps and border traps. However it is believed that the increasing of border traps is the main reason for our samples [49]. Border traps are easily generated by radiation damage. These traps may charge and discharge when the gate bias changes. Eventually they cause the hysteresis of the C-V curve. In our experiments, it is found that high-k material is much easier affected by the EUV irradiation. It is also observed that more border traps are generated in high-k materials in comparison with in SiO_2 dielectric. We could not make sure what kind of border traps are generated now (positive trap or negative trap). In the latter part of this chapter, we will discuss the self-annealing effect of the damages in dielectrics, some information will help us to distinguish what kinds of border traps are generated during EUV irradiation.

We use in-situ measurement to study the correlation between charge trapping and interface generation as the irradiation dose increases. Fig. 3-15 shows the in-situ measured C-V curve of the ALD Al_2O_3 sample. In the beginning of irradiation, the ALD Al_2O_3 sample quickly traps positive charges and the C-V curve shifts toward negative voltage. Nevertheless, as the dosage increases, the charge trapping rate in

Al_2O_3 seems to slow down. At the same time, the interface state density still increases quickly when dosage increases. The distortion of C-V curves in Fig. 3-14 is the evidence.

3-2-3 ΔV_{fb} and ΔV_{mg}

Different dielectrics have quit different responses to the EUV irradiation. It has been shown in Fig. 3-10~ Fig. 3-14 that different V_{fb} shifts are produced when the dielectrics are irradiated by EUV to the same dosage at the beam line 08A1. After EUV irradiation, the ΔV_{fb} of the SiO_2 sample shows the lowest magnitude of only -0.30V. The ΔV_{fb} of the HfAlO, HfSiO, and ALD Al_2O_3 samples are -0.99 V, -0.9 V, and -1.92 V, respectively. The MOCVD Al_2O_3 sample shows the worst ΔV_{fb} of -2.39 V. The ΔV_{mg} values are also extracted. They are -0.23 V for SiO_2 sample, -0.768 V for HfAlO sample, -0.77 V for HfSiO sample, -2.24 V for MOCVD Al_2O_3 sample, and -1.51V for ALD Al_2O_3 sample. From the Eq.2.4 and Eq.2.5, the ΔN_{ot} and ΔN_{it} on etch dielectrics can be calculated. These values are listed in Table 3-2. High-frequency method (Terman method) is also used to extract the energy distribution of the interface states before and after EUV irradiation. Fig. 3-16 shows the difference in the energy distribution of the interface states before and after EUV irradiation of all samples. It is obvious that after the EUV irradiation the interface state densities of all samples increase about one order of magnitude. And, the EUV generated interface states are donor-like and locate at the lower half of the energy gap of Si. . In Table 3-2, it is found that even if the MOCVD Al_2O_3 sample have the largest V_{fb} and V_{mg} shifts, the magnitudes of ΔN_{ot} and ΔN_{it} are not consistent with the ΔV_{fb} and ΔV_{mg}. We can understand this phenomenon from the Eq. 2.4 and Eq. 2.5. Because high-k materials have different dielectric constants, the extracted ΔN_{ot} and ΔN_{it} are affected by different

accumulation capacitances. From device point of view, MOCVD Al_2O_3 may suffer from the worst device application, but from the material aspect, MOCVD Al_2O_3 is not the worst dielectric on radiation hardness.

In Table 3-2, it is observed that after EUV irradiation the ALD Al_2O_3 sample suffers from the worst hysteresis and ΔN_{it}. However the MOCVD Al_2O_3 sample suffers from the worst ΔV_{fb} and ΔN_{ot}. From the TEM micrograph, it is known that there is no SiO_2-like IL on the ALD Al_2O_3 sample. Since the SiO_2 sample exhibits the best radiation hardness, the SiO_2-like IL results in better radiation hardness so the ΔN_{it} of MOCVD Al_2O_3 sample is lower then that of the ALD Al_2O_3 sample. The ALD and MOCVD Al_2O_3 samples both suffer from large ΔV_{fb} than the other samples after EUV irradiation. However, the MOCVD Al_2O_3 sample behaves worse than the ALD Al_2O_3 sample because the quality of ALD Al_2O_3 is better than the MOCVD Al_2O_3.

From the basic C-V curve measurements, it is observed that the SiO_2 sample has the best EUV hardness and the MOCVD Al_2O_3 sample is in the worst case. It is known that the radiation hardness is related to many factors like e-h pairs generation rate, bonding energy, and original trap density, etc. In this thesis, we use the same irradiation dosage for each high-k dielectric and higher irradiation dosage for the SiO2, but SiO_2 shows the best immunity to EUV irradiation. This result can be explained by several reasons. First, SiO_2 has the longest attenuation length (0.1 μm) in EUV range among these dielectrics. The attenuation length in SiO_2 is about 5 times longer than that in the other dielectrics. Owing to the longest attenuation length, SiO_2 absorbs less energy from EUV and then less e-h pairs are generated in SiO_2. Second, the growth temperature of SiO_2 is 900 ^oC, which is much higher than the deposition temperatures of the other dielectrics. The higher deposition temperature results in less original trap density in the dielectric and then less EUV generated e-h pairs would be trapped. Third, the band gap of SiO_2 is the largest. This property also makes e-h pairs

not generated so much.

For the high-k dielectrics, it is hard to predict their radiation hardness from a single factor. However, we can discuss the observed phenomena from two directions: charge generation and charge trapping. The amount of e-h pairs generated by EUV irradiation is the first essential factor. Total energy absorbed by dielectric, band gap, binding energy, and bond energy, ect., all of these factors determine the number of e-h pairs and eventually the number of charges may be captured in the dielectric. As we know, The band gap of Al_2O_3 is 8.8 eV and the band gap of HfO_2 is 6 eV. The band gap of HfAlO is between that of HfO_2 and Al_2O_3 and the band gap of HfSiO is between that of HfO_2 and SiO_2.When the same dose EUV irradiates on high-k samples, the attenuation length affects e-h pair generation less than the band gap because the high-k materials have similar attenuation length from 0.02μm to 0.029μm. Finally, more e-h pairs can be generated in HfAlO than the others because HfAlO has the narrowest band gap. Even if sufficient e-h pairs are generated, charges must be trapped in the dielectric so that they can affect the C-V curve and can be detected. Intrinsic traps or radiation induce traps might be important factors in charge capturing. Combining all of these factors we observe the experimental result of flat-band shift is MOCVD Al_2O_3(-2.39V) >ALD Al_2O_3(-1.92V) > HfAlO(-0.99V) > HfSiO(-0.9V). The ALD Al_2O_3 and MOCVD Al_2O_3 samples have the largest flat-band voltage shift of -2.39V and -1.92V. This suggests that even if Al_2O_3 have less e-h pairs due to its large band gap but it traps more charges. The trap density in the Al_2O_3 may be much higher than the other high-k dielectrics. The overall radiation hardness depends on several factors. When we need to predict radiation hardness of a material, all factors must be taken into consideration.

3-2-4 Recovery Property

After EUV irradiation, the MIS capacitors are damaged to different levels, we are curious about if these damages are permanent or not? Can they be fixed by time or another ways? The recovery properties of the MIS capacitors are shown in V_{fb}, V_{mg}, and hysteresis, and are discussed as follows.

In the previous sections, it has been shown that after EUV irradiation, the hysteresis is getting worse, and it is known that the hysteresis is caused by border traps generated by EUV. Interface traps also increase as the irradiation dosage increases, and the interface states cause C-V curve distortion. It is curious that is there any way to know what kinds of traps are generated by EUV in each dielectric? Would it be the same for every dielectric? Fig. 3-17(a) and Fig. 3-17(b) shows the C-V curves of the ALD Al_2O_3 sample at various times after EUV irradiation. Fig. 3-17(a) shows the C-V curves swept from negative voltage to positive voltage (forward sweep) and Fig. 3-17(b) shows the C-V curves swept from positive voltage to negative voltage (reverse sweep). We can combine these two figures into a full hysteresis loop. After EUV irradiation, the C-V curve distorts apparently and the hysteresis is getting worse. In Fig. 3-17(a) the distortion of the forward swept C-V curve quickly recovers in 2 hrs and the V_{fb} recovers to some extent. In this period, the reverse swept C-V, shown in Fig. 3-17(b), almost does not change. These phenomena implies that donor-type interface states and border hole-traps are generated by EUV irradiation and these defects can be annealed gradually. The decrease of interface states density reduces the C-V distortion and the decreasing of border traps reduce the hysteresis. After 2 hrs, the C-V curve in forward sweep and reverse sweep shift in parallel. This means the decreasing of border traps and interface traps slow down, and the detrapping of the positive charges trapped in the dielectric dominates the C-V curve

shift.

Fig. 3-18 shows that the distortion and hysteresis of the C-V curve do not change with time and only C-V shift occurs on the SiO_2 sample. These phenomena imply that very few border traps are generated and the EUV generated interface states cannot recover at room temperature. In Fig. 3-19, the hysteresis of the MOCVD Al_2O_3 sample does not recover too much with time. But the distortion and shift of C-V curve reduces with time. These phenomena imply that the EUV irradiation generates both border traps and interface states in MOCVD Al_2O_3. The border traps do not recover with time while the interface states and the trapped holes recover gradually at room temperature.

The recovery of C-V curve of the HfSiO sample is shown in Fig. 3-20. Sever distortion of the C-V curve after EUV irradiation is observed. The distortion at the upper half of the C-V curve indicates lots of donor-like interface states distributed at the lower half of the Si band gap. These interface states cannot recover at room temperature. EUV irradiation also generates border traps so that the hysteresis increases after EUV irradiation. Some border traps disappear in a few minutes but the remaining border traps do not decrease after 660 sec. Fig. 3-21 shows the C-V curves of the HfAlO sample with time. It is interesting that after EUV irradiation, negative border traps are generated. This is quite different from the other sample on which positive border traps are generated. Part of the border traps disappears in 600 sec. However, the remaining border traps, interface states, and trapped positive charges do not change up to 3600 sec.

Figure 3-22(a) ~ Fig. 3-26(a) show the flat band voltage and mid-gap voltage as a function of storage time at room temperature. It is clear that the shifts of flat band voltage and mid-gap voltage recover with time. This phenomenon is explained as follows. The shifts of flat band voltage and mid-gate voltage after EUV irradiation is

mainly due to hole trapping. The trapped holes in dielectrics are not stable, they will detrap to substrate and/or gate or neutralized by electrons from substrate and/or gate. Therefore, the main reason of V_{fb} and V_{mg} recovery is the vanish of the trapped holes, we find all C-V curves will come closer and closer to the original curve with time. Immediately after EUV irradiation, the whole dielectric is charged with the trapped holes so that a huge V_{fb} and V_{mg} shift occur. However, the charges near the Si substrate and gate electrode could not stay for a long time. They quickly tunnel into substrate and gate electrode in a short time. On the contrast, the charges trapped in the bulk of the dielectric need weeks to months or even years to escape.

From the previous discussion we can find that the hysteresis will be self-annealed within 10 minutes to 2 hours after EUV irradiation and it begin to slow down. The self-annealing of hysteresis can also be observed in Fig. 3-22(a) to Fig. 3-26(a). The semi-log plots show that the hysteresis does not decrease as quick as ΔV_{fb} and ΔV_{mg}. This means that the border traps keep in a much stable situation and the positively shift of the whole C-V curve is dominated by the hole detraping.

The recovery (self-annealing) is almost like the reverse sequence of radiation damage. When the EUV irradiation damages the capacitor, the dielectric traps positive charges and have interface states increasing. Form Fig. 3-22(a) to Fig. 3-26(a), we can basically see the positive charges discharge from the dielectric. The ΔN_{it} annealing with time can be estimated from Eq.2.5. Figure 3-22(b) to Fig. 3-26(b) show that the ΔN_{it} decreases with time, which means the interface states are also self-annealed. In fact, the C-V curve distorts from the original C-V curve after EUV irradiation, the distortion gradually recovers to the original shape, this is also an evidence of N_{it} decrease.

Compared with the ALD Al_2O_3 sample, the ΔN_{it} self-annealing of the MOCVD Al_2O_3 sample is much slower. The MOCVD Al_2O_3 sample shows about 50% ΔN_{it}

annealing after $5x10^6$ sec, but the ALD Al_2O_3 sample anneals more than 60% ΔN_{it} after $5x10^5$ sec. This is because the SiO_2-like IL makes the N_{it} annealing of the MOCVD Al_2O_3 sample behaves similar to the SiO_2 sample.

3-2-5 In-situ Measurement versus Ex-situ Measurement

In-situ measurement and ex-situ measurement were performed on the ALD Al_2O_3 sample. Different responses to the same sample in the same irradiation dosage are observed.

The difference between these two measurements is the setup during the EUV irradiation. For the ex-situ measurement, the sample is directly stuck on the sample holder and the electrodes of the sample are floating during the whole irradiation period. The in-situ measurement allows us to monitor the device characteristics during the irradiation, so it can reduce the experiment times. We only have to do the vacuum chamber operation once to get the full information of the effects of various irradiation dosages. Because the in-situ measurement lets us measure the dosage effects on the same sample, it also can eliminate the variation between different samples. The electrodes of sample are connected to measurement equipment, i.e. Agilent 4284 for C-V during the EUV irradiation.

Figure 3-27 shows the in-situ and ex-situ measured C-V curves of the ALD Al_2O_3 sample after 157 mJ/cm^2 and 275 mJ/cm^2 EUV irradiation. Under the close irradiation dosage, it is obvious that the in-situ measurement detects much less interface states and border traps. This is because in the ex-situ measurement, the EUV generated e-h pairs cannot flow out of the dielectric, most of the electrons and holes will recombine in the dielectric eventually. The energy released during high energy e-h pairs recombination generates lots of border traps and interface states. On the

other hand, in the in-situ measurement condition, electrons transfer away from dielectric and only some trapped hole can generate border traps and interface states.

3-3 EUV Radiation on MOSFETs

In this section, we examine the characteristics of MOSFETs before and after EUV irradiation. MOSFETs with two different gate dielectrics, 15 nm SiO_2 and 15 nm Al_2O_3, are prepared. The gate electrode is a 150-nm-thick n^+ poly-Si. Basic electrical characteristics, dose effect, V_{th} shift and swing degradation, and leakage current affected by EUV irradiation will be discussed. Finally, the correlation of radiation damages between MOSFETs and MIS capacitors caused by EUV irradiation will be discussed

3-3-1 Basic Electrical Characteristics

The gate width and gate length of all MOSFETs measured are 150 μm and 20 μm, respectively. Fig. 3-28 shows the basic transfer characteristics of the SiO_2 and Al_2O_3 MOSFETs. The initial subthreshold swing of the SiO_2 MOSFET is about 109 mV/dec. The on-current is about $1x10^{-4}$ A and the leakage current in the off-state is about $3x10^{-12}$ A. The on/off current ratio is $3.33x10^7$. The transfer characteristic of the Al_2O_3 MOSFET is also shown in Fig. 3-28. At V_d = 0.1 V, there is a kink at the sub-threshold region. This kink indicates lots of interface states at the Al_2O_3/Si interface. The Al_2O_3 MOSFET shows an on-current of about $1.83x10^{-5}$ A and an off-current of $1.4x10^{-12}$ A. The on/off current ratio is $1.29x10^7$. The subthreshold swing is 110 mV/dec.

3-3-2 Dose Effect

Fig. 3-29 shows the dosage effects of the EUV irradiation on the SiO_2 MOSFET. After EUV irradiation, the transfer characteristic changes at some places. First, the whole I_d-V_g curve shifts negatively. It has been discussed in the previous section that e-h pairs are generated during EUV irradiation and some holes are trapped in the gate dielectric. The negative shift of the I_d-V_g curve confirms that there are also net positive charges be trapped in the gate oxide. Second, the subthreshold swing increases. This phenomenon indicates that under EUV irradiation, the interface state density between gate dielectric and substrate increases. This phenomenon has also been observed on the MIS capacitors. Holes are not only trapped in the gate dielectric but also transferred to the interface to generate interface states. Both degradations increase with the increase of irradiation dosage as shown in Fig.3-30 (a). Third, the leakage current in the off-state increases as the irradiation dosage increases. This is major degradation on the SiO_2 MOSFET by EUV irradiation. The leakage current can increase by two orders of magnitude. Fig. 3-30 (b) shows the leakage current of the SiO_2 MOSFET in the off-state as a function of dosage.

The I_d-V_g curve of the MOSFET using Al_2O_3 as gate dielectric is shown in Fig. 3-31. Similar to the Al_2O_3 MIS capacitor, the Al_2O_3 MOSFET is vulnerable and is easily affected by EUV irradiation. The subthreshold swing quickly degrades after a 55.12 mJ/cm^2 EUV irradiation, and then saturates. The leakage current in the off-state after EUV irradiation increases by orders of magnitude.

3-3-4 Leakage Current Mechanism

After EUV irradiation, the leakage current in the off-state increases, we are wandering what happened during the irradiation. Fig. 3-32 shows the I_d-V_g curve and

I_s-V_g curve. The I_d and I_s currents are different in the off-state. By analyzing the gate leakage current, the magnitude of gate current is very small. Under this bias the gate leakage current is about 10^{-12} to 10^{-13} A so it is not the main reason for the off-state leakage current. By measuring the n^+-p junction, it is found that the component of leakage current is cause by the junction leakage at reverse bias as shown in Fig. 3-33. At the reverse bias, the junction exhibits a high leakage current after EUV irradiation.

The junction leakage is caused by the interface state increased under the isolation oxide edge. Fig.3-34 shows mechanism of leakage current. EUV is hard to damage p-n junction, however the isolation oxide is very thick and it is easily damaged by EUV irradiation. After EUV irradiation the interface states increase under the isolation oxide just as the radiation induced interface states under gate oxide. As we apply a reverse bias, the interface states in the depletion region are as generation centers and the generation centers will contribute the leakage current. In the next section we also can find the leakage current decreasing with time and it is also consist with the decreasing of interface states.

3-3-5 Self-Annealing with time

The MOSFETs also exhibit self-annealing phenomena. The radiation damages don't change the MOSFETs permanently and they also changes with time. Figure 3-35 to Fig. 3-38 show how the SiO_2 MOSFET recoveries with time after 2hr EUV irradiation. In Fig. 3-35, the leakage current in the off-state decreases with time as depicted in Fig. 3-36. This means the interface states under the field oxide decreases. This phenomenon is consistent with the previous observation that the damages may be self-annealed at room temperature. The V_{th} and subthreshold swing also recover with time as shown in Fig. 3-37 and Fig. 3-38. The recovery of subthreshold swing

indicates the annealing of interface states under gate oxide. In the previous study on the MIS capacitors, positive flat-band voltage shift is observed during room temperature storage and is explained by the detrapping of the trapped holes. The positive shift of the I_d-V_g curve in Fig. 3-38 also refers to the same mechanism.

Table 3-1: The different MIS capacitors dielectrics fabricate condition and properties.

Dielectric	Gate	Forming Method	Deposition Temp.	Dielectric constant
SiO_2	TiN	Furnace	**900°C**	**3.7**
Al_2O_3	TiN	ALD	**300°C**	**7.9**
Al_2O_3	TiN	MOCVD	**500 °C**	**5.13**
HfSiO	TiN	MOCVD	**500°C**	**9.55**
HfAlO	TiN	MOCVD	**500°C**	**13.04**

Table 3-2: The different response of interface states, oxide traps and hysteresis in different material after EUV irradiation.

	SiO_2 (440mJ/cm^2)	**Al_2O_3** (MOCVD) (275 mJ/cm^2)	**HfAlO** (275 mJ/cm^2)	**HfSiO** (275 mJ/cm^2)	**Al_2O_3** (ALD) (275 mJ/cm^2)
V_{fb}	**-0.08 V (Best)**	**-2.39 V (Worst)**	**-0.9 V**	**-0.99 V**	**-1.92 V**
Hysteresis	**0.018V (Best)**	**0.216V**	**0.282**	**0.193V**	**0.353V (Worst)**
N_{ot}	**1.13x10^{11} (Best)**	**4.481x10^{12} (Worst)**	**4.32x10^{12}**	**3.64x10^{12}**	**3.37x10^{12}**
N_{it}	**9.4x10^{10} (Best)**	**3.9x10^{11}**	**2.64x10^{11}**	**2.73x10^{11}**	**7.2x10^{11} (Worst)**

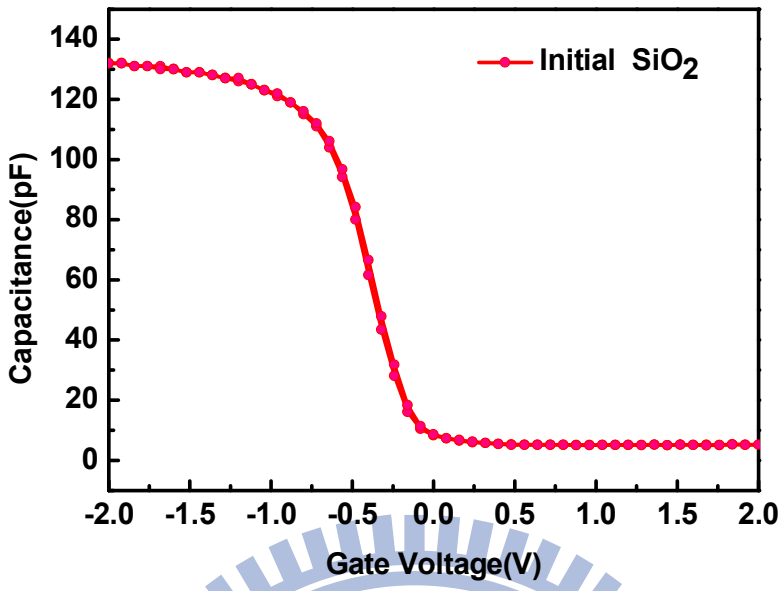


Fig. 3-1: High-frequency C-V curve of MIS capacitor with TiN metal gate and SiO_2 insulator at 100 kHz.

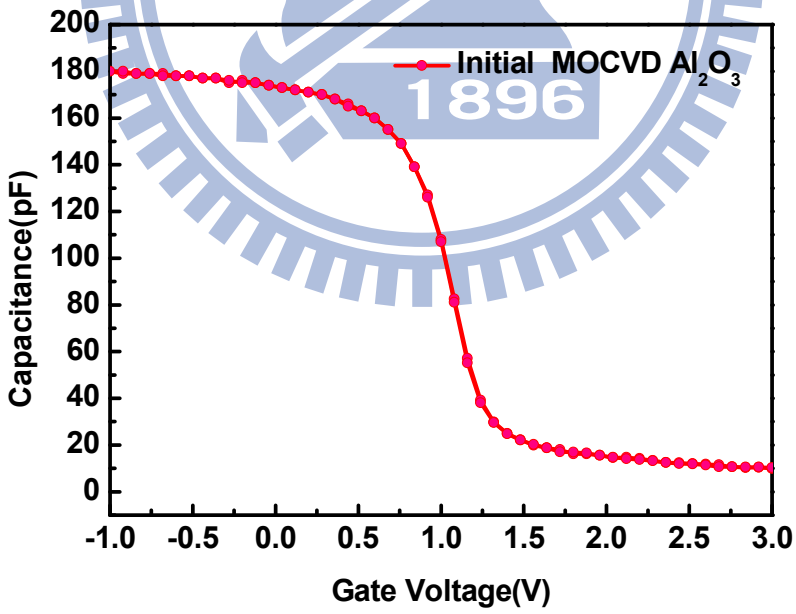


Fig. 3-2: Hhigh-frequency C-V curve of MIS capacitor with TiN metal gate and MOCVD Al_2O_3 insulator at 100 kHz.

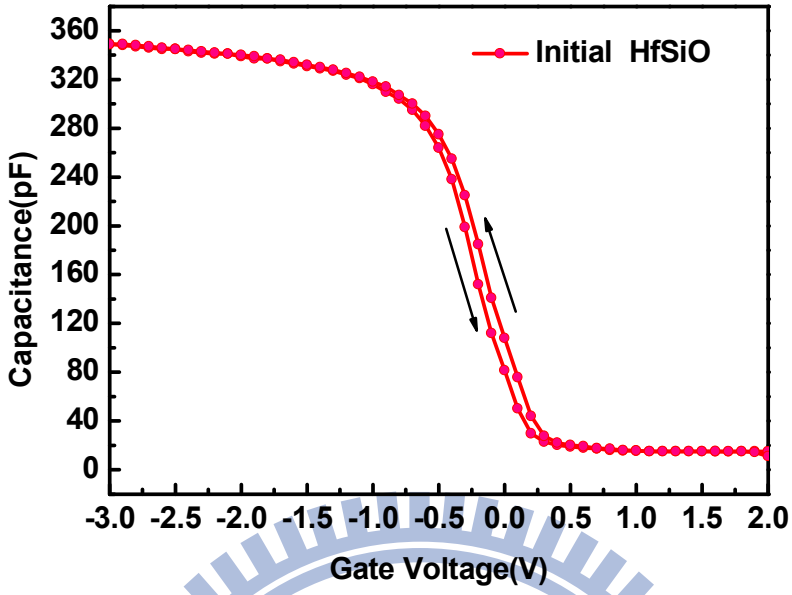


Fig. 3-3: High-frequency C-V curve of MIS capacitor with TiN metal gate and HfSiO insulator at 100 kHz.

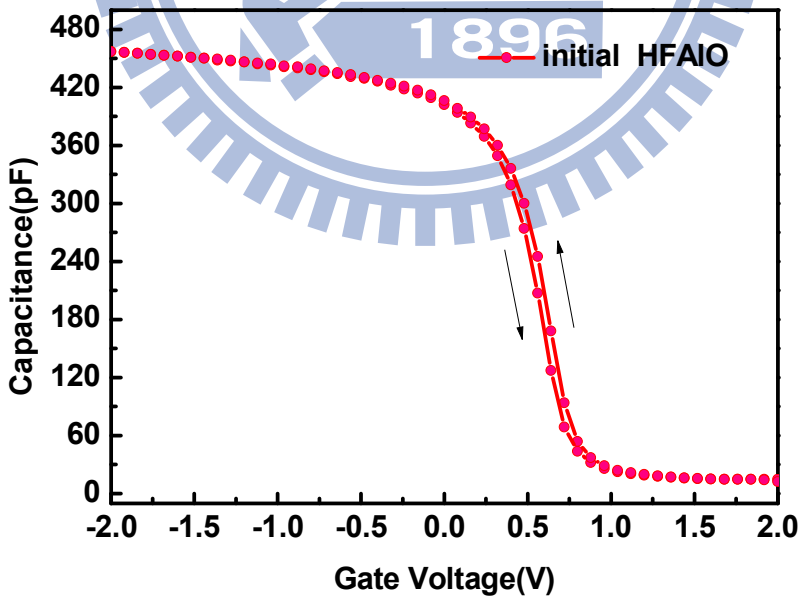


Fig.3-4: High-frequency C-V curve of MIS capacitor with TiN metal gate and HfAlO insulator at 100 kHz.

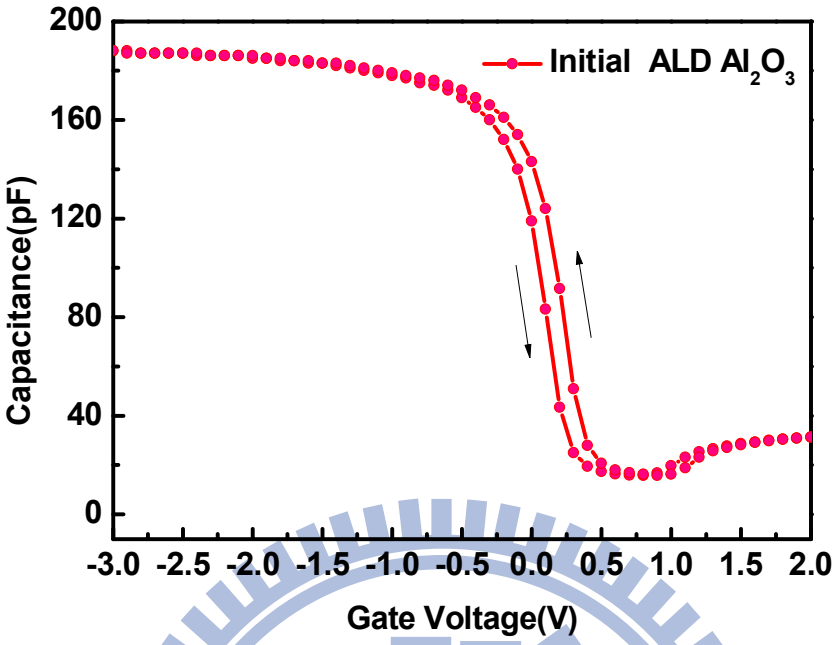


Fig. 3-5: High-frequency C-V curve of MIS capacitor with TiN metal gate and ALD Al_2O_3 insulator at 100 kHz.

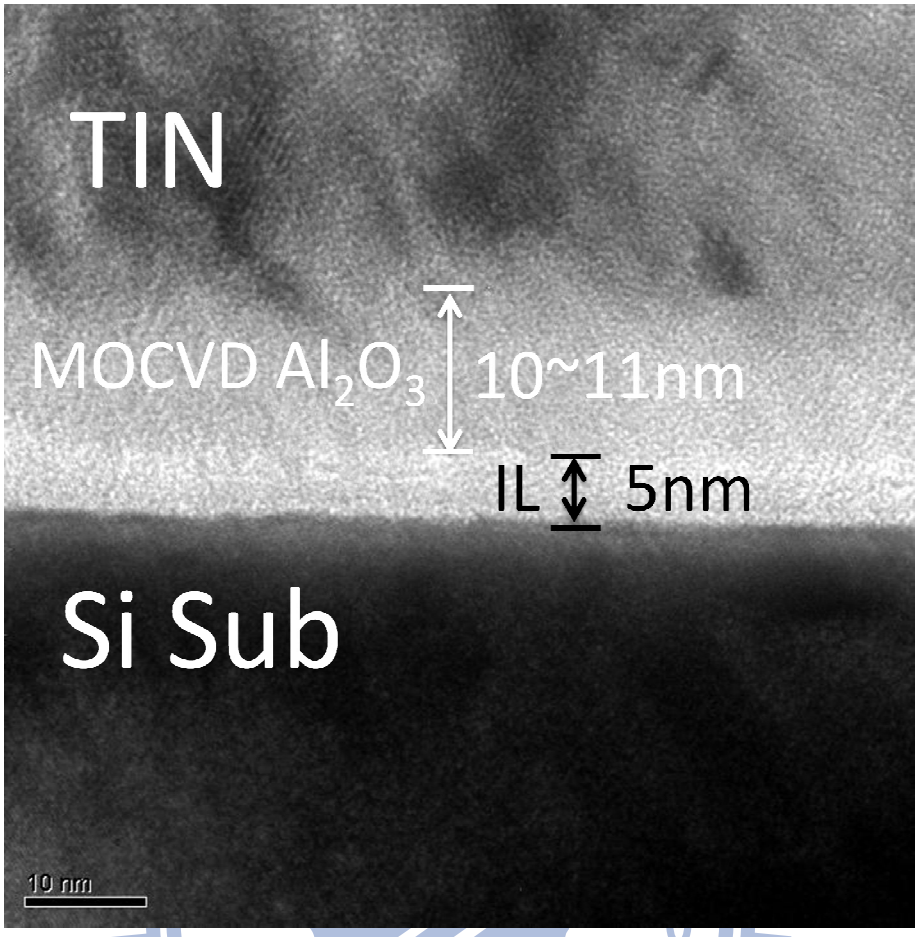
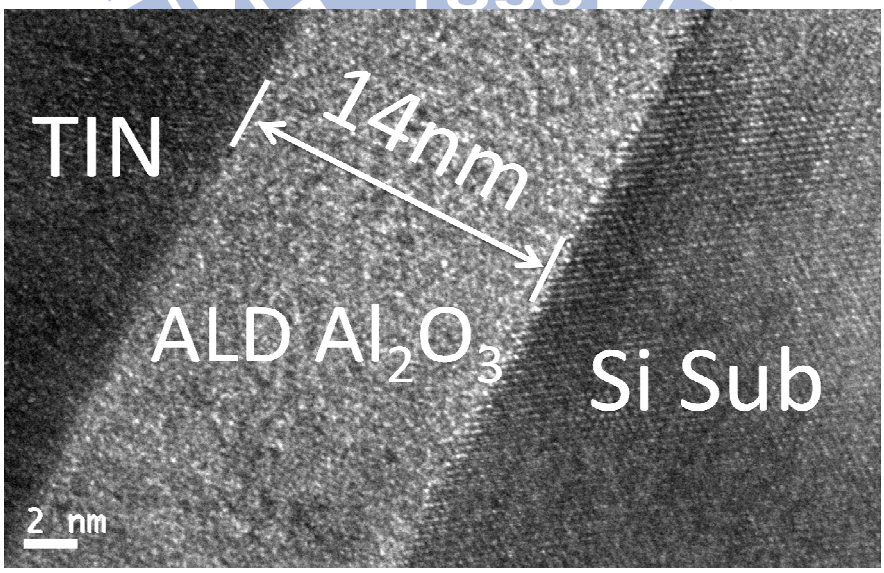


Fig. 3-6: Cross section of MOCVD Al_2O_3 with IL and rough surface between the TiN.



(b)

Fig. 3-7: Cross section of ALD Al_2O_3 without IL and smooth between the TiN.

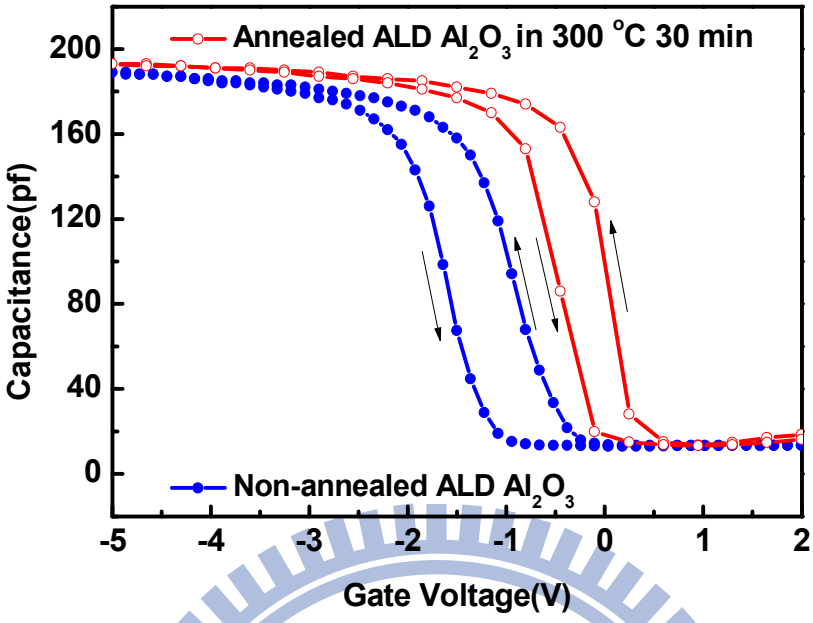
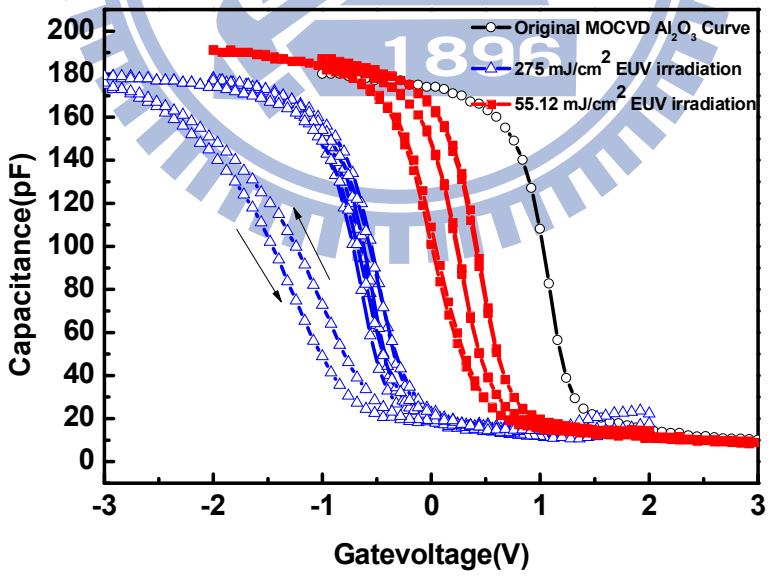


Fig. 3-8: Comparison of non-annealed and annealed High-frequency C-V curve of TiN + ALD Al_2O_3 capacitor after 300°C 30mins in high-vacuum furnace.



(a)

Fig. 3-9: Damage variation on one chip of MOCVD Al_2O_3 sample at 275mJ/cm^2 dosage and 55.12mJ/cm^2 dosage.

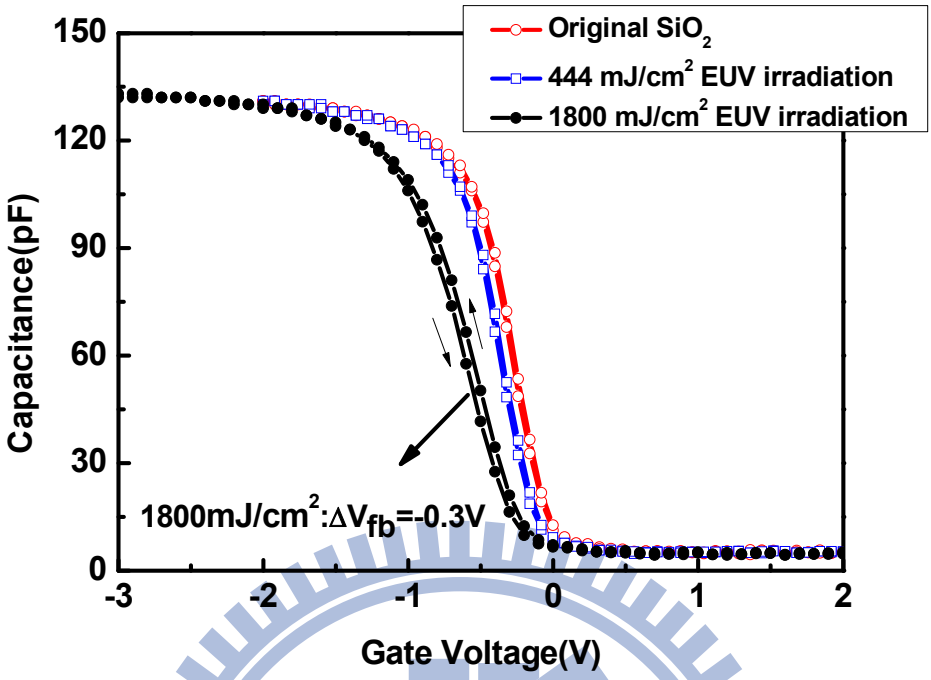


Fig. 3-10: High-frequency C-V curve of TiN+SiO_2 capacitor with EUV iradiation dosage at 444mJ/cm^2 and 1800mJ/cm^2.

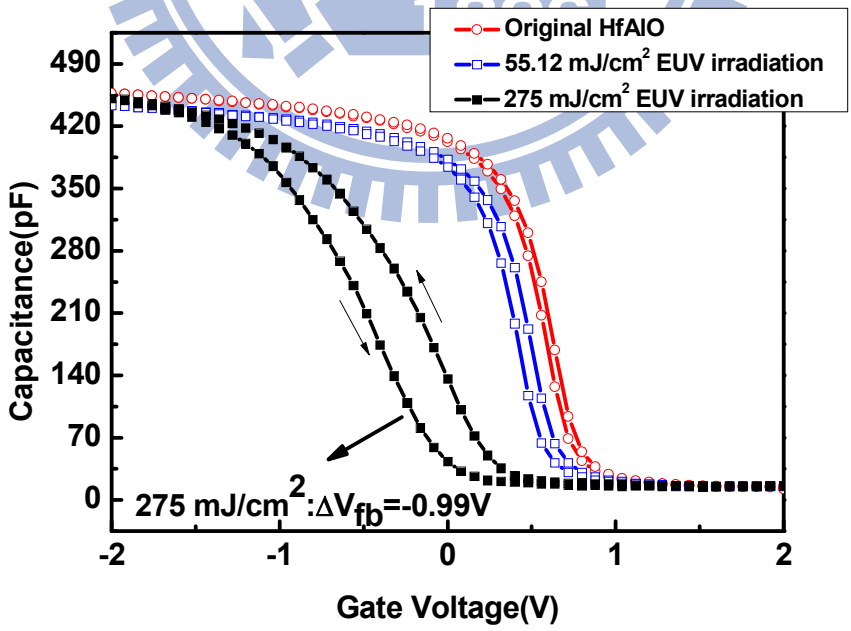


Fig. 3-11: High-frequency C-V curve of TiN + HfAlO capacitor with EUV irradiation dosage at 55.12 mJ/cm^2 and 275mJ/cm^2.

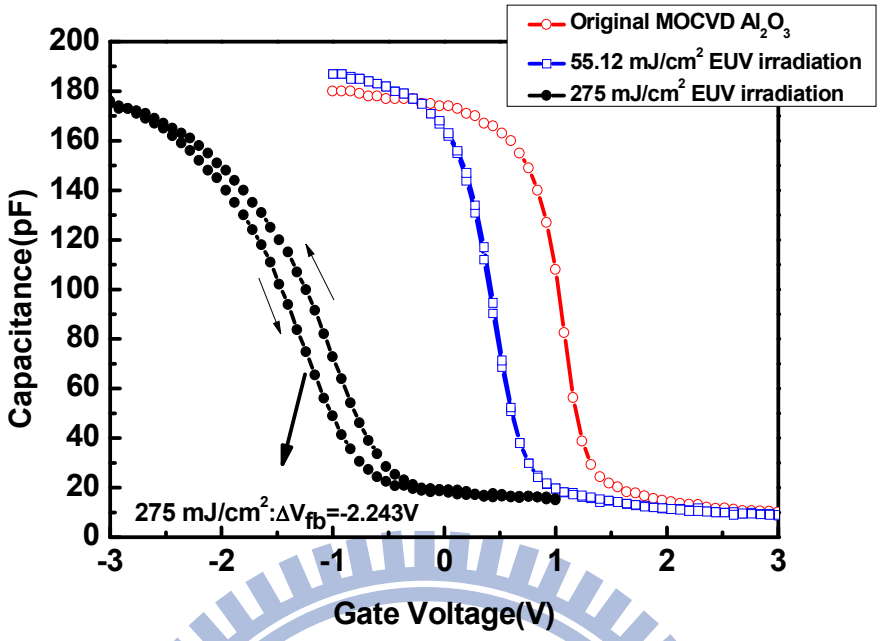


Fig. 3-12: High-frequency C-V curve of TiN + MOCVD Al_2O_3 capacitor with EUV irradiation dosage at 55.12 mJ/cm^2 and 275mJ/cm^2.

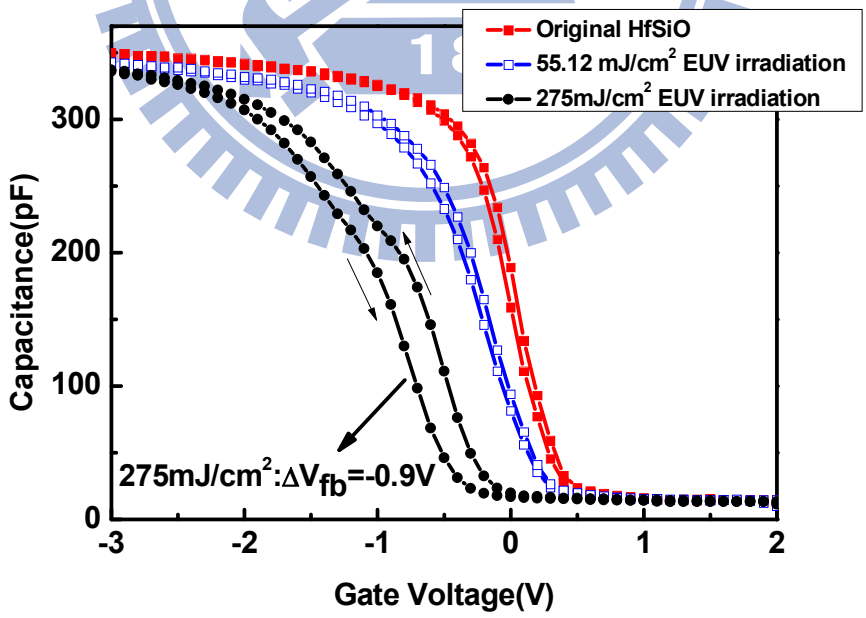


Fig. 3-13: High-frequency C-V curve of TiN + HfSiO capacitor with EUV irradiation dosage at 55.12 mJ/cm^2 and 275mJ/cm^2.

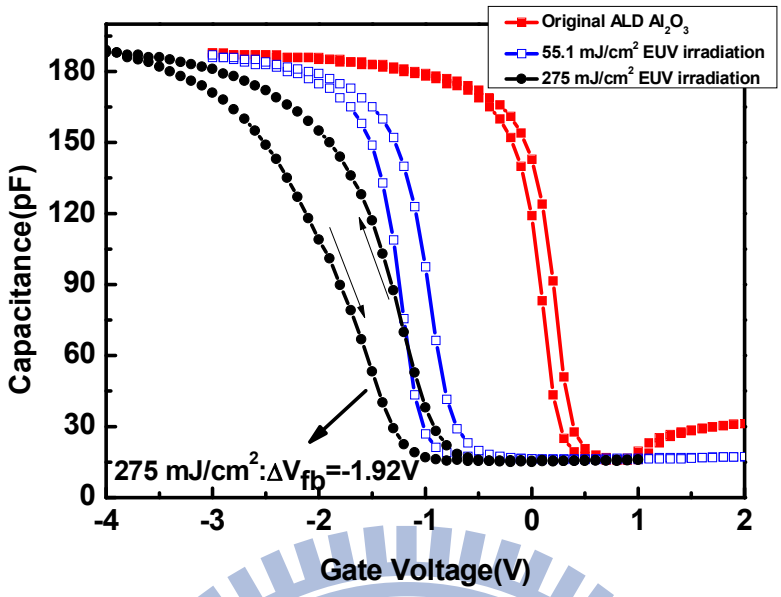


Fig. 3-14: High-frequency C-V curve of TiN + ALD Al_2O_3 capacitor with EUV irradiation dosage at 55.12 mJ/cm^2 and 275mJ/cm^2.

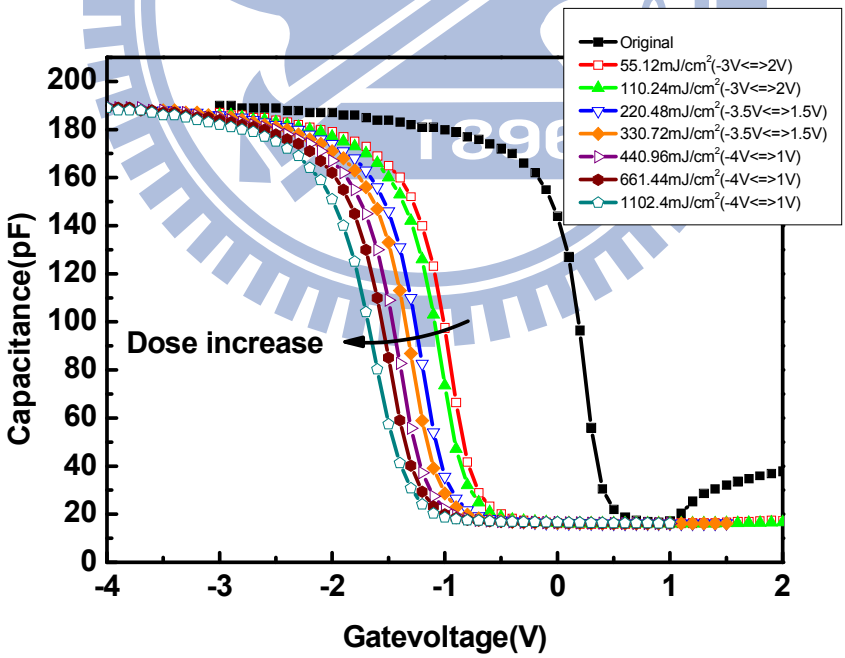
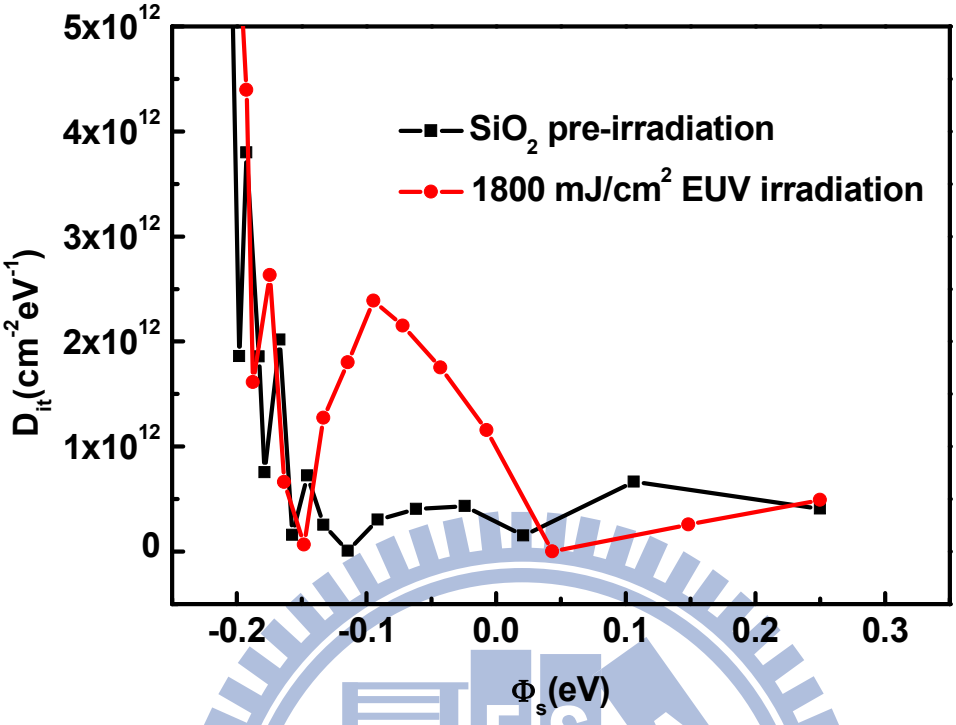
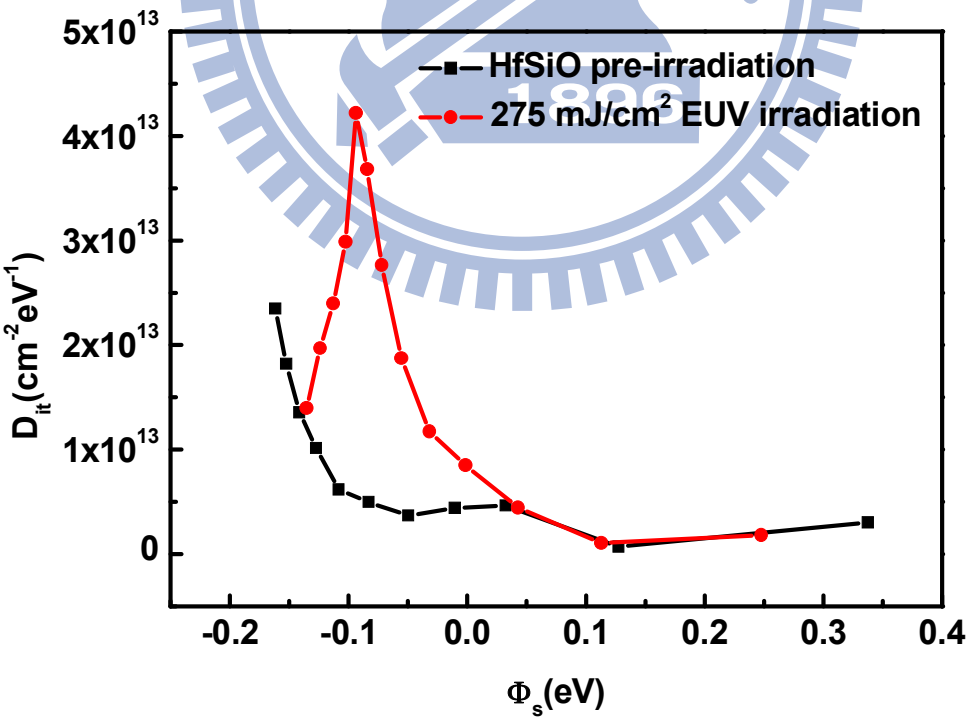


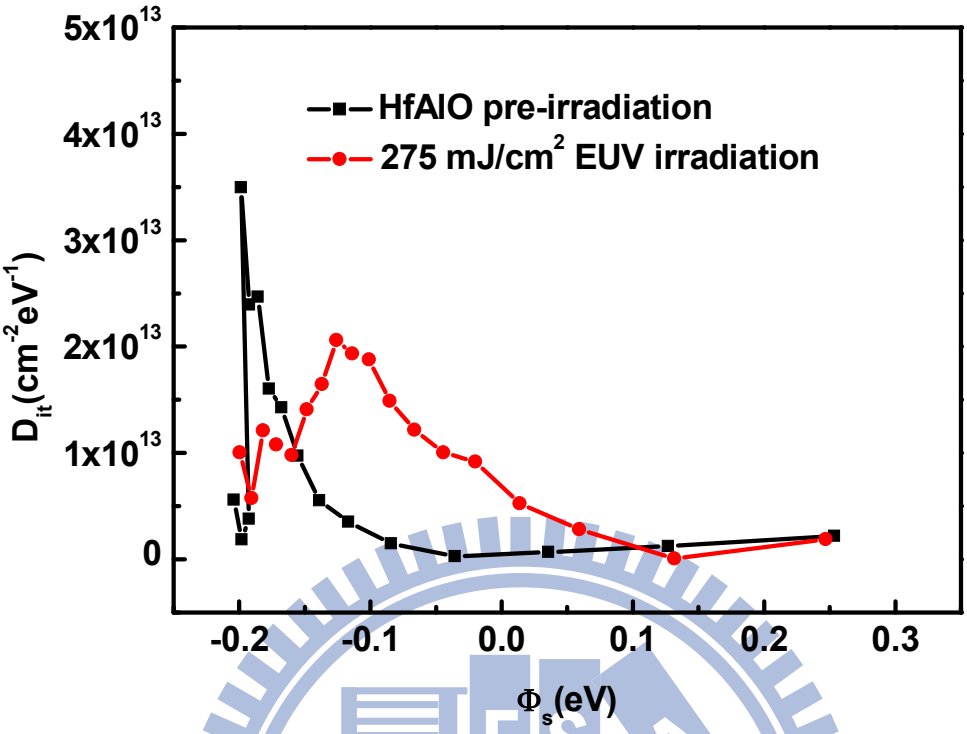
Fig.3-15: High-frequency C-V curve of in-situ TiN + ALD Al_2O_3 sample with EUV irradiation dosage from 55.12 mJ/cm^2 to 1102.4 mJ/cm^2.


5x10^12
4x10^12
3x10^12
2x10^12
1x10^12
0
D_it(cm^-2eV^-1)
SiO2 pre-irradiation
1800 mJ/cm^2 EUV irradiation
-0.2
-0.1
0.0
0.1
0.2
0.3
Φs(eV)

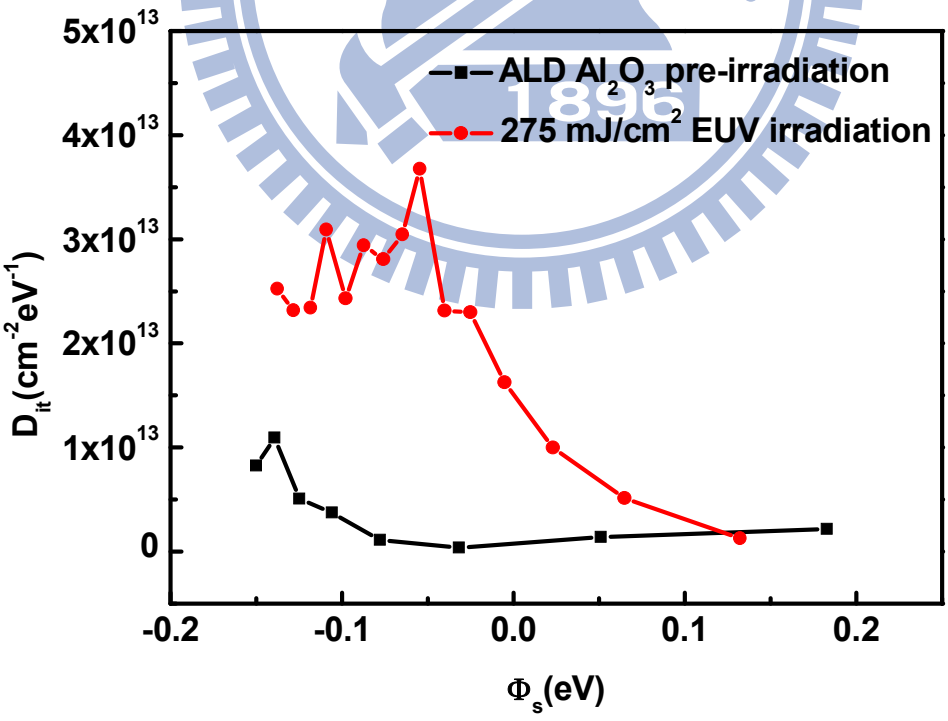
(a)


5x10^13
4x10^13
3x10^13
2x10^13
1x10^13
0
D_it(cm^-2eV^-1)
HfSiO pre-irradiation
275 mJ/cm^2 EUV irradiation
-0.2
-0.1
0.0
0.1
0.2
0.3
0.4
Φs(eV)

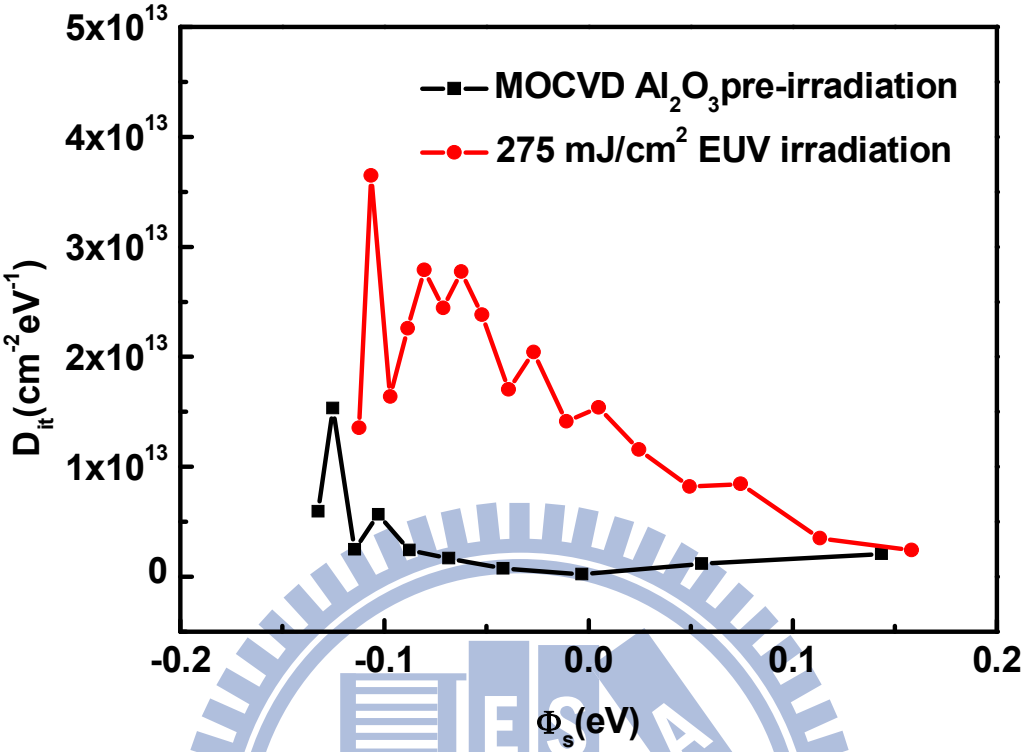
(b)


HfAlO pre-irradiation
275 mJ/cm2 EUV irradiation
Dit(cm-2eV-1)
Φs(eV)
5x10^13
4x10^13
3x10^13
2x10^13
1x10^13
0
-0.2
-0.1
0.0
0.1
0.2
0.3

(c)


ALD Al2O3 pre-irradiation
275 mJ/cm2 EUV irradiation
Dit(cm-2eV-1)
Φs(eV)
5x10^13
4x10^13
3x10^13
2x10^13
1x10^13
0
-0.2
-0.1
0.0
0.1
0.2

(d)



(e)

Fig. 3-16 Comparison of interface trap density as a function of surface potential between Pre-irradiation and after 1800mJ/cm^2 dosage for (a) SiO_2 and 275mJ/cm^2 dosage for (b) HfSiO, (c) HfAlO, (d) ALD Al_2O_3 and (e) MOCVD Al_2O_3 sample.

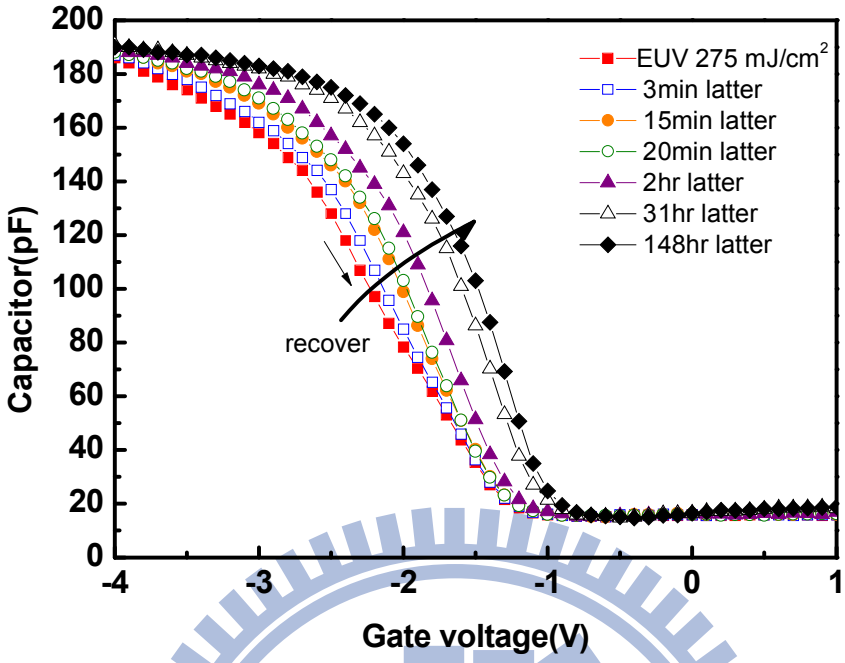


Fig. 3-17(a): Recovery behavior of ALD Al_2O_3 sample after 275mJ/cm^2 EUV irradiation for forward sweep high-frequency C-V curve.

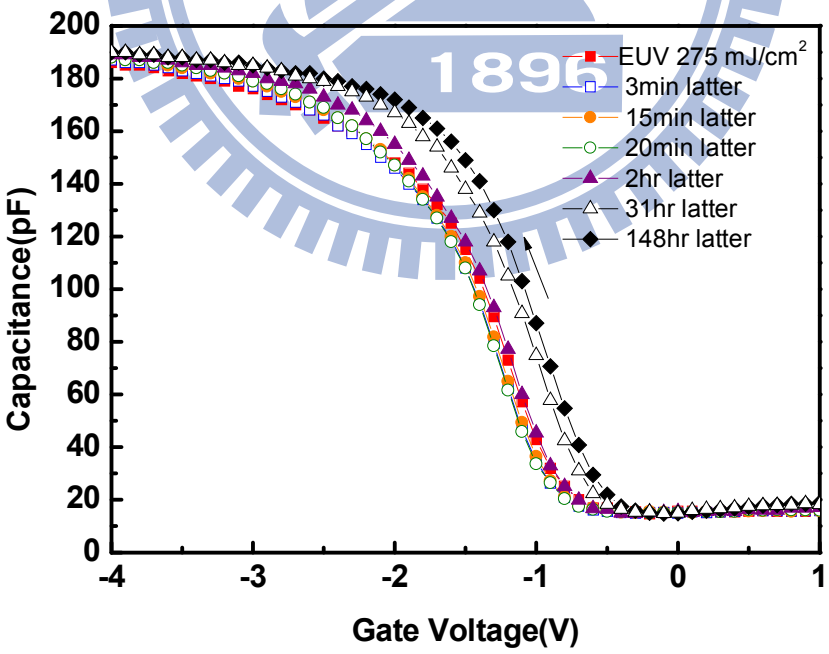


Fig. 3-17(b): Recovery behavior of ALD Al_2O_3 sample after 275mJ/cm^2 EUV irradiation for reverse sweep high-frequency C-V curve.

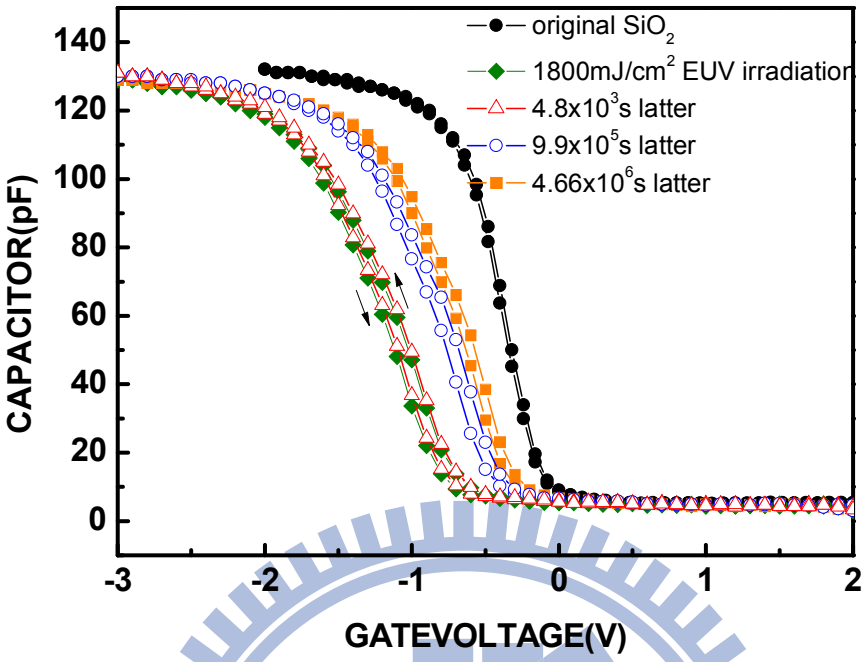


Fig. 3-18: High-frequency C-V curve of SiO_2 sample recovery behavior from $4.8x10^3$ s to $4.66x10^6$ s after 1800mJ/cm^2 EUV irradiation.

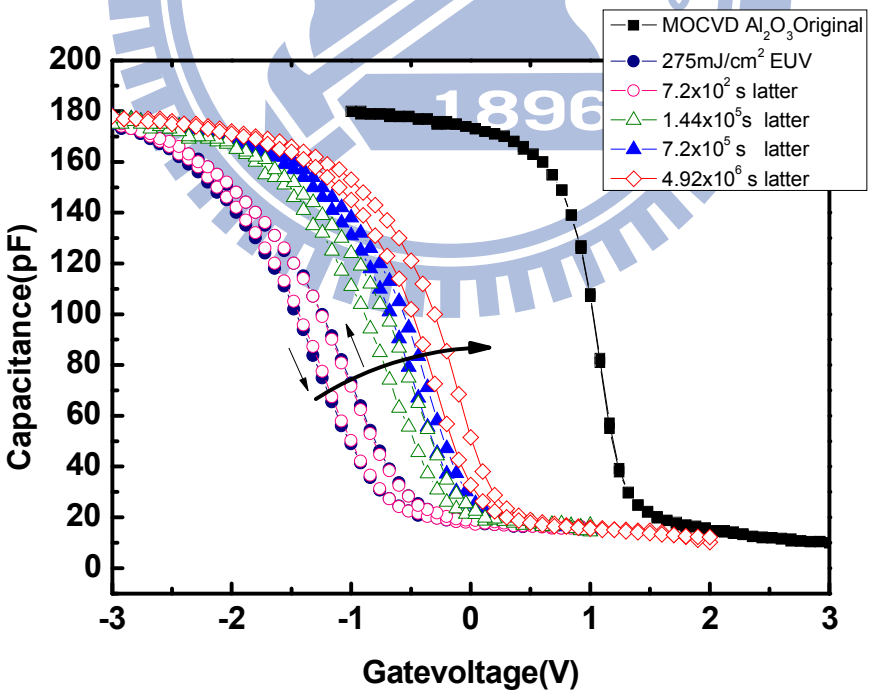


Fig. 3-19: High-frequency C-V curve of MOCVD Al_2O_3 sample recovery behavior from $7.2x10^2$ s to $4.92x10^6$ s after 275 mJ/cm^2 EUV irradiation.

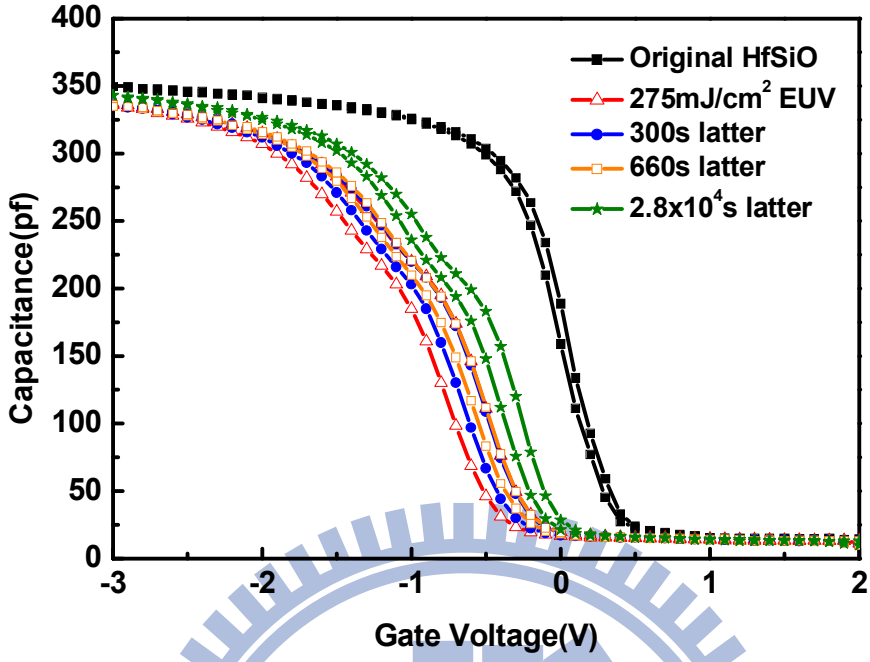


Fig. 3-20: High-frequency C-V curve of HfSiO sample recovery behavior from $3x10^2$ s to $2.8x10^4$ s after 275 mJ/cm^2 EUV irradiation.

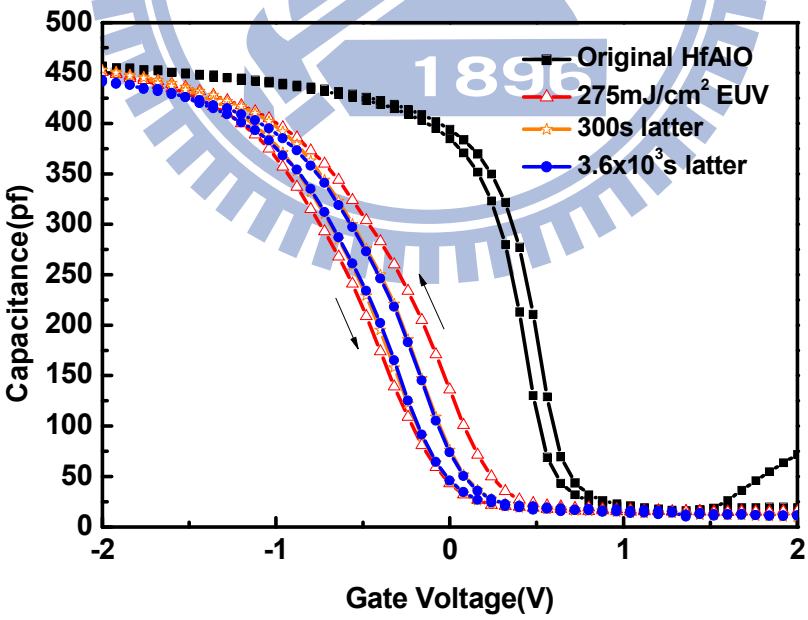


Fig. 3-21:High-frequency C-V curve of HfAlO sample recovery behavior from $3x10^2$ s to $3.6x10^3$ s after 275 mJ/cm^2 EUV irradiation.

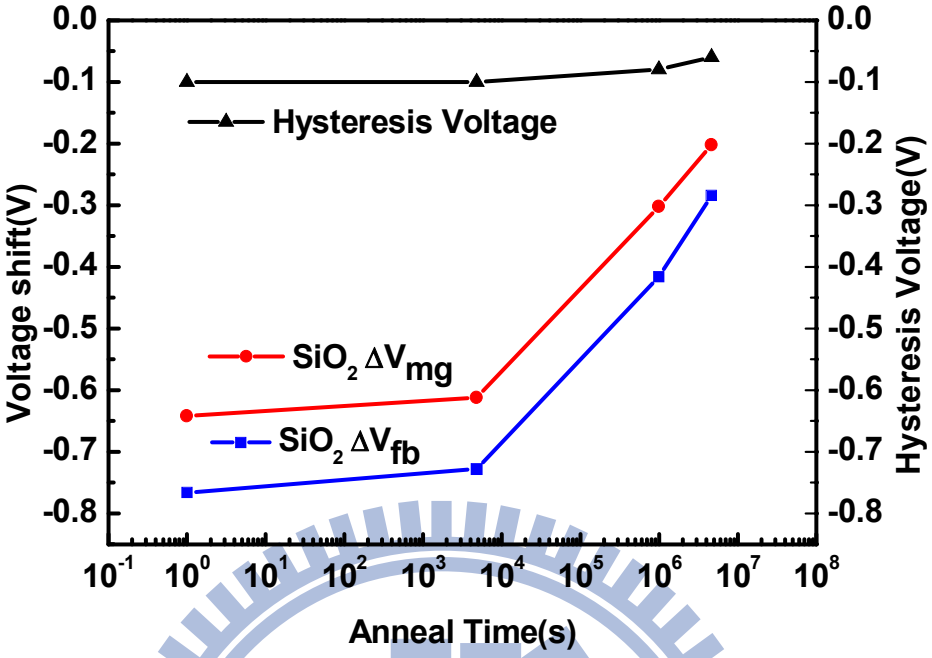


Fig. 3-22(a): Hysteresis voltage, ΔV_{fb} and ΔV_{mg} as a function of time of SiO_2 sample.

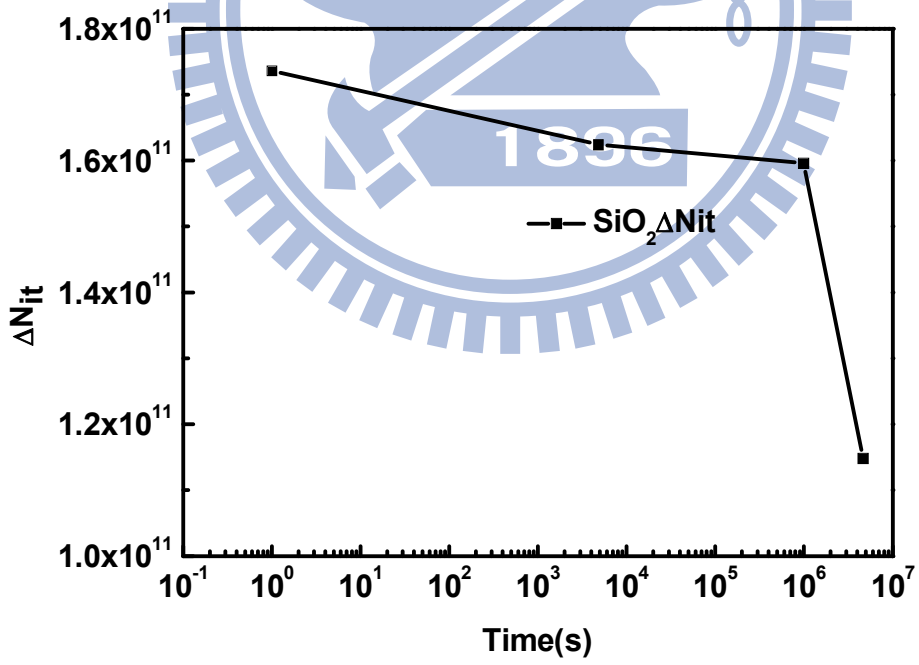


Fig. 3-22(b): The ΔN_{it} values as a function of time of SiO_2 sample.

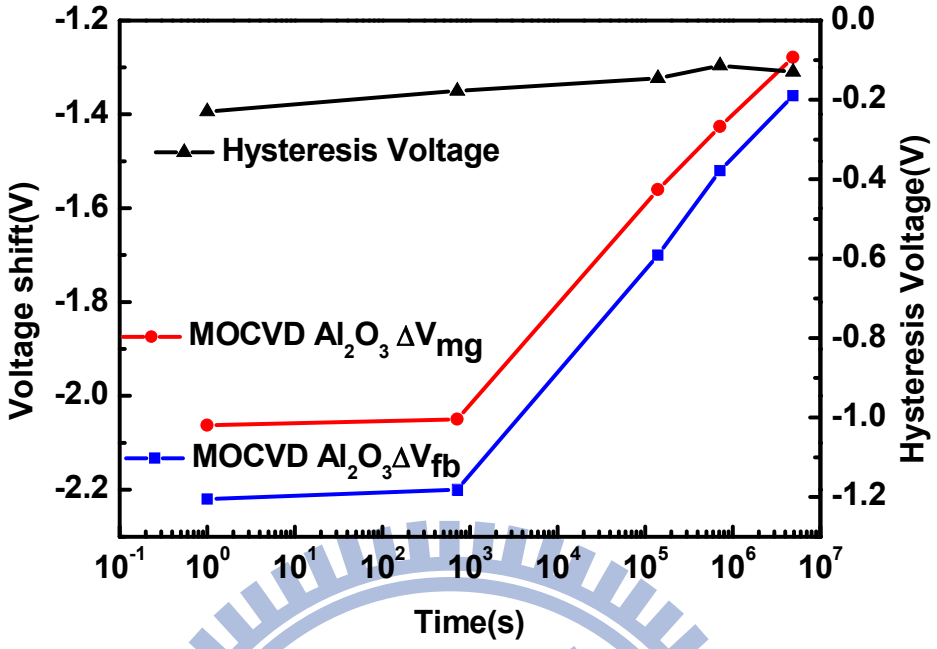


Fig. 3-23(a): Hysteresis voltage, ΔV_{fb} and ΔV_{mg} as a function of time of MOCVD Al_2O_3 sample.

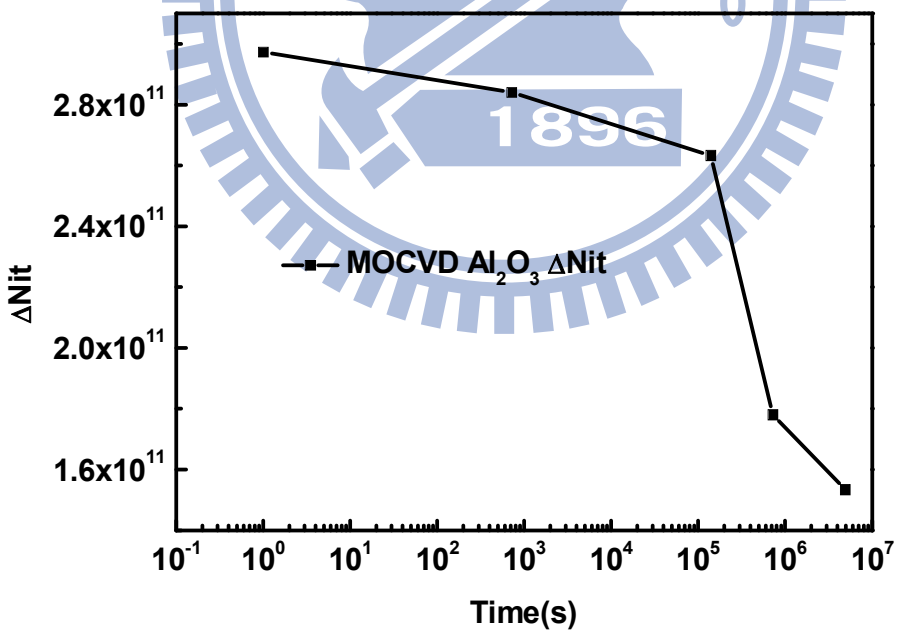


Fig. 3-23(b): The ΔN_{it} values as a function of time of MOCVD Al_2O_3 sample.

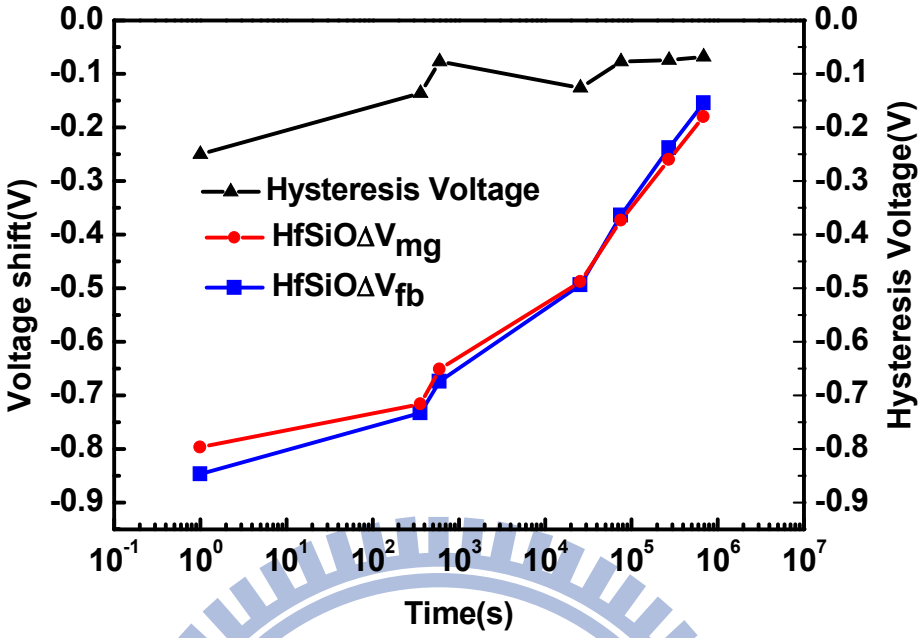


Fig. 3-24 (a): Hysteresis voltage, ΔV_{fb} and ΔV_{mg} as a function of time of HfSiO sample.

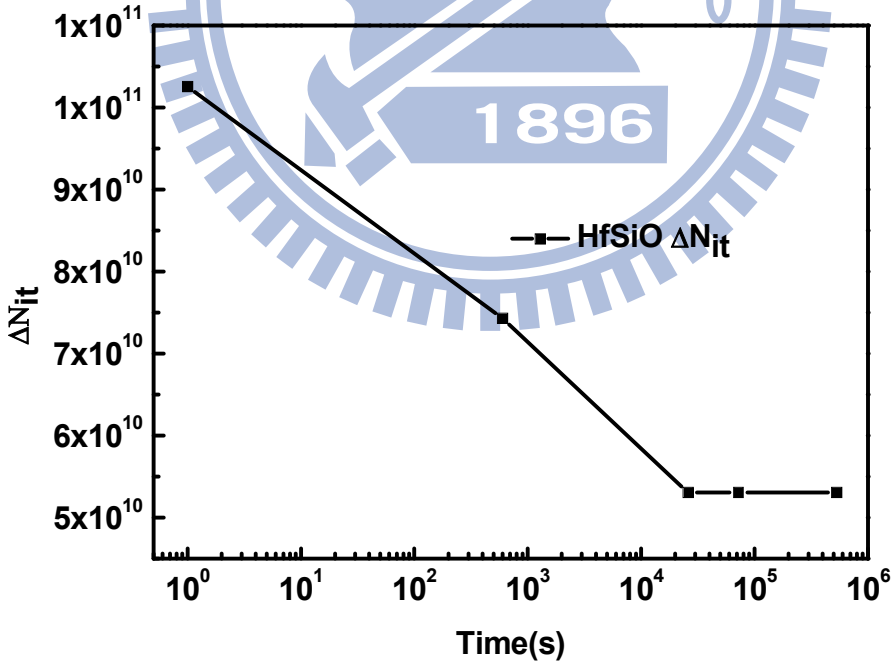


Fig. 3-24(b): The ΔN_{it} values as a function of time of HfSiO sample.

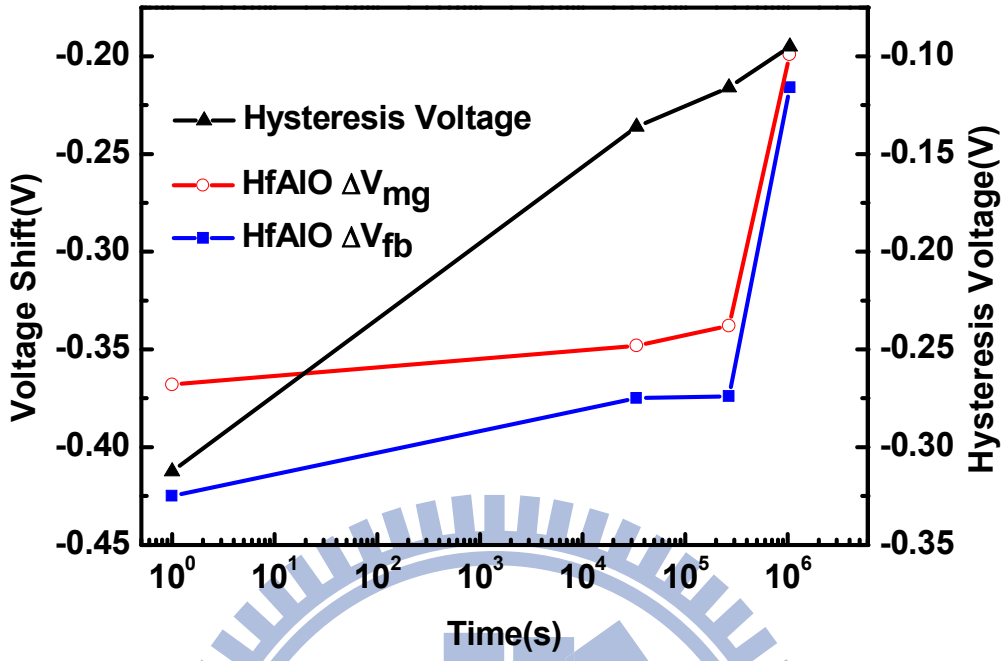


Fig. 3-25(a): Hysteresis voltage, ΔV_{fb} and ΔV_{mg} as a function of time of HfAlO sample.

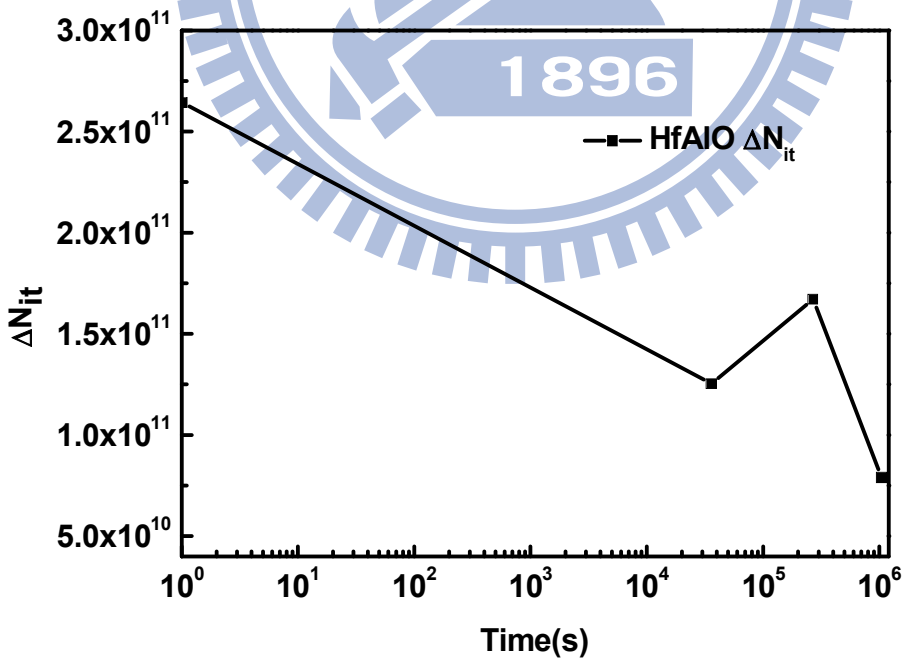


Fig. 3-25(b): The ΔN_{it} values as a function of time of HfALO sample.

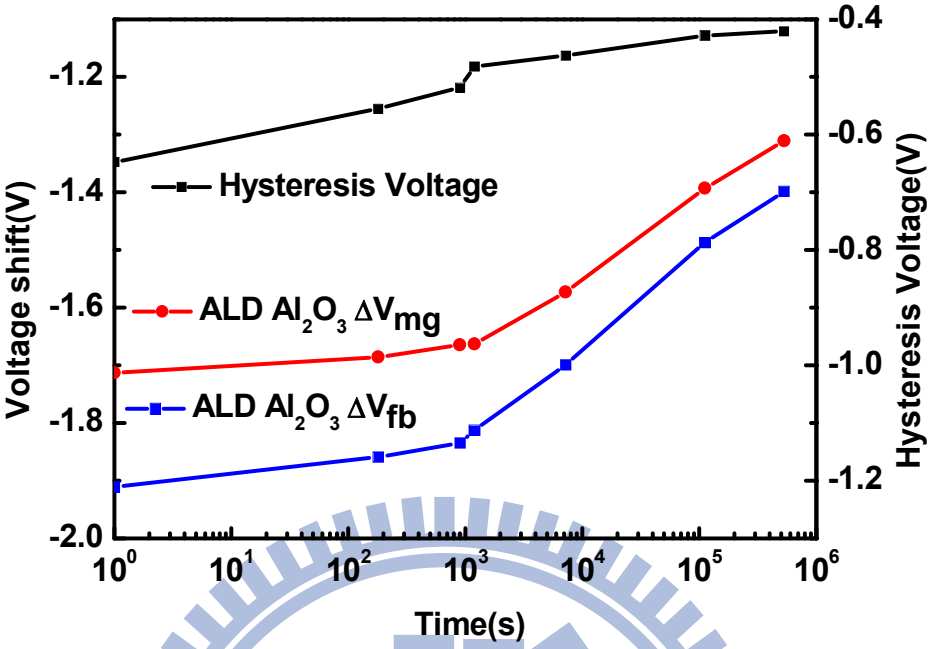


Fig. 3-26(a): Hysteresis voltage, ΔV_{fb} and ΔV_{mg} as a function of time of ALD Al_2O_3 sample.

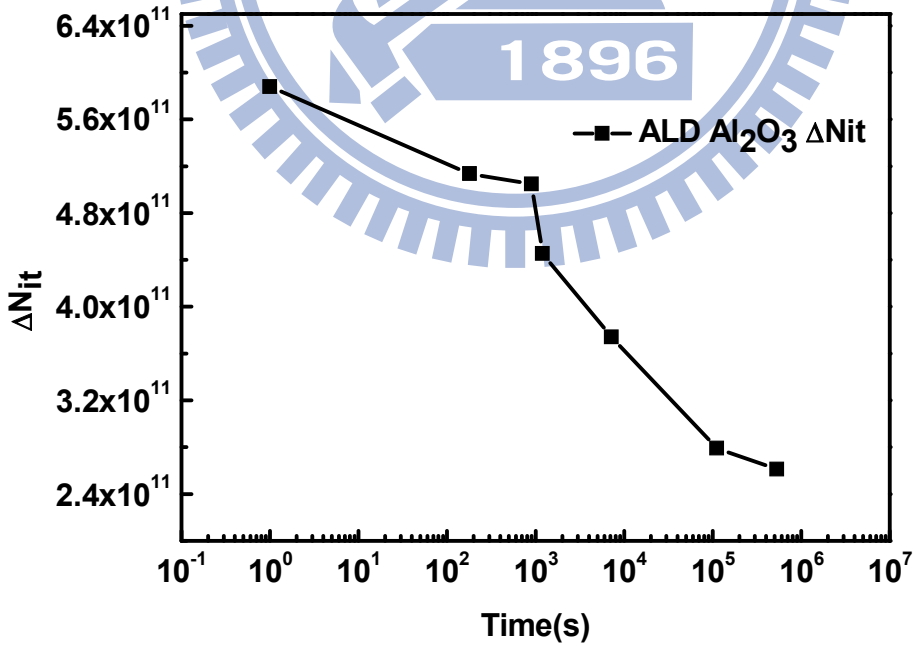


Fig. 3-26(b): The ΔN_{it} values as a function of time of ALD Al_2O_3 sample

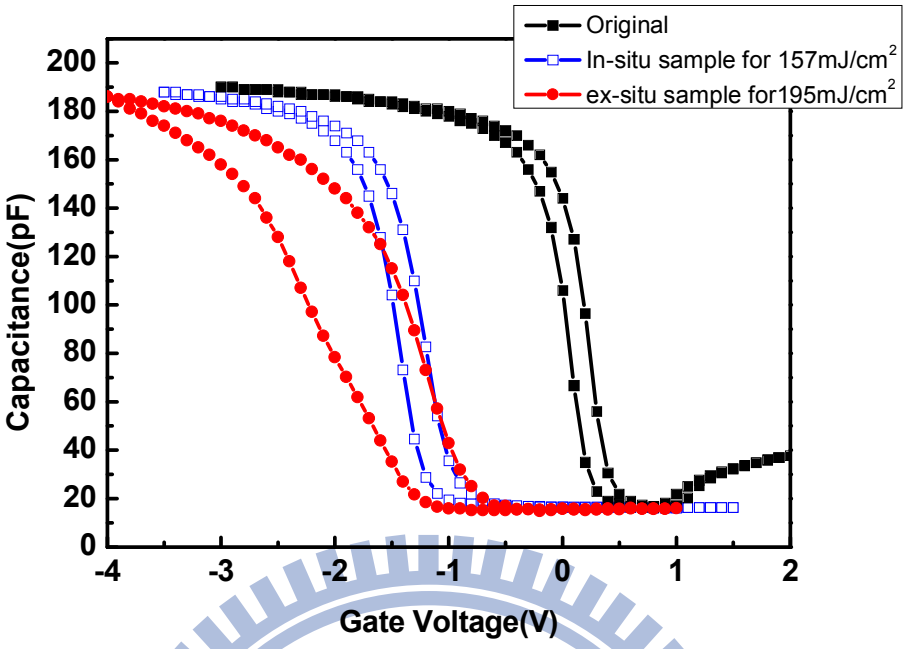


Fig. 3-27: Difference response of high-frequency C-V curve between in-situ and non ex-situ ALD Al_2O_3 samples under close EUV irradiation dosage.

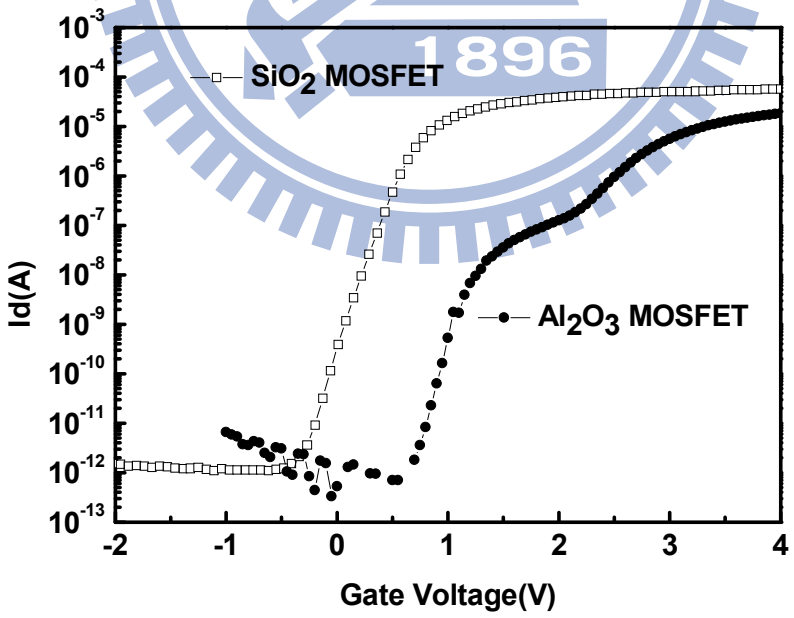


Fig. 3-28: Basic characteristic I_d-V_g curve of SiO_2 and Al_2O_3 MOSFET (V_d = 0.1V).

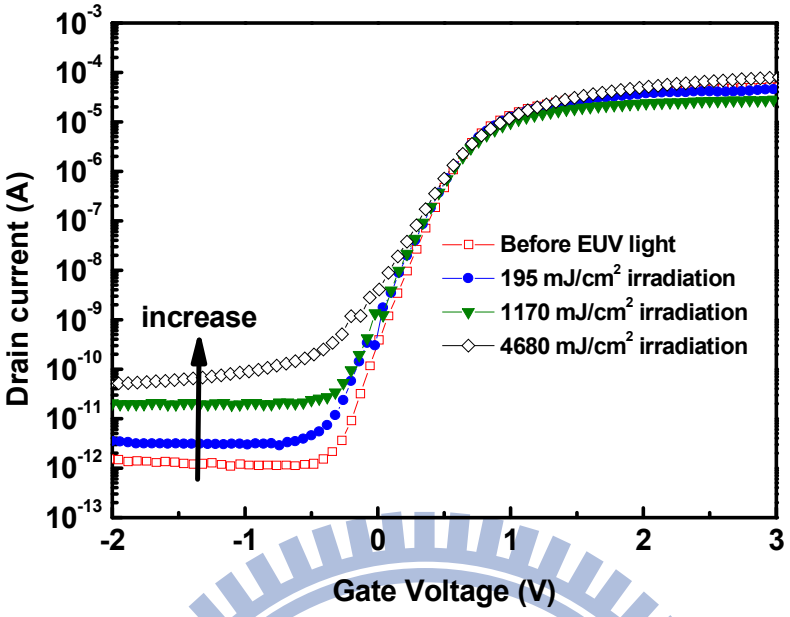
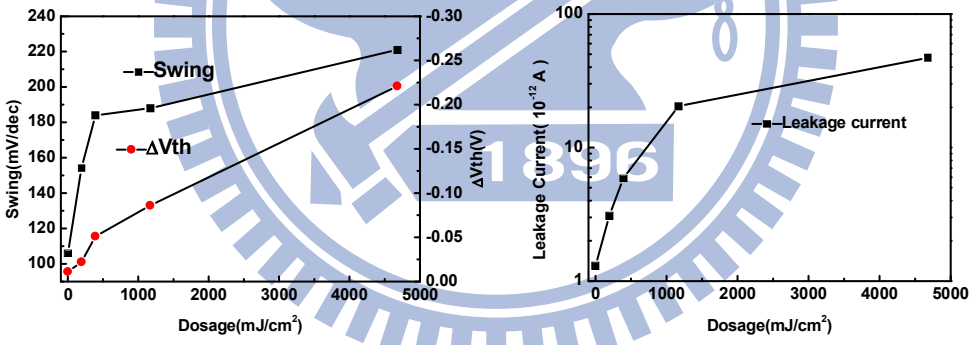


Fig. 3-29: I_d-V_g curve of SiO_2 MOSFETs with different EUV irradiation dosage from 195mJ/cm^2 to 4680mJ/cm^2 (V_d=0.1).



(a) (b)

Fig. 3-30: (a) Swing and V_{th} of SiO_2 MOSFETs as a function of EUV dosage. (b)Leakage current of SiO_2 as a function of dosage.

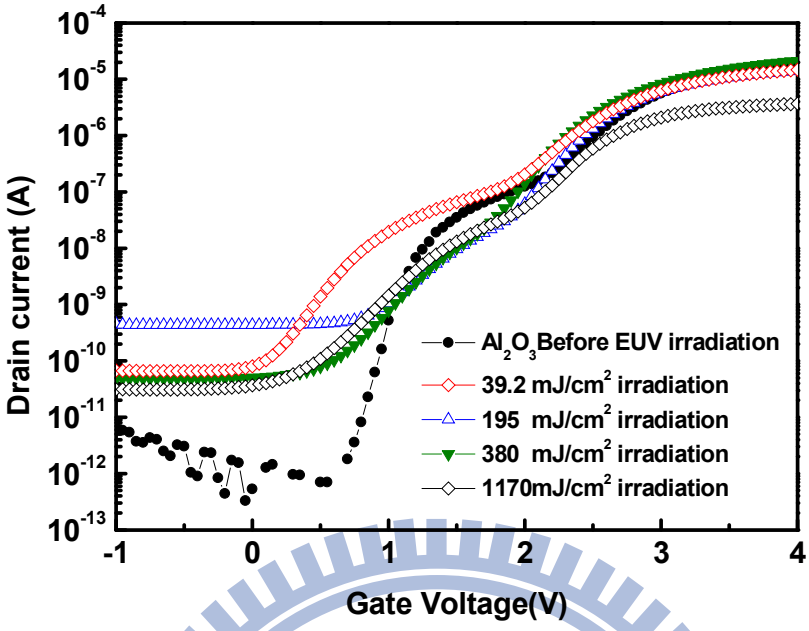


Fig. 3-31: I_d-V_g curve of Al_2O_3 MOSFETs with different EUV irradiation dosage from 39.2mJ/cm^2 to 1170mJ/cm^2 (V_d=0.1).

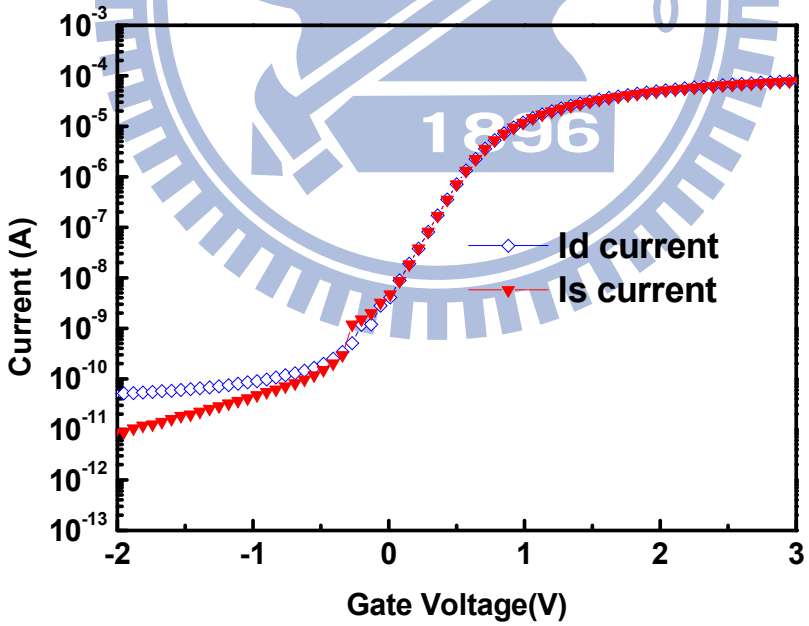


Fig. 3-32: I_d-V_g curve and I_s-V_g of SiO_2 MOSFETs.

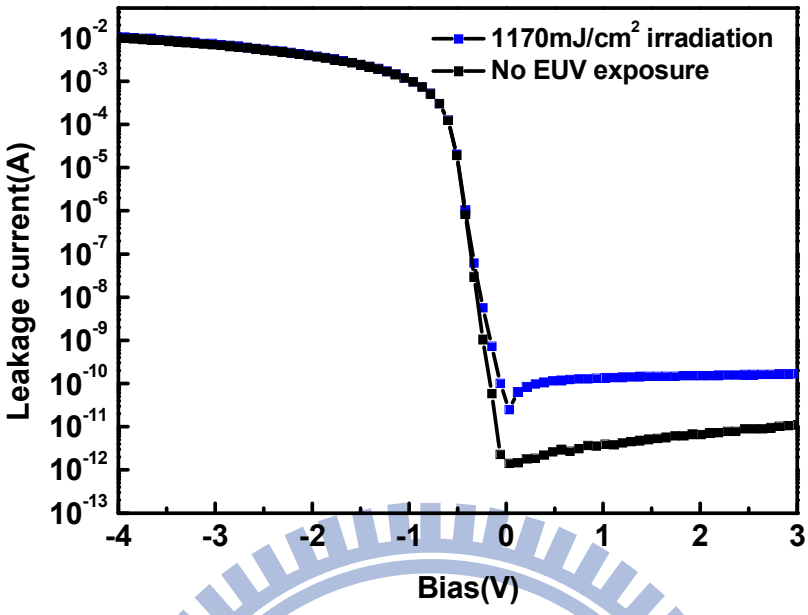


Fig. 3-33: Junction current before and after 1170mJ/cm^2 EUV irradiation.

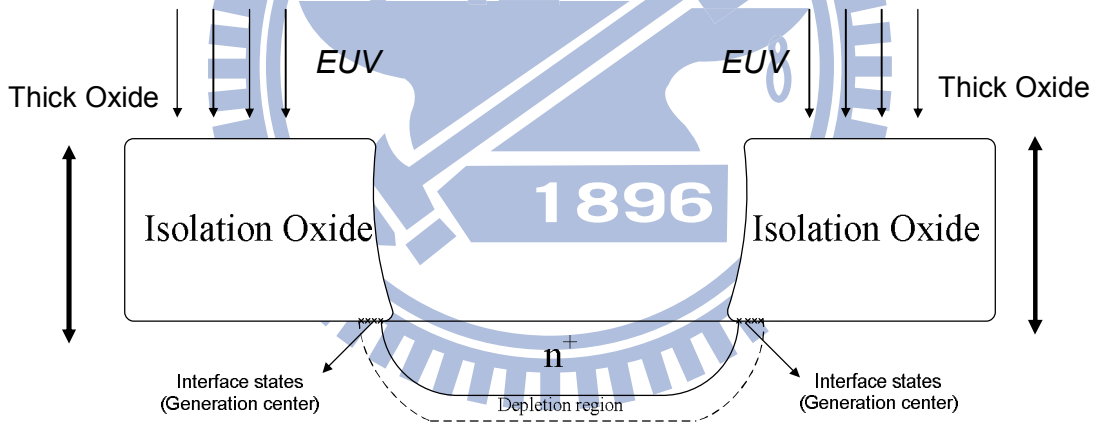


Fig. 3-34 The schematic cross-sectional structure of EUV irradiation damage between isolation oxide and depletion region where the interface states are as generation centers.

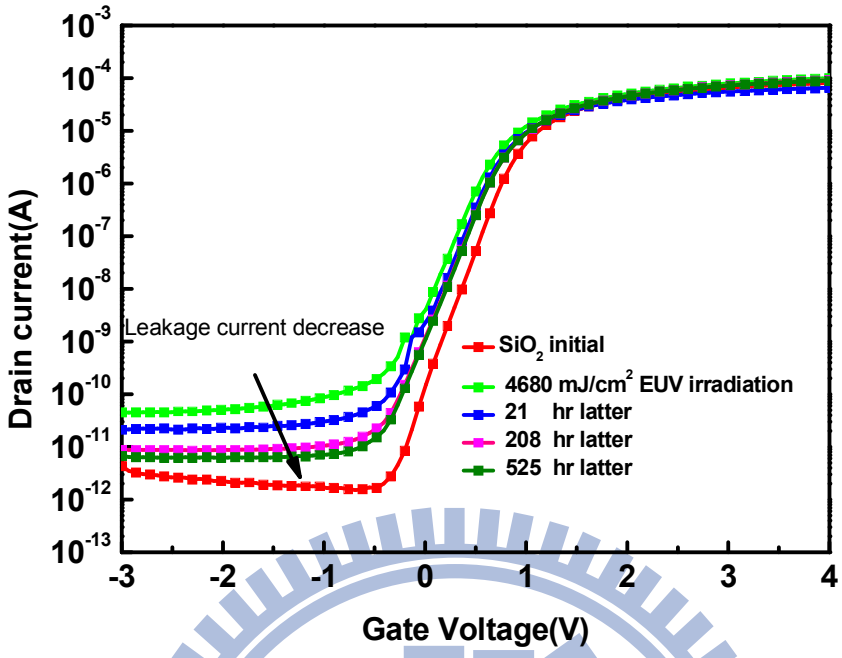


Fig. 3-35: I_d-V_g curve of SiO_2 MOSFETs with storage in room temperature from 21hr to 208hr after 4680mJ/cm^2 EUV irradiation.

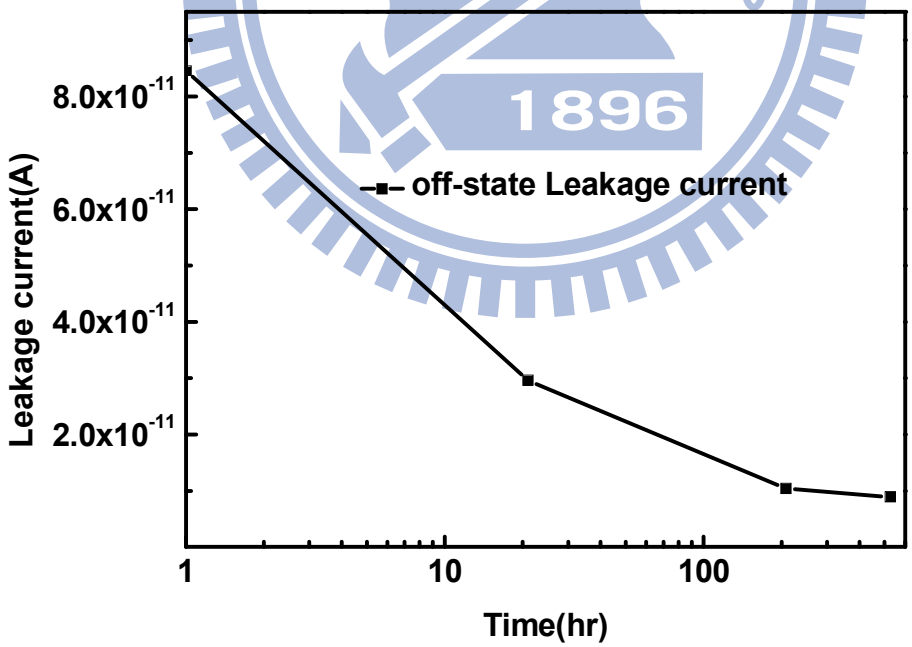


Fig. 3-36: The leakage current of SiO_2 as a function of time after 4680mJ/cm^2 EUV irradiation.

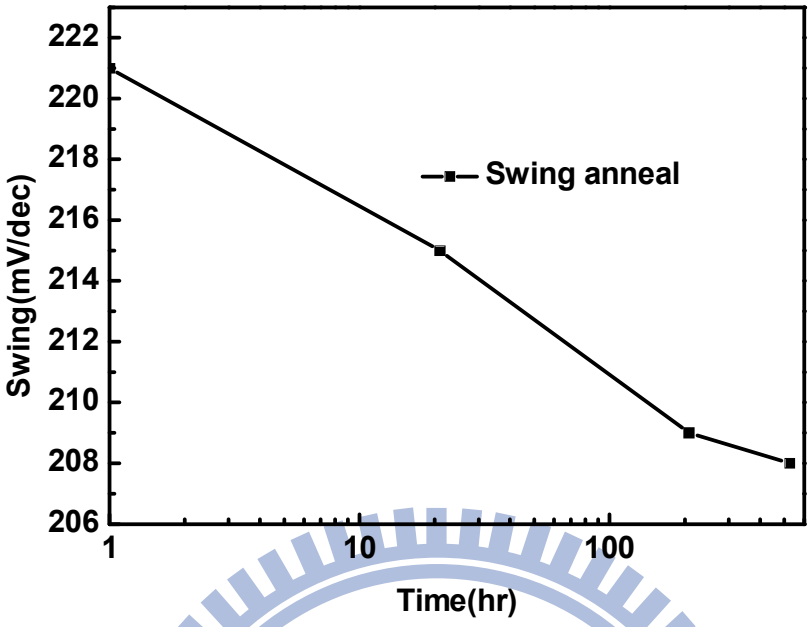


Fig. 3-37: The swing of SiO_2 MOSFET as a function of time after 4680mJ/cm^2 EUV irradiation.

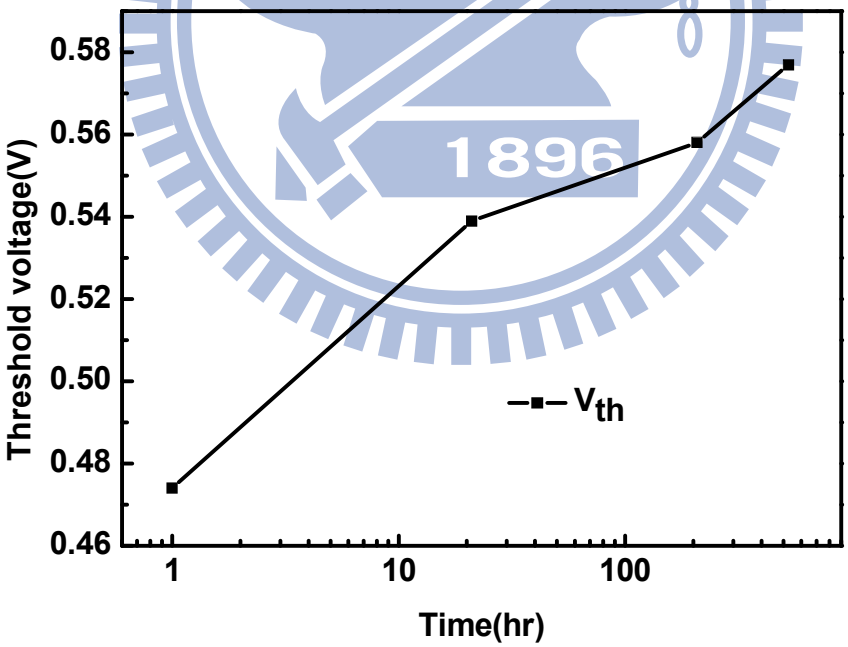


Fig. 3-38: The V_{th} of SiO_2 MOSFET as a function of time after 4680mJ/cm^2 EUV irradiation.

Chapter 4
Summary and Future Works

4-1 Summary

In this thesis we have demonstrated that the EUV have strong effect on the high-k/metal gate MIS capacitors and MOSFETs. EUV makes C-V curves of the MIS capacitors shift and distortion. These phenomena are due to hole-trapping in the oxide and the increase of interface states. Hysteresis phenomenon is also observed before and after EUV irradiation. But the hysteresis increases after EUV irradiation. It is believed that the border traps are increase by EUV irradiation. We have listed the results of all dielectrics affected by EUV in Table 3-2. The different gate dielectrics have different responses to the EUV irradiation. By continuous monitoring C-V and I-V curves after irradiation, the self-annealing behavior is observed. The type of interface states (donor-like or acceptor-like) and border traps (hole or electron) can be determined due to the different self-annealing behavior. For SiO_2 and HfSiO exhibit more donor-like interface states in the lower Si band gap. The Al_2O_3 also have donor-like interface states and more hole border traps after EUV irradiation. By contrast the HfAlO sample exhibit electron border traps after EUV irradiation. In the aspect of device fabrication we have shown the Al_2O_3 dielectric is the worst case in radiation hardness and SiO_2 shows the best radiation hardness in all materials.

The I_d-V_g curves show that after EUV irradiation the V_{th} of the MOSFETs with SiO_2 and Al_2O_3 as gate dielectric both shift negatively. The phenomenon consists with that observed on the MIS capacitors. Swing degradation is also an evidence of interface states increase by EUV irradiation. Off-state leakage current increases when

the irradiation dosage is increases. The reason which causes off-state leakage current can be identified by measuring the n^+-p junction characteristic. It is believed that EUV irradiation induces interface states at the field oxide/Si interface. The interface states are normally acts as generation and recombination centers. Therefore, the interface states around the S/D junction results in high generation current. The self-annealing on the MOSFETs is also investigated. Without any treatment, the device parameter of leakage current, sub-threshold swing and V_{th} can be partially recovered to a better level after long time storage at the room temperature.

4-2 Future Works

In order to predict the response of EUV irradiation damage in each material, the fundamental material characteristics should be fully understood. The total energy absorption, energy band gap, intrinsic trap density, radiation induce defect traps, charge capture cross-section, and interface states distribution before and after EUV irradiation, all of these factors can help us to predict the response to EUV irradiation.

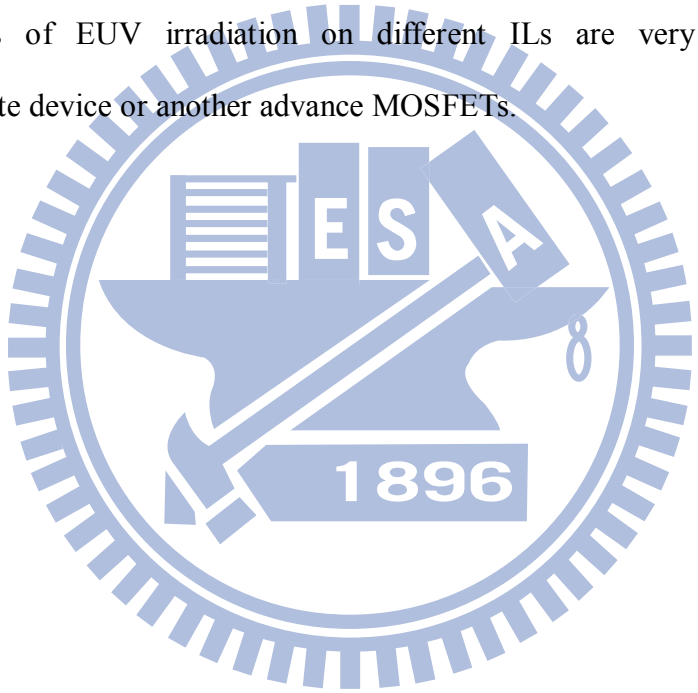
Radiation hardness is an important issue in the process. As the EUV is introduced into IC process, how to provide a good way to protect device from EUV damage is also an important issue. Capping a radiation hard film on the top, using different S/D structure, using different isolation structure may be helpful on radiation hardness. It has been reported that different gate thicknesses have different responses to the radiation. The test of EUV radiation on thinner gate dielectric thickness should be performed.

After irradiation, we have tested the effect of long time storage at room temperature. However, EUVL is used in the prior process steps which are gate pattern or the first layer metal interconnection. There are many processes after these crucial

steps. If the radiation damage can be delimited by 500 ^{o}C ~ 600 ^{o}C thermal treatment, we can use the temperatures in the latter process to eliminate the radiation damage. The radiation damage issue can be much more relieved. The annealing effect at low temperature within 600 ^{o}C should be researched.

Even the radiation damage can be annealed by some annealing step. However the device reliability is also need to be noticed after EUV irradiation. NBTI and PBTI tests should also be taken.

In this thesis we have noticed that IL plays an important role in radiation damage. The researches of EUV irradiation on different ILs are very important for high-k/metal gate device or another advance MOSFETs.



References

[1]. Lithography in international technology roadmap for semiconductor, pp.11-12, 2009

[2]. M. D. Austin, H. Ge, W. Wu, M. Li, Z. Yu, D. Wasserman, S. A. Lyon, and S. Y. Choub "Fabrication of 5 nm linewidth and 14 nm pitch features," *Appl. Phys. Lett.*, Vol.84 pp.5299 – 5301, 2004.

[3]. O. Wooda, C. S. Koayb, K. Petrillob, H. Mizunoc, S. Raghunathana, J. Arnoldb, D. Horakb, M. Burkhardtd, G. Mcintyreb, Y. Denge, B. L. Fontainee, U. Okoroanyanwua, A. Tchikoulaevaf, T. Wallowe, J. H. C. Chenb, M.Colburnb, S. S.C. Fanb, B. S. Haranb, and Y. Yinb "Integration of EUV lithography in the fabrication of 22-nm node devices by nanoimprint lithography" Proc. SPIE, Vol. **7271**, pp. 727104-1-727104-9, 2009

[4]. A. G. Revesz "Defect structure and irradiation behavior of noncrystalline SiO_2 vitreous silica and silicon-silicon dioxide interface defect structure and behavior during ionizing or particle irradiation," *IEEE Transactions on Nuclear Science.*, Vol.18, pp. 113-116, 1971

[5]. C. M. Svensson, ''The Defect Structure of the Si-SiO_2 interface, a model based on trivalent silicon and its hydrogen 'compounds'," *The physics of SiO_2 and Its Interface*, pp. 328-332, 1978

[6]. S. K. Lai "Interface trap generation in silicon dioxide when electrons are captured by trapped holes," *J. Appl. Phys.* ,Vol. 54, pp. 2540-2546,1983

[7]. S. N. Rashkeev, C. R. Cirba, D. M. Fleetwood, R. D. Schrimpf, S.C. Witczak, A. Michez, and S. T. Pantelides "Physical model for enhanced interface-trap formation at low dose rates," *IEEE Transactions on Nuclear Science* Vol. 49, pp. 2650 – 2655, 2002

[8]. S. K Lai, "Two-carrier nature of interface-state generation in hole trapping and radiation damage" *Appl. Phys. Lett.* Vol. 39 pp. 58-61, 1981

[9]. F. J. Grunthaner, P. J. Grunthaner, R. P. Vasquez, B. F. Lewis, and J. Maserjian "High-resolution X-Ray photoelectron spectroscopy as a probe of local atomic

Structure: application to amorphous SiO_2 and the Si-SiO_2 Interface," *Phys. Rev. Lett.*, Vol. 43, pp. 1683–1686, 1979

[10]. S. Ogawa, M. Shimaya, and N. Shiono "Interface-trap generation at ultrathin Si02 (4-6 nm)-Si interfaces during negative-bias temperature aging" *Journal of Applied Physics*, vol. 77, no. 3, p.p 1137-1148, 1995

[11]. E. Atanassova, A. Paskaleva and N. Novkovski "Effects of radiation and charge trapping on the reliability of high-k gate dielectrics," *Microelectronics Reliability* ,Vol. 48, pp. 514-525, 2008

[12]. E. P. Gusev, C. D'Emic, S. Zafar and A. Kumar, "Charge trapping and detrapping in HfO_2 high-k gate stacks," *Microelectronic Engineering* Vol.72, Pages 273-277, 2004

[13]. S. Zafar, A. Callegari, V. Narayanan, S. Guha, "Impact of moisture on charge trapping and flatband voltage in Al_2O_3 gate dielectric films". *Appl. Phys. Lett*, Vol. 81, pp.2608– 2617, 2002

[14]. S. Zafar, A. Callegari, E. Gusev and M. Fischetti, "Charge trapping in high-k gate dielectric stacks," in *IEDM Tech. Dig*, 2002, pp. 517-520

[15]. T. P. Ma and P. V. Dressendorfer "Ionizing radiation effects in MOS Devices and Circuits," Wiley, New York, 1989

[16]. K. Neumeier H. P. Bruemmer, "Radiation hard LOCOS field oxide," *IEEE Transactions on Nuclear Science* Vol. 41, pp.572-576, 1994

[17]. G. Anelli, M.Campbell, M. Delmastro, F. Faccio, S. Floria,; A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical Design Aspects,", *IEEE Transactions on Nuclear Science*, Vol. 46, pp.1690-1696, 1999

[18]. F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors (0.13 um)," *IEEE Transactions on Nuclear Science*, Vol.52, pp.2413-2420, 2005

[19]. S. Nakayama and T. Sakai, “The effect of nitrogen in p^+ polysilicon gates on boron penetration in to silicon substrate through the gate oxide” in *VLSI Symp. Tech. Dig.*, 1996, pp.228-229

[20]. N.D. Arora, E. Rios and C.L. Huang “Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance,” *IEEE Transactions on Electron Devices*, Vol.42, pp. 935-943,1995

[21]. Process Integration, Devices and Structures in International Technology Roadmap for Semiconductor, pp.11-14, 2001

[22]. E. Josse and T. Skotnicki, “Polysilicon gate with depletion-or-metallic gate with buried channel: what evil worse ?” in *IEEE IEDM Tech. Dig.*, 1999, pp. 661–664

[23]. S. K Lai **“**Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology” *J. Appl. Phys.* Vol. **54**, pp. 2540-2546, 1983

[24]. M. Fischetti, D. A. Neumayer, and E. A. Cartier, “Effective electron mobility in Si inversion layers in metal–oxide-semiconductor systems with a high-k insulator: the role of remote phonon scattering,” *J. Appl. Phys.*, Vol. 90, pp. 4587, 2001.

[25]. S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick and R. Chau., “High mobility Si/SiGe strained channel MOS transistors with HfO_2/TiN gate stack,” in *IEDM Tech. Dig.*, 2003, pp. 653–656.

[26]. H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata, and H. Iwai, ”Study of the manufacturing feasibility of 1.5-nm direct-tunneling gate oxide MOSFET’s: uniformity, reliability, and dopant penetration of the gate oxide,” *IEEE Transactions on Electron Devices* Vol. 45, pp. 691-700, 1998

[27]. D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt and G. Timp “The electronic structure at the atomic scale of ultrathin gate oxides” *NATURE*, Vol. 399, pp. 758-761 ,1999

[28]. International technology roadmap for semiconductors 2007 edition ,process integration, device, and structures.

[29]. J.H. Stathis and D.J. DiMaria "Reliability projection for ultra-thin oxides at low voltage" in *IEDM Tech. Dig*, 1998 pp. 167-170

[30]. C. Chaneliere, J.L. Autran, R.A.B. Devine and B. Balland "Tantalum pentoxide (Ta_2O_5) thin films for advanced dielectric applications" *Materials Science & Engineering* Vol.22, p.269-322, 1998

[31]. A. Chatterjee, R.A. Chapman, K. Joyner, M. Otobe , S. Hattangady, M. Bevan, G.A. Brown, H. Yang, Q. He, D. Rogers, S.J. Fang, R. Kraft, A.L.P. Rotondaro, M. Terry, K. Brennan, S.-W. Aur, J.C. Hu, H. L. Tsai, P. Jones, G. Wilk, M. Aoki, M. Rodder, and I. C. Chen "CMOS Metal replacement gate transistors using tantalum pentoxide gate insulator" in *IEDM Tech. Dig*, 1998 , pp.777-780

[32]. R. A. McKee, F. J. Walker, and M. F. Chisholm "Crystalline oxides on silicon: The first five monolayers" *Phys. Rev. Lett.* Vol.81, pp.3014–3017, 1998

[33]. M. Kawasaki, K. Takahashi, T. Maeda, R. Tsuchiya, M. Shinohara, O. Ishiyama, T. Yonezawa, M. Yoshimoto, and H. Koinuma "Atomic control of the $SrTiO_3$ crystal surface" *Science* Vol. 266., pp. 1540-1542,1994

[34]. K. Eisenberg, J. M. Finder, Z. Yu, J. Ramdani, J. A. Curless, J. A. Hallmark, R. Droopad, W. J. Ooms, L. Salem, S. Bradshaw, and C. D. Overgaard, "Field effect transistors with $SrTiO_3$ gate dielectric on Si", *Appl. Phys. Lett.*,Vol.76, 1324-1329, 2000

[35]. T. M. Klein, D. Niu, W. S. Epling, W. Li, D. M. Maher, C. C. Hobbs, R. I. Hegde, I. J. R. Baumvol, and G. N. Parsons "Evidence of aluminum silicate formation during chemical vapor deposition of amorphous Al_2O_3 thin films on Si(100)" *Appl. Phys. Lett*. Vol. **75**, pp.4001-4003, 1999

[36]. L. Manchanda, W. H. Lee, J. E. Bower, F. H. Baumann, W. L. BroIwn, C. J. Case, R. C. Keller, Y. O. Kim, E. J. Laskowski, M. D. Morris, R. L. Opila, P. J. Silverman, T. W. Sorsch and G. R. Weber. "Gate quality doped high-k films for CMOS beyond 100 nm: 3 - l0nm Al_2O_3 with low leakage and low interface states" in *IEDM Tech. Dig* .1998 , pp. 605-608

[37]. G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, R. S. Urdahl, "Intermixing at the tantalum oxide/silicon interface in gate dielectric structures," *Appl. Phys. Lett.*, Vol.73, pp. 1517-1519, 1998

[38]. T. M. Klein, D. Niu, W. S. Epling, W. Li, D. M. Maher, C. C. Hobbs, R. I. Hegde, I. J. R. Baumvol, G. N. Parsons, "Evidence of aluminum silicate formation during chemical vapor deposition of amorphous Al_2O_3 thin films on Si.100," *Appl. Phys. Lett.*, Vol.75 , pp.4001-4003, 1999

[39]. E.P. Gusev, E. Cartier, D.A. Buchanan, M. Gribelyuk, M. Copel,H. Okorn-Schmidt and C. D Emic "Ultra thin high-k metal oxides on silicon: processing, characterization and integration issue," *Microelectronic Engineering* Vol.59, pp. 341-349, 2001

[40]. S. A. Campbell, D. C. Gilmer, X. C. Wang, M. T. Hsieh, H. S. Kim, W. L. Gladfelter and J. Yan, "MOSFET transistors fabricated with high permitivity TiO_2 dielectrics," *Electron Devices, IEEE Transactions on*, Vol.44, pp. 104-109, 1997

[41]. S. A. Campbell, H. S. Kim, D. C. Gilmer, B. He,T. Ma and W. L. Gladfelter "Titanium dioxide (TiO_2) based gate insulators," *IBM Journal of Research and Development*, Vol.43, pp.383-392, 1999

[42]. J. P. Chang, Y. S. Lin, S. Berger, A. Kepten, R. Bloom and S. Levy, "Ultrathin zirconium oxide films as alternative gate dielectrics," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* , Vol.19, pp.2137-2143, 2001

[43]. M. Copel, M. Gribelyuk and E. Gusev, "Structure and stability of ultrathin zirconium oxide layers on Si(001)," *Applied Physics Letters* , Vol.76, pp.436-438, 2000

[44]. M. Copel, M. Gribelyuk and E. Gusev, "Structure and stability of ultrathin zirconium oxide layers on Si(001)," *Applied Physics Letters* , Vol.76, pp.436-438, 2000

[45]. B. H. Lee, L. Kang, R. Nieh, W. J. Qi and J. C. Lee, "Thermal stability and

electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters* , Vol.76, no.14, pp.1926-1928, Apr 2000

[46]. G. D. Wilk, R. M. Wallace, J. M. Anthony,"High-κ gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics* , Vol.89, pp.5243-5275,2001

[47]. R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar and M. Radosavljevic, "Application of high-k gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Microelectronic Engineering*, Vol. 80, pp.1-6, 2005

[48]. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mclntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams and K. Zawadzki "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," in *IEDM Tech. Dig*, 2007, pp.247-250

[49]. W. Kesternich,; , "Search for radiation-induced electrical degradation in ion irradiated sapphire and polycrystalline Al_2O_3," *Journal of Applied Physics* , Vol.85, no.2, pp.748-752, Jan 1999

[50]. B. D. Evans, "A review of the optical properties of anion lattice vacancies, and electrical conduction in [alpha]-Al_2O_3: their relation to radiation-induced electrical degradation," Journal of Nuclear Materials, Volume 219, Fabrication and Properties of Ceramics for Fusion Energy, 1995, pp. 202-223

[51]. Chen, D.K., Mamouni, F.E. Zhou, X.J. Schrimpf R.D. Fleetwood, D.M. Galloway, K.F. Lee, S. Seo, H. Lucovsky, G. Jun, B. Cressler, J.D. "Total Dose and Bias Temperature Stress Effects for HfSiON on Si MOS Capacitors,"*IEEE*

Transactions on Nuclear Science, Vol.54, no.6, pp.1931-1937, Dec. 2007

[52]. V. Banine, O. Frijns, G. Swinkels "Requirements and prospects of next generation Extreme Ultraviolet Sources for Lithography Applications (LPP and DPP), 2007 International EUVL Symposium, Sapporo, Japan

[53]. L.M. Terman "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes, "Solid-State Electronics, Volume 5, Issue 5, 1962, pp. 285-299,

[54]. *"Semiconductor Devices: Physics and Technology"*, S. M. Sze. New York: Wiley, 1985; 2nd ed., 2001

簡歷

姓　　名:李勃學

性　　別:男

出生年月日:民國七十四年十月九日

住　　址:台中縣外埔鄉水美村二崁路 57 號

學　　歷:

國立台中第一高級中學 (90.9~93.6)

國立交通大學電子工程學系(93.9~97.6)

國立交通大學電子研究所碩士班(97.9~99.7)

碩 士 論 文:

極紫外光對於高介電常數薄膜之影響與其特性之研究

Effect of Extreme Ultra-Violet Radiation on High Dielectric Constant Dielectrics