802.11a/g 正交分頻多工外部接收器之設計與實現

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摘要

本論文提出用於 IEEE 802.11a/g 正交分頻多工基頻外部接收器的設計與實現。所提出的外部接收器架構中，共包含了四個主要的模組分別為 Demapping，Deinterleaver，Depuncture 和 Viterbi Decoder，而 Viterbi Decoder 為外部接收器的主要模組。根據 IEEE 802.11a 規格，迴旋碼 1/2 為基本的編碼格式，加上了 Puncture 模組可以增加不同的資料傳輸速率，也因此 Viterbi Decoder 的架構也必須配合不同的資料傳輸速率而有所更改。此篇論文也探討了高精度(Soft-Decision)解析度與 Viterbi decoder 的追溯長度(Traceback-length)對於外部接收器效能的影響與複雜度的最佳化。本論文所完成之電路由 0.18 um CMOS 製程所製造，其最高操作頻率為 25MHz，最大資料速率為 67.5Mbps，而在 1.8V 狀況下的功率消耗為 78.85mW。

Design and Implementation of 802.11a/g OFDM-Based Outer Receiver

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Abstract

In this thesis, an IEEE 802.11a/g OFDM-based outer receiver design and implementation is presented. This proposed outer receiver consists of four modules. They are “Demapping”, “Deinterleaver”, “Depuncture”, and “Decoder” (Viterbi decoder), respectively. Viterbi Decoder is the main function module. According to IEEE 802.11a/g, the convolutional code 1/2 is the base coding rate. Through adopting the puncture scheme, the 802.11a/g transceiver owns several data rates. Therefore, Viterbi decoder of outer receiver needs to be modified with its structure. We also discuss the soft decision resolution and traceback-length to get the optimized solution between performance and complexity. The chip is fabricated in 0.18 um CMOS process, and the maximum throughput rate can achieve 67Mbps under clock rate 25MHz. The power consumption is below 78.83mW under 1.8V.