Chapter 1

Introduction

1.1 Introduction to Outer Receiver

Since the first wireless local area network (WLAN) product appears, people seem to be interested in “wireless” especially. Behind the convenience of the wireless communication for daily life, we should overcome many technique problems which the “wireless” brings us, i.e. the unpredictable channel. For increasing the resistance of channel noise, we usually use channel coding methodology in transmitter. For example, the IEEE 802.11a/g [1] [2] employs convolutional code in transmitter. Figure 1 depicts the IEEE 802.11a/g OFDM-based baseband system architecture. For general definition, the outer receiver includes modules as demapping, deinterleaver, depuncture, decoder, and descrambler in baseband physical layer. Actually, the decoder module is known as Viterbi decoder which is the efficient method for the realization of maximum likelihood decoding of convolutional codes [3] [4].

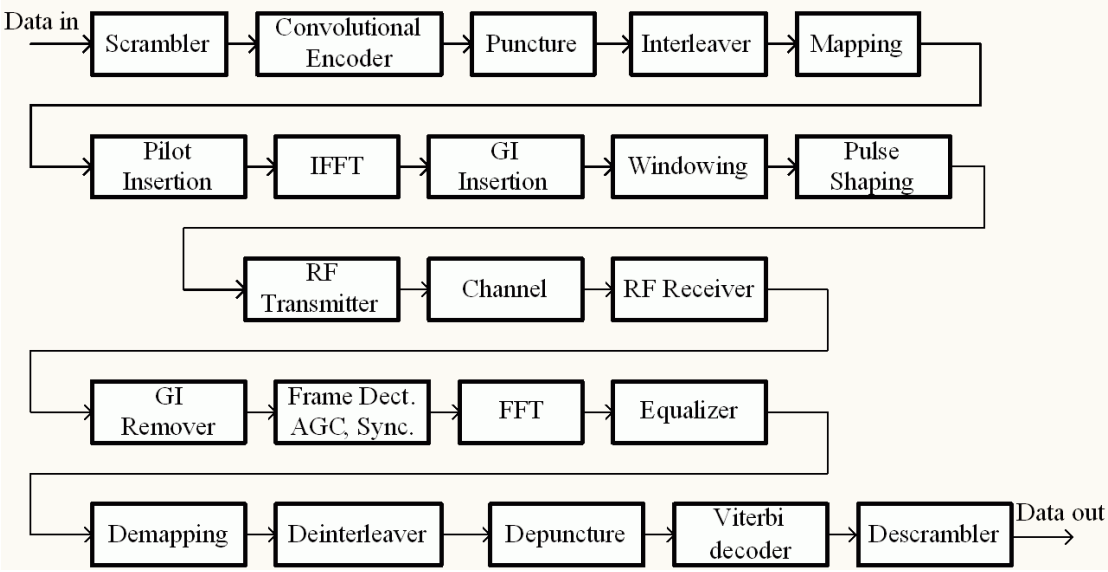

Figure 1: IEEE 802.11a baseband system

People never stop chasing high speed while they enjoy the internet. Therefore, IEEE 802.11 group and ETSI BRAN (European Telecommunication Standards Institute Broad Radio Access Network) developed 802.11a/b/g which own high speed data rate. For high data rate transmission applications, high QAM (Quadrature Amplitude Modulation) technology has been proposed to achieve this goal. But the system which applies high QAM technology requests higher SNR to keep the same BER compared with BPSK or QPSK. Therefore, we need more hardware cost to compensate high QAM performance loss. This is the trade off between performance and hardware complexity.

1.2 Design and Implementation Issues

It is straightforward that IEEE 802.11a timing-related parameters have restricted the Viterbi decoder for optimal architecture. Table 1 shows Timing-related parameters. For the duration of the SIGNAL BPSK-OFDM symbol 4us, we demand 80 clock periods to handle one OFDM symbol data for system clock rate 20MHz. Therefore, Viterbi decoder architecture needs to be modified.

Since the IEEE 802.11a/g is the application of high QAM technology, we have two methods to improve the coding gain. One is that the use of soft decision algorithm, and another is about the traceback length of Viterbi decoder. No matter what using soft decision algorithm or changing the traceback length, they encounter all the same issues: the trade off between performance and hardware complexity.

Table 1: Timing-related parameters

Parameter	Value
N_{SD}: Number of data subcarriers	48
N_{SP}: Number of pilot subcarriers	4
N_{ST}: Number of subcarriers, total	52 ($N_{SD} + N_{SP}$)
Δ_F: Subcarrier frequency spacing	0.3125 MHz (=20 MHz/64)
T_{FFT}: IFFT/FFT period	3.2 μs ($1/\Delta_F$)
$T_{PREAMBLE}$: PLCP preamble duration	16 μs ($T_{SHORT} + T_{LONG}$)
T_{SIGNAL}: Duration of the SIGNAL BPSK-OFDM symbol	4.0 μs ($T_{GI} + T_{FFT}$)
T_{GI}: GI duration	0.8 μs ($T_{FFT}/4$)
T_{GI2}: Training symbol GI duration	1.6 μs ($T_{FFT}/2$)
T_{SYM}: Symbol interval	4 μs ($T_{GI} + T_{FFT}$)
T_{SHORT}: Short training sequence duration	8 μs ($10 \times T_{FFT}/4$)
T_{LONG}: Long training sequence duration	8 μs ($T_{GI2} + 2 \times T_{FFT}$)

1.3 Organization of Thesis

This thesis is organized as follows: The first chapter describes a briefly introduction of the outer receiver. In chapter 2, the specification of IEEE 802.11a/g relative to the outer receiver and the system requirements will be presented. Chapter 3 describes the design of the outer receiver, including demapping, deinterleaver, depuncture, and Viterbi decoder, respectively. And it also shows the simulation result. In chapter 4, the ASIC implementation issues, and the result of the implementation are shown. Chapter 5 shows the integration and evaluation in system-level by Agilent ADS platform. Finally, a brief conclusion and future work are presented in chapter 6.