Chapter 2

Architecture of Outer Receiver

2.1 IEEE 802.11a/g Standard relative to Outer Receiver

The IEEE 802.11g WLAN standard operational modes are included as mandatory mode and two optional modes. The mandatory mode is ERP (Extended Rate PHY) /OFDM, one of optional modes is PBCC, and other is CCK-OFDM mode. Because the IEEE 802.11g OFDM modes shall follow IEEE 802.11a exactly, we only describe IEEE 802.11a standard about outer receiver briefly [1] [2].

2.1.1 Scrambler

The frame synchronous scrambler uses the generator polynomial S(x) as follows, and is illustrated in Figure 2:

$$S(x) = x^7 + x^4 + 1 \tag{2.1}$$

In the outer receiver, we can use the same scrambler structure to descramble the received data.

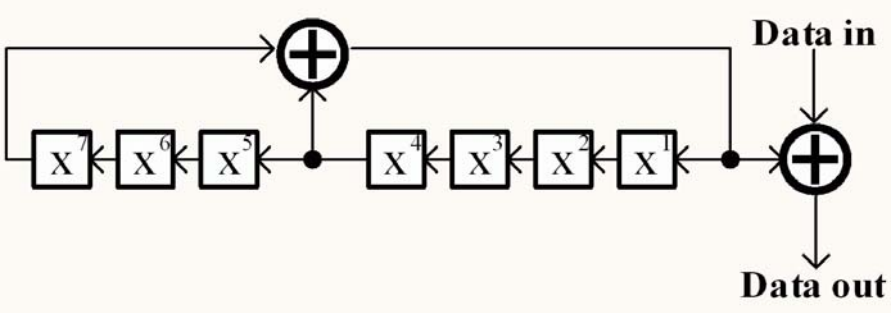


Figure 2: Scrambler

2.1.2 Convolutional encoder

The convolutional encoder of transmitter provide coding rate r=1/2, and its generator polynomial can be derive from Figure 3. Other rates are derived from it by employing “puncturing” methodology. Puncturing is a procedure for omitting some of the encoded bits in the transmitter and inserting a dummy “zero” metric into the convolutional decoder on the receive side.

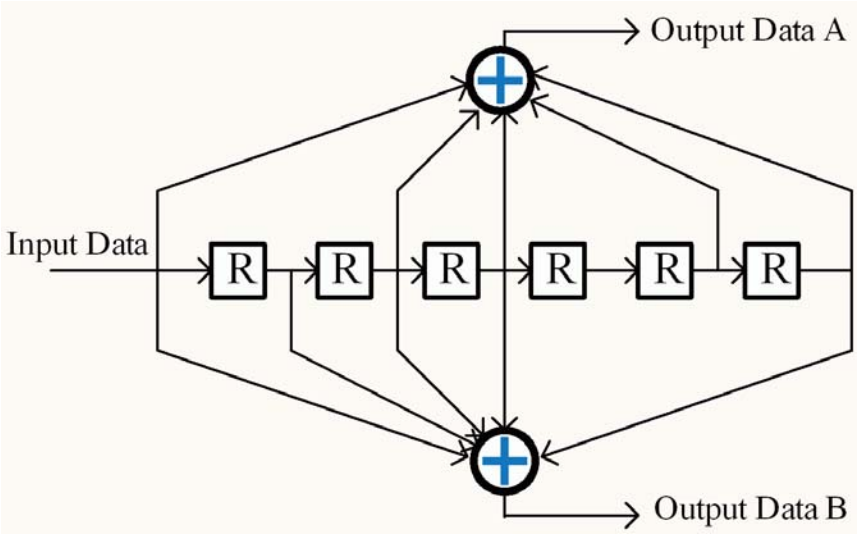


Figure 3: (2, 1, 7) convolutional encoder

2.1.3 Interleaving

All encoded data bits shall be interleaved by a block interleaver with a block size corresponding to the number of bits in a single OFDM symbol, NCBPS. The interleaver is defined by a two-step permutation. The first permutation ensures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second ensures that adjacent coded bits are mapped alternately onto less and more significant bits of the constellation and, thereby, long runs of low reliability (LSB) bits are avoided. We shall denote by *k* the index of the coded bit before the first permutation; *i* shall be the index after the first and before the second permutation, and *j* shall be the index after the second permutation, just prior to modulation mapping.

The first permutation is defined by the rule

$$i = (N_{CBPS}/16)(k \bmod 16) + floor(k/16), k = 0,1,..., N_{CBPS} - 1 \quad (2.2)$$

The function floor (.) denotes the largest integer not exceeding the parameter.

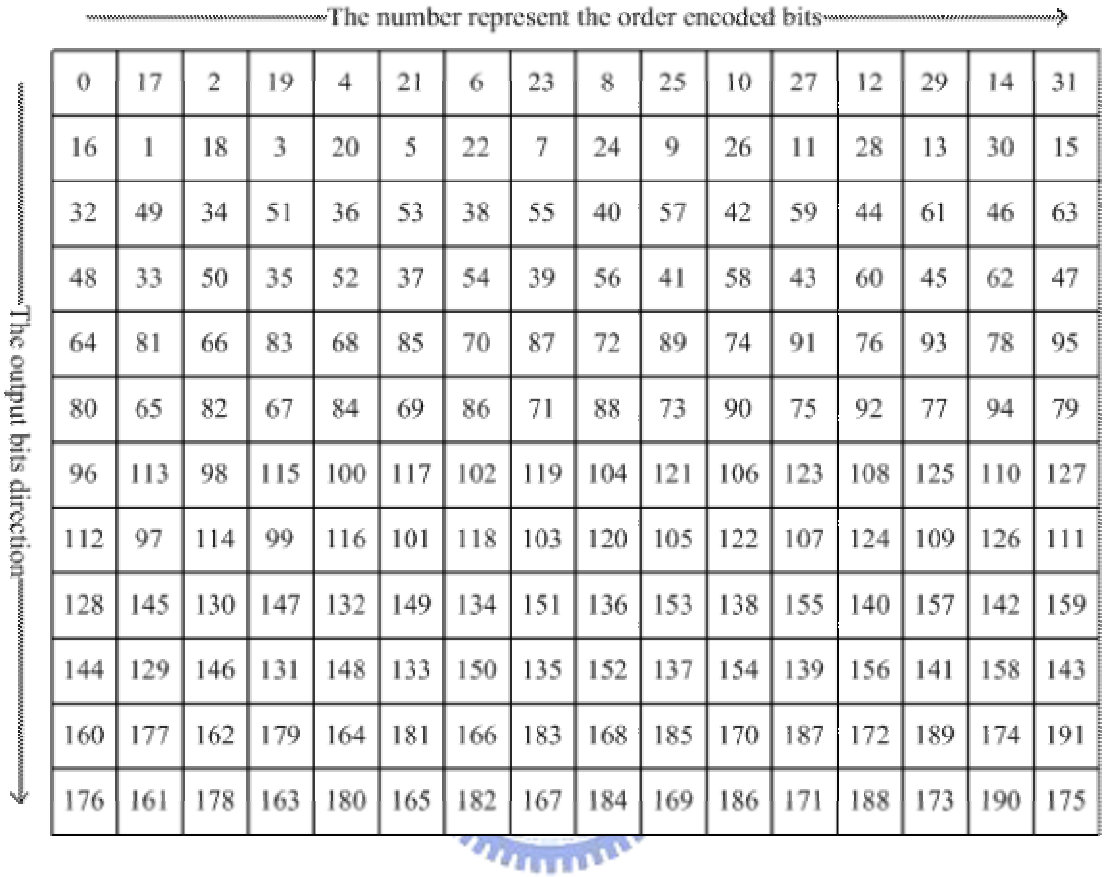
The second permutation is defined by the rule.

$$j = s \times floor(i/s) + (i + N_{CBPS} - floor(16 \times i / N_{CBPS})) \bmod s, i = 0,1,..., N_{CBPS} - 1 \quad (2.3)$$

The value of s is determined by the number of coded bits per subcarrier, NBPSC, according to

$$s = \max(N_{BPSC}/2,1) \quad (2.4)$$

The deinterleaver, which is the inverse operation of interleaver, is also defined by two permutations. In Figure 4, we take 16QAM case as an example.



0	17	2	19	4	21	6	23	8	25	10	27	12	29	14	31
16	1	18	3	20	5	22	7	24	9	26	11	28	13	30	15
32	49	34	51	36	53	38	55	40	57	42	59	44	61	46	63
48	33	50	35	52	37	54	39	56	41	58	43	60	45	62	47
64	81	66	83	68	85	70	87	72	89	74	91	76	93	78	95
80	65	82	67	84	69	86	71	88	73	90	75	92	77	94	79
96	113	98	115	100	117	102	119	104	121	106	123	108	125	110	127
112	97	114	99	116	101	118	103	120	105	122	107	124	109	126	111
128	145	130	147	132	149	134	151	136	153	138	155	140	157	142	159
144	129	146	131	148	133	150	135	152	137	154	139	156	141	158	143
160	177	162	179	164	181	166	183	168	185	170	187	172	189	174	191
176	161	178	163	180	165	182	167	184	169	186	171	188	173	190	175

Figure 4: 16-QAM interleaving

2.1.4 Puncture

According to the original Convolutional coding rate r=1/2, we can derive other coding rate by applying puncturing procedure. By employing coding rate r=1/2, 3/4, and 2/3, IEEE 802.11a supports eight different data rate. By stealing the encoded data, the coding rate varies with the puncture scheme. Figure 5 depicts the puncture procedure.

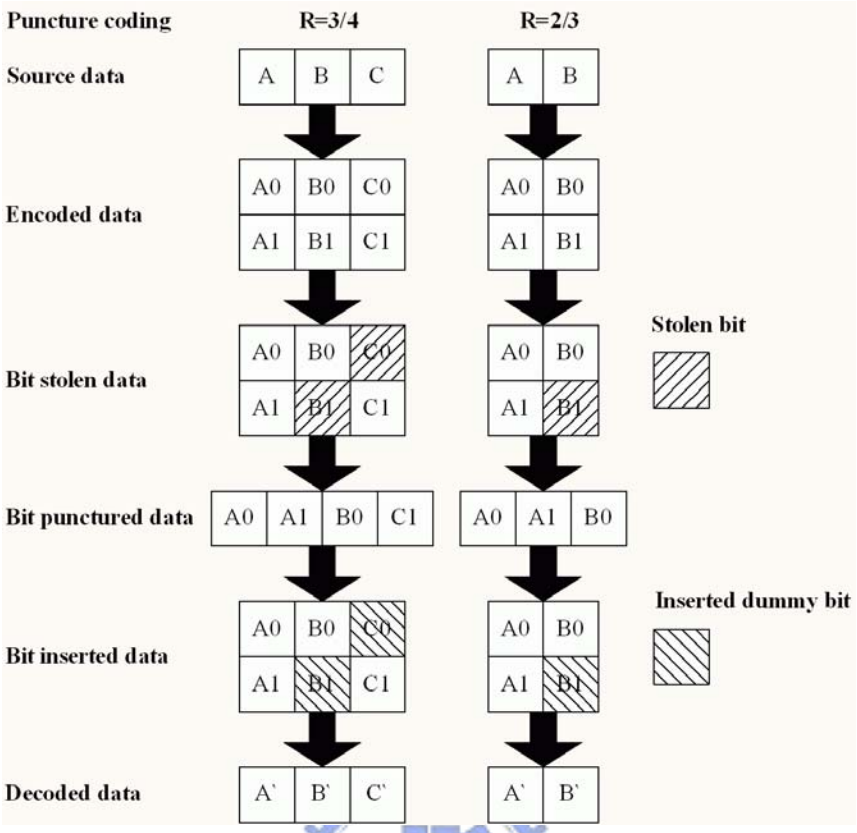


Figure 5: Puncture procedure

2.1.5 Mapping

The OFDM subcarriers shall be modulated by using BPSK, QPSK, 16-QAM, and 64-QAM modulation. The bits which have passed encoder and interleaver shall be divided into group N_{BPSC}(1,2,4, or 6) bits and converted into complex numbers representing BPSK, QPSK, 16-QAM, and 64-QAM constellation point in figure 6 . The mapping conversion adopts Gray-coded, illustrated in Figure 6. The output value d, are formed by multiplying the resulting (I+jQ) value by a normalization factor K_{MOD}, as described in Equation (2.5). The normalization factor is shown in table 2.

$$d = (I + jQ) \times K_{MOD} \tag{2.5}$$

Table 2: Normalization factor K_{MOD}

Modulation	K_{MOD}
BPSK	1
QPSK	$1/\sqrt{2}$
16-QAM	$1/\sqrt{10}$
64-QAM	$1/\sqrt{42}$

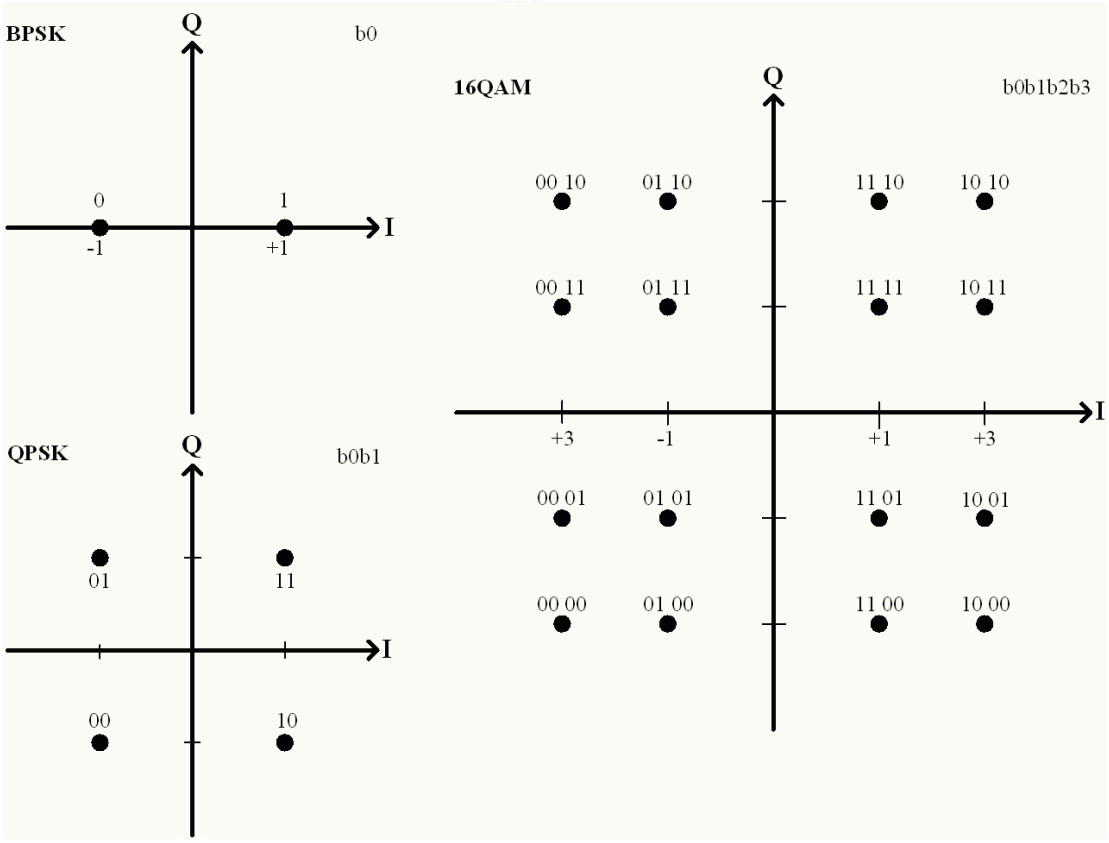


Figure 6-1: BPSK, QPSK, and 16-QAM constellation bit encoding

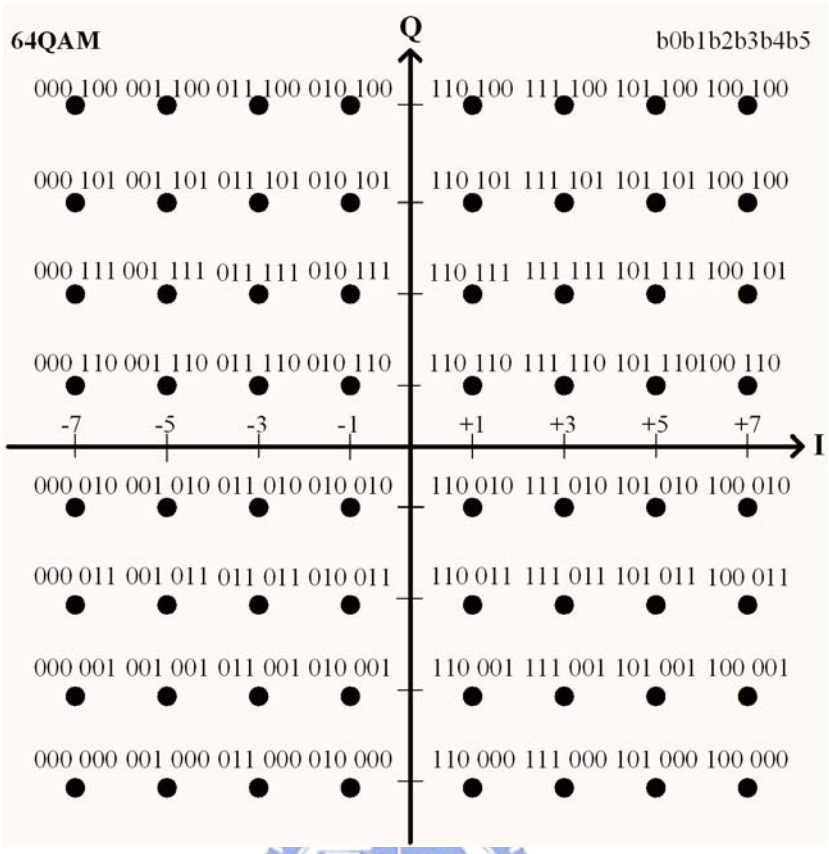


Figure 6-2: 64-QAM constellation bit encoding

2.2 System Requirements to Outer Receiver

2.2.1 Data Flow

From chapter 1, we know that the outer receiver consists of demapping, deinterleaver, depuncture, and Viterbi decoder. As shown in Figure 7, the equalizer takes 48 clock cycles to send one OFDM symbol useful data, and the demapping module shall be combinational circuit giving data to deinterleaver module. With different modulation and coding rate, the deinterleaver has specified output type which will be described in chapter 3. If the outer receiver speed requirement allows,

the outputs of demapping or depuncture modules can be removed but will increase clock latency.

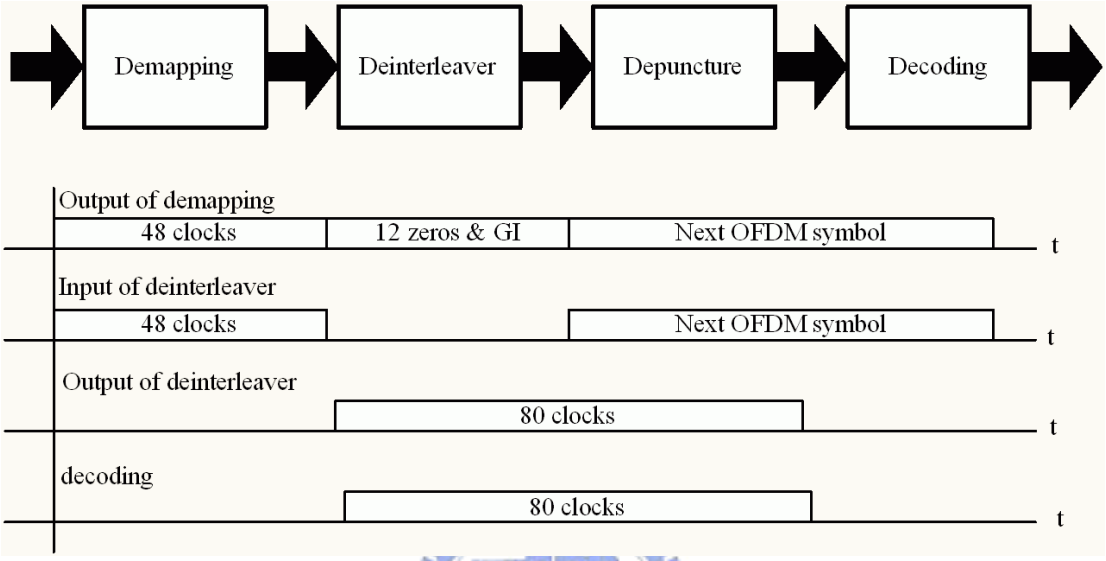


Figure 7: Outer receiver data flow timing diagram

2.2.2 Clock Latency Requirement

Depends on the symbol interval of timing-related parameters and outer receiver clock rate which have mentioned in chapter 1, we know that there are only 48 clock cycles which include useful data during one OFDM symbol 80 clock cycles, and other clock cycles are null bits and guard interval part. For pipeline architecture of outer receiver, we still have 80 clock cycles slack to decode the received data from equalizer. No matter what we use which modulation or coding rate, the decoding period needs to be kept within 80 clock cycles. In worst case 54Mbps (64-QAM,

coding rate 3/4), we define *Num*acs to be the stage number of ACS module radix-2. We need modified Viterbi decoder to satisfy the Equation (2.6).

$$80 \geq N_{DBPS} / Num_{acs} \quad (2.6)$$

*N*DBPS is the data bits per OFDM symbol. In worst case, *N*DBPS=216. So *Num*acs shall be 3 to satisfy Equation (2.6).

2.3 Modified Viterbi decoder Architecture

2.3.1 3 stages radix-2 ACS

According to the timing-related parameters and outer receiver clock rate, we modified Viterbi decoder architecture. From Equation (2.6), we set *Num*acs equal to 3. In the Viterbi decoder with 3 stages radix-2 ACS, the decoded bits are 3 bits every clock cycle. The throughput of Viterbi decoder is 60Mbps on clock rate 20MHz, not considering the whole system throughput.

2.3.2 Modified Outer Receiver clock rate

Although the design specification target on the clock rate 20MHz in outer receiver, we still can employ PLL technology to apply higher clock rate in outer receiver. Therefore, the ACS can decrease its stages number but still can complete the decoding work during one OFDM symbol period. Take an example: 1 stage radix-4 ACS applies clock rate 40MHz.

2.4 Multi-Rate System

There are 8 different rates in IEEE 802.11a, shown in Table 3. The incoming data after synchronization is subcarrier based with 20 MHz clock rate. The number of coded bits per OFDM symbol is varied with different modulation while the coded bits per subcarrier are also varied with modulation. The number of message bits per subcarrier is also varied with modulation. If we want to do real time decoding which means we have to decode a subcarrier per clock, this would result in variable throughput mechanism.

Table 3: The 8 data rates of IEEE 802.11a and the corresponding parameters

Data rate (Mbits/s)	Modulation	Coding rate	Coded bits Per Subcarrier	Coded bits Per OFDM symbol	Data bits Per OFDM symbol
6	BPSK	1/2	1	48	24
9	BPSK	3/4	1	48	36
12	QPSK	1/2	2	96	48
18	QPSK	3/4	2	96	72
24	16-QAM	1/2	4	192	96
36	16-QAM	3/4	4	192	144
48	64-QAM	2/3	6	288	192
54	64-QAM	3/4	6	288	216