Chapter 5

Integration and Evaluation

5.1 Integration

The task of the outer receiver is to decode the received data from the equalizer, including PLCP header and DATA part of PPDU shown in Figure 51. The PLCP header includes the information of RATE and LENGTH. Table 10 shows the contents of RATE field. The first coded OFDM symbol given by the equalizer must be the PLCP header. The modulation type of the header is BPSK, and the data rate is 1/2. The decoded procedure of the PLCP header is different from other data rate case. For the data flow issue, the equalizer has to transmit the next coded OFDM symbol as soon as possible. Therefore, while the all header data enter the traceback module, the decoder begins to throw the output bits. The header is decoded faster, the throughput rate is higher. So the traceback-length should be cut to be 8-state (8x3=24).

Table 10: Contents of the RATE field

Rate(Mbit/s)	RATE field
6	1101
9	1111
12	0101
18	0111
24	1001
36	1011
48	0001
54	0011

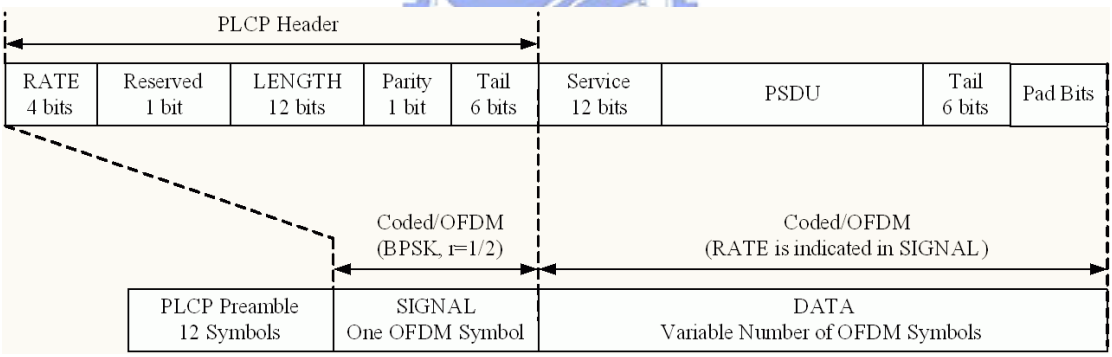

Figure 51: IEEE 802.11a packet data frame format

Remember that the component after Viterbi decoder is the scrambler mentioned in Figure 2. In general, the scrambler on transmitter side and on receiver side is the same one. In the proposed outer receiver, the number of the Viterbi decoder output bits each time is 3-bit. Therefore, we shall modify the original scrambler suit to the 3-bit input

as depicted in Figure 52. And as depicted in Figure 53, the indicators of the receiver are presented, including header error and correct header cases. Finally, the proposed outer receiver is shown in Figure 54.

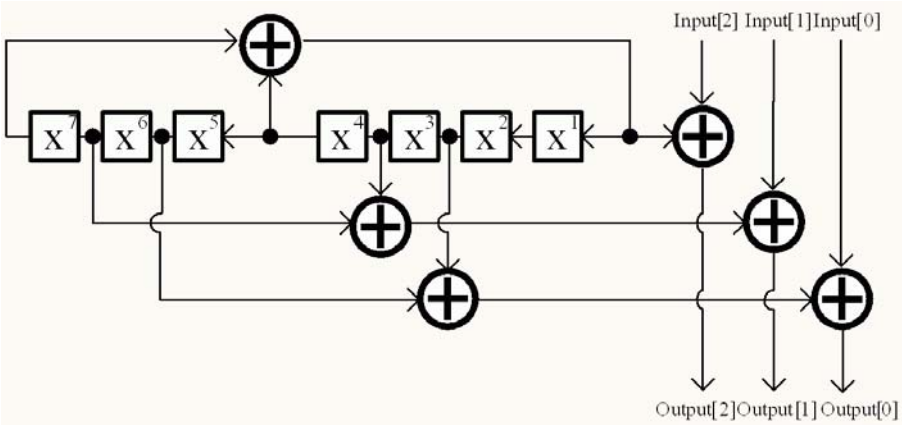

Figure 52: The modified 3-bit scrambler

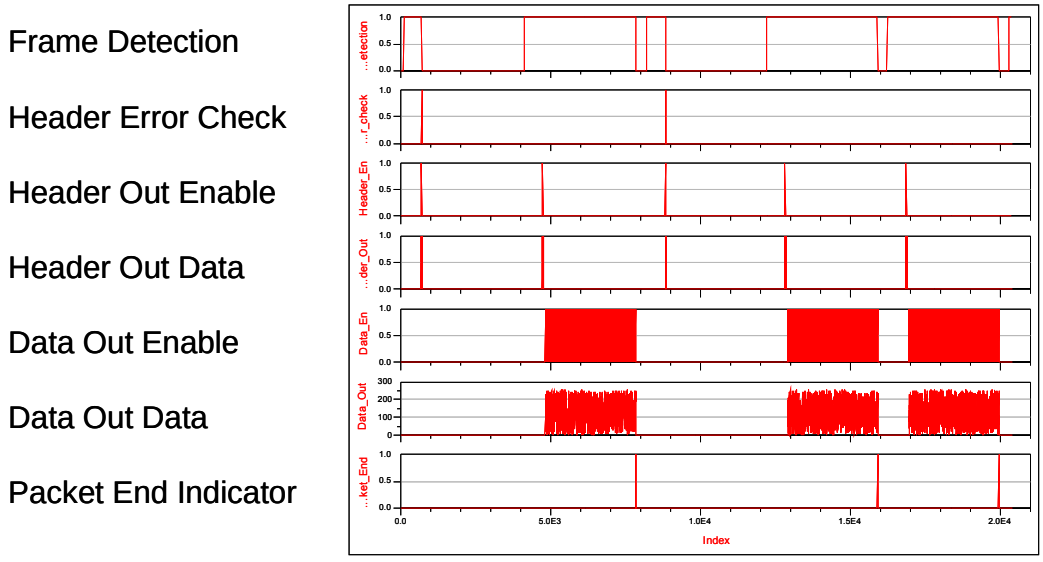

Figure 53: The indicators of the receiver

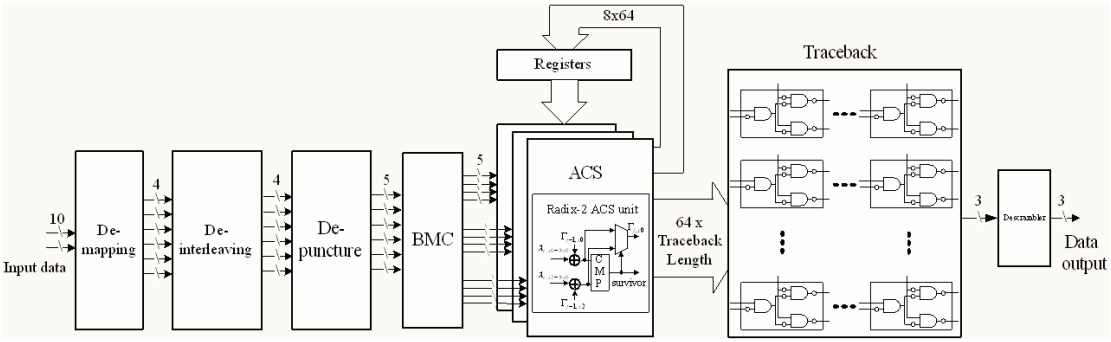

Figure 54: The proposed outer receiver architecture

5.2 The Interface between Outer Receiver and MAC

Since the PLCP header contains the information of RATE, LENGTH, the output result will be wrong while the contents of RATE and LENGTH go wrong. Therefore, the outer receiver shall prevent from the event happened. The RATE field has the specified format shown in Table 10 and so if the other case appears, the header error occurs. And we have the even parity check and tail bits for the detection of the header error. If the header error occurs, the outer receiver will request MAC to transmit the OFDM symbol of header again. In Figure 55, RF, baseband, and MAC interface is presented. MAC transmits one byte data to the baseband transmitter. Although the proposed outer receiver decodes 3 bits output each time, we collect 1-Byte and transmit the data to MAC.

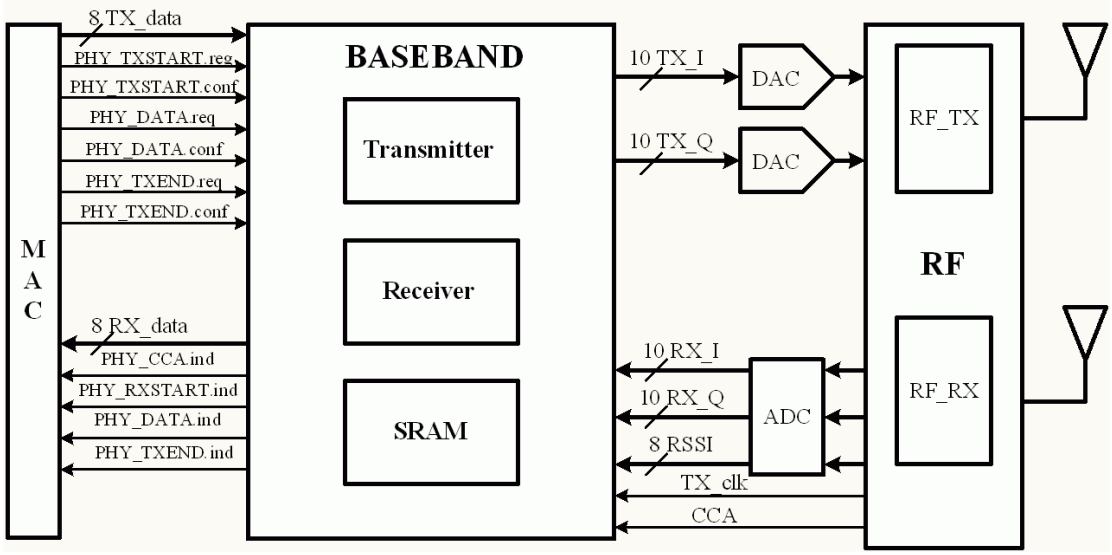

Figure 55: RF, baseband and MAC interface

5.3 Evaluation

We integrate IEEE 802.11a transmitter, inner receiver which includes frame synchronization, FFT/IFFT, equalizer, and the proposed outer receiver into IEEE 802.11a transceiver. Besides the outer receiver, all other IPs are provided by TWT lab research members. By Agilent ADS simulation platform, we can simulate the hardware performance. For the convenience of packet error detection, we adopt CRC-16 to the transmitter and receiver, which CRC-16 is depicted in Figure 56. We calculate the packet error rate (PAR) at a length of 1024 bytes. In Figure 57, the PAR result for 8 different data rate with traceback-length 90 is shown.

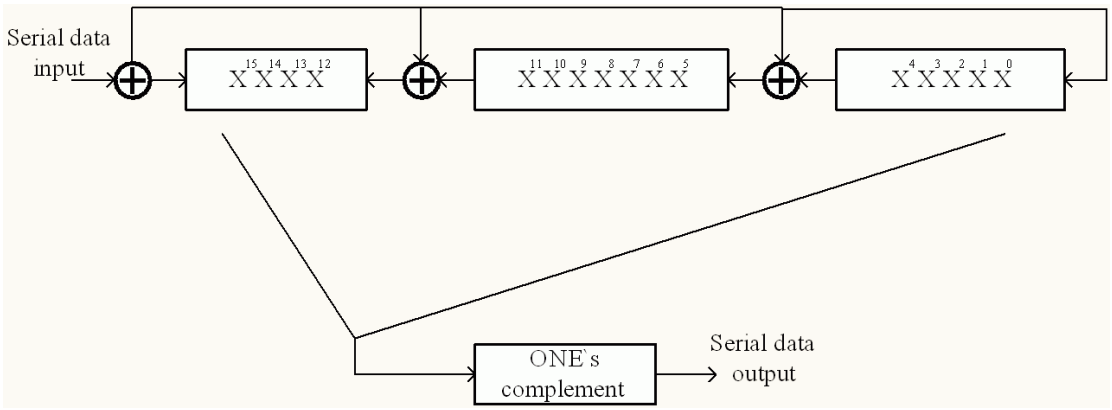

Figure 56: CRC-16 structure

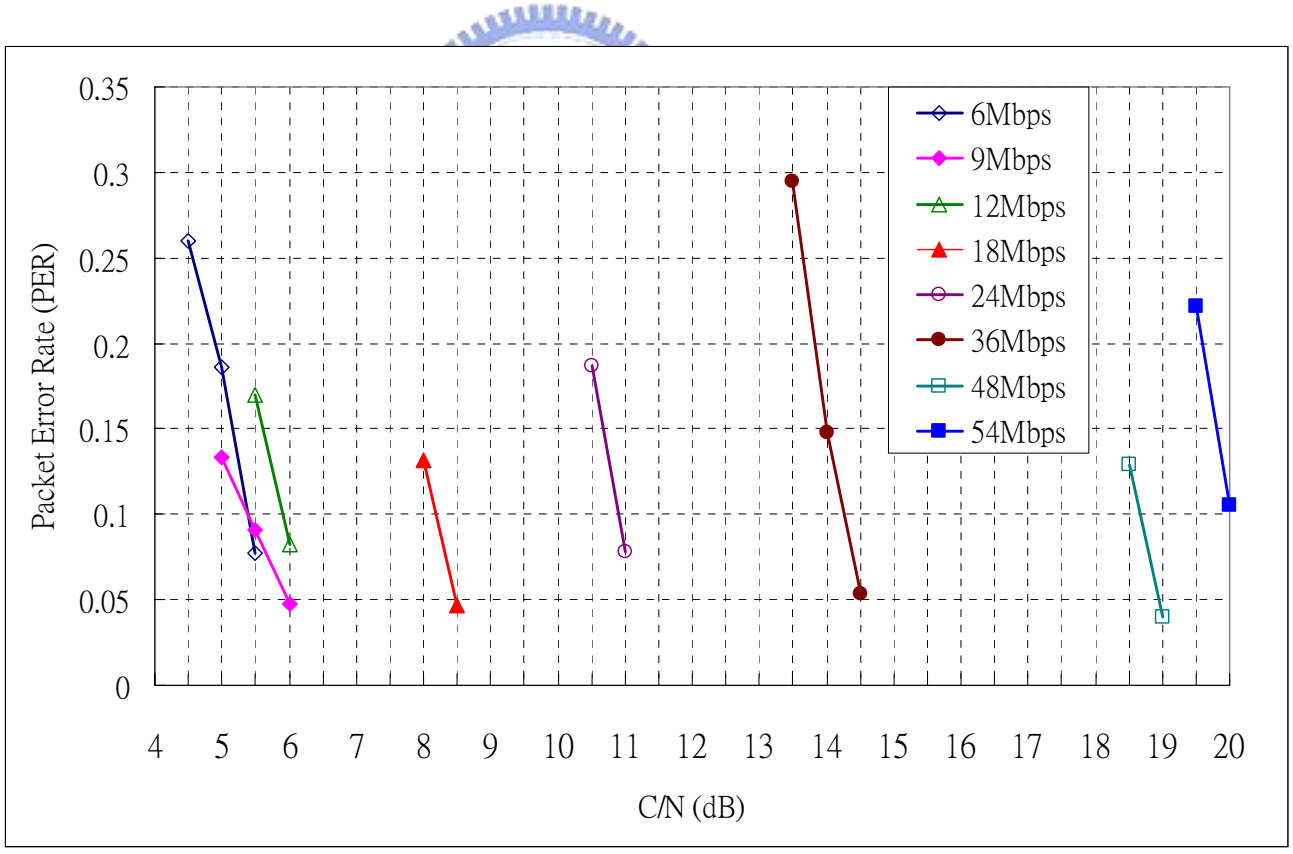

Figure 57: PER for 8 different data rate with traceback-length 90

5.4 Comparisons

We take some published Viterbi decoders which are listed below [6] [11] [12] [13] as comparison with the proposed Viterbi decoder in Table 11. Because these Viterbi decoders employ in specified applications, they concern about different performance issues. The low complexity and high performance design can be implemented in our implementation.

Table 11: Comparisons of Viterbi decoders

Ref	Specfication	Feature	Power	Speed	Area	Gate Count	Traceback-Length	Soft-decision Resolution
[6]	(2,1,7) convolutional code	VLSI Design and Implementation of High-Speed Viterbi Decoder	183mW @2.5V	200Mb/s @100Mhz	3.88mm^2 @0.25um CMOS	50k	32	3-bit
[11]	(2,1,7) convolutional code	A Viterbi decoder based on Shuffle-exchange type Interconnection structure		19Mb/s @19Mhz	39.78mm^2 @1.2um CMOS			
[12]	(2,1,7) convolutional code	Scalar power and area efficient high throughput Viterbi decoder	120mW @3V	50Mb/s (100MBd)	1.42mm^2 @1.2um CMOS			
[13]	(2,1,7) convolutional code	A 16-level radix-4 decoder with match path and prediction algorithm	83mW @3.3V	133Mb/s @66Mhz	5.69mm^2 @0.35um CMOS	156k		4-bit
	(2,1,7) convolutional code	The proposed Viterbi decoder	78.85mW @1.8V	75Mb/s @25Mhz	4mm^2 @0.18um CMOS	131k	63	4-bit

Beside the comparison with Viterbi decoders, we also compare the system performance between the proposed design and Atheros. Table 12 shows the SNR of PER achieve 10% at a length of 1024 bytes. If we apply traceback-length 90 to the receiver system simulation, we can get better performance.

Table 12: Comparison with Atheros for PER versus SNR for system performance

Data rate (Mbps)	Atheros Design SNR	T=90 Design Design SNR	
6	5.4	5.4	0
9	5.8	5.4	-0.4
12	7	5.9	-1.1
18	9.5	8.1	-1.4
24	11.3	10.9	-0.4
36	14.9	14.3	-0.6
48	18.6	18.6	0
54	20.6	20.1	-0.5