國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

適用於 802.11a/b/g 無線區域網路之 CMOS 前端發射器設計

5/2.4GHz CMOS Transmitter Front-End Design for 802.11a/b/g Wireless LAN

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中華民國九十三年六月

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碩士論文

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摘要

這篇論文依據 IEEE 802.11a/b/g standard 的規範，提出雙頻前端發送器的規格。同時採用聯電 CMOS 0.18 微米混合信號製程，分別針對高線性度及低功率的考量完成兩個 5GHz 直接轉換(Direct-Conversion)前端發射器設計。量測結果顯示，高線性度的前端發射器在低頻(BB/1MHz)信號及本地振盪(LO/5.25GHz)輸入下，升頻後輸出之高頻(RF/5.251GHz)信號，可獲得功率轉換增益 8.6dB，同時在輸入功率-5.3dBm 之 1dB 壓縮點(P1dB)有最大輸出功率 2.3dBm，及擁有 6.3 dBm IIP3 及 13 dBm OIP3 的高線性度。此電路在 1.8V 供應電壓下消耗 68mW 功率，可滿足 802.11a 54Mb/s 64QAM 信號傳送 mask 的要求。最後，並以此 5GHz 電路模組完成了雙頻前端發送器設計，該發送器為了節省功率及降低面積，共用單一一個升頻混波器加上兩個前端放大器分別對 5GHz 及 2.4GHz 頻段信號作放大，模擬結果分別在 2.4GHz 操作下達到 7dB 轉換增益，並在輸入功率 1dB 壓縮點

(P1dB)-5dBm 下有最大輸出功率 1dBm，而在 5.25GHz 操作下達到 7.1dB 轉換增益，並在輸入功率 1dB 壓縮點(P1dB)-5.3dBm 下有最大輸出功率 0.4dBm，皆符合雙頻發送器的規格規範，該電路在 1.8V 供應電壓下消耗 44mW 功率。

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Abstract

Based on IEEE 802.11a/b/g standards, the specification of dual-band transmitter front-end has been specified. Two 5GHz CMOS RF transmitters front-end have been implemented by UMC 0.18um CMOS mixed-mode technology. One is designed for high linearity while another is designed for low power applications. The transmitters adopted the same direct-conversion architecture and composed of a quadrature single-side band mixer and a pre-amplifier. With inputting 1MHz base band (BB) signals and 5.25GHz local oscillator (LO) signals, after up-conversing, the output frequency locates at 5.251 GHz. The measurement results exhibit that the TXFE for high linearity design achieves enough conversion gain of 8.6 dB for specification, and obtains high linearity performance of 6.3 dBm IIP3 and 13 dBm OIP3. Moreover, the

maximum output power is 2.3dBm for input 1dB compression point of -5.3 dBm (P1dB). This transmitter could meets the transmit spectrum mask for 802.11a 54Mb/s, 64QAM signals with consuming 68mW at 1.8V power supply. Finally, based on this 5GHz transmitter architecture, the dual-band transmitter front-end has been proposed. To improve the power consumption and decrease the circuit area, a novel architecture adopted single mixer and followed by two pre-amplifiers. Simulation results indicate that this design achieves 7.0dB conversion gain, and obtains the maximum output power of 1dBm for -5dBm P1dB for 2.4 GHz operation while achieves 7.1dB conversion gain, and obtains the maximum output power of 0.4dBm for -5.7dBm P1dB for 5.25 GHz operation which could meet the specifications of dual-band transmitter front-end. This dual-band transmitter consumes only 44mW at 1.8 power supply.

To My Family

獻給我的家人

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很高興終於能夠順利完成這篇論文，首先要感謝我的指導教授溫瓌岸教授。老師在我碩士班這兩年多來，在學識上、或是在人生啟蒙上都給予我悉心的指導與教誨。若沒有老師的鞭策，這本論文絕對無法完成。此外，感謝高曜煌教授、詹益仁教授、與陳巍仁教授撥冗擔任我的口試委員，耐心聆聽與指教，並提供寶貴意見，使得本論文得以更加完整。

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誌于　　2004

林木山

Contents

List of Figures

List of Tables

Chapter 1
Introduction

1.1 Background

In recent years, the proliferation of multiple WLAN standards has created the need of multi-mode, multi-band transceivers. The extent of the demands made on multi-standard single RF chips further increases the complexity of the circuits and the required flexibility, these requirements lead to high power consumption, degradation of low-noise characteristics, and large chip size. Therefore, it attracts the research of design and integrating multi-mode/multi-band RF circuits. The major challenge of such a flexible radio is the ability to operate at a wide radio frequency (RF) range and a varied dynamic range while preserving power efficiency and maintaining low cost. CMOS process technology has been proven to be a viable candidate for a low-cost radio solution due to its compatibility with high levels of integration.

1.2 Motivation

For the concern of high integration and low power consumption, there are a few

existing designs with dual or multiple frequency bands [8], [9].The most popular architecture is to design individual transmitting paths for different communication standards. The disadvantage of such design is its large area required, and duplicated power consumption. And the more advanced design is to merge different modules (ex: LNA and mixer) to save current dissipation [1], or to design a single module with dual-band operation [2], which has saved the chip area and obtain higher integration level.

In this thesis, the objective is to derive a transmitter design applied for dual-band dual-mode WLAN IEEE 802.11 a/b/g standard. The transmitter consists of a quadrature mixer and a power amplifier driver: pre-amplifier. The mixer has two input signals: base band modulated signal and local oscillator (LO) signal which provides the carrier frequency of up-conversion, and one output signal: radio frequency (RF) after up-conversion. Since the LO matching is not so critical, although operating on high frequency band, a novel mixer reuse structure with dual-band LO matching was proposed. After up-conversion by the mixer, the output signal of 5 GHz and 2.4 GHz then pass through a dual-band LC-tank filter which separates into two paths for further processing by two pre-amplifiers. The proposed RF front-end not only maintains its high-integration, it is also expandable to multiple frequency bands if necessary. These are the factors that make our RF

front-end architecture highly suitable for the mobile systems in the future.

1.3 Existing Architectures

Based on the reason of easily integrating, the direct-conversion architecture was chosen rather than super-heterodyne architecture. Detail comparison will be described latter. The mixer design of the transmitter faces many compromises between conversion gain, local oscillator power, linearity, noise figure, port-to-port isolation, voltage scaling and power consumption, especially for 5 GHz than 2.4 GHz band design. **TABLE 1** lists the literatures proposed in recent years.

TABLE 1 5-GHz Transmitter Performance of Recently Literatures

	JSSC[3]	JSSC[4]	JSSC[5]	JSSC[6]	JSSC[7]	ISSCC[8]	ISSCC[9]
	2000(a)	2002(a)	2003(a)	2003(a)	2003(a)	2004(a/b/g)	2004(a/b/g)
Process	0.25	0.25	0.18	0.18	0.18	0.18	0.25
P1dB(dBm)			19				
O-P1dB(dBm)	-2.5			6	5		
OIP3(dBm)					15	17.3/13.3	
Carrier Suppression(dB)	22.4	29		41	38		
Side-band Rejection(dB)	33.4	51		54	50		45
EVM(dB)			-33	-33	-29.3		
Output Power(dBm)		22		-5		0/-1	8//9
TX Power Dissipation(mW)	120	790	380	302	135	134	670/710
Integration		PA	LPF/VGA/PA	DAC/LPF	LPF		PA

And Fig. 1 summarize the required performance for each specification such as

ouput-P1dB, OIP3, carrier rejection, side-band rejection and maximum output power, etc.

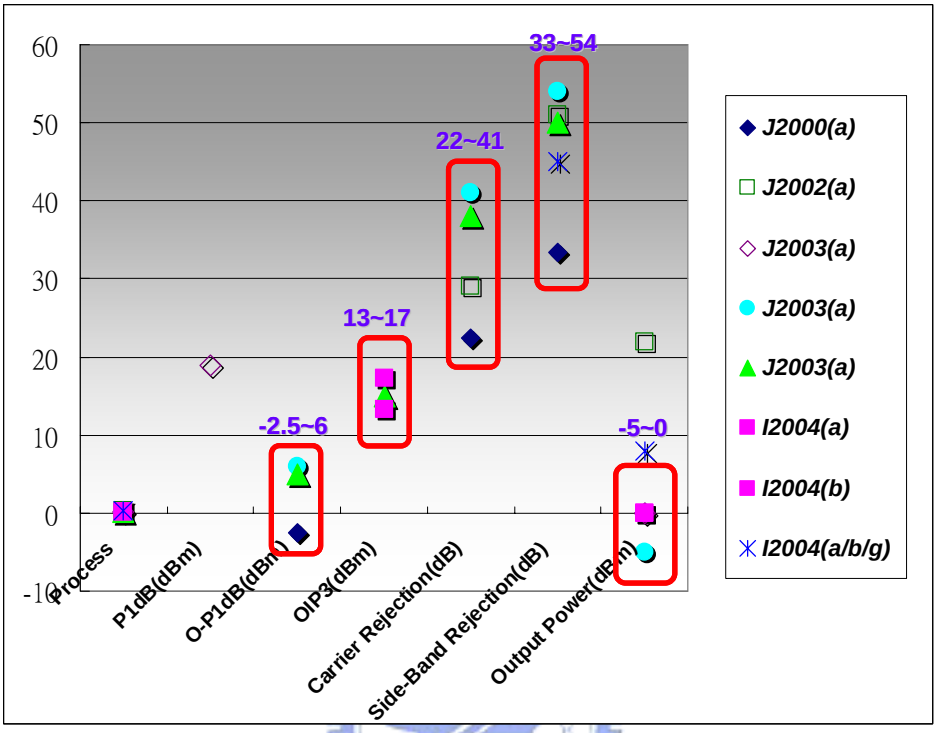


Fig. 1 Performance Summary of the Literatures

In this work, two 5 GHz CMOS direct-conversion transmitters with different circuit architectures have been implemented for 802.11a transmission specification. After comparing the performance of both architectures, one of the two implementations has been applied for another dual-band design. A novel mixer reuse dual-band transmitter has been implemented that is capable of operating at two different frequencies and satisfies the specification of 802.11a and 802.11b, respectively.

1.4 Organization

This thesis describes the design of RF transmitter frond-end for 5 GHz and 2.4 GHz wireless LAN applications. Chapter 2 reviews two conventional transmitter architectures, and states the advantages and drawbacks of each architecture and also expresses why a direct-conversion architecture was chosen, what issues will induce and how to resolve. Chapter 3 introduces the IEEE 802.11a and 802.11b standard for transmission, and institutes the transmitter specification which could meet these two standards simultaneously. Chapter 4 deals with the analyses for mixer, and pre-amplifier, respectively. Chapter 5 then describes two implementations of 5 GHz transmitter. One is designed for high linearity while the other is designed for low power application. After comparing the performance of these two transmitters, a dual-band transmitter has been proposed. Chapter 6 shows the experimental results including layout considerations, high frequency balun design, testing setup, and measurement results. Chapter 7 draws a conclusion and states how to improve this work in the future.

Chapter 2

Architecture

The recent surge in application of radio-frequency (RF) transceivers has been accompanied with aggressive goals: low cost, low power dissipation, and small form factor. The architecture and frequency plan of the RF transceiver play an important role in the complexity and performance of the overall system. Because the base band signal is produced in the transmitter and hence is sufficiently strong. There are fewer transmitter architectures than those of receivers, due to issues such as noise, interference rejection, and band selectivity being more relaxed in transmitter designs. Two of the most common choices in transceiver architecture are the traditional "super-heterodyne" and "direct conversion" architecture [11].

2.1 Super-Heterodyne Transmitter

2.1.1 Operation of Super-Heterodyne Transmitter

A transmitter architecture as shown in Fig. 2 is called "super-heterodyne" architecture [10]. In the first stage, after passing through the DAC and low-pass

filter (LPF) to select the desired band signal, the base band modulated in-phase and quadrature-phase signals first up-converse to intermediate frequency (IF) by LO1, and then sum up. This stage is followed by a band-pass filter (BPF) to filter out-of-band image occurred from the mixer in the first stage. Continuously, the intermediate frequency signal up-converses again to expected RF band by LO2 and followed by another band-pass filter (BPF) to further filter out-of-band image and then a power amplifier driver and finally a power amplifier to amplify the signal to desired power level.

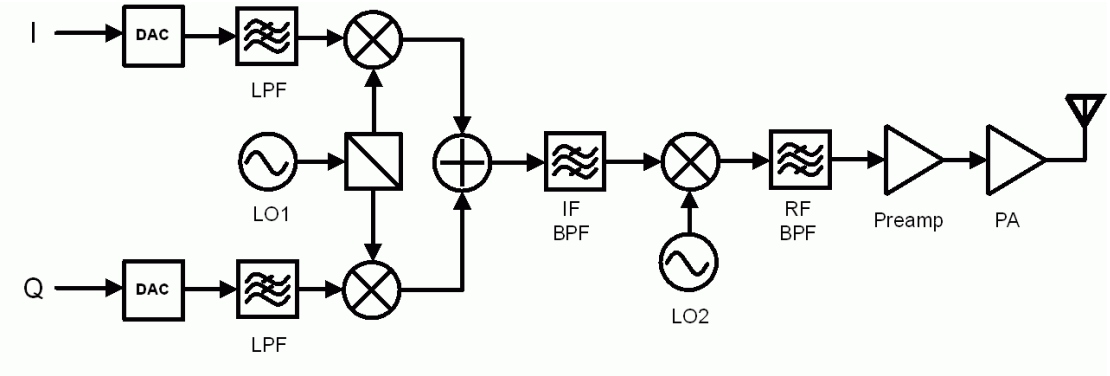


Fig. 2 Super-Heterodyne Transmitter

2.1.2 Advantages and Drawbacks

Due to the twice of up-conversions, a super-heterodyne transmitter is also called “two-step transmitter”. By properly choosing the IF frequency, the frequency of two VCOs: LO1 and LO2 will be far from the frequency of the PA and this will prevent the “injection pulling” problem. The injection pulling phenomenon will be express later. Besides, since the in-phase and quadrature-phase signals are summed

at IF frequency which will be lower than RF frequency, I/Q mismatch problem resulted from process variation will be mitigated. However, a high-Q filter is required for the image-reject BPF, but a high-Q filter is hard to implement on chip. This violates the objectives of highly integration and low cost. In the meanwhile, two frequency synthesizers are needed for each LO1 and LO2 resulting in more circuits and higher power consumption. Finally, the frequency planning is complicated for LO1 and LO2 to avoid the image problem as far as possible.

2.2 Direct-Conversion Transmitter

2.2.1 Operation of Direct-Conversion Transmitter

Another conventional architecture for transmitter is shown as Fig. 3. As implied by the name of “direct-conversion”, the base band in-phase and quadrature-phase signals first pass through the DAC and low-pass filter (LPF) and then directly up-converse to RF band by only one mixer and of course only one LO signal is required. After summing the I/Q signals on RF band, continuously, the signal passes through a power amplifier driver: pre-amplifier and a BPF as well, and finally passes through a power amplifier to provide enough power level to the antenna. As for the BPF, its function is the same as the last one in super-heterodyne transmitter to filter out-of-band image

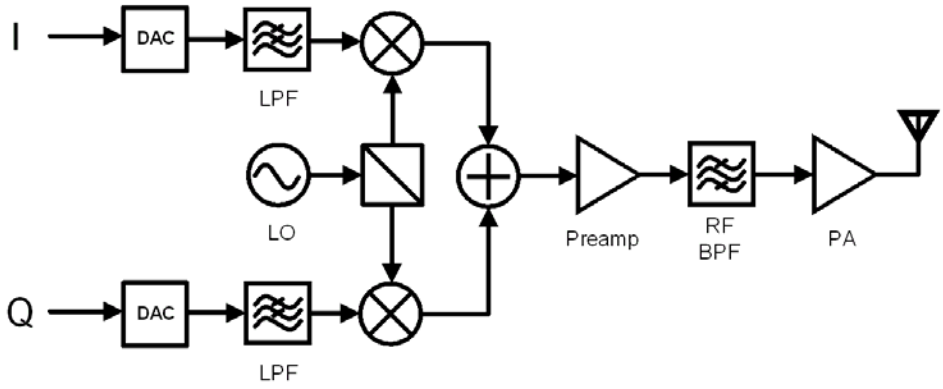


Fig. 3 Direct-Conversion Transmitter

2.2.2 Advantages and Drawbacks

Obviously, the difference of direct-conversion transmitter from super-heterodyne one is that only one frequency synthesizer for LO is needed and no high-Q BPF is required. Therefore, comparatively speaking, a direct-conversion transmitter has the benefit of lower power consumption and highly integration. However, at the cost of suffering from some issues: LO leakage, injection-pulling, etc.

a. LO Leakage

As we know that the coupling between radio frequency signals is very serious and almost inevitable. As for direct-conversion transmitter, the coupling effect will result in LO signal leaks to base band or to RF band as shown in Fig. 4. The LO leakage to base band will have LO signal modulated by itself. This “self-mixing” effect will induce a DC-offset term at the mixer output, and probably saturates the

DC operation of the next stage [12]. Besides, the LO leakage to RF band will desensitize next stage since for direct-conversion transmitter, the LO frequency is the same or almost close to the desired RF frequency. However, this issue will be mitigated by properly choosing the mixer architecture and carefully layout.

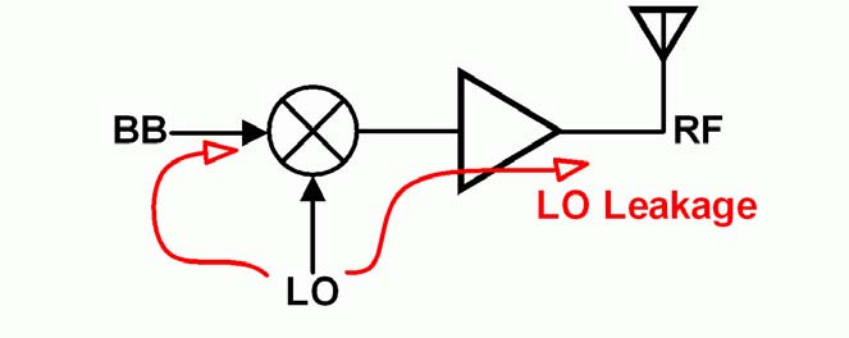


Fig. 4 LO Leakage Issue

b. Injection-Pulling

In a direct-conversion architecture, assume the frequency of the interference signal (injected signal) is close to the frequency of the desired signal and has a magnitude comparable to the desired signal. When magnitude of the interference increases, frequency of the desired signal may shift toward the interference frequency and eventually be locked to that frequency. This phenomenon is called “Injection Pulling” or “Injection Locking” [11]. Fig. 5 describes the phenomenon of injection pulling that the LO pulling goes more critical as the output power rises. Because the carrier frequency is equal to the local oscillator frequency in a direct-conversion architecture and the power of a PA is higher than that of the local

oscillator, it is easier to induce large interference. Even the injection level is 40 dB below original LO, it may still creates considerable disturbance. Thus, good isolation from PA to VCO becomes important. Usually, VCO must be followed by a buffer stage to improve isolation and driving ability.

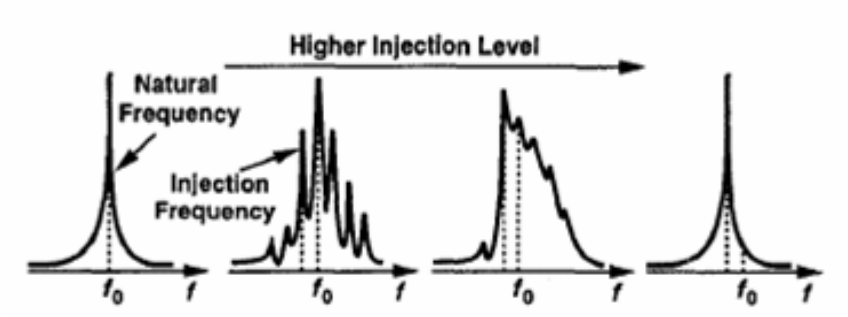


Fig. 5 Injection Pulling [11]

Further, this phenomenon can be resolved by "offsetting" the LO frequency. That is, by adding or subtracting the output frequency of another oscillator. But another mixer and BPF are required. Additionally, a new architecture of "Even-Harmonic mixer" has been induced against this problem [13][14]. This novel architecture is able to merely use half of LO frequency to achieve the same RF modulated frequency.

2.3 Summary

The direct-conversion architecture is more easily to be integrated than super-heterodyne since the latter requires a high-Q band pass filter. Therefore large lump components are forced to be implemented off chip. The use of direct-conversion techniques is a promising approach for highly integrated wireless

transceivers due to their potential for low-power fully monolithic operation and extremely broad bandwidth. Their potential for broadband operation is especially important for future wireless communication applications, where a combination of digital cellular, GPS, and WLAN applications are required in a single portable device. Based on these reasons, the direct-conversion architecture is chosen as the system architecture.

Chapter 3

System Behavior Analysis

In this chapter, the IEEE 802.11a and 802.11b standard will be introduced. Since IEEE 802.11g adopts both the modulations of 802.11a/b standard, a specification of transmitter front-end suited for 802.11 a/b/g will be instituted.

3.1 Specification Introductions

3.1.1 IEEE 802.11a Standard

a. Operating Channels

The operating channel scheme for 802.11a standard is depicted in Fig. 6, which shall be used with the FCC U-NII (Unlicensed National Information Infrastructure) frequency allocation [15]. The total bandwidth is 300 MHz divided for lower, middle, and upper sub-bands. The lower and middle U-NII sub-bands accommodate eight channels in a total bandwidth of 200 MHz. The upper U-NII band accommodates four channels in a 100 MHz bandwidth. The centers of the outermost channels shall be at a distance of 30 MHz from the edge of band for the lower and

middle U-NII bands, and 20 MHz for the upper U-NII band. The total frequency range is 5.15-5.25 GHz for lower band, 5.25-5.35 GHz for middle band, and 5.725-5.825 GHz for upper band, respectively. The bandwidth of each channel is 20 MHz, and each channel has 52 sub-carriers for OFDM modulation with each sub-carrier having bandwidth of 300 kHz. The maximum output power constraint with antenna gain is 40mW for lower band, 200mW for middle band, and 800mW for upper band, respectively.

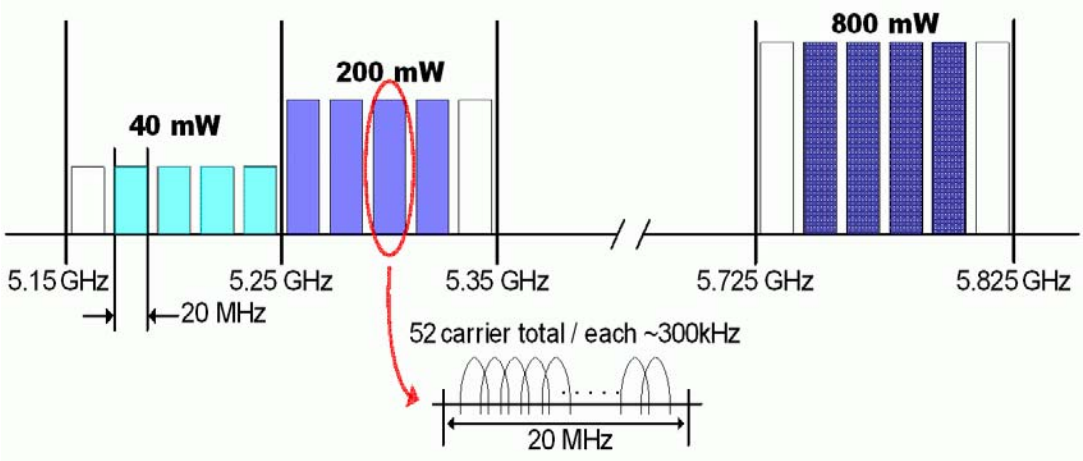


Fig. 6 Channel Allocation of 802.11a Standard

b. Transmit Spectrum Mask

The transmitted spectrum shall have a 0dBr (dB relative to the maximum spectral density of the signal) of bandwidth not exceeding 18 MHz, -20dBr at 11Mhz frequency offset, -28dBr at 200 MHz frequency offset and -40dBr at 30 MHz frequency offset and above. The transmitted spectral density of the transmitted signal shall fall within the spectral mask, as shown in Fig. 7.

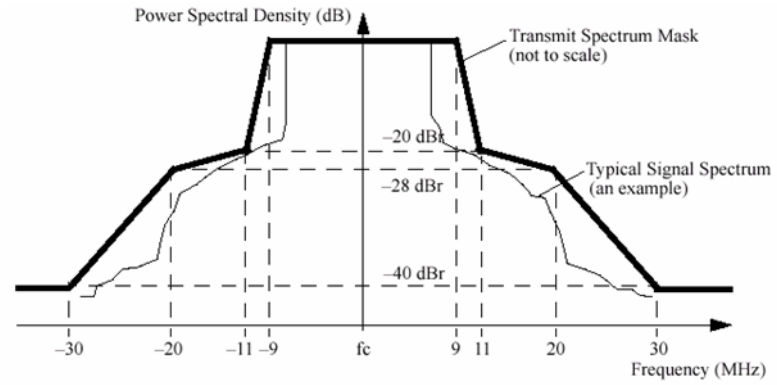


Fig. 7 802.11a Transmit Spectrum Mask

c. PAPR Requirement

As for PAPR constraints, since each channel in IEEE 802.11a standard composes of 52 sub-carriers. By imaging that each of the 52 sub-carriers of the OFDM signal is a single-tone sinusoid wave such that the composite waveform in the time domain will have large peaks and valleys. If the peaks of all 52 sinusoid waves should line up in time, the peak voltage will be 52 times larger than that of a single sinusoid wave. In this critical case, the peak-to-average ratio will be 10log (52)=17 dB. Therefore, the transceiver must be able to accommodate signals whose peak amplitudes are 17 dB larger than the average signal. This translates into the need for a large power back-off in the transmitter. However, in practical applications, since the signal peaks are infrequent, the peak-to-average ratio requirement can be significantly less than 17 dB without major degradation in the overall SNR. For instance, in the case of 16-QAM modulation, simulation indicates that a 6dB peak-to-average ratio degrades the system SNR by only 0.25 dB [4]. And in practice,

peak-to-average ratios as low as 4 dB may meet the error vector magnitude (EVM) and packet error rate (PER) requirements of the IEEE 802.11a specifications. Generally, a 6dB PAPR is demanded for moderate performance. But in this thesis, the PAPR was set to be 7dB for 1dB design margin.

d. Center Frequency Leakage

Certain transmitter implementations may cause leakage of the center frequency component. Such leakage shall not exceed -15 dB relative to overall transmitted power or, equivalently, +2 dB relative to the average energy of the rest of the sub-carriers.

3.1.2 IEEE 802.11b Standard

a. Operating Channels

The IEEE 802.11b standard can be discriminated by two operation areas: North American and European [16]. In this thesis, the design target is the North American operation. The operating channels scheme for 802.11b standard is shown as Fig. 8. The frequency range is from 2400 MHz to 2483.5 MHz with total bandwidth of 83.5 MHz. For non-overlapping operation, three channels are used and the channel center frequencies are: 2412 MHz, 2437 MHz, and 2462 MHz, respectively. Each channel has bandwidth of 20 MHz. As for overlapping operation, six channels are selected. The center frequency of each channel shall be at a distance of 10 MHz from the

others from 2412 MHz to 2462 MHz. The maximum allowable output power for North American operation is 1000mW.

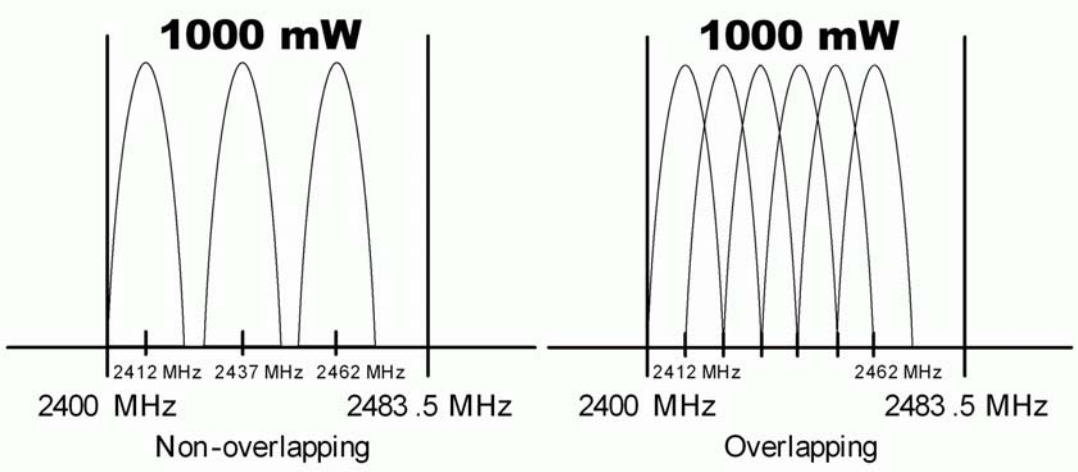


Fig. 8 Channel Allocation of 802.11b Standard

b. Transmit Spectrum Mask

The transmitted spectrum shall have a 0dBr (dB relative to the SIN(x)/x peak) bandwidth not exceeding 22 MHz, -30dBr at frequency offset of 11MHz to 22 MHz, -50dBr at frequency offset of 22 MHz and above. The transmitted spectral density of the transmitted signal shall fall within the spectral mask, as shown in Fig. 9.

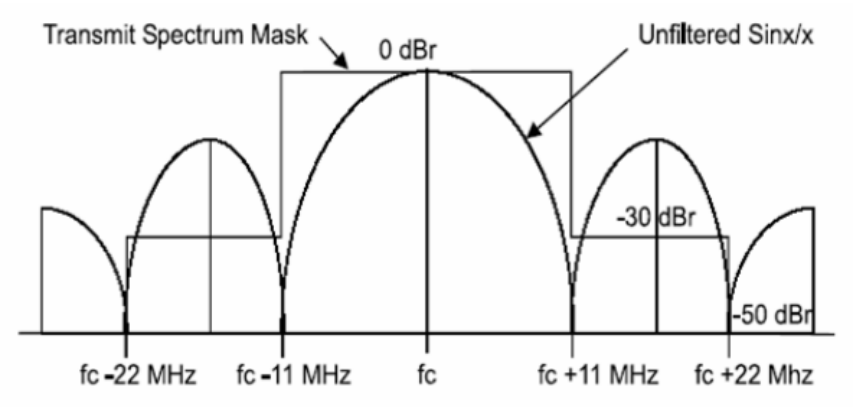


Fig. 9 802.11b Transmit Spectrum Mask

c. Center Frequency Leakage

The RF carrier suppression, measured at the channel center frequency, shall be at least 15 dB below the peak SIN(x)/x power spectrum. And this RF carrier suppression shall be measured while transmitting a repetitive 01 data sequence with the scrambler disabled using D-QPSK modulation.

3.1.3 Summary

As we know that the 802.11g standard adopts both the modulations of 802.11a and 802.11b with data rate from 1 to 54Mbps and the transmission requirement for 802.11g also agrees with 802.11a/b respectively. A simple summary of specification about 802.11 a/b/g is listed at **TABLE 2**.

TABLE 2 802.11a/b/g Specification Summary

	802.11a/g	802.11b/g
Frequency range	5.15~5.825 GHz	2400~2483.5 MHz
Channel bandwidth	20MHz	About 20MHz
Total bandwidth	300 MHz	83.5 MHz
Modulation	OFDM	CCK/DSSS
Data rate	6~54 Mbps	1~11 Mbps
Maximum output power	200 mW(Middle Band)	1000mW(USA)
Carrier suppression	15 dBc	15 dBc
PAPR requirement	4~6dB at least	

From the table above, in order to conform with the 802.11a and 802.11b or even 802.11g standards, a minimum operation bandwidth of 300 MHz is required. As for the maximum output power level will be discuss later.

3.2 System Architecture

The whole direct-conversion transceiver is shown as Fig. 10. The analog RF transceiver consists of a transmitter, a receiver, and single frequency synthesizer. The transmitter front-end contains two quadrature mixers for I/Q channel respectively and a single pre-amplifier while the back-end includes a band-pass filter, and a power amplifier.

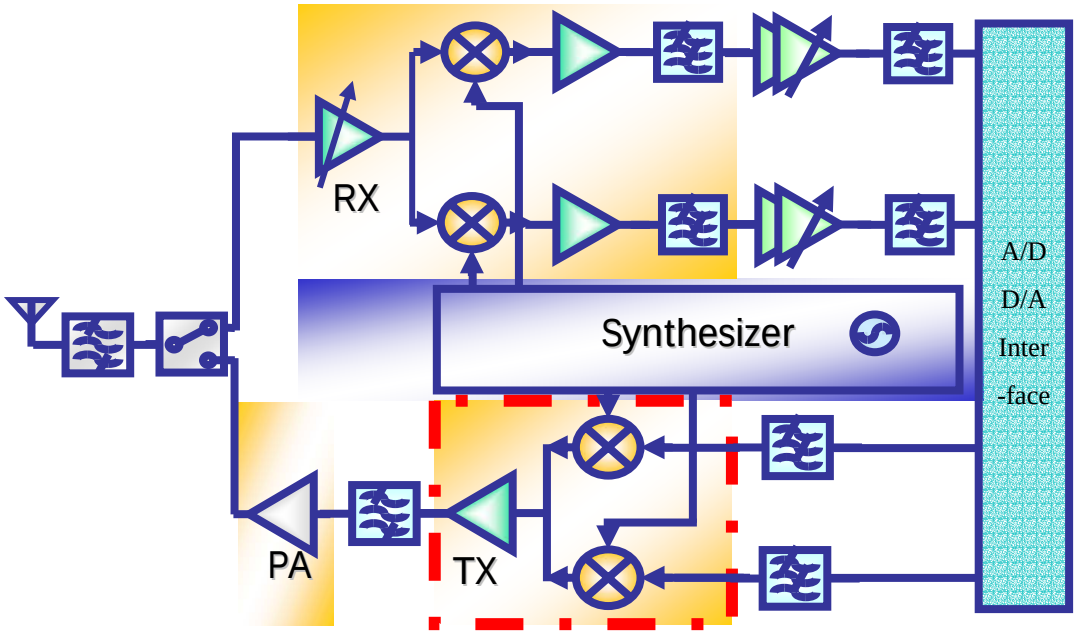


Fig. 10 Analog Transceiver Architecture

3.3 Specification Analysis

In this section, the gain and linearity link-budget will be described. For transmitter, since the input signals come from base band modulated signals which have enough power level, the noise figure issue will be omitted. The transmitter chain of each block is shown in Fig. 11. They are in sequence DAC, LPF,

Quadrature-Mixer, Preamp, BPF, PA (power amplifier), Switch of transmitting/receiving, and at last a channel-select BPF from right to left. And finally, the signals pass through a RF antenna for transmission.

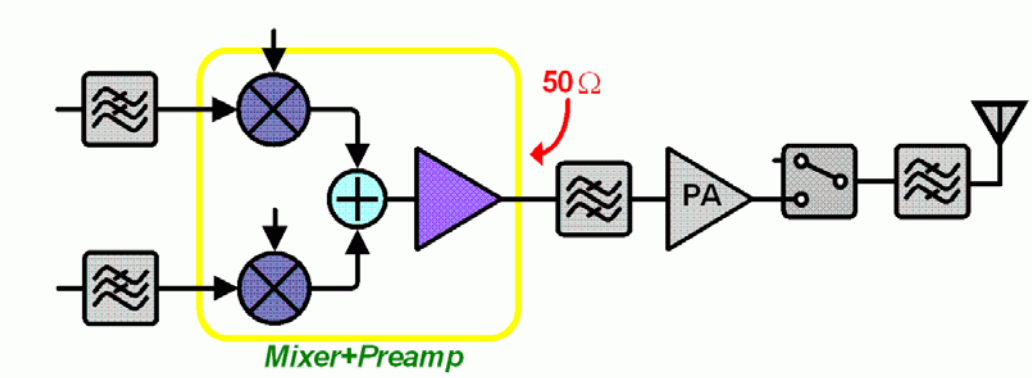


Fig. 11 Transmitter Architecture

3.3.1 802.11a/g

The IEEE 802.11a/g contains three sub-bands, and each band has different output power requirement. In this thesis, the lower band and middle band are the objective for 5 GHz design. For middle band design, the maximum output power with antenna gain is

$$200mW = 10 * \log(\frac{200mW}{1mW}) = 23dBm.$$

Subtracting from antenna gain of 6 dB, transmitter front-end average output power is

$$23dBm - 6dB = 17dBm.$$

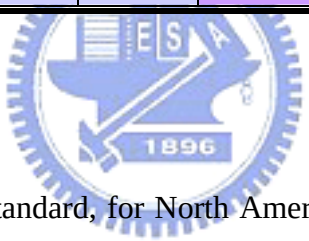
For OFDM modulation, an additional constraint of PAPR is demanded for 7 dB with 1dB design margin. Therefore, the transmitter front-end peak output power is

$$17dBm + 7dBm = 24dBm .$$

This value is required at the output of last BPF. A transmitter must be able to transmit this peak value rather be saturated. Therefore, the linearity of the transmitter front-end will be a “bottleneck” for our design. The system planning is shown as **TABLE 3**. The power amplifier gain was set to be 28 dB [10].

TABLE 3 802.11a/g System Planning

Parameters	BPF1	T/R	PA	BPF2	Mixer+Preamplifer	LPF	DAC	Unit
Pout,avg	17	19	21	-7	**-5**			dBm
Pout,peak	24	26	28	0	**2**	-5		dBm
Gain	-2	-2	28	-2	**7**	-5		dB
OP-1dB	infinite	infinite	28	Infinite	**2**	**-5**		dBm
OIP3	infinite	infinite	38.5	infinite	**12.5**			dBm



3.3.2 802.11b/g

As for IEEE 802.11b/g standard, for North American operation, the maximum output power is

$$1000mW = 10\log(\frac{1000mW}{1mW}) = 30dBm$$

Subtracting from antenna gain of 6 dB: transmitter front-end average output power:

$$30dBm - 6dB = 24dBm$$

Similarly, this value is required at the output of last BPF. The system planning is shown at **TABLE 4**. If the power amplifier gain is also set to be 28 dB, a very interesting conclusion was arose that the specification of transmitter front-end for 802.11a and 802.11b are the same except the operation band.

TABLE 4 802.11b/g System Planning

Parameters	BPF1	T/R	PA	BPF2	Mixer+Preamplifer	LPF	DAC	Unit
Pout	24	26	28	0	**2**	-5		dBm
Gain	-2	-2	28	-2	**7**	-5		dB
OP-1dB	infinite	infinite	28	infinite	**2**	-5		dBm
OIP3	infinite	infinite	38.5	infinite	**12.5**			dBm

3.3.3 Dual-Band Specification Summary

Based on the results of system planning for 802.11a and 802.11b from **TABLE 3** and **TABLE 4**, a dual-band transmitter front-end specification for 802.11 a/b/g standard was specified at **TABLE 5**.

TABLE 5 Dual-Band TX-FE Specification

Parameters	802.11a/b/g Specification
Frequency Range	2.4-2.4835GHz/5.15- 5.825GHz
Conversion Gain	7 dB
Input-P1dB	-5 dBm
Output P1dB	2 dBm
OIP3	12.5 dBm
RF Return Loss	<-15 dB
LO Return Loss	<-15 dB
Carrier suppression	<15 dBc

Chapter 4

Circuit Analysis

Each system block in RF front-end will be discussed in detail in this chapter, including mixer and preamplifier circuit design and analysis. At first, the trade-off between gain and linearity will be described using model of cascaded nonlinearity stages. Then the design procedure and circuit analysis for mixer and preamplifier will be introduced.

4.1 Transmitter Design Considerations

A transmitter front-end system composes of a mixer and pre-amplifier. Since the signals are processed by these cascaded stages, it is important to know how the nonlinearity of each stage is refereed to the input of the cascade. In particular, it is desirable to calculate an overall input third intercept point in terms of the IP3 and gain of the individual stages. Consider two or more nonlinear stages in cascade as shown in Fig. 12 [10]. If the input-output characteristics of each stages are expressed, respectively, as

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \quad (1)$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^2(t) + \beta_3 y_1^3(t) \quad (2)$$

$$\vdots$$

the input third intercept point can be derived as

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{\alpha_1^2}{A_{IP3,2}^2} + \frac{\alpha_1^2 \beta_1^2}{A_{IP3,3}^2} + \dots \quad (3)$$

where $A_{IP3,1}$ and $A_{IP3,2}$ represent the input IP3 of the first and second stages and so on. Interestingly, proper choice of the values and signs of the terms can yield an arbitrarily high IP3. In practice, however, since the base band signal is produced in the transmitter and hence is sufficiently strong, the noise of the mixer is not so critical here as in receivers, other considerations such as noise, gain, and active device characteristics may not permit this choice. Besides, if each stage in a cascade architecture has its gain greater than unity, the nonlinearity of the latter stages becomes increasingly critical because the IP3 of each stage is effectively scaled down by total gain preceding that stage. This formula is merely an approximation, since each stage in a cascade has a narrow frequency band in RF systems. Thus, the nonlinearity terms which fall out of the band are heavily attenuated, and then are omitted. In practice, more precise calculations or simulations must be performed to predict the overall IP3.

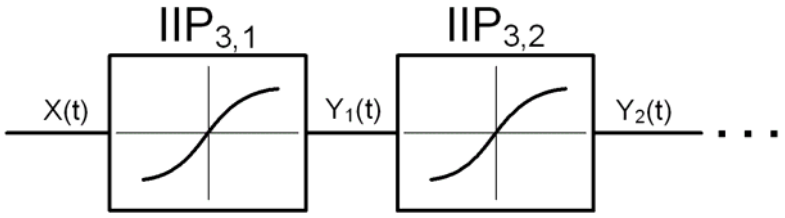


Fig. 12 Cascaded Nonlinearity Stages

4.2 Mixer Design

The main function for up-conversion mixers is to translate the BB frequency input signal into IF or RF band by multiplying LO frequency signal generated by local oscillator in the time domain. Multiplication thus results in output signals at the sum and difference frequencies of the input BB and LO signals. Theoretically, all devices with nonlinear characteristics can be mixers. The higher order terms of the characteristics offer the function of frequency translation.

4.2.1 Mixer Topology

Mixers can be mainly discriminated by passive mixers and active mixers by their gain performance. Active mixer generally provides some gain but passive not. Further, for passive mixers, the widely used topology is passive switching mixer as shown in Fig. 13. This mixer has the benefits of high linearity, no DC power consumption and easier implementation, but at the cost of higher requirement of LO power which is hard to reach for local oscillator. Besides, isolation is always a weakness to passive mixer, resulting in LO leakage problem described in chapter 2.

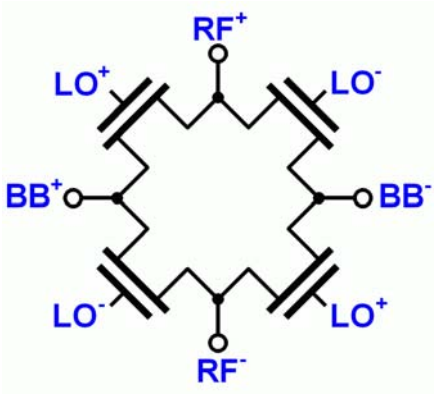
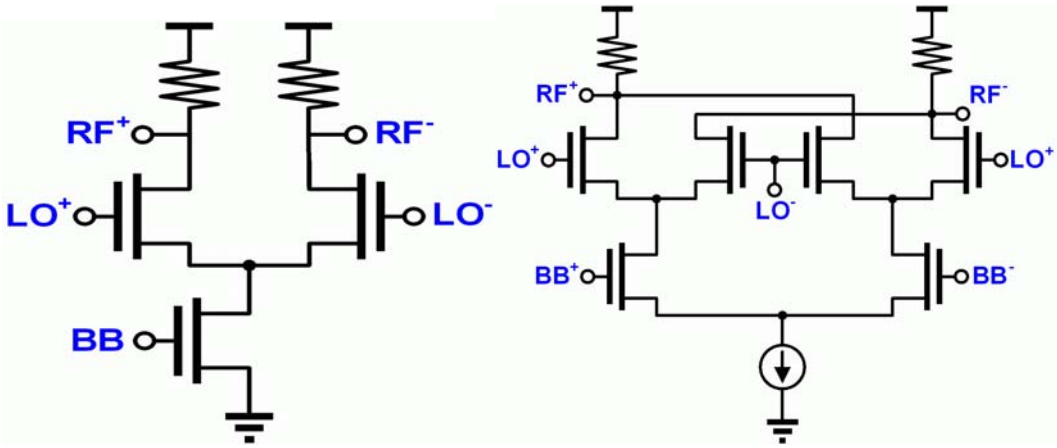


Fig. 13 Passive Mixer

For active mixers, two of the widely used topologies are single-balanced mixer and double-balanced mixer which are depicted in Fig. 14. Unlike passive mixers, these topologies would provide kind of gain and good isolation from LO to BB, although they would perform worse linearity, and power consumption. And most distinctness between single-balanced and double-balanced mixer is that the single-balanced mixer has still LO-RF feedthrough problem. This problem is more critical for direct-conversion architecture since the feedthrough term is located on desired RF band and would infringe the LO rejection constraint in both 802.11a/b specifications. Moreover, the double balance mixer has double conversion gain compared with the single balance mixer. So the double balance topology is chosen in our design. Detail analysis will be described in latter section.



(a) (b)

Fig. 14 (a) Single Balanced Mixer (b) Double Balanced Mixer

4.2.2 General Considerations

As shown in Fig. 15 is conventional double balance mixer which is also called "Gilbert cell" mixer. The operation can be divided into three stages: input gm-stage, switching-stage, and loading-stage. The gm-stage provides the transconductance that converts the input voltage into current domain. This stage also contributes most gain of an active mixer. Then, by switching the current signal in the switching-stage, nonlinearity effect will result in frequency translation. After the translation, current signals are again transformed to voltage domain by the loading-stage, and differentially output.

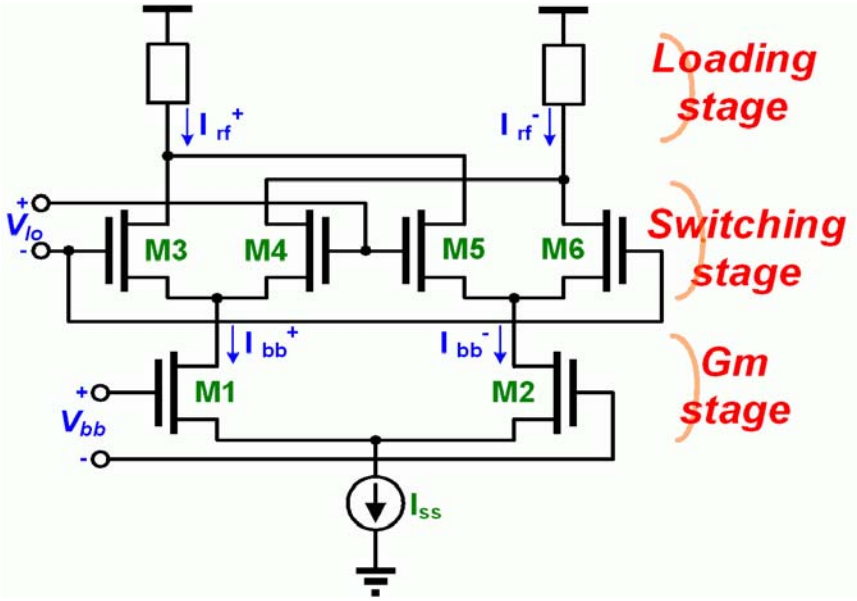


Fig. 15 Gilbert Cell Mixer

4.2.3 Conversion Gain

Since the switching level of the switching-stage in the mixer will enormously affect gain performance, here the analysis of conversion gain will be sorted by large and small LO amplitude [19].

a. For Large LO Amplitude

The operation of the switching-stage is a nonlinear function of V_{LO} expressed by $f(V_{LO})$. If we assume BB and LO signal are both sinusoid waveform which are expressed as $V_{LO}(t) = A_{LO}\cos\omega_{LO}t$ and $V_{BB}(t) = A_{BB}\cos\omega_{BB}t$. For assuming LO amplitude is large, $f(V_{LO})$ can be modeled by using the sgn function with a periodic function oscillating at ω_{LO} and which can be further expanded in a fourier series with fundamental frequency ω_{LO}:

$$f(V_{LO})=\frac{1}{2}+\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_{LO}t \tag{4}$$

as shown in Fig. 16. Therefore, we can derive the RF output signal is $V_{RF}(t)=V_{RF}^{+}(t)-V_{RF}^{-}(t)$, and in which $V_{RF}^{+}(t)$ and $V_{RF}^{-}(t)$ are the positive and negative port of the differential output. Furthermore,

$$V_{RF}^{+}(t)=\left\{\begin{array}{l} A_{BB}\cos_{BB}t\cdot g_m\cdot\left[\frac{1}{2}-\frac{2}{\pi}\cos\omega_{LO}t+\frac{2}{3\pi}\cos 3\omega_{LO}t-\ldots\right] \\ +(-1)\cdot A_{BB}\cos_{BB}t\cdot g_m\cdot\left[\frac{1}{2}+\frac{2}{\pi}\cos\omega_{LO}t-\frac{2}{3\pi}\cos 3\omega_{LO}t+\ldots\right] \end{array}\right\}\cdot R_L$$

$$=(-1)\cdot A_{BB}\cos_{BB}t\cdot g_m\cdot 2\left(\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_{LO}t\right)\cdot R_L \tag{5}$$

, and similarly,

$$V_{RF}^{-}(t)=A_{BB}\cos_{BB}t\cdot g_m\cdot 2\left(\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_{LO}t\right)\cdot R_L .$$

So

$$V_{RF}(t)=V_{RF}^{+}(t)-V_{RF}^{-}(t)=(-1)\cdot A_{BB}\cos_{BB}t\cdot g_m\cdot 4\left(\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_{LO}t\right)\cdot R_L \tag{6}$$

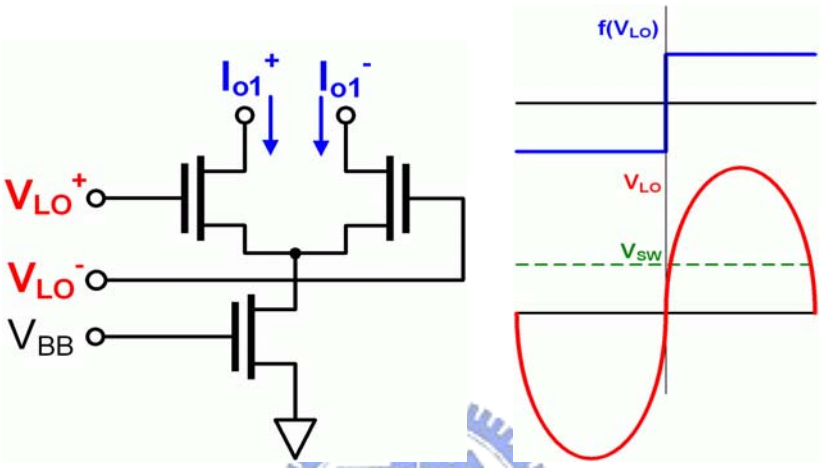
, and then with trigonometric expansion, this term further becomes

$$V_{RF}(t)=(-1)A_{BB}g_m 4R_L\frac{1}{\pi}\left[\cos(\omega_{BB}+\omega_{LO})+\cos(\omega_{BB}-\omega_{LO})\right] \tag{7}$$

of the fundamental term. For the upper side band mixing, after dividing by $V_{BB}(t)$, we get the conversion gain of

$$G_c = \frac{4}{\pi} g_m R_L \tag{8}$$

From (8) that in order to achieve high conversion gain, the only way is to increase the transconductance of the gm-stage and loading R_L. Furthermore, one thing important appears that G_c is independent of A_{LO}.



(a) (b)

Fig. 16 (a) Single Balance Mixer (b) Function of Switching Pair for Large LO

Besides, from (6), we can see that $V_{RF}(t)$ does not include any term from BB or LO. Ideally, the LO-to-BB and LO-to-RF isolation is infinite for double balance mixer. But process variation will induce gain and phase mismatch around switch stage. Therefore, carefully layout and symmetry board design still dominate isolation performance.

b. For Small LO Amplitude

Now, let us assume LO amplitude is small which is between V+ and V- and

$$f\left(V_{LO}(t)\right) = \frac{V_{LO} - V_-}{V_+ - V_-}.$$

To simplify our discussion, let us for the present case set V^+=1 and V^-=0 as shown in

Fig. 17, and then $f(V_{LO}(t)) = V_{LO}(t) = A_{LO}\cos\omega_{LO}t$. The derive of $V_{\mathrm{RF}}^{+}(t)$ is now easier which becomes

$$V_{\mathrm{RF}}^{+}(t) = \left\{ \begin{array}{l} \left[A_{BB}\cos_{BB} t \cdot g_m \cdot (-1) \cdot A_{LO}\cos\omega_{LO}t \right] \\ +\left[(-1) \cdot A_{BB}\cos_{BB} t \cdot g_m \cdot A_{LO}\cos\omega_{LO}t \right] \end{array} \right\} \cdot R_L$$

$$= (-1) \cdot A_{BB}\cos_{BB} t \cdot g_m \cdot 2 \cdot A_{LO}\cos\omega_{LO}t \cdot R_L ,$$

and similarly,

$$V_{\mathrm{RF}}^{-}(t) = A_{BB}\cos_{BB} t \cdot g_m \cdot 2 \cdot A_{LO}\cos\omega_{LO}t \cdot R_L ,$$

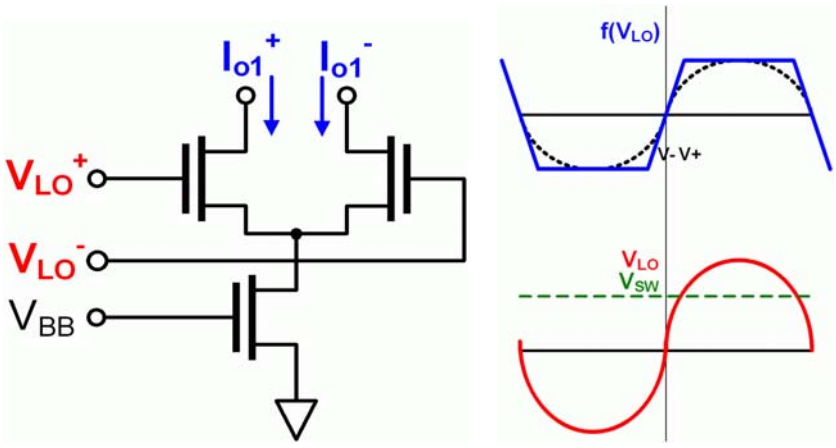
$$V_{RF}(t) = V_{RF}^{+}(t) - V_{RF}^{-}(t) = (-1)A_{BB}\cos_{BB} t \cdot g_m \cdot 4 \cdot A_{LO}\cos\omega_{LO}t \cdot R_L .$$

Now the equation can be expanded again into

$$V_{RF}(t) = (-1)A_{BB}A_{LO}g_m 2R_L\left[\cos(\omega_{BB} + \omega_{LO}) + \cos(\omega_{BB} - \omega_{LO})\right] \quad (9)$$

And the conversion gain is

$$G_c = 2A_{LO}g_m R_L \quad (10)$$



(a) (b)

Fig. 17 (a) Single Balance Mixer (b) Function of Switching Pair for Small LO

Referring to (10), however, that G_c is proportional to A_{LO}, which is not acceptable for our design. Since $V_{LO}(t)$ is usually generated from some frequency synthesizer,

and its exact amplitude is hard to control, leading to a G_c that is hard to control. As a result, the switching-stage has been designed to operate at border between large and small LO amplitude. Operating at this border will gain a G_c independent of A_{LO} with requiring less LO amplitude. As we know that, for a differential pair, the completely switching voltage is

$$V_{sw} = \sqrt{\frac{2I_s}{\mu C_{ox}\left(\frac{W}{L}\right)}} = \sqrt{2}V_{ov}\,. \tag{11}$$

To decrease the requirement of LO amplitude of switching-stage, we must have over-drive voltage of switching-stage as small as possible [17]. And from (11), device ratio must be as large as possible leaving the trade-off between conversion gain and LO amplitude requirement by modulating I_s value.

4.2.4 Linearity

This section focuses on another important performance for transmitter, which is linearity. First, we assume the switching-stage operates at large enough LO amplitude and consequently do not contribute distortion. Therefore, distortion comes primarily from the input V-I conversion: gm-stage, and also assume that this distortion is dominated by nonlinear square law I-V characteristics of the MOS transistors biased in saturation.

Referring to the source-couple pair (SCP) $M_{1\text{-}2}$ in Fig. 15, from the square law

[18], we know that

$$I_{bb}^{+}=\frac{k}{2}(V_{gs_1}-V_t)^2,\quad k=\mu_0 c_{ox}\frac{W}{L}. \tag{12}$$

Since the source of the SCP is common node that

$$V_{bb}^{+}-V_{gs_1}=V_{bb}^{-}-V_{gs_2}\Rightarrow V_{gs_1}=V_{bb}^{+}-V_{bb}^{-}+V_{gs_2}=V_{bb}+V_{gs_2}. \tag{13}$$

Substituting (13) into (12), we obtain

$$I_{bb}^{+}=\frac{k}{2}(V_{bb}+V_{gs_2}-V_t)^2 \tag{14}$$

Similarly,

$$I_{bb}^{-}=\frac{k}{2}(V_{gs_2}-V_t)^2\Rightarrow V_{gs_2}-V_t=\sqrt{\frac{2I_{bb}^{-}}{k}} \tag{15}$$

Again substituting (15) into (14), we get

$$I_{bb}^{+}=\frac{k}{2}\left(V_{bb}+\sqrt{\frac{2\left(I_{SS}-I_{bb}^{+}\right)}{k}}\right)^2. \tag{16}$$

After normalizing by $I_{bb_n}^{+}=\frac{2I_{bb}^{+}}{k}$ and $I_{SS_n}=\frac{2I_{SS}}{k}$, (16) is changed to

$$\sqrt{I_{bb_n}^{+}}=\left(V_{bb}+\sqrt{I_{SS_n}-I_{bb_n}^{+}}\right). \tag{17}$$

That is

$$V_{bb}=\sqrt{I_{bb_n}^{+}}-\sqrt{I_{SS_n}-I_{bb_n}^{+}}=\sqrt{\frac{I_{SS_n}}{2}+i_{bb_n}^{+}}-\sqrt{\frac{I_{SS_n}}{2}-i_{bb_n}^{+}}, \tag{18}$$

where $i_{bb_n}^{+}$ is the small signal part of $I_{bb_n}^{+}$. And then factoring out the I_{SS_n}, we get

$$V_{bb}=\sqrt{\frac{I_{SS_n}}{2}}\left(\sqrt{1+\frac{2i_{bb_n}^{+}}{I_{SS_n}}}-\sqrt{1-\frac{2i_{bb_n}^{+}}{I_{SS_n}}}\right), \tag{19}$$

which (19) gives V_{bb} in terms of $i_{bb_n}^{+}$. The square root terms in (19) can be expanded

around $\frac{2i_{bb_n}^{+}}{I_{SS_n}}$ and we have

$$V_{bb} = \sqrt{\frac{I_{SS_n}}{2}} \left[\begin{array}{l} (1 + \frac{1}{2}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right) - \frac{1}{8}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right)^2 + \frac{1}{16}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right)^3 + \ldots) \\ -(1 - \frac{1}{2}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right) + \frac{1}{8}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right)^2 + \frac{1}{16}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right)^3 + \ldots) \end{array} \right] \tag{20}$$

$$= \sqrt{\frac{I_{SS_n}}{2}} \left[\frac{2i_{bb_n}^{+}}{I_{SS_n}} + \frac{1}{8}\left(\frac{2i_{bb_n}^{+}}{I_{SS_n}}\right)^2 + \ldots \right] \tag{21}$$

Since V_{bb} is input and $i_{bb_n}^{+}$ is output, each $i_{bb_n}^{+}$ term can also be expanded as a Taylor series in power of V_{bb}. That is

$$i_{bb_n}^{+} = a_1 V_{bb} + a_2 V_{bb}^2 + a_3 V_{bb}^3 + \ldots \tag{22}$$

Substituting each $i_{bb_n}^{+}$ term in (21) using (22), we have

$$V_{bb} = \sqrt{\frac{I_{SS_n}}{2}} \left[\begin{array}{l} \frac{2}{I_{SS_n}}\left(a_1 V_{bb} + a_2 V_{bb}^2 + a_3 V_{bb}^3 + \ldots\right) + \\ \frac{1}{8}\left(\frac{2}{I_{SS_n}}\right)^2 \left(a_1 V_{bb} + a_2 V_{bb}^2 + a_3 V_{bb}^3 + \ldots\right)^2 + \ldots \end{array} \right] \tag{23}$$

Finally, we can solve for the coefficients $a_1, a_2, a_3, \ldots$ by equating the coefficients of $V_{bb}, V_{bb}^2, \ldots$ on both sides of (23).

For the V_{bb} term,

$$1 = \sqrt{\frac{I_{SS_n}}{2}}\left(\frac{2}{I_{SS_n}} a_1\right) \Rightarrow a_1 = \sqrt{\frac{I_{SS_n}}{2}}\,. \tag{24}$$

For the V_{bb}^2 term,

$$0 = \sqrt{\frac{I_{SS_n}}{2}}\left(\frac{2}{I_{SS_n}} a_2\right) \Rightarrow a_2 = 0\,. \tag{25}$$

For the V_{bb}^3 term,

$$0 = \sqrt{\frac{I_{SS_n}}{2}}\left(\frac{2}{I_{SS_n}}a_3 + \frac{1}{8}\left(\frac{2}{I_{SS_n}}\right)^3 a_1^3\right) => a_3 = -\frac{1}{8}\left(\frac{2}{I_{SS_n}}\right)^2 a_1^3. \quad (26)$$

And as we know that, $IM_3 = \frac{3}{4}\frac{a_3}{a_1}A_{bb}^2$ [10], then substituting by (24) and (26), we get $IM_3 = \frac{3}{16}\frac{1}{I_{SS_n}}A_{bb}^2 = \frac{3}{16}\frac{k}{2I_{SS}}A_{bb}^2 = \frac{3}{32}\frac{k}{I_{SS}}A_{bb}^2$ (27)

, for which $k = \mu_0 c_{ox}\frac{W}{L}$ and (27) can be wrote as

$$IM_3 = \frac{3}{32}\frac{\mu C_{ox}\frac{W_1}{L_1}}{I_{SS}}A_{bb}^2. \quad (28)$$

And then

$$A_{IP_3}^2 = \frac{32}{3}\frac{2I_{D1}}{\mu_0 C_{ox}\frac{W_1}{L_1}} \quad (29)$$

In order to mitigate the nonlinearity effect due to interferences, that is low IM_3 and high A_{IP_3} are desired. Referring to (28) and (29), we observe that high I_{ss} is unavoidable and I_{D1} as well, while the $\frac{W_1}{L_1}$ ratio must be kept low. But high I_{ss} will burn more power consumption, and low $\frac{W_1}{L_1}$ will decrease the main source of conversion gain, leaving a trade-off between power consumption, linearity, and conversion gain to design a mixer.

If V_{bb} is small, then the current flowing through M1 can be assumed to be equal to that through M2, or half of I_{SS}. Then (29) can be rewrote as

$$A_{IP_3}^2 = \frac{32}{3}\frac{2I_{D1}}{\mu_0 C_{ox}\frac{W_1}{L_1}} = \frac{32}{3}\frac{2\frac{1}{2}\mu_0 C_{ox}\frac{W_1}{L_1}(V_{GS_1}-V_t)^2}{\mu_0 C_{ox}\frac{W_1}{L_1}} = \frac{32}{3}(V_{GS1}-V_t)^2 \quad (30)$$

, and

$$A_{IP_3} = 4\sqrt{\frac{2}{3}}\left(V_{GS_1}-V_t\right). \quad (31)$$

From (31), we also see that, a high over-drive voltage (V_{ov}) of the input gm-stage is desired to achieve higher linearity.

4.3 Pre-amplifier design

In the transmitter design, a power amplifier (PA) is followed by the up-conversion mixer to provide the required output power to a 50-Ω antenna. For most of Wireless LAN applications, a PA circuit must be able to achieve 25-30dBm output power. In order to deliver required output power to a 50-Ω antenna at lower supply voltages, a matching network can be interposed between the PA and the load. The matching network transforms R_L to a smaller value such that the limited voltage swing provided by the PA can still deliver the required output power. The enormous currents in the output device and the matching network are one of the difficulties in the design of power amplifiers and especially the package. Besides, a series resistance of a few tens of milliohms in the transistor, and the “radio-frequency choke” (RFC), or the matching network may result in a considerable loss, therefore, a precise modeling of transistors or even package is indispensable for PA designer.

In practice, PA design has involved a substantial amount of trial and error, and an additional power supply voltage will be required to obtain the high power gain.

Due to these reasons, a discrete and off-chip implementation of PA is chosen in our transmitter design. Instead, following the up-conversion mixer is a power amplifier driver (Pre-amplifier). This preamplifier stage will be design as the same way of designing a power amplifier, but the power gain constraint is released here. As described in chapter 3, an off-chip PA with power gain of 20~28dB is required for system specification, and the total gain of mixer with adding preamplifier stage is set to be 7~15dB [10].

4.3.1 General Considerations

Generally, in the field of communication, we can distinguish signals into two parts: amplitude and phase. As a result, power amplifier can also be divided into two categories: one is linear operation and another is constant-envelope operation [21]. The transistor in linear operation acts as a current source and the RF output power is proportional to the RF input power. The transistor “on” voltage does not saturate. Otherwise, the transistor in constant-envelope operation operates as a switch. The linear operation includes class-A,B,C,AB type power amplifier, and which is suitable for linear amplitude modulation, while the constant-envelope operation includes class-D,E,F type power amplifier, and which is suitable for phase

modulation. Roughly speaking, the linear operation has high linearity but poor efficiency. However, the constant-envelope operation has excellent efficiency.

The need for linear power amplifiers arises in many RF applications, especially, for multi-carrier systems, for example, in this thesis, OFDM application in 802.11a/g standard. Since amplifiers simultaneously process many channels, it needs to be linear enough to avoid cross modulation. The nonlinearity of PAs is usually characterized by a two-tone test. For adjacent channel interference, the third-order IM components are important.

At present, most linear PAs designed for portable devices employ a class A output stage and exhibit efficiencies around 30% to 40%.

4.3.2 Loading Line Theorem

As we know that, a small signal amplifier adopts conjugate matching to obtain maximum output power as shown in Fig. 18, where $R_L=R_o$. However, as signal power increases, the output power will be less than expected due to the limit of current or voltage driving capability.

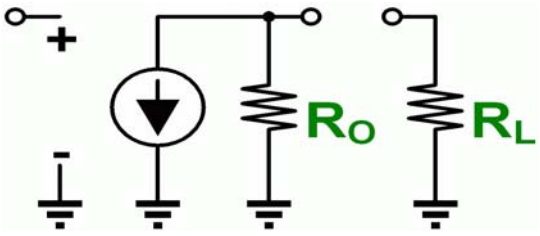


Fig. 18 Output Impedance with Linear Resistance Model

Therefore, different from the design of small signal amplifier, a power

amplifier is biased at the middle of maximum output swing of current and voltage as shown in Fig. 19. Besides, by properly choosing R_{load}, the signal will have maximum swing under the limit of current and voltage. And the maximum output power is larger than that by conjugate matching.

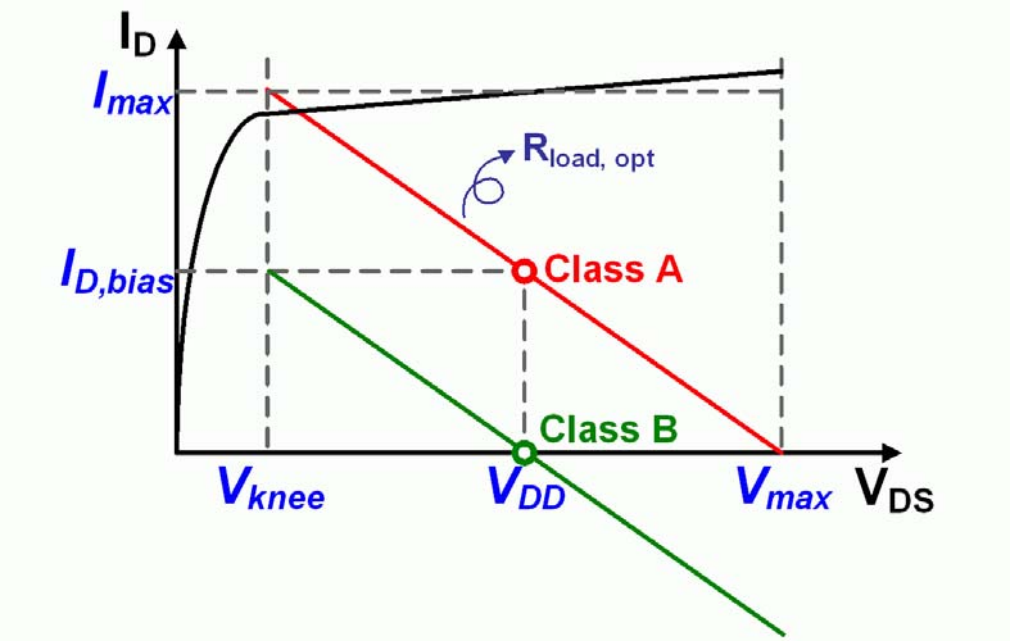


Fig. 19 PA Bias Condition and Loading Line

We will introduce two extreme kinds of power amplifiers: class A and class B [20]. Class A has excellent linearity but poor efficiency, while class B has better efficiency but worse linearity.

a. Class A PA

The bias point for class A PA is depicted in Fig. 19. At first, the optimum R_{load} is decided by

$$R_{opt} = \frac{V_{\max} - V_{knee}}{I_{\max}} \tag{32}$$

We have

$$V_{rms} = \frac{(V_{\max} - V_{\min})}{2\sqrt{2}}, \quad I_{rms} = \frac{(I_{\max} - I_{\min})}{2\sqrt{2}} \tag{33}$$

and

$$V_{DC} = \frac{(V_{\max} + V_{\min})}{2}, \quad I_{DC} = \frac{(I_{\max} + I_{\min})}{2}. \tag{34}$$

The output power can be expressed as:

$$P_{out} = V_{rms} I_{rms} = \frac{(V_{\max} - V_{\min})}{2\sqrt{2}} \frac{(I_{\max} - I_{\min})}{2\sqrt{2}} = \frac{(V_{\max} - V_{\min})(I_{\max} - I_{\min})}{8} \tag{35}$$

The dc power consumption is also shown as:

$$P_{DC} = V_{DC} I_{DC} = \frac{(V_{\max} + V_{\min})}{2} \frac{(I_{\max} + I_{\min})}{2} = \frac{(V_{\max} + V_{\min})(I_{\max} + I_{\min})}{4} \tag{36}$$

From (35) and (36), and by definition that the drain efficiency of a class A PA is:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\frac{(V_{\max} - V_{\min})(I_{\max} - I_{\min})}{8}}{\frac{(V_{\max} + V_{\min})(I_{\max} + I_{\min})}{4}} \leq 50\% \tag{37}$$

Ideally, for $V_{min}=I_{min}=0$, the efficiency of a class A PA is 50%. In fact, since the device's characteristic such as breakdown voltage and knee voltage are not equal to 0, the efficiency is always less than 50%.

b. Class B PA

As for class B PA, it conducts half a cycle, and the drain current is severely clipped which would induce serious nonlinearity and result in worse linearity than class A PA. The only difference from class A PA is dc current as:

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} \mathrm{I}_{\max} \left|\sin\theta\right| d\theta = \frac{\mathrm{I}_{\max}}{\pi}. \tag{38}$$

And the dc power consumption is expressed as:

$$P_{DC} = V_{DC} I_{DC} = \frac{(V_{\max} + V_{\min})}{2} \frac{I_{\max}}{\pi} = \frac{I_{\max}(V_{\max} + V_{\min})}{2\pi}. \tag{39}$$

The drain efficiency of a class B PA is

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\pi}{4} \frac{(V_{\max} - V_{\min})}{(V_{\max} + V_{\min})} < \frac{\pi}{4} \approx 0.785. \tag{40}$$

It can be seen from (40) that class B PA has a maximum efficiency of around 78 percent which is superior to class A PA.

4.3.3 Two-Stage Configuration

Most power amplifiers employ a two-stage configuration, with matching networks placed at the input, between the two stages, and at the output as shown in Fig. 20. Since the output stage typically exhibits a power gain of less than 10 dB, a high-gain driver is added so as to lower the minimum required input level. The input and output matching networks in Fig. 20 serve different purposes: N_1 provides a 50-Ω input impedance, while N_3 amplifies the voltage swings produced by the output stage so as to deliver the required power to R_L. In our transmitter system, since the up-conversion mixer and preamplifier are implemented on a single chip, the first matching network for 50-Ω input matching can be removed. As for N2, it provides desired load and source impedance simultaneously for driver stage and output stage and hence simplifies the design procedure.

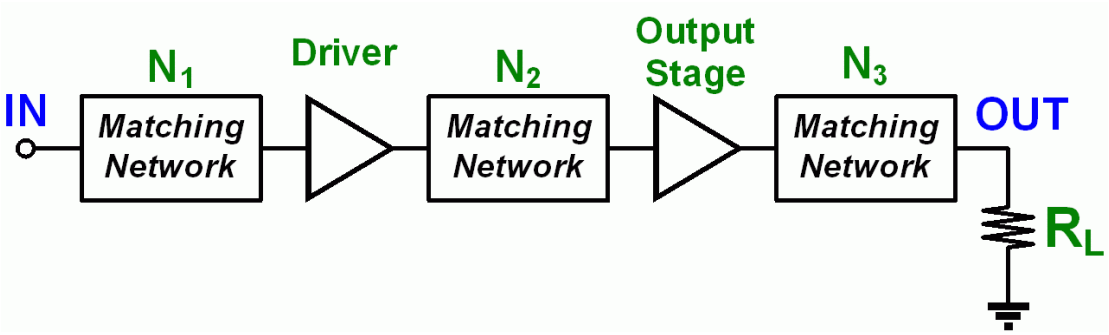


Fig. 20 Two Stage Configuration

Chapter 5

Circuit Implementation

According to the specification expressed in **TABLE 5**, a mixer must perform high 1dB compression point. As we know that I/V transfer characteristic of the gm-stage dominates the linearity of a mixer. There are several circuit techniques for improving the linearity of MOS transconductance elements. In this chapter, two 5GHz transmitter front-end utilizing two of the techniques will be introduced and implemented. One is to degenerate the source-coupled pair by a MOS transistor operating in the triode region [22] which is designed for higher linearity, whereas another is to simply add two auxiliary cross-coupled differential pairs to the source-coupled pair [23], [24], meanwhile, with the on-chip differential-to-single circuit, this transmitter front-end has better power consumption and is designed for low power application. And finally, a novel structure of mixer-reuse dual-band transmitter front-end will be proposed. Simulation results also have been listed after each circuit.

5.1 5GHz TX-FE for High Linearity Design

The differential topology is employed throughout this transmitter front-end circuit to minimize the undesired coupling, especially the local oscillator leakage though the mixers to the antenna as it causes the dc offset to corrupt the desired low-frequency signals at receiver.

The circuit block is depicted in Fig. 21. The direct-conversion architecture was adopted. Two mixers were employed to up-converse the base band I/Q signals respectively with quadrature local oscillator signals. The RF quadrature signals are then summed up and output to the differential preamplifier.

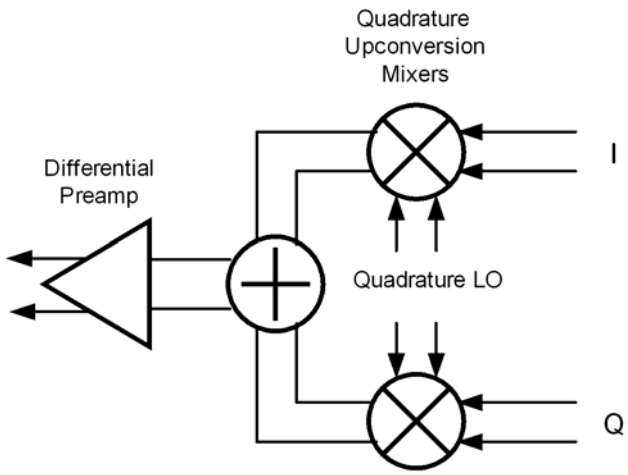


Fig. 21 5GHz TXFE for High Linearity Circuit Block

5.1.1 Mixer Design

Fig. 22 is the illustration of the first linearization technique. Transistors M1 and M1' form the input differential pair while M3 and M3' provide the bias current, and the transfer characteristic of which is linearized by the voltage-controlled

degeneration “resistors” M2 and M2’.

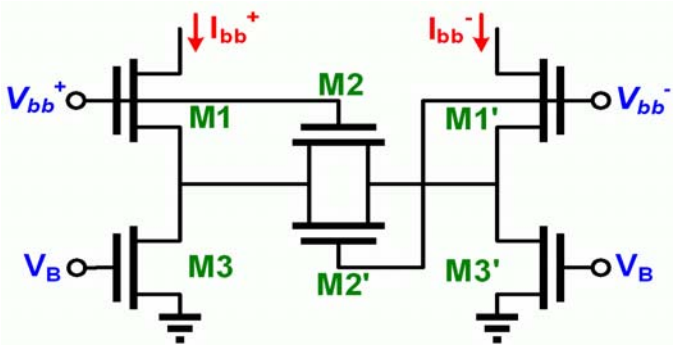


Fig. 22 Gm-stage using Triode-Region MOS Degeneration

In order to get a qualitative understanding of the behavior of this new input stage, the circuit is first analyzed using the simple square-law MOSFET. For convenience, the following parameters are introduced [25]:

$$a = 1 + \frac{\beta_1}{4\beta_2} \tag{41}$$

and

$$g_{m0} = \frac{\partial I_{out}}{\partial V_{in}}|_{@V_{in}=0} = \frac{I_{bias}}{a(V_{GS} - V_T)_{M1}} \tag{42}$$

where $\beta = \mu_0 c_{ox} \frac{W}{L}$. For low values of the input voltage V_{in}, transistors M2 and M2’ are operated in triode region and we can get another normalized transfer characteristic as followed:

$$i = v\sqrt{1 - \frac{v^2}{4}} \tag{43}$$

, where $v = g_{m0} \frac{V_{in}}{I_{bias}}$ and $i = \frac{I_{out}}{I_{bias}}$. An interesting conclusion comes out that within a limited input voltage range the transfer characteristic of the input gm-stage is similar to that of a conventional source-coupled pair which is biased at an overdrive voltage of $a(V_{GS} - V_T)_{M1}$. However, when the swing of input signal voltage

increases, M2' would eventually enter the saturation region, whereas M2 stays in the triode region because $V_{GS,M2}$ is increasing but $V_{GS,M2'}$ is decreasing. In this way, the equivalent degeneration resistance may not have distinct change, and the gm characteristic would maintain constant for wider input range. The simulation result of gm transfer characteristic is shown in Fig. 23 and the ripple in the gm curve can be reduced by lowering the quiescent gate overdrive voltage V_{GS}-V_T of the transistors.

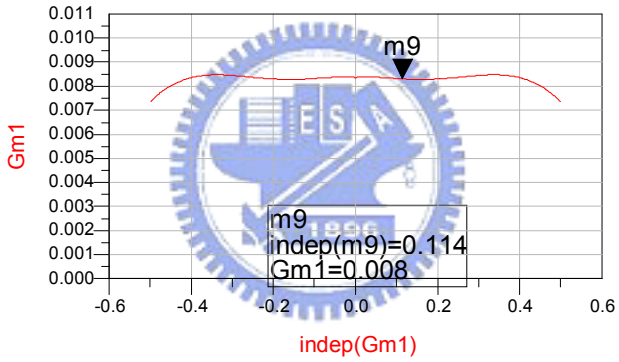


Fig. 23 Gm-stage Transfer Characteristic

If the input common-mode voltage is not constant with respect to the bulk potential, even-order terms will appear in the v/i transfer characteristic. These distortions may be minimized by increasing the bulk reverse voltage to reduce the body effect. Furthermore, for a purely differential mode input signal, the remaining even-order distortions would result from device mismatch, which has to be minimized by appropriate layout disposition. Besides, for transistors operating more

deeply in strong inversion, the optimum ratio β_1 / β_2 is slightly larger than 6. On the contrary, that "hump" tends to disappear at lower current densities where the optimum β_1 / β_2 is smaller than 6.

When the ratio β_1 / β_2 has been decided, referring to (29), in order to achieve high IP3, the bias current I_D must be large and input dimension ratio must be small. But high gain requires high transconductance indicating high I_D and W/L is desired which leaves a compromise between transconductance and linearity.

The I/Q quadrature Gilbert-type mixer is depicted in Fig. 24. The loading resistors have been replaced by inductors due to the finite voltage headroom issue. The inductors were designed to resonate the capacitance seen from output nodes of the mixer at frequency of 5.25GHz by

$$f = \frac{1}{2\pi\sqrt{LC}}. \tag{44}$$

A conjugate matching at the output loading will transfer the maximum output power to the next stage. No doubt that parasitic capacitance of the input of next stage will be taken into consideration in the simulation.

Referring to the discussion in section 4.2.3, in order to perform more ideal switch feature, and achieve higher linearity and high conversion gain and also mitigate the requirement of LO amplitude, the switching-stage is designed to have as less as possible V_{ov}. From (11), the W/L of the switching-stage is required to be

large, and I_s is to be small. But large size of the transistor will induce considerable parasitic capacitance at the common drain of the switching-stage, which are either output nodes of mixer. The large capacitive characteristic would force to lower the loading inductance for output resonance. The loading impedance $Z_{load} = Q\omega L$ thus drops and then the gain of mixer drops in the same manner. Hence, leaving an optimum size of switching-stage for specified LO amplitude and bias current.

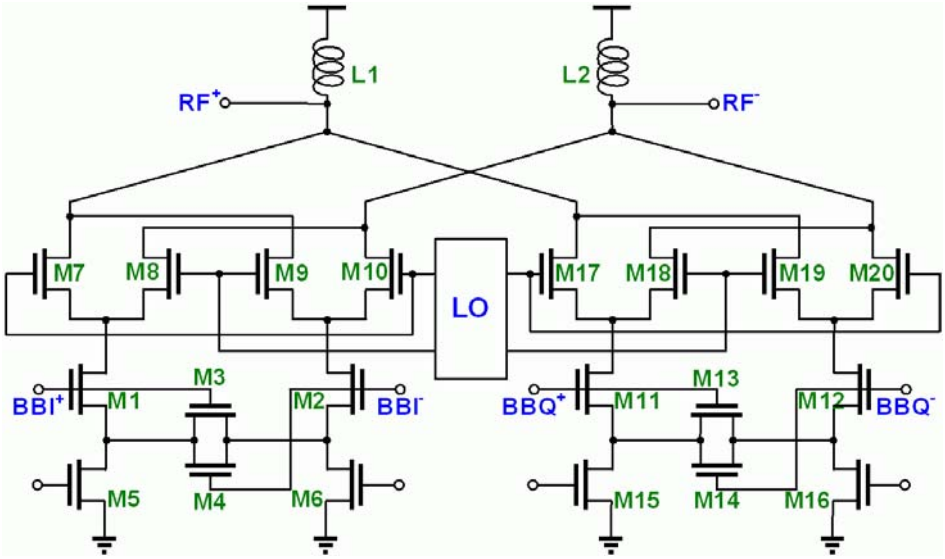


Fig. 24 Quadrature Gilbert-Type Mixer

5.1.2 Preamplifier Design

The differential outputs RF+ and RF- of the mixer then couple to the preamplifier with two series ac couple capacitors. In this way, the DC offset issue comes from self-mixing of mixer can be eliminated. The preamplifier employs two-stage configuration we described before, and of course, adopts fully-differential topology. The circuit is depicted in Fig. 25. The first stage is a common-source

amplifier which provides adequate power gain to RF signal for driving an off-chip PA while the last stage is a source-follow amplifier which plays a role of an output buffer to increase isolation and also provides 50Ω output matching.

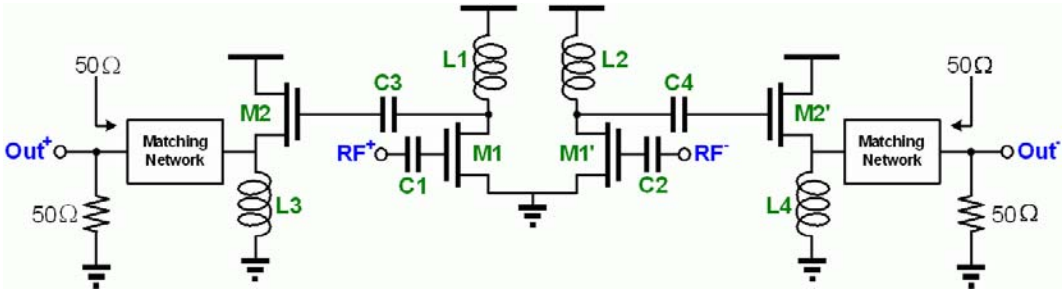


Fig. 25 Differential Preamplifier

The first stage of a balance source-couple pair adopts grounded-source to have better IM3 performance [26]. And the common-source amplifiers have been biased at class AB topology for the compromise between linearity and power efficiency. In order to achieve output power of more than 2dBm demanded in the specification and we also preserve 5dB for design margin. For VDD=1.8 and V_{knee}=0.7=Vmin, we have Vmax=2VDD=3.6V, and from (35)

$$P_{out} = 7.6dBm = 5.8mW = V_{rms} I_{rms} = \frac{(V_{\max} - V_{\min})(I_{\max} - I_{\min})}{8} \qquad (45)$$

, we get Imax is equal to around 16mA. Furthermore, from (32)

$$R_{opt} = \frac{V_{\max} - V_{knee}}{\mathrm{I}_{\max}} \qquad (46)$$

R_{opt} has been set to be 180Ω. The I-V curve simulation result is shown in Fig. 26. We choose inductors as loading to resonate the capacitance at drain of common-source amplifier resulting in real part impedance of about 180Ω. The source degeneration of source-follow amplifier also uses inductors to save some

voltage headroom. One must be concerned is that the bias current of the source-follow amplifier has to be large enough to make the loss of this output buffer as less as possible.

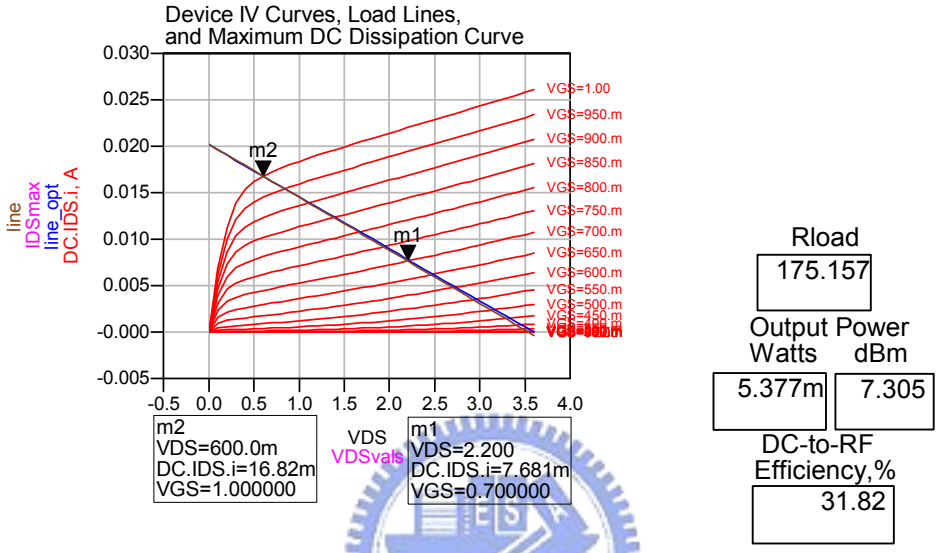


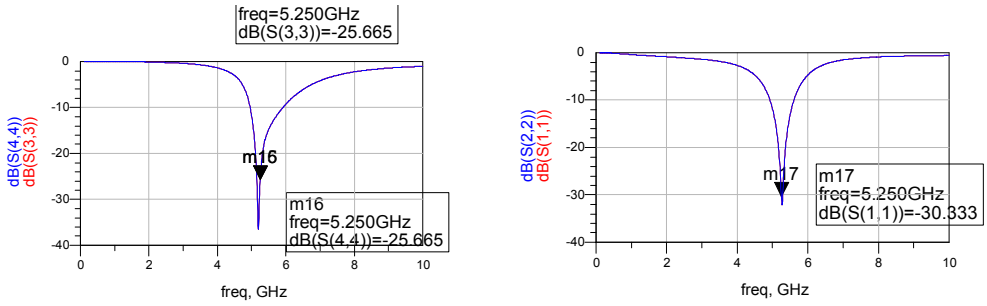
Fig. 26 I-V Curve Simulation of Class A PA

5.1.3 Simulation Results

In order to double-check this design, this circuit has been implemented for on-wafer testing and package testing, respectively. Besides, for convenient measurement, we both only observe the single output of the preamplifier with another port termination to $50\,\Omega$ during simulation and measurement.

a. On-Wafer Testing

At first, we must make sure RF output and LO matching which are depicted in Fig. 27. The return loss for RF output and LO are both more than 20dB.



(a) (b)

Fig. 27 (a) Output Return Loss (b) LO Return Loss

Then, as the discussion in 4.2.3, we have to find the adequate LO amplitude applying to switching-stage which is best located on the boundary of “linear” and “saturate” output power. The relation between LO power and output power has been illustrated in Fig. 28 with fixing input power of -7dBm. When LO power is small, output power is proportional to LO power, then output power maintains constant and is independent of LO power until LO power reaches -5dBm. Therefore, LO power has been set to be -5dBm for each simulation below.

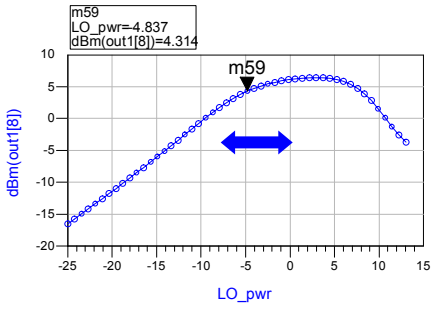


Fig. 28 LO Power vs. Output Power

Furthermore, we can see the frequency response of output power as LO frequency sweep from 3GHz to 7GHz with inputting a base band signal of -7dBm in

Fig. 29. This transmitter front-end (TXFE) obtains over 7dB power gain from 4.75GHz-5.65GHz of 900MHz bandwidth and has maximum output power at LO frequency of around 5.2GHz which also indicates that every resonator in mixer and preamplifier achieves conjugate matching at desired frequency of 5.2GHz.

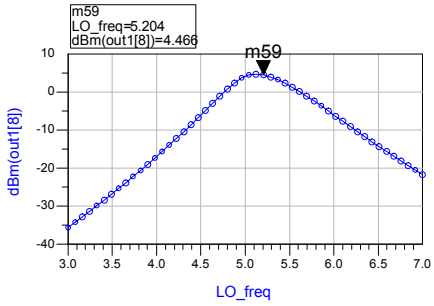
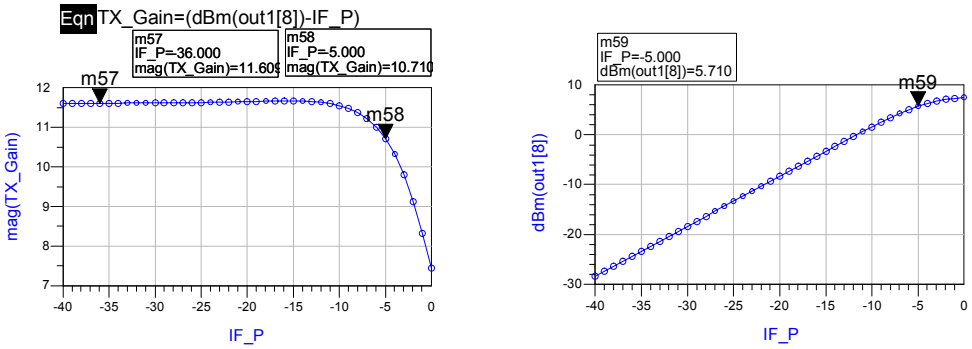


Fig. 29 LO Frequency vs. Output Power

When inputing a base band signal of 1MHz and -7dBm and LO signal of 5.25GHz and -5dBm, this TXFE has 11.6dB conversion gain and -5dBm input P1dB as shown in Fig. 30(a) while obtains the maximum output power of 5.7dBm for 1dB compression point as shown in Fig. 30(b).



(a) (b)

Fig. 30 (a) Input Power vs. Conversion Gain (b) Input Power vs. Output Power

Moreover, the spectrum depicted in Fig. 31 and Fig. 32 displays the harmonic

term of 5GHz signal and the adjacent band power, respectively. We have more than 37dB harmonic rejection and even non-existence of DC-offset and also 95dB LO suppression and 110dB side-band rejection.

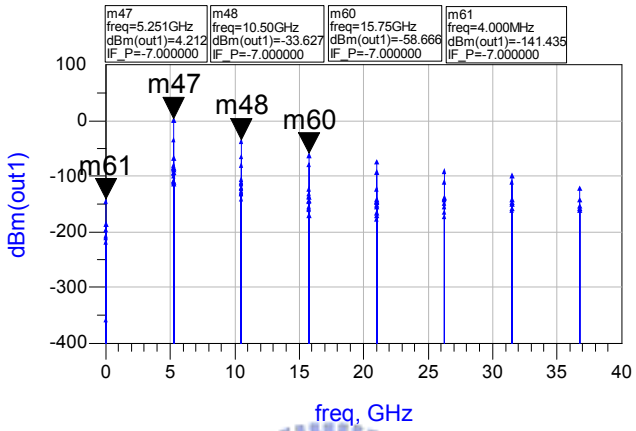


Fig. 31 Harmonic Term of 5GHz Output Signal

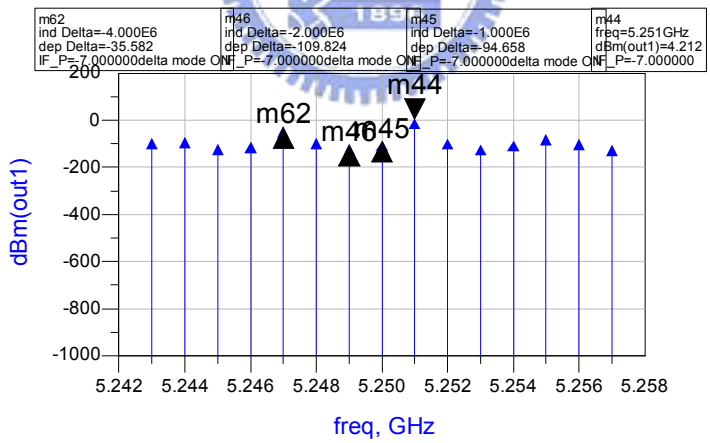
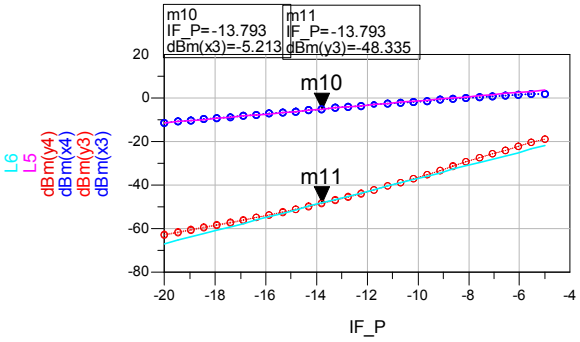


Fig. 32 LO Rejection and Side-Band Rejection

Finally, the IP3 is tested by inputting 6MHz and 7MHz base band signals simultaneously. The simulation is depicted in Fig. 33. The intersection point of the two extending straight lines indicates that this TXFE has input-IP3 of 7.8dBm and

output-IP3 of 16.3dBm.



IF_P	IIP3_dBm2	IIP3_mV2	OIP3_dBm2	OIP3_V2
-13.793	7.768	2.446	16.348	6.568

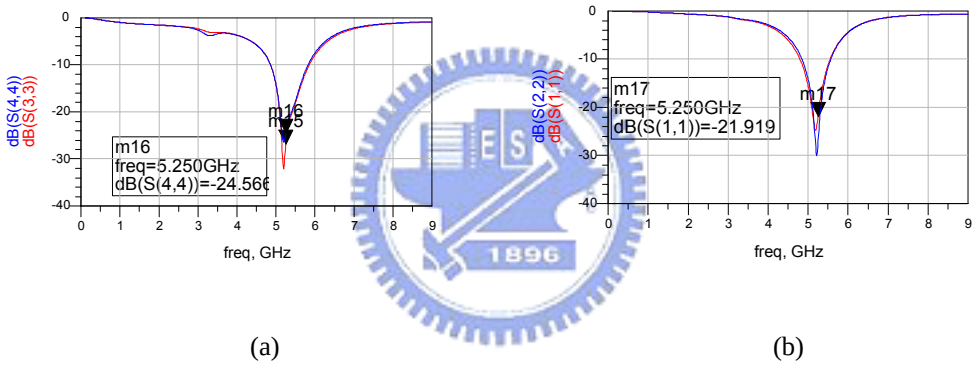
Fig. 33 IIP3 and OIP3

This on-wafer transmitter front-end consumes 40mA for 1.8V power supply.

b. Package Testing

As for the package version, the simulation results is shown in Fig. 34~ Fig. 40. The output and LO matching still have more than 20dB return loss. The LO power has been set to be -5dBm in every simulation for the same reason. The frequency response of output power indicates that this TXFE achieves more than 7dB gain from 4.7GHz~5.85GHz of 1150MHz bandwidth and has maximum output power at LO frequency of around 5.2GHz. For the same input signals, the TXFE for package version has better conversion gain of 13.88dB and the same input 1dB compression point of -5dBm and also achieve better maximum output power of 7.85dBm for 1dB

compression. However, due to the unbalance of package model around GND, VDD, and output nodes. This package version has worse harmonic rejection of 20dB and DC-offset suppression of 19dB and also worse LO suppression of 40dB and side-band rejection of 55dB than on-wafer version. Finally, for the two-tone test, with the same input signals, this TXFE has input-IP3 of 7dBm and output-IP3 of 17.3dBm which is close to the simulation of on-wafer version. This TXFE for package version consumes also 40mA for 1.8V power supply.



(a) (b)

Fig. 34 (a) Output Return Loss (b) LO Return Loss

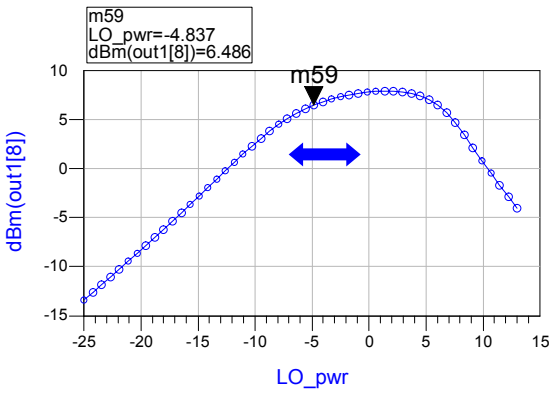


Fig. 35 LO Power vs. Output Power

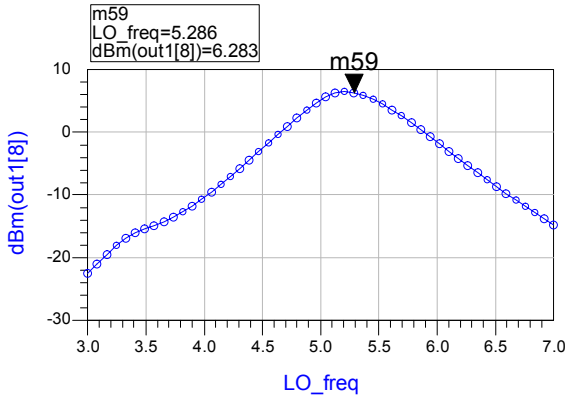
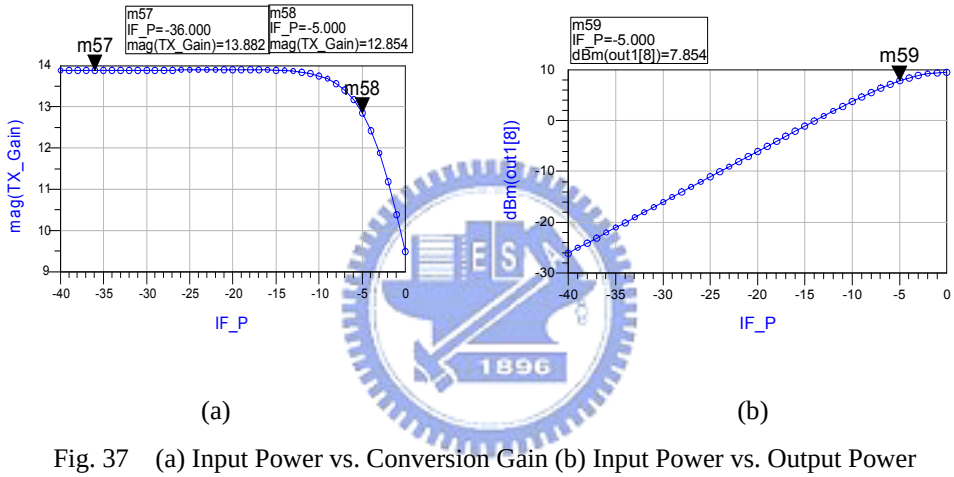


Fig. 36 LO Frequency vs. Output Power



(a) (b)

Fig. 37 (a) Input Power vs. Conversion Gain (b) Input Power vs. Output Power

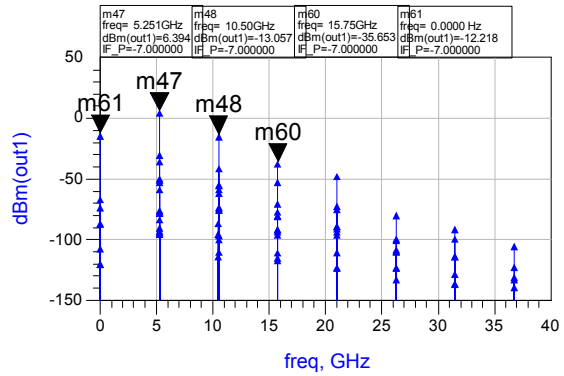


Fig. 38 Harmonic Term of 5GHz Output Signal

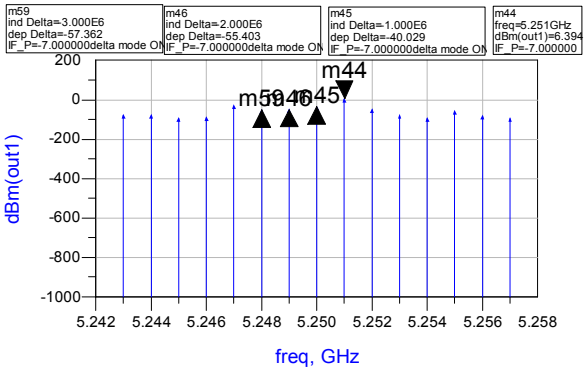
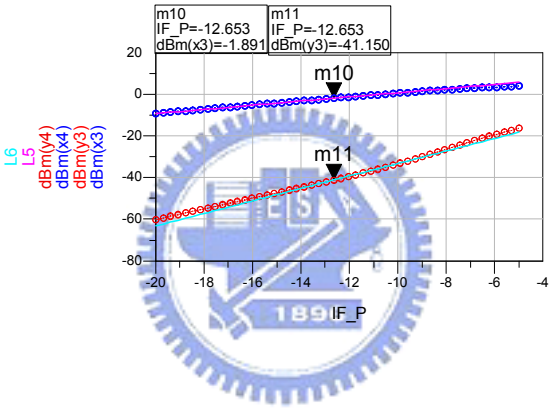


Fig. 39 LO Rejection and Side-Band Rejection



IF_P	IIP3_dBm2	IIP3_mV2	OIP3_dBm2	OIP3_V2
-12.653	6.977	2.233	17.739	7.708

Fig. 40 IIP3 and OIP3

5.1.4 Discussions

The simulation results will be listed in detail in section 5.3. Each performance in the on-wafer version and package version could meet the specification described in **TABLE 5**. The only shortage of this TXFE is that, due to the differential topology from mixer to preamplifier, an additional differential-to-single circuit must be

required off-chip, and the current dissipation is double for twice of signal paths. These two drawbacks will disobey the objective of SOC. Therefore, the second edition 5GHz circuit has been implemented as followed.

5.2 5GHz TX-FE for Low Power Design

In order to improve current dissipation and chip area, and also achieve the objective of “SOC”. We have implemented another transmitter front-end with an on-chip differential-to-single (D/S) circuit [7]. Moreover, we adopted another structure of gm-stage in mixer circuit. The circuit block is illustrated in Fig. 41. The D/S circuit converts differential outputs of mixer into single-ended. Thus, only single-end preamplifier is required resulting in current dissipation and area saving. The off-chip power amplifier is to be used for saving the overall system power.

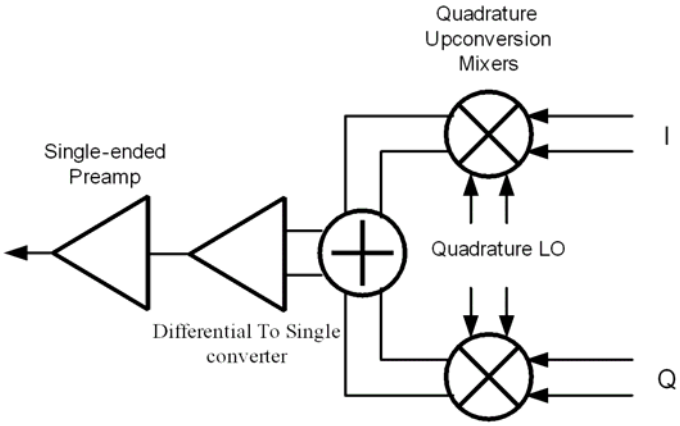


Fig. 41 5GHz TXFE for Low Power Circuit Block

5.2.1 Mixer Design

Due to the requirement of P1dB in the specification, a mixer must has a large-signal swing capability at their inputs, and which is gm-stage. Another

proposed mixer adopted different conventional structure of gm-stage as shown in Fig. 42. In this circuit the gm stage is the cross-coupled quad cell formed by two unsymmetrical differential pairs (M2, M2' and M3, M3') and a conventional, symmetrical differential pair (M1, M1') [27]. After the input differential signals transferring from voltage to current domain, the currents are added together at drain of each half differential pair.

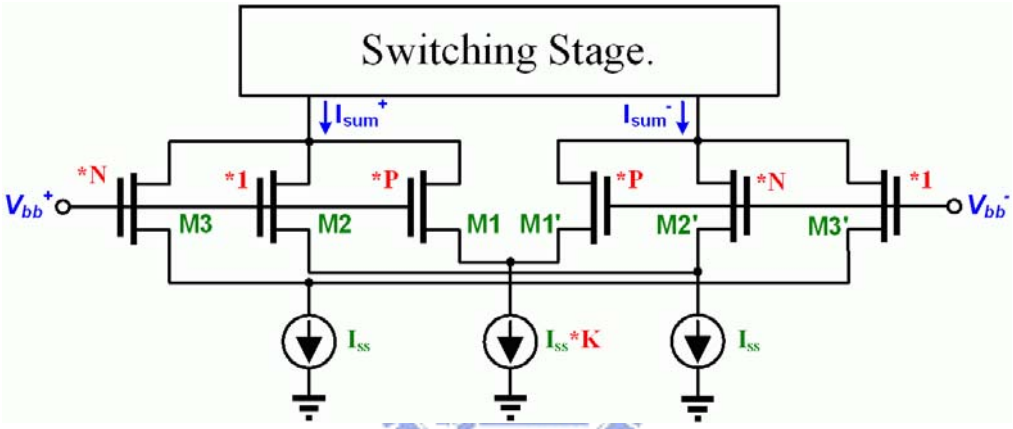


Fig. 42 Gm-stage using Multi-Gm Current Addition Technique

The aim is to make this transfer function as linear as possible, which is equivalent to make gm(v_{in}) as flat as possible, and also make the linear input range large enough. At first, by choosing the N factor of W/L ratio of two unsymmetrical differential pairs, the center of the linear transconductance can be offset from origin to obtain desired linear input range. It is important to note that V_{offset} is a function of N [28]. Therefore, the distance from the center of the linear range to the point of origin, vin=0, is approximately equal to

$$V_{offset} \approx \frac{1}{2}\left(\frac{I}{k}(n+1)\right)^{1/2}\left[\left(\frac{1}{n}\right)^{1/2}-1\right] \tag{47}$$

which causes the linear range is now limited by:

$$-\left[0.28\left(\frac{4I}{k}\right)^{1/2}+V_{offset}\right] \le v_{in} \le \left[0.28\left(\frac{4I}{k}\right)^{1/2}-V_{offset}\right] \tag{48}$$

As mentioned above, when these two cells are added together, the nonlinear range of one cell destroys the linear range of the other cell. This arrangement results in the problem that the region near the origin has very bad linearity since it contains only the nonlinear ranges of both cells. Besides, the larger N will causes the worse linear region near the origin. Thus, an additional symmetrical differential pair has been designed to compensate the nonlinearity around the origin. The height and width of this non-offset gm can be controlled by the widths of M1 and M1' and the DC bias current, which are the P and K factors respectively. Each of the three differential pairs behaves as reasonably linear transconductance. The overall transconductance is the sum of the individual transconductances, and can be made roughly constant over a large range. The simulation result is depicted in Fig. 43.

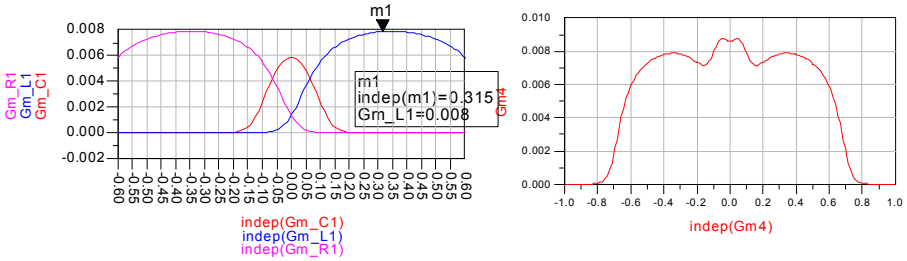


Fig. 43 Gm-stage Transfer Characteristic

One should notice that the parameter N is independent of the parameters K, and P. this is a significant advantage of the proposed circuit topology since it simplifies the linearization of the transconductance. However, the circuit is much more sensitive to the transistor mismatch. It should be pointed out that large N requires smaller process tolerances, which are difficult to control. Larger process tolerances results in worse linearity; thus, there exists a tradeoff between the input range and linearity. Besides, the larger I_{bias} , the wider of the gm characteristic.

The circuit of mixer using multi-gm current addition technique is shown in Fig. 44. We adopted the same switching-stage and load inductors as previous implementation. In order to make a comparison of this structure of gm-stage with previous one, the total bias current is also set to be the same.

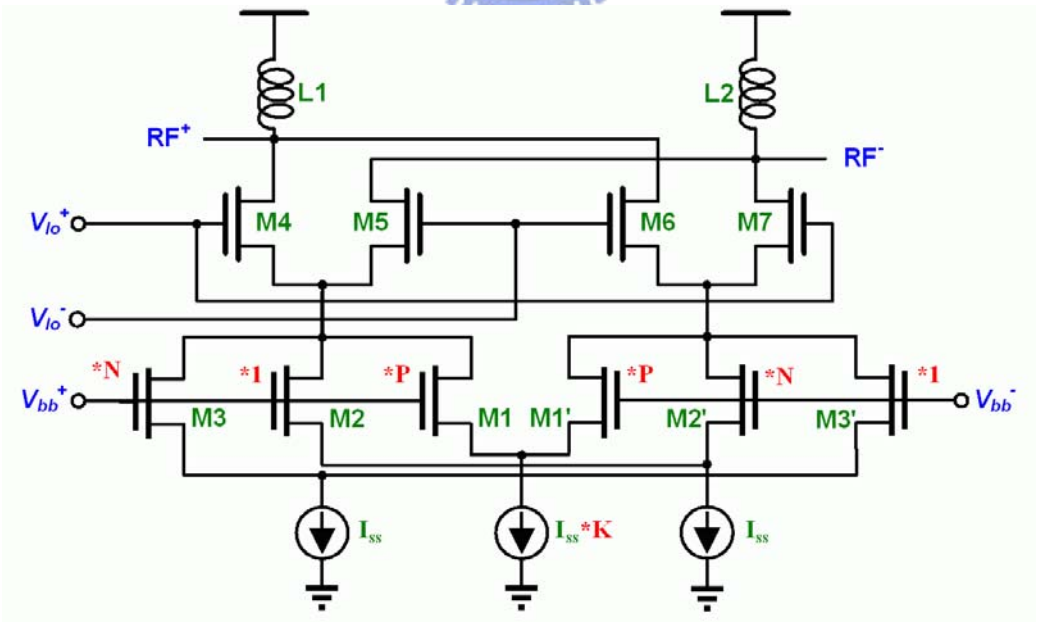


Fig. 44 Gilbert-Type Mixer with Multi-Gm Cell

5.2.2 Differential-to-Single Circuit Design

The differential-to-single (D/S) converter consists of a common source amplifier M1 which is biased by M2 as depicted in Fig. 45. The gate of the common-source amplifier senses the positive node of the differential signal in the voltage domain and combines with the negative node in the current domain at the drain. Therefore, if the common-source amplifier was designed to have unit gain, the differential outputs of mixer can be subtracted from each other at the drain resulting in double odd-order terms of the outputs while canceling out the ever-order terms. Since the parasitic capacitance at the gate and drain are different, a capacitor was added in parallel at the drain to compensate the mismatch. The voltage gain of the differential-to-single stage is simulated as shown in Fig. 46. The 6dB voltage gain indicates the D/S stage has desired unity gain performance. The D/S converter shares the load inductors of the previous up-conversion mixers at gate and drain respectively, and consequently, saving area and power consumption, however, at the cost of worsening P1dB performance.

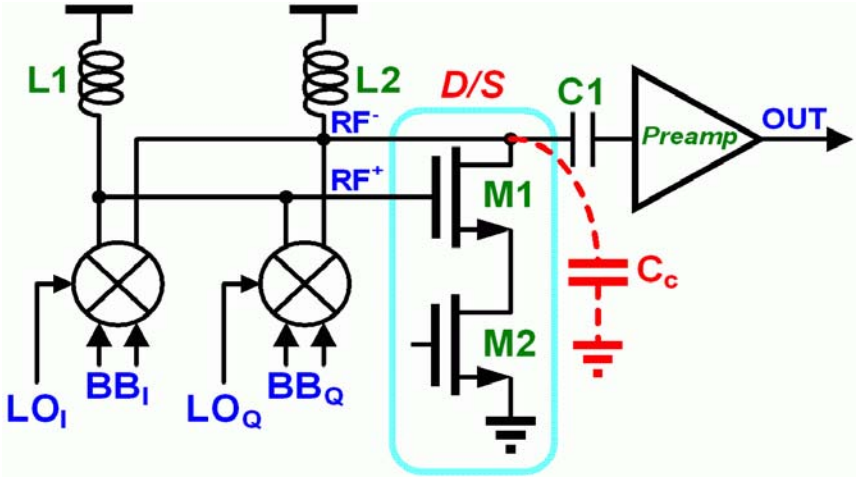


Fig. 45 Differential-to-Single Circuit

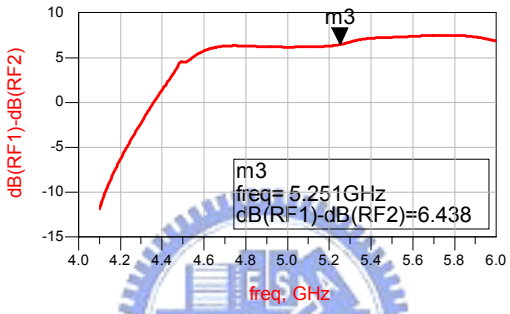


Fig. 46 Voltage Gain of Differential-to-Single Circuit

5.2.3 Preamplifier Design

Following by the D/S stage, the signal then couples to a single-ended preamplifier with a series capacitor C1. The preamplifier design also adopted two-stage configuration. The circuit is depicted in Fig. 47. The first stage is still a common-source amplifier which is operated at Class AB topology to obtain adequate linearity and power efficiency simultaneously. However, the second stage is replaced with the same common-source amplifier for saving more current dissipated than the previous source-follow amplifier. The second stage amplifier is

operated at Class AB topology as well to further improve the power efficiency. Two stages are connected by a series ac couple capacitor C2. Two of the common-source amplifiers employ inductors L1 and L2 as load at drain for the reason of saving voltage headroom and resonating the parasitic capacitance at desired frequency to obtain the optimum R_{load}. The output impedance also has been transferred into 50Ω matching.

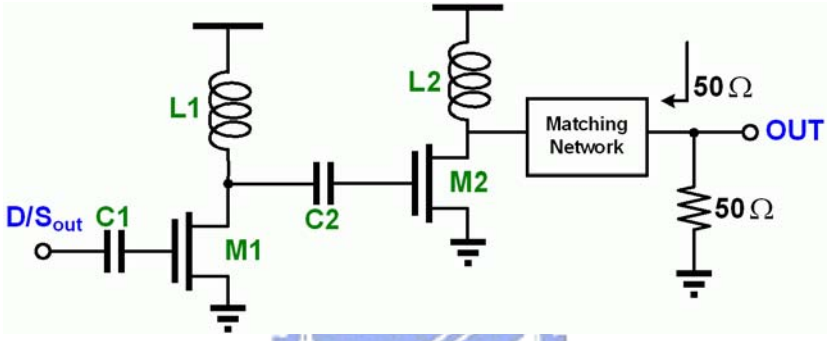
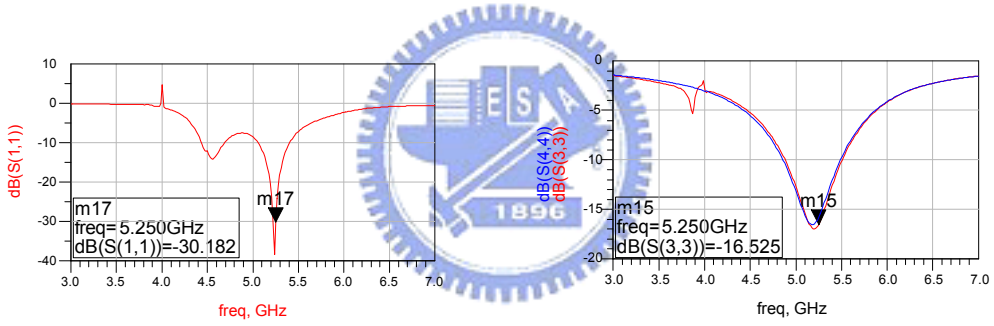


Fig. 47 Preamplifier

5.2.4 Simulation Results

This TXFE has been designed for package version only. The package model is provided by SPIL and has been added in simulation. The simulation results are shown as Fig. 48~Fig. 54, which in sequence are return loss, LO power relation, LO frequency response, conversion gain and maximum output power, output spectrum, and two-tone test. The output return loss is 30dB, while LO return loss is 16.5dB. In Fig. 49, the LO power is also set to be the same as -5dBm to compare with first implementation. In Fig. 50, when input a base band signal of -13dBm, the output has maximum power around 5.2GHz, and achieve more than 7dB from

4.57GHz~5.63GHz of 1060MHz bandwidth. The conversion gain has been designed equally to first implementation of 13.46dB. However, this TXFE performs P1dB of -10dBm and maximum output power of 2.3dBm, which is depicted in Fig. 51. The output spectrum is shown as Fig. 52 and Fig. 53. This TXFE has excellent harmonic rejection of 61dB and 172dB DC-offset suppression and 22dB LO suppression and 38dB side-band rejection. Moreover, it has input-IP3 of 2.8dBm and output-IP3 of 13.2dBm as shown in Fig. 54. This TXFE of package version consumes 25.3mA for 1.8V power supply.



(a) (b)

Fig. 48 (a) Output Return Loss (b) LO Return Loss

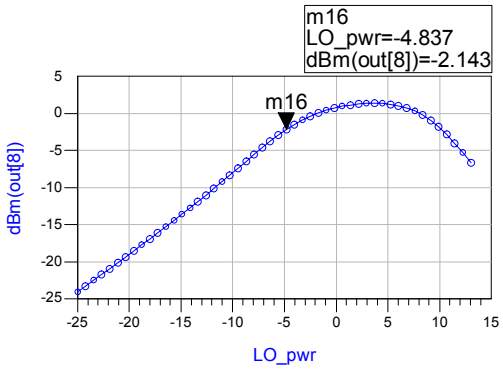


Fig. 49 LO Power vs. Output Power

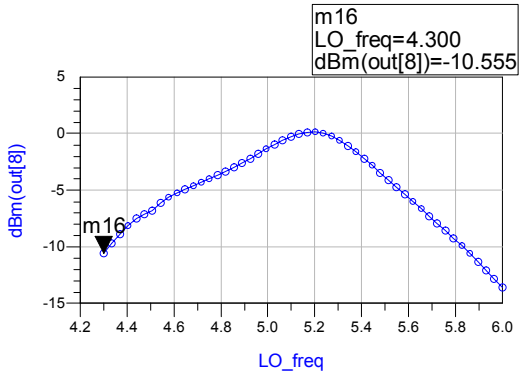
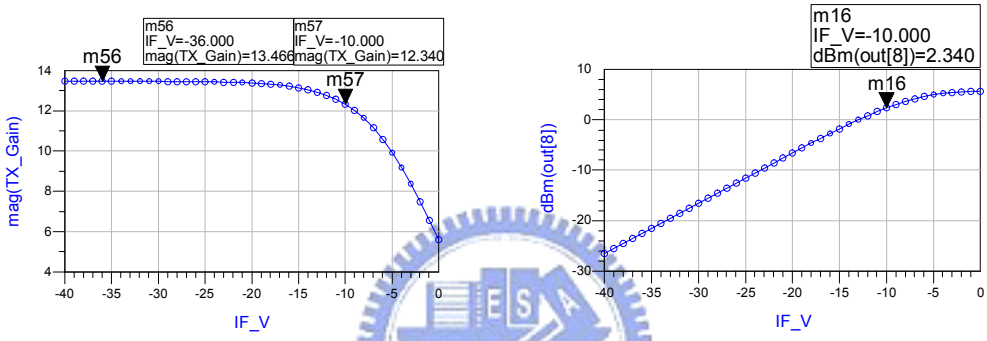


Fig. 50 LO Frequency vs. Output Power



(a) (b)

Fig. 51 (a) Input Power vs. Conversion Gain (b) Input Power vs. Output Power

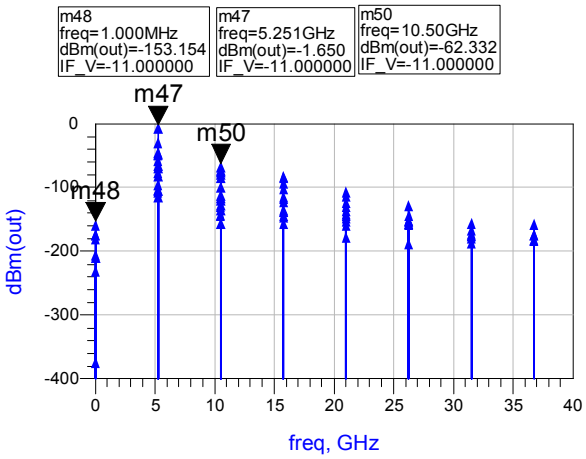


Fig. 52 Harmonic Term of 5GHz Output Signal

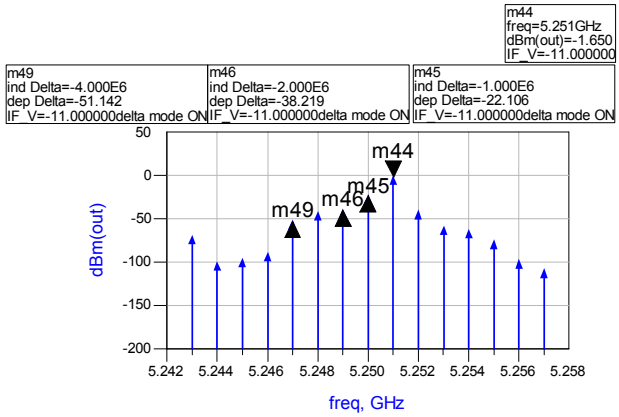
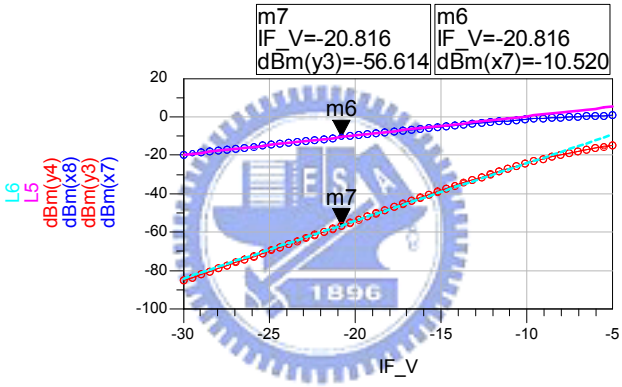


Fig. 53 LO Rejection and Side-Band Rejection



IF_V	IIP3_dBm2	IIP3_mV2	OIP3_dBm2	OIP3_V2
-30.000	2.786	1.378	13.187	4.564

Fig. 54 IIP3 and OIP3

5.3 Comparisons

Based on the equivalent LO power and power conversion gain performance, the simulation results of both transmitters front-end for package version are summarized in

TABLE 6. The transmitter front-end for high linearity design *(TXFE-HL)* achieves better linearity performance but consume 68mW. Due to the use of differential-to-single circuit, the transmitter front-end for low power design (*TXFE-LP*) merely employed single-end preamplifier. Besides, the current hungry source follow amplifier is replaced with common-source amplifier. Although, current dissipation of the mixer in each TXFE has been designed equally, the TXFE-LP has power consumption of 45mW which is lower than TXFE-HL. The differential-to-single circuit also provides good harmonic rejection and good DC-offset cancellation. However, taking the mismatch induced by process variation into consideration, the second TXFE performs worse linearity of Input-P1dB and OIP3 and worse LO suppression due to the multi-gm gm-stage must require large enough N to achieve desired input 1dB compression point, and large N will require smaller process tolerances, which are difficult to control. Therefore, we prefer the triode-MOS degeneration gm-stage in next mixer design, and also replace the preamplifier with two-stage common-source amplifier to implement a dual-band transmitter front-end.

TABLE 6 Summary of the Simulation Results for TXFE-HL and TXFE-LP Implementations

Parameters	*TXFE-HL* Package Simulation	*TXFE-LP* Package Simulation	802.11a Specification
Frequency Range	RF=4.7~5.85GHz	RF=4.57~5.63GHz	RF=5.15- 5.35GHz
Power Consumption	38mA/68mW	25.3mA/45mW	N/A
Conversion Gain	13.88 dB	13.46 dB	7 dB
Input-P1dB	-5 dBm	-10 dBm	-5 dBm
Output P1dB	7.85 dBm	2.3 dBm	2 dBm
IIP3	7.0 dBm	2.8 dBm	N/A
OIP3	17.3 dBm	13.2 dBm	12.5 dBm
RF Return Loss	-24 dB	-30 dB	<-15 dB
LO Return Loss	-22 dB	-16 dB	<-15 dB
Harmonic Rejection	20 dB	61 dB	N/A
Carrier Suppression	40 dB	22 dB	>15dBc
Side-Band Rejection	55 dB	38 dB	N/A

5.4 Dual band Transmitter Front-End Design

Before undertaking the design of dual-band transmitter frond-end, one thing must be taken into account is the power consumption issue. Recently, many literatures have described some kind of structures in order to decrease this issue. Most are the folded-cascode structures for low power supply operation [29], and the others are the current reuse techniques [30].

Besides, for a current commutating mixer, the input matching of the switching stage is not very stringent as well as RF output matching, since the signal from the local oscillator is used to turn on/off the MOSFET of the switching-stage, but does not really import a signal. Therefore, a mixer reused structure with switched mode dual-band LO matching has been proposed in this dual-band transmitter design,

which has better power consumption performance. Moreover, without additional MOSFET in the switching stage, the parasitic capacitance induced around the drain will be mitigated. However, RF port output matching is critical for each band to obtain maximum output power. Consequently, two pre-amplifier had been designed for 5 GHz and 2.4 GHz band respectively. And an additional band selection control signal has been joined to control the LO matching and the nodes mixer output simultaneously. The block diagram of this design is shown as Fig. 55.

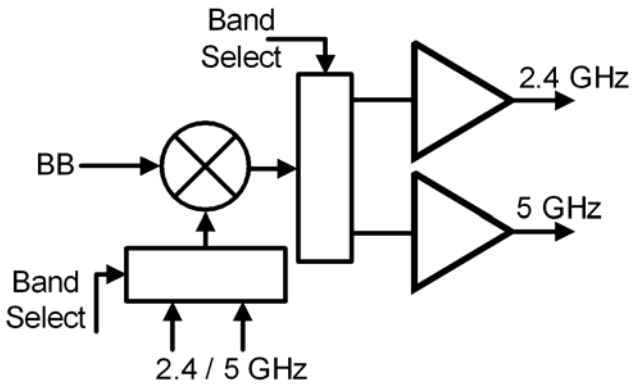


Fig. 55. Dual-Band Block Diagram

5.4.1 Mixer Design

Referring to **TABLE 6** and the discussion in section 5.3, we adopt the triode-MOS degeneration gm-stage in this mixer design. This mixer has a differential I/Q quadrature input but a passive LC current combiner is used to convert mixer differential output into a single-ended output. The band-select mechanism is accomplished by LO matching network of switching-stage and LC-tank of loading-stage as well which is illustrated in Fig. 56.

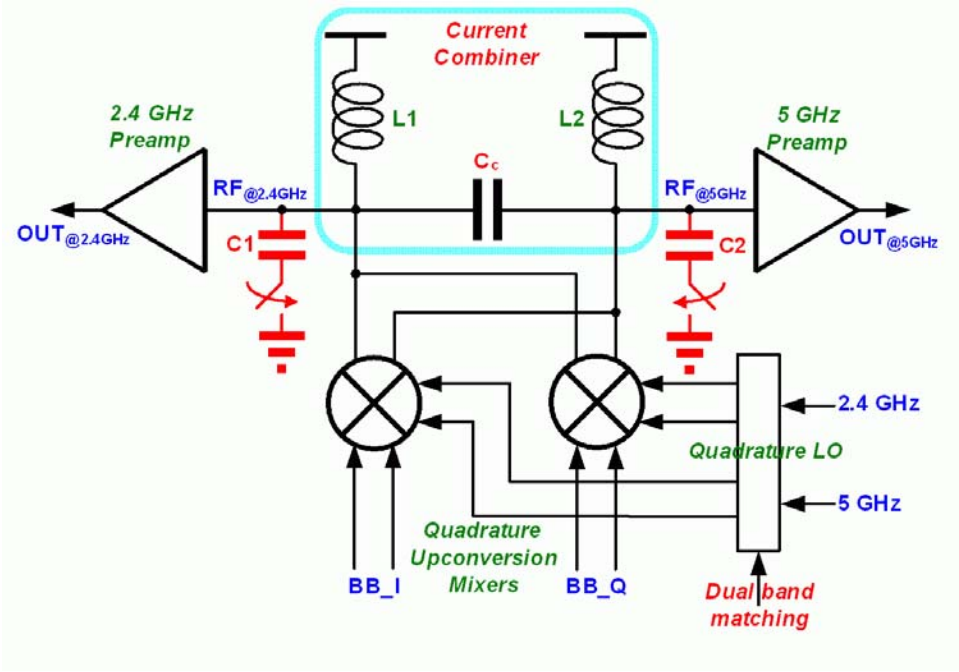


Fig. 56. Dual-Band Mixer

The current combined circuit [31] shown in Fig. 56 consists of two inductors and one capacitor. The purpose of the current-combiner is to combine the currents such that they are in phase with one another. In this way, the output will have a larger AC output swing due to the increased signal current. And the even-order distortion will be rejected by each other. Fig. 57(a) shows the ideal AC equivalent model. In the ideal case, it is assumed that all component Q's are high enough to be neglected and the output impedances of the current sources are also high enough to be neglected. The additional parallel capacitor C_p is the sum of all parasitic capacitance at mixer output node (RF) including C_{db} of switching-stage and input capacitance of the preamplifier. At first, C_p can be combined with L by

$$C_p \,||\, L = \frac{\frac{1}{j\omega C_p}\cdot j\omega L}{\frac{1}{j\omega C_p} + j\omega L} = \frac{j\omega L}{1-\omega^2 L C_p} = Z_c \tag{49}$$

as shown in Fig. 57(b).By source transformation, the parallel Z_c and current source can be converted to a voltage source and a series Z_c. The current combiner C_c can be split into two capacitors of $2C_c$ as shown in Fig. 57(c). The series Z_c and $2C_c$ can act like a short at resonance as seen in Fig. 57(d). We can derive that

$$\left(Z_c + 2C_c\right) = \frac{j\omega L}{1-\omega^2 L C_p} + \frac{1}{j\omega 2C_c} = 0 \Rightarrow \omega = \sqrt{\frac{1}{L\left(2C_c + C_p\right)}}\,. \tag{50}$$

Further, the voltage source and series $2C_c$ are converted back into a current source and a parallel $2C_c$ and by substituting (68), we obtain

$$I = \frac{V}{Z} = \frac{(i)\frac{j\omega L}{1-\omega^2 L C_p}}{\frac{1}{j\omega 2C_c}} = (-1)(i)\frac{\omega^2 2C_c L}{1-\omega^2 L C_p} = (-1)(i)\,. \tag{51}$$

The ac current has been aligned in phase as Fig. 57(e). Once again, the parallel Z_c and $2C_c$ can act like an open at resonance resulting in Fig. 57(f). Therefore, by switching the current's direction, the negative sign disappears and the current source is aligned in the same direction as the other one. The current combiner doubles the output current at the resonant frequency,

$$\omega_o = \sqrt{\frac{1}{L\left(2C_c + C_p\right)}} = 5GHz\,. \tag{52}$$

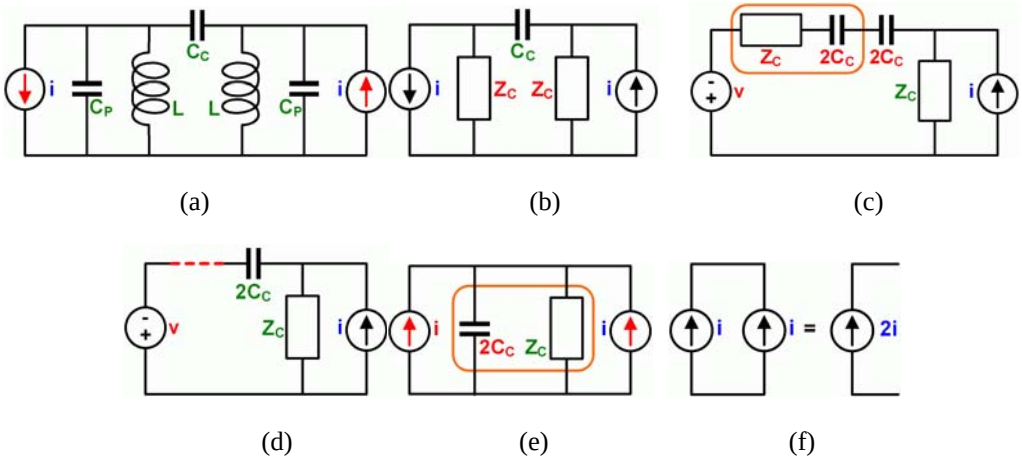


Fig. 57 Equivalent Circuit of Current Combiner

A passive current combiner has a desired band pass response for up-conversion mixer application. Moreover, for the dual-band operation of this mixer, two additional capacitors have been paralleled around the loading inductors. And with the control signal switching, the capacitance seen from mixer output node can be increased, resulting in a smaller resonant frequency.

$$\omega_o = \sqrt{\frac{1}{L_1(2C_c + C_p + C_1)}} = 2.4GHz \qquad (53)$$

A conjugating matching would transfer the maximum output power of mixer to the next stage, and each of the balanced output nodes would couple to 5GHz and 2.4GHz preamplifier, respectively. On the other side, the LO matching network adopted switch-able parallel capacitor as depicted in Fig. 58. When V_{sw} is high, the network obtains 2.4GHz matching, the other else.

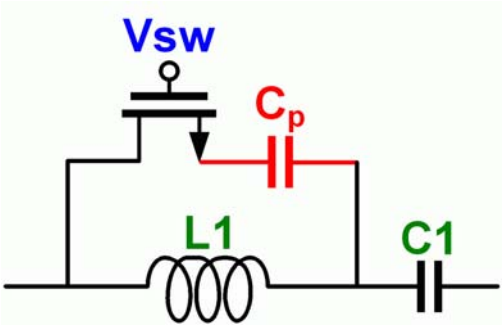


Fig. 58 LO Dual-Band Matching Network

5.4.2 Preamplifier Design

The circuits for 2.4GHz and 5GHz preamplifier are depicted in Fig. 59 and Fig. 60. Two common-source amplifiers have been used in two-stage configuration. They are mostly alike with previous design. Excepting that for 5GHz preamplifier, an additional degeneration inductor has been used at the first stage to achieve required linearity.

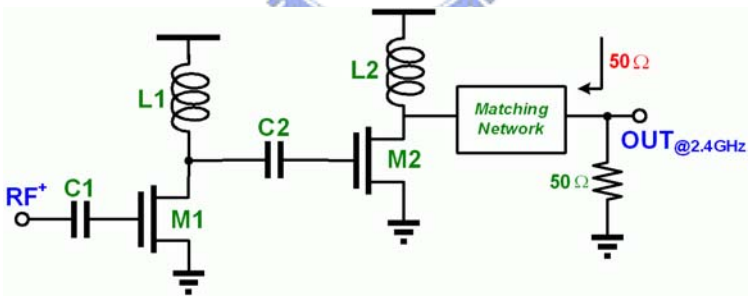


Fig. 59 2.4 GHz Preamplifier

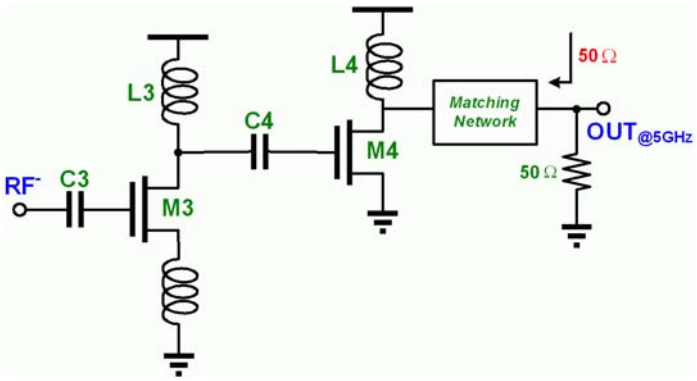
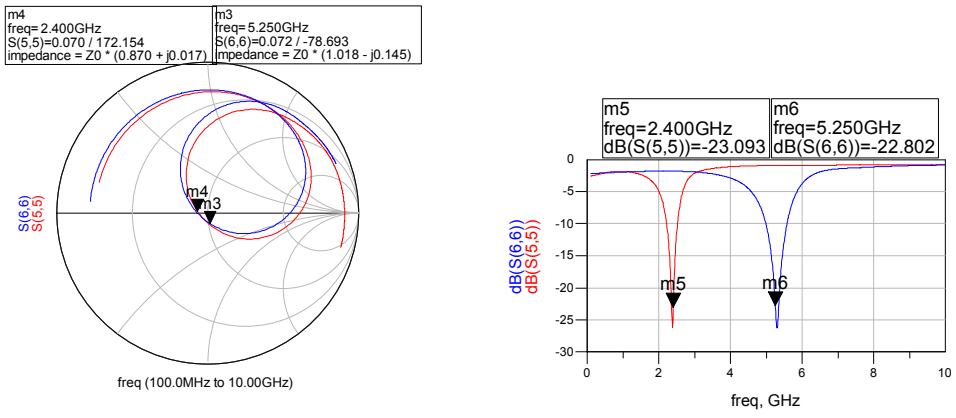


Fig. 60 5 GHz Preamplifier

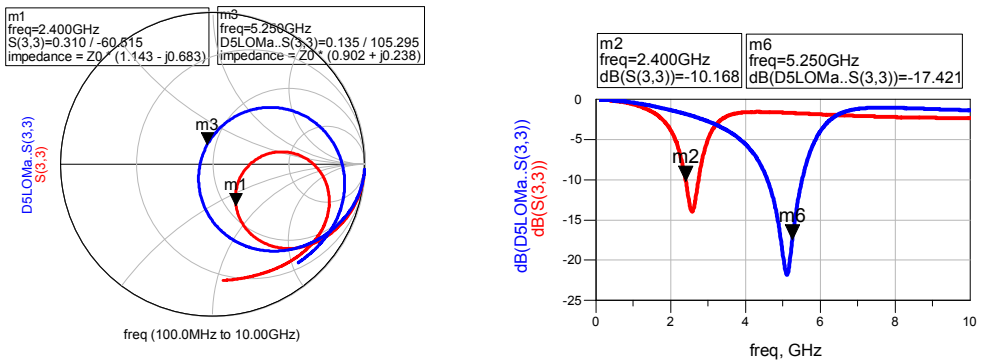
5.4.3 Simulation Results

The simulation results for dual-band transmitter front-end are depicted in Fig. 61~Fig. 66. The output return loss is 23dB for 2.4GHz and roughly the same for 5.25GHz. The LO dual-band matching network obtains 10dB return loss for 2.4GHz input and 17dB for 5.25GHz input. The power conversion gain has been designed to 7dB for both bands and either has nearly input P1dB of -5dBm and maximum output power of 1dBm. The frequency responses illustrate that the dual-band matching network and dual-band load of mixer well function at desired frequency. Finally, the two tone test shows that the input-IP3 is about 5.8dBm and output-IP3 is about 10dBm for operation of both bands. The simulation results will be listed in detail in the next section. This dual-band transmitter front-end consumes 24.4mA for 1.8V power supply.



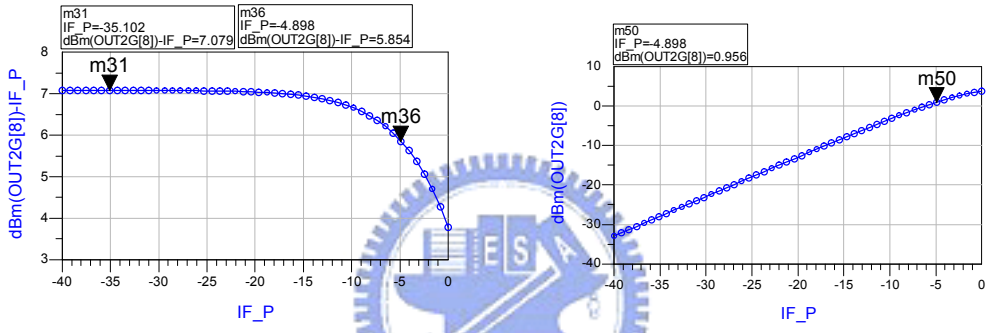
(a) (b)

Fig. 61 Dual-Band Output Matching (a) Smith Chart (b) Return Loss



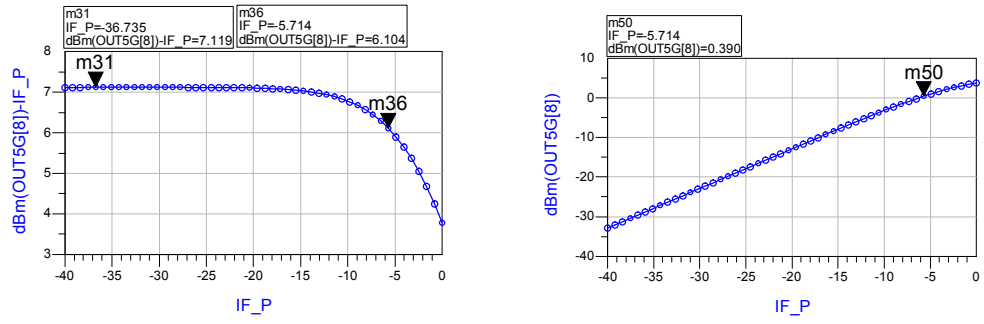
(a) (b)

Fig. 62 Dual-Band LO Matching (a) Smith Chart (b) Return Loss



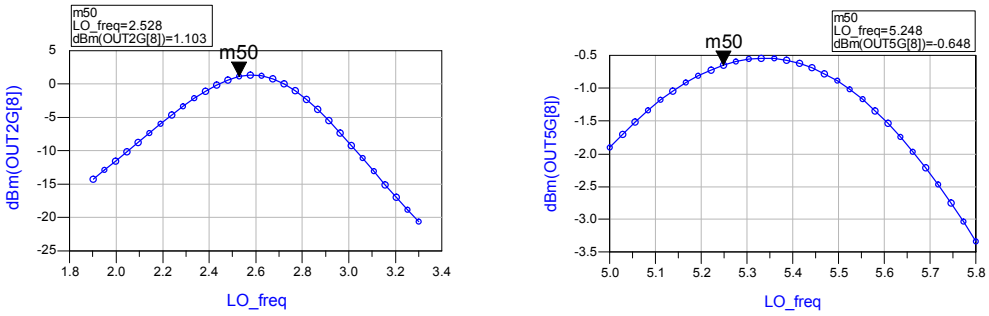
(a) (b)

Fig. 63 (a) Conversion Gain & P1dB (b) Maximum Output Power (for 2.4 GHz)



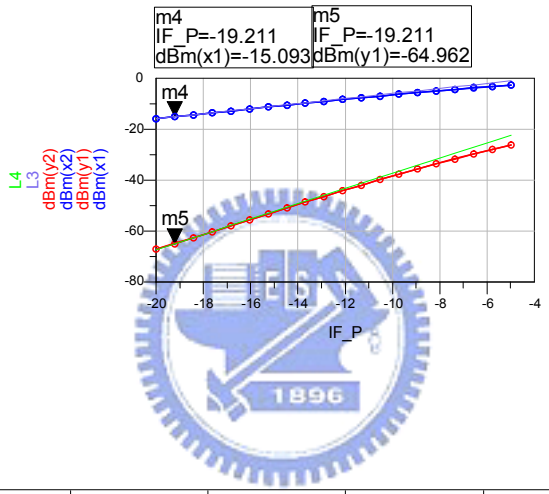
(a) (b)

Fig. 64 (a) Conversion Gain & P1dB (b) Maximum Output Power (for 5.2 GHz)



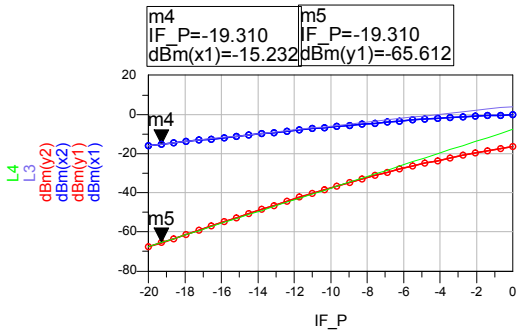
(a) (b)

Fig. 65 Frequency Response for (a) 2.4GHz (b) 5.2 GHz



IF_P	IIP3_dBm1	IIP3_mV1	OIP3_dBm1	OIP3_V1
-19.211	5.724	1.933	9.841	3.105

(a)



IF_P	IIP3_dBm1	IIP3_mV1	OIP3_dBm1	OIP3_V1
-19.310	5.880	1.968	9.958	3.147

(b)

Fig. 66 IIP3 and OIP3 for (a) 2.4GHz (b) 5.2GHz

5.4.4 Simulation Summary

The simulation results for dual-band operation are summarized in **TABLE 7** with specification of 802.11a/b/g. Since the preamplifier for 5GHz/ 2.4GHz are separately designed, the output return loss is easily designed. This circuit achieves required power conversion gain with bandwidth of 300MHz for 2.4GHz and 400MHz for 5.25GHz. The linearity performances of P1dB and OIP3 are also closed to the specification.

TABLE 7 Dual-Band Simulation Summary

Parameters	2.4 GHz design	5 GHz design	802.11a/b/g Specification
Frequency Range	2.40-2.70GHz	5.15-5.55GHz	2.4-2.485GHz 5.15- 5.825GHz
Conversion Gain	7.0 dB	7.1 dB	7 dB
Input-P1dB	-5 dBm	-5.7 dBm	-5 dBm
Output P1dB	1 dBm	0.4 dBm	2 dBm
OIP3	9.8 dBm	9.9 dBm	12.5 dBm
RF Return Loss	-23 dB	-22 dB	<-15 dB
LO Return Loss	-10 dB	-17 dB	<-15 dB

Chapter 6

Experimental Results and Discussions

After each circuit has been designed and simulated, this chapter will start with introducing some back-end considerations, including of layout technique, design of printed circuit board (PCB), measurement setup…etc, since these back-end considerations also dominant the performance of our design at radio frequency. Layout skill always plays an important role to implement a RF circuit, since signals will suffer from coupling to each other at radio frequency and process variation will be anther worry. The parasitic effects of package and bond wire will also interferer our design. Besides, since a radio frequency signal has relative short wave length, the microstrip line on PCB will be tough to design precisely, and either the constraint of matching to 50Ω. Then, we will introduce the electrostatic-discharging (ESD) protection, and package model. Continuously, as for measurement, a low frequency transformer and 5GHz quadrature phase shifter have been adopted. And the measurement setup of one-tone test and two-tone test for the implementation of 5GHz transmitter front-end will be introduced. Finally, the measurement results of

5GHz implementation (1) and (2) will be listed, respectively.

6.1 Layout Considerations

The common centroid layout skill was extensively used on MOS layout to prevent the device from process variation, and then decreases the probability of circuit mismatch. The layout of the wire between four quadrature phase signals coming from local oscillator (LO) must keep symmetrical to decrease the phase error to obtain a better DC offset cancellation and even-order harmonic rejection. Meanwhile, the I/Q branch of the mixer and the fully-differential RF path also need to be maintained symmetry for the same reason.

To avoid the unwanted RF noise coupling from substrate to desired signal, all the RF signal path have metal lines shield under them. The Metal 1 was chosen for less parasitic capacitance due to the longer distance from the signal path while the distance between signal path and grounded line on the same layer was kept as far as possible for the same reason, since large parasitic capacitance will limit the range of using inductors. To improve the isolation between different blocks, local substrate contacts have been used to surround each device including MOS transistors, capacitors, inductors and resistors. And grounded metal lines have been used again which are placed between components and signal paths to provide additional isolation and decrease the feedthrough from LO to BB and LO to RF, and also

self-mixing phenomenon will be resolved. The layout of grounded metal lines is illustrated in Fig. 67.

Moreover, any parasitic capacitance distributed around the RF path should be avoided for more accurate and more expectable experimental result. So the RF signal paths must keep as short as possible, especially the node of mixer I/Q summation and the drain of the first stage of pre-amplifier: common source amplifier and the output matching network. Since too much parasitic capacitance distributed over these nodes will limit the range of using inductor (ex: large capacitor will force to use the small inductor and results in smaller series parasitic resistor and either worse gain performance).

Finally, the Separate ground pads and VDD pads have been used for the mixer, pre-amplifier, and ESD protection. The base band signal, LO signal source and RF output are place perpendicularly to mitigate coupling effect, meanwhile, ground pads and DC pads are placed between each RF pads for the shielding of coupling. And unwanted coupling between the inductors is maintained below a few percent by proper spacing.

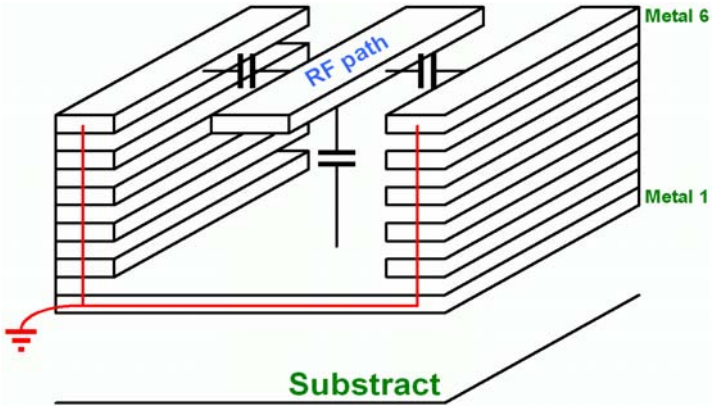


Fig. 67 Layout of Grounded Metal Line

6.2 ESD Protection

For thin oxide process, ESD protection is also a critical issue due to that the shorter of the channel, the smaller tolerance of the gate voltage. Thus, MOSFET will be easily pierced. Fig. 68 illustrates the ESD protection circuit used in out design. The diode-chain protection will guide large number of charge to GND or VDD, and the large gate-grounded NMOS will break down once a large potential across VDD and GND resulting in the charge in VDD flowing through NMON to GND. The ESD protection circuit is added to each I/O pin. This circuit is provided by UMC with 3.6kV human body mode (HBM) tolerance and induces around 40fF parasitic capacitance at each pad.

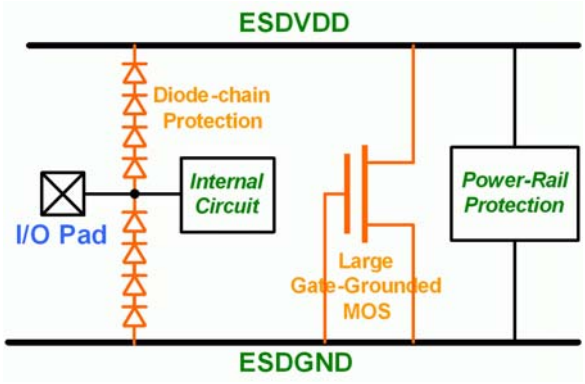


Fig. 68 ESD Protection Mechanisms

6.3 Package Topology

The QFN20D package provided by SPIL is employed in our design. This package is limited by 20 I/O pins. The overall area of package is 2.5*2.5 mm^2. The package model including bond wire effect of each I/O pin is depicted in Fig. 69. The parasitic capacitance induced at each I/O pad is around 40fF while the series inductance induced by bone wire is about 1nH. Furthermore, the parallel capacitance will lead to signal coupling between adjacent pin which are the most concern of our design.

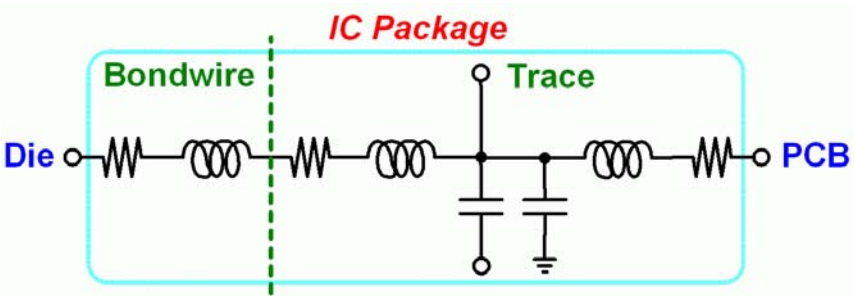


Fig. 69 Package Model

6.4 PCB Design

As for the implementation of printed-circuit board (PCB), we adopt “RO4003”

as our dielectric owning to this material has less loss at high frequency operation. The dielectric constant is around 3.4 at 5GHz. Besides, we employ four-layer board to firm up the copper signal line, and further stabilize the RF signal path.

6.5 Measurement Setup

Three additional off-chip components must be employed for measurement. They are in sequence transformer, power combiner, and quadrature phase shifter for 5GHz signal.

6.5.1 Transformer

A transformer is used at input to convert the single-end base band signal comes from ESG to differential and then input to the gm-stage of mixer. The transformer is shown in Fig. 70 which is produced by Mini-Circuits ADT4-6T.

Fig. 70 Transformer

6.5.2 Power Combiner

A power combiner is used to add together two sinusoidal waves with different frequency and then input to the transformer for conversion of single-end to differential. The power combiner is 2way-0°, by Mini-Circuits ZFSC-2-10G as shown in Fig. 71.

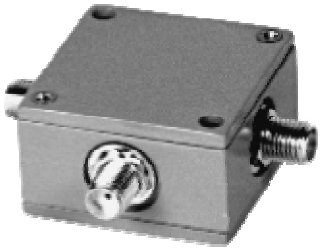
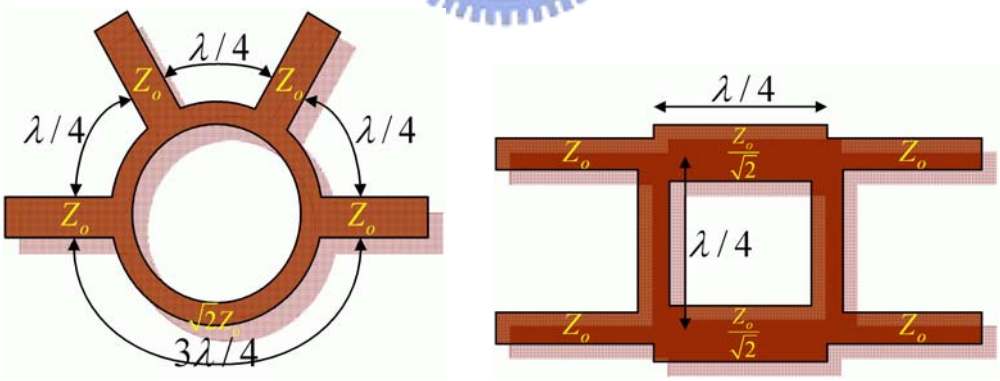


Fig. 71 Power Combiner

6.5.3 5GHz Quadrature Phase Shifter

A quadrature phase shifter is used to convert single-tone signal comes from LO ESG of 5.25GHz to four output signals with quadrature phase. This quadrature phase shifter is designed and simulated by ADS-Momentum and implemented on PCB using microstrip line. It is realized with combination of a rate race coupler to provide 180° phase shifter and two branch line couplers to provide additional 90° phase shifter as depicted in Fig. 72.



(a) (b)

Fig. 72 (a) Rate Race Coupler (b) Branch Line Coupler

Fig. 73 shows quadrature phase shifter implemented on PCB and the measured loss and phase of each output port is summarized at **TABLE 8**.

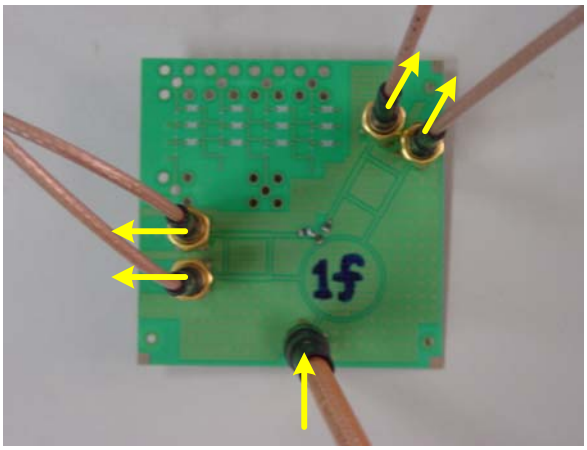


Fig. 73 Quadrature Phase Shifter on PCB

TABLE 8 Measured Loss and Phase of Quadrature Phase Shifer

0Port Number	1	2	3	4
Loss	6.9 dB	7.4 dB	7.9 dB	6.9 dB
Phase	90°	0°	180°	276°

6.5.4 One-Tone Test

The measurement setup for one-tone test is shown in Fig. 74. Three signal generators have been used to supply two base band I/Q signals with 90° phase difference, and one LO signal. They are in sequence Agilent E4438C ESG and Agilent 83731B Synthesized signal Generator. Two transformers and one quadrature phase shifter have been used for signal conversion. One of the output is detected by Agilent E4446A Spectrum Analyzer with another terminated by 50Ω.

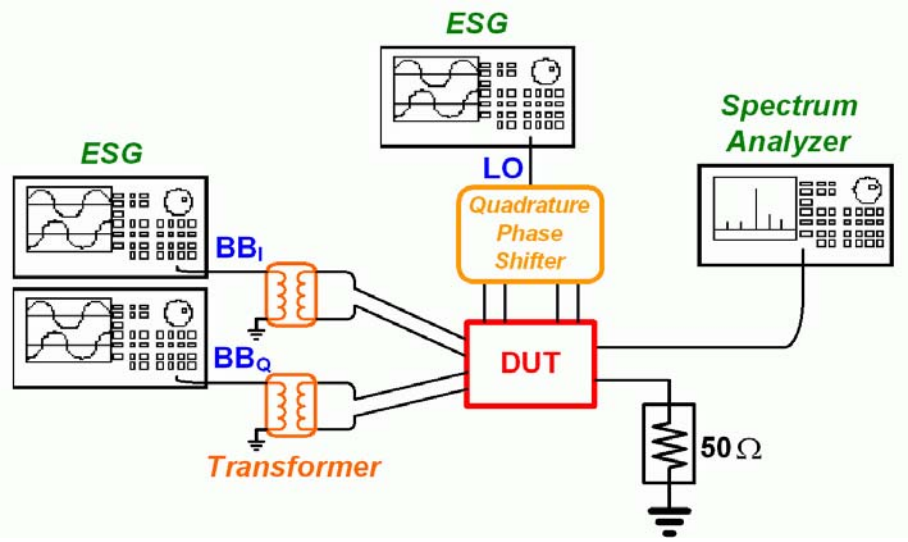


Fig. 74 One-Tone Test Measurement Setup

6.5.5 Two-Tone Test

The testing setup of two-tone test is similar to one-tone test which is illustrated in Fig. 75 except that two additional power combiners have been used. Besides, four signal generators provide four base band signals with two different frequencies and each frequency has 90° phase offset. The I/Q signals are individually added together by the power combiner, and then similarly pass through the transformer for conversion. The LO signals are still provided by a signal generator and the quadrature phase shifter, and a Spectrum Analyzer is used to measure the power of output spectrum.

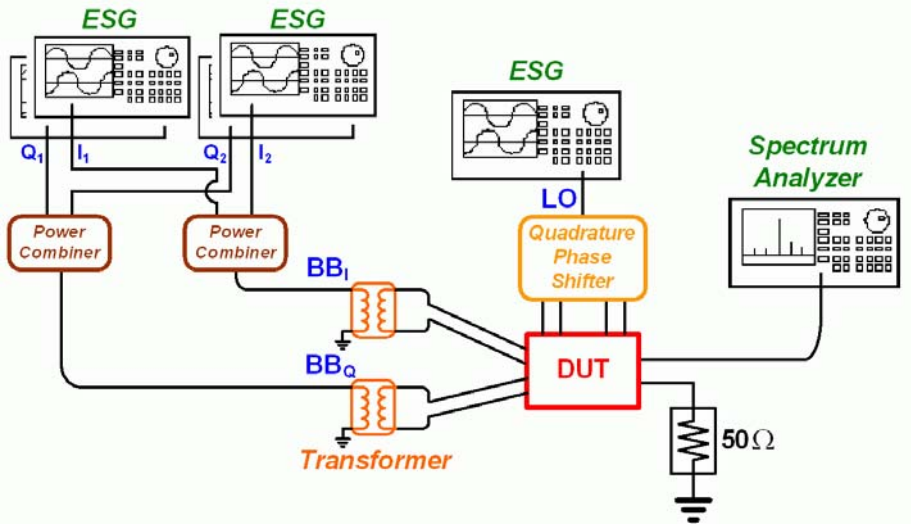


Fig. 75 Two-Tone Test Measurement Setup

Fig. 76 is the overview of our measurement environment. It shows two LO signal generators, two BB signal generators, one power supply, and one spectrum analyzer. And the connection of measurement is shown in Fig. 77.

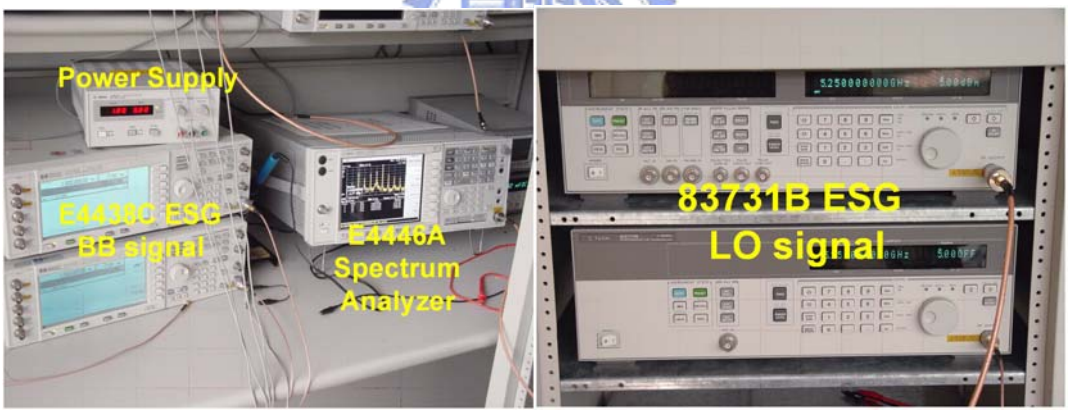


Fig. 76 Instruments Overview

Fig. 77 Measurement Connection

6.6 Measurement Results of 5GHz TXFE-HL

In order to doubly verify this design, on wafer version and package version are both implemented. The circuits are layouted and fabricated by UMC 0.18um single-ploy-six-metal (1P6M) CMOS technology. Each layout composes of a quadrature mixer, I/Q summation, and a fully-differential pre-amplifier.

6.6.1 On-Wafer Testing

Fig. 78 shows the overall layout of the on-wafer version. The die area is 2140*1410 um^2 including pads. And the microphotograph of this chip is also shown in Fig. 79.

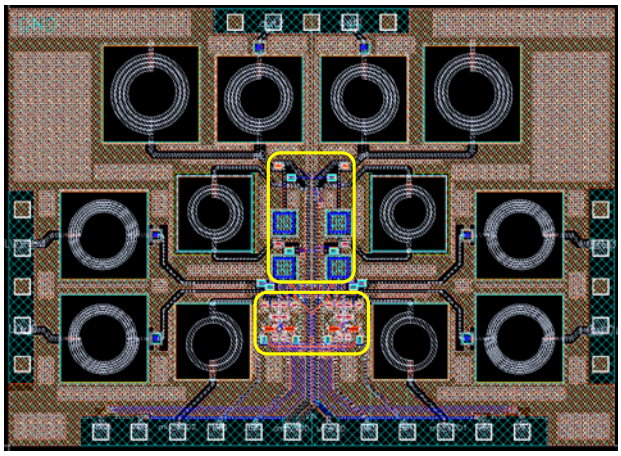


Fig. 78 Layout of 5GHz TXFE-HL (On-Wafer Design)

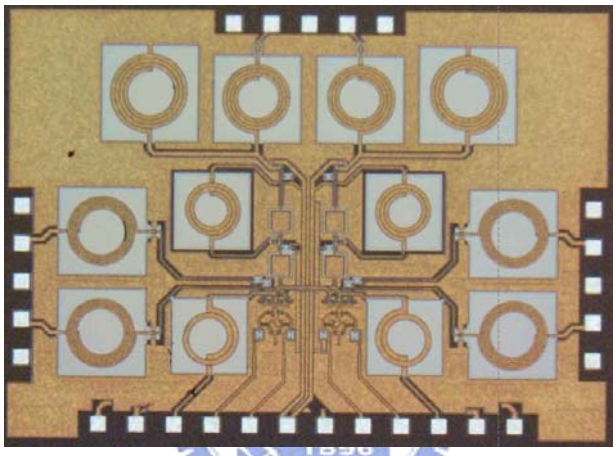


Fig. 79 Microphotograph of On-Wafer Design

Fig. 80 shows the output spectrum of one-tone up-conversion. The measured RF output frequency locates at 5.251GHz and the power is -3.987dBm while the input LO frequency locates at 5.25GHz with 8dBm power and the input BB frequency locates at 1MHz with -7dBm power. After calibrating the loss contributing from cable, SMA connector, and the quadrature phase shifter at RF output path of 3.8dB and at LO path of 13dB, the power conversion gain of upper-side band is equal to $\left(-3.987-\left(-7\right)+3.8\approx\right)7dB$, when the equivalent input LO power is -5dBm. Fig. 80 also illustrates the side-band rejection of 33dB referring

to lower-side band of 5.249GHz and the carrier rejection of 40.8dB when input BB power is -7dBm.

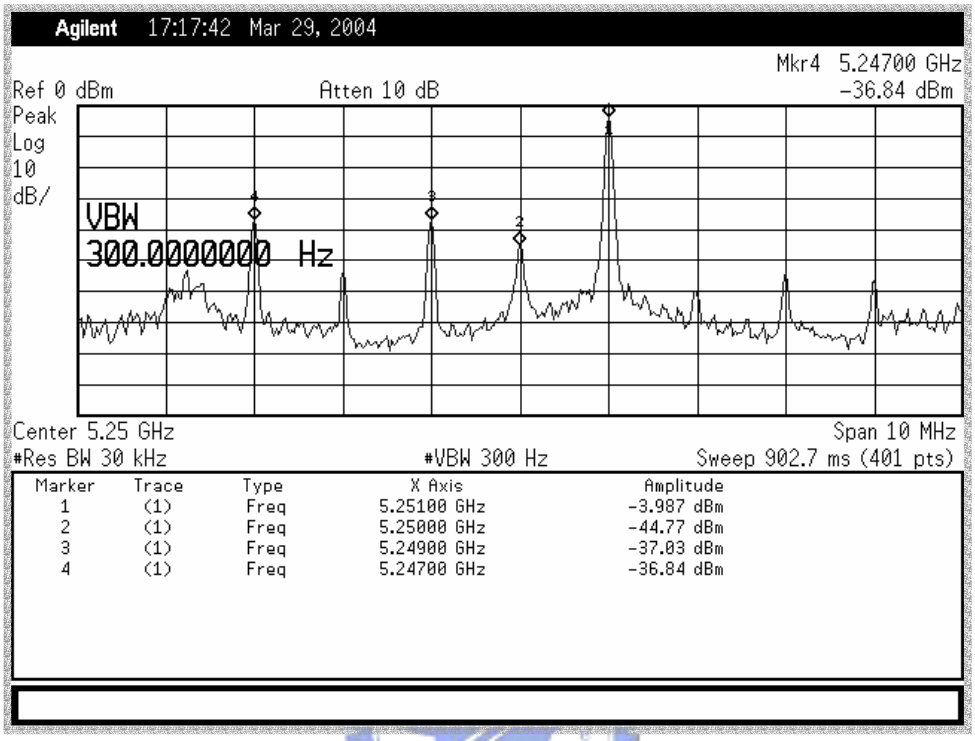


Fig. 80 5GHz TXFE-HL Output Spectrum for On-wafer Design

The measurement items are LO frequency vs. output power, input power vs. output power, and input power vs. conversion gain as shown in Fig. 81~Fig. 83. The solid line (blue) expresses the simulation result while the circle-solid line (red) expresses the measurement result. In Fig. 81, since the on-wafer testing is very sensitive to interference around, the output frequency response is not very smooth. However, we can still judge that the resonator functions as expected, but the conversion gain is abated by 4.7dB at desired frequency. Fig. 82 and Fig. 83 also show that the measured output power and 7.2dB conversion gain which are both abated by 4.4dB comparing to simulation with input P1dB of -6dBm slightly worse

than simulation result.

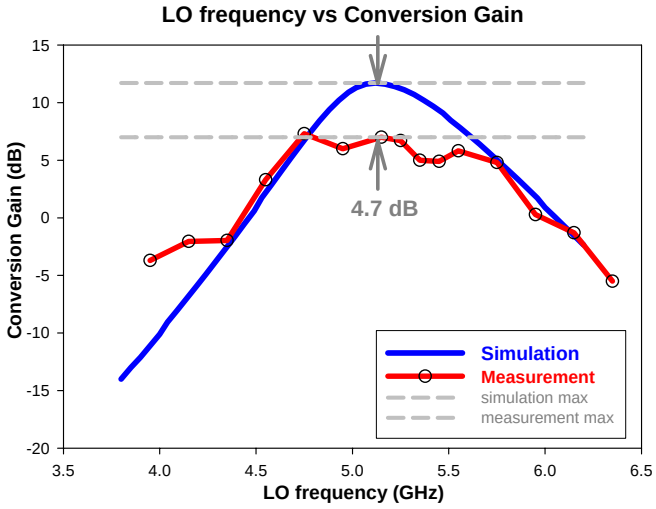


Fig. 81 LO Frequency vs. Conversion Gain (TXFE-HL On-Wafer Design)

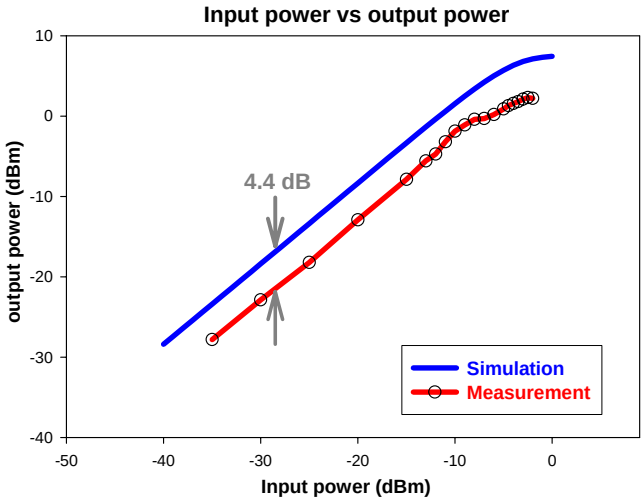


Fig. 82 Input Power vs. Output Power (TXFE-HL On-Wafer Design)

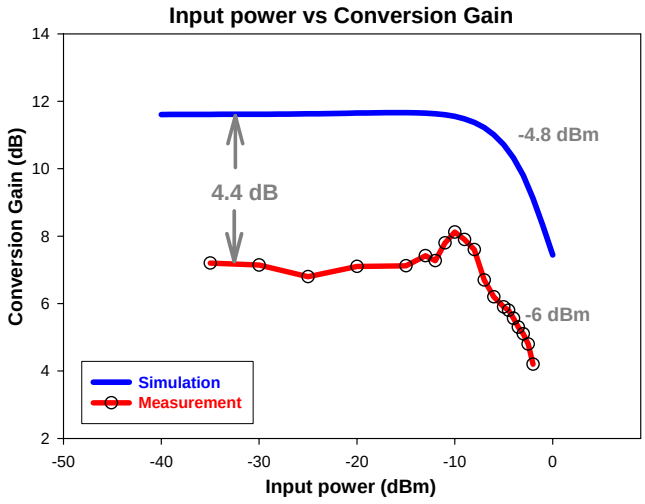


Fig. 83 Input Power vs. Conversion Gain (TXFE-HL On-Wafer Design)

6.6.2 Package Testing

Fig. 84 shows the overall layout of the 5GHz implementation for package version. The die area is 2040*2030 um^2 without including pads. And Fig. 85 is the overview of chip on PCB with two transformers soldering together.

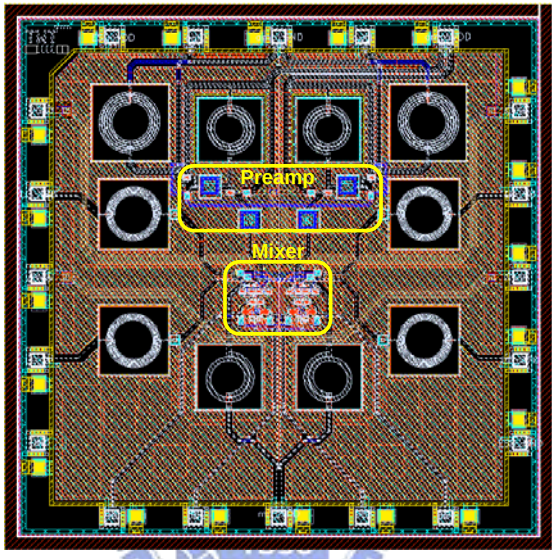


Fig. 84 Layout of 5GHz TXFE-HL (Package Design)

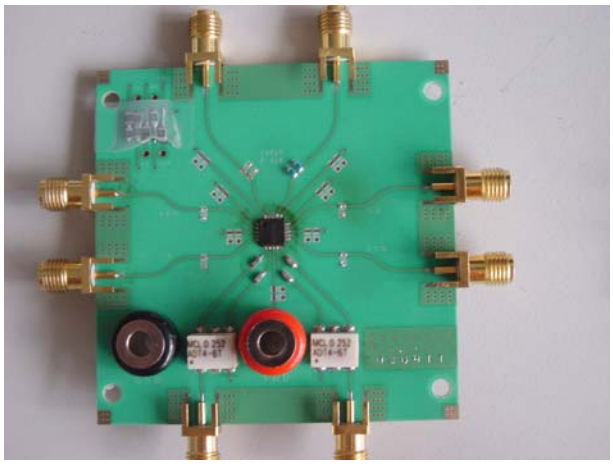


Fig. 85 Overview of Chip On PCB (TXFE-HL)

Fig. 86 shows the output spectrum of one-tone up-conversion for package version. The measured RF output frequency locates at 5.251GHz and the power is

-0.31dBm while the input LO frequency locates at 5.25GHz with 5dBm power and the input BB frequency locates at 1MHz with -7dBm power. Similarly we first calibrate out the loss contributing from cable, SMA connector, and the quadrature phase shifter at RF output path of 1.5dB and at LO path of 10dB and the power conversion gain of upper-side band is equal to $\left(-0.31-\left(-7\right)+1.5\approx\right)8.2dB$ for equivalent input LO power of -5dBm. Fig. 86 also illustrates the side-band rejection of 33dB referring to lower-side band of 5.249GHz and the carrier rejection of 27dB when input BB power is -7dBm.

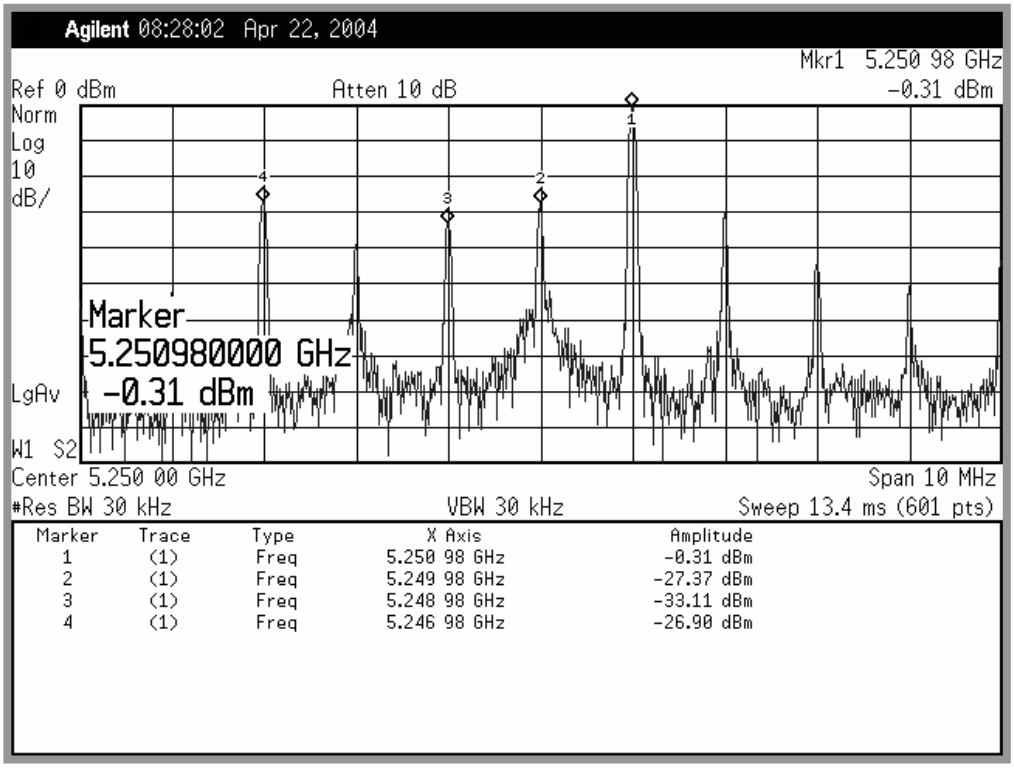
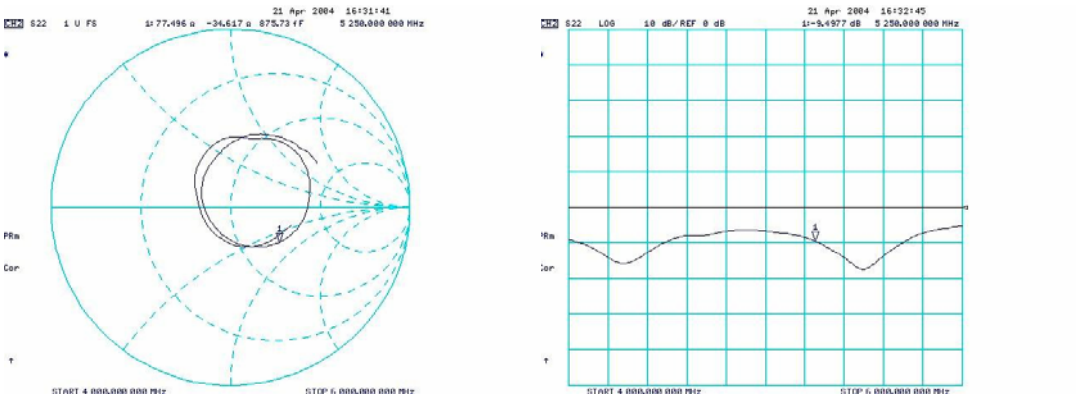


Fig. 86 5GHz TXFE-HL Output Spectrum for Package Design

The measurement items are LO/RF matching, LO power vs. output power, LO frequency vs. output power, input power vs. output power, input power vs. conversion gain, and two-tone test for IP3 as shown in Fig. 87~Fig. 94. The LO

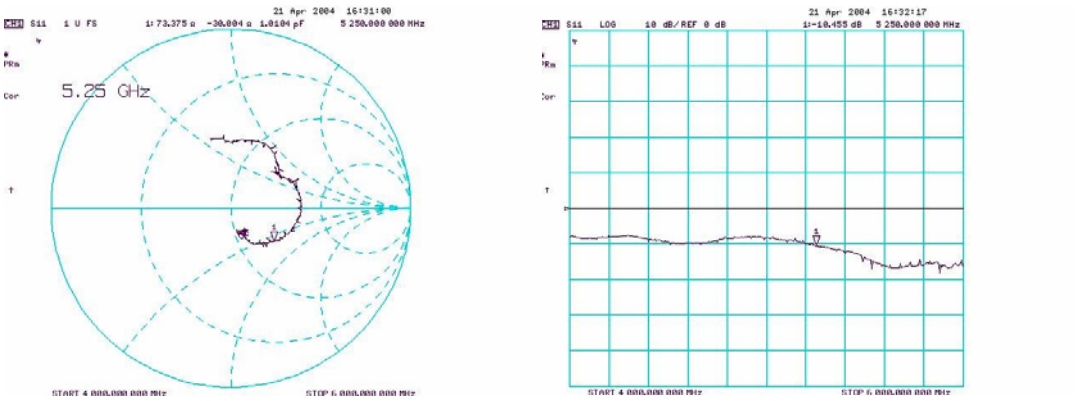
return loss is 9.5dB while RF output return loss is 10.45dB at frequency of 5.25GHz, which are both worse than simulation result but maybe acceptable.

In Fig. 89, we can see that the measurement result resemble simulation but with ~5dB degradation, when the LO power are both set -5dBm at the border of linear and constant region. This degradation of 5dB also replies on output frequency response output power and conversion gain. Fig. 90 shows that the measured maximum output power does not locate at 5.25GHz, but with some frequency offset. We can judge that some or all of the resonators in this design function wrong. Besides, the measured maximum output power also degrades by about 2.5dB, which is resulted from output matching degrading by more than 6dB, and this assumption will be verified as followed. Fig. 92 also shows that the conversion gain is 8.6dB which is abated by 5.3dB comparing to simulation with input P1dB of -5.3dBm closed to simulation result.



(a) (b)

Fig. 87 LO Matching (a) Smith Chart (b)LOG



(a) (b)

Fig. 88 RF Matching (a) Smith Chart (b)LOG

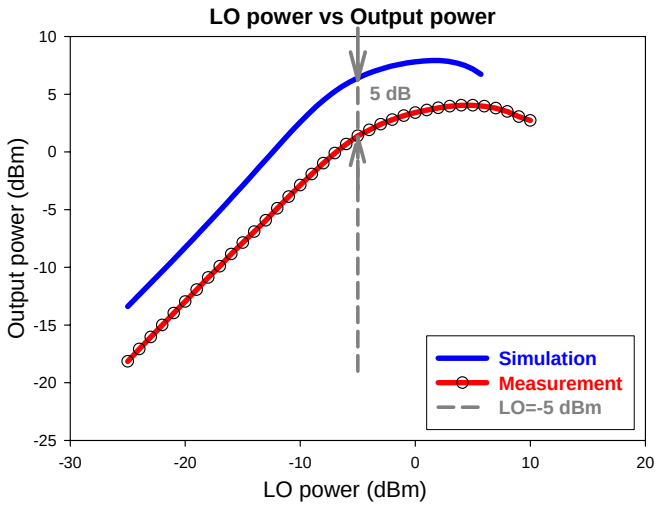


Fig. 89 LO Power vs. Output Power (TXFE-HL Package Design)

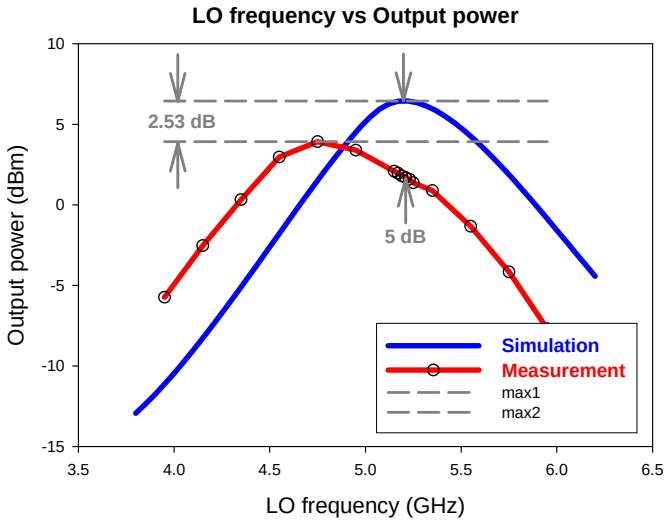


Fig. 90 LO Frequency vs. Output Power (TXFE-HL Package Design)

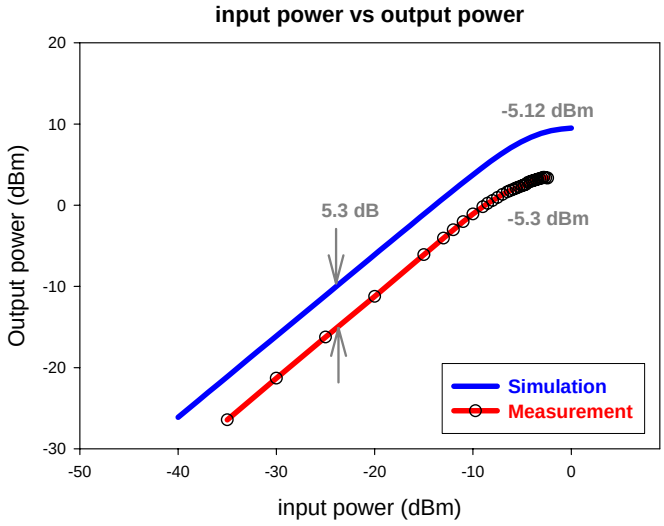


Fig. 91 Input Power vs. Output Power (TXFE-HL Package Design)

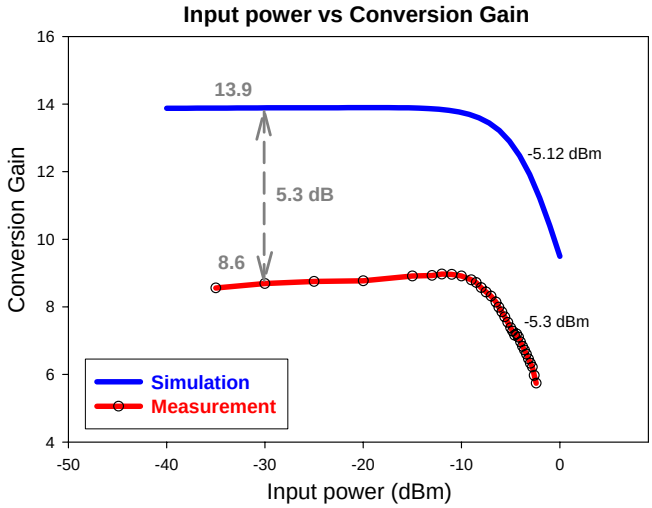


Fig. 92 Input Power vs. Conversion Gain (TXFE-HL Package Design)

Fig. 93 shows the output spectrum of two-tone up-conversion testing. The measured RF output frequency locate at 5.256GHz and 5.257GHz and the IM3 appear at 5.255GHz and 5.258GHz while the input LO frequency maintains at 5.25GHz and the input two-tone BB frequency locates at 6MHz and 7MHz. The measured input power vs. IM3 is depicted in Fig. 94. This circuit achieves input IP3 of 6.29dBm and output IP3 of 13dBm.

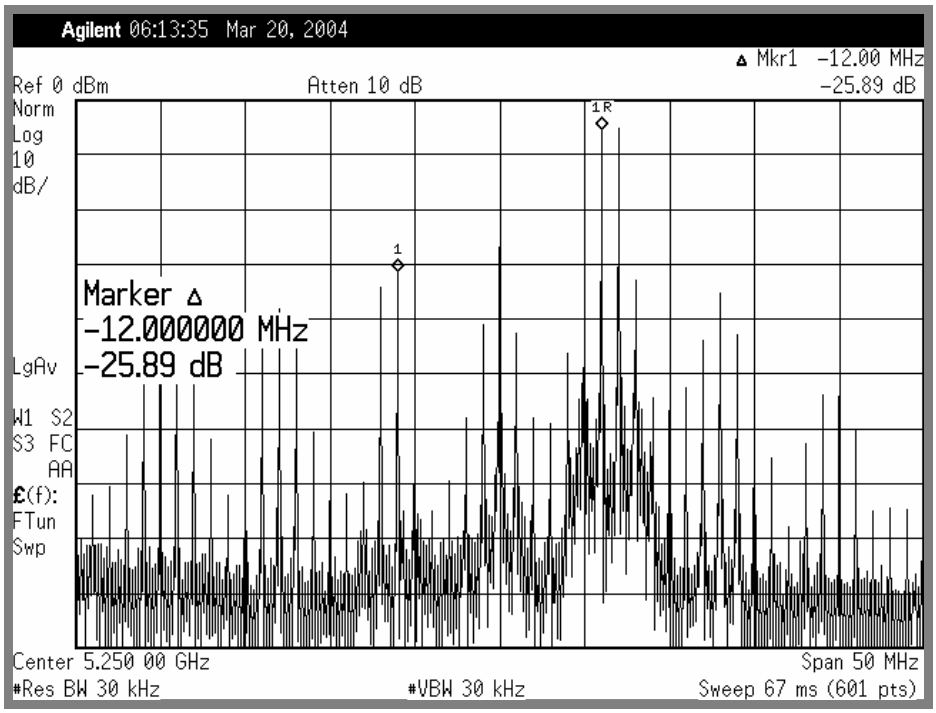


Fig. 93 Output Spectrum of Two-Tone Test for 5GHz TXFE-HL Package Design

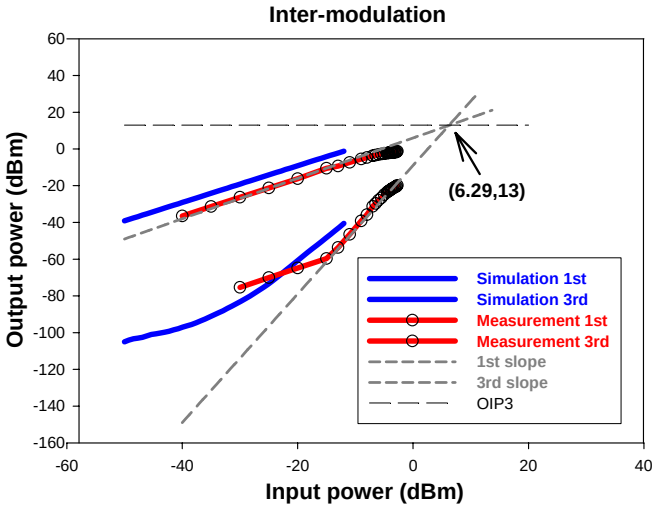
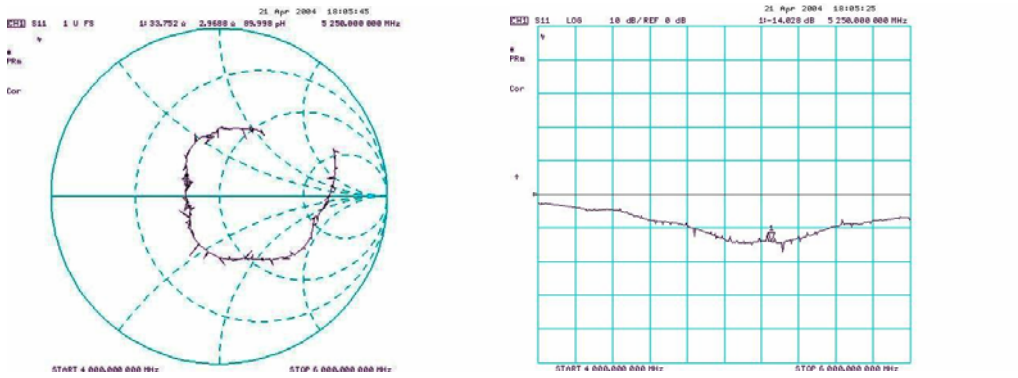


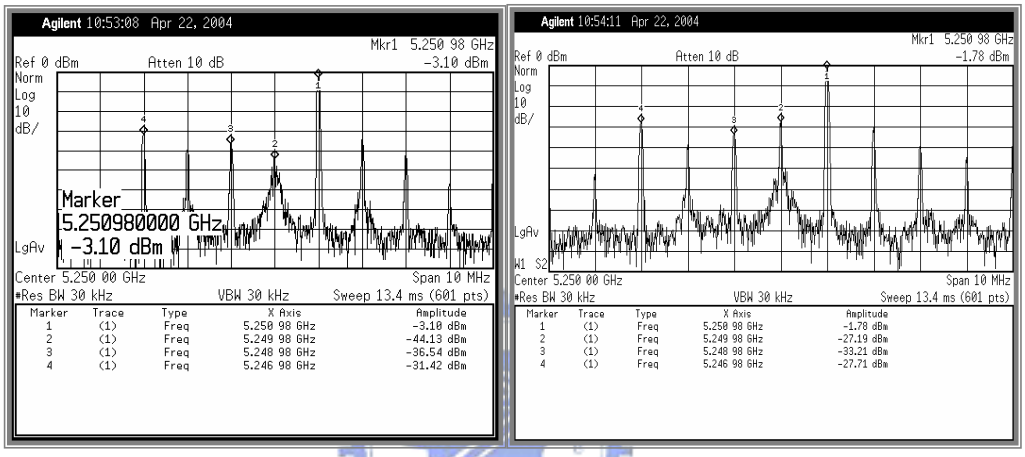
Fig. 94 Two-Tone Test & IP3 (TXFE-HL Package Design)

After off-chip matching, the RF output return loss could be improved to 14dB as shown in Fig. 95. Fig. 96 also shows the output power increases by about 1.3dB after off-chip matching.



(a) (b)

Fig. 95 RF Matching Improvement (a) Smith Chart (b) LOG



(a) (b)

Fig. 96 Output Spectrum (a) Before (b) After Off-Chip Matching

Finally, Fig. 97 shows the transmitted spectrum of a 64-QAM OFDM signal against the spectrum mask defined by the 802.11a standard. With a total output power of -6.58dBm, the output spectrum is well below the spectrum mask, indicating a good linearity margin.

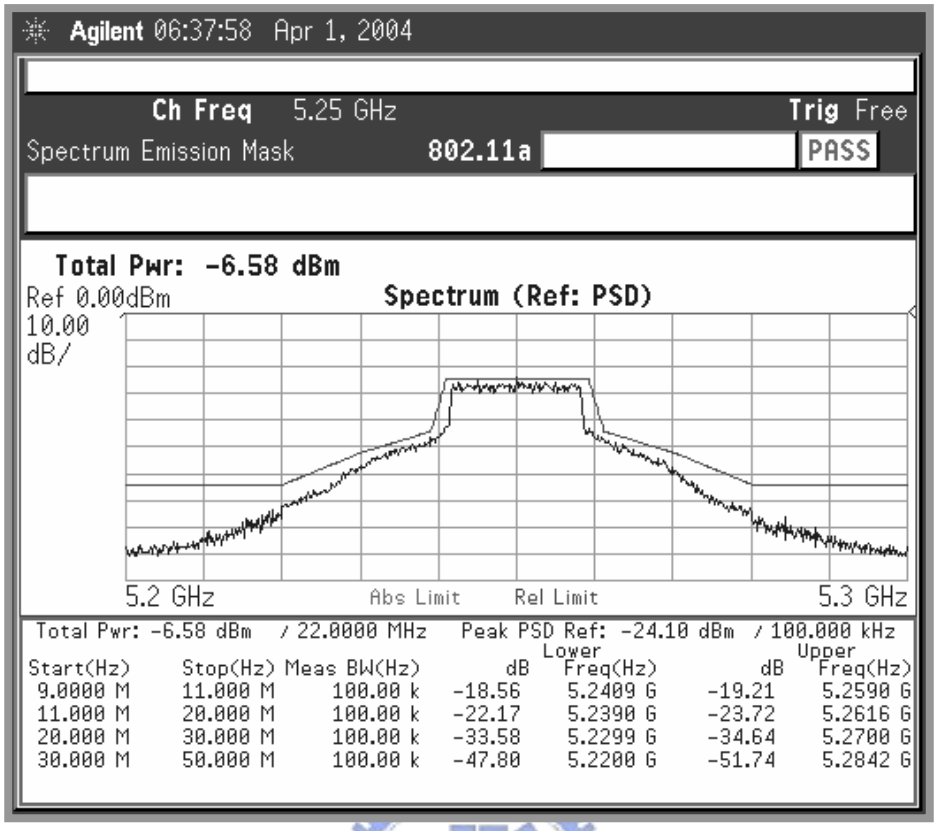


Fig. 97 Transmit Spectrum Mask for 802.11a 54Mb/s, 64-QAM Signals

6.7 Measurement Results of 5GHz TXFE-LP

Another design of the TXFE is fabricated only for package testing. Fig. 98 shows the layout and the die area is 2020*2000 um^2. And this time the die includes a new structure of quadrature mixer with wide-swing Sooch current mirror bias, a differential-to-single circuit, and finally a single-ended pre-amplifier. And Fig. 99 is the overview of chip on PCB with two transformers soldering together.

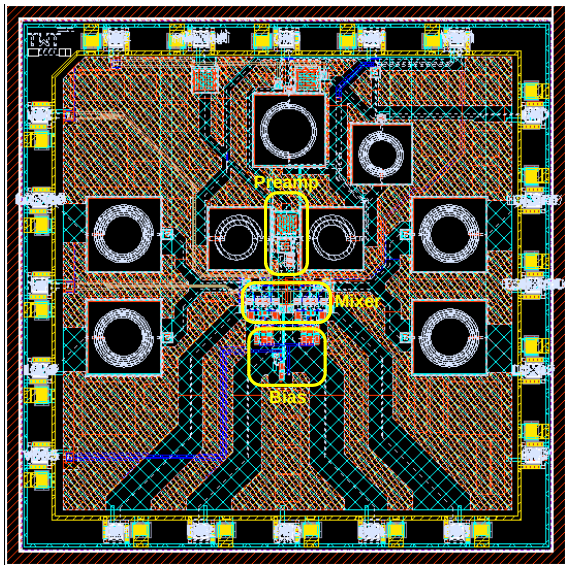


Fig. 98 Layout of 5GHz TXFE-LP (Package Design)

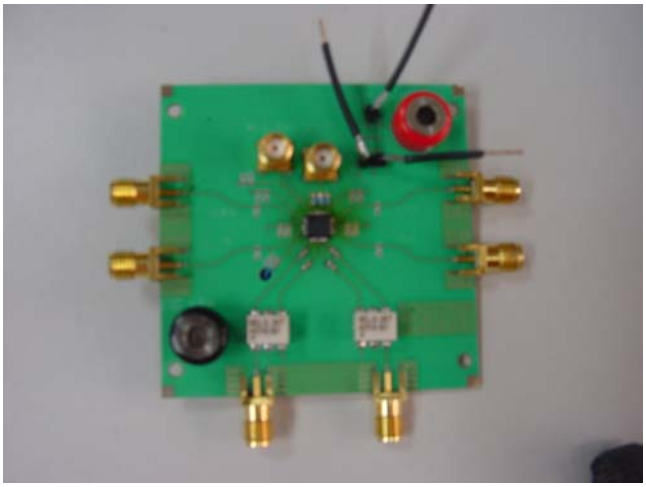


Fig. 99 Overview of Chip On PCB (TXFE-LP)

Fig. 100 shows the measured output spectrum with the same condition as previous setup. The LO matching and RF output matching are shown in Fig. 101 and Fig. 102. The return loss is 8.6dB for LO input and 10.6dB for RF output port.

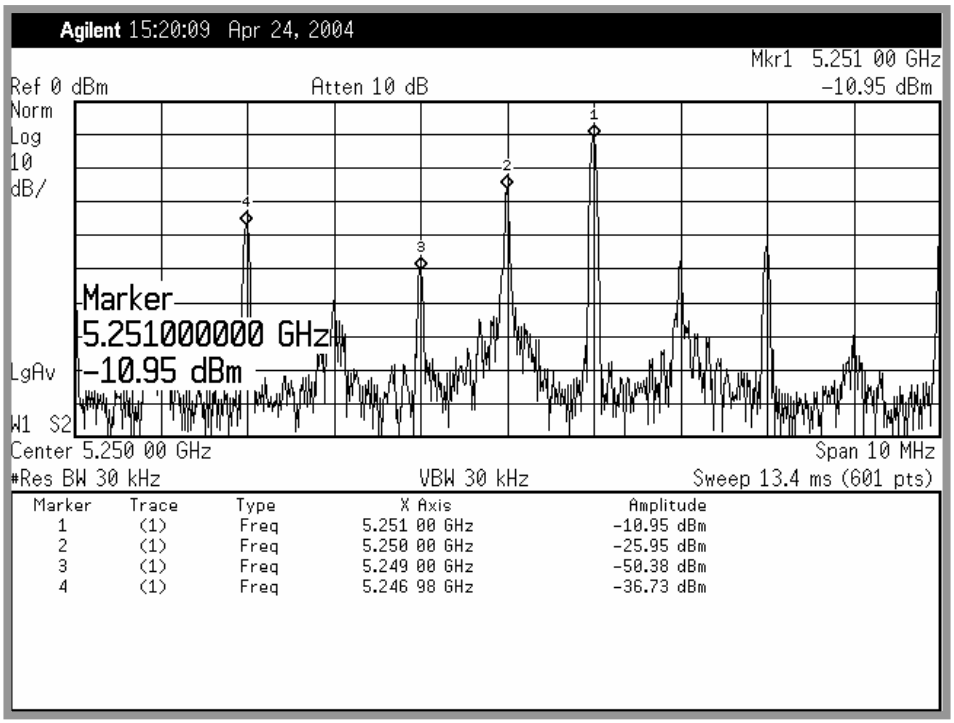
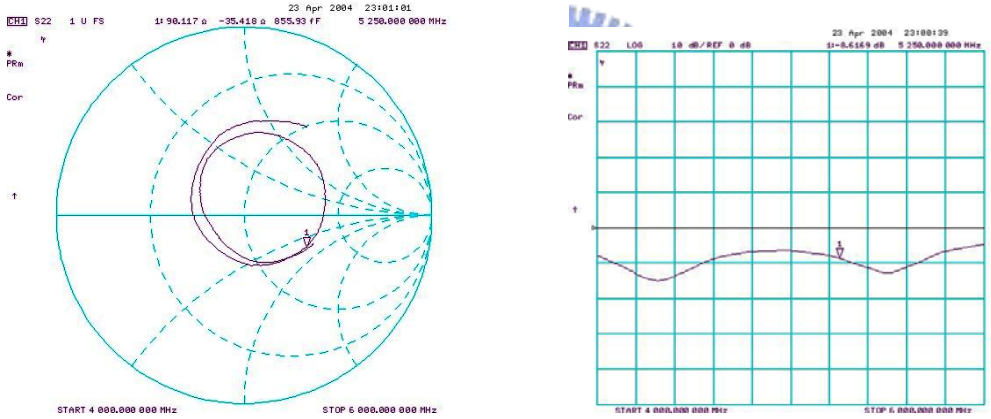
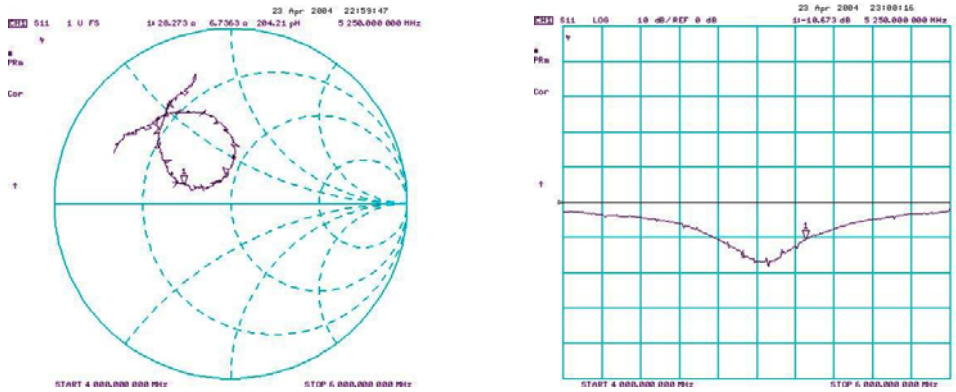


Fig. 100 5GHz TXFE-LP Output Spectrum for Package Design



(a) (b)

Fig. 101 LO Matching (a) Smith Chart (b) LOG



(a) (b)

Fig. 102 RF Matching (a) Smith Chart (b) LOG

Fig. 103 shows the measurement result of conversion gain with LO frequency sweeping from 3.2GHz to 6.2GHz. The measured frequency response of conversion gain is much different from simulation results for either the gain performance or the bandwidth. The gain is 16dB less than simulation result and besides, it doesn't exhibit any peak value at any frequency band. This might be caused by some reasons and we will verify later. Fig. 104 shows the measured result of conversion gain versus input power. Once again, the gain performance is much different from the simulation result although the P1dB is better. And it also indicates the phenomenon of gain-peaking.

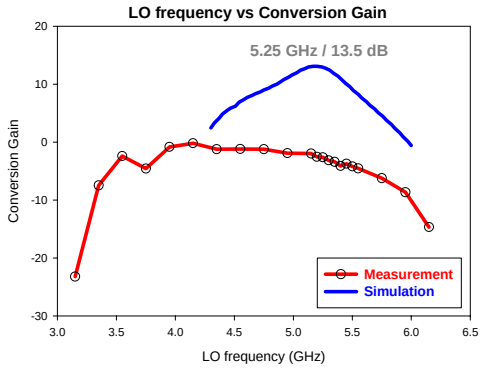
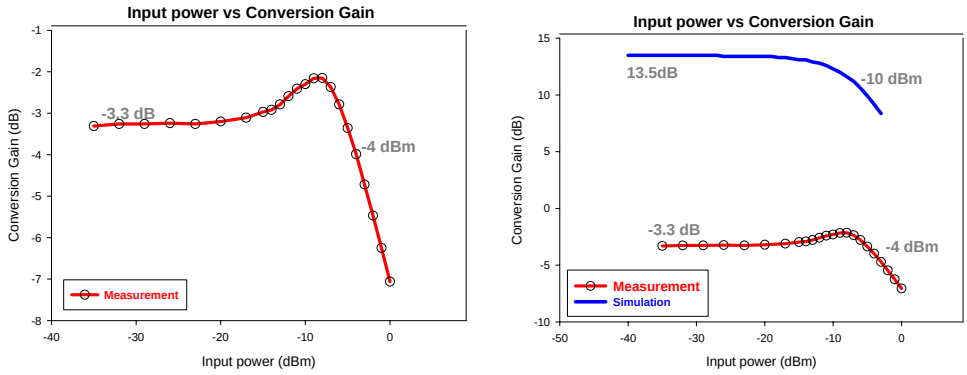


Fig. 103 LO Frequency vs. Conversion Gain (TXFE-LP Package Design)



(a) (b)

Fig. 104 Input Power vs. Conversion Gain (TXFE-LP Package Design)

The probable location causes the difference between simulation and measurement is over the interface of mixer and differential-to-single stage which is illustrated in Fig. 105. Since the compensated capacitance C_c is connected to the global GND, the induced parasitic capacitance is hard to estimate precisely. And in order to test single module by oneself, we reserve an I/O pin at the gate of M1, however the package bondwire will induce considerable parasitic inductance and owing to the imprecise package model, this would be another “offender.”

Besides, the multi-gm mixer adopts large number of device size ratio to perform the offset of gm characteristic, and this large N exceeds the limit of RF model and thus forces us to replace with Mixed-mode MOS to implement which is of risk in RF design. And the large device size ratio also makes the circuit very sensitive to process variation. Fig. 106 shows the post-simulation result by adding the bondwire inductor and changing the capacitance between Cc and board ground which indicates that the simulation result is similar to the measurement result.

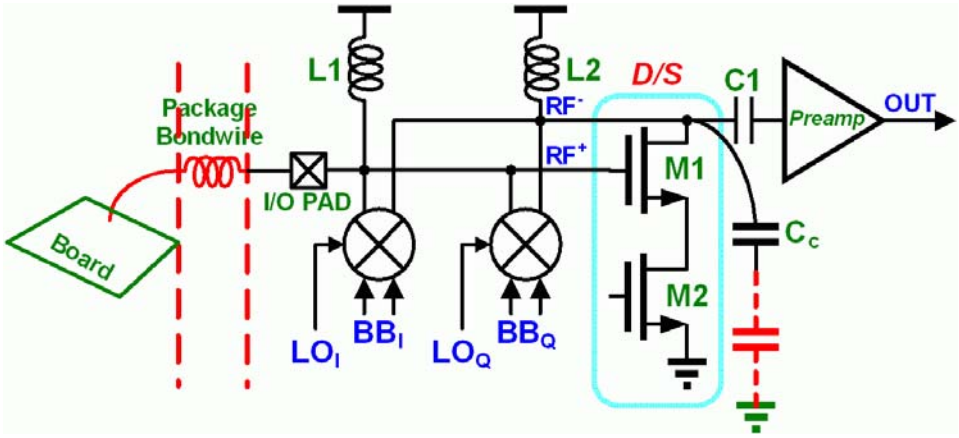


Fig. 105 Differential-to-Single Converter of 5GHz TXFE-LP Circuit

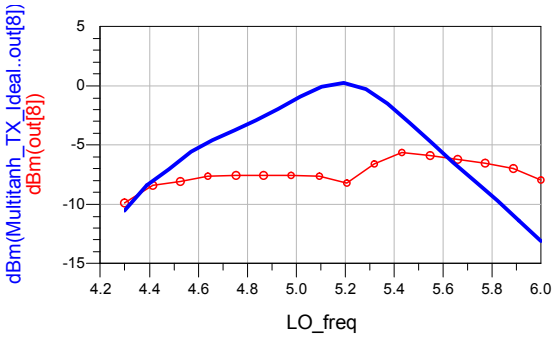


Fig. 106 Post-Simulation of the TXFE-LP Design

Another reason is the phase delay mismatch of the differential signals: RF+ and RF- which is caused by the RC-delay at the drain of M1. Ideally, the inductors L1 and L2 would resonate the parasitic capacitance at the gate and the drain, but any inaccurate estimation of parasitic effect will induce considerable phase delay, resulting in degrading of D/S performance. Fig. 107 is the phase post-simulation results of the differential signals, which indicates the phase difference of the differential signals is not 180 degree anymore.

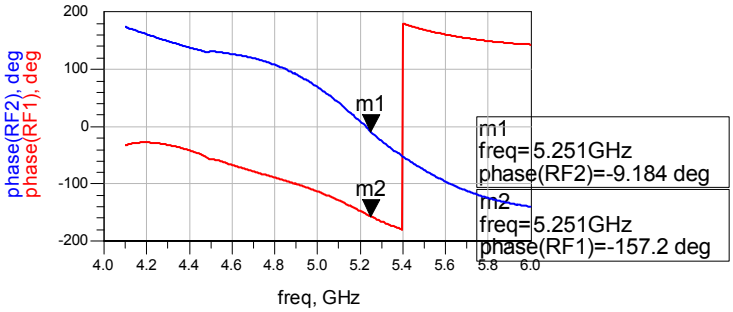


Fig. 107 Phase Post-Simulation of the Differential Signals

6.8 Summary

TABLE 9 summarizes the measurement results of 5GHz TXFE-HL for on-wafer and package testing. It also lists the specification of 802.11a standard and a reference publication. We can see a good agreement between our specification and the publishing paper. At the same time, since we reserve some design margin, although the measurement is not as respect but which can still meet the specification indicating that this is a successful circuit design.

TABLE 9 Measurement Summary and Comparison

Parameters	On-wafer Simulation	On-wafer Measurement	Package Simulation	Package Measurement	802.11a. Specification	[7]2003 JSSC Razavi
Frequency Range	RF=5.15-5.35GHz	RF=4.75-5.25GHz	RF=5.15-5.35GHz	RF=4.35-5.45GHz	RF=5.15- 5.35GHz	RF=5.15- 5.35GHz
Power Consumption				68mW		135mW
Conversion Gain	11.6 dB	7.2 dB	13.88 dB	8.6 dB	7 dB	N/A
Input-P1dB	-4.9 dBm	~-6 dBm	-5.1 dBm	-5.3 dBm	-5 dBm	N/A
Output P1dB	5.7 dBm	0.54 dBm	7.85 dBm	2.3 dBm	4 dBm	5dBm
IIP3	7.7 dBm	N/A	7.0 dBm	6.29 dBm	N/A	N/A
OIP3	16.3 dBm	N/A	17.3 dBm	13 dBm	14.5 dBm	15dBm
RF Return Loss	25 dB	-12 dB	24 dB	-9 dB	<-15 dB	N/A
LO Return Loss	30 dB	dB	22 dB	-15 dB	<-15 dB	N/A
Side band rejection	109 dB	33 dB	55 dB	33 dB	N/A	50 dB
Carrier rejection	94 dB	40.8 dB	40 dB	27 dB	<-15 dB	38 dB

Chapter 7

Conclusions and Future Works

7.1 Conclusions

Two CMOS transmitter front-ends for 802.11a standard have been implemented by UMC 0.18um 1P6M process. Each of the transmitters front-end adopted different skills to linearize the mixer. The first one employs triode region MOS as source degeneration of gm-stage, while the second one employs multi-gm current addition technique. The measurement results indicate that the TXFE-HL circuit has linearity performance of -5.3dBm input P1dB, 2.3dBm output P1dB, 6.29dBm input IIP3 and 13dBm output IIP3, and it also achieves 8.6dB power conversion gain when consumes power of 68mW. The carrier suppression is 27dB while the side-band rejection is 33dB. And it also passes the transmit spectrum mask for 802.11a 54Mbps, 64-QAM OFDM signals.

As for the TXFE-LP circuit, due to the process variation, the imprecise parasitic capacitance induced at GND or VDD pads and imprecise package model, the measurement result is different from the simulation. However, it still has proper

function to up-converse a base band signal to RF band.

Finally, a novel architecture of dual-band transmitter front-end has been proposed. This transmitter adopts single mixer followed by two preamplifiers operated at 2.4/5GHz respectively. In this way, the current dissipation and chip area could be saved. The simulation results indicate this circuit achieves 7dB power conversion gain with input P1dB of -5dBm for 5GHz and 2.4GHz, respectively, and it consumes only 44mW at 1.8V power supply.

7.2 Future Works

As for the future works, we first divide the circuit into several segments, and discuss how to improve the performance for each segment, respectively. The main objectives are still multi-band, low power, high linearity and single chip.

First, the two linearization mechanism employed in gm-stage of mixer could be made a more detail comparison, and even try to combine both the linearization mechanism to achieve higher input P1dB [32][33]. Besides, LC-tank current folded technique [34] must be utilized to apply the trend of shorter channel inducing lower supply voltage design. Fig. 108 expresses the operation of this technique. The stack of three MOS stages can be reduced to only one MOS by replacing the current source with the LC-tank providing the DC current for gm-stage and switching stage of mixer and the gm-stage is changed from NMOS to PMOS. In this way, the mixer

can be adopted for low power supply application.

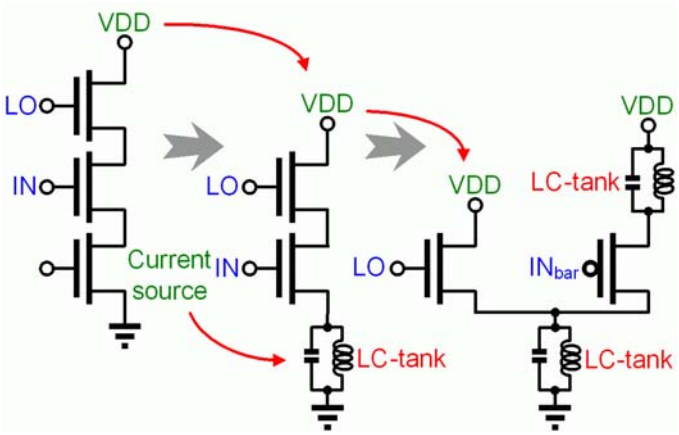


Fig. 108 Design for Low Power Supply Application

On the other hand, since the two preamplifiers in dual-band transmitter front end proposed in this thesis are always on, a high frequency switch circuit must be utilized to save more power consumption, so that the bias current of preamplifier could be permitted higher to gain higher output power. Besides, as we know that the 802.11a operates at three bands, and each band requires different output power, so a programmable power mechanism as shown in Fig. 109 also needs to be designed [7].

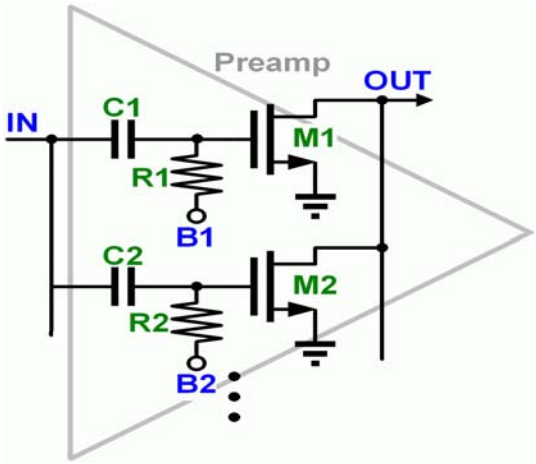


Fig. 109 Binary Weighted Programmable Preamplifier

At last, in order to mitigate the difficulty on measurement, we would suggest implementing an on-chip VCO.

Fig. 110 illustrates another architecture for multi-band application. By utilizing the dual-band transmitter proposed in this thesis, the base band signal can be up-conversed by two step to obtain 3~9GHz RF output signals.

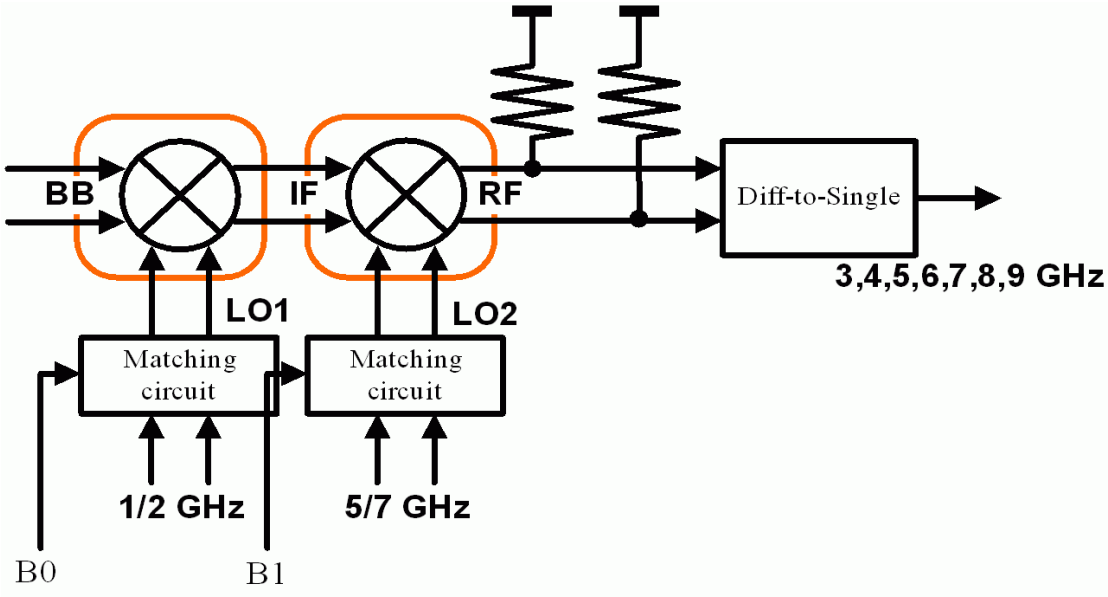


Fig. 110 Multi-Band Architecture

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適用於 802.11a/b/g 無線區域網路之 CMOS 前端發射器設計