國 立 交 通 大 學

電子工程學系　　電子研究所

碩 士 論 文

研究鍺表面鈍化於未來鍺通道金氧半場效電晶體之效能影響

Investigation of the Effect of Surface Passivation on the Performance of Future Ge-channel MOSFETs

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摘要

此論文中，首先我們分析二氧化鍺表面鈍化的鍺電容。透過電導和費米能階移動效率的方法說明能帶缺陷密度可因300度的氫氣氮氣混合之熱退火而被有效降低，而在能隙中央位置的值大約在$5\times10^{11}cm^{-2}eV^{-1}$左右。透過$\ln\tau$對$E_T-E_i$圖型的外插，我們可萃取出缺陷的電子或電洞補捉截面積，分別是$2.7\text{-}4.2\times10^{-16}cm^2$和$7.8\text{-}9.6\times10^{-16}\ cm^2$。並透過低溫量測萃取出鍺能隙中的缺陷分佈。

根據電容的經驗，我們成功地製作出搭配原子層沉積三氧化二鋁高介電層之反轉式(inversion-mode)純鍺P型場效電晶體。表面鈍化與無表面鈍化的樣品其載子遷移率分別為矽普遍曲線(universal curve)之1.7倍與1.3倍。而由於300度的氫氣氮氣混合之熱退火可有效降低缺陷密度，使我們得到較佳的電流開關比(3.3 orders)與次臨界擺幅(170mv/dec)。透過電荷幫浦(charge pumping)量測，估計出能隙中央位置的平均缺陷密度與電子和電洞補捉截面積的幾何平均，並與分析電容所萃取出來的結果一致。利用

我們的實驗結果分析在鍺表面加入二氧化鍺的優缺點。好處是可得到較低的缺陷密度與較高的載子遷移率;缺點是可靠度表現較差，有較嚴重的載子捕捉現象與次臨界擺幅劣化現象。

最後，我們製作出搭配原子層沉積三氧化二鋁高介電層之反轉式(inversion-mode)純鍺N型場效電晶體。我們先用實驗證明SiO_2/GeO_2絕緣比SiO_2絕緣有更低的接面逆偏漏電，而同樣是SiO_2/GeO_2絕緣700度比500度退火有更低的接面逆偏漏電。元件的電流開關比可到達三個數量級(W/L=100μm/10μm)，不過卻有很大的源極與汲極寄生電阻。N型場效電晶體比起P型場效電晶體有較差的電性表現，將可能原因整理出來分別是:在介面處帶有大量負電(受體形式介面缺陷)造而嚴重的庫倫散射、反轉層電荷流失、與很大的寄生電阻。

Investigation of the Effect of Surface Passivation on the Performance of Future Ge-channel MOSFETs

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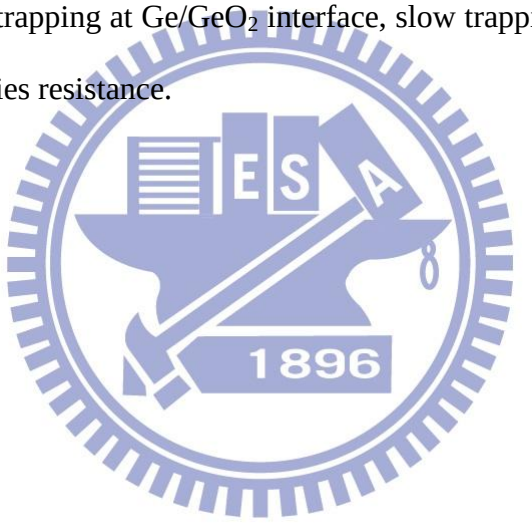
Abstract

In this thesis, firstly, high-k/GeO_2/Ge capacitors were fabricated and analyzed electrically. Interface state density was shown to be reduced effectively through 300℃ 30 minutes FGA, with value about 5×10^{11} $cm^{-2}eV^{-1}$ near the midgap from either conductance or Fermi-level efficiency method. By extrapolation of $\ln\tau$ vs $(E_T - E_i)$ plot, σ_n and σ_p were 2.7-4.2$\times10^{-16}$$cm^2$ and 7.8-9.6$\times10^{-16}$ cm^2 respectively. Besides, D_{it} distribution in the bandgap was extracted by means of low temperature measurement.

Secondly, from the experiences in high-k/GeO_2/Ge capacitors, we successively demonstrated the device characteristics of the inversion-mode Ge p-FETs with ALD-Al_2O_3 gate dielectrics. GeO_2 passivation as well as no passivation sample had their high field mobility 1.7X and 1.3X higher than the Si universal curve respectively. Also, better on/off ratio (3.3 orders) and subthreshold swing (170mv/dec) were attained for Ge p-FET after 300℃ 30 minutes FGA, resulted from lower reverse bias junction leakage and better interface quality. Then, charge pumping was applied to reconfirm the results in Chapter two. $\overline{D_{it}}$ after FGA between $E_{em,e}$ and $E_{em,h}$ is $4.2\times10^{11}cm^{-2}eV^{-1}$ and $\sqrt{\sigma_p\sigma_n}$ was 5.4×10^{-16} cm^2 for 500℃ GeO_2 passivation sample. Furthermore, pros and cons of adding the GeO_2 layer were summarized: lower D_{it} value verified from either charge pumping or gated diode

measurement made the mobility higher for GeO_2 passivation sample, while it suffered from more carrier-trapping due to border traps at the GeO_2/Al_2O_3 interface and more severe subthreshold swing degradation.

Finally, device characteristics of inversion-mode Ge n-FETs with ALD-Al_2O_3 gate dielectrics were also demonstrated. SiO_2/GeO_2 isolation as well as 700℃ 30s dopant activation did we obtain the lowest reverse bias junction leakage of 1.9×10^{-2} A/cm^2 at 2V and magnitudes of the rectifying ratios reached 4.2 orders. On/off ratio of our n-FETs (W/L= 100μm/10μm) reached 3 orders but series resistance larger than 1.7kΩ was extracted. It was concluded that much severe n-FET performance degradation compared with p-FET could be explained in terms of fast trapping at Ge/GeO_2 interface, slow trapping by GeO_2/Al_2O_3 border traps and parasitic S/D series resistance.



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Chapter 1

Introduction

1.1 Scaling of CMOS Technology and Research Motivation

Not only the 1st transistor invented in 1947 by Brattain, Bardeen and Shockley but the 1st integrated circuits developed in 1958 by Kilby were both made of Germanium. However, the 1st MOSFET fabricated in 1960 by Kahng and Atalla was made of silicon; they showed good quality and stability of Si/SiO_2 interface while oxide of Germanium was soluble in water and thermal instability. Because of plentiful supply of Si, Si-based MOSFETs have become the driving force for the semiconductor industry in the last four to five decades. Despite architecture and working principle of the MOSFET have remained the same, the physical dimensions have been continually reduced to double the number of transistors on a chip every eighteen months according to Moore's Law. The decrease in transistor dimensions has led to increase in microprocessor performance over technology generations. Even so, the conventional device dimension scaling cannot continue forever.

R. Chau, Intel Corporation, has demonstrated the scaling roadmap in the progress of the Si MOSFETs, as shown in **Fig. 1.1**. At 90nm node, substrate engineering and uniaxial strain technologies have been developed to enhance the carrier mobility in the channel. When scaling down to the 45-nm node, high-k materials replacing ultra-thin conventional SiO_2 or oxynitrides are introduced as alternative gate dielectrics for leakage concerns and reliability issues. As devices are further scaled down, unfortunately, performance is no longer keeping up with the scaling trend, as shown in **Fig 1.2**, which is related to the increase in parasitic charges as the devices are scaled down.

Many novel device structures and materials are continuously proposed and explored eagerly, in order to mitigate the huge scaling pressure required to improve device

performances. Alternatives to boost performance include Ge/III-V channel materials, carbon nanotubes, semiconductor nanowires and graphene. Among above advanced researches, the feasibility of integrating various prevailing high-*k* dielectrics with high mobility channels is the most promising since they can be integrated into a Si CMOS front-end process more easily than the other alternatives.

As shown in **Table 1.1**, the material properties of bulk Si, Ge, GaAs, and InAs at 300 K are compared [1]. Since Ge possesses 3× electron and 4× hole mobility than those of Si, it is considered the potential candidate for p- and n-channel materials of high performance logic devices. Actually, Ge will not be used for long channel transistors where mobility determines the drive current or for those short channel devices for which the high field saturation velocity influences the drive current, **Fig 1.3**. Nevertheless, Ge will be used in very short channel MOSFETs (beyond or at 22 nm node) exhibiting (quasi-)ballistic transport. According to M. Lundstrom [2], the drive current is determined by the carrier injection probability which is related to the mobility at low field, and that explains why Ge MOSFETs are expected to have a higher drive current than Si MOSFETs for very short channel device.

Up to date, the promising device characteristics of Ge channels with either HfO_2 or Al_2O_3 high-*k* dielectrics have been continually demonstrated, and the long channel performance of unstrained device overtakes the universal hole mobility of Si transistor 3 times at high electric field [3]. Therefore, it is believed the MOS capacitor and device properties integrating various high-k dielectric materials onto Ge substrates are worth being studied.

1.2 A SWOT Analysis of Germanium for Advanced CMOS

In order to enhance the CMOS performance continuously, Cu/low-k and high-k/metal gates have already been used, and it is predicable that the past few decades Si channel is going to be replaced by other high mobility materials. Germanium has emerged as an exciting alternative material for high-performance scaled CMOS. However, many difficulties are still

unsettled. The feasibility of Ge is discussed through the SWOT analysis [4].

Strength

The most obvious strengths of Germanium are its high carrier mobility and low band gap nature. Bulk hole mobility (1900cm^2/Vs) of Ge is the highest among all of the known semiconductor material, while bulk electron mobility (3900cm^2/Vs) is also high enough to allow matched P- and n- MOSFET performance. Also, the lower band gap (0.66eV) characteristic enables to lower the Schottky barrier height and thus lower the contact resistance than the Si counterpart.

Ultra shallow P+/n junctions can be achieved by a pre-amorphization implant (PAI) prior to the B implant. PAI can not only suppress the channeling effect but enhance the activation level 20-fold to $2\times10^{20}cm^{-3}$. One key advantage of Boron doping in Germanium over Si is Boron being almost diffusionless at the 400℃~600℃ temperature range required for dopant activation, so that junction depth < 20nm can be achieved.

Besides, mobility of Ge MOSFET can be further enhanced through strain. (100) substrates with uniaxial strain for $[-1\ 1\ \sqrt{2}]$ channels can improve the hole mobility in Ge by 2.2×. [5]

Weakness

Several critical aspects of Ge technology still need to be solved, including low n-type doping, small band gap, and large lattice mismatch with Si, etc.

Low solid solubility and fast diffusion of n-type dopant in Ge is the main reason for low activation level S/D doping (<5-6×1019/cm3), which causes larger sheet resistance and contact resistance and largely degrades the NMOSFET performance.

Band-to-band tunneling or trap-assisted tunneling cause serious junction leakage problem for the small band gap material, especially for high S/D doping required for

aggressively scaled down devices. Therefore, the junction leakage is a real concern and alternative device geometries, such as thin epi-Ge on Si, Ge-on-insulator, or FinFETs are necessary.

Virtual substrates of epitaxial Ge on bulk Si wafers offers significant advantages over bulk Ge, such as lower cost, greater mechanical strength, lighter weight and increased compatibility with existing Si processing equipment. However, lattice mismatch between Ge and Si is 4%, which may cause serious dislocation problems for epitaxial Ge on the mandatory Si substrate. It is reported that the final defect density is an inverse function of the Ge layer thickness, so that threading dislocation density (TDD) in 100 nm thick layers cannot get below 4-5×$10^{9}$$cm^{-2}$ (4×10^{8} cm^{-2} for 300 nm layers) [6].

Opportunities

Although the performance of Ge nMOSFETs is still unsatisfied, CMOS might come in reach by combination with III/V materials such as InGaAs with their extremely high electron mobility. An attractive opportunity is the combination of a similar gate stack starting from Si as the passivation layer, with selective deposition of both Ge and III/V channel materials in trenches on STI Si substrates. Moreover, Ge devices other than MOSFETs can offer added functionality such as integrated optical interconnects and other optical components; low-thermal budget Ge FETs can be integrated after BEOL for 3D-IC [7].

Threats

Even the n-type doping, Ge layer quality and passivation of Ge surfaces issues can be solved, whether or not Ge will be used is still an uncertainty from the following three aspects: timing, cost, and junction leakage. 1. Can the Integrated Device Manufacturers wait until Ge technology has matured enough for integration in manufacturing? 2. Is it worth adding such process complexity? 3. Will Si CMOS finally be beaten by Ge? It seems that Ge can hardly

match leakage performance of Si, as shown in Fig1.3. It is also reported that I_{off} in Ge is 100× higher, but only a slight increase in I_{on} from simulation of a 15 nm L_g device. [5]

1.3 Scope and Organization of the Thesis

The promising high-mobility substrate material, Ge, is investigated in this thesis since great progress in the deposition of high-k materials renews interest in high mobility substrates as a transport channel combined with various high-k dielectrics. One of the largest obstacles of Ge MOSFETs is the high defect density at the Ge dielectric interface, which degrades drive current, alters the threshold voltage, and increases the leakage currents. Therefore, surface passivation of Ge is a key challenge to achieve high performance Ge MOSFETs. The thesis is divided into five chapters and arranged as follows:

Chapter 1, a brief overview of the background and motivation is described. The MOSFET scaling roadmap and the probable ways to boost device performance for next generation are mentioned. Next, one of the most promising alternative channel materials, Ge, is investigated through the SWOT analysis.

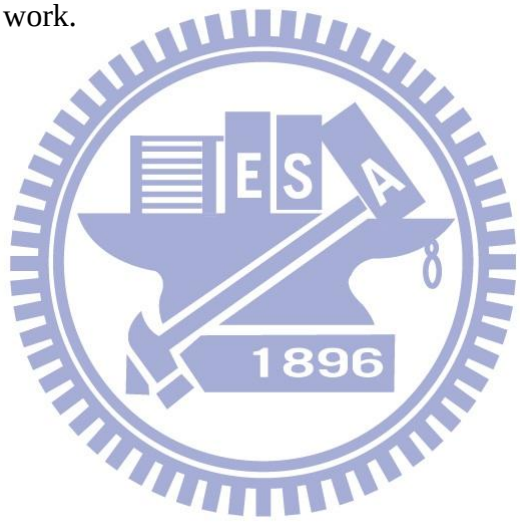
Chapter 2, GeO_2 passivation Ge PMOS and NMOS capacitors with different GeO_2 growing temperature were fabricated, and emphasis was put on obtaining a high quality interface for later application in the MOSFET gate dielectric. Theory of the conductance method was discussed in detail, and utilizing it to extract the interface state density for different passivation sample. Then, the effect of FGA on the admittance behavior of Ge MOS capacitors was investigated. With the help of low temperature measurement, D_{it} distribution in the upper half band gap was illustrated.

Chapters 3, Ge PMOSFETs with and without GeO_2 surface passivation were fabricated. Effect of FGA on the Ge p+/n junction and device electrical characteristic was studied. Also, D_{it} of the two samples was examined by gated-diode and charge pumping measurement, to reconfirm the value of D_{it} extracted by the conductance method reasonable. Then, mobility

extracted from split-CV of our samples was compared with other published data. Finally, CVS was done to test reliability of the two samples.

Chapter 4, Ge NMOSFETs with different thickness GeO_2 surface passivation were fabricated, and we showed that SiO_2/GeO_2 isolation layer was essential to reduce junction leakage current. Then, mobility extracted from split-CV of our samples was compared with other published data. Again, charge pumping and gated diode measurement were done to attain the interface information while CVS was done to observe different trapping behaviors of Ge NMOSFETs with different GeO_2 thickness.

Chapter 5, we summarized the experimental results in the thesis, gave the conclusions and suggestions for future work.



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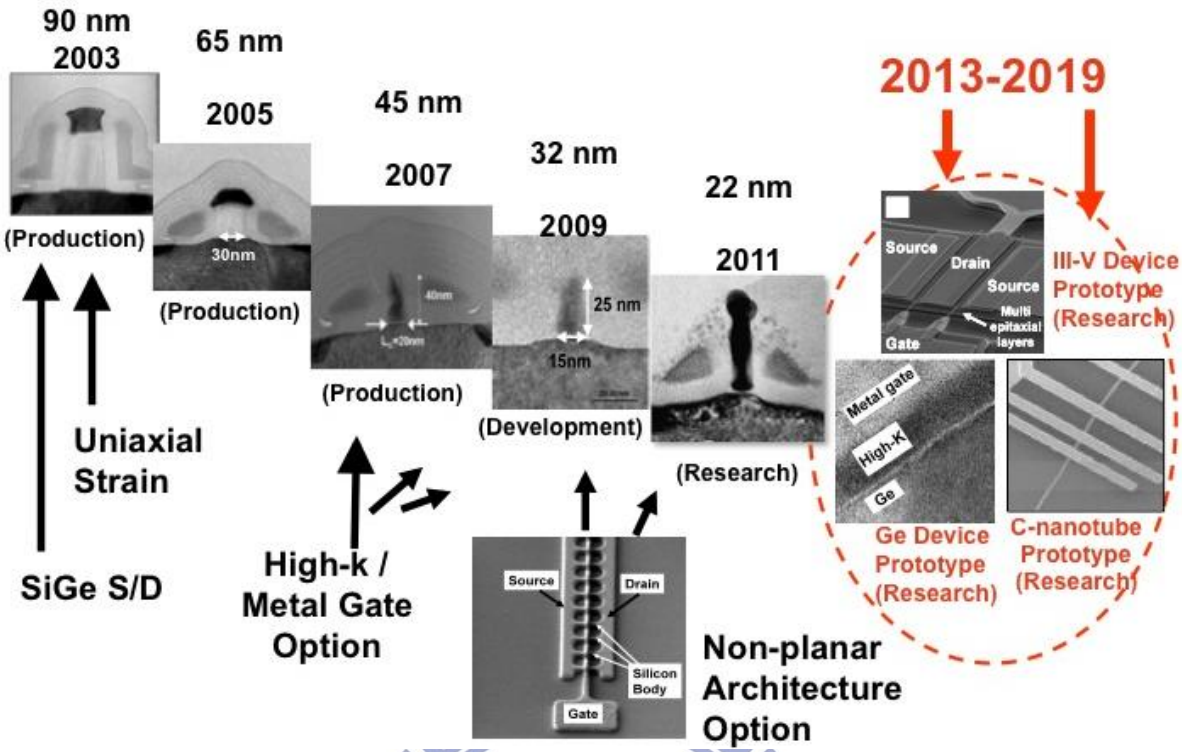

Fig. 1.1 Transistor scaling and research roadmap is demonstrated by R. Chau, Intel Corp.

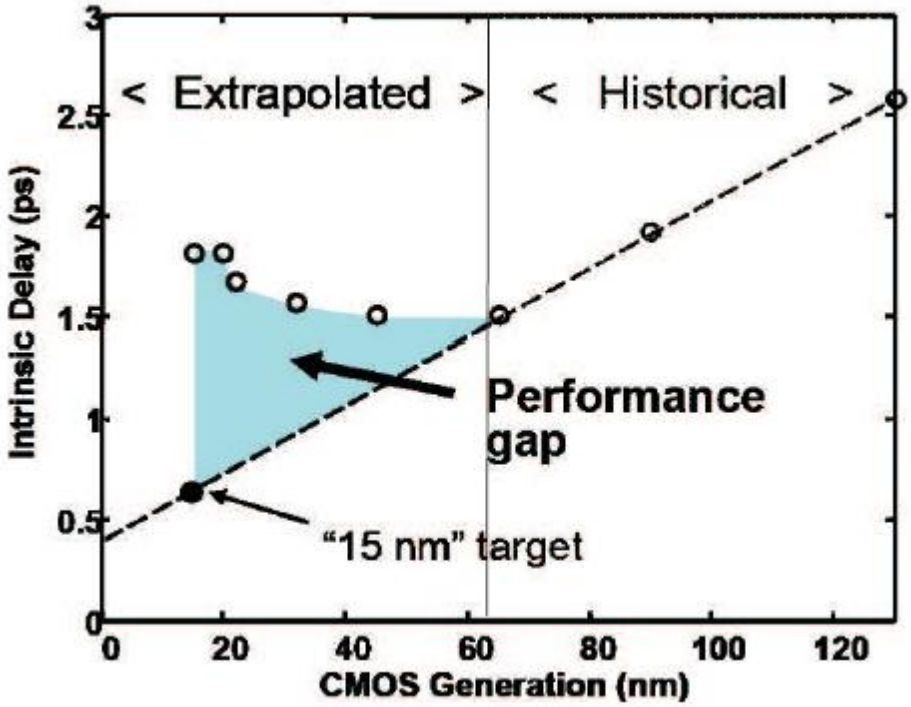

Fig. 1.2 Illustration of the performance gap between projected performance and actual performance for CMOS circuit downscaling.

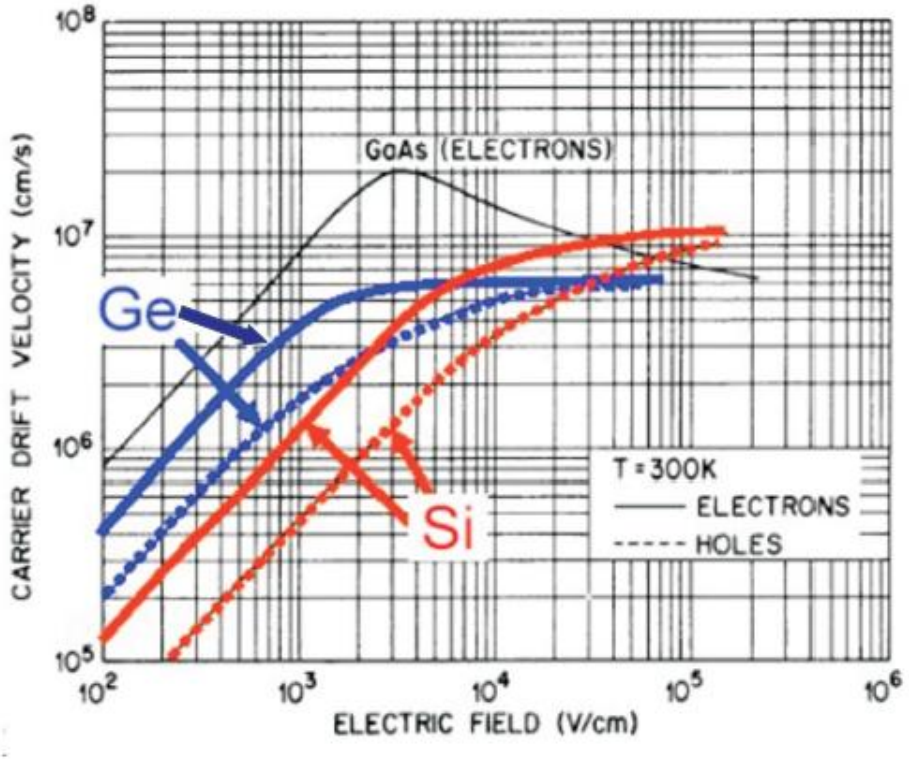

Fig. 1.3 Carrier velocities as a function of electric field for Ge, Si and GaAs are shown. The mobility is the slope of drift velocity and the electric field.

	Ge	Si	GaAs	InAs
Bandgap (eV)	0.66	1.12	1.42	0.35
Hole mobility (cm^2/V-S)	1900	450	400	460
Electron mobility (cm^2/V-S)	3900	1500	8500	33000
Conduction band DOS Nc (cm^{-3})	1.04E19	2.8E19	4.7E17	8.7E16
Valance band DOS Nv (cm^{-3})	6E18	1.04E19	7E18	6.6E18
Lattice constant (Å)	5.646	5.431	5.653	6.058
Dielectric constant	16	11.9	13.1	15.2
Melting point (°C)	937	1412	1240	942
Dopant activation limit (cm^{-3})	P : (4-6)E19	P : (1-2)E20	Si : (4-6)E18	Si : (1-3)E18

Table 1.1 Material properties of bulk Ge, Si, GaAs, and InAs at 300 K are compared.

Chapter 2

Atomic-Layer-Deposited Al_2O_3 Dielectric Films on the Bulk GeO_2 Passivation Germanium Substrates

2.1 Introduction

High-k Al_2O_3 is considered a potential alternative gate dielectric material on Si substrates for application to metal oxide semiconductor field effect transistors (MOSFETs) because of its wide band gap energy (ca. 8.8eV), large conduction/valance band offsets, and high thermodynamic stability. Several reports have described the characteristics of ALD-Al_2O_3 dielectric films grown on Si using trimethylaluminum [TMA, Al $(CH_3)_3$] as the precursor and H_2O as the oxidant because of the excellent ALD mechanism and broad process window [1], [2].In recent years, many investigators have studied the deposition of ALD-HfO_2 high-k layers on high-mobility Ge substrates [3] using a variety of oxidants in efforts aimed at enhancing the driving current in MOSFETs. However, the primary obstacle affecting the characteristics of high-k/Ge structures is the presence of GeO_x native oxides which degrades the Ge device performance, leading to higher value of D_{it} and thus lower mobility. Therefore, many efforts have been devoted to surface passivation of the non Si/SiO_2 interface, including incorporation of ultra-thin Si [4], AlN_x [5] and GeON [6]dielectric interlayers, plasma treatment with NH_3 or PH_3 [7][8], and more recently, GeO_2 passivation[9]. In this thesis, GeO_2 passivation is adopted to passivate the Ge surface.

Interface passivation is a key challenge for realizing Ge/III-V CMOS, and how to evaluate the interface quality correctly is of great importance. The bandgap of Ge and III-V substrates also affects the admittance characteristics in many aspects which are obviously different from the Si-based devices. For that reason, correct interpretation of the routinely used admittance characteristics becomes of paramount importance in Ge/III-V technology.

The admittance of an MOS structure is measured as a function of DC gate voltage and frequency by applying a small AC signal and DC bias voltage on the MOS capacitor. Admittance characteristics (C-V and conductance characteristics) are frequently used to characterize crucial parameters of Si MOS capacitors such as the flatband voltage, fixed charge, effective oxide thickness, doping level, and most importantly, the semiconductor dielectric interface quality.

In this chapter, low-frequency C-V curves for high frequency measurement of Ge MOSCAPs are first shown, followed by the conductance method to extract D_{it} and the estimation of capture cross section based on the Shockley-Reed-Hall theory. Next, the admittance behaviors affected by FGA are discussed through the slope of the C-V curve, G_p/ω data, and more intuitionally, the Fermi level movement efficiency. Finally, D_{it} distribution across the bandgap is illustrated with the help of low temperature measurement.

2.2 Fabrication of ALD-Al_2O_3/GeO_2/Ge MOSCAP

(100)-oriented P-Ge substrate and N-Ge substrate with doping concentration 2E15cm^{-3} (resistivity ca. 2Ω·cm) and 1.5E14cm^{-3} (ca. 10Ω·cm) respectively were used for MOSCAP fabrication. Before gate dielectric formation, all of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide, followed by a thin GeO_2 layer being formed to passivate the Ge surface, with oxidation condition 500℃ 10s, 550℃ 10s on p-Ge and n-Ge. Next, an 80 cycles ALD-Al_2O_3 thin film was grown on each sample at 160℃. Then, 4000 Å Al was deposited by thermal coater and the capacitors front electrodes were patterned through lithography and etching, while a thermal coater 4200 Å Al layer was deposited as the backside contact.

Forming gas annealing (FGA) at 300℃ in a H_2/N_2 (5%) mixed ambient for 30 minutes was performed to investigate the effect of FGA on electrical characteristic.

The process flow and device structure are shown in **Fig. 2.1**.

2.3 Admittance Behavior of Ge MOSCAP

For state-of-the-art Si/SiO_2, Si/SiON and even Si/SiO_2/high-k MOS capacitors, interface traps have a negligible contribution to the C-V characteristic and do not interfere with the common parameters extraction. However, this is no longer the case when Si/SiO_2 interface has been replaced by high-k/Ge or III-V structure.

Interface traps alter the admittance characteristic in two ways. Firstly, the interface traps modify the relationship between the gate voltages and interface Fermi level positions, causing so-called stretch-out of the C-V characteristic. Since capacitance is directly determined by band bending (band bending determines C_s), a stretch-out of the C-V results. Secondly, the interface traps contribute admittance to the MOS admittance. Based on the equivalent circuit, the relation between D_{it} and parallel conductance divided by frequency (G_p/ω) is derived.

2.3.1 CV Characteristics of Ge MOSCAP

Relative to the Si MOS capacitor, high frequency measurement of low band gap Ge MOSCAPs shows low frequency CV characteristics, as predicted by Nicollian and Brews several decades ago. **Fig 2.2** depicts the multi frequency and quasi-static CV for different passivation Ge MOSCAPs, with EOT and V_{fb} calculated. Also, minority carrier response times ($\tau_R = \frac{C_D}{G_I}$) [10] are calculated to be 0.07μs and 0.16μs, and the transition frequency $f_{tran} = \frac{C_{dep}}{2\pi C_{ox}\tau_R}(1 - \frac{C_{HF}}{C_{ox}})$, at which the capacitance in inversion is midway between C_{ox} and HF capacitance $C_{HF,}$ are 167KHz and 79KHz for P-Ge and N-Ge respectively.

2.3.2 Conductance Method to Extract D_{it}

The common approaches toward extracting the value of D_{it} for Si MOS capacitors, namely the Terman and high–low frequency capacitance methods cannot be applied to Ge devices adequately because the frequently observed "minority carrier response" causes humps in the CV curve, which largely overestimates the D_{it} value. On the other hand, conductance method is more accurate to extract since the substrate conductance G_{sub} is only contributed from interface density, as seen in equivalent circuit model of **Fig 2.3** [11].

The band diagram of a typical MOS structure is shown in **Fig 2.3(e)**, where a gate voltage V_G is applied between the metal and the semiconductor, which fixes the value of the surface Fermi level. The C-V measurements consist in applying on top of the static gate bias voltage a small sinusoidal voltage with frequency f and amplitude of 25 mV. This small periodic gate voltage causes the bands and the surface potential in the semiconductor to periodically move up and down, causing the interface traps lying around the value of the surface potential to fill and empty. Only if the traps around the surface potential have a characteristic response time that is of the order of the measurement frequency f can they interact with the measurement ac signal and affect the total impedance of the MOS capacitor. The capture and emission of carriers by interface traps is an energy dissipating process due to the time lag of the interface trap occupation compared to the required equilibrium trap occupation, and the lossy capture-emission process of carriers is modeled as a resistor (R_{it}) in series with C_{it}. The circuit can be simplified as in Fig. 2.2 (b),

$$C_P = C_{it}+C_S = \frac{qD_{it}}{1+(\omega\tau_{it})^2} + C_S \,, G_P = G_{it} = \frac{qD_{it}\omega^2\tau_{it}}{1+(\omega\tau_{it})^2} \qquad (2.1)$$

Where $Cit=q^2D_{it}$, $\omega=2\pi f$, f is measurement frequency and $\tau_{it} = R_{it}C_{it} = \frac{1}{V_{th}\sigma N} e^{\frac{\Delta E}{kT}}$, the interface trap time constant. From (2.1), conductance method is easier and the more direct way to extract D_{it} than capacitance based methods, since it is not necessary to know the exact value of semiconductor capacitance C_S. From the circuit model, an important prerequisite is

that capture and emission behavior only occur between the trap and majority carrier band edge; in other words, it is invalid to extract D_{it} when V_G is biases at weak inversion region and will be discuss later in details. Therefore, p-Ge and n-Ge are required to extract the lower half and upper half bandgap, respectively, of the D_{it} profile.

By utilizing (2.2), G_P can be determined from the measurement (C_m and G_m) by eliminating the oxide capacitance.

$$\frac{G_P}{\omega} = \frac{G_{it}}{\omega} = \frac{\omega C_{ox}{}^2 G_m}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.2}$$

Equation (2.1) is valid for an interface trap with single energy level in the bandgap; in reality, interface traps are continuously distributed across the bandgap. If the time constant dispersion and trap energy level distribution across bandgap are taken into account, eq. (2.1) is modified:

$$\frac{G_P}{\omega} = \frac{G_{it}}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \tag{2.3}$$

When G_p/ω is plotted as a function of f, the maximum appears at $f = \frac{1.98}{2\pi\tau_{it}}$, and at that maximum

$$D_{it} = \frac{2.5}{q} \left(\frac{G_P}{\omega}\right)_{Max} \tag{2.4}$$

G_p/ω plots are repeated at different gate voltages to scan trap energies to obtain an interface state density distribution across the bandgap.

It is worthy to note that according to the emission time constant ($\tau = \frac{1}{V_{th}\sigma N} e^{\frac{\Delta E}{kT}}$), the behavior of interface trap time constant as a function of temperature determines the part of interface traps in the bandgap observable in the MOS admittance characteristic. That is, traps located nearer to midgap become observable for higher temperatures while traps more located toward the band edges become observable for lower temperature. For small band gap Ge, midgap traps are able to be observed at room temperature; if decreasing the temperature, the observable energy windows shift toward the band edges as shown in **Fig 2.4**, where the effective density of states of the conduction (N_c) and the valence (N_v) bands, electron and hole

thermal velocity, change in Ge bandgap with temperature are all taken into account.

Fig 2.5 illustrates the G_p/ω versus f plots of our GeO_2 passivation Ge MOSCAPs, and measurement is performed at room temperature. G_p/ω curves are shown at the gate voltages Fermi level is near the midgap where interface states are able to capture and emission with the small signal AC bias. The peak value of each G_p/ω curve corresponds to the interface state density and thus D_{it} as a function of gate voltage can be plotted. A tricky issue then arises, how to transform the D_{it} (V_G) into D_{it} (E) plot? We are able to do so by two different approaches. A first way is to utilize frequency corresponding to the maximum G_p/ω; by the equation $\Delta E = kT\ln(\frac{V_{th}\sigma N}{\pi f})$ combined with the value of maximum value of G_p/ω, D_{it} across the bandgap can be obtained by repeated at different gate voltages to scan trap energies. The second way is to directly find the relation between gate voltage and surface potential by quasi-static CV measurement and Berglund integral, and the surface potential can be converted to energy in the bandgap by eq. (2.5) and (2.6)

$$\varphi_S = \int_{V_{FB}}^{V_G}(1 - \frac{C_{LF}}{C_{OX}})\, dV_G \quad (2.5)$$

$$E_T - E_i = q(\varphi_S - \varphi_B) \text{ and } \varphi_B = \frac{kT}{q}\ln(\frac{N}{n_i}) \quad (2.6)$$

We chose the latter one eventually because in the first approach neither the value of capture cross section nor its dependence on energy were known, in spite of the value of σ is assumed to be a constant of $10^{-15}cm^2$ in some papers. The results for integration of the QSCV are shown in **Fig 2.6**. Then, the D_{it} profile of each sample near midgap before FGA is demonstrated in **Fig 2.7**. We get the following conclusions: 1. 550℃ GeO_2 passivation is obviously better than 500℃ GeO_2 passivation before FGA. 2. It exhibits symmetric D_{it} distribution for GeO_2 passivation, which is different from the asymmetric profile of Si passivation (larger D_{it} in upper half bandgap) [13]. 3. The result shows more interface states in the midgap due to larger G_p/ω peak value as more band bending in the depletion region. This phenomenon is indeed so-called “weak inversion response”, for which the equivalent

circuit in **Fig 2.2(a)** is not valid anymore; instead, the circuit should be modified as shown in **Fig 2.8**[14]. In the weak inversion regime, interface traps can communicate with both the majority and minority carrier bands because of the much smaller minority carrier time constant as Fermi level located near the midgap, and the "dual communication" leads to a larger conductance response than the typical depletion response. For the Si/SiO_2 interface, this effect does not occur at room temperature in the 1 kHz to 1 MHz frequency window because the time constants of that interaction are too large to happen. By contrast, small bandgap materials like germanium, the weak inversion response is shown to be present in the 1 kHz to 1 MHz measurement range. Therefore, directly applying conductance technique to Ge MOSCAPs will lead to overestimation of interface trap density.

Whether or not weak inversion response is observed within the typical measurement window depends on the bandgap of the semiconductor, capture cross section of the trap, and the temperature. From the emission time constant ($\tau = \frac{1}{V_{th}\sigma N} e^{\frac{\Delta E}{kT}}$), it is concluded that smaller bandgap material, larger capture cross section, and higher temperature make the weak inversion response more significant. In our case of Ge MOSCAPs, low temperature measurement is needed to alleviate the dual communication.

Although frequency corresponding to the maximum Gp/ω is not employed in determining the position in the bandgap, it can be used to estimate the capture cross section [15] by eq. (3.7), as shown in **Fig 2.9**.

$$\ln \tau = \ln \frac{1}{V_{th}\sigma n_i} + \frac{1}{kT}(E_T - E_i) \qquad (2.7)$$

From our results, σ_n and σ_p are extracted from n-Ge and p-Ge respectively with the extrapolation of $\ln \tau$ VS $(E_T - E_i)$ plot, and larger σ_n (2.7-4.2$\times 10^{-16}$ cm^2) is obtained compared with σ_p(7.8-9.6$\times 10^{-16}$ cm^2). The derived capture cross section is substituted into the emission time constant so that **Fig 2.4** can be illustrated. This value is extremely important since it offers us the information about the part of interface states observable in the 1 kHz to 1

MHz frequency window. However, the value of σ will be double checked by charge pumping measurement of Ge MOSFET to see if it is reasonable.

Parasitic series resistance arising from low substrate doping and contact resistances or leakage through gate dielectric, can contribute measured admittance. They need to be included in the equivalent circuit model as R_s and G_t (Fig. 2.2 (d)) to extract the accurate value of interface trap conductance and capacitance. In this thesis, however, we assumed the two effects to be negligible because gate dielectric is quite thick (80 cycles ALD-Al_2O_3), and no significant frequency dispersion is observed in the accumulation region of CV curve.

2.4 Effect of FGA on Electrical Characteristics

Fig 2.10 depicts the multi frequency CV curves and QSCV after forming gas annealing (FGA). It is concluded that subsequent FGA processing effectively improved the interface quality, since CV characteristics after FGA show deeper "dip" and frequency dispersion becomes much less in depletion region for each sample. Also, the slope of CV curve in depletion region reflects the interface quality; the sample with FGA shows steeper slope which stands for less stretch-out and much more efficient band bending as gate voltage increases. Besides, CV hysteresis is expected to be lower after FGA which is attributed to the effective D_{it} reduction.

Unfortunately, the peaks are not observed in the G_p/ω versus plots after FGA (see **Fig 2.11**). Nevertheless, it is still rational to conclude that the interface state density apparently decreases due to much lower G_p/ω data in the 100 kHz to 1 MHz range. The relations between gate voltage and surface potential after FGA are derived by integration of the Berglund integral from QSCV, as demonstrated in **Fig 2.12**. For a given gate voltage (corresponding to a given surface potential), we choose the minimum and maximum values of G_p/ω data in the 100 kHz to 1MHz range and interpret them as the lower bound and upper

bound of D_{it}, as shown in **Fig 2.13**. The midgap D_{it} value will be reconfirmed by charge pumping measurement of GeO_2 passivation Ge MOSFET in the next chapter.

The amount of Fermi level movement with respect to a certain gate bias change reflects the trap density level at the oxide semiconductor interface. High trap density hinders Fermi level movement. Fermi Level Efficiency (FLE) [16] is defined as $\frac{d\varphi_S}{dV_G} = \frac{dE_F}{qdV_G}$. Using the depletion width approximation for perfect oxide semiconductor interface, the amount of band-bending can be calculated when applying a gate bias V_G:

$$V_G = V_{FB} + \varphi_S + \frac{qN}{C_{OX}}\sqrt{\frac{2\varepsilon_{Ge}\varphi_S}{qN}}, \text{ and } FLE = \frac{d\varphi_S}{dV_G} = \left(1 + \sqrt{\frac{2\varepsilon_S qN}{\varphi_S}}\frac{1}{2C_{OX}}\right)^{-1} \quad (2.8)$$

The ratio $\frac{d\varphi_S}{dV_G}$ should be quite close to 1 due to low substrate doping (~$1\times10^{15}cm^{-3}$) and high C_{OX} (~$0.5\mu F/cm^2$). Comparisons of the FLE of our samples before and after FGA are displayed in **Fig 2.14**, about 15~30% enhancement of Fermi level movement efficiency is achieved by FGA. In reality, the existence of interface states affects the Fermi level position, causing less band bending due to an additional $\frac{q\overline{D_{it}}q\varphi_s}{C_{OX}}$ term. If D_{it} near the midgap is assumed to be a constant, denoted by $\overline{D_{it}}$, eq. (2.8) is modified as follows,

$$V_G = V_{FB} + \varphi_S + \frac{qN}{C_{OX}}\sqrt{\frac{2\varepsilon_{Ge}\varphi_S}{qN}} + \frac{q\overline{D_{it}}q\varphi_s}{C_{OX}}\ ;\ FLE = \frac{d\varphi_S}{dV_G} = \left(1 + \sqrt{\frac{2\varepsilon_S qN}{\varphi_S}}\frac{1}{2C_{OX}} + \frac{q^2\overline{D_{it}}}{C_{OX}}\right)^{-1} \quad (2.9)$$

Eq. (2.9) implies that FLE about 78% near the midgap corresponds to $\overline{D_{it}}$ $6\times10^{11}(cm^{-2}eV^{-1})$, which is quite consistent with the G_p/ω data. Also, the D_{it} reduction is about $4.2\sim8.4\times10^{11}(cm^{-2}eV^{-1})$, resulted from FLE enhancement 15~30% after FGA. Not only from conductance method but from FLE do we get the same result; 550℃ GeO_2 passivation has better interface quality than 500℃ GeO_2 passivation before FGA, but the two interfaces become similar after FGA.

2.5 Low Temperature Measurement of Ge MOSCAP

In order to obtain the full distribution of D_{it} in the bandgap, conductance method is applied at low temperatures. Measurements with temperature 77 K, 120K, 180K and 250 K allow sampling of the D_{it} within the Ge bandgap, because each temperature monitors a limited part of the bandgap (**Fig. 2.4**). The multi frequency CV characteristics measured at 77K, 120K, 180K, 250K are shown in **Fig. 2.15**. Thermal generation (inversion response) almost disappears at 77K and CV curves look steeper in the depletion region, while the hump due to weak inversion response is still visible at 250K in C-V measurements.

Fig 2.16 illustrates the G_p/ω versus f plots of our 550℃ GeO_2 passivation Ge MOSCAP at 77K and 250K. The peaks neither exist nor shift to higher frequency as gate bias moved towards accumulation region. However, we interpret the largest G_p/ω value to represent D_{it} at the specific position in bandgap (for a given gate voltage). The upper half bandgap D_{it} distribution of our 550℃ GeO_2 passivation sample is shown in **Fig. 2.17**, and weak inversion response is suppressed with lower temperature measurement as predicted before. Two assumptions are made to get the distribution: 1. Capture cross section is a constant for different temperature and position in the bandgap. 2. Gate voltage and surface potential relation is the same for room temperature and low temperature; to be more precise, QSCV should be measured under low temperature to derive the corresponding $V_G - \varphi_S$ relation.

At 77K, no frequency dependent flatband shift is observed, indicating that D_{it} near the conduction band edge should be very low for our 500 or 550℃ GeO_2 passivation PMOSCAPs. This is inconsistent with the result extracted from **Fig. 2.17**. From low temperature G_p/ω data of another gate voltage range (**Fig. 2.18**), peaks occur at higher frequencies as gate bias is swept towards accumulation region, which means traps closer to conduction band edge are probed. D_{it} near band edges should be $1\text{-}4\times10^{11}cm^{-2}eV^{-1}$ according to G_p/ω data, and such low D_{it} value explains the CV curve without "frequency dependent flatband shift". Nevertheless, the peak-observable range for 77K is V_G=-0.32~-0.38V

(V_G=-0.32~-0.42V for 120K), which are slightly "lower" than V_{fb} and should not make the Fermi-level of $1.5\times10^{14}cm^{-3}$ n-Ge locate at the D_{it} observable energy range at 77K (120K). There still exist flaws in both approaches mentioned above, and we are facing a dilemma of the correct extraction of D_{it} distribution. Therefore, further investigation is needed.

High frequency measurement of Ge MOSCAPs shows low frequency CV characteristics at room temperature, so it is necessary to clarify how the minority carriers show up fast enough to follow the ac signal. Two main mechanisms are responsible for this phenomenon:

1. Diffusion-induced inversion response. The diffusion-induced inversion generation component becomes more important for smaller bandgap semiconductors or higher temperatures. In the diffusion case minority carriers diffuse from bulk to surface contributing to the inversion at the MOS interface. This response increases with increasing intrinsic carrier concentration (n_i), which is much larger for Ge as compared to Si. The diffusion-induced inversion response is modeled by inserting a conductance, $\frac{G_{diff}}{A} = \frac{q^2}{kT}\frac{L_{mir}}{\tau_{mir}}\frac{n_i^2}{N_{maj}}$ into the equivalent circuit [17].
2. Generation-recombination induced inversion response. Minority carriers are generated through bulk traps in depletion region, which is more prominent at lower temperatures than the diffusion-induced inversion generation. An additional conductance $\frac{G_{gr}}{A} = \frac{q}{\varphi_s}\frac{W}{\tau_T}n_i$ is added in parallel with the G_{diff}, as illustrated in **Fig. 2.19(a)** [17].

In strong inversion region, G_{sub} can de decomposed into G_{gr} and G_{diff}, where G_{gr} dominates at lower temperature and G_{diff} at higher temperature. It has been reported that the crossover temperature is about 45℃ [10] for Pt/HfO_2/5E14 n-Ge MOSCAP, meaning that the leading mechanism changes from G_{gr} to G_{diff} at 45℃. Because $G_{diff} \propto n_i^2$, $G_{gr} \propto n_i$, the activation energy for diffusion induced inversion response is expected to be E_g, while for generation-recombination induced inversion E_a should be $E_g/2$. Arrhenius plot of the substrate conductance at 100 kHz and -1.2 V (180K, 250K, and 297K) of our 550℃ GeO_2 passivation

MOSCAP is shown in **Fig. 2.19(b)**, and the extracted activation energy equals to 0.32eV, showing generation-recombination induced inversion to be dominant at lower temperature.

2.6 Conclusions

GeO_2 passivation Ge PMOS and NMOS capacitors with different GeO_2 growing temperature were fabricated. Theory of the conductance method was discussed in detail, and utilizing it to extract the interface state density for different passivation samples. D_{it} of each sample was effectively reduced through FGA. Not only from G_p/ω value but from Fermi level efficiency did we attain similar result, D_{it} near midgap was about 5×10^{11} and 1×10^{12} $cm^{-2}eV^{-1}$ with and without FGA respectively. Also, σ_n ($2.7\text{-}4.2 \times 10^{-16}cm^2$) and σ_p($7.8\text{-}9.6\times10^{-16}$ cm^2) could be extracted by extrapolation of $\ln\tau$ VS $(E_T - E_i)$ plot.

Low temperature measurement was performed to extract D_{it} near band edges, with the normally observed U-shaped distribution derived. However, the reason for unobservable peaks was still unclear and further investigation was needed. We also utilized the G_{sub} biasing in strong inversion to make the Arrhenius plot, proving that activation energy equal to $E_g/2$ at lower temperature (<45℃). Generation-recombination induced inversion response is the dominating mechanism that causes low frequency CV characteristics for high frequency measurement at room temperature.

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	Step.1	Step. 2 RTO	Step. 3	Step. 4	Step. 5	Step. 6
P500	Cyclic DHF clean of p-Ge	500℃10s	ALD Al_2O_3 160°C 80 cycles	Al deposition + Lithography + etching	backside contact (Al)	FGA 300℃, 30min
P550		550℃10s				
N500	Cyclic DHF clean of n-Ge	500℃10s				
N550		550℃10s				

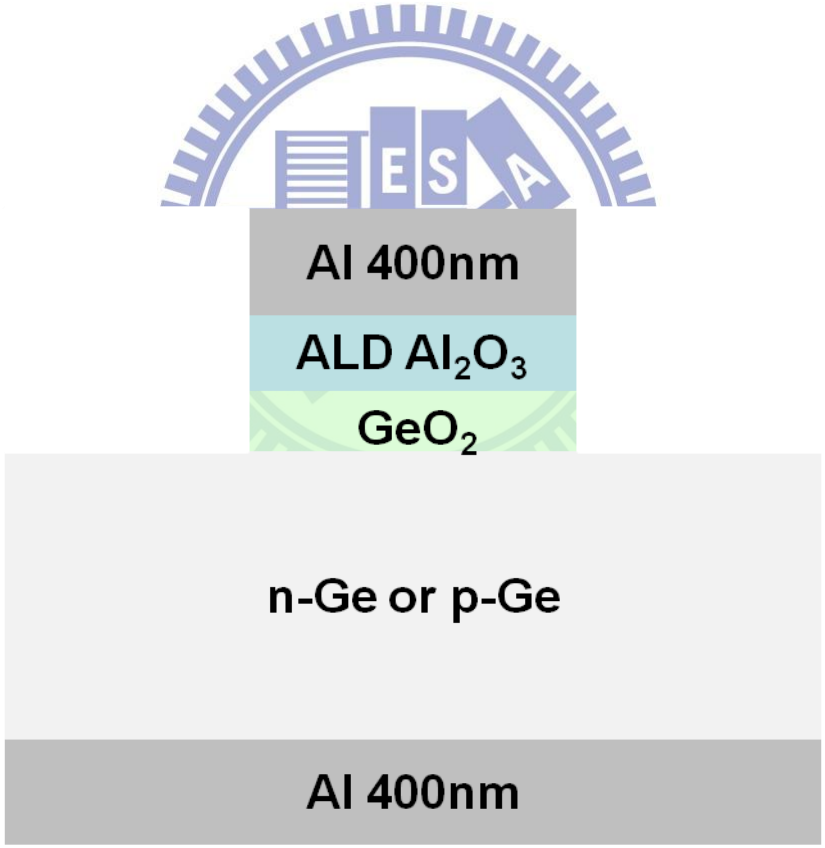


Fig. 2.1 Process flow of Ge MOSCAPs and their device structure.

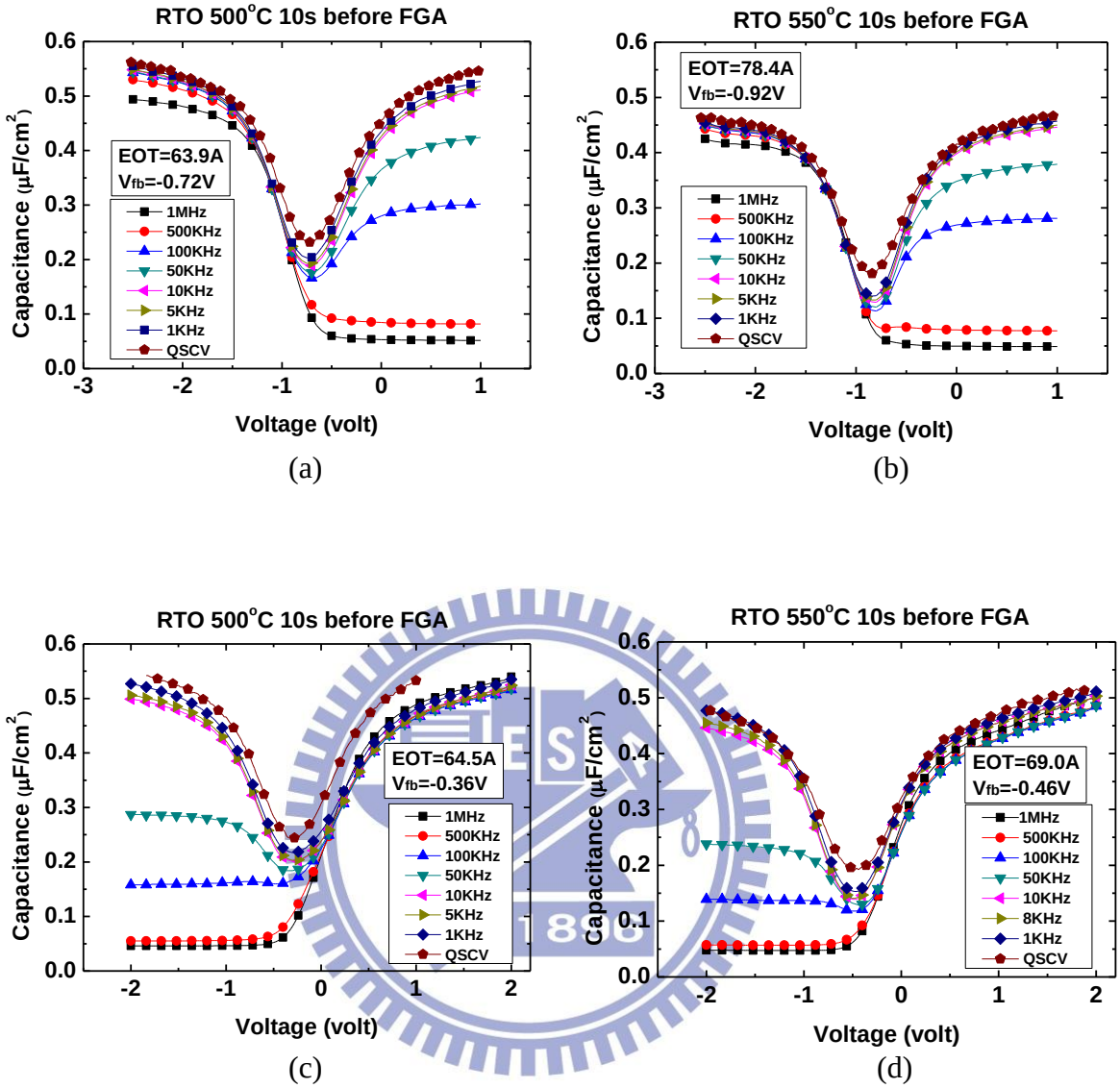
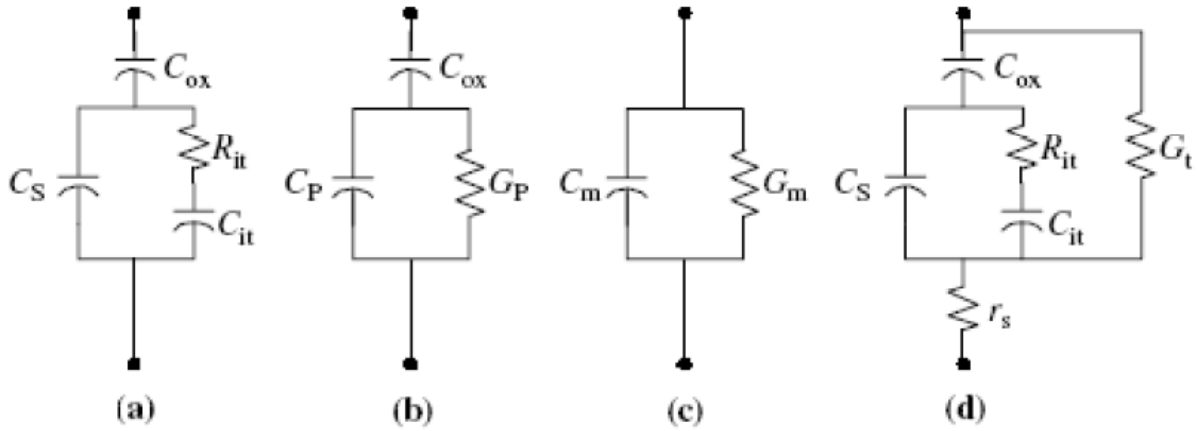
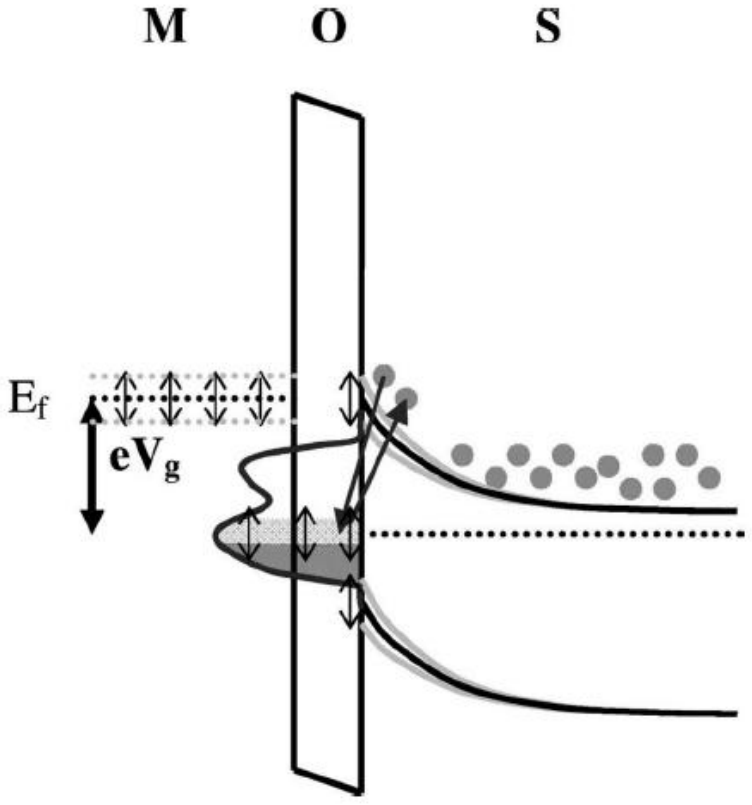


Fig. 2.2 Multi frequency and quasi-static CV of Ge MOSCAPs before FGA are depicted. (a) p-Ge, RTO 500℃ 10s. (b) p-Ge, RTO 550℃ 10s. (c) n-Ge, RTO 500℃ 10s. (d) n-Ge, RTO 550℃ 10s.





(e)

Fig 2.3 Equivalent circuit models for conductance measurements; (a) MOS capacitor with single level interface traps, (b) simplified circuit of (a), (c) measured circuit, (d) including series resistance and tunnel conductance due to gate leakage. (e) The band diagram of a typical MOS structure is illustrated, with surface potential in the semiconductor to periodically move up and down because of a small sinusoidal voltage on top of the static gate bias.

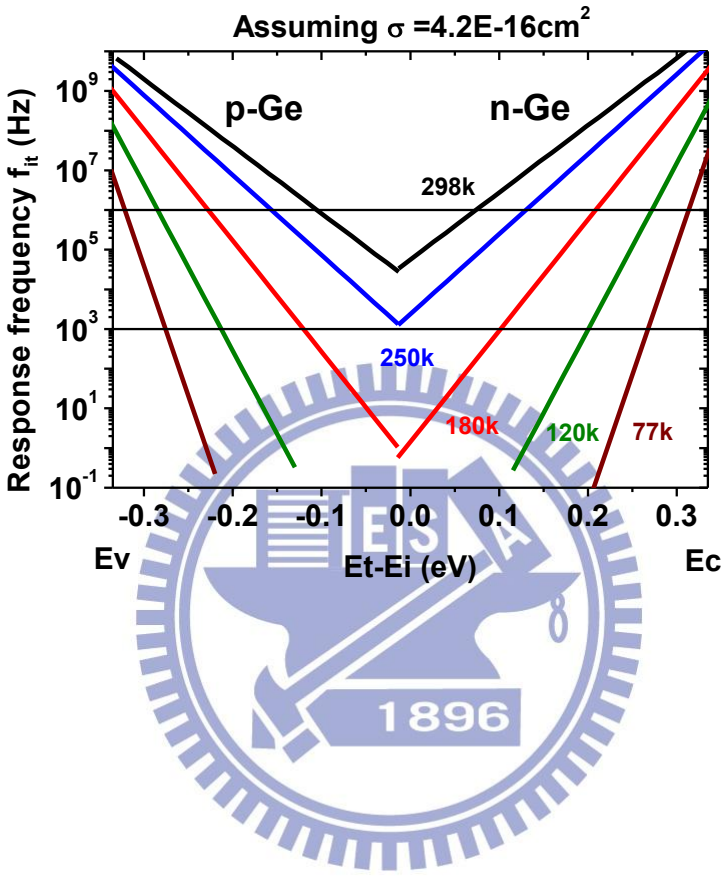


Fig 2.4 The behavior of the interface trap time constant as a function of temperature determines the part of interface traps in the bandgap observable in the MOS admittance characteristic.

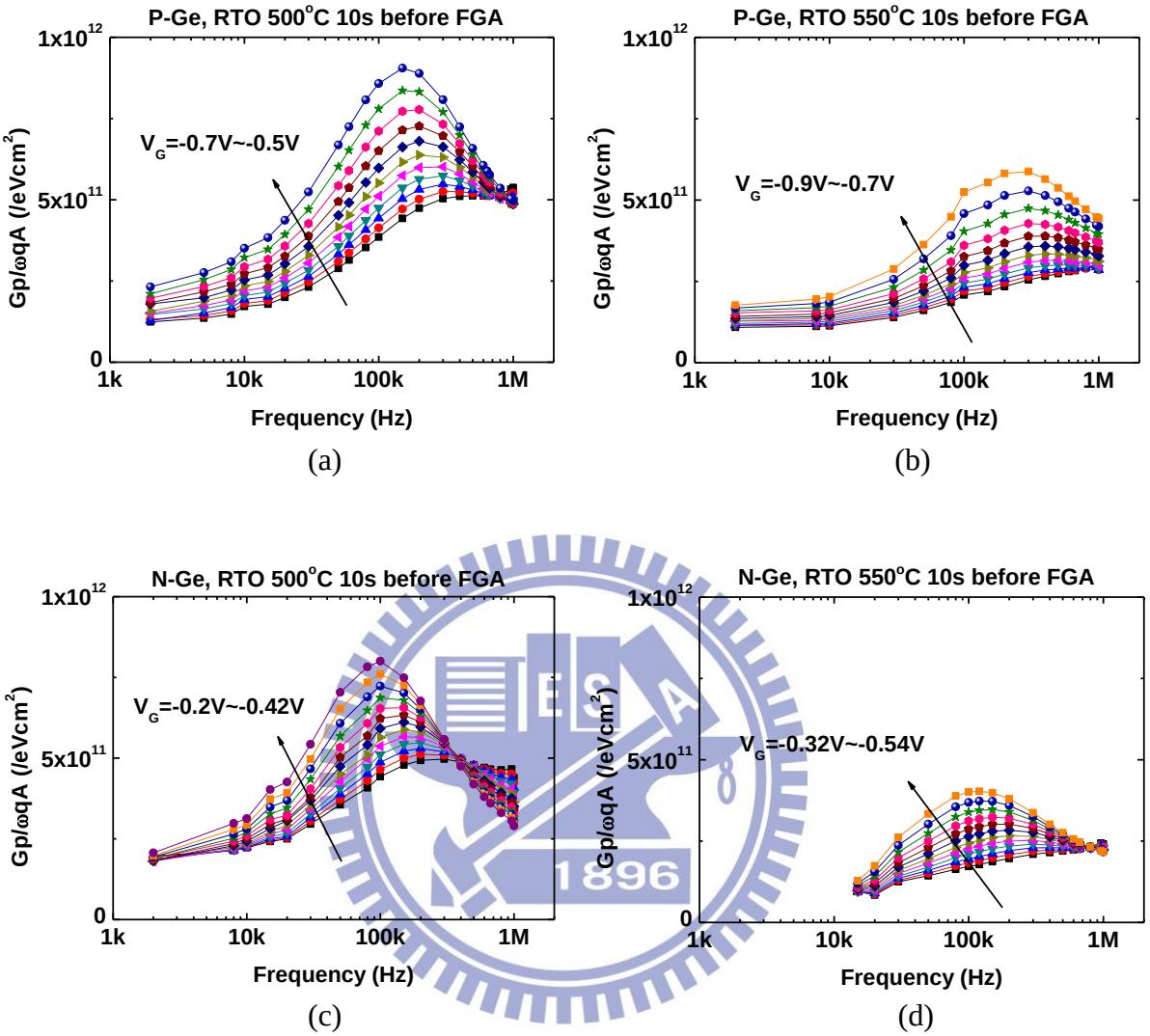
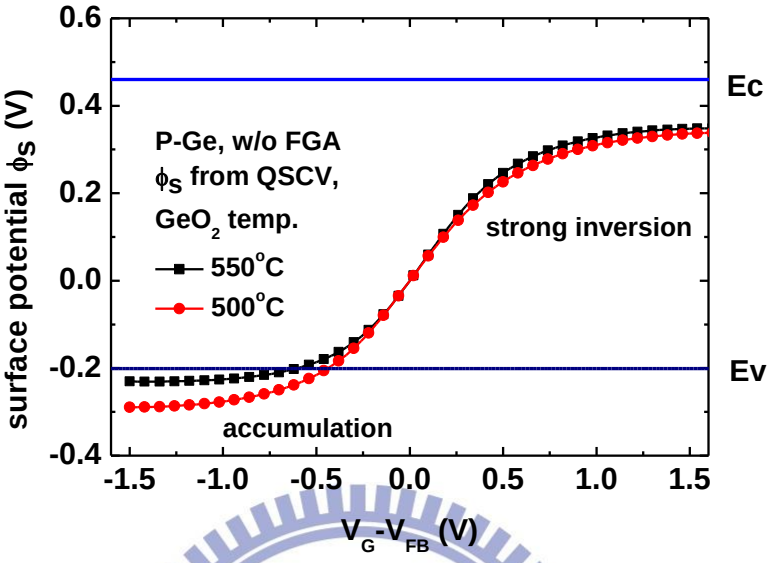
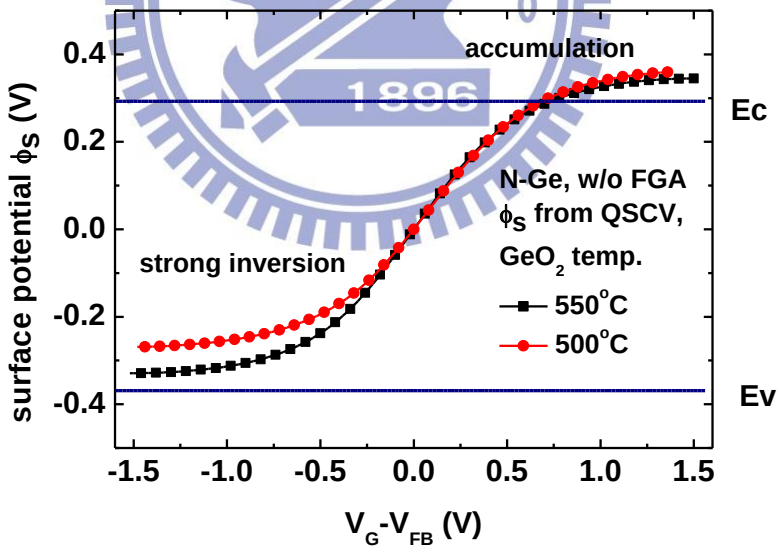


Fig. 2.5 G_p/ω versus f of Ge MOSCAPs before FGA are depicted. (a) p-Ge, RTO 500℃ 10s. (b) p-Ge, RTO 550℃ 10s. (c) n-Ge, RTO 500℃ 10s. (d) n-Ge, RTO 550℃ 10s.



(a)



(b)

Fig. 2.6 Relation between gate voltage and surface potential by integration of quasi-static CV before FGA are calculated. (a) p-Ge. (b) n-Ge.

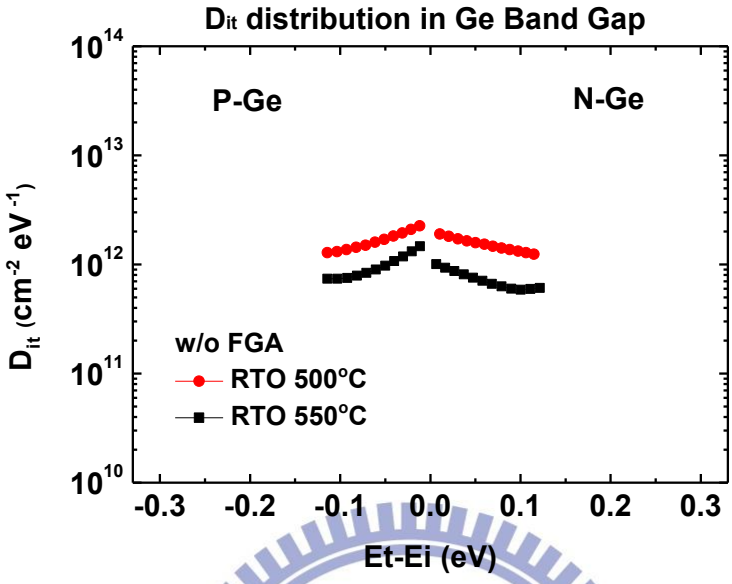


Fig. 2.7 D_{it} profile of each sample near midgap before FGA is demonstrated.

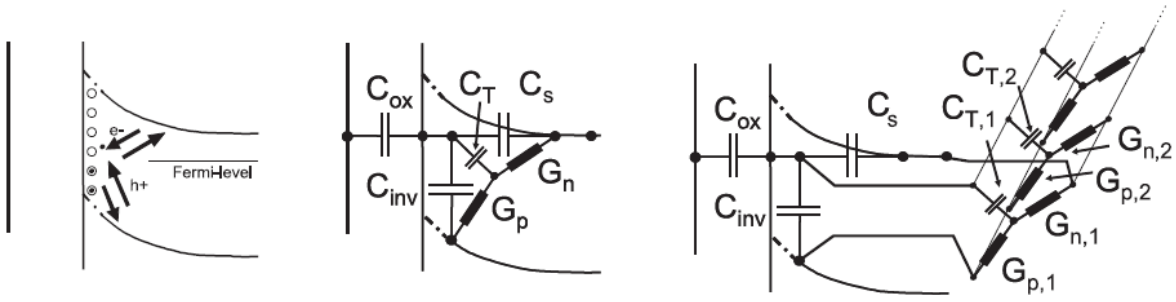


Fig. 2.8 A band diagram showing the weak inversion response (left) and the general equivalent circuits used to model the MOS capacitor C-V and G-V characteristics across the bandgap for an n-type capacitor. The first circuit (middle) models one trap only: C_{ox} is the oxide capacitance, C_{inv} the inversion capacitance, C_s the depletion (and accumulation) capacitance, C_T the trap capacitance, and G_n, G_p electron and hole trap conductance, respectively. For distribution of interface states a series of Y-circuits is used (right).

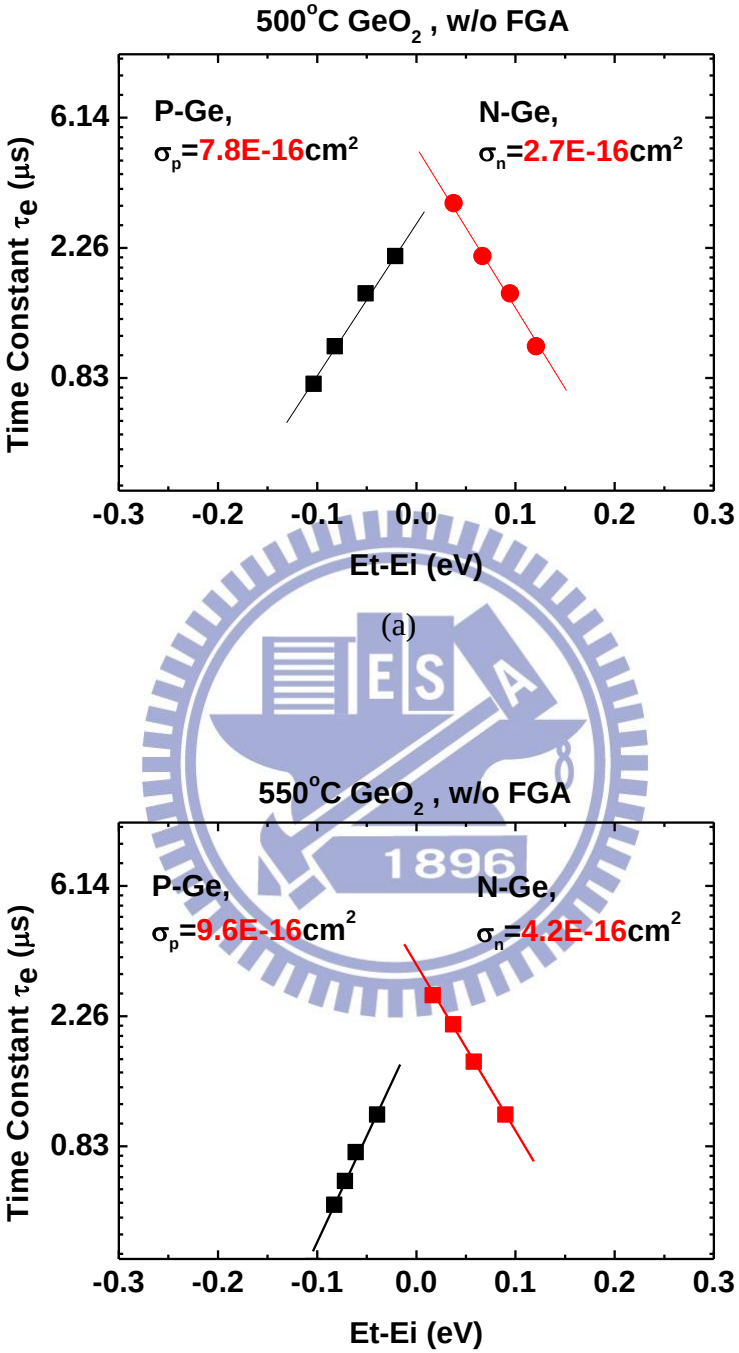


Fig. 2.9 σ_n and σ_p are extracted from n-Ge and p-Ge respectively with the extrapolation of $\ln\tau$ VS $(E_T - E_i)$ plot. (a) RTO 500℃ 10s. (b) RTO 550℃ 10s.

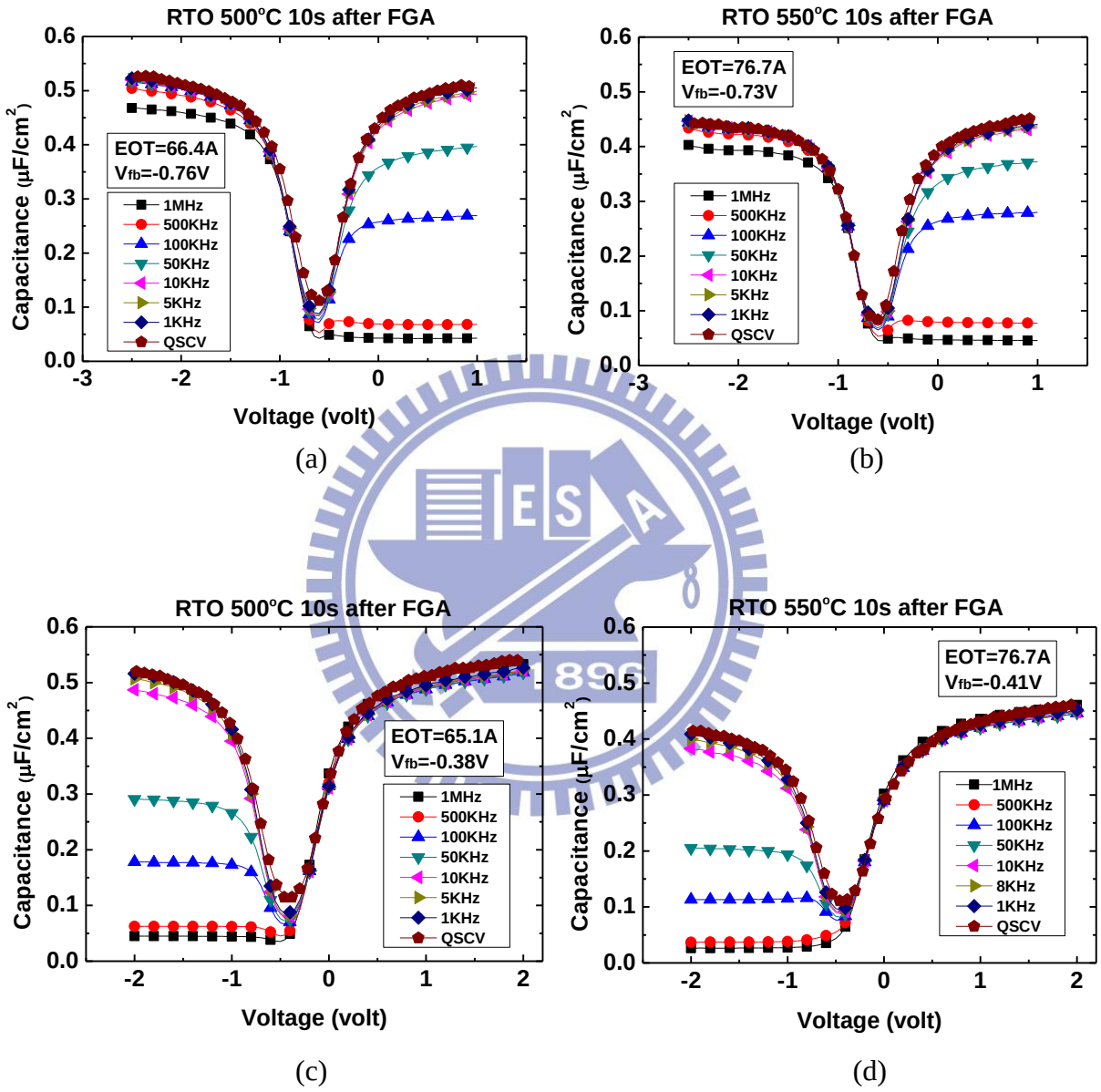


Fig. 2.10 Multi frequency and quasi-static CV of Ge MOSCAPs after FGA are depicted. (a) p-Ge, RTO 500℃ 10s. (b) p-Ge, RTO 550℃ 10s. (c) n-Ge, RTO 500℃ 10s. (d) n-Ge, RTO 550℃ 10s.

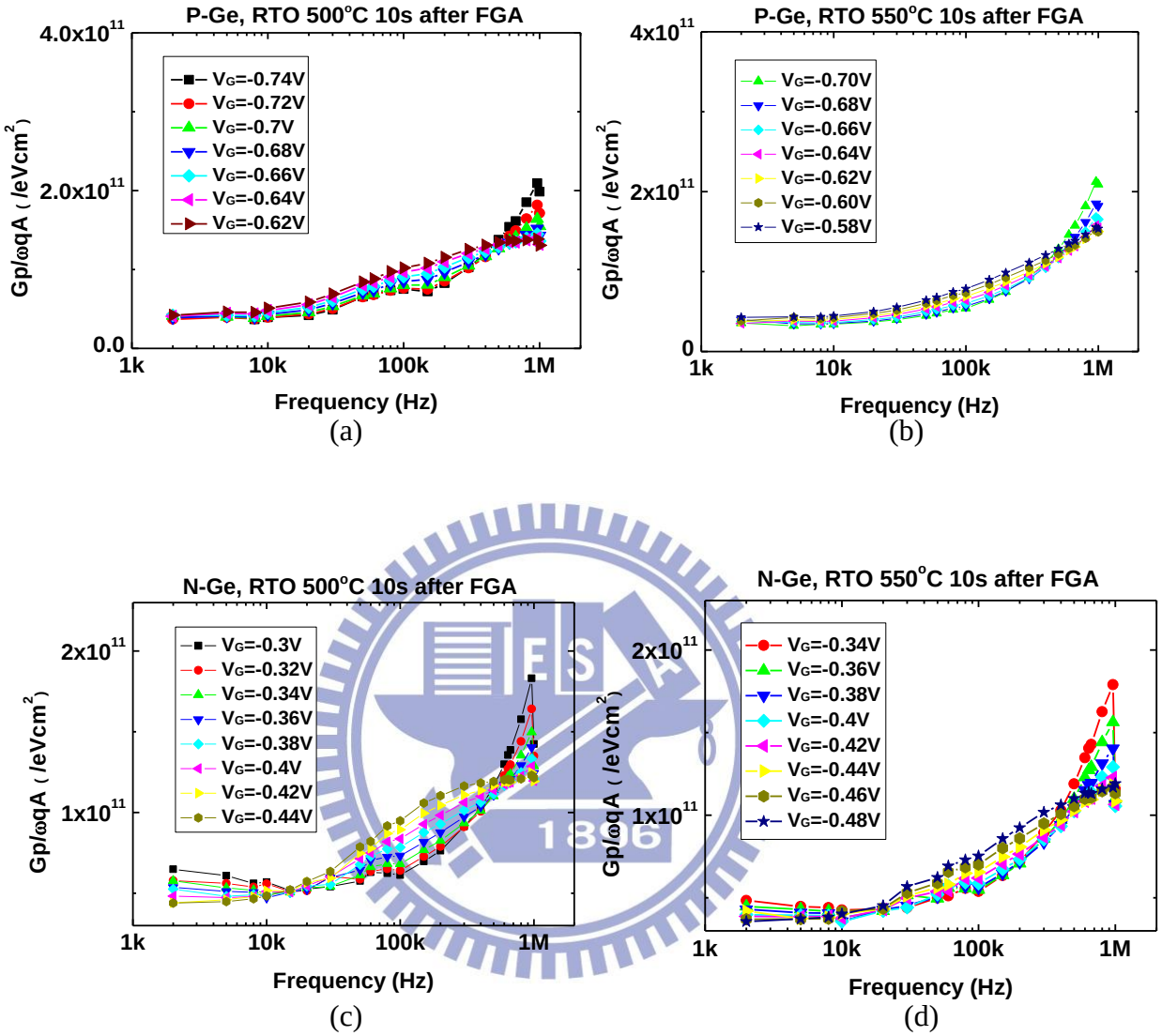


Fig. 2.11 G_p/ω versus f of Ge MOSCAPs after FGA are depicted. (a) p-Ge, RTO 500℃ 10s. (b) p-Ge, RTO 550℃ 10s. (c) n-Ge, RTO 500℃ 10s. (d) n-Ge, RTO 550℃ 10s.

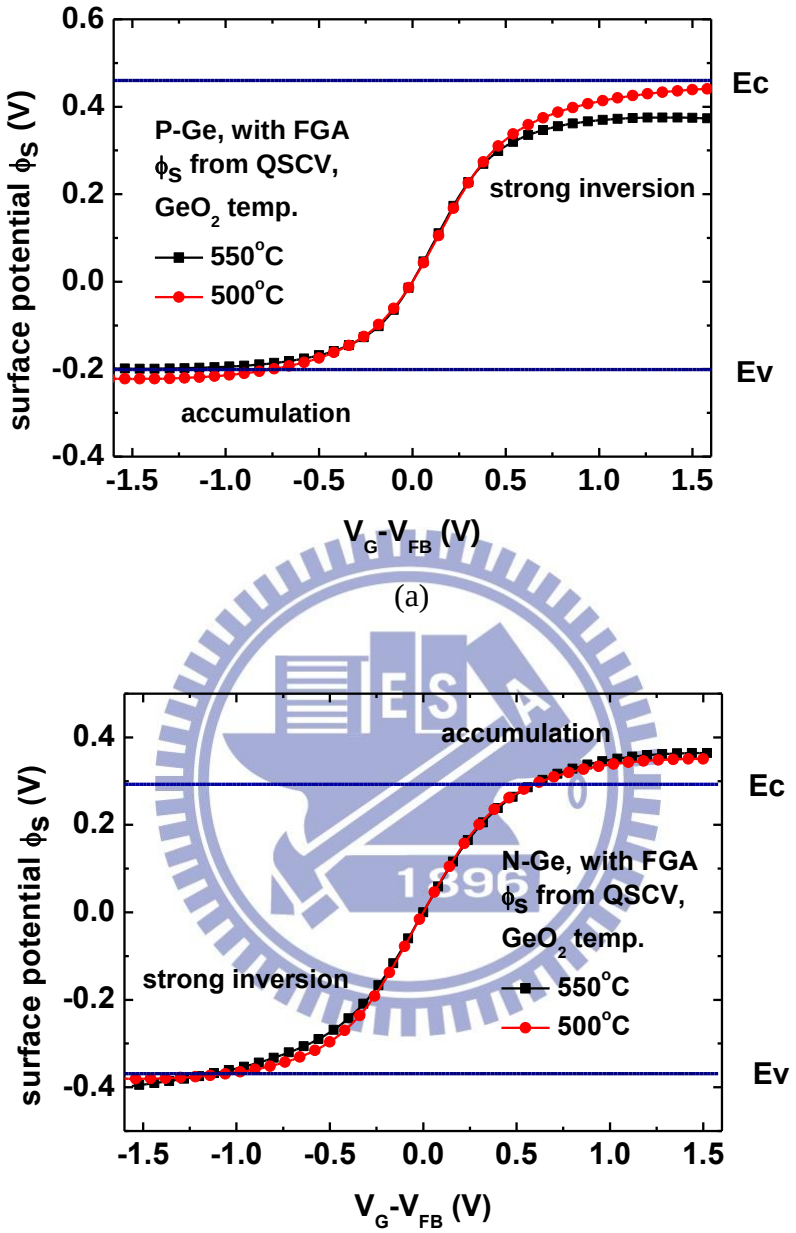


Fig. 2.12 Relation between gate voltage and surface potential by integration of quasi-static CV after FGA are calculated. (a) p-Ge. (b) n-Ge.

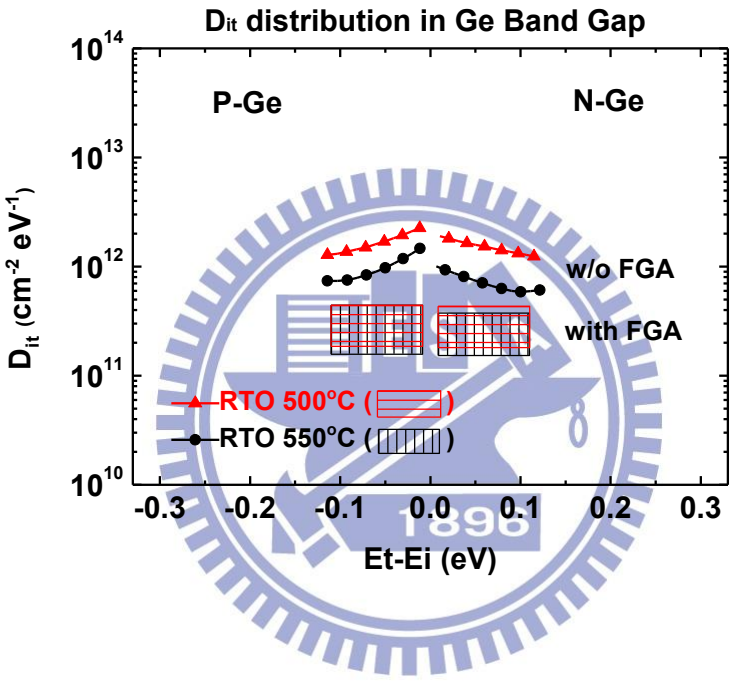


Fig. 2.13 Comparison of D_{it} profile of each sample near midgap with and w/o FGA is demonstrated.

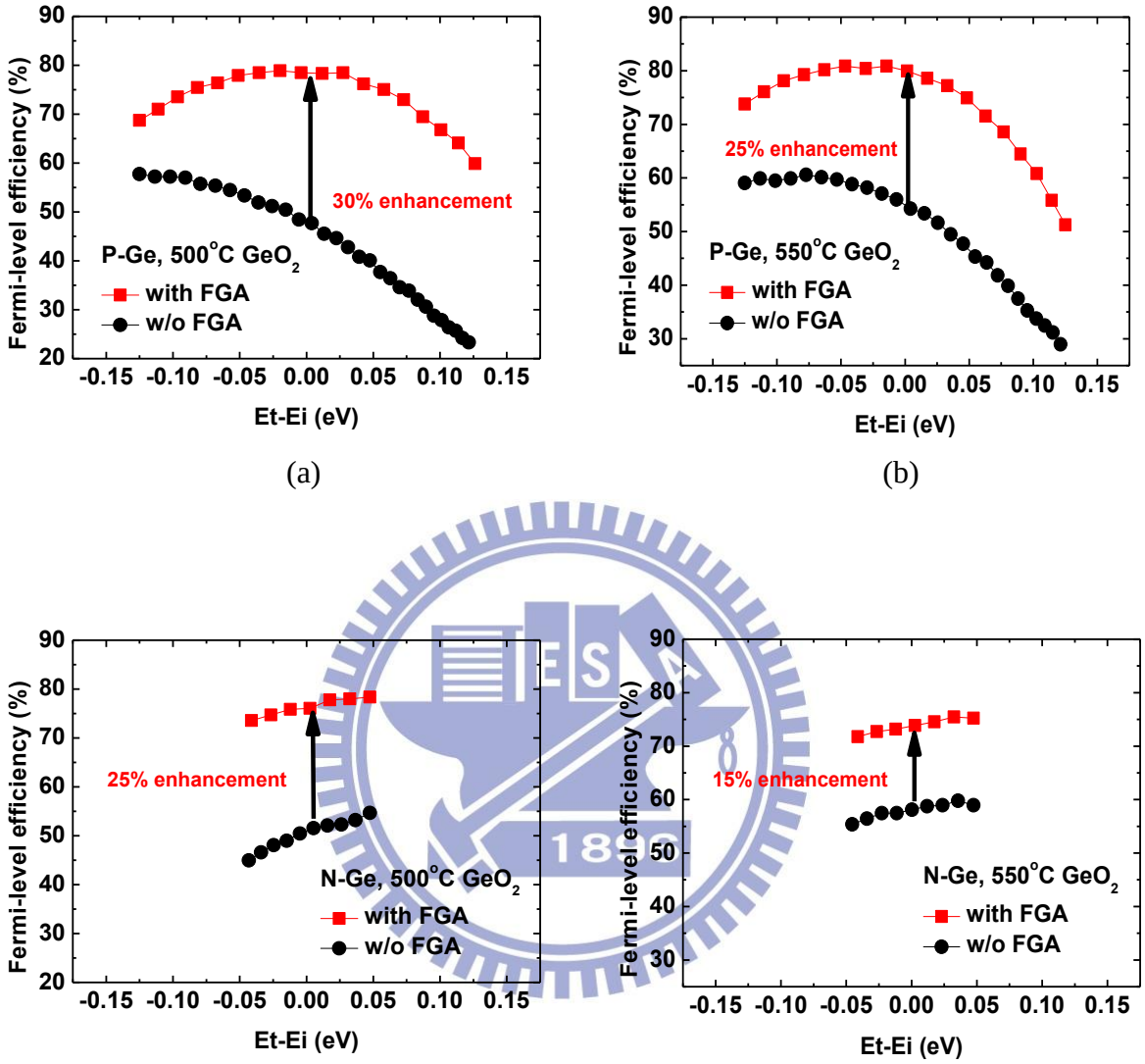
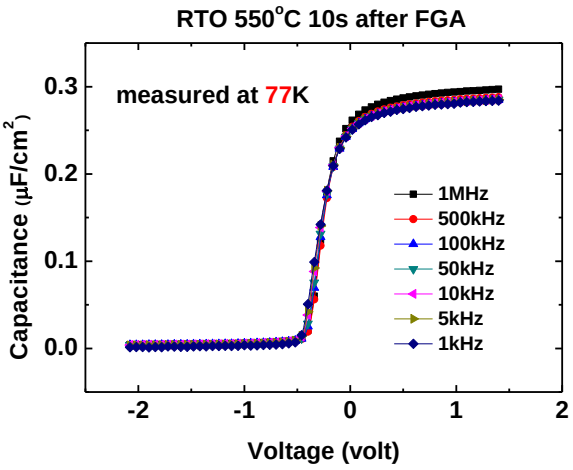
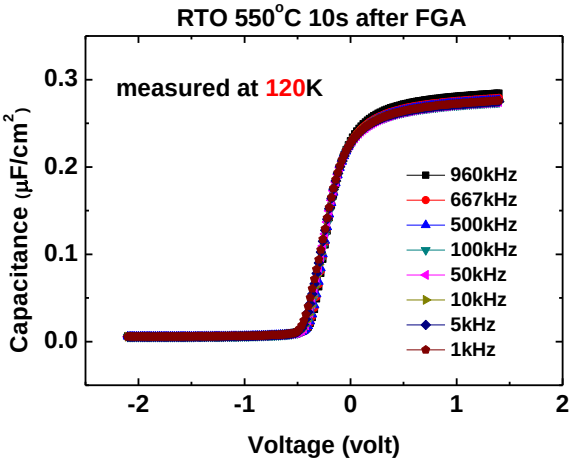


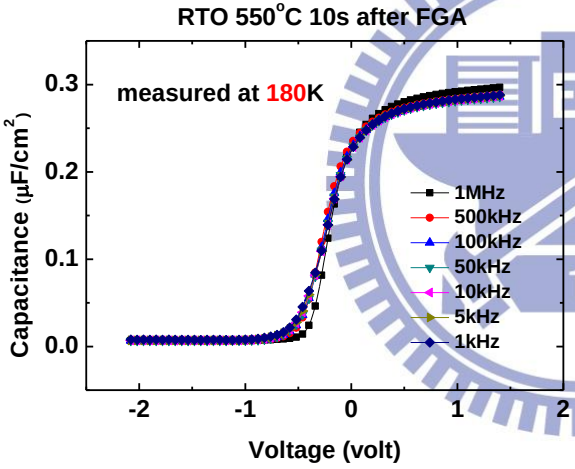
Fig. 2.14 Comparisons of the FLE of our samples before and after FGA are displayed. (a) p-Ge, RTO 500℃ 10s. (b) p-Ge, RTO 550℃ 10s. (c) n-Ge, RTO 500℃ 10s. (d) n-Ge, RTO 550℃ 10s.



(a)



(b)



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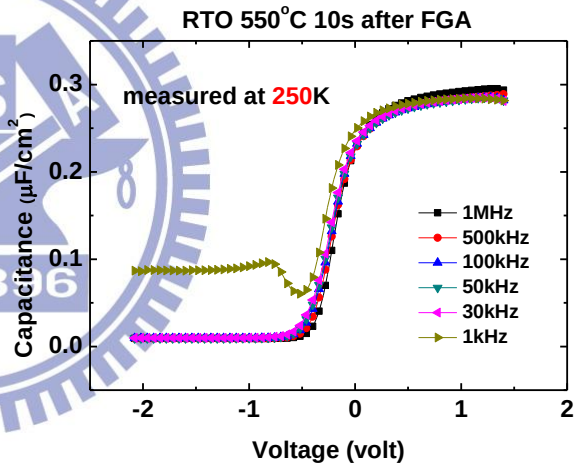
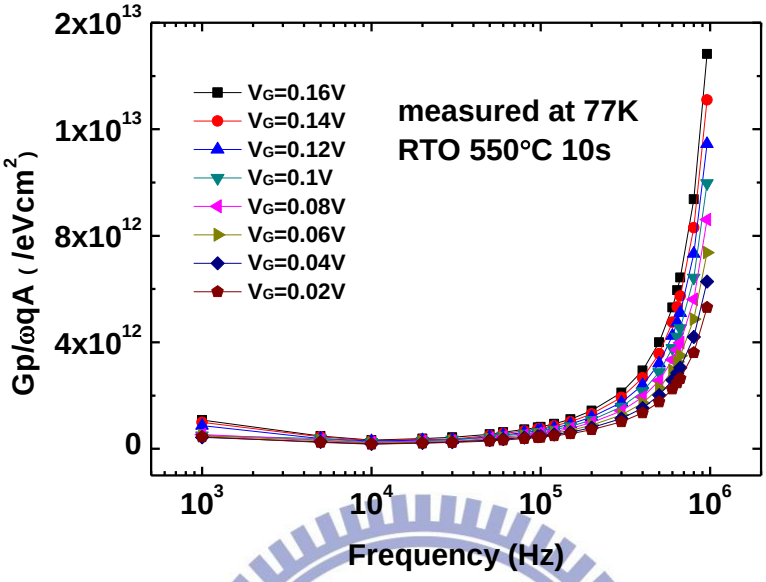
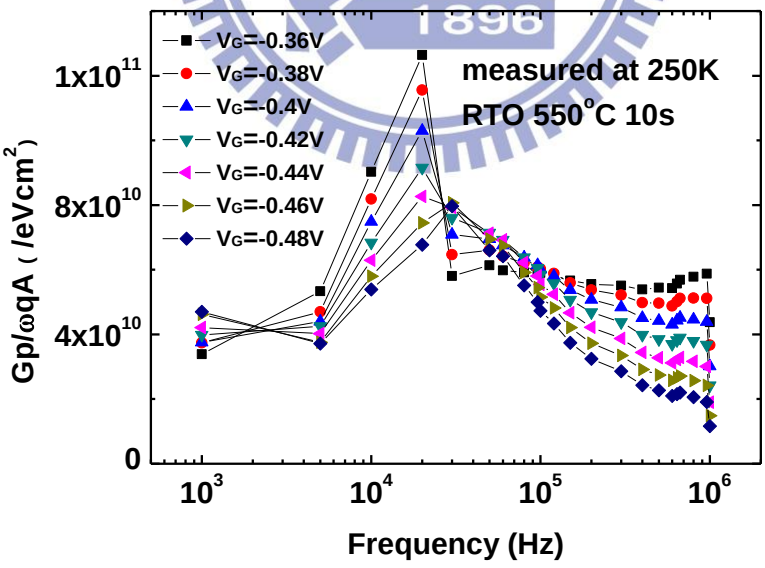


(d)

Fig. 2.15 Multi frequency CV characteristics of 550℃ GeO_2 passivation PMOSCAP after FGA are measured at low temperature. (a) 77K (b) 120K (c) 180K (d) 250K



(a)



(b)

Fig. 2.16 G_p/ω data of 550℃ GeO_2 passivation PMOSCAP after FGA are illustrated. (a) 77K (b) 250K

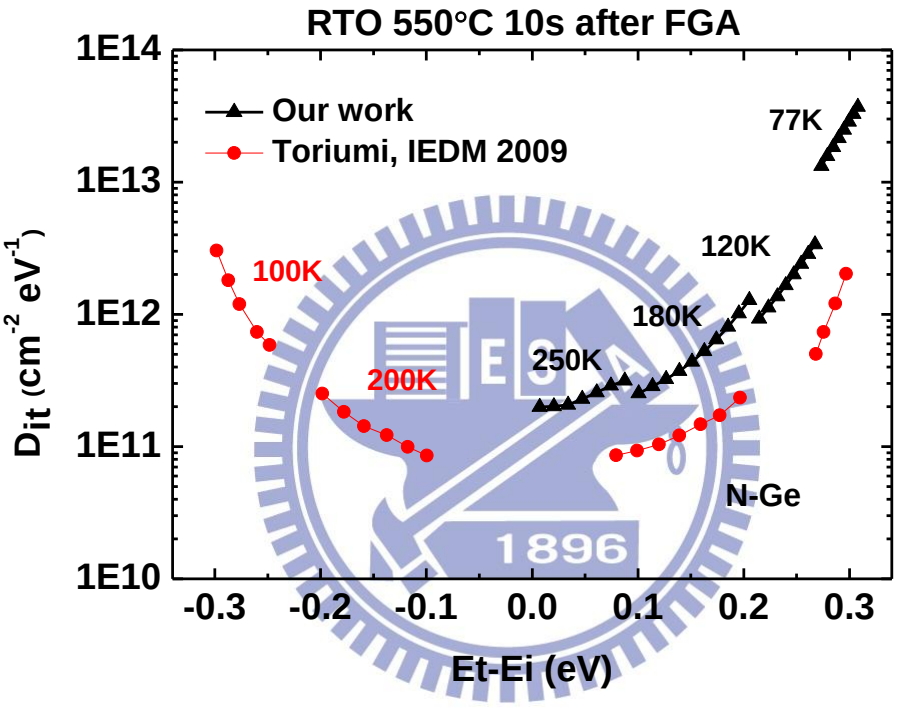
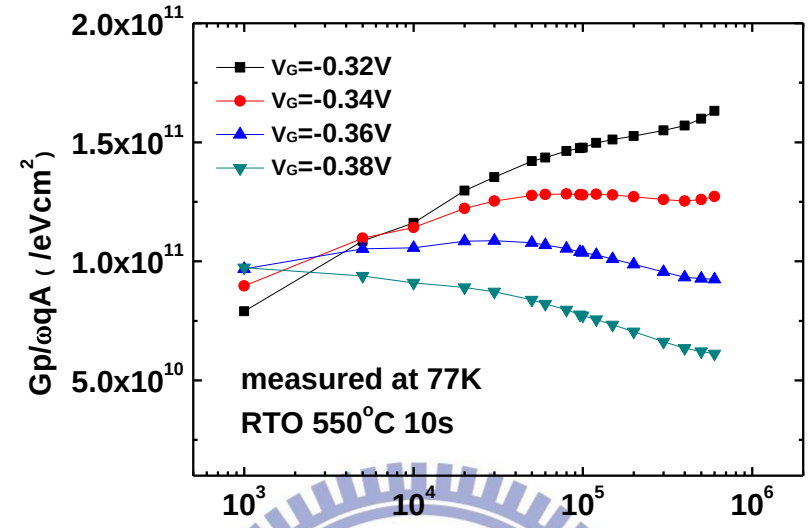
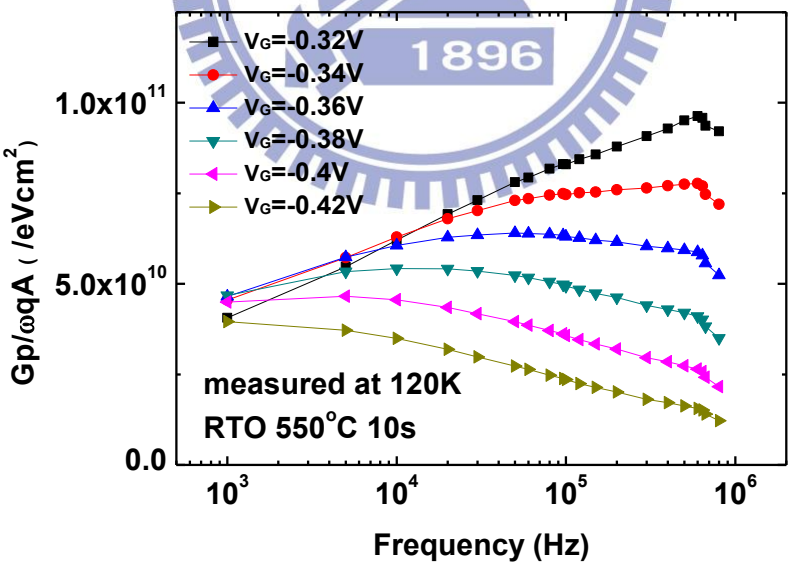


Fig. 2.17 D_{it} profile in the upper half bandgap for 550℃ 10s GeO_2 passivation after FGA is demonstrated.

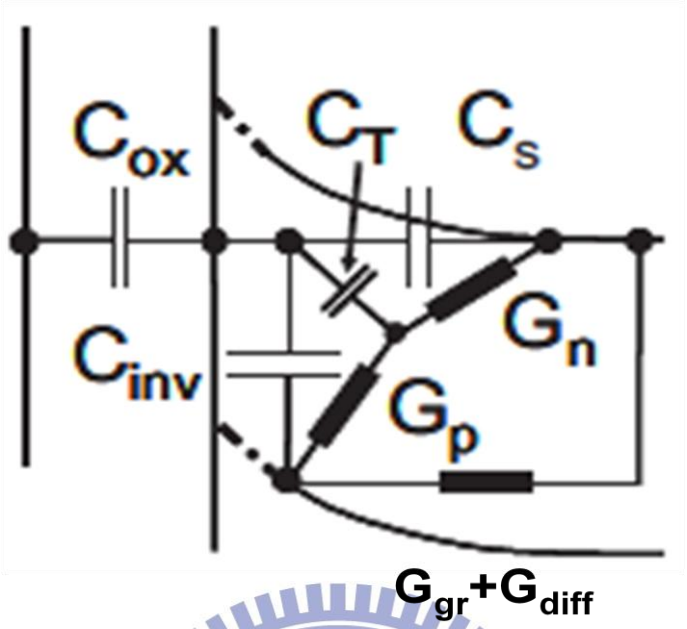


(a)

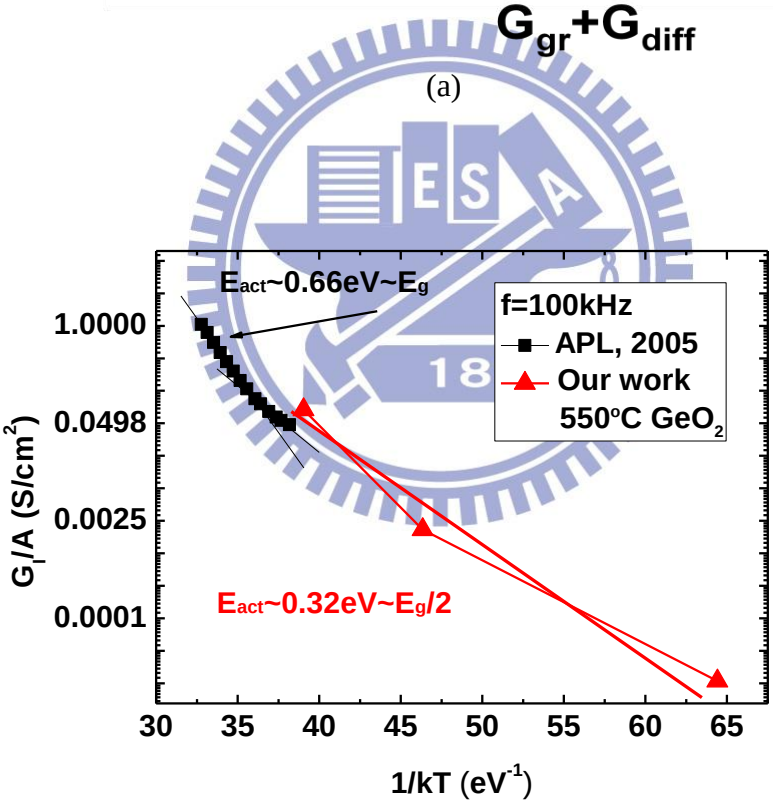


(b)

Fig. 2.18 G_p/ω data of 550℃ GeO_2 passivation PMOSCAP after FGA are illustrated at the peak-observable gate voltage range. (a) 77K (b) 120K



(a)



(b)

Fig. 2.19 (a) Diffusion-induced and generation-recombination induced inversion response are modeled by inserting corresponding conductance in parallel when bias in inversion regime. (b) Arrhenius plot of the substrate conductance at 100 kHz and -1.2 V (180K, 250K, and 297K) of our 550℃ GeO_2 passivation MOSCAP is shown.

Chapter 3

Inversion-Mode Ge p-MOSFET with Atomic-Layer-Deposited Al_2O_3 Gate Dielectrics

3.1 Introduction

When Si complementary metal-oxide-semiconductor (CMOS) technologies gradually scale to 22 nm node, the high mobility semiconductor materials receive renewed interest in MOSFET applications to pursue much higher device performance. In particular, Ge and III-V-based channels with various prevailing gate dielectrics are promising structures to replace the conventional Si MOSFETs. Nevertheless, several formidable challenges remain if we are to realize state-of-the-art Ge devices. Adequate surface passivation with a low D_{it} value and larger junction leakage due to lower band gap are essential to be solved, which make the high performance Ge devices feasible. The junction leakage should be overcome by alternative device geometries, such as thin epi-Ge on Si, Ge-on-insulator, or FinFETs. Much effort have been spent on the high quality epitaxial Ge [1]; however, difficulties still exist and this is beyond the scope of the thesis. We adopt the GeO_2 layer experience from Chapter 2 to passivate the Ge surface.

In this chapter, effects of inserting a GeO_2 layer and performing FGA on junction or device electrical characteristics are discussed, including series resistance, subthreshold swing, and mobility. Also, interface qualities for different samples are characterized by charge pumping and gated-diode measurement; reliability issues for GeO_2 are investigated through applying stress. Finally, the pros and cons of a GeO_2 passivation layer before high-k deposition are summarized according to our experimental results.

3.2 Fabrication of Gate-Last Ge p-MOSFET

(100)-oriented n-Ge substrate doped with Sb at level of 1.5E14cm^{-3} (resistivity ca. 10Ω·cm) was used for Ge PMOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide, then a 420-nm-thick SiO_2 layer was capped for the field oxide by PECVD.

First, the source/drain region was opened through the 1st Mask, followed by implantation of the Boron (1×10^{15} cm^{-2}, 60 keV) into the n-Ge, with dopant activation condition 500℃, 30s. Next, active area (AA) was opened through the 2nd Mask, and the wafers were split into two conditions: a no passivation sample and a 500℃ 10s GeO_2 passivation sample. After that, an 80 cycles ALD-Al_2O_3 was deposited as the high-k gate dielectric. Right after excavating the contact hole on S/D region through the 3rd Mask, a 400nm Al metallization was performed which was then patterned to define metal pads through the 4th Mask. Finally, a 400nm Al layer was deposited as the backside contact.

Forming gas annealing (FGA, 300℃, 30 min, H_2/N_2=5%) was performed to investigate the effect of FGA on electrical characteristics.

The process flow and device structure are shown in **Fig. 3.1.**

3.3 Effect of FGA on Ge p-MOSFET Electrical Characteristics

3.3.1 P$^+$N Ge Junction Characteristics

Figures 3.2(a) (b) display the effects of 300℃ FGA on the junction characteristics of Ge p-MOSFETs for the two samples. The reverse bias leakage current density (J_R) at -2V for no passivation sample are 1.4×10^{-2} A/cm^2 and 6.9×10^{-3} A/cm^2, while the forward bias current at 2 V are 9.2×10^{2} A/cm^2 and 4.7×10^{2} A/cm^2, without and with FGA respectively. On/off ratio

of 4.8 orders is achieved, but junction leakage seems unacceptably high compared with the Si device. We suppose that large value of J_R in this case originated mainly from the contribution of the generation current, which is dependent on the level of substrate doping (1.5E14 cm^{-3}), residual metal contamination after surface cleaning, bulk defects in the Ge substrate and the D_{it} at the SiO_2/Ge interface. Therefore, the lower J_R after FGA is attributed to the effective reduction of the defects. On the other hand, an additional 300℃ 90 minutes thermal annealing is definitely to cause dopant diffusion, and lower doping concentration verified by series resistance of the junctions (**Figure 3.3**) may account for the slight decrease of the forward current (J_F).

To compare junction characteristics between 500℃ 10s GeO_2 passivation and no passivation sample, junctions with GeO_2 passivation showing lower J_F and larger J_R is inferred to correlate with lower concentration of the S/D region. Lower concentration causing larger series resistance degrades the forward current, while it widens the depletion width to induce more generation current simultaneously. However, we are still not clear about the extent of oxidation enhanced diffusion (OED) of B in Ge, and it requires being under further investigation. From the result of larger J_R for GeO_2 passivation sample, it can be mentioned in advance that off current of I_D-V_G and the gated-diode current biased in accumulation are both larger for this sample.

3.3.2 Basic Device Characteristics

Several studies have demonstrated that FGA or pure H_2 annealing can result in improved high-k/Ge interfaces, and so did we obtain the same results in the Chapter 2. Utilizing the conductance method, we did obtain a lower D_{it} value of about 5×10^{11} $cm^{-2}eV^{-1}$ and a better FLE of at least 15% enhancement for the MOS capacitors after performing FGA at 300℃. Hence, we anticipate that the fabricated p-MOSFETs would exhibit enhanced performance as a result of improvements on not only the p+/n junction but also the dielectric interface.

Fig. 3.4 displays the I_D-V_D characteristics of the p-MOSFETs with and without FGA. As expected, the devices undergone FGA at 300℃ exhibit superior performance with larger drive current. From linear region of I_D-V_D curves for different gate overdrive and various gate lengths, we are able to extract the S/D series resistance by the Terada and Muta method (see **Fig. 3.5**). For the two samples, source/drain series resistance (R_{SD}) and G/S,D overlap (ΔL) are both increased due to more diffusion of dopants and lower S/D doping, caused by addition 300℃ 90 minutes thermal annealing.

I_D-V_G characteristics of the p-MOSFETs are shown in **Fig. 3.6**, where higher on current (less coulomb scattering), lower off current (less defects), and better subthreshold swing (less D_{it}) are observed for both samples. However, GIDL becomes more severe after FGA for p-MOSFETs, with larger gate/drain overlapped region and lower doping concentration taken into consideration. The GIDL increases a half order as V_D changes from -0.1V to -2.1V before FGA; in contrast, it increases two orders after FGA. Consequently, we believe the latter mechanism to be dominant, since only slight increase of ΔL should not be responsible for the huge increase of GIDL and moderate doping density rather than too high doping does GIDL occur (band bending much less than Eg for high doping).

In **Fig. 3.7**, we compare I_D-V_G characteristics of the two samples. No passivation sample shows higher on current (lower R_{SD}), lower off current (narrower depletion width), and better subthreshold swing than the GeO_2 passivation sample. It is not fair to jump to conclusions that GeO_2 passivation sample has inferior performance; instead, thermal budget of S/D dopants should be kept the same at a more equal footing.

Fig. 3.8 demonstrates the gated-diode measurement to detect the interface state density roughly. $I_{gen,s}$ are 6.6×10^{-8}A and 4.0×10^{-8}A for the no passivation and GeO_2 passivation sample after FGA, respectively, indicating D_{it} of no passivation sample is larger than that of GeO_2 passivation sample.

Split–CV before FGA is measured to extract the effective mobility. **Fig. 3.9** shows the

split-CV of the two samples. The effective inversion and depletion charge are the integration of C_{gc} and C_{gb} over V_G respectively, eq. (3.1).

$$Q_{inv} = \int_{V_{FB}}^{V_G} C_{gc} dV_G \; ; \; Q_b = \int_{V_{FB}}^{V_G} C_{gb} dV_G \tag{3.1}$$

The effective mobility and effective electric field can be derived from Q_{inv} and Q_b, eq(3.2).

$$\mu_{eff} = \frac{g_d L}{W Q_{inv}} \; ; \; E_{eff} = \frac{Q_b + Q_{inv}/\eta}{\varepsilon_{Ge}}, \eta = 2 \text{ for electrons and 3 for holes} \tag{3.2}$$

The μ_{eff} - E_{eff} plot is depicted in **Fig. 3.10** [2] and no passivation as well as GeO_2 passivation sample have their high field mobility 1.3X and 1.7X higher than the Si universal curve respectively, where higher mobility of GeO_2 passivation sample is attributed to the better interface quality and less coulomb scattering.

An unusual phenomenon is observed where mobility seems to degrade after FGA, as demonstrated in **Fig. 3.11**. From our data, the slope of C_{gc} is much steeper after FGA so that Q_{inv} becomes much larger at the same gate bias, while drain conductance (g_d) only increases slightly. The much larger Q_{inv} and little increase of g_d lead to lower mobility after FGA, which is not consistent with the field effect mobility (g_m increases after FGA). We still need more time to figure out the mechanisms behind it.

3.3.3 Charge Trapping Behavior of Ge p-MOSFETs

For Ge PMOSFET, the GeO_2 passivation sample shows more hole trapping than no passivation sample under static stress V_G-V_{th} = -4V, caused by bulk traps in GeO_2 and border traps at the GeO_2/Al_2O_3 interface (see **Fig. 3.12a**). Besides, the γ value of zafar model [3] is extracted to be 0.17 and 0.22 for GeO_2 passivation and no passivation respectively. Smaller γ represents wider distribution of the capture time and more short time constant slow traps existed, indicating ratio of early traps is larger for GeO_2 passivation sample, as depicted in **Fig. 3.12b**. Also, GeO_2 passivation sample shows a little more severe SS degradation under static stress (**Fig. 3.12c**).

3.4 Charge Pumping Applicability on Ge MOSFET

3.4.1 Review of Charge Pumping Theory

The charge pumping method requires fully functional MOSFETs as test structures. The MOSFET source and drain are tied together and reverse biased with voltage V_R, while a time varying gate voltage is applied to drive the surface under the gate into inversion and accumulation. The charge pumping current is measured at the substrate, at the source/drain tied together or at the source and drain separately.

At a certain energy level, the emission process is no longer capable of evacuating carriers sufficiently fast from the traps to keep up with the changing Fermi level and the equilibrium distribution of carriers in the traps can no longer be maintained (a non quasi-static condition occurs). It continues until V_{th} or V_{fb} is reached, and then recombination takes place. Charge pumping current is originated from the net recombination of charge located between $E_{em,e}$ (lowest energy level electrons being emitted as holes rush to surface) and $E_{em,h}$ (highest energy level holes being emitted as electrons rush to surface), making the carriers flow into the S/D (substrate) larger than flow out of it[4].

3.4.2 Average D_{it} and Capture Cross Section Extraction

Fixed amplitude charge pumping method was applied on the Ge p-MOSFFET (**Fig. 3.13)** and the maximum value of I_{CP} is used to estimate the mean D_{it} near the midgap. Sufficiently high frequencies (500 kHz- 2 MHz) were chosen to avoid the influence of traps in the high-k dielectric in order to study the interface traps at the Ge-Oxide interface only. Charge pumping current is proportional to the amount of interface traps located between electron and hole emission levels, as expressed in eq. (3.1)

$$I_{cp} = q\,A\,f \int_{E_{em,h}}^{E_{em,e}} D_{it}\,(E)dE \quad \text{or} \quad I_{cp} = q\,A\,f\,\overline{D_{it}}\,(E_{em,e} - E_{em,h}) \tag{3.1}$$

Therefore, the average D_{it} value between $E_{em,e}$ and $E_{em,h}$ is $\overline{D_{it}} = \frac{I_{cp}}{q\,A\,f\,(E_{em,e}-E_{em,h})}$, where the position of $E_{em,e}, E_{em,h}$ should be evaluated first, shown from eq.(3.2) to (3.4).

$$E_{em,e} = E_i + kT\ln\left(\frac{1}{V_{th,e}\sigma_n n_i t_{em,e}}\right);\ E_{em,h} = E_i - kT\ln\left(\frac{1}{V_{th,h}\sigma_p n_i t_{em,h}}\right) \quad (3.2)$$

$$t_{em,e} = \frac{|V_{TH}-V_{FB}|}{\Delta V_A}t_f;\ t_{em,h} = \frac{|V_{TH}-V_{FB}|}{\Delta V_A}t_r \quad (3.3)$$

Capture cross section of hole and electron are still unknown quantities, but the geometrical average of them can be calculated by extrapolating t_r/t_f so that I_{cp} becomes zero, eq. (3.4).

$$I_{cp} = qAf\,\overline{D_{it}}\left(E_{em,e} - E_{em,h}\right) = 2qAf\,\overline{D_{it}}\,kT\,\ln\left(\frac{1}{V_{th}n_i\sqrt{\sigma_p\sigma_n}\frac{|V_{TH}-V_{FB}|}{\Delta V_A}\sqrt{t_r t_f}}\right) \quad (3.4)$$

I_{cp} versus transition time are plotted in **Fig. 3.14**, and the t_r/t_f corresponding to zero I_{cp} current are equal to 2.63×10^{-5}s and 1.29×10^{-5}s for GeO_2 passivation and no passivation sample, indicating that $\sqrt{\sigma_p\sigma_n}$ are 5.4×10^{-16} cm^2 and 1.1×10^{-15} cm^2 respectively. The $\sqrt{\sigma_p\sigma_n}$ derived from conductance method for 500℃ GeO_2 passivation is 4.6×10^{-16} cm^2, with similar result obtained from two different approaches. 5.4×10^{-16} cm^2 and 1.1×10^{-15} cm^2 are substituted into eq. (3.2) with t_r/t_f 100ns, ΔV_A=1.3V, and $\left(E_{em,e} - E_{em,h}\right)$ are 0.28eV (GeO_2) and 0.24eV for the two samples. Thus, $\overline{D_{it}}$ after FGA between $E_{em,e}$ and $E_{em,h}$ is $4.2\times10^{11}cm^{-2}eV^{-1}$ for 500℃ GeO_2 passivation (consistent with the result from conductance method) and $1.1\times10^{12}cm^{-2}eV^{-1}$ for no passivation sample.

Charge pumping is one of the most reliable and sensitive techniques for D_{it} characterization, but only a very small part of the Ge bandgap, close to midgap region, can be scanned at room temperature. The interface trap density ($\frac{Icp}{q\,A\,f}$, $\#/cm^2$) is strongly underestimated because the traps near the band edges are not measured. Based on the emission level theory, the positions of electron and hole emission level of Ge as a function of t_r/t_f at different temperatures are calculated, as shown in **Fig. 3.15.** It is concluded that low-temperature measurements or transition times down to 6ns at 300K with high-frequency setup of 1GHz bandwidth enable us to probe the D_{it} closer to band edges [5].

3.4.3 D_{it} Distribution in Ge Band Gap

The energy distribution of D_{it} is obtained by using variable rising time and falling time. By changing t_f while keeping t_r constant, the energy is gradually swept through upper band gap and D_{it} at different electron emission energy ($E_{em,\ e}$) can be extracted. Likewise, by changing t_r while keeping t_f constant, lower bandgap D_{it} profile can be illustrated. **Fig. 3.16** shows the I_{cp} versus base voltage graph for fixed t_r, changing t_f and fixed t_f, changing t_r [6]. They are converted to D_{it} distribution according to eq. (3.5).

$$D_{it}(E_{em,e}) = -\frac{t_f}{qAkTf}\frac{dI_{CP}}{dt_f}\ (t_r \text{ constant})\ ;\ D_{it}(E_{em,h}) = -\frac{t_r}{qAkTf}\frac{dI_{CP}}{dt_r}\ (t_f \text{ constant}) \qquad (3.5)$$

Fig. 3.17 depicts the D_{it} distribution in the Ge band gap, and the passivation sample truly exhibits lower D_{it} value. Symmetric distribution is attained and consistent with conductance method again. Unfortunately, we are not able to obtain the midgap profile. In order to make the $E_{em,e}, E_{em,h}$ approach the midgap, t_r/t_f much longer than 100ns (at least 1μs) should be applied so that low frequency measurement (lower than 50 kHz) is needed. For low frequency measurement practical, annealing condition must be optimized and our $100\mu m^2$ junction area should be smaller.

3.4.4 Limitations of Charge Pumping on Ge

The biggest obstacle using charge pumping on Ge is that junction leakage and noise can jeopardize charge pumping measurements, especially for large and defective Ge junctions. The small voltage difference between S/D and bulk can be sufficient to cause leakage currents to dominate charge pumping currents. For charge pumping measurements to be effective, it is preferable to have well optimized and small junctions.

There exist issues for charge pumping at low temperatures related to electrical contacts. The series resistance might increase at low temperature due to freeze-out of Schottky contacts, while Charge pumping measurements are sensitive to excessive series resistance.

3.5 Conclusions

In Chapter 3, we investigated the effect of FGA on Ge p^+n junction and device characteristics. On/off ratio of our p^+n junction and p-FET reached 4.8 orders and 3 orders respectively (500℃ 30s dopant activation, W/L = 100μm/10μm), with better on/off ratio (3.3 orders) and subthreshold swing (170mv/dec) obtained after FGA. Charge pumping measurement was done to obtain the midgap D_{it} information, and $\overline{D_{it}}$ after FGA between $E_{em,e}$ and $E_{em,h}$ is $4.2\times10^{11}cm^{-2}eV^{-1}$ for 500℃ GeO_2 passivation and $1.1\times10^{12}cm^{-2}eV^{-1}$ for no passivation sample. Besides, $\sqrt{\sigma_p\sigma_n}$ were 5.4×10^{-16} cm^2 and 1.1×10^{-15} cm^2 for samples with and without GeO_2 passivation respectively. Both $\overline{Dit}$ and $\sqrt{\sigma_p\sigma_n}$ were consistent with the results derived from conductance method applied to MOSCSPs in Chapter two, reconfirming the validity of conductance method.

Pros and cons of adding the GeO_2 layer were summarized according to our experimental data. Lower D_{it} value verified from either charge pumping or gated diode measurement made the mobility higher for GeO_2 passivation sample, while it suffered from more severe carrier-trapping due to border traps at the GeO_2/Al_2O_3 interface and more severe subthreshold swing degradation.

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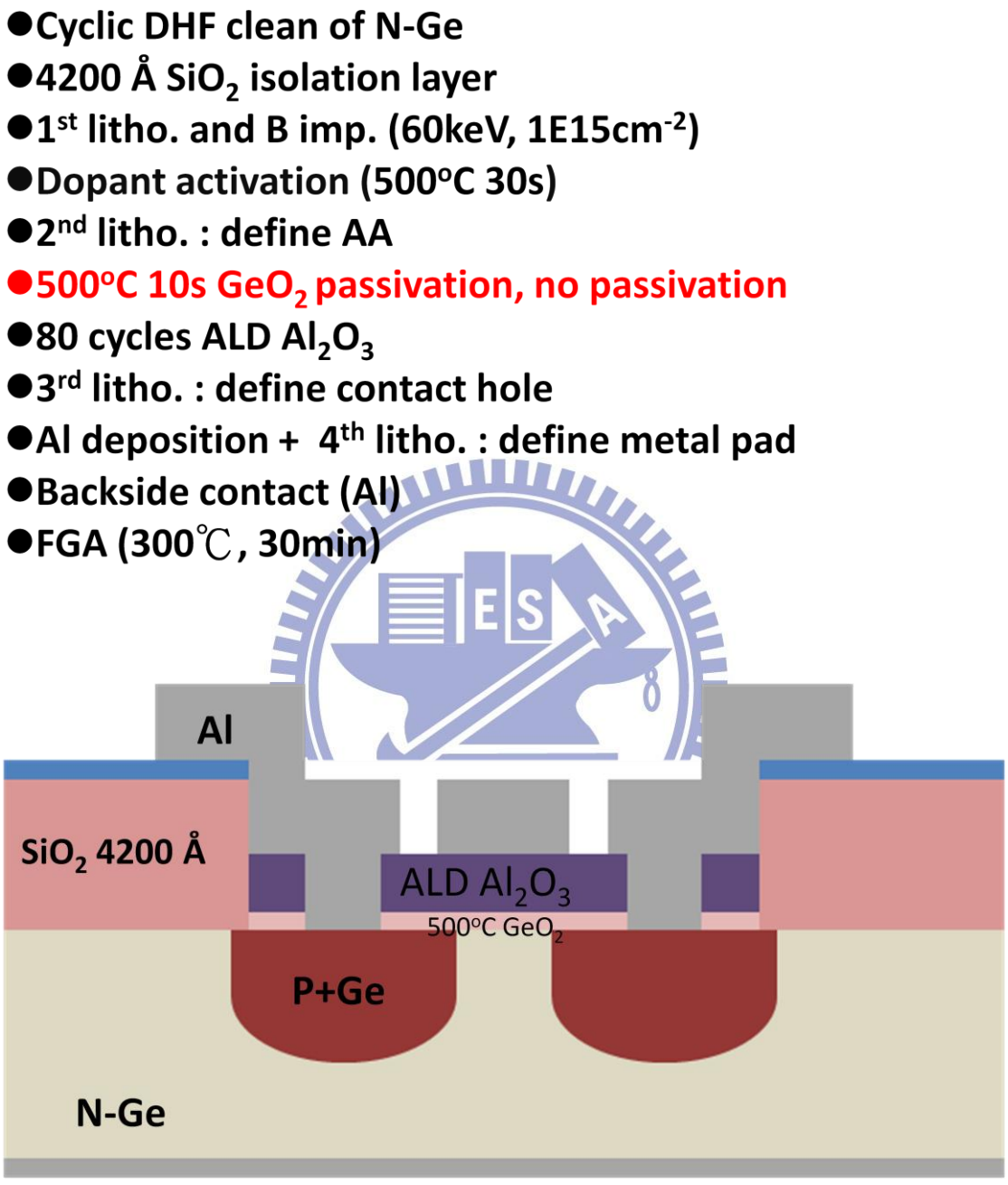
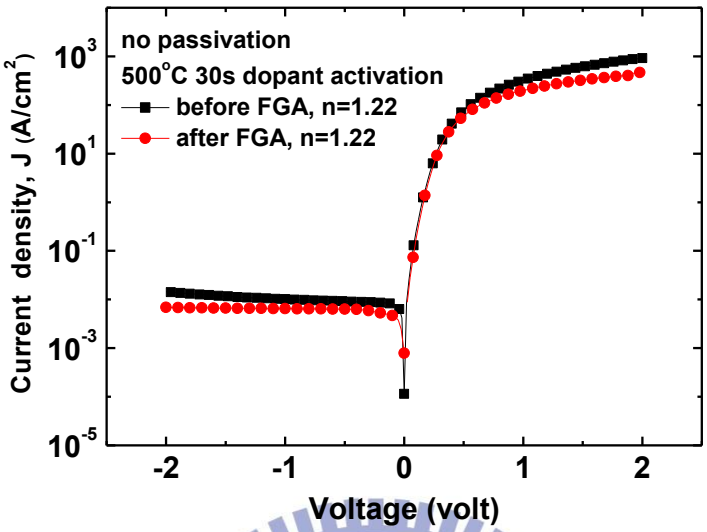
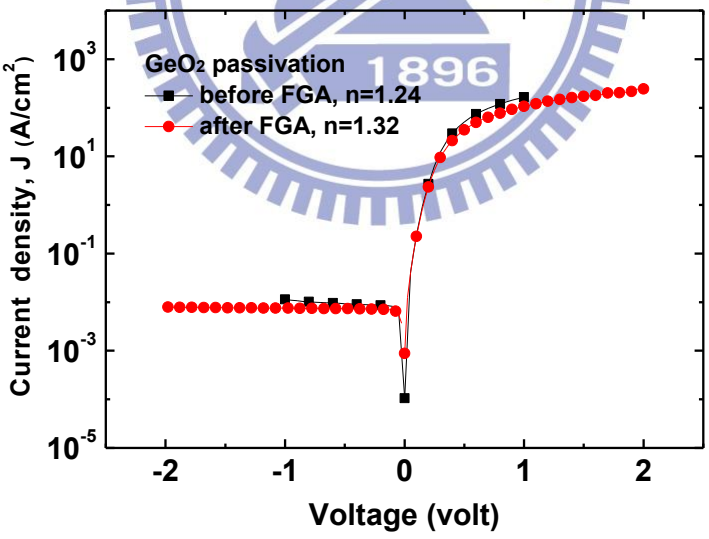


Fig. 3.1 Process flow of Ge p-MOSFETs and their device structure.

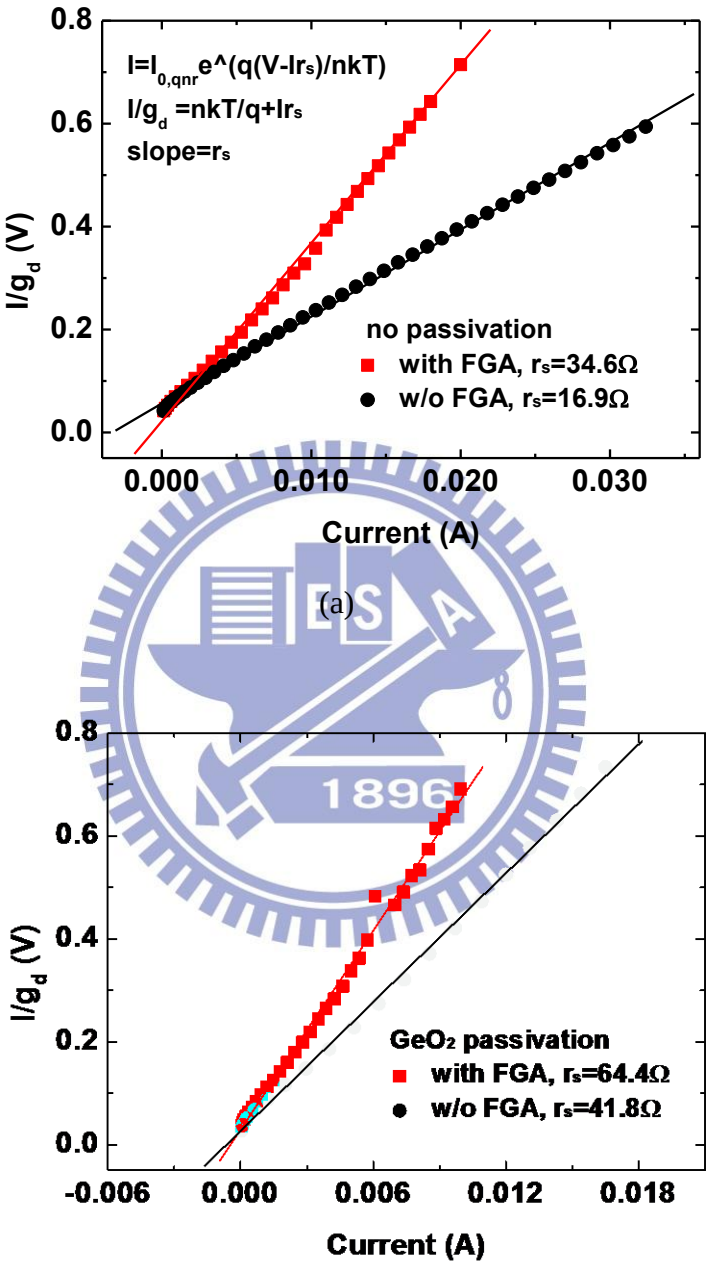


(a)



(b)

Fig. 3.2 I–V characteristics of p^+n junctions activated at 500℃ of the two samples, before and after performing FGA. (a) No passivation (b) GeO_2 passivation



(a)

(b)

Fig. 3.3 Series resistance extracted from p^+n junctions of the two samples, before and after performing FGA. (a) No passivation (b) GeO_2 passivation

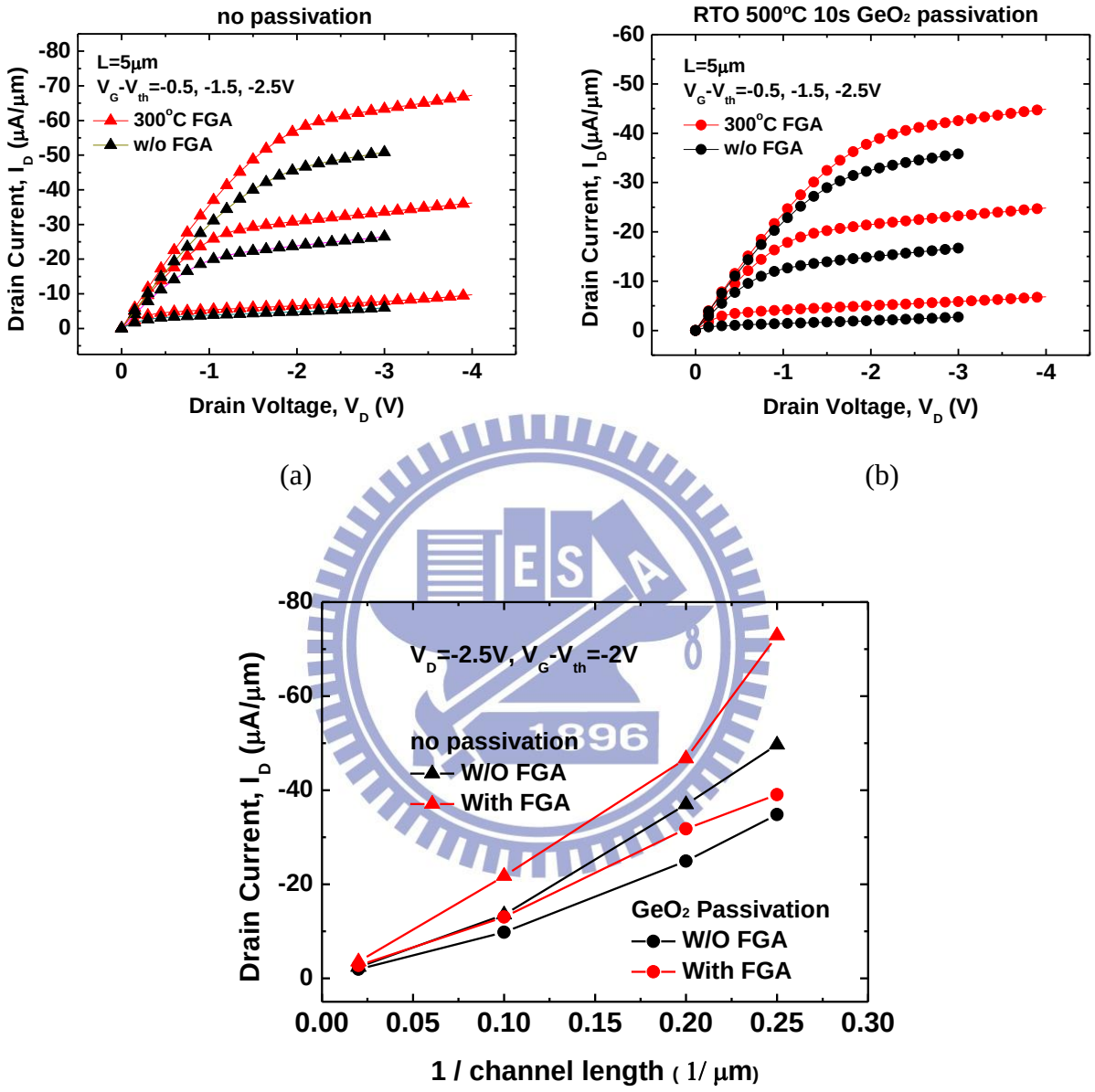
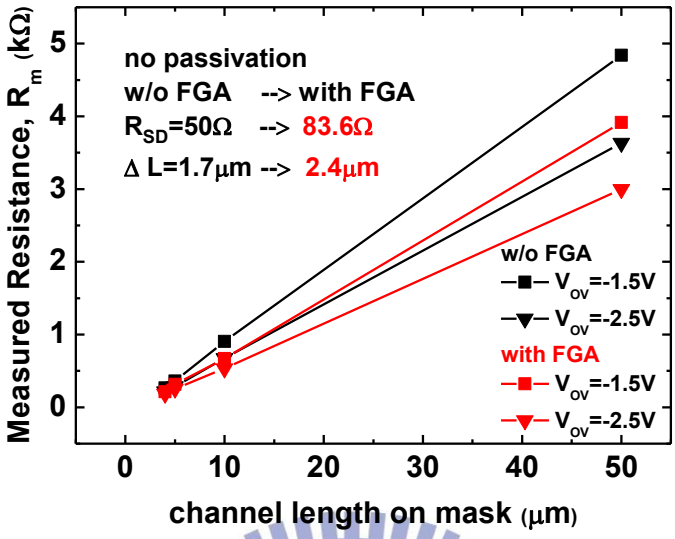
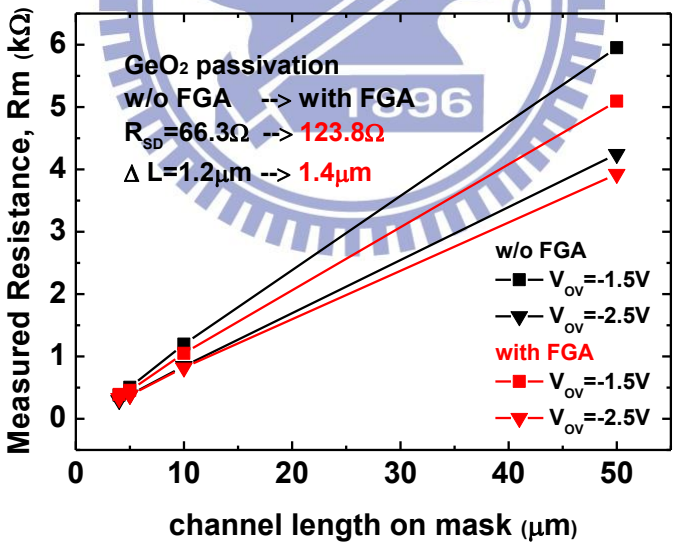


Fig. 3.4 Effects of FGA at 300℃ on the I_D-V_D characteristics of Ge p-MOSFETs. (a) No passivation. (b) GeO_2 passivation. (W/L=100μm/5μm) (c) I_D characteristics with various gate lengths.

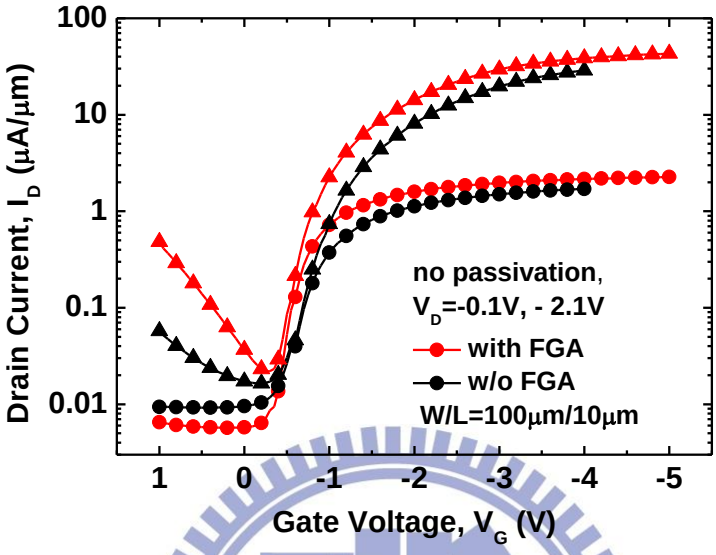


(a)

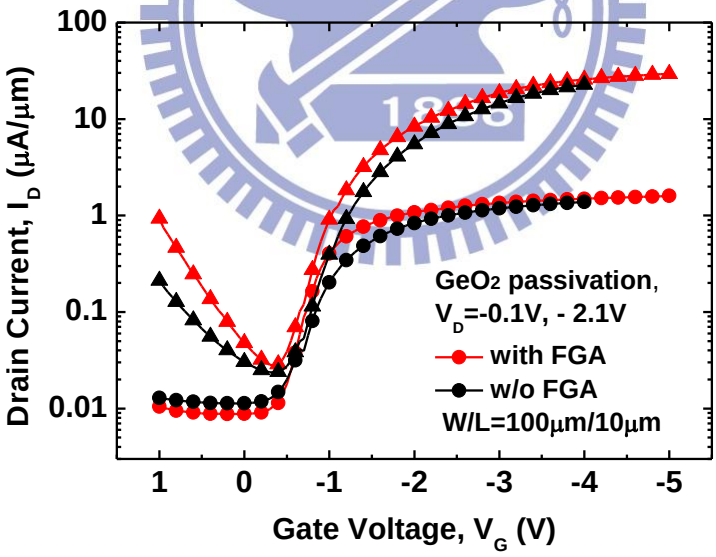


(b)

Fig. 3.5 Effects of FGA at 300℃ on the series resistance from Terada and Muta method. (a) No passivation. (b) GeO_2 passivation.



(a)



(b)

Fig. 3.6 Effects of FGA at 300℃ on the I_D-V_G characteristics of Ge p-MOSFETs. (a) No passivation. (b) GeO_2 passivation.

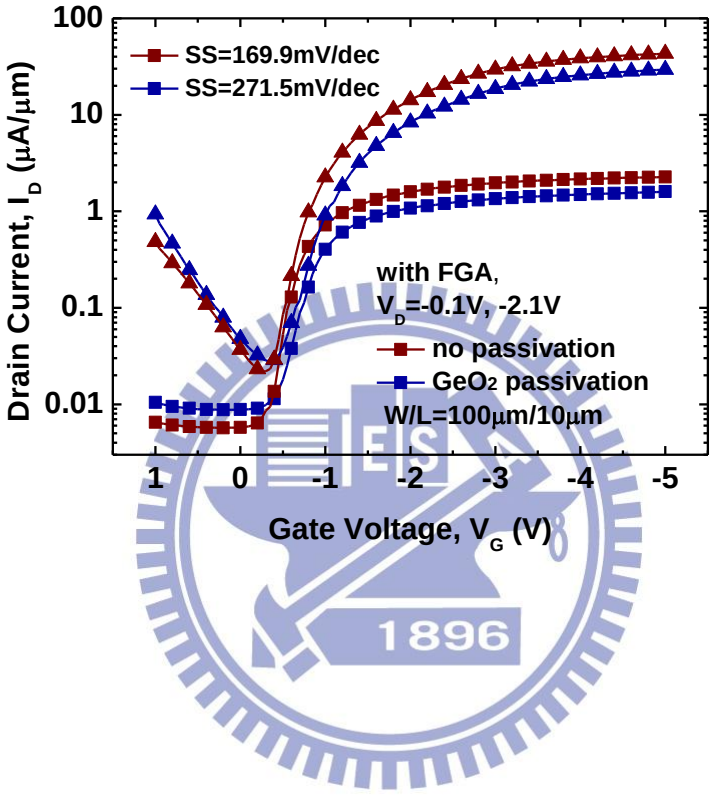


Fig. 3.7 Comparison of I_D-V_G characteristics between no passivation and GeO_2 passivation sample.

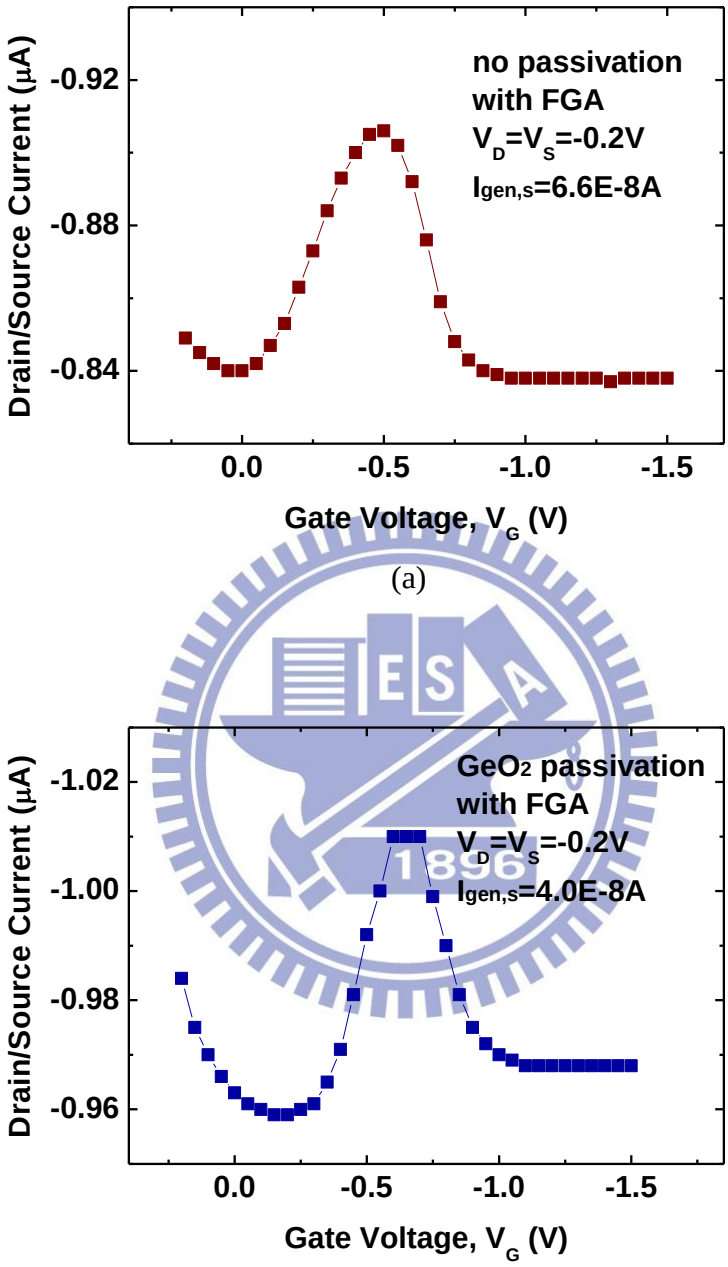
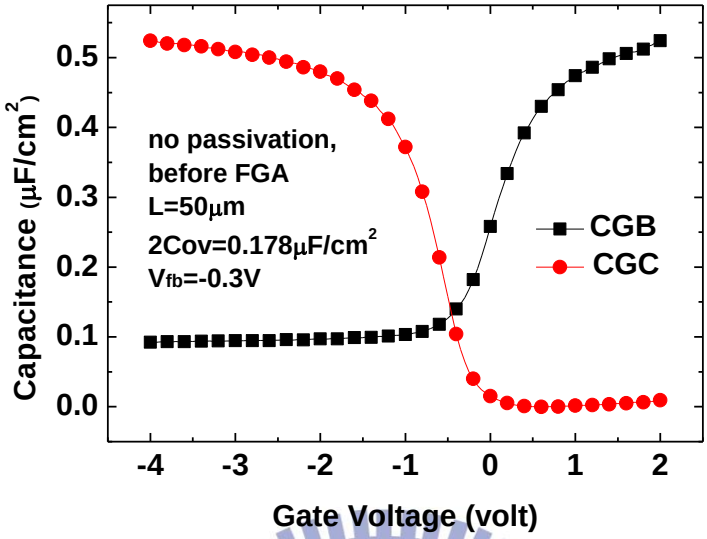
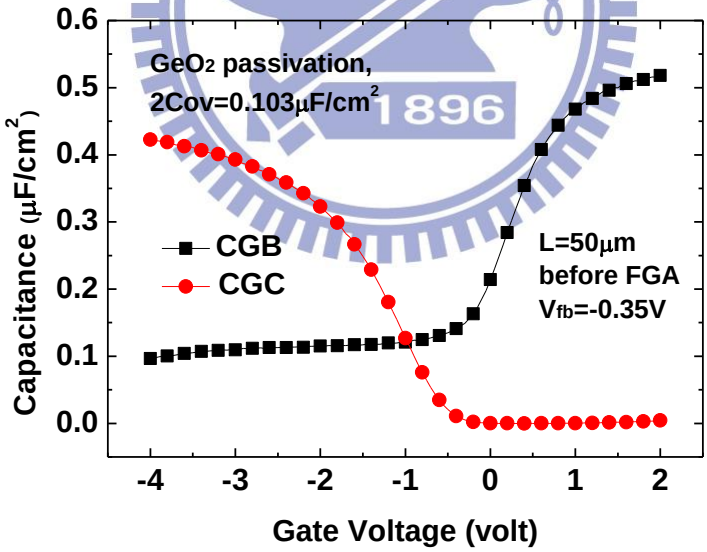


Fig. 3.8 Gated-diode measurement detects the interface state density roughly. (a) No passivation. (b) GeO_2 passivation.



(a)



(b)

Fig. 3.9 Split-CV before FGA is measured. (a) No passivation. (b) GeO_2 passivation.

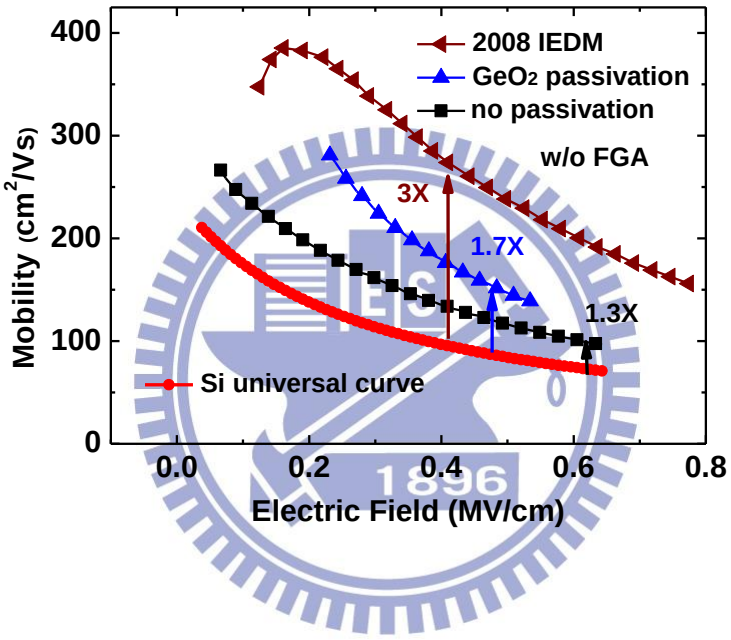


Fig. 3.10 Effective mobility VS effective electric field is plotted before FGA with the highest published hole mobility up to date.

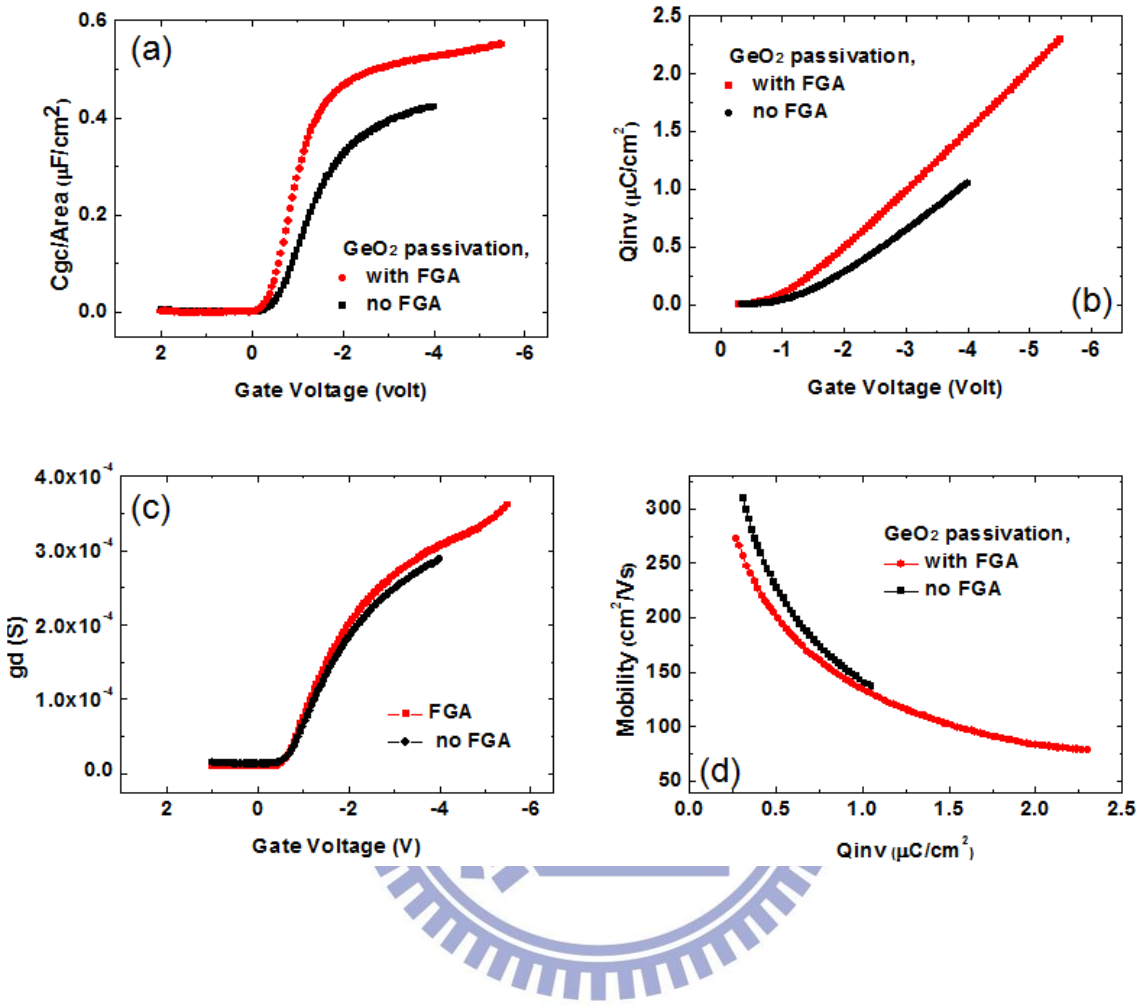
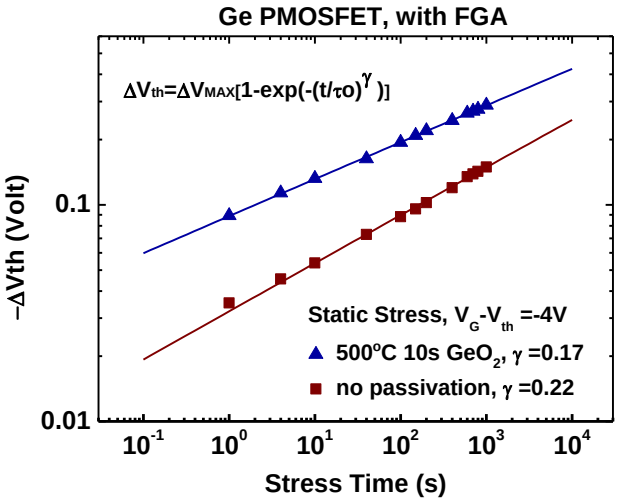
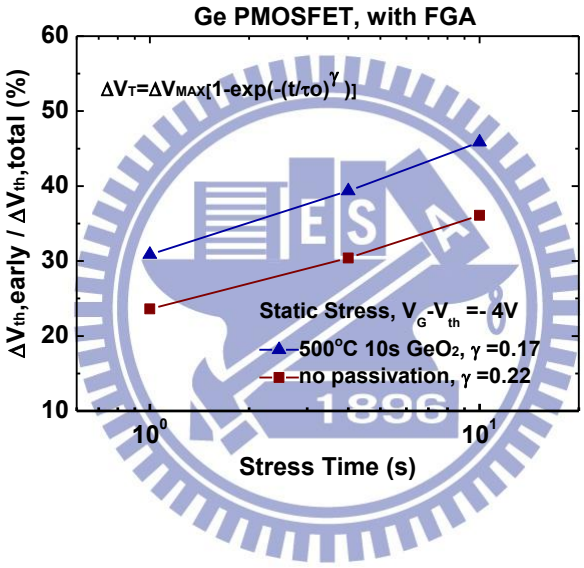


Fig. 3.11 Effects of FGA at 300℃ on the effective mobility of GeO_2 passivation Ge p-MOSFETs. (a) C_{gc}-V_G plot. (b) Q_{inv}-V_G plot. (c) g_d-V_G plot. (d) μ_{eff} - Q_{inv} plot.



(a)



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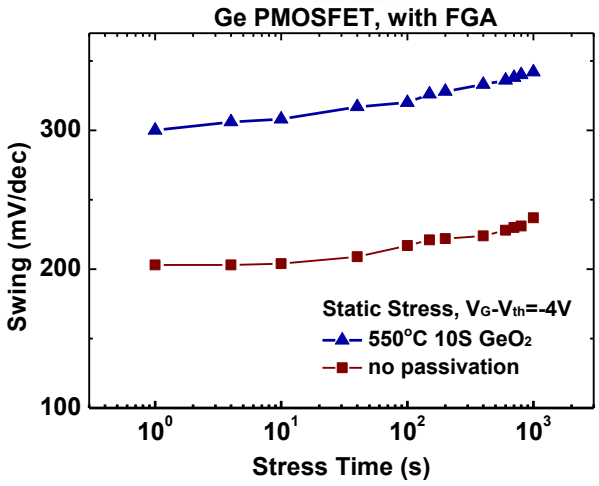
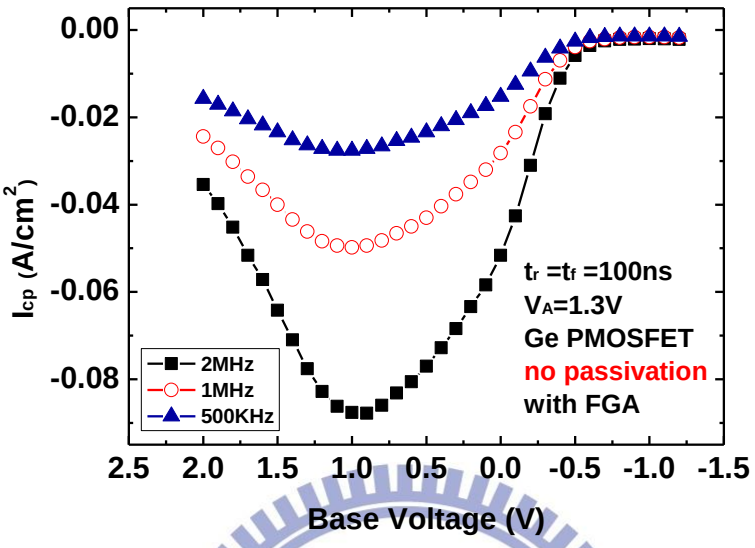


(c)

Fig. 3.12 Reliability is compared between no passivation and GeO_2 passivation sample under static stress after FGA. (a) Charge trapping behavior. (b) Ratio of early traps. (c) Subthreshold swing degradation.



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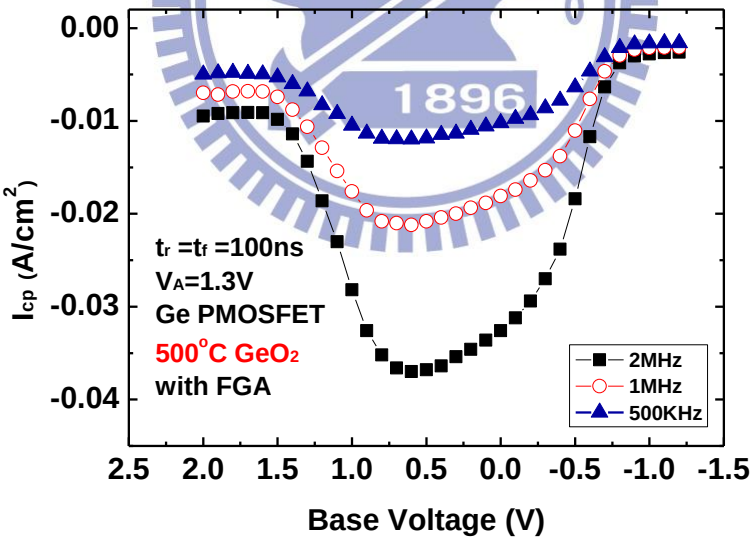
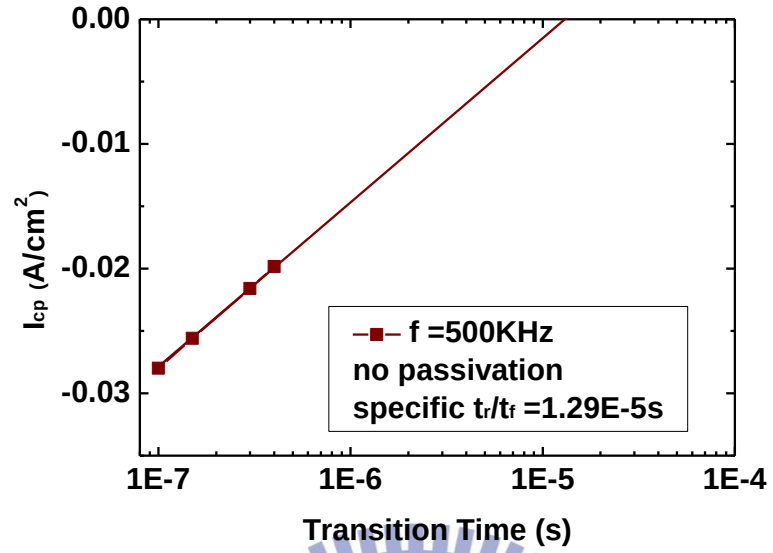


(b)

Fig. 3.13 Fixed amplitude charge pumping method was applied on the Ge p-MOSFFET after FGA. (a) No passivation. (b) GeO_2 passivation.



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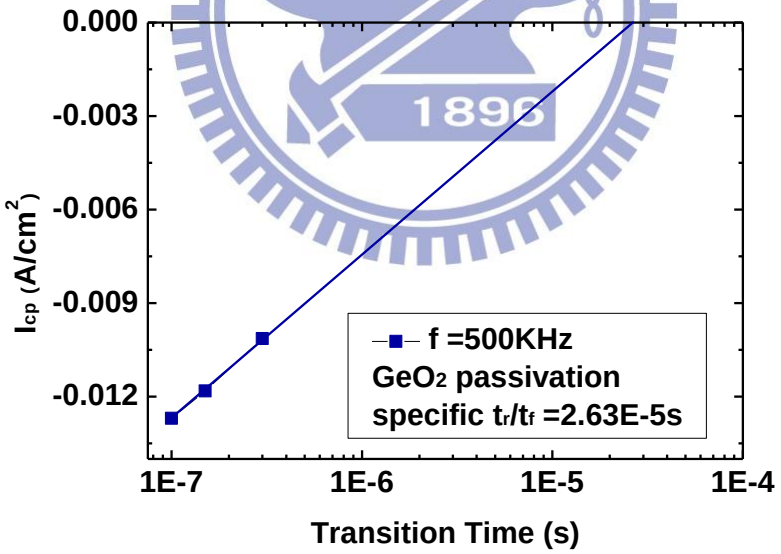


(b)

Fig. 3.14 I_{cp} versus transition time are plotted after FGA, with specific t_r/t_f extracted. (a) No passivation. (b) GeO_2 passivation.

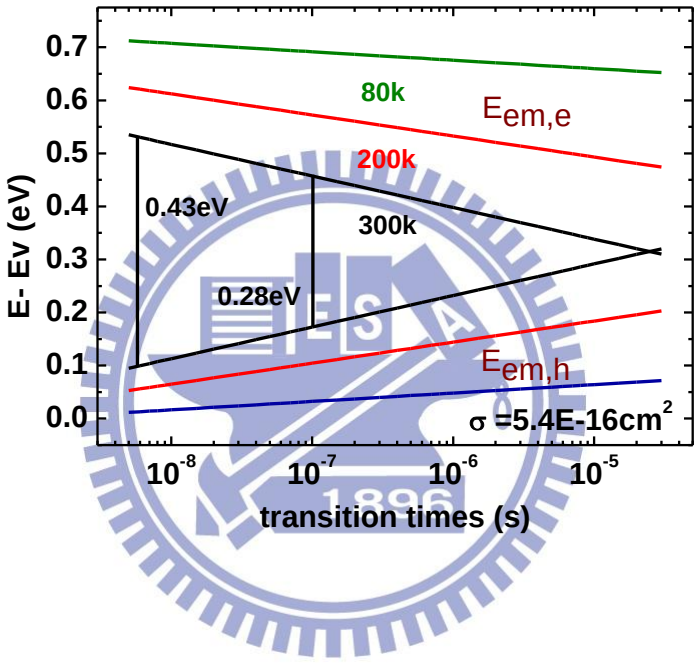
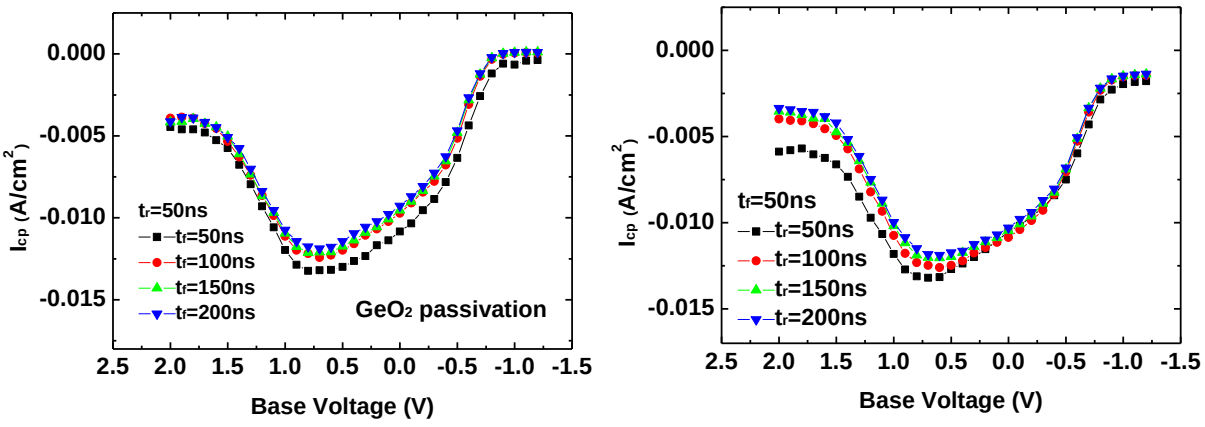


Fig. 3.15 Positions of electron and hole emission level of GeO_2 passivation sample as a function of t_r/t_f at different temperatures are calculated.



(a) (b)

Fig. 3.16 I_{cp} versus base voltage of GeO_2 passivation after FGA are measured. (a) Fixed t_r, changing t_f (b) Fixed t_f, changing t_r.

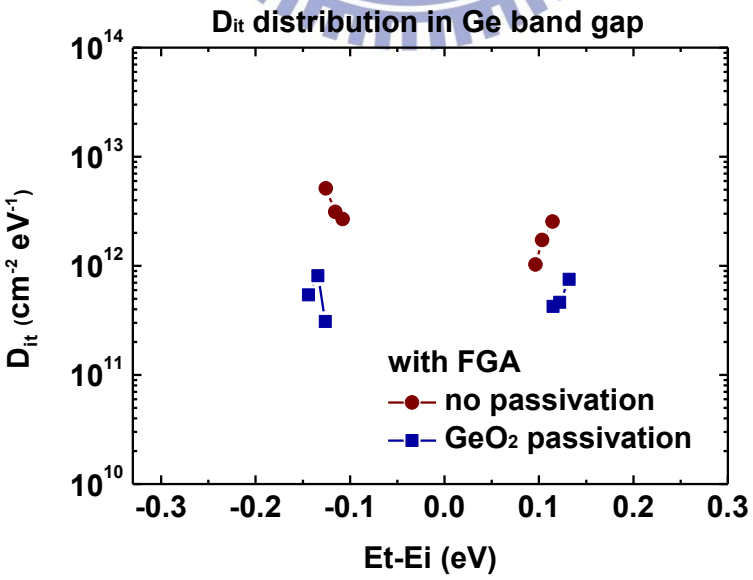


Fig. 3.17 D_{it} distribution in the Ge band gap of the two samples is depicted.

Chapter 4

Inversion-Mode Ge n-MOSFET with Atomic-Layer-Deposited Al_2O_3 Gate Dielectrics

4.1 Introduction

Ge has become of great interest as a channel material for future technology nodes, owing to its high bulk electron and hole mobility. Although high-k/Ge p-MOSFET with mobility 3X higher than Si universal curve has been reported recently [1], the performance of promising Ge n-MOSFETs is still unsatisfactory with low extracted electron mobility. The mechanisms of n-MOSFET degradation can be explained in terms of fast trapping at Ge/GeO_2 interface, slow trapping by GeO_2/Al_2O_3 border traps and parasitic S/D series resistance [2]. Passivation of Ge interface and activation of n-type dopants have been considered the major challenges to achieve high performance Ge CMOS.

In this chapter, SiO_2/GeO_2 isolation is demonstrated to be better than the SiO_2 isolation, with the underlying leakage paths and mechanisms analyzed. Then, the device electrical characteristics of Ge n-MOSFET with different GeO_2 thickness are discussed, including series resistance, subthreshold swing, and mobility. The interface qualities for different samples are characterized by charge pumping and gated-diode measurement, in order to find the correlation between interface quality and device characteristic. Reliability issues for GeO_2 are investigated through applying constant voltage stress, and it is confirmed that low conduction band offset of GeO_2 on Ge is a potential problem.

4.2 Fabrication of Gate-Last Ge n-MOSFET

(100)-oriented p-Ge substrate doped with Ga at level of 2E15cm^{-3} (resistivity ca. 2Ω·cm) was used for Ge NMOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide. Then, a 550℃ 60s GeO_2 layer was added (for some samples) before 420-nm-thick SiO_2 layer capped by PECVD, acting as the field oxide.

First, the (source/drain) region was opened through the 1st Mask, followed by implantation of the P (1×10^{15} cm^{-2}, 30 keV) into the p-Ge, while dopant activation condition was 700℃, 30s. Next, active area (AA) was opened through the 2nd Mask, and the wafers were split into two conditions: a 550℃ 10s GeO_2 and a 550℃ 60s GeO_2 passivation sample. After that, an 80 cycles ALD-Al_2O_3 was deposited as the high-k gate dielectric. Right after excavating the contact hole on S/D region through the 3rd Mask, a 400nm Al metallization was performed which was then patterned to define metal pads through the 4th Mask. Finally, a 400nm Al layer was deposited as the backside contact.

The process flow and device structure are shown in **Fig. 4.1**.

4.3 Result and Discussion

4.3.1 SiO_2/GeO_2 Isolation VS SiO_2 Isolation

Junction characteristic of the Ge n-MOSFET with the same annealing condition but with different isolation is discussed, in order to obtain a low reverse bias current of junction and thus low off state current of MOSFET. It is believed that junction leakage is composed of area leakage J_A below the drain and isolation leakage J_I at the drain-isolation interface. Since it is proved that GeO_2 passivation reduces the D_{it} value, we expect the junction leakage to be suppressed effectively. **Figures 4.2(a) (b)** demonstrate the comparison of junction IV for

different isolation and illustrations to explain the characteristic. Isolation with GeO_2 passivation exhibits lower reverse current and larger forward current, which are explained by less generation and less recombination occur when biasing in reverse and forward bias respectively.

4.3.2 N^+P Ge Junction Characteristics

The presence of an n^+p shallow junction having an acceptable leakage current is critical to obtain high-performance Ge n-MOSFETs. Previous studies of P ion implantation into Ge [3], [4] have revealed that an RTA temperature above 500℃ is essential to achieve sufficient dopant activation and full recrystallization of the amorphous Ge region. In this study, we found that an annealing temperature of 500℃ was insufficient to repair all of the implant-induced damage. Raising the temperature to 700℃ decreased the value of J_R to 1.9×10^{-2} A/cm^2 at 2V, a reduction of more than one order of magnitude relative to the 500℃ annealing but with similar J_F, as indicated in **Fig. 4.3(a)**. The junction characteristic of n-MOSFETs with different GeO_2 thickness is compared in **Fig. 4.3(b)** with on/off ratio of 4.2 orders in both cases, but junction leakage seems unacceptably high compared with the Si device. Not much difference is observed between the two samples because 700℃ 30s thermal budget is much larger than additional 550℃ 50s for GeO_2 layer under high-k dielectric while little J_F degradation is caused by more dopant diffusion and slight series resistance increase.

4.3.3 Basic Device Characteristics

Fig. 4.4 displays the I_D-V_D characteristics of the n-MOSFETs without FGA. Drain current at low drain voltage is not linearly increasing as V_D increases due to the large series resistance. In **Fig. 4.5**, I_D-V_G characteristics shows the on/off ratio to be about three orders of magnitude, while much inferior subthreshold swing compared with p-MOSFET (450 mV/dec for 550℃ 60s GeO_2 passivation sample) is attained. From linear region of I_D-V_D curves for different gate

overdrive and various gate lengths, we are able to extract the S/D series resistance by the Terada and Muta method (see **Fig. 4.6**). For the two samples, source/drain series resistance (R_{SD}) are both larger than 1.7kΩ, which are much larger than the p-FET counterparts. In our experiments a higher thermal budget (700℃, 30s) is required for n-type dopant activation, which causes more dopant diffusion (either out of the surface or into the substrate) and lower electrical activation, accounting for the observed larger series resistance (sheet resistance and contact resistance) in Ge NMOSFET. Large series resistance leads to drain conductance and thus mobility degradation. Also, we believe the much inferior subthreshold swing compared with p-MOSFET is due to the series resistance, which degrades the drain current at low V_D.

Fig. 4.7 demonstrates the gated-diode measurement to detect the interface state density roughly. $I_{gen,s}$ are 4.32E-8A and 3.97E-8A for 550℃ 10s and 550℃ 60s GeO_2 passivation sample respectively, indicating thicker GeO_2 thickness lowers the D_{it} value but causes drain current to decrease .

Split–CV is measured to extract the effective mobility. **Fig. 4.8 (a)** shows the effective mobility as a function of Q_{inv} compared with other published data [2] [5], revealing that thicker GeO_2 sample has little enhancement in mobility due to less coulomb scattering. Since S/D parasitic resistance can result in a significant reduction in the drain voltage falling across the channel and influence the drive current as well as the effective mobility extraction, the effective inversion mobility with R_{SD} eliminated is depicted in **Fig. 4.8 (b)**, utilizing eq. (4.1).

$$\mu_{eff} = \frac{L_{eff}}{W_{eff} Q_{inv} \left(\frac{1}{g_d} - R_{SD} \right)} \tag{4.1}$$

In fact, the true mobility should be even higher if we take interface trap charges into account. [6] The integration of C_{gc} includes not only Q_{inv} but also Q_{it}, so that Q_{inv} is overestimated and mobility is indeed higher.

4.3.4 Charge Trapping Behavior of Ge n-MOSFETs

The slow trapping can occur via bulk traps of high-k dielectric or border traps between interfacial transition oxide and high-k dielectric, where the traps are so slow that they can respond only to DC sweep but not AC frequency. GeO_2 has its a potential problem due to low conduction band offset (0.6eV for CB offset and 3.8eV for VB offset) with Ge[2], which can cause severe charge trapping in bulk traps of Al_2O_3 and the slow traps at GeO_2/Al_2O_3 interface.

For our Ge n-MOSFETs, either thicker GeO_2 passivation or thinner GeO_2 passivation show more severe charge trapping under static stress compared with Ge p-MOSFETs as expected because of much lower conduction band offset and the preference of electron trapping (**Fig. 4.9a**). Besides, the γ value of zafar model is extracted to be 0.15 and 0.17 for 550℃ 10s and 550℃ 60s GeO_2 passivation sample respectively. Smaller γ represents wider distribution of the capture time and more short time constant slow traps existed, indicating ratio of early traps is larger for 550℃ 10s GeO_2 passivation sample, as depicted in **Fig. 4.9b**. Thinner GeO_2 sample exhibits more V_{th} shift in the beginning, because tunneling into GeO_2/Al_2O_3 interface is faster. However, thicker GeO_2 sample eventually shows more V_{th} shift than the thinner one as stress time becomes longer which is attributed to more total amount of slow traps (traps in GeO_2 layer). Therefore, a crossover point is observed. From **Figs. 4.9(a) and (c)**, it is observed that the crossover point shifts to lower stress time (18.5s→1.5s) as static stress voltage increases. We believe the effect of different capture rate at GeO_2/Al_2O_3 interface in the beginning diminishes for larger stress voltage.

Besides, thicker GeO_2 passivation sample shows better subthreshold swing due to better interface quality, while not much difference in swing degradation is observed. Also, it's intuitive to expect that more severe swing degradation occurs for larger stress voltage for each sample (Fig. 4.10).

4.4 Conclusions

In Chapter 4, we investigated the characteristics of Ge n^+p junction with different isolation and thermal budget. It was concluded that SiO_2/GeO_2 isolation as well as 700℃ 30s annealing enable us to obtain the lowest reverse bias junction leakage of 1.9×10^{-2} A/cm^2 at 2V and magnitudes of the rectifying ratios reaching 4.2 orders. On/off ratio of our n-FETs (W/L =100μm/10μm) reached 3 orders but series resistance larger than 1.7kΩ was attained which strongly affected the subthreshold swing and mobility extraction. The slightly higher effective mobility for thicker GeO_2 passivation sample was due to better interface quality, which was reconfirmed by lower $I_{gen,s}$ from gated-diode measurement and better subthreshold swing. However, both of our samples had their mobility much lower than the electron universal curve, which could be explained by fast trapping at Ge/GeO_2 interface, slow trapping by GeO_2/Al_2O_3 border traps and parasitic S/D series resistance.

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[6] W. Zhu, J. P. Han, and T.P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-K dielectrics," *IEEE Transactions on Electron Devices*, 51:98-105, 2004.

- Cyclic DHF clean of P-Ge
- 550°C 60s GeO_2 + SiO_2 isolation layer
- 1st litho. and P imp.(30keV, 1E15cm^{-2})
- Dopant activation (700°C 30s, 500°C 60s)
- 2nd litho. : define AA
- GeO_2 passivation (550°C 10s, 60s) +80 cycles ALD Al_2O_3
- 3rd litho. : define contact hole
- Al deposition + 4th litho. : define metal pad
- Backside contact (Al)

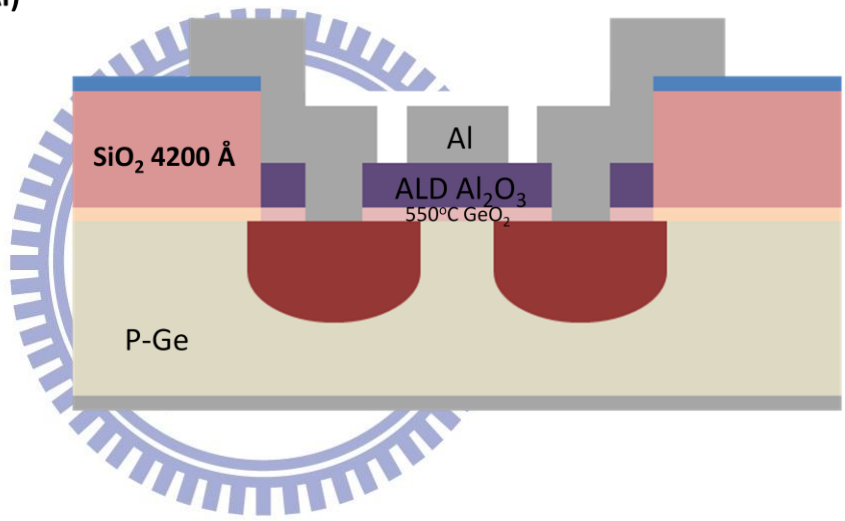


Fig. 4.1 Process flow of Ge n-MOSFETs and their device structure.

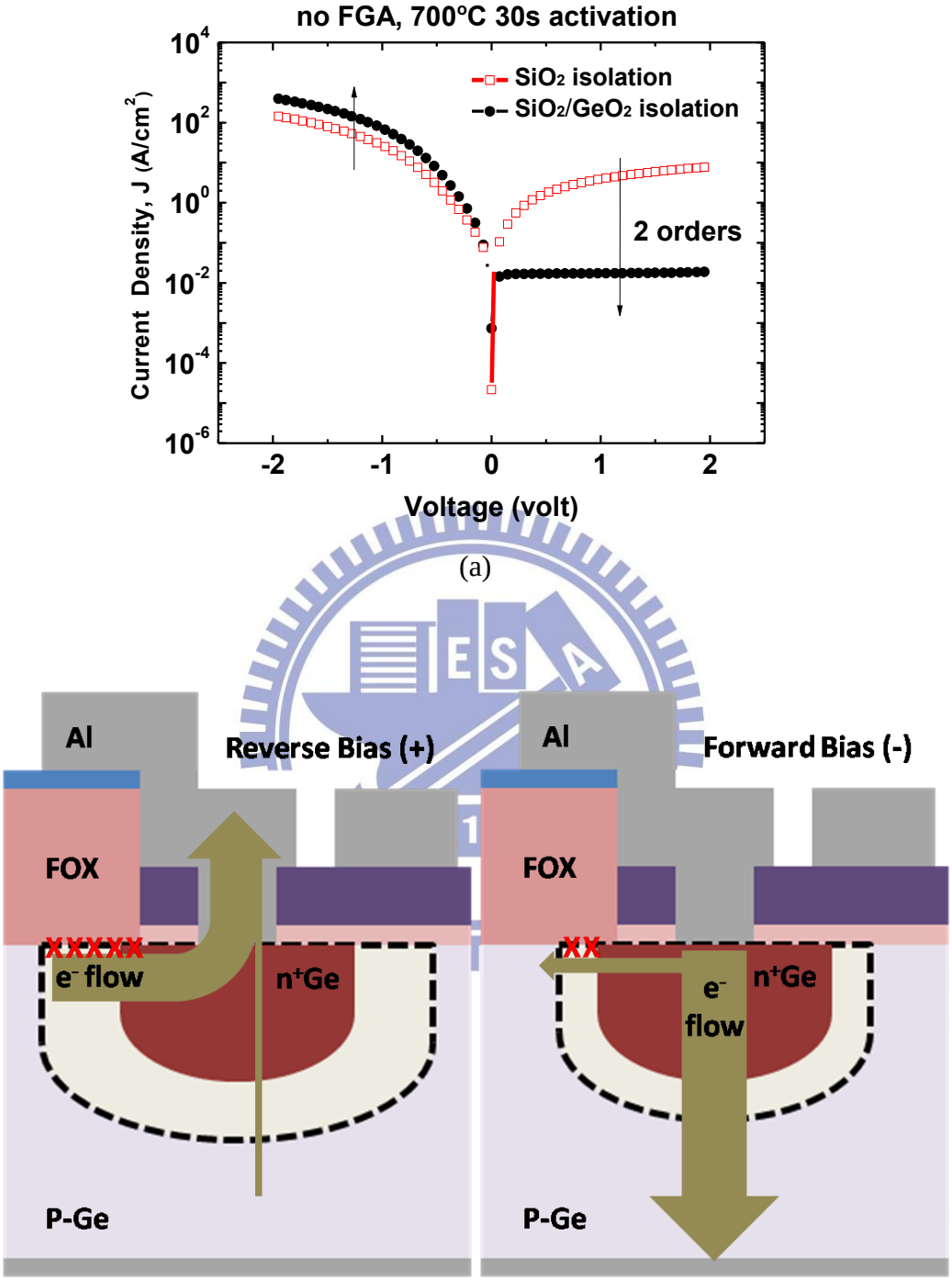
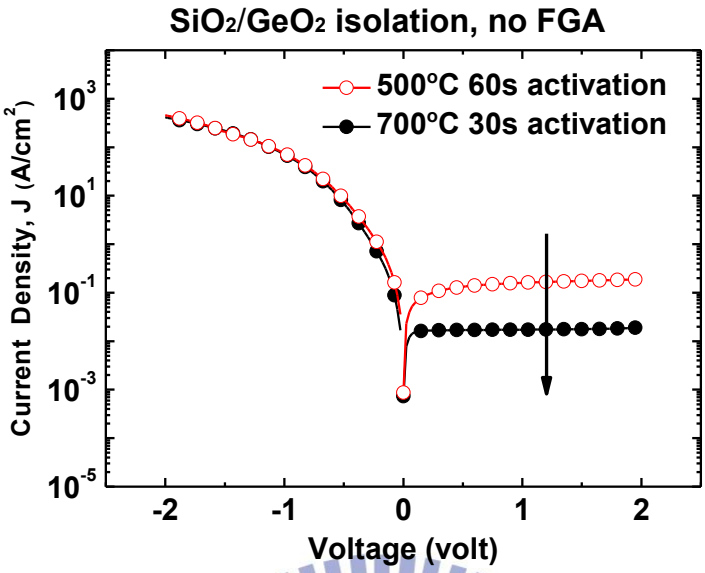


Fig. 4.2 (a) Junction IV is compared for different isolation. (b) Illustrations to explain the junction characteristic in (a).



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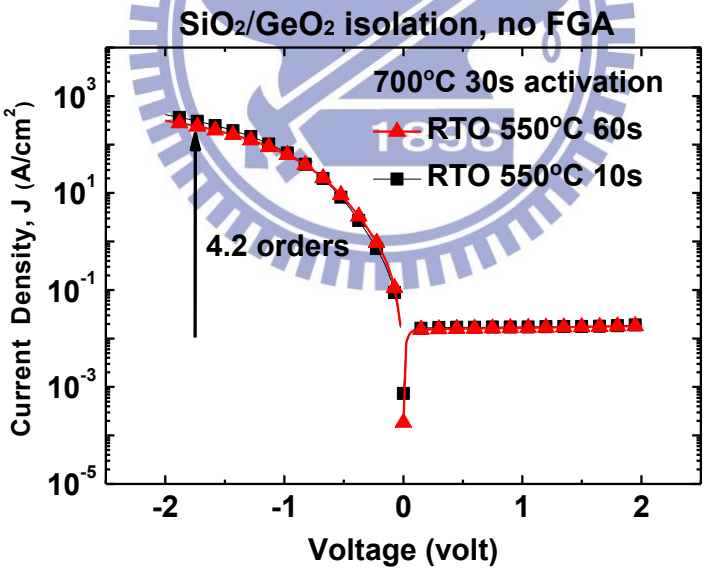
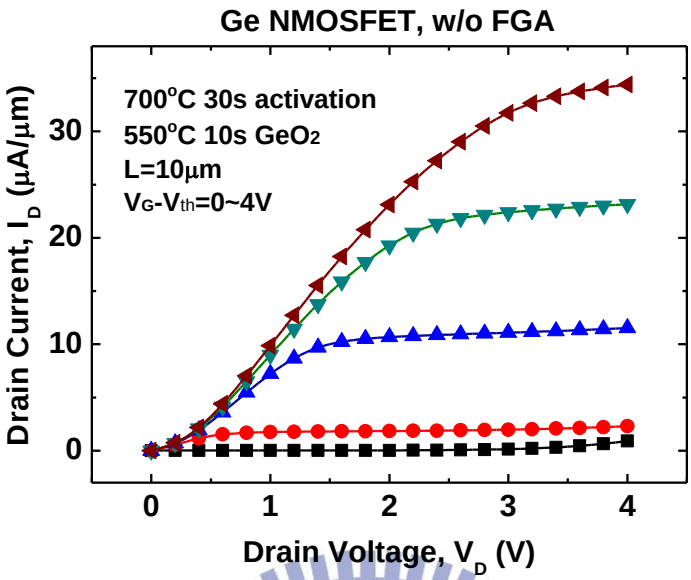
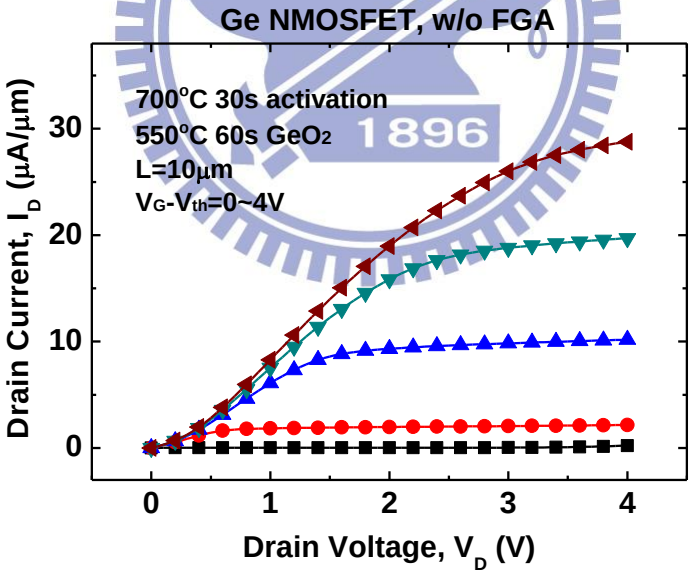


(b)

Fig. 4.3 (a) Junction IV is compared for different activation temperature. (b) Junction characteristic of n-MOSFETs with different GeO_2 thickness (different thermal budget) is compared.

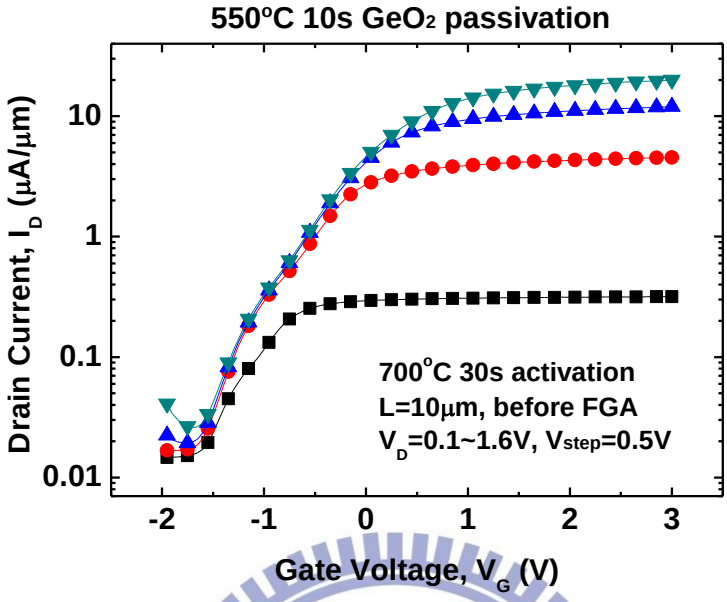


(a)



(b)

Fig. 4.4 I_D-V_D characteristics of Ge n-MOSFETs are plotted. (a) 550℃ 10s GeO_2 passivation (b) 550℃ 60s GeO_2 passivation (W/L=100μm/10μm)



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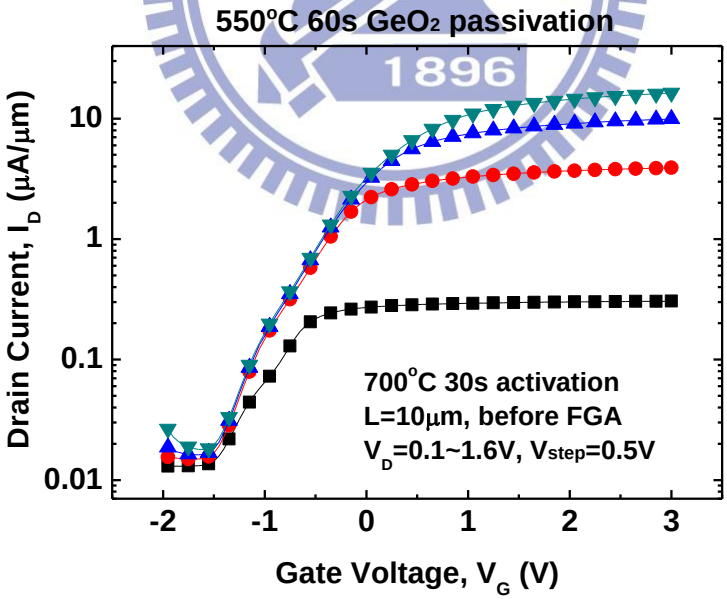
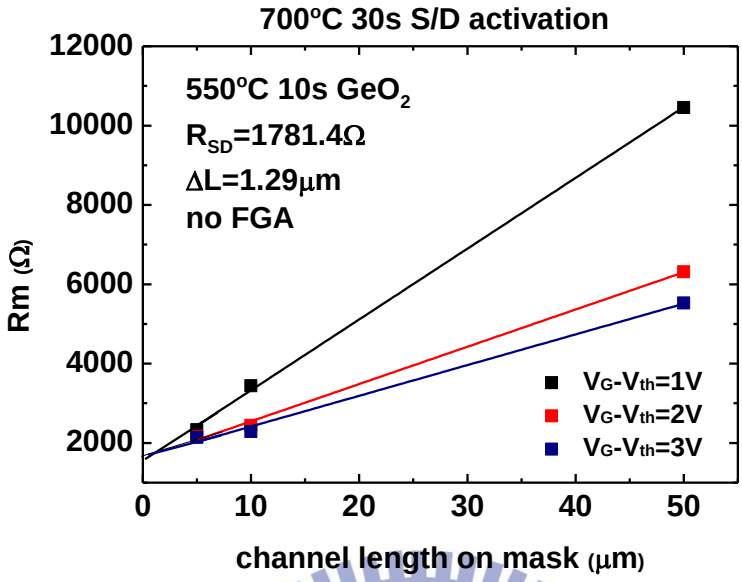


(b)

Fig. 4.5 I_D-V_G characteristics of Ge n-MOSFETs are plotted. (a) 550℃ 10s GeO_2 passivation (b) 550℃ 60s GeO_2 passivation (W/L=100μm/10μm)



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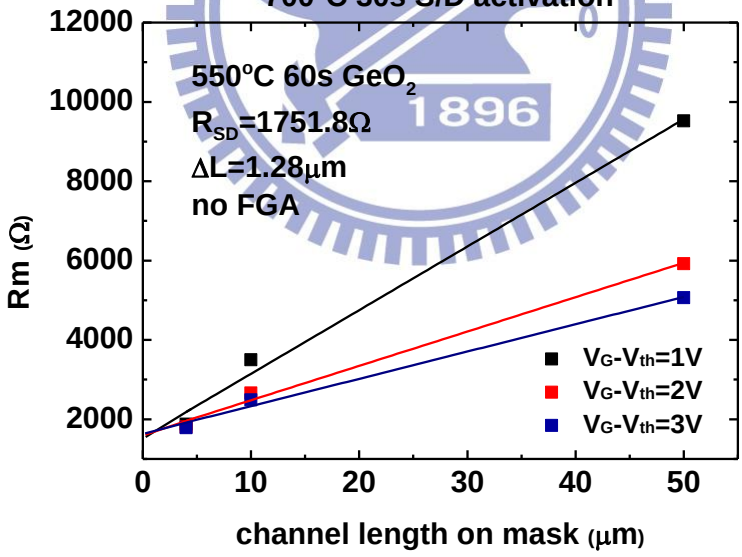
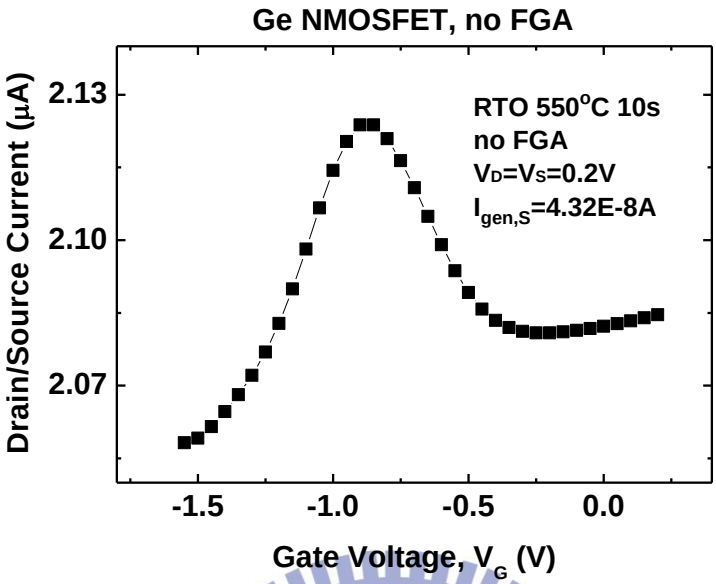


(b)

Fig. 4.6 Series resistances of Ge n-MOSFETs are extracted by Terada and Muta method. (a) 550℃ 10s GeO_2 passivation (b) 550℃ 60s GeO_2 passivation



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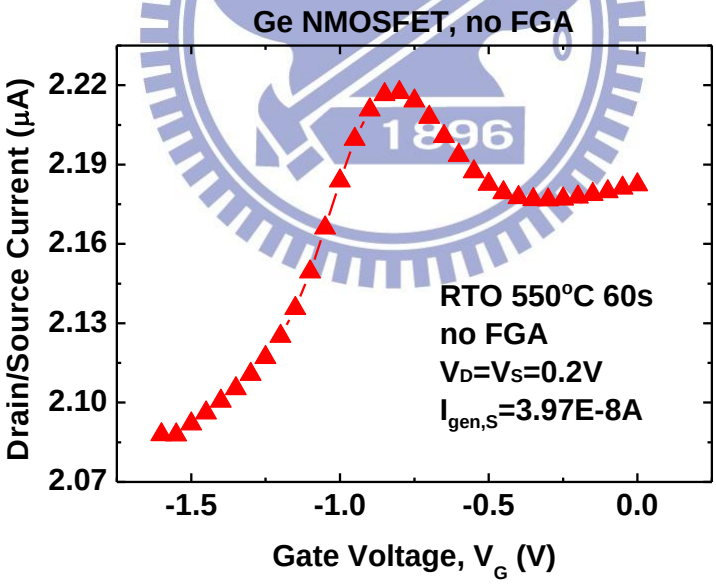
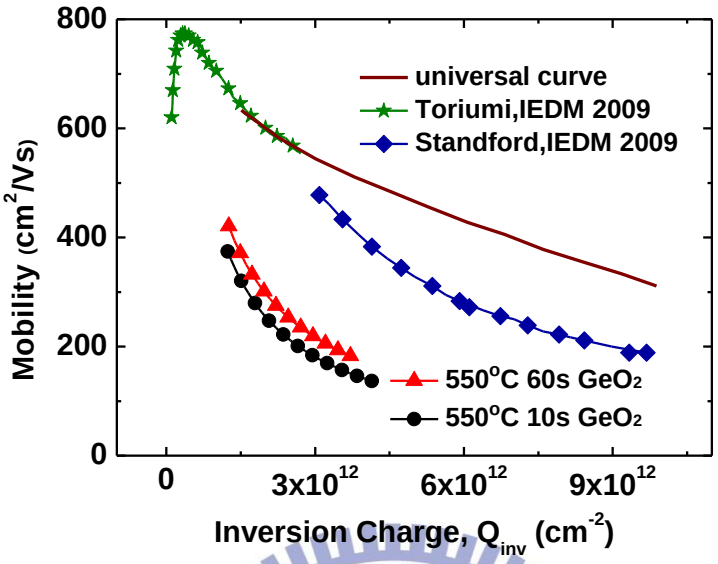


(b)

Fig. 4.7 Gated-diode measurement detects the interface state density of Ge n-MOSFETs roughly. (a) 550℃ 10s GeO_2 passivation (b) 550℃ 60s GeO_2 passivation



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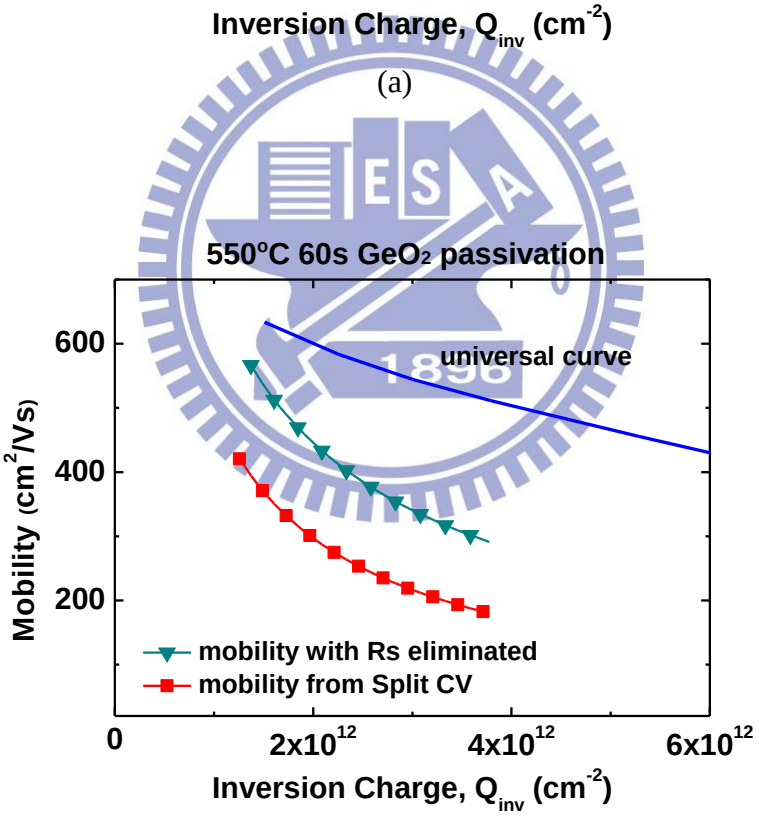
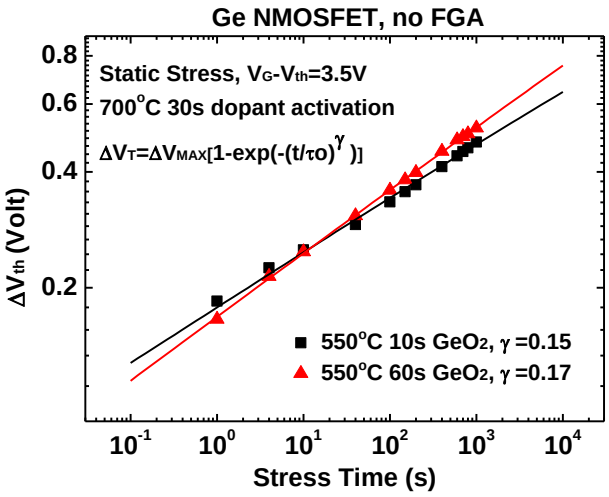


(b)

Fig. 4.8 (a) Effective mobility of our samples as a function of Q_{inv} and other published data are shown. (b) Effective inversion mobility with R_{SD} eliminated is demonstrated.



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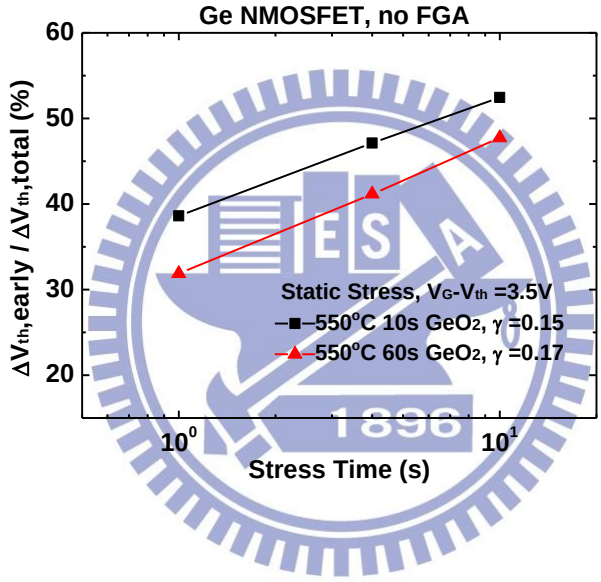

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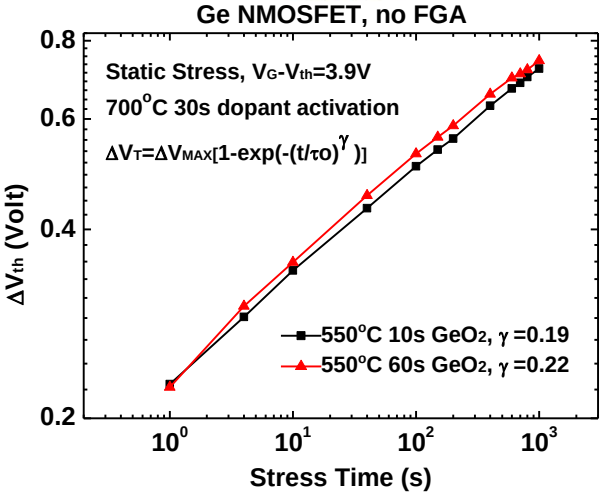

(c)

Fig. 4.9 Charge trapping behavior is compared between thicker and thinner GeO_2 passivation sample under static stress. (a) V_G-V_{th} =3.5V. (b) Ratio of early traps. (c) V_G-V_{th} =3.9V.

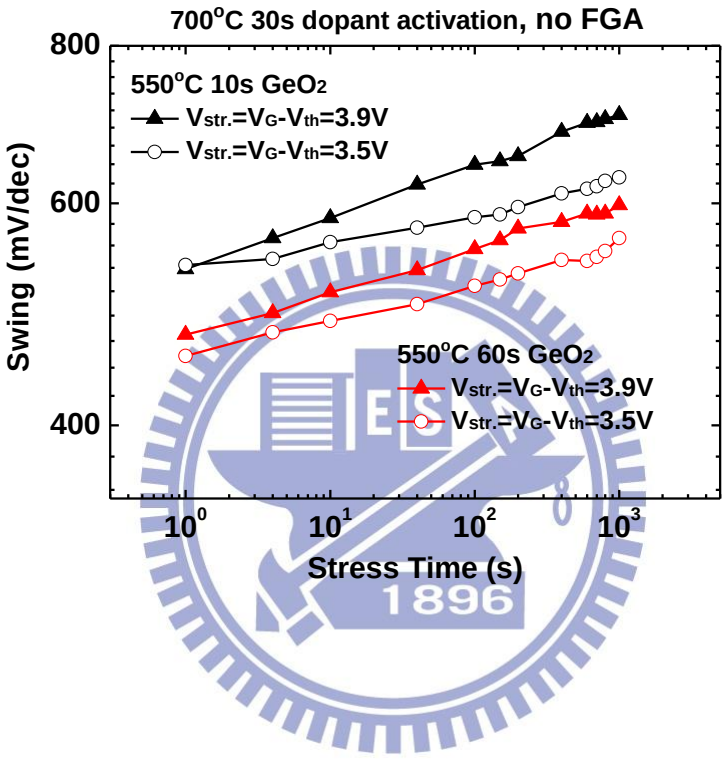

Fig. 4.10 Characteristic of subthreshold swing degradation of two stress voltages for each sample is illustrated.

Chapter 5

Conclusions and Suggestions for Future Work

5.1 Conclusions of this study

In this thesis, firstly, we had shown that D_{it} can be reduced effectively through 300℃ 30 minutes FGA from MOSCAP analysis, with value about 5×10^{11} $cm^{-2}eV^{-1}$ near the midgap from either conductance or Fermi-level efficiency method. By extrapolation of $\ln\tau$ vs $(E_T - E_i)$ plot, σ_n and σ_p were 2.7-4.2$\times10^{-16}cm^2$ and 7.8-9.6$\times10^{-16}$ cm^2 respectively.

Secondly, from the experiences in high-k/GeO_2/Ge capacitors, we successively demonstrated the device characteristics of the inversion-mode Ge p-FETs with ALD-Al_2O_3 gate dielectrics. GeO_2 passivation as well as no passivation sample had their high field mobility 1.7X and 1.3X higher than the Si universal curve respectively. Also, better on/off ratio (3.8 orders) and subthreshold swing (170mv/dec) were attained for Ge p-FET after 300℃ 30 minutes FGA, resulted from lower reverse bias junction leakage and better interface quality. Then, charge pumping was applied to reconfirm the results obtained from Chapter two. $\overline{D_{it}}$ after FGA between $E_{em,e}$ and $E_{em,h}$ is $4.2\times10^{11}cm^{-2}eV^{-1}$ and $\sqrt{\sigma_p\sigma_n}$ was 5.4×10^{-16} cm^2 for 500℃ GeO_2 passivation sample. Furthermore, pros and cons of adding the GeO_2 layer were summarized: lower D_{it} value verified from either charge pumping or gated diode measurement made the mobility higher for GeO_2 passivation sample, while it suffered from more carrier-trapping due to border traps at the GeO_2/Al_2O_3 interface and more severe subthreshold swing degradation.

Finally, device characteristics of inversion-mode Ge n-FETs with ALD-Al_2O_3 gate dielectrics were also demonstrated. SiO_2/GeO_2 isolation as well as 700℃ 30s dopant activation did we obtain the lowest reverse bias junction leakage of 1.9×10^{-2} A/cm^2 at 2V and magnitudes of the rectifying ratios reached 4.2 orders. On/off ratio of our n-FETs (W/L =

100μm/10μm) reached 3 orders but series resistance larger than 1.7kΩ was extracted. The slightly higher effective mobility for thicker GeO_2 passivation sample was due to better interface quality, which was reconfirmed by lower $I_{gen,s}$ from gated-diode measurement and better subthreshold swing. However, both of them were still much lower than the Si universal mobility for electrons. It was concluded that much severe n-FET performance degradation compared with p-FET could be explained in terms of fast trapping at Ge/GeO_2 interface, slow trapping by GeO_2/Al_2O_3 border traps and parasitic S/D series resistance.

5.2 Suggestions for Future Work

Relatively inferior performance of Ge n-FET compared with p-FET was obtained. We believed activation of n-type dopants have been considered one of the major challenges to achieve high performance Ge CMOS. In our experiments, 700℃ 30s dopant activation definitely caused too much dopant diffusion, which led to large series resistance and punch-through in n-FET with gate length 4μm. Therefore, gas phase doping or metal S/D Ge N-FETs are worthy to study in future work. In order to carry out high performance metal S/D n-FET, reducing the electron barrier height of metal/n-Ge Schottky contact while increasing the hole barrier height is an important issue with high priority, which can be achieved by adding an insulator to minimize wave function penetration or dipole engineering.

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