國 立 交 通 大 學

電 子 工 程 學 系 電 子 研 究 所

碩 士 論 文

具摻雜析離層蕭特基 SONOS
之元件製作與特性分析

Fabrication and Characterization of Dopant Segregated Schottky Barrier SONOS Devices

學號姓名：9711536 張民尚 (Ming-Shung Chang)

指導教授：邱碧秀 博士 (Dr. Bi-Shiou Chiou)

吳文發 博士 (Dr. Wen-Fa Wu)

中 華 民 國 九 十 九 年 十 月

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研究生:張民尚 Student: Ming-Shang Chang

指導教授:邱碧秀 Advisor: Bi-Shiou Chiou

吳文發 Wen-Fa Wu

國立交通大學

電子工程學系 電子研究所

碩士論文

A thesis

Submitted to Department of Electronics Engineering & Institute of Electronics College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirement

for the Degree of Master

in

Electronics Engineering

October 2010

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 九 年 十 月

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研究生：張民尚　　　　　　　　　　　　　　指導教授：邱碧秀

吳文發

國立交通大學電子工程學系　電子研究所碩士班

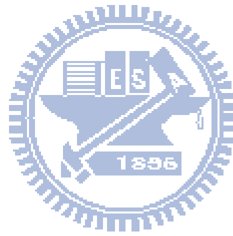
中文摘要

近年來，蕭特基電晶體被大量研究，主要是因為可以有效地微縮元件、低溫製造且擁有較低的寄生電阻。正因為如此，在未來的 CMOS 製程中蕭特基電晶體有機會取代 p-n 接面電晶體。然而因為蕭特基電晶體有幾乎定值的蕭基特能障落在源極端，造成驅動電流太小和 Ambipolar 效應。因此發展出用矽化物離子植入技術來製造出具摻雜析離層蕭特基電晶體,此電晶體是在源極和汲極接面做出摻雜的離子延伸，來抑制 Ambipolar 效應。

SONOS 型記憶體逐漸成為非揮發性記憶體中的主流，主要原因是製程簡單、耗電量低而且可以做 2 bit 儲存等等優點。因此本文把具摻雜析離層蕭特基電晶體用在 SONOS 型記憶體上,並且探討具摻雜析離層蕭特基 SONOS 型記憶體,蕭特基 SONOS 型記憶體和量產型 SONOS 記憶體的特性比較,例如:寫入抹除速度、保持力(Retention)和耐久力(Endurance)。

從本研究中可發現，蕭特基 SONOS 型記憶體擁有比較大的記憶窗(Memory window)約為 6V，量產型 SONOS 記憶體相較之下只有 3.2V；而且也擁有快速的寫入的速度，在外加電壓 10^{-4} 秒下約有 3V 的記憶窗，量產型 SONOS 記憶體相較之下只有 1V 的記憶窗；但是由於開關電流的比值(On-off ratio)太小，大約 30.3，以至於很

難分辨〝0〞和〝1〞。也因此使用具摻雜析離層蕭特基 SONOS 型記憶體來取代蕭特基 SONOS 型記憶體。本研究中可以發現具摻雜析離層蕭特基 SONOS 型記憶體在外加電壓 10^{-4} 秒下約有 2V 的記憶窗；驅動電流為 6.7×10^{-5}A; 導通電壓為 4.38V，相較之下傳統型記憶體在外加電壓 10^{-4} 秒下只有 1V 的記憶窗；驅動電流為 6.8×10^{-7}A; 導通電壓為 6.89V。而且相對於其他 SONOS 型記憶體，具摻雜析離層蕭特基 SONOS 型記憶體有較佳的持久力和耐久力。經本實驗可發現具摻雜析離層蕭特基 SONOS 型記憶體經過 10 年之後仍能維持 3V 的記憶窗，且對於經過寫入抹除 10^4 次的元件，10 年之後也能維持 1.3V 的記憶窗。量產型 SONOS 記憶體相較之下，經過 10 年之後只有 0.7V 的記憶窗。



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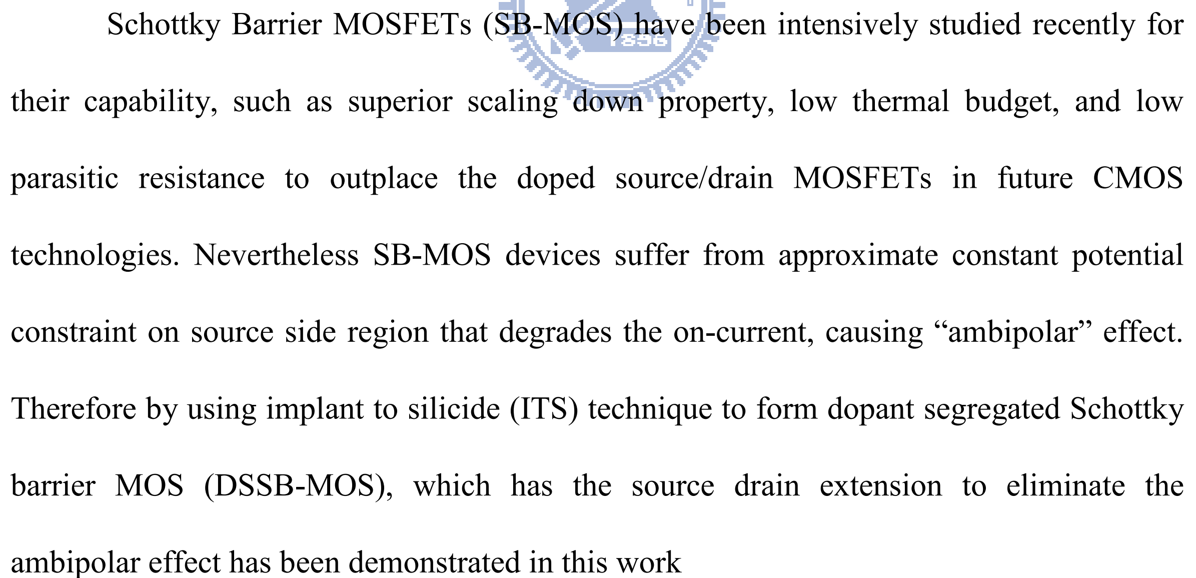
Student: Ming-Shang Chang

Advisor: Bi-Shiou Chiou
Wen-Fa Wu

Department of Electronics Engineering Institute of Electronics
National Chiao Tung University

ABSTRACT

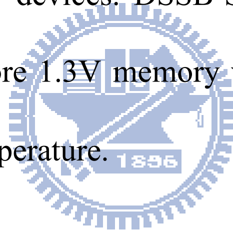


Schottky Barrier MOSFETs (SB-MOS) have been intensively studied recently for their capability, such as superior scaling down property, low thermal budget, and low parasitic resistance to outplace the doped source/drain MOSFETs in future CMOS technologies. Nevertheless SB-MOS devices suffer from approximate constant potential constraint on source side region that degrades the on-current, causing “ambipolar” effect. Therefore by using implant to silicide (ITS) technique to form dopant segregated Schottky barrier MOS (DSSB-MOS), which has the source drain extension to eliminate the ambipolar effect has been demonstrated in this work

SONOS type memory plays an essential role in the nonvolatile memory market, due to less complexity of process, low power consumption and two bits storage ability. In this work, DSSB-MOS technique is used in SONOS memory devices. P/E speed, retention, and endurance characteristics of SB-SONOS, DSSB-SONOS and conventional SONOS

memory devices are investigated and compared in this work.

SB-SONOS device has largest memory window about 6V and provides fastest program speed for V_{TH} shift about 3V with programming time of 10^{-4} seconds compared to conventional SONOS device which has memory window about 3V and program speed for V_{TH} shift about 1V with programming time of 10^{-4} seconds. But SB-SONOS shows small on/off ratio around 30.3, causing difficult to differentiate between “0” and “1”. Therefore DSSB-SONOS device has been attempted to replace SB-SONOS device. For DSSB-SONOS device, it shows the better program speed for V_{TH} shift about 2V with programming time of 10^{-4} seconds compared to conventional SONOS device. And for reliability, DSSB-SONOS device exhibits excellent retention and endurance performance compared to other SONOS memory devices. DSSB-SONOS devices retain 3V memory window after 10years and furthermore 1.3V memory window is obtained after subject to 10^4 times of P/E cycles at room temperature.



致謝

在碩士的這二年的生活裡即將成為過去，隨著論文的完成也漸漸感受到這兩年內學到和所經歷的是多麼的重要。在這兩年的學習，我受到了許多人的幫助與指導才得以順利完成論文，在此謹以此文感謝。

首先要感謝這兩年指導我的兩位指導老師，分別是邱碧秀老師和吳文發老師。兩位老師在研究與論文中都給予最大的支持與指導，因此才能在兩年中完成這份論文與研究，此外每每與老師們討論過後，皆會有意想不到的收穫。不僅僅在專業知識上，老師們的學術態度與為人處事也提供了相當好的典範。

其次要感謝已經畢業的鄧志剛學長和吳抒樺學姐，在我們剛進來碩班的時候，不厭其煩的帶領我們學習國家奈米元件實驗室的機台與操作環境，而且在研究上發現問題，也會耐心的教導我們，使我研究能輕易的上手。

此外，還要感謝實驗室的同伴肇中，跟我一起奮鬥一起努力，有問題的時候也會義不容辭的幫忙。還有侯拓宏老師實驗室的小P學長，冠良學長 還有昌哥，當我去找您們求助時，也不會因為我是別的實驗室就對我有所保留，真的很謝謝你們。

接著，要感謝在清大的阿幹還有連振炘老師實驗室的章緯學長、林靖璋學長、羅彥翔學長、阿古學姐在實驗上和論文上都給我很多的幫助。另外要感謝楊紹輝、蔡侃學、榜哥、謝智翔可以一起歡笑，有事沒事可以一起聚餐，把我當成一家人。

此外，還要謝謝阿耀，平常可以一起打球，抒發實驗壓力。謝謝大豆和書除在口試的時候可以幫我借到投影機和筆電，使的口試得以順利進行。感謝小武、天線、貴庚、老劉平常有空就會找我打球、打麻將等等的休閒活動。還有謝謝博哥、蔡董、掃把在實驗中給我的建議。

最後，我要感謝我的父母。感謝他們在我的求學中大力的栽培漢默默的付出，使我在生活上無後顧之憂，進而順利的完成此論文，完成學業。總而言之，感謝各位在我兩年的碩士生活的指導與照顧，在此感謝。

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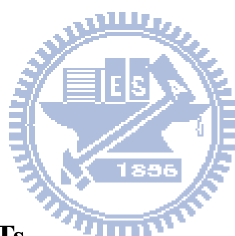

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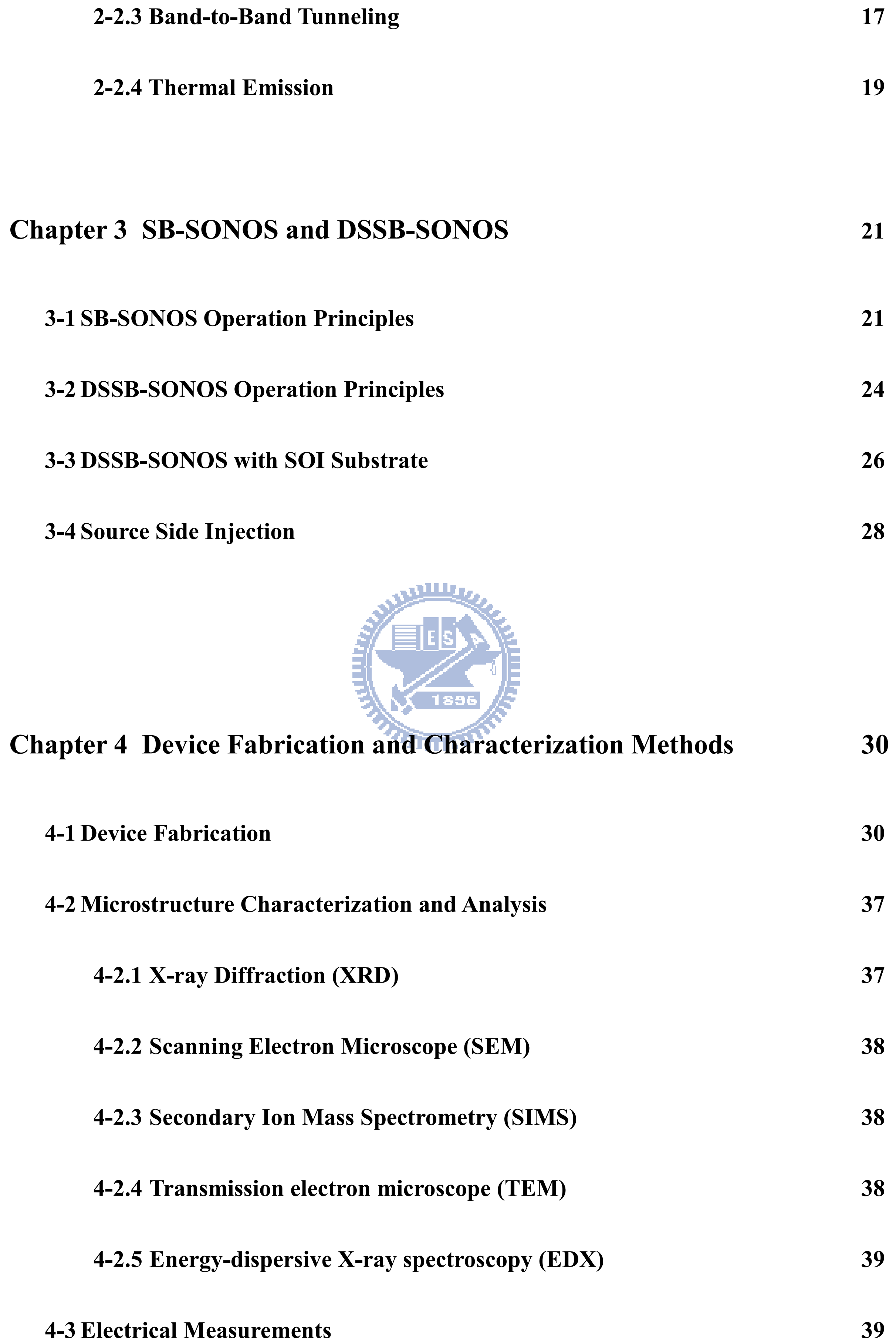

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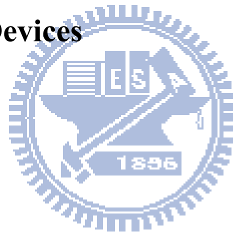

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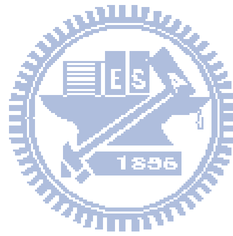


CHAPTER 1

Introduction

1-1. CMOS Technology

Frank Wanlass invented CMOS in 1967 [1]. CMOS technology is used in microprocessors, controllers and other circuit. In order to approach the benefits, such as high density devices, low power consumption, and low manufacturing costs, CMOS downsizing becomes the principle trend for latest few years.

According to the Moore's law, the roadmap pointed out that the technology will step to 32 nm nodes until 2013. But in the ITRS 2009 update published, 25 nm nodes is expected to start production until 2012, as shown in the Table 1-1 and Fig. 1-1 [2]. It shows that the device scaling down is an instant problem for future years. And from the reference, it shows that parasitic series resistance Rs has become an important performance-limiting factor in CMOS devices with sub-30 nm gate length [3–7]. Moreover, with CMOS down-sizing, serious short-channel- effects (SCE) attributed to the insufficient gate control ability and the performance non-uniformity for short channel devices [8]. Therefore, to alleviate these drawbacks, Schottky-Barrier MOSFETs (SB-MOS) have been investigated for the nano-scale devices.

YEAR OF PRODUCTION	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*
Flash Uncontacted Poly Si ½ Pitch (nm)	38	32	28	25	23	20	18	15.9
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	52	45	40	36	32	28	25	22.5
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	54	45	38	32	27	24	21	18.9
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22	19.8
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17	15.3

Long-term Years

YEAR OF PRODUCTION	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*
Flash Uncontacted Poly Si ½ Pitch (nm)	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5
MPU Printed Gate Length (nm)	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9
MPU Physical Gate Length (nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4

Table 1-1 List of device requirements for the current and forthcoming transistors according to the ITRS [2].

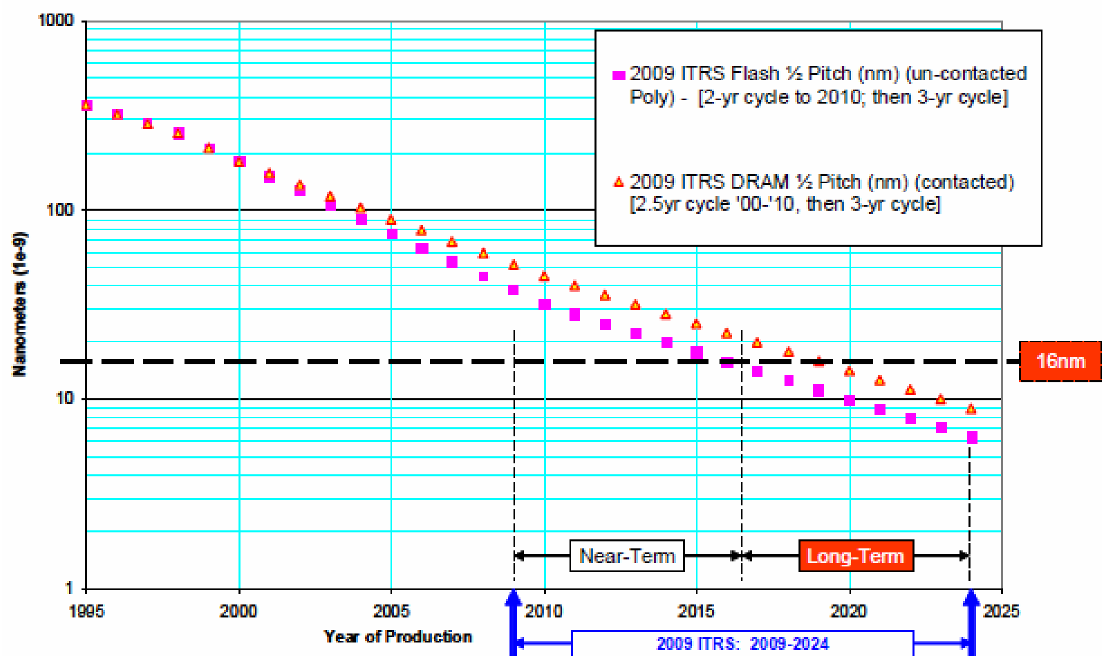


Fig. 1-1 DRAM and Flash memory half pitch trends [2].

1-2. Schottky Barrier MOSFETs

Schottky barrier source/drain structure was published in 1994 by J.R Tucker [9].

Schottky-barrier MOSFETs (SB-MOS) which utilize metal silicides for source/drain instead of conventional MOSFETs with heavily doped layer, the schematic structures of SB-MOS and conventional MOSFETs are shown in Fig. 1-2 and Fig. 1-3. Using metal silicides for source/drain is not only decreased the parasitic series resistance Rs but also lower the thermal budget. Owing to Schottky barrier height between metal silicides and Si interface remains approximately constant, short-channel-effect (SCE) can be eliminated. Using silicides for source/drain indeed overcome the problem with devices down-scaling.

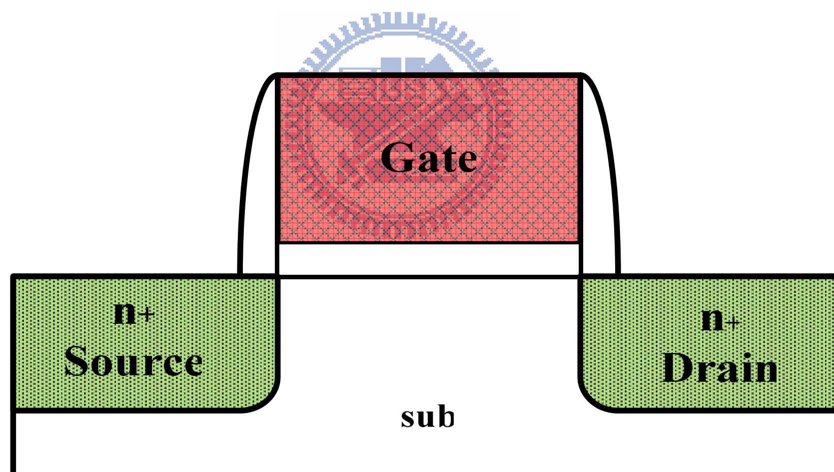


Fig. 1-2 The schematic structure of conventional MOSFETs.

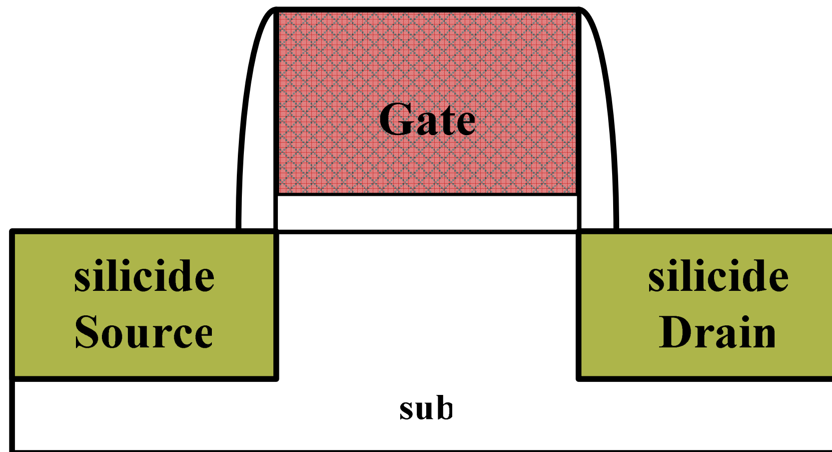
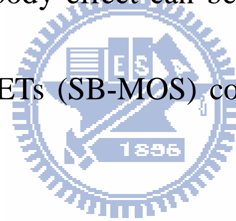


Fig. 1-3 The schematic structure of SB-MOS [13].

Schottky-barrier MOSFETs (SB-MOS) are also attractive used in silicon-on-insulator (SOI). Since, floating body effect can be suppressed on the partially depleted SOI for Schottky barrier MOSFETs (SB-MOS) compared to conventional p-n junction SOI MOSFETs [10,11].



Schottky barrier MOSFETs (SB-MOS) however have some following draw-backs. First, the drive current is smaller than the conventional MOSFETs and the leakage current is larger than conventional MOSFETs. Second, SB-MOS devices depict very poor on/off current ratio [11-13]. Third, The SB-MOS exhibits the ambipolar condition. In order to eliminate the ambipolar effect while keeping the advantages for SB-MOS devices, SB-MOS with ultra-short source/drain extention by using implant-to-silicide (ITS) process was proposed. After implantation and activation annealing, dopant will segregate at metal silicide and silicon interface. This kind of mechanism is called “dopant

segregation". Fig. 1-4 shows the schematic structure of SB-MOS with dopant segregation (DSSB-MOS). DSSB-MOS devices show the leakage current significantly lower than SB-MOS. Besides, the drive current is also significantly larger than SB-MOS. This concept has been approved in n-channel and p-channel SB-MOS [13].

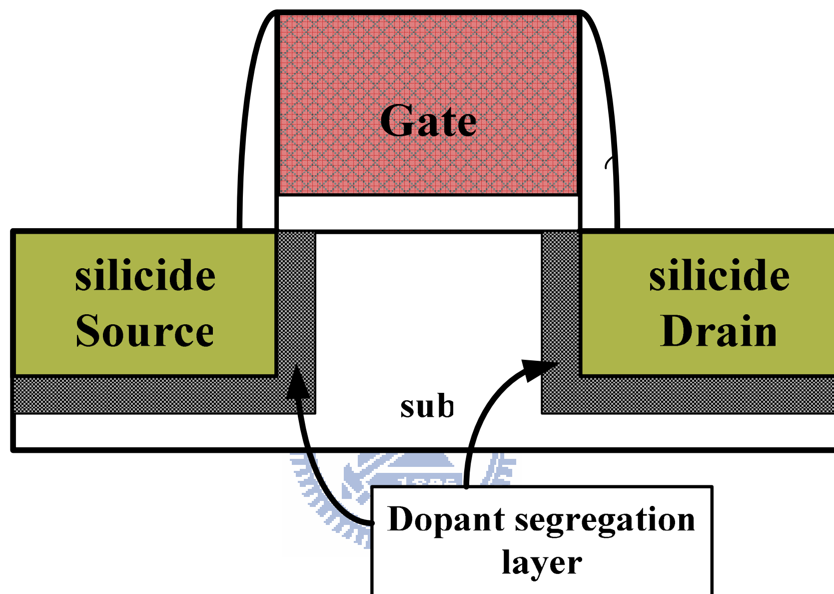


Fig. 1-4 The schematic structure of DSSB-MOS [13].

1-3. Metal Silicide Selection

In order to use metal silicide into device fabrication, the silicide properties must be considered carefully. The properties include low resistivity, good thermal stability, no metal compound formation, and low electrons and holes Schottky barrier height. However, there is no metal silicide that can meet these requirements. Such as Table 1-2

shows, Ir_3Si_5 is stable under 500~1000 temperature range, but it shows high resistivity [14,15].

Among the silicide, titanium disilicide ($TiSi_2$) is the first successful metal silicide that has been used in CMOS process due to the low resistivity and good thermal stability [16]. But when used in DSSB-MOS, the critical drawback appears which is Ti may react with the dopants B and As [17]. The compound phase are Ti and the dopant B, As nucleates the tiny crystals at these locations where silicide grain boundaries are butted to the silicide silicon interface. This compound formation effect renders $TiSi_2$ very ineffective as a diffusion source for As and especially B and leads to unacceptably high contact resistances. For another silide material such as $YbSi_{2-x}$, $ErSi_{2-x}$, it proposed low Schottky barrier height for electron, however there are still serious problems such as oxidation and “pinhole formation” during Yb silicidation [18]. The presence of pinholes may result in short circuits or direct contact of upper layers to Si substrate, and thus decrease the device reliability [19].

Silicide	φ_{bn}	φ_{bp}	ρ	T_f	DDS	Remark	Ref
IrSi	0.93	----	500	400-550	Si	Diffusion control growth	[14]
Ir_3Si_5	0.85	----	4000	500-1000	Si	Diffusion control growth	[14]
Pt_2Si	0.85	----	14-16	200-300	Si/Pt	Diffusion control growth	[14]
PtSi	0.88	0.21	28-35	300-500	Si/Pt	Diffusion control growth	[14]
$IrSi_3$	-----	0.94	350-580	1000	Si	Nucleation control growth	[14]
YSi_2	0.39	----	69	400	Si	Easy oxidation	[14]
$DySi_{2-x}$	0.37	0.73	250-380	300	Si	Easy oxidation	[14]
$ErSi_{2-x}$	0.39	0.7	30	300-350	Si	Easy oxidation	[14]
$YbSi_{2-x}$	0.27	0.85	34	350	Si	Easy oxidation	[14]
NiSi	0.65	0.45	10.5-15	250-400	Ni	Diffusion control growth	[14]
$TiSi_2$	0.61	0.49	10-15	750-900	Si		[15]
$CoSi_2$	0.65	0.45	18	550-900	Co		[15]

Table 1-2 The property of SB-MOS devices with various silicide for source/drain φ_{bn}: Schottky barrier height for electron, φ_{bp}: Schottky barrier height for hole, ρ: specific resistivity, T_f: typical formation temperature, DDS: dominant diffusion species during the silicide growth.

Recently, nickel silicide has been recognized as a promising material for SB-MOS. For Ni film on silicon, there are three types of silicide phases, Ni_2Si, NiSi, $NiSi_2$. For NiSi, it has the lowest resistivity and $NiSi_2$ has the highest resistivity. NiSi is metastable state, therefore it could be easily turn to $NiSi_2$ phase [20,21]. Moreover NiSi Schottky barrier height for electrons and holes are 0.65eV and 0.45eV, respectively, almost in the mid-gap to silicon. Therefore, by implantation into dopant for p-type (B) and n-type (As) followed with drive-in annealing at low temperature can get the similar performance for

P-MOSFETs and N-MOSFETs. Therefore, NiSi presents a promising material for SB-MOS technology.

1-4. Motivation

Because DSSB-MOS has been one of the most candidate devices for future years, this works try to apply the structure on non-volatile memory. Commercial non-volatile memories use poly-silicon floating gate as charge-storage material. This structure was published by Kahng and Sze at 1967 [22]. However floating gate technology has two major drawbacks. First, the floating-gate memory devices face several scaling down challenges beyond the 45-nm technology. This is due to coupling issue [23-26]. Secondly, floating-gate memory requires high voltage applied during program and erase, it will put high power consumption. In order to overcome these kinds of drawbacks, "SONOS", short for "silicon-oxide-nitride-oxide-silicon", become one of the most attractive candidates for flash memory. The structures for floating gate and SONOS devices are depicted at Fig. 1-5 and Fig. 1-6. Contrary to the floating gate devices where charge is stored in the floating gate, SONOS cell transistors use nitride on top of the tunnel oxide as a charge trapping layer. Since charges are independently trapped in nitride, it will naturally immune to the capacitance coupling interference due to the adjacent memory

cells [23]. Therefore SONOS flash memory is ideal for scaling down. Moreover, it provides high program/erase speed compared to the floating gate [23-26].

High performance Schottky barrier SONOS with dopant segregation (DSSB-SONOS) memory device is confirmed. It shows high program speed, excellent short channel behavior, and little damage for stressing compared to conventional SONOS device.

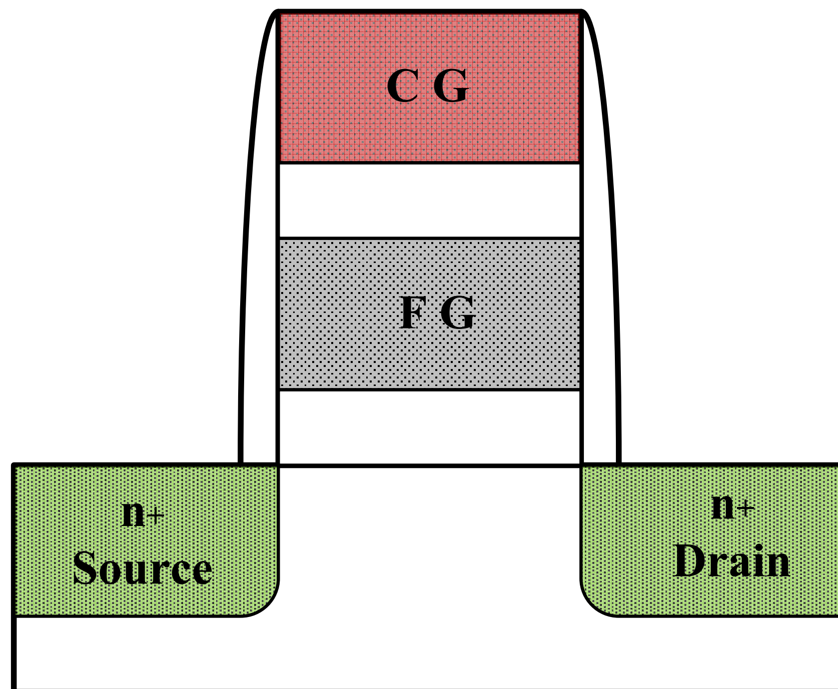


Fig. 1-5 The schematic structure of floating gate [26].

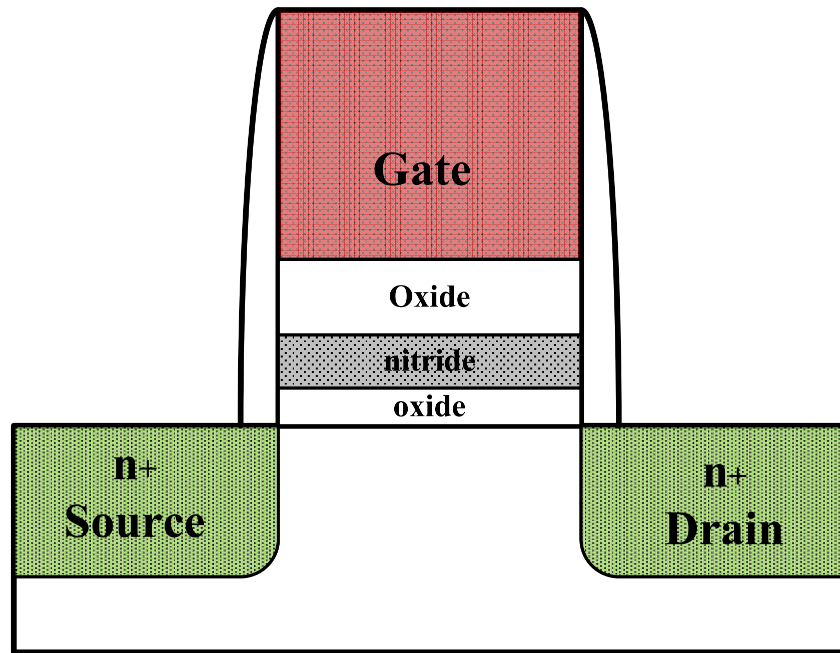
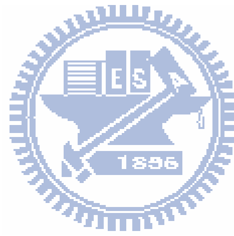


Fig. 1-6 The schematic structure of SONOS device [26].



CHAPTER 2

Operation Principles of SONOS Memory Devices

2-1. Reading Operation

In this chapter, program and erase mechanism of nonvolatile memory will be introduced. For floating gate and SONOS devices, the data stored can be determined by threshold voltage. The formula for charge storage based on a shift in the threshold voltage on nonvolatile memory device can be written as [18]

$$\Delta V_{TH} = -\frac{Q_S}{C} \tag{2-1}$$

Where Q_S is charge in silicon semiconductor, and C is the capacitance of the gate insulator. As shown in Fig. 2-1, when electron is charged by nitride (or floating gate) the V_{TH} will increase, called program state. On the other hand, when electron leak out from nitride (floating gate) or hole is charged by nitride, the V_{TH} will decrease, called erase state.

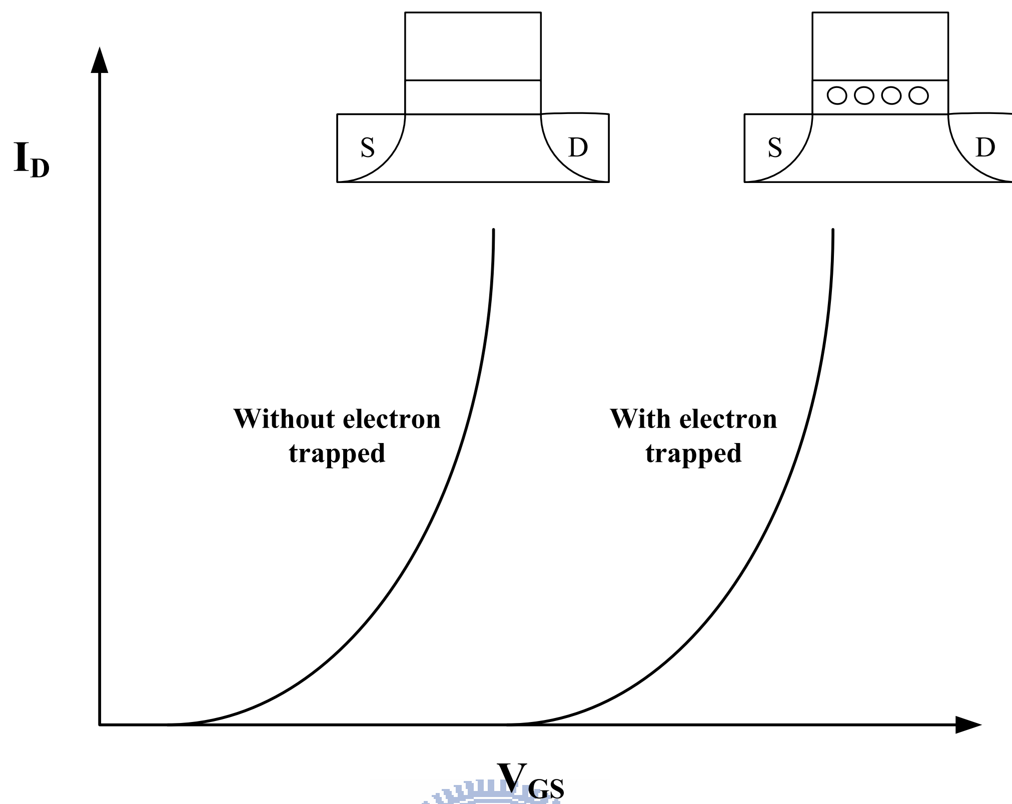


Fig. 2-1 The concept of nonvolatile charge storage based on a shift in the threshold voltage [18].

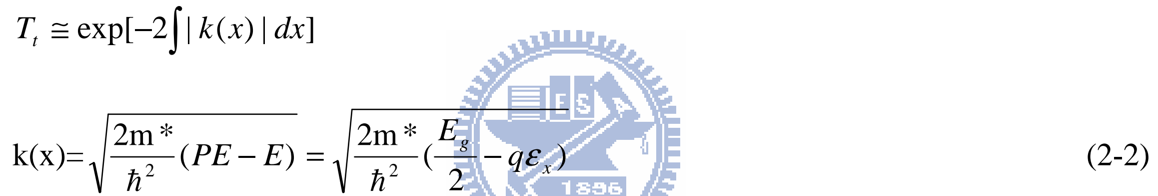
2-2. Carrier Injection Mechanism

2-2.1. F-N Tunneling

For SONOS memory, when programming, electron is tunneling through the tunneling oxide and then will be trapped at nitride. Eectron is hard to leak out from nitride due to the barrier height for top and bottom oxide, as shown in Fig. 2-2. As Fig.

2-3 shows, when the electric field built up across tunneling oxide for $E_{OX} = \frac{V_{OX}}{T_{OX}}$ higher than $\frac{\phi}{T_{OX}}$ where ϕ is for gate oxide to silicon barrier height, hence this kinds of mechanism is called F-N tunneling [27,28]. And when $E_{OX} = \frac{V_{OX}}{T_{OX}}$ is smaller than $\frac{\phi}{T_{OX}}$, called it direct tunneling. Direct tunneling is independent to temperature, it dominate only as the gate oxide sufficiently thick [29]. Otherwise, F-N tunneling happens only at high vertical electric field. It can be proved by using tunneling probability T_t which is given by the WKB approximation (Wentzel-Kramers-Brillouin method). Tunneling probability T_t is given by [30]

$$T_t \cong \exp[-2\int |k(x)|\, dx]$$



$$\mathrm{k(x)}=\sqrt{\frac{2\mathrm{m}^*}{\hbar^2}(PE-E)} = \sqrt{\frac{2\mathrm{m}^*}{\hbar^2}(\frac{E_g}{2}-q\varepsilon_x)} \qquad (2\text{-}2)$$

where PE is potential energy, E is the incoming electron energy, E_g is the band-gap ε_x is the electric field, m* is the effective electron mass. For F-N tunneling,

$$T_{F-N} = \exp(-\frac{4\sqrt{2m^*}(q\phi_B)^{1.5}}{3q\hbar\varepsilon_x}), \qquad (2\text{-}3)$$

From the formula, it shows F-N tunneling is only field dependence. And for direct tunneling

$$T_{dir} = \exp(-\frac{2d\sqrt{2qm^*\phi_B}}{t_{ox}}), \qquad (2\text{-}4)$$

is thickness dependence.

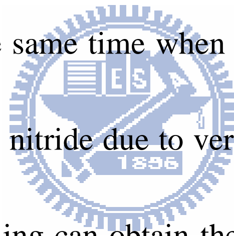
Fig. 2-2 The typical band diagram for flat band condition, when on program state electron is trapped at nitride, on erase state electron leak out from nitride.

(a) (b)

Fig. 2-3 The typical band diagram for (a) under $E_{OX} < \frac{V_{OX}}{T_{OX}}$ is direct tunneling condition (b) under $E_{OX} > \frac{V_{OX}}{T_{OX}}$ is F-N tunneling condition [27-29].

2-2.2. Channel Hot Electron Tunneling

When large electric field exists, carriers will get high energy. And for carriers with high energy, these kinds of carriers are called “hot carriers”. Hot electron tunneling is different to F-N tunneling owing to the electrons tunneling tend to be trapped spontaneously. Hot electron tunneling occurs at pinch-off region where $V_{DS} > V_{GS} - V_t$, due to large electric field at drain side region. For conventional SONOS, pinch-off region is at drain side, so at drain side carriers may cause impact-ionization. And by impact-ionization, it will create electron and hole pairs, called “hot electron and hot hole“, as Fig. 2-4(a) shown [31]. At the same time when gate apply positive bias, hot electron may tunnel through gate oxide to nitride due to vertical electric field. For flash memory, using channel hot electron tunneling can obtain the highest program speed compared to F-N tunneling. However it will also damage tunneling oxide and cause the retention characteristics degradation. When hot electron has sufficient high energy to overcome the gate oxide potential barrier (3.2eV), it is called” lucky electron”, as Fig. 2-5 shown [32].



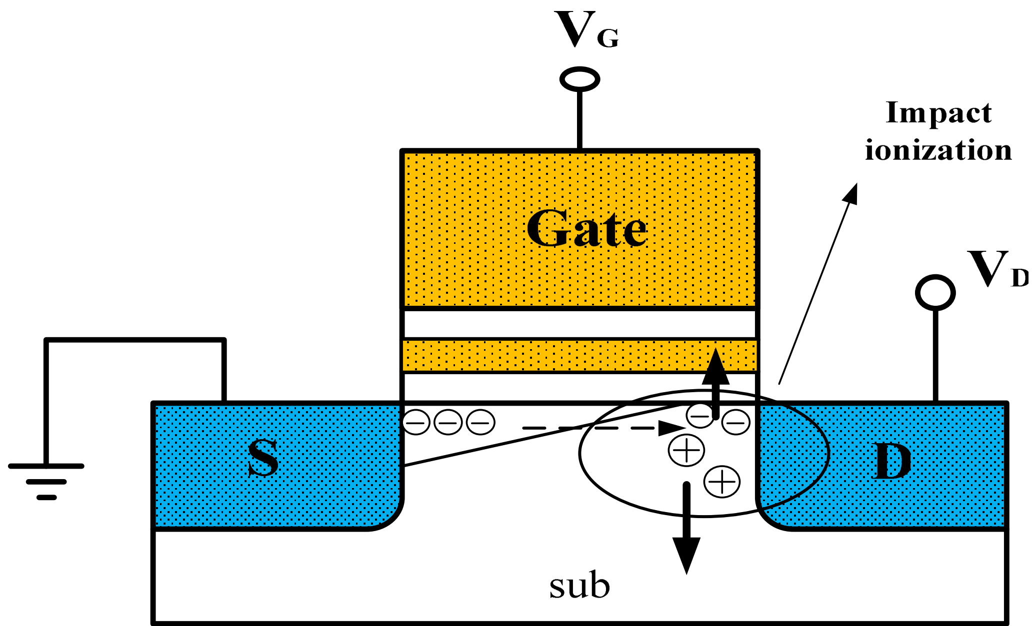


Fig. 2-4 Channel Hot Electron Injection (CHEI), at pinch-off region, strong lateral field accelerate electrons causing impact ionization, and then electron tunnel to nitride due to strong vertical electric field [31].

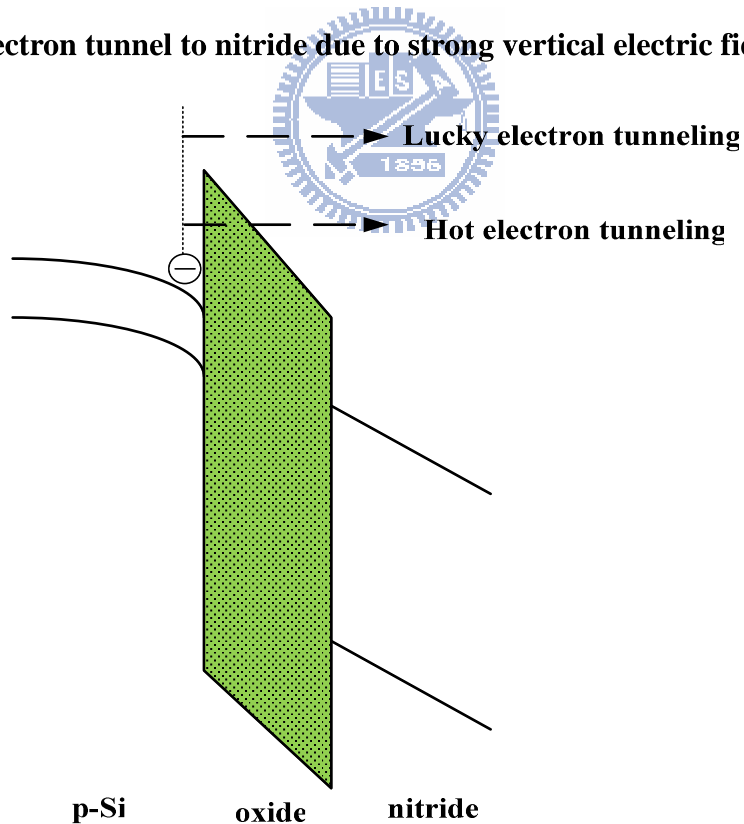
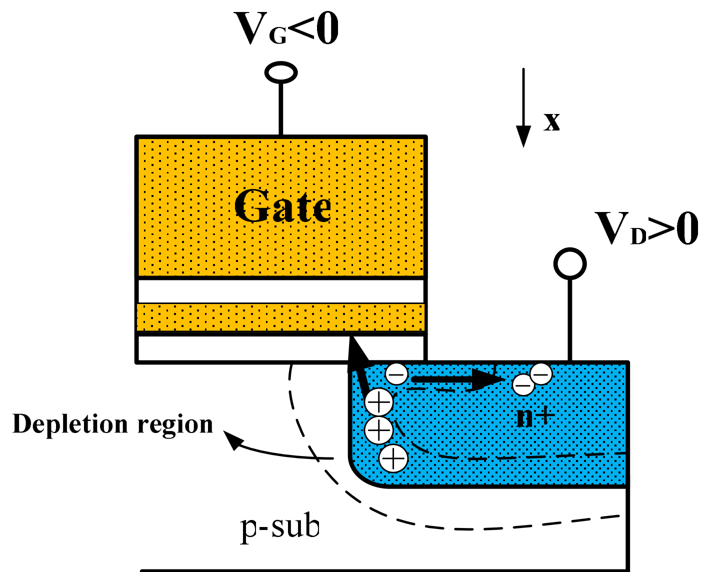


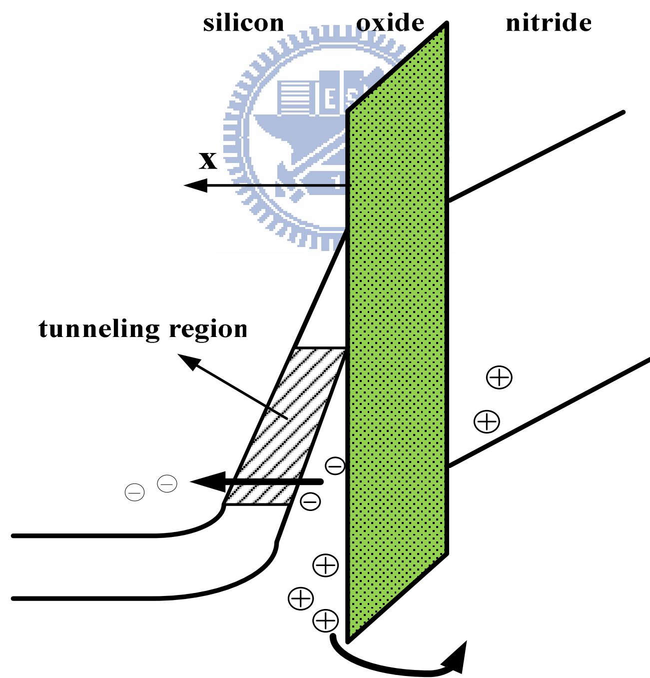
Fig. 2-5 The typical band diagram for hot electron tunneling and lucky electron tunneling [32].

2-2.3. Band-to-Band Tunneling

Band to band tunneling (BTBT) mechanism has been mainly focused on the leakage current in MOSFETs, such as body-to-drain junction leakage and gate-induce drain leakage (GIDL) [33]. From Fig. 2-6 shows the typical cross-sectional view of N-MOSFETs. When a highly negative bias is applied to the gate, causing strong vertical electric field drops at gate oxide and n^+ region. And owing to high electric field, large band bending occurred; electrons in n^+ region may tunnel from valence band to conduction band, and it is called "BTBT". At the same time, portions of holes which is left in the valance band may also tunneling through the gate oxide to nitride due to negative gate bias. C.Hu published band-to-band tunneling model at 1992. The BTBT tunneling current depends to lateral electric field and vertical electric field. In this work, we choose BTBT to erase because it has the fast erase speed compared to use F-N tunneling to erase.



(a)



(b)

Fig. 2-6 Band to band tunneling (BTBT), (a) When gate applied negative bias, and drain applied positive bias, then brings out deep depletion region causing electrons tunnel from valance band to conduction band (b) the typical BTBT band diagram shows hole back tunneling to nitride [33].

2-2.4. Thermal Emission

The thermal emission theory is derived by Beth [34]. The assumptions are (1) the barrier height $q\phi_B$ is much larger than kT, (2) under thermal equilibrium, and (3) the net current flow does not affect the equilibrium. The current density:

$$J_{s\rightarrow m} = \int qv_x dn \tag{2-5}$$

And by using the density of states concept and the distribution function, the formula can be transformed to

$$J_{s\rightarrow m} = A^*T^2 \exp(-\frac{q\phi_B}{kT})\exp(\frac{qV}{kT}) \tag{2-6}$$

where A^* is the Richardson constant, T is the absolute temperature, k is the Boltzmann constant, q is the electron charge, V is the applied bias across the Schottky contact, and ϕ_B is the effective Schottky barrier height. Fig. 2-7 shows the typical Schottky barrier band diagram. When electron is tunneling from metal to silicon, the on current only depends on Schottky barrier heights. Because the Schottky barrier height for electron is remain the same and unaffected by applied voltage so the emission current is

$$J_{m\rightarrow s} = A^*T^2 \exp(-\frac{q\phi_B}{kT}) \tag{2-7}$$

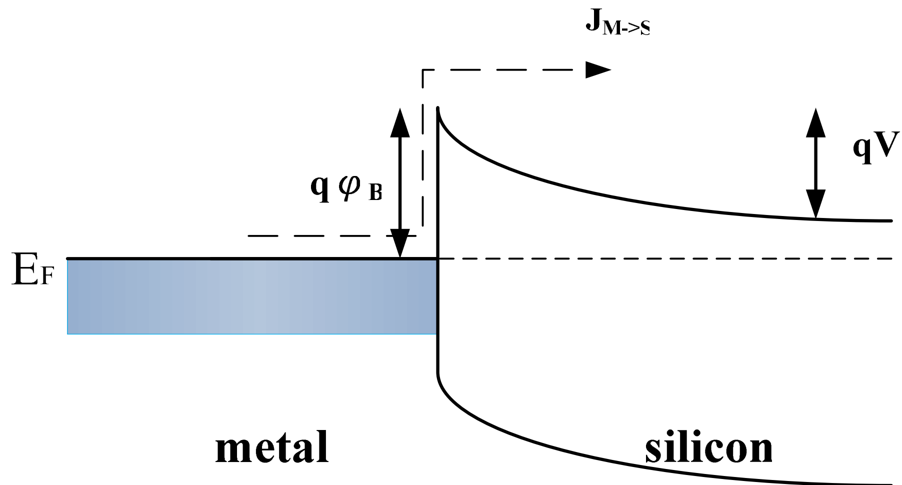
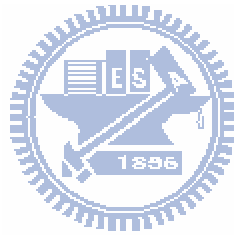


Fig. 2-7 The typical Schottky barrier band diagram, the emission current depends only on barrier heights [30].



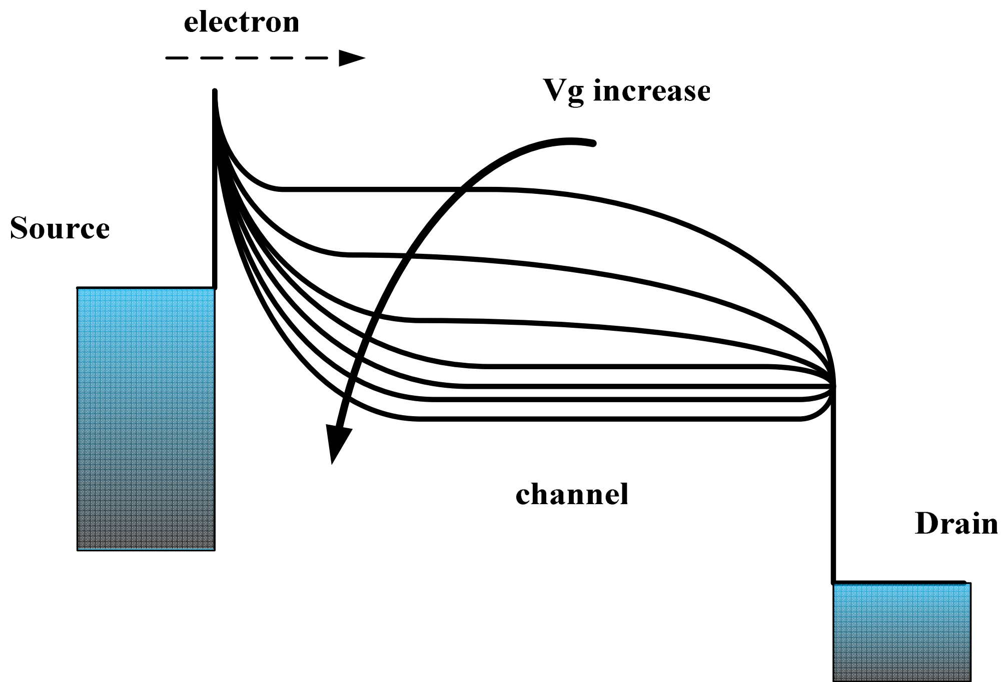
CHAPTER 3

SB-SONOS and DSSB-SONOS

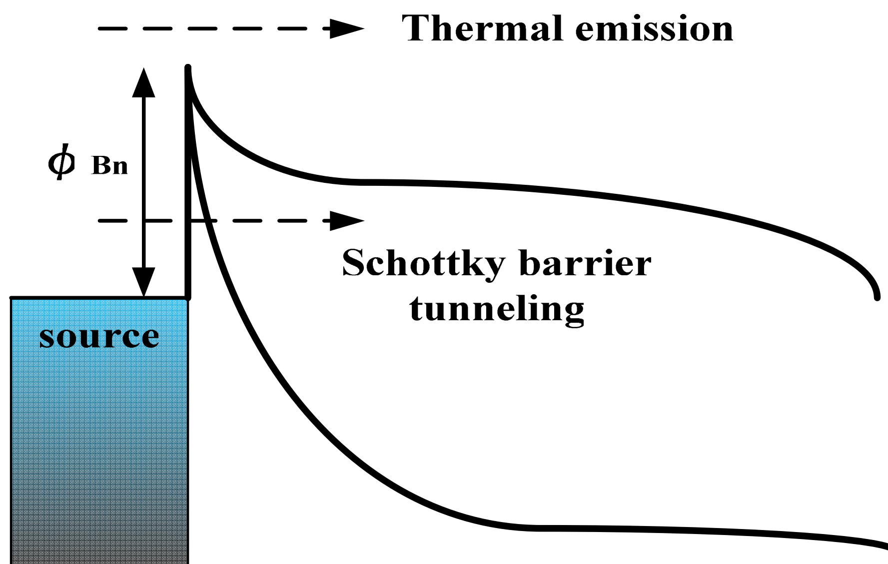
3-1. SB-SONOS Operation Principles

Since, SB-SONOS use metal silicides for source/drain, indicating that the tunneling current depends on the Schottky barrier height for electron and hole which is produced by metal silicides. Like conventional SONOS, SB-SONOS principle is based on the control of the channel conductivity by the gate electrode which is isolated from the substrate by a thin gate oxide layer.

When SB-SONOS operating at positive gate bias ($V_g > 0, V_D > 0$), Gate controls the tunneling current from Schottky barrier at the source side to channel. Typical band diagram are sketched in Fig. 3-1(a) and (b) [34-36]. Under low gate bias, small tunneling current inject from source to channel which is limited by large band width. At low gate bias, the current is dominated by thermionic emission. As the gate voltage increases, the barrier width become narrow due to the band bending, causing electron easily tunnel to channel. At high electric field, the current is dominated by field emission, as shown in Fig. 3-1(b).



(a)



(b)

Fig. 3-1 (a) The band diagram for SB-SONOS when V_g>0, V_D>0. By increasing the V_g, larger band bending occurred and then causing electrons much easily tunnel through the barrier from source to channel. (b) From the band diagram plot it shows that Schottky barrier tunneling is much faster than thermal emission tunneling [34-36].

When SB-SONOS operating at negative gate bias ($V_g < 0, V_D > 0$), hole also pass through Schottky barrier to form hole channel. Similar to on state, as increasing the negative gate bias, the barrier width for hole becomes narrowing, thereby reduce the hole tunneling distance, causing large drain current at negative bias, the typical band diagram is sketched in Fig. 3-2 [34-36]. In order to eliminate the ambipolar behavior, different metal silicide material is performed. Different material has different Schottky barrier height for electron (ϕ_n) and hole (ϕ_p). For N-type SONOS, it use $ErSi_{2-x}$ 、$YbSi_{2-x}$ or $DySi_{2-x}$ to form silicide, due to low Schottky barrier height for electron. And for P-type SONOS, it use PtSi due to low Schottky barrier height for hole [37-41].

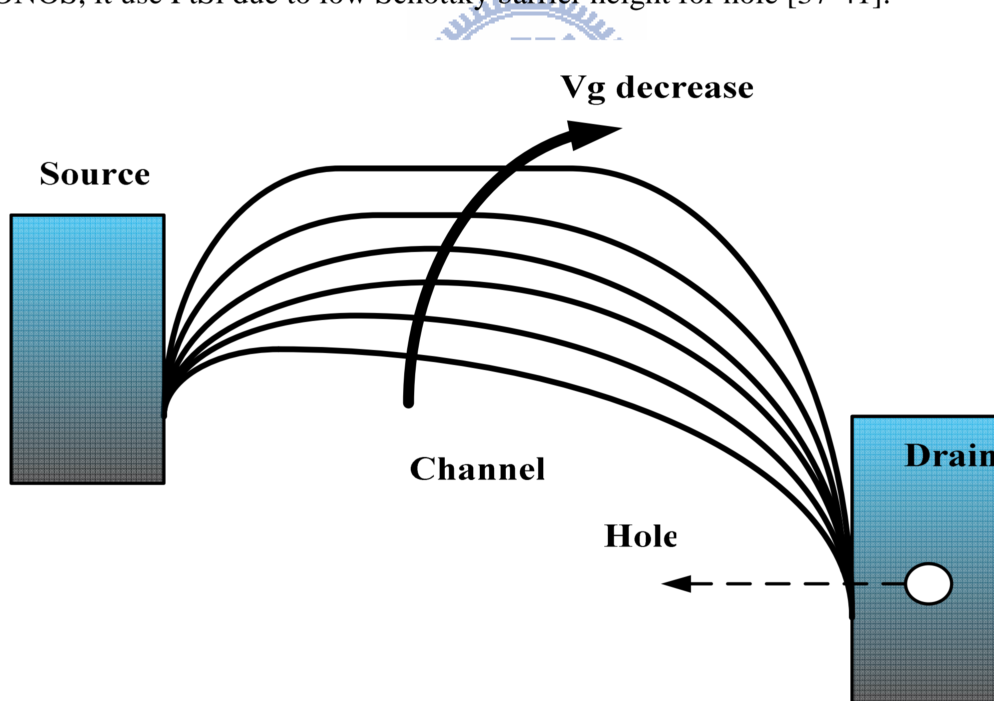


Fig. 3-2 The band diagram for SB-SONOS when $V_g<0$, $V_D>0$. By decreasing the V_g, the band bending is getting sharper and then causing holes much easily tunnel through the barrier from drain to channel [34-36].

3-2. DSSB-SONOS Operation Principles

However using different metal silicide is indeed eliminate ambipolar effect, but for CMOS technology, the process with dual-silicide is hard to receive, because each metal silicide shows particular forming temperature. Therefore, DSSB-SONOS has been demonstrated to improve the performance. From the plot it can find out that DSSB-SONOS shows large on/off current ratio compared to SB-SONOS, as shown in Fig. 3-3.

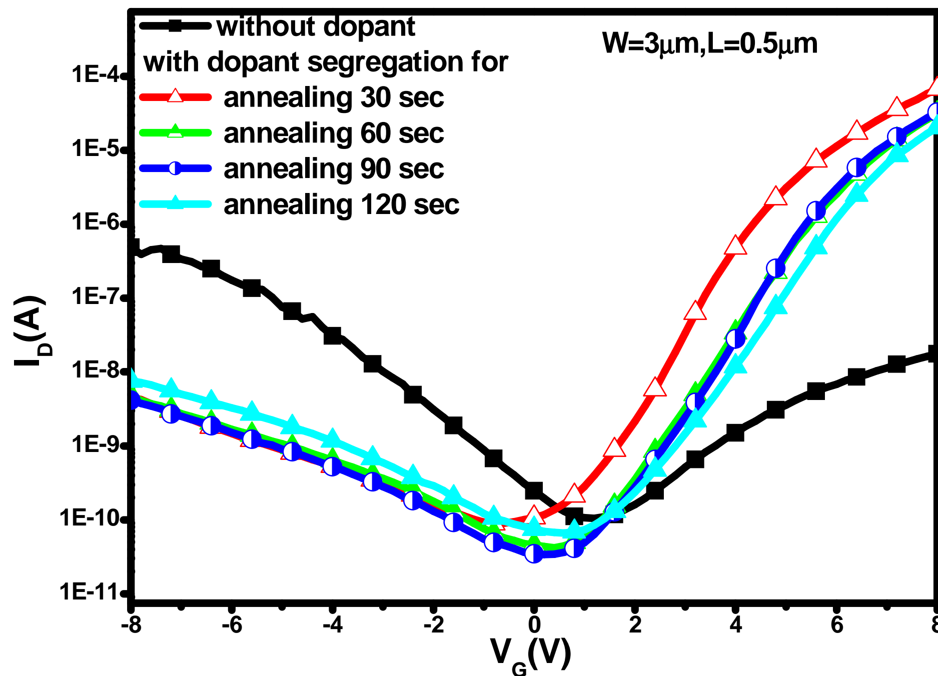
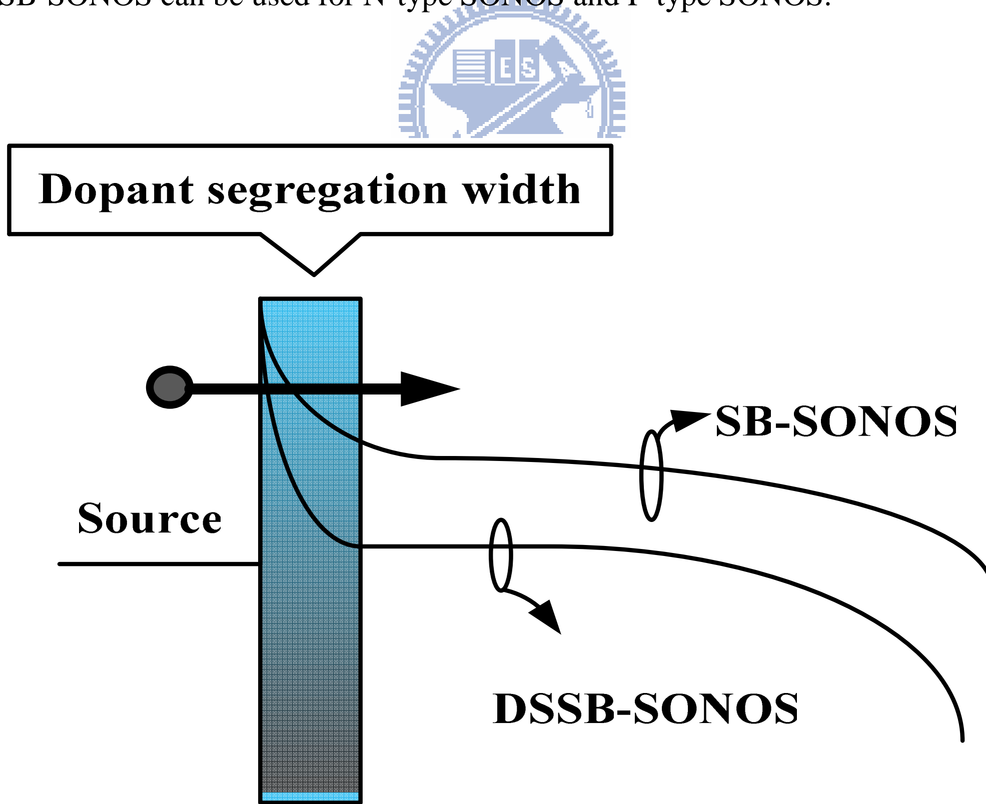
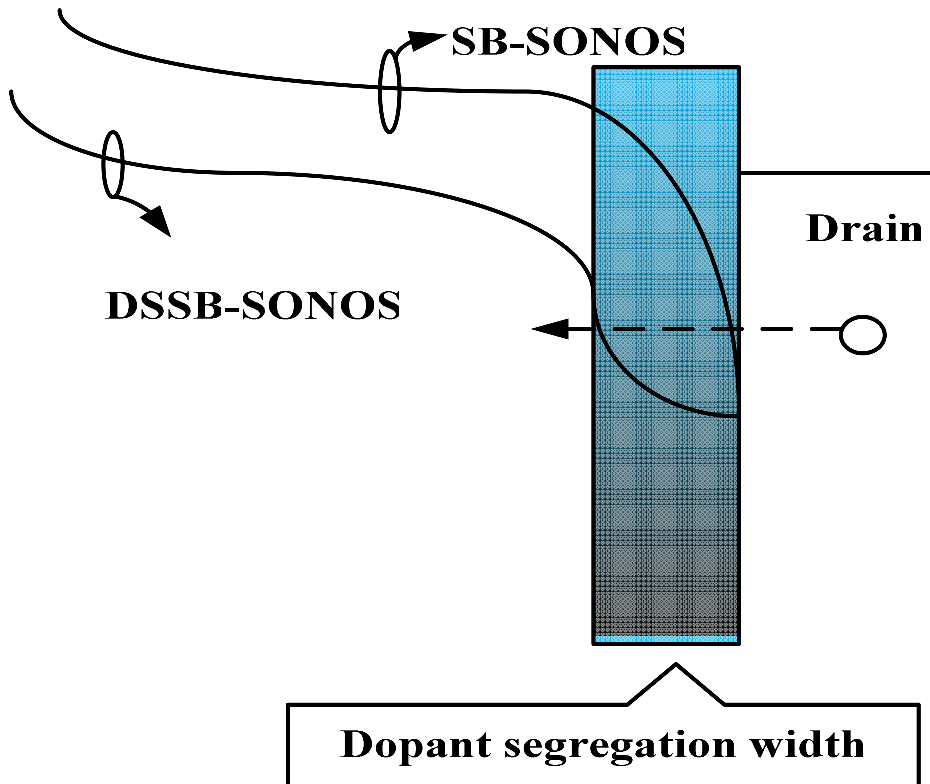


Fig. 3-3 The I-V characteristic for SB-SONOS and DSSB-SONOS devices.

The difference transfer characteristics between two devices can be considered by energy band bending along the channel. Typical band diagram is shown in Fig. 3-4. For SB-SONOS with doping A_S, it shows that when under positive gate bias, the band bending of conduction band can lower the effective Schottky barrier height at source side region, increasing the drive current. On the other hand, under negative gate bias, the band bending of valance band can widen the Schottky barrier width at drain side region, minimize the hole leakage current. And it shows the device with doping A_S for dopant segregation, the I-V characteristic is similar to conventional N-MOSFETs, that means DSSB-SONOS can be used for N-type SONOS and P-type SONOS.



(a)



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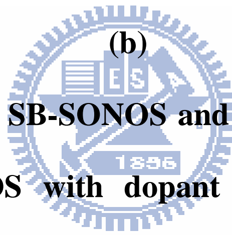
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Fig. 3-4 The band diagram for SB-SONOS and DSSB-SONOS (a) at on-state it shows that SB-SONOS with dopant segregation have larger band bending, causing large on-state current. (b) at off-state it shows that SB-SONOS with dopant segregation have larger band bending, causing band width larger near the drain side and suppress the off-state current [34-36].

3-3. DSSB-SONOS with SOI Substrate

Using Schottky barriers as the source/drain junctions, however, has its downside that can not control the silicide and dopant segregation depth, and will cause the performance un-stability. And it is well known that the dopant concentration peak decreases with

increasing the NiSi thickness [42]. Hence, SB-SONOS is attempted to use SOI substrate to replace bulk substrate, in order to control the silicide depth. Recently, a study of the Si body thickness in SOI substrate has also revealed the interest of ultra thin (~10 nm) channel thickness in order to increase the drive current [43]. The reason is that, the shape of the Schottky barrier is dependent on the Si body thickness. Moreover, by using SOI substrate could also decrease the sub-threshold swing. The typical formula for sub-threshold swing is [30]:

$$S \cong \frac{kT}{q} \ln 10 * (1 + \frac{C_D}{C_{ox}}) \tag{3-1}$$

where C_D is the depletion-layer capacitance, C_{ox} is gate oxide capacitance. For bulk substrate, the sub-threshold swing value can be decreased to 60 (mV/decade) when decreasing the gate oxide thicknesses. For SOI wafer, the typical formula for sub-threshold swing is:

$$S \cong \frac{kT}{q} \ln 10 (\frac{\frac{1}{C_{ox1}} + \frac{1}{C_{si}} + \frac{1}{C_{ox2}}}{\frac{1}{C_{si}} + \frac{1}{C_{ox2}}}) \tag{3-2}$$

Where C_{ox1} is gate oxide capacitance, C_{si} is silicon across capacitance, C_{ox2} is buried oxide capacitance. When buried oxide is much thicker than gate oxide and the silicon, then

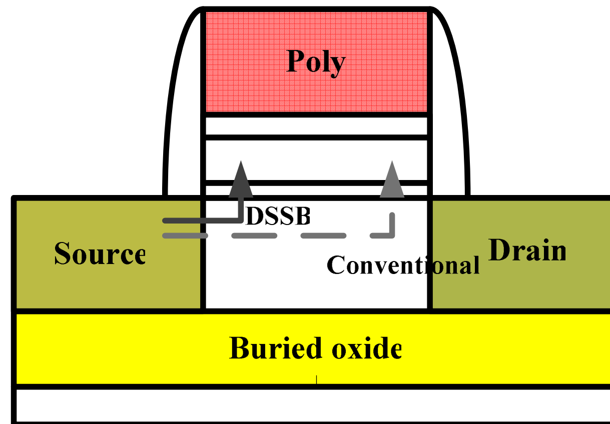
$$S \cong \frac{kT}{q} \ln 10 \tag{3-3}$$

The sub-threshold swing value could be decreased to minimum value, and then

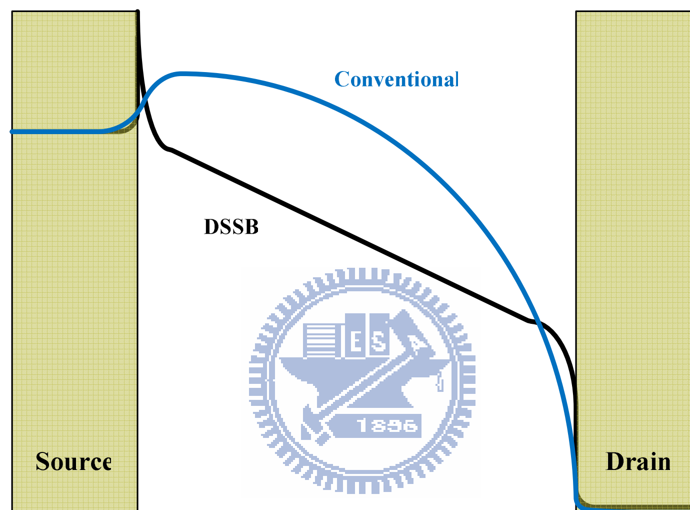
improve the device performance. For conventional SONOS, electrons use thermal emission to overcome the barrier heights. However, DSSB-SONOS with SOI Substrate could obtain much smaller sub-threshold swing because it use tunneling rather than thermal emission, as the Fig. 3-1(b) shows [34-36].

3-4. Source Side Injection

Fig. 3-5 shows the injection mechanism for conventional SONOS and DSSB-SONOS. For conventional SONOS, hot electron tunneling occurs at pinch-off region where $V_{DS} > V_{GS} - V_t$, due to large electric field at drain side region. Pinch-off region is at drain side, so at drain side carriers may cause impact-ionization. And by impact-ionization, it will create electron and hole pairs. At the same time, when gate apply positive bias, hot electron may tunnel through gate oxide to nitride due to vertical electric field, as shown in Fig. 2-4. However, for DSSB-SONOS, when the program condition of V_G>0 and V_D>0, large band bending occurs at source side region, hence electron can easily tunnel through the Schottky barrier. And then, owing to drain side region has low vertical electrical field compared to source-side region (V_{GS}>V_{GD}), charge may be trapped at source side rather than drain side. Hence, for DSSB-SONOS, charge injects to source side region; for conventional SONOS, charge injects to drain side region [44].



(a)



(b)

Fig. 3-5 (a) The difference between DSSB-SONOS and conventional SONOS devices in terms of charge injection of hot electrons. For DSSB- SONOS devices, charge inject to source side and for conventional SONOS devices, charge inject to drain side (b) The typical energy band diagram of DSSB-SONOS and the conventional SONOS devices [44].

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CHAPTER 4

Fabrication and Characterization Methods

4-1. Device Fabrication

The process flow of SB-SONOS, DSSB-SONOS, and conventional SONOS devices are shown from Fig. 4-1 to Fig. 4-5. The starting material was boron-doped 6 inch test wafer with a resistivity of 4~100Ω-cm. At first, a 550 nm thick thermal oxide was grown to form buried oxide which was deposited by horizontal furnace, and then followed by a conformal deposition of 60 nm thick amorphous Si (α-Si) layer. Sequentially, a solid-phase-crystallization (SPC) at 600℃ in a N_2 ambient for 24 hours was performed to transform the α-Si into poly-Si. Afterward, through I-line stepper and TCP9400-poly etcher to define active region, as shown in Fig. 4-1.

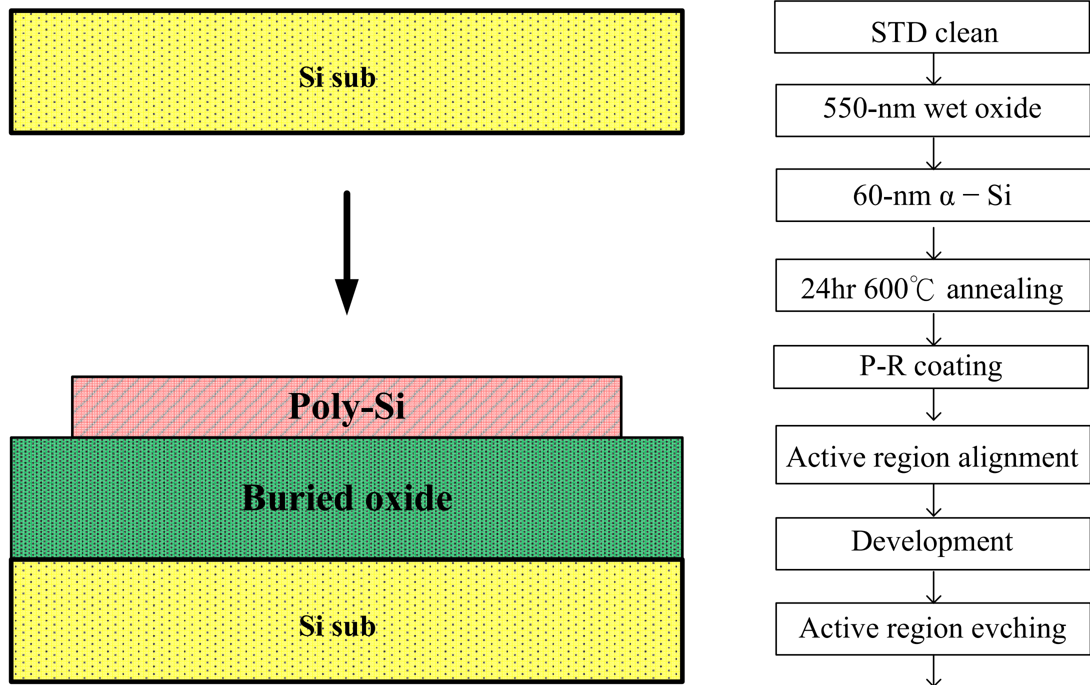


Fig. 4-1 Key fabrication and process flow of active region.

After active region forming, a 4 nm thick SiO_2 was grown to form tunneling layer which was deposited by vertical furnace. Sequentially, a 8 nm thick nitride (as trapping layer) and 12 nm thick tetra-eth1-ortho-silicate (TEOS) SiO_2 (as blocking layer) films were deposited by horizontal furnace. At last 100 nm thick phosphorous in-situ doped poly was sequentially deposited for gate electrode. Then we use I-line stepper, TCP9400-poly etcher and TEL5000-oxide etcher to define gate region, as shown in Fig. 4-2.

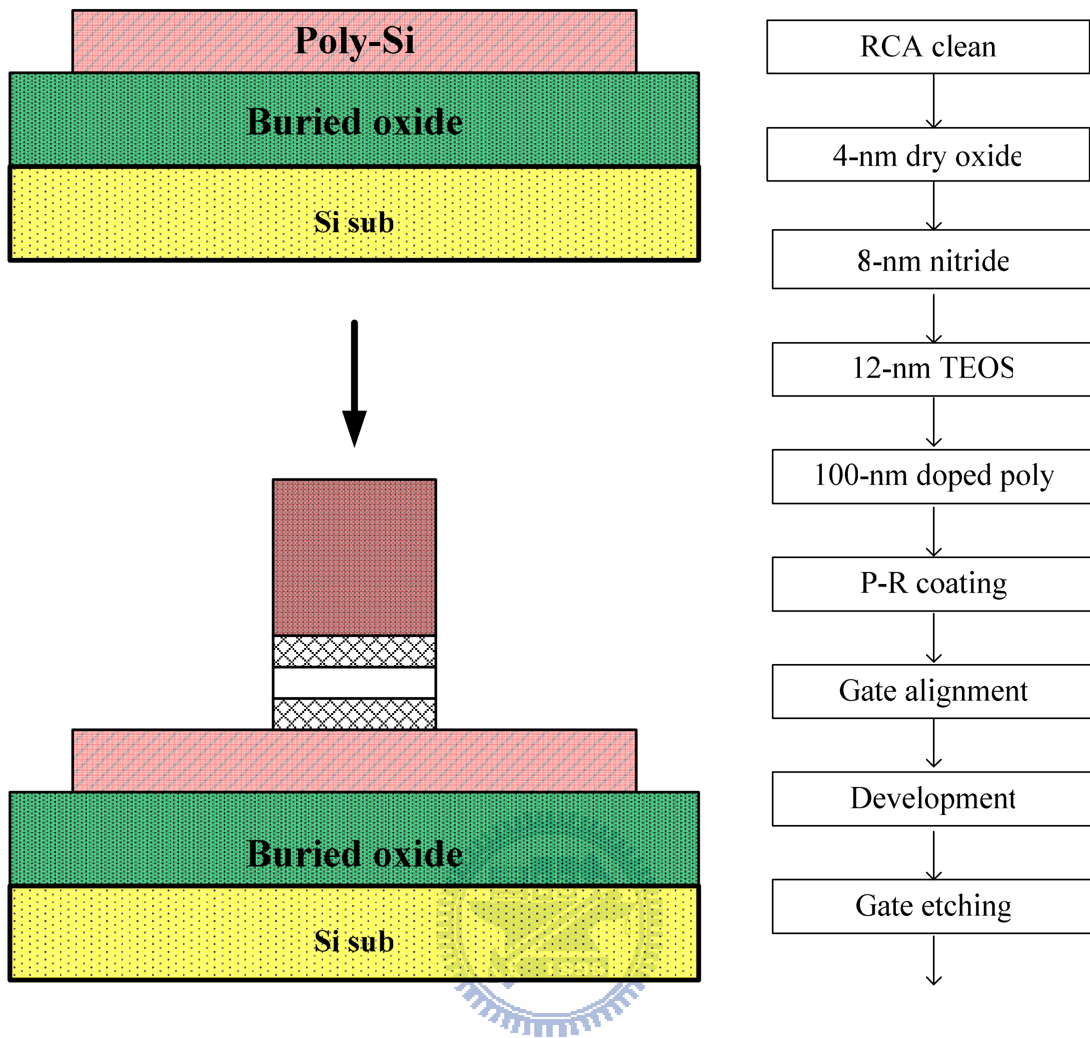


Fig. 4-2 Key fabrication and process flow of gate region.

For conventional SONOS device, after gate region forming, as shown in Fig. 4-2, a 150 nm thick TEOS was grown to form sidewall spacer which was deposited by horizontal furnace and then followed with plasma etching by TEL5000-oxide etcher. Then, implant As with energy 10keV and dose $5\times10^{15}\,cm^{-2}$ into active region. Before activation annealing, use DHF (50:1) to remove the native oxide then followed with activation annealing for 1100℃ 10seconds, as shown in Fig. 4-3.

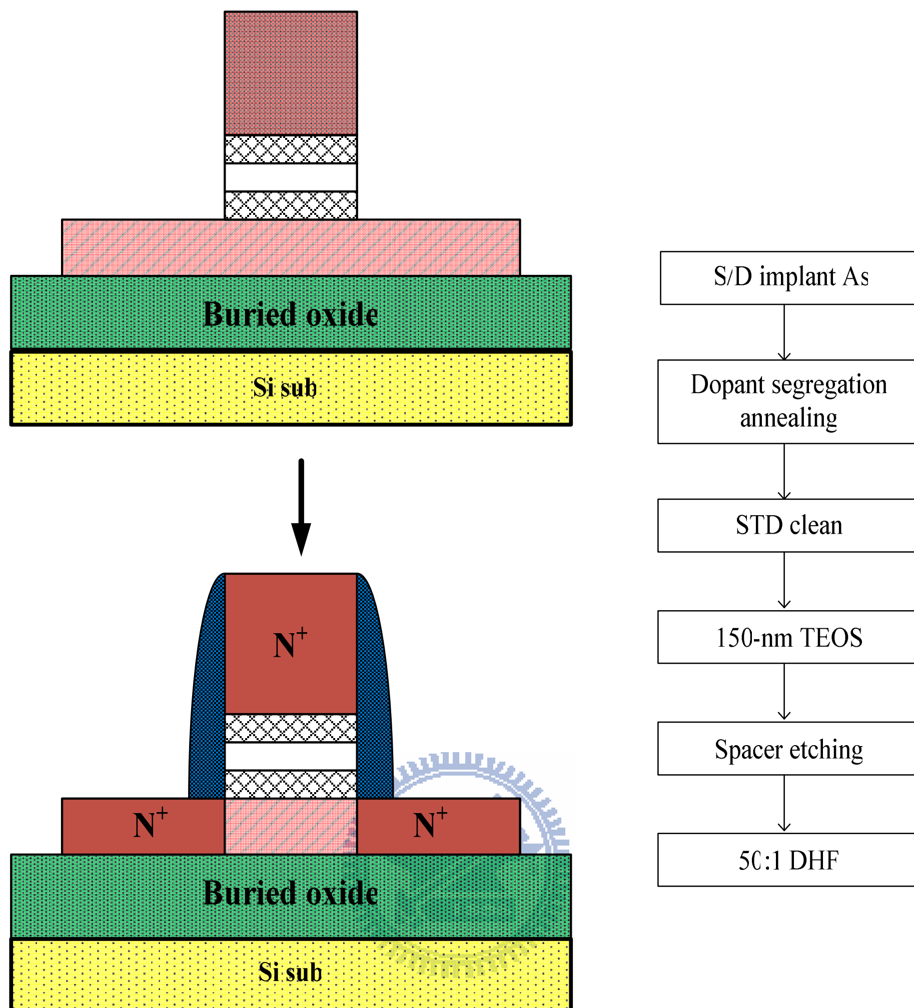


Fig. 4-3 Key fabrication and process flow of conventional SONOS device.

For SB-SONOS and DSSB-SONOS devices, after gate region forming, as shown in Fig. 4-2, a 150 nm thick TEOS was deposited by horizontal furnace and etched by TEL5000 oxide etcher to form sidewall spacer. Afterward, 20 nm thick nickel and 10 nm thick titanium nitride was deposited by FSE Cluster PVD. And then proposed self-aligned

silicidation by using rapid-thermal annealing (RTA) for one step annealing and two step annealing. For one step annealing, the RTA process is at 550℃ in a N_2 ambient for 30seconds, and for two step annealing, the forming process is at 300℃ in a N_2 ambient for 15~60 minutes, owing to find the best first step annealing time, and then following with RTA at 550℃ in a N_2 ambient for 30seconds to transform form Ni_2Si to NiSi. The sheet resistance for NiSi is 4.3Ω/□. And the un-reacted Ni was removed by H_2SO_4/H_2O_2 (3:1) solution. Hence, NiSi was formed at source/drain and gate region. The SB-SONOS process was then performed and the resulting structure is shown in Fig. 4-4.

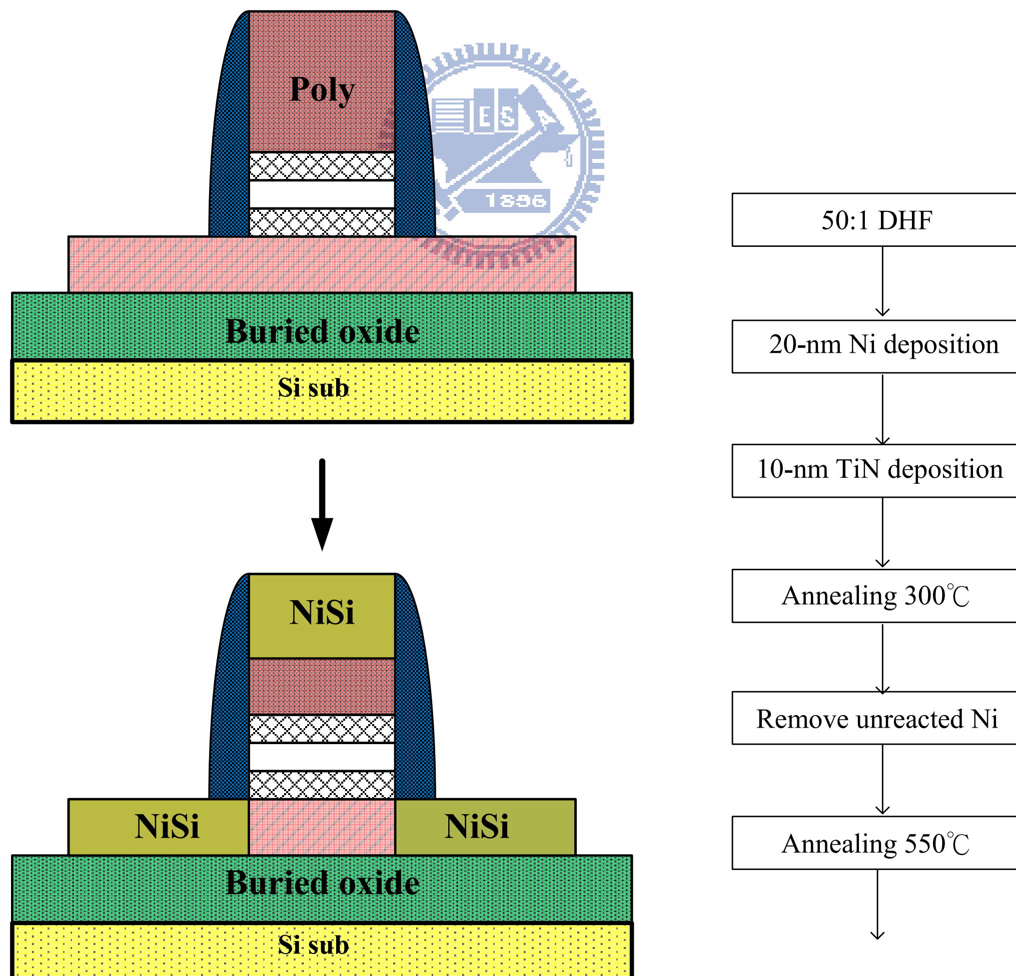


Fig. 4-4 Key fabrication and process flow of SB-SONOS device.

To improve SB-SONOS characteristics, ITS technique were used which is implanted As to the silicide with energy 10keV and with the dose 5×10^{15} cm^{-2} to formed DSSB-SONOS. And then followed with RTA at 500℃、600℃、700℃ in a N_2 ambient for 30seconds、60seconds、90seconds、120seconds to activate dopant. After activation annealing, dopant will segregate at silicide and Si interface, as shown in Fig 4-5. For different activation annealing time, different dopant segregated width at interface will get, so could obtain different I-V characteristics.

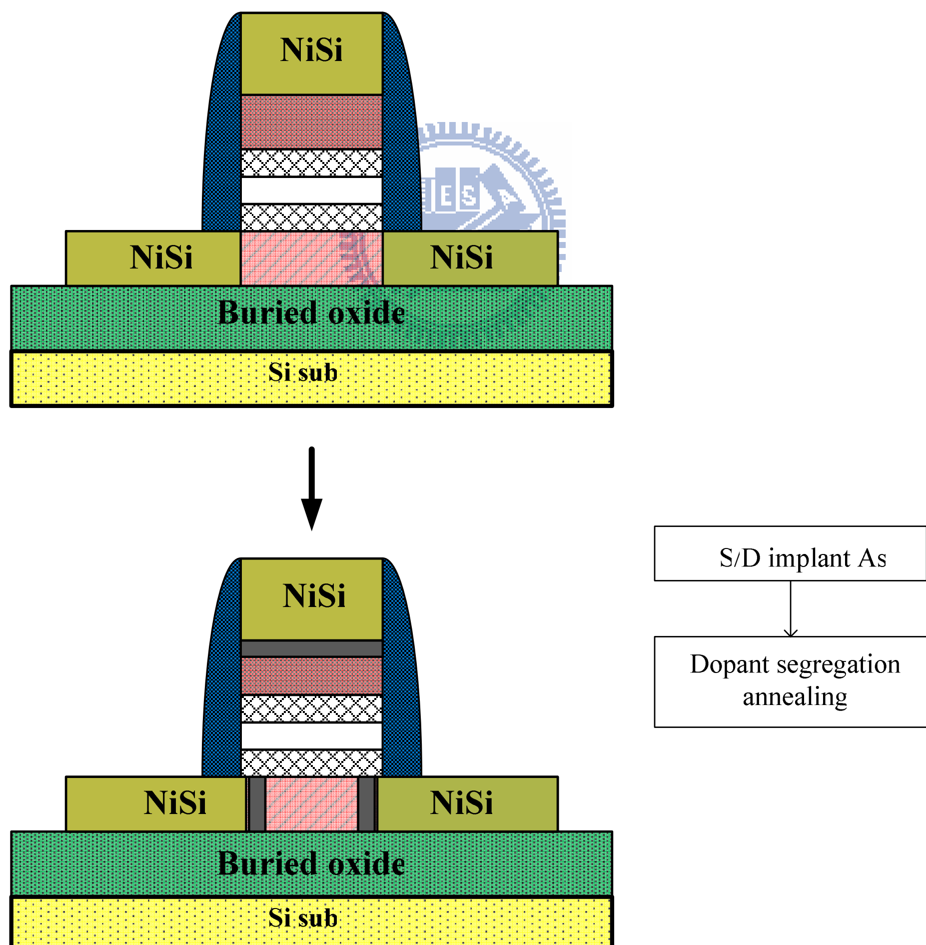


Fig. 4-5 Key fabrication and process flow of DSSB-SONOS device.

For material analysis like XRD and sheet resistance measurement, since different NiSi thickness will cause different sheet resistance, so we use the structure for NiSi on poly silicon. The starting wafer was boron-doped 6 inch test wafer with a resistivity of 4~100Ω-cm. a 550 nm thick thermal oxide was grown to form buried oxide which was deposited by horizontal furnace, and then followed by a conformal deposition of 60 nm thick amorphous Si (α-Si) layer. Sequentially, a solid-phase-crystallization (SPC) at 600 ℃ in a N_2 ambient for 24 hours was performed to transform the α-Si into poly-Si.

Then, 20 nm thick nickel and 10 nm thick titanium nitride was deposited by FSE Cluster PVD. Afterward, proposed self-aligned silicidation by using rapid-thermal annealing (RTA) at 300℃~750℃ for 30seconds in a N2 ambient to obtain the sheet resistances versus annealing temperature plot. For NiSi XRD analysis, the wafers apply the same condition to DSSB-SONOS devices of two step annealing. The process is shown in Fig. 4-6.

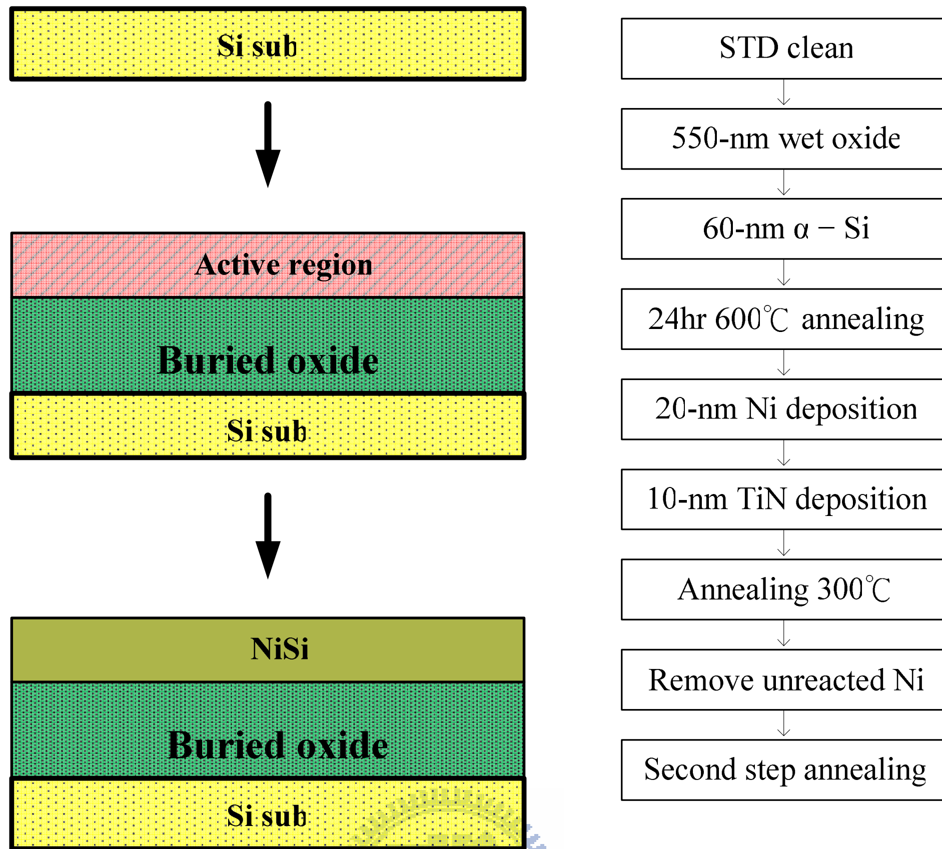


Fig. 4-6 Key fabrication and process flow of NiSi on poly silicon.

4-2. Microstructure Characterization and Analysis

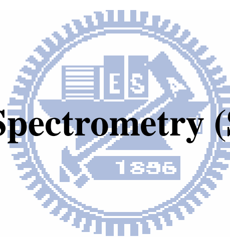
4-2.1 X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is used for phase identification of a crystalline material and can determined crystal structure. It provides information on structures, phases, and other structural parameters, such as average grain size, crystal defects. The X-ray Diffraction analysis is performed by using 2θ scan from 2theta (20) to 2theta (80) and use Reciprocal space mapping to obtain crystalline material and crystal phase. The peak of

X-ray diffraction is produced by constructive interface of the monochromatic beam scattered from each set of lattice planes at specific angles. In this work, we use XRD system to analyze the crystalline status of NiSi film. (In NDL)

4-2.2 Scanning Electron Microscope (SEM)

Scanning electron microscope (SEM) is a type of electron microscope that images the sample surface by scanning it with a high-energy beam of electrons in a raster scan pattern. The SEM analysis is performed with 15 kV accelerating voltage and enlargement factor of 55000. (In NDL)



4-2.3 Secondary Ion Mass Spectrometry (SIMS)

Secondary ion mass spectrometry (SIMS) is an analytic technique to analyze the composition of solid phase and thin films by sputtering the surface of the specimen with a focused primary ion beam and collecting and analyzing ejected secondary ions. Secondary ions which are formed during the sputtering are extracted and analyzed using a mass spectrometer. It can provide elemental depth profiles over a depth range from a few angstroms to tens of microns. (In NDL)

4-2.4 Transmission electron microscope (TEM)

The cross section of fabricated sample could be observed by using Transmission

electron microscope (TEM). The principle of TEM is similar to that of optical microscope. In TEM, observation is made in an ultra high vacuum condition, where an electron beam is focused onto the sample by using electromagnetic lenses Because the wavelength of the electron beam is less than that of visible spectra, the resolution of TEM is higher than that of the conventional optical microscope. In this work, the SB-SONOS is prepared by using a focus ion beam (FIB) system with FEI Tecnai™ G2 F-20 for observing the structure. (In MA-tek.)

4-2.5 Energy-dispersive X-ray spectroscopy (EDX)

Energy-dispersive X-ray spectroscopy (EDX) is an analytical technique used for the elemental analysis or chemical characterization of a sample. It is one of the variants of X-ray fluorescence spectroscopy which relies on the investigation of a sample through interactions between electromagnetic radiation and matter, analyzing X-rays emitted by the matter in response to being hit with charged particles. In this work, the source/drain region for SB-SONOS is analyzed by using 200keV electron beam to analyze the silicided region. (In MA-tek.)

4-3 Electrical Measurements

The measurement system combined Keithley 4200 and pulse generate card for 4205-PG2 is used to measure I-V, retention and endurance characteristics of SB-SONOS,

DSSB-SONOS and conventional SONOS devices.

For programming operation, a positive voltage is applied to the gate in order to cause a strong electric field and the tunneling of electrons induced in the channel through the thin tunnel oxide layer and captured by the trapping centers in the storage nitride layer. For erasing operation, source is grounded, drain is applied positive voltage, and a negative voltage is applied to the gate in order to de-trap the electrons stored in the nitride layer.

The retention characteristic refers to the ability of the memory cell to keep the trapped charge over a period of time to retain the stored data information. When measurement, we place sample over a period of time (1sec, 10sec, 100sec, 10^3sec, 10^4sec and 10^5sec) and then get the I_D-V_{GS} plot to observe the threshold voltage. The 10 years line is extracted by extension line. The extension line starts from the 10^4 sec to 10^5 sec and then extends the line to 10 years.

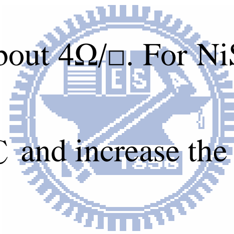
For endurance characteristic refers to the reliability of the memory cell which is defined by the number of P/E cycles that can still retain acceptable P/E window on device without failure. However, P/E operations of flash memory are applied with a very high voltage hence the energetic carriers would degrade the tunneling oxide and nitride trapping layer. This work will stress the sample with 10^4 times P/E cycles to to observe the threshold voltage degradation. (In NTHU)

CHAPTER 5

Results and Discussion

5-1. Material Analysis

Fig. 5-1 shows the temperature window for NiSi. It shows Ni film on silicon, there are three types of silicide phases, Ni_2Si, NiSi, $NiSi_2$ which are formed at temperature 300℃, 500℃, 750℃, respectively. Among the three types of silicide phases, $NiSi_2$ has the highest resistivity, Ni_2Si has the sheet resistance about 11Ω/□ and NiSi has the lowest resistivity with sheet resistance about 4Ω/□. For NiSi, which is metastable state, could be easily turn to $NiSi_2$ phase at 700℃ and increase the sheet resistance, as shown in Fig. 5-1



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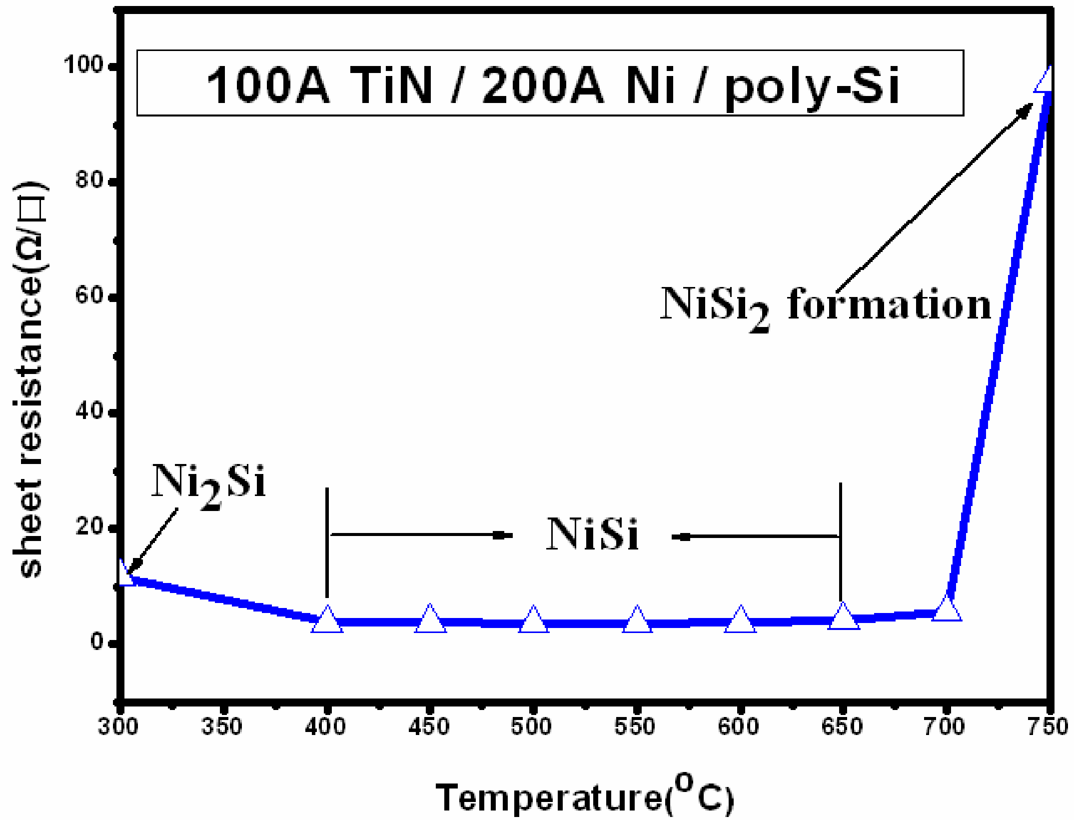

Fig. 5-1 Sheet resistances of nickel silicide film as a function of annealing temperature.

Table 5-1 shows the sheet resistances of NiSi. It shows one step annealing for 550℃ 30 seconds and two step annealing for 300℃ 15minutes~60minutes following with 550℃ 30 seconds. For one step annealing, the sheet resistance is 4.22Ω/□ and for two step annealing, the sheet resistances are 4.68Ω/□, 4.74Ω/□, 4.29Ω/□, 4.51Ω/□, respectively for the first step annealing 300℃ 15minutes, 30minutes, 45minutes, 60minutes following with the second step annealing 550℃ 30 seconds. And Fig. 5-2 shows the X-ray Diffraction (XRD) of the silicide for two step annealing. From the above data, it can be found that 300℃ 45minutes is the suitable annealing condition to form Ni_2Si and then using rapid thermal annealing (RTA) 550℃ 30 seconds to transfer from

Ni_2Si phase to NiSi phase.

	R_{SD}(Ω/□)
One step annealing 550℃, 30sec	4.22
Two step annealing	
1st: 300℃, 15min 2nd: 550℃, 30sec	13.37 4.68
1st: 300℃, 30min 2nd: 550℃, 30sec	13.74 4.74
1st: 300℃, 15min 2nd: 550℃, 30sec	11.76 4.29
1st: 300℃, 15min 2nd: 550℃, 30sec	12.33 4.51

Table 5-1 Sheet resistances of nickel silicide with silicidation for different annealing condition.

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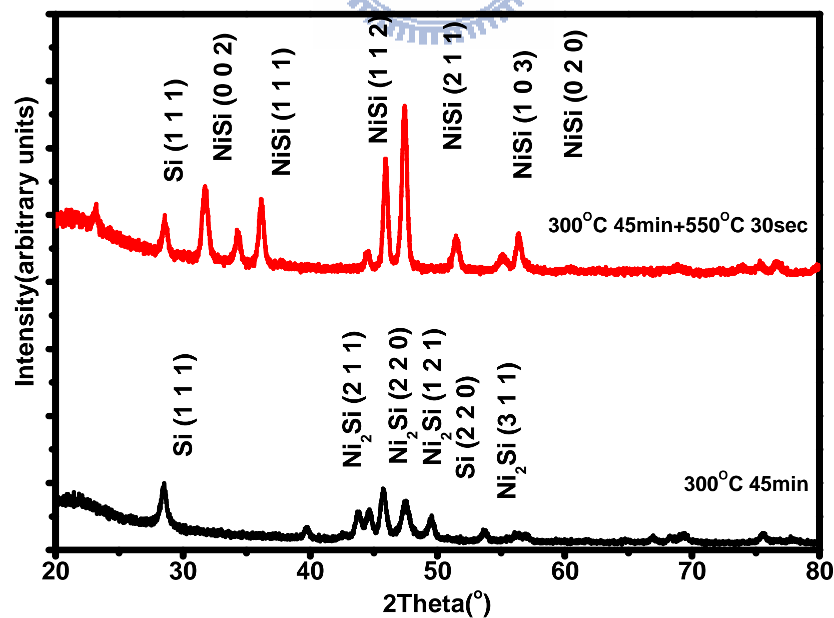
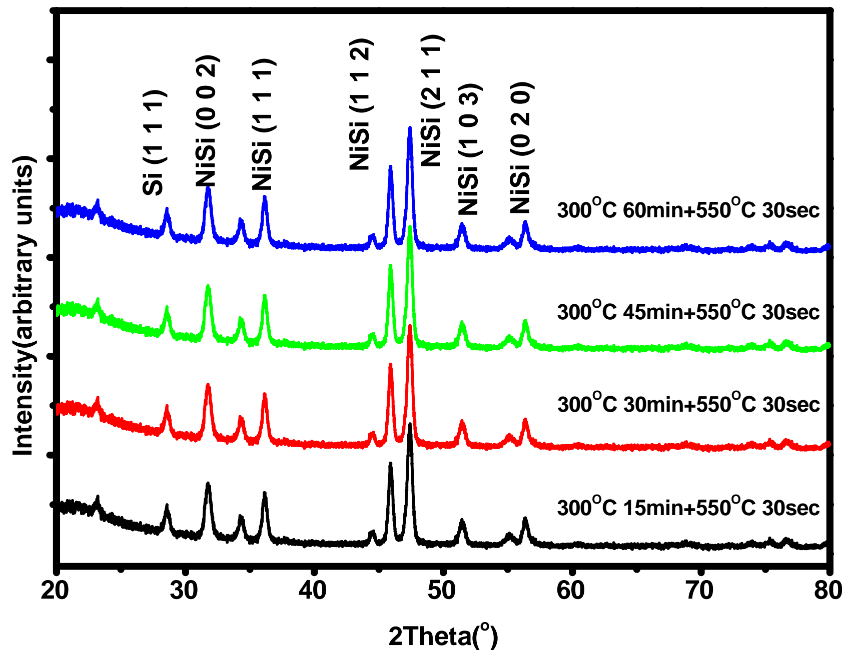


(a)



(b)

Fig. 5-2 (a)XRD spectra of Ni silicide with first step annealing for 300℃, 45 minutes and two step annealing for 300℃, 45 minutes followed with 550 ℃, 30 seconds for second step (b) XRD spectra of Ni silicide for different first step annealing time followed with 550℃, 30 seconds for second step.

5-2. The Characteristics of SB-SONOS and DSSB-SONOS Memory Devices

The DSSB-SONOS device is determined by cross-sectional transmission electron microscope (TEM) image, as shown in Fig. 5-3. The thickness of tunneling oxide is about 4.4 nm, trapping layer is about 7.1 nm, and blocking oxide is about 12.9 nm. From energy-dispersive x-ray spectroscopy (EDX) analysis at point A and B labeled in Fig. 5-4(a), it is observed that the silicided doesn't growth into the channel region.

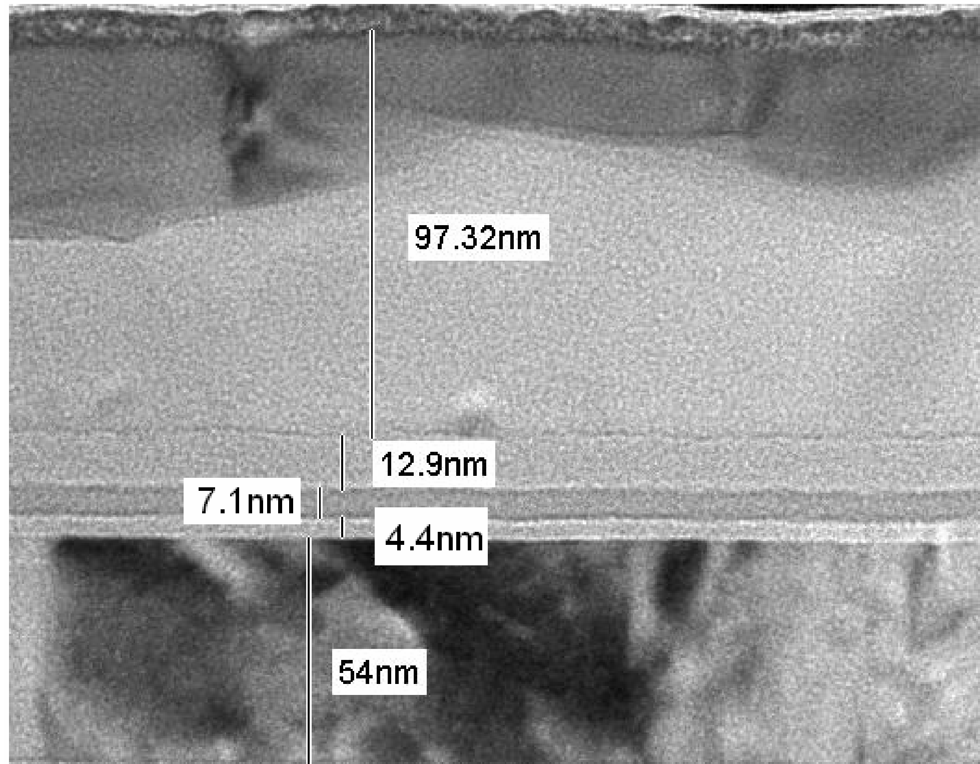
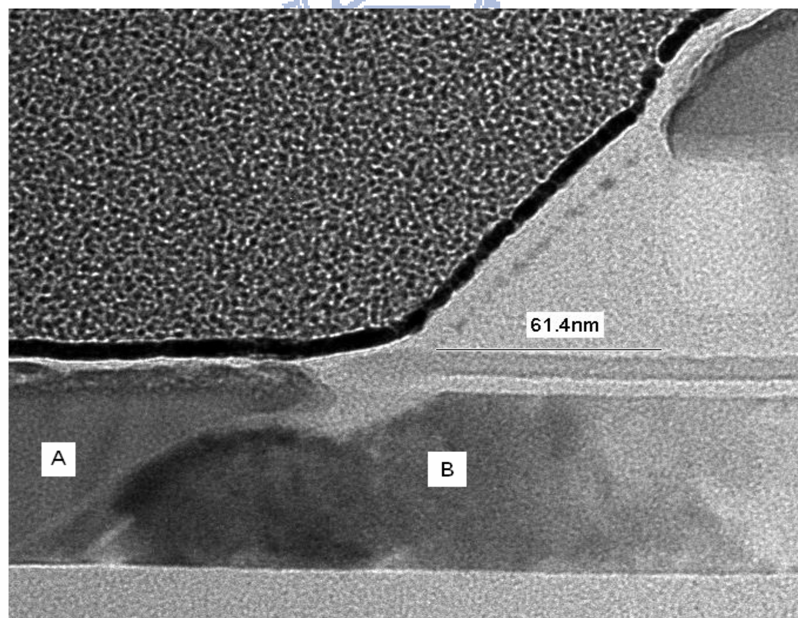
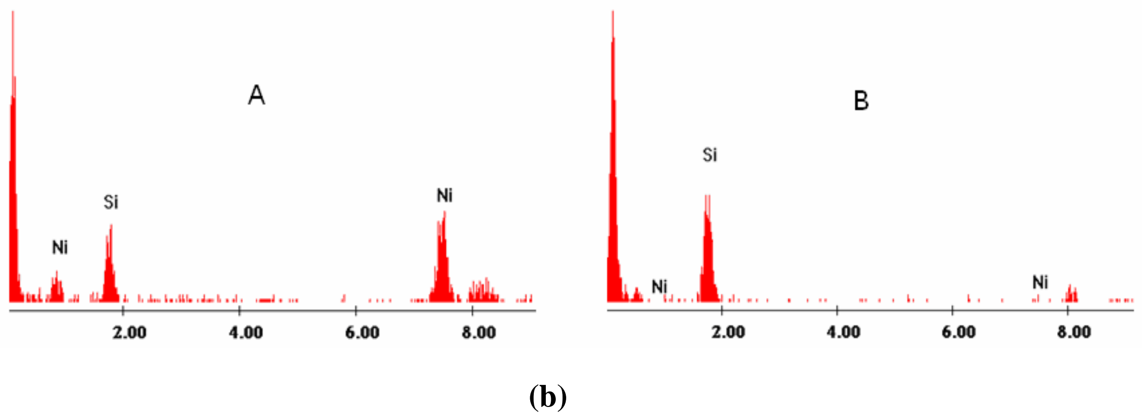


Fig. 5-3 TEM image of DSSB-SONOS for gate structure.



(a)



(b)

Fig. 5-4 (a)TEM image of DSSB-SONOS for source/drain structure (b) The EDX analysis data of point A and point B.

Fig. 5-5 shows the current-voltage characteristics with shifting the fresh state of threshold voltage to the same value. The figure includes the fresh state, the program state, and the erase state of three devices, respectively for SB-SONOS, DSSB-SONOS, and conventional SONOS devices. From the figure, it shows that different types of devices have different I-V characteristics, sub-threshold swing, and memory window, and different P/E speed, retention, endurance characteristics. From Fig. 5-5, it shows that DSSB-SONOS devices have the largest on current and small sub-threshold swing. And SB-SONOS devices have largest memory window but also show the small on current. All of the performances for SB-SONOS, DSSB-SONOS, and conventional SONOS devices will be discussed in this work.

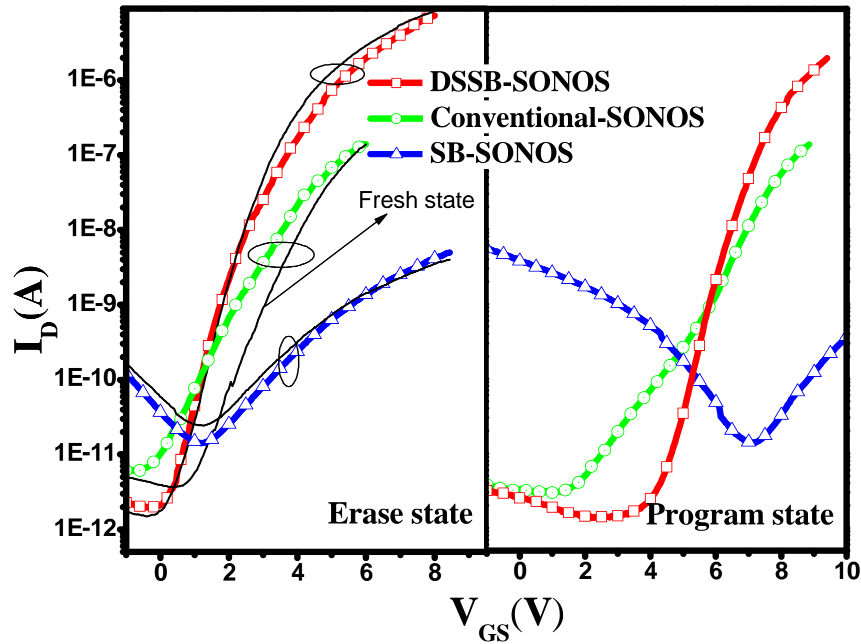


Fig. 5-5 Current-voltage characteristics of conventional SONOS, SB-SONOS, and DSSB-SONOS devices with shifting the fresh state of threshold voltage to the same value.

Fig. 5-6 shows the I_D-V_G characteristics of the three devices, the devices are for channel length 1μm and width 3μm. DSSB-SONOS devices show the better sub-threshold swing and larger on current. The principle was stated in the previous chapter. DSSB-SONOS devices have larger on current than conventional SONOS devices, due to low parasitic resistance. And SB-SONOS devices show small on current about 10^{-9} order, due to approximate constant potential at source side region, as shown in Fig. 3-1 and Fig. 3-2. And the current density formula is shown in below.

$$J_{m \to s} = A^{*}T^{2}\exp(-\frac{q\phi_B}{kT}) \quad (2\text{-}7)$$

according to the formula, it shows that the current density depends to the Schottky barrier height. Since, SB-SONOS has larger Schottky barrier height and barrier width, causing low drive current.

DSSB-SONOS devices provide higher on current about 10^{-6} order, due to high electric field at source side region, causing large band bending and then electron can easily tunnel from source to channel, as shown in Fig. 3-4(a). Moreover, DSSB-SONOS devices show small leakage current. The reason is also due to band bending. DSSB-SONOS devices show large Schottky barrier width at drain side region, causing leakage current is suppressed, as shown in Fig. 3-4(b). For SB-SONOS, because we apply drain voltage to 3V so it shows the leakage current is larger than drive current. In other words, on state bias(V_{GS}=8V) is smaller than off state bias(V_{GD}=11V), causing larger leakage current.

The I_D-V_G characteristics also show the subthreshold swing difference between SB-SONOS, DSSB-SONOS, and conventional SONOS devices. Since, DSSB-SONOS devices rely on Schottky barrier tunneling for drain current; on the contrary, conventional SONOS devices rely on thermal emission, as shown in Fig. 3-1(b). It is well known that tunneling is much faster than thermal emission and it is the reason why DSSB-SONOS devices have small subthreshold swing and small V_{TH} value.

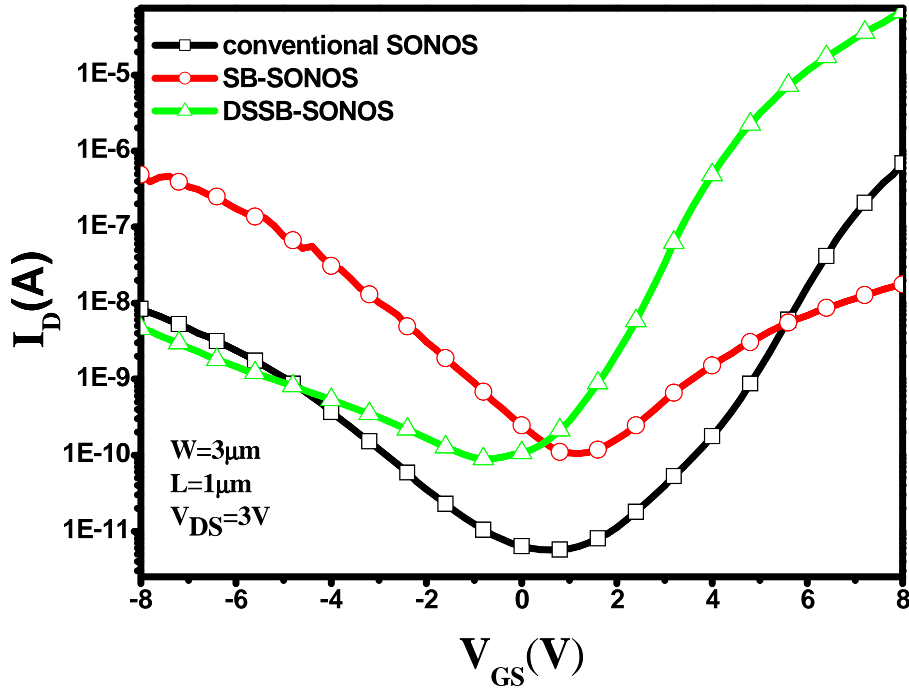


Fig. 5-6 I_D-V_G characteristics of conventional SONOS, SB-SONOS, and DSSB-SONOS devices.

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Fig. 5-7 and Fig. 5-8 show the I_D-V_G characteristics of conventional SONOS and DSSB-SONOS devices with different channel lengths. Both two devices show that the on current significantly increases with reducing the channel length. It can be found that for conventional SONOS devices, the threshold voltage significantly increase from 4.78V, 6.89V, 7.83V, to 8.44V, respectively for channel length 0.5μm, 1μm, 5μm, 20μm. That means short-channel effect is performed. However, DSSB-SONOS devices show little threshold voltage degradation when reducing channel length. The threshold voltage merely increases from 4.05V, 4.38V, 4.45V, to 4.8V, respectively for channel length

0.5um, 1um, 5um, 20um. For SB-SONOS and DSSB-SONOS, it use metal silicide for source/drain, and it may cause MILC effect. However, from Fig. 5-4(b), it shows Ni concentration is too small that MILC effect is not apparently. So the explanation for the phenomenon is owing to Schottky barrier height between metal silicides and Si interface remains approximately constant, therefore short-channel-effect (SCE) can be eliminated. For conventional SONOS devices, when decreasing the channel length, drain induce barrier lowering (DIBL) effect is occurred, causing serious short channel effect.

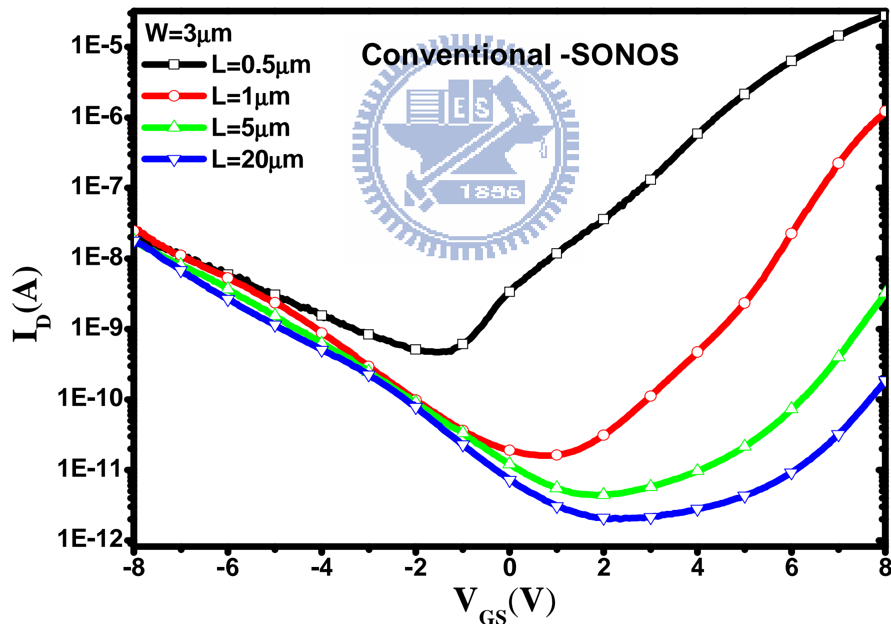


Fig. 5-7 Transfer characteristics of conventional SONOS devices with different channel lengths.

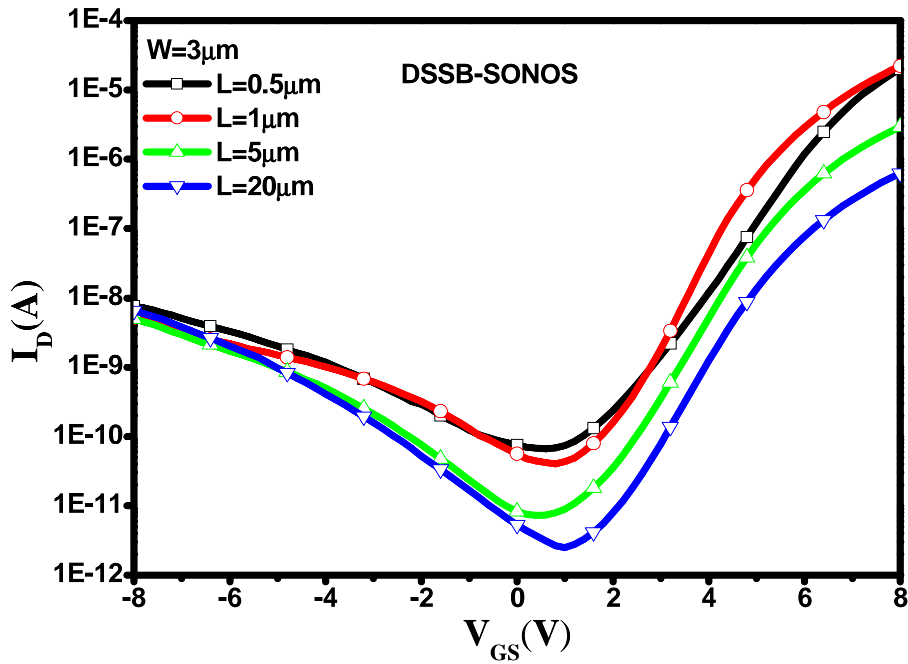
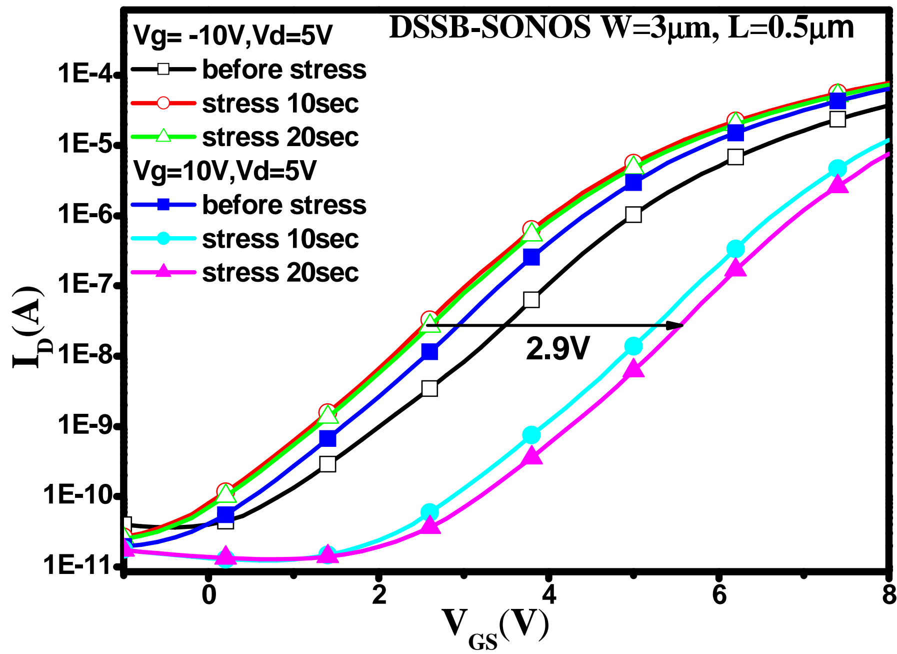
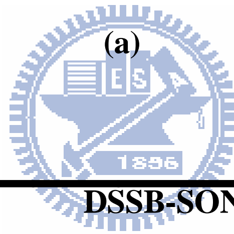


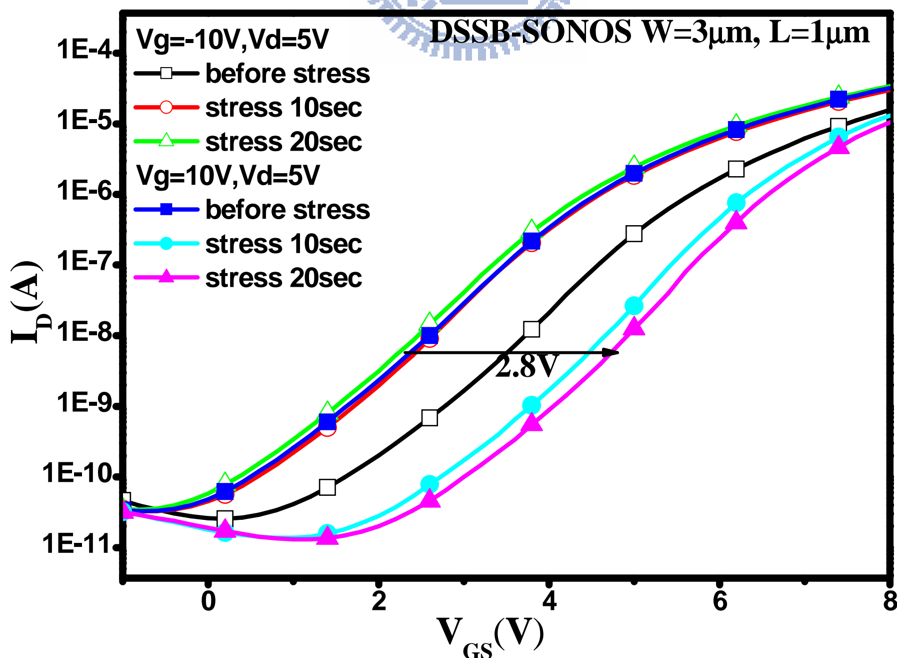
Fig. 5-8 Transfer characteristics of DSSB-SONOS devices with different channel lengths.

Fig. 5-9 shows the memory window of DSSB-SONOS devices with different channel lengths. The I_D-V_G curves started from fresh state, and then apply V_G=-10V and V_D=5V to erase. Afterward, apply V_G=10V and V_D=5V to program in order to get the memory window. It shows that when increasing the channel length the memory window decrease from 2.9V to 0.2V for channel length from 0.5μm to 20μm.



(a)





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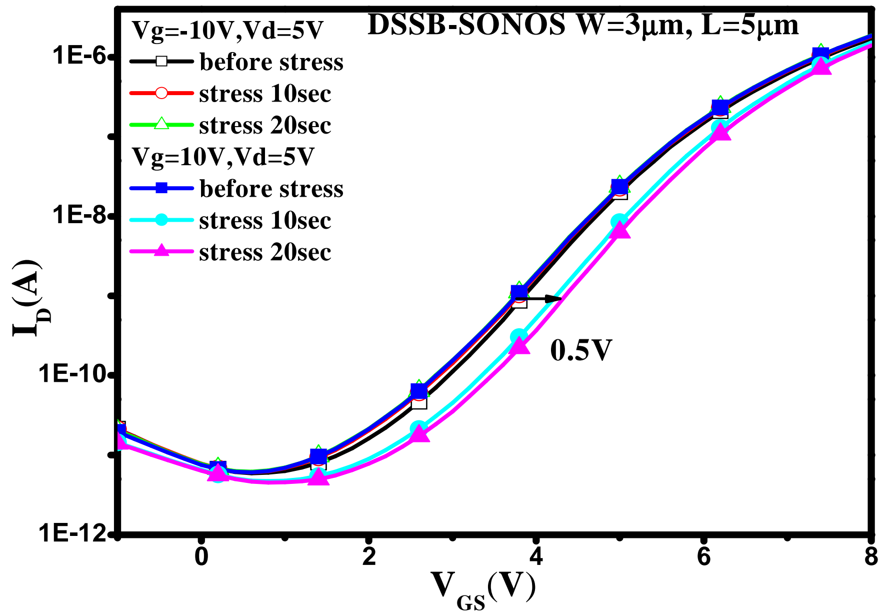
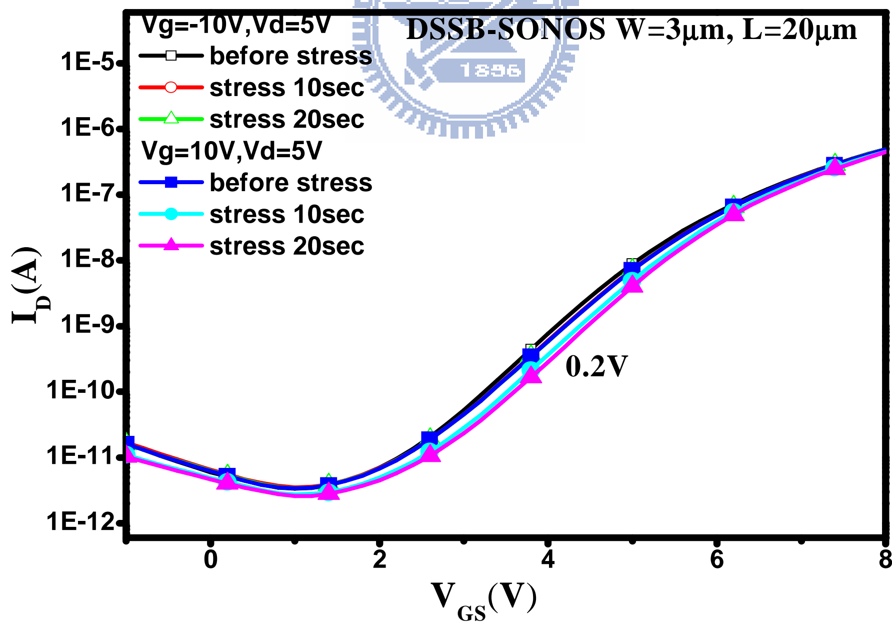


(c)



(d)

Fig. 5-9 Memory window of DSSB-SONOS devices with different channel lengths (a) 0.5um (b) 1um(c) 5um (d) 20um.

5-3. The Program and Erase Characteristics of SB-SONOS and DSSB-SONOS Memory Devices

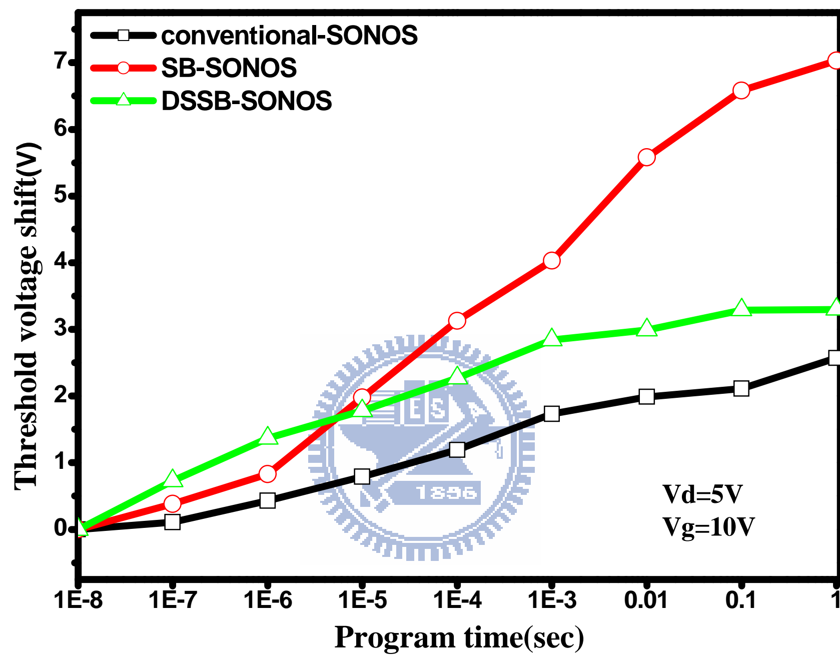
As shown in Fig. 5-9, when increasing the channel length, the memory window decreases. This is due to source side injection mechanism. When programming, for program condition of V_G=10V and V_D=5V, large band bending occurs at source side region, hence electron can easily tunnel through the Schottky barrier. And then, owing to drain side region has low vertical electrical field compared to source-side region (V_{GS}>V_{GD}), charge may be trapped at source side rather than drain side, as shown in Fig. 3-5 [44].

It is well known that under the same program/erase (P/E) condition, the number of electron trapped is the same. So when Fig. 5-9 shows the phenomenon of the larger channel length has smaller memory window, the reason might be the ratio of trapped charge ratio relative to the channel length. Since non-uniformed trapped, which means source side injection, by increasing the channel length the non-uniformed trapped may have small effect on long channel devices. And it is the possible reason for the memory window decreasing when increasing the channel length. However, source side injection has not been proven, therefore this work will try to use programming and erasing characteristics to prove this mechanism.

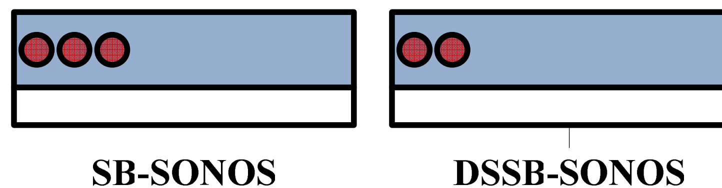
For non-volatile memory device, one of the most important characteristics is program/erase speed. Fig. 5-10(a) shows the program speed of conventional SONOS, SB-SONOS, and DSSB-SONOS devices with V_G=10V and V_D=5V. SB-SONOS devices have fast programming speed for the threshold voltage shift nearly to 3V with program time of 10^{-4} seconds. And conventional SONOS shows slow programming speed for the threshold voltage shift nearly to 1V with program time of 10^{-4} seconds. For conventional SONOS devices, they use thermal emission rather than SB-SONOS and DSSB-SONOS devices use Schottky barrier tunneling to obtain drain current. That is the reason why causing conventional SONOS devices have slower program speed, as shown in Fig. 3-1. And for SB-SONOS and DSSB-SONOS devices, SB-SONOS devices show faster program speed compared to DSSB-SONOS devices. Owing to SB-SONOS devices have larger injection position compared to DSSB-SONOS devices which only have small injection position at source side, causing larger memory window, the typical sketch as shown in Fig. 5-10(b). And Fig. 5-9 also shows that short channel length device gets larger memory window. Therefore it can conclude that larger injection position cause larger threshold voltage shift and that is reason why SB-SONOS devices have fast program speed.

From programming characteristics, as shown in Fig. 5-10, DSSB-SONOS devices have larger threshold voltage shift with program time of 10^{-7} and 10^{-6} seconds. Owing to

DSSB-SONOS devices have larger electric field at source side region compared to SB-SONOS devices. But when increasing the programming time, SB-SONOS devices show larger threshold voltage shift, due to larger injection position for electrons, causing larger memory window.



(a)



(b)

Fig. 5-10 (a) The program characteristics of conventional SONOS, SB-SONOS, DSSB-SONOS devices. (b) The typical sketch for injection position of SB-SONOS and DSSB-SONOS devices.

Fig. 5-11 shows the erase speed of conventional SONOS, SB-SONOS, and DSSB-SONOS devices. SB-SONOS devices show the fast erase speed for the threshold voltage shift nearly to 2V with erase time of 10^{-1} seconds compared to the other devices. The fast erase speed for SB-SONOS devices are due to ambipolar effect which causing hole can easily tunnel through to channel, as shown in Fig. 3-2. However, SB-SONOS devices show small on current that makes it hard to differentiate between "0" and "1", as shown in Fig. 5-12. The on/off ratio is merely 3.03×10^{1}. In order to overcome the problem, DSSB-SONOS devices have been attempted to replace SB-SONOS, due to large on current. In other words, sacrifice the memory window and programming speed to obtain higher on-off ratio.

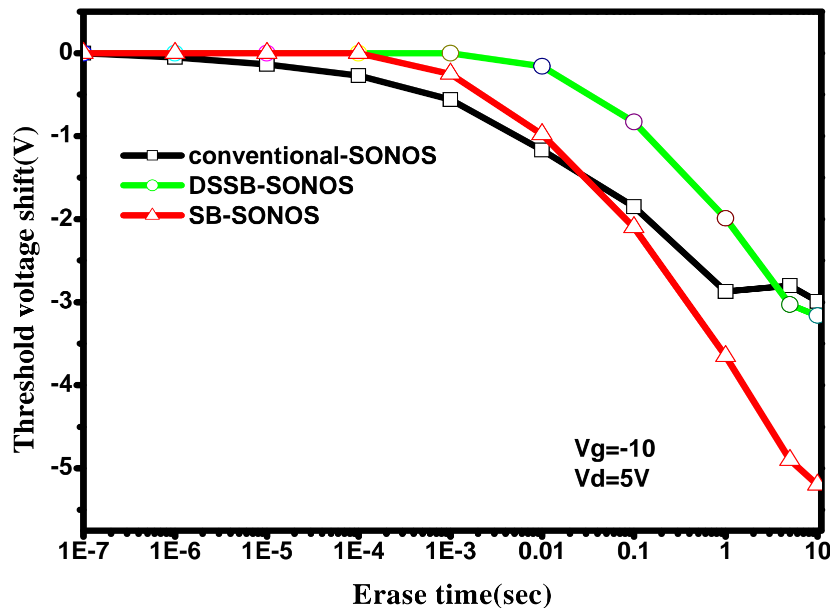


Fig. 5-11 The erase characteristics of conventional SONOS, SB-SONOS, DSSB-SONOS devices.

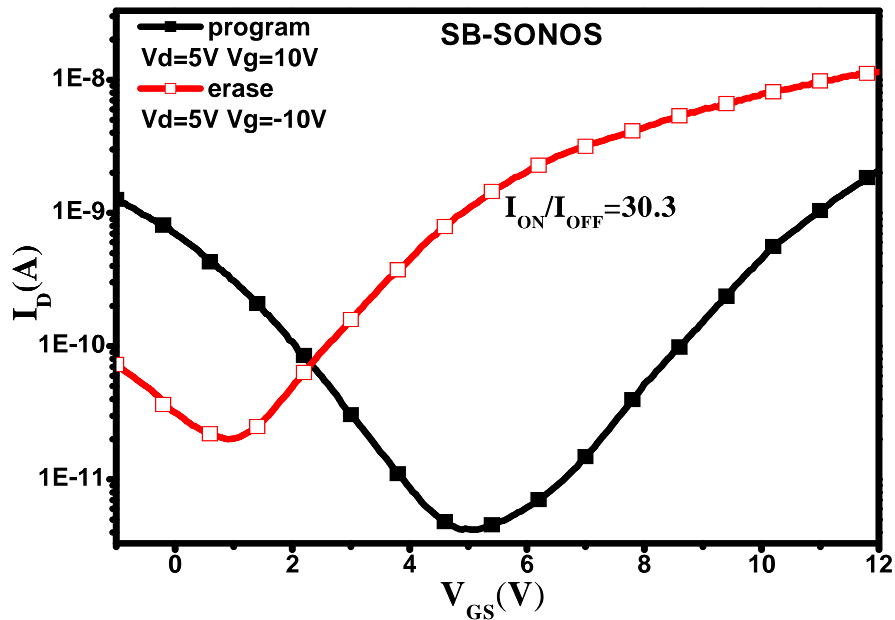


Fig. 5-12 Transfer characteristics of SB-SONOS devices.

The activation temperature is the most important process parameter to form dopant segregation. The transfer characteristics of DSSB-SONOS devices with different activation condition are listed in Table 5-2. From Table 5-2, it shows the transfer characteristics for annealing condition from 500℃ 30seconds, 60 seconds, 600℃ 30 seconds, 60 seconds, 90 seconds, 120 seconds, to 700℃ for 30 seconds, 60 seconds. It shows the tendency for activation temperature 500℃, the on current increases with increasing the activation time. For 600℃, the on current decreases with increasing the activation time. And for 700℃, it is found the on current decreasing significantly, especially for short channel device.

RTA (for activation)		Ion(μA)	Ioff (pA) (V_G@0.6V)	V_G@-8V(nA)	Ion/Ioff @V_D=3V
Temp(℃)	Time(sec.)				
Device Width=3μm, Length=1μm					
500	30	77.69	45.14	24.35	1.7×10^6
	60	114.66	59.97	106.65	1.9×10^6
600	30	22.01	40.49	5.13	5.4×10^5
	60	12.59	17.77	3.24	7.1×10^5
	90	14.79	24.23	7.06	6.1×10^5
	120	7.88	22.53	3.40	3.5×10^6
700	30	X	X	X	X
	60	X	X	X	X
Device Width=3μm, Length=10μm					
700	30	0.18	93.34	1765.1	1.95×10^3
	60	0.095	19.74	503.7	4.81×10^3

Table 5-2 The transfer characteristics of DSSB-SONOS devices with dopant activation annealing at 500℃ for 30seconds, 60seconds, 600℃ for 30seconds, 60seconds, 90seconds, 120seconds, and 700℃ for 30seconds, 60seconds.

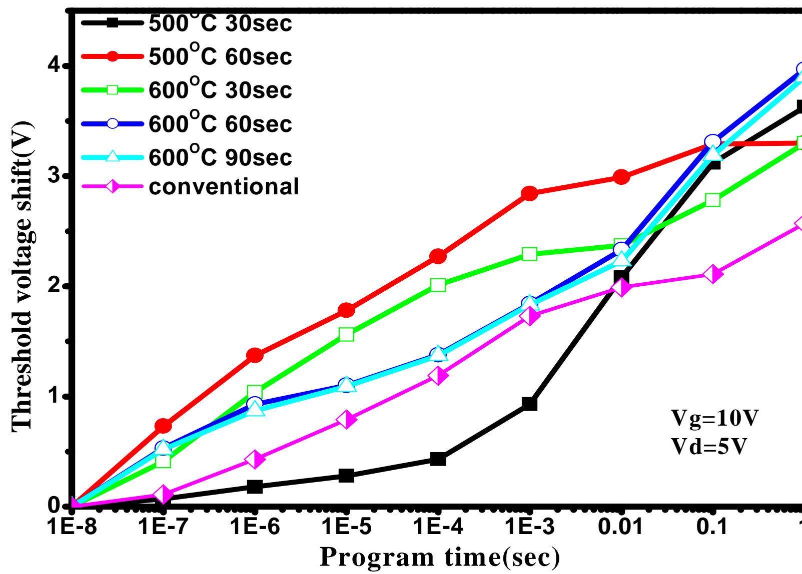
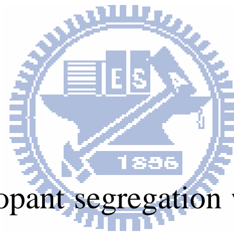


Fig. 5-13 Programming characteristics of DSSB-SONOS devices with different activation condition.



This result is attributed to dopant segregation width. When activation temperature at 500℃ 30seconds, it shows insufficient thermal budget, causing insufficient dopant segregation width at Si and NiSi interface. When increasing the annealing time to 60seconds, dopant segregation width increase, providing large band bending at source side region. Hence, the on current increases for activation temperature at 500℃ 60seconds compared to activation temperature at 500℃ 30seconds. The result can also be responded at program speed, as shown in Fig. 5-13. Fig. 5-13 shows the program speed for different annealing condition of DSSB-SONOS and conventional SONOS devices. For DSSB-SONOS devices with activation condition at 500℃ 30seconds, small electric

field is across at source side region, owing to not enough dopant concentration segregate at silicide and silicon interface. When increasing the annealing time to 60seconds, the program speed increase significantly due to enough thermal budgets for dopant activation. The SIMS spectra for activation condition of 500℃ are shown in Fig. 5-14. For annealing temperature to 600℃, it is found that the on current and program speed decreases with increasing annealing time, owing to dopant segregation width increases. And cause the Schottky barrier junction approach to p-n junction, in other word, the advantage for DSSB-SONOS will disappear. It can be shown at Fig. 5-15, when annealing temperature increase to 600℃ 90 seconds, program speed is approach to conventional SONOS. The SIMS spectra for activation condition of 600℃ are shown in Fig. 5-15.

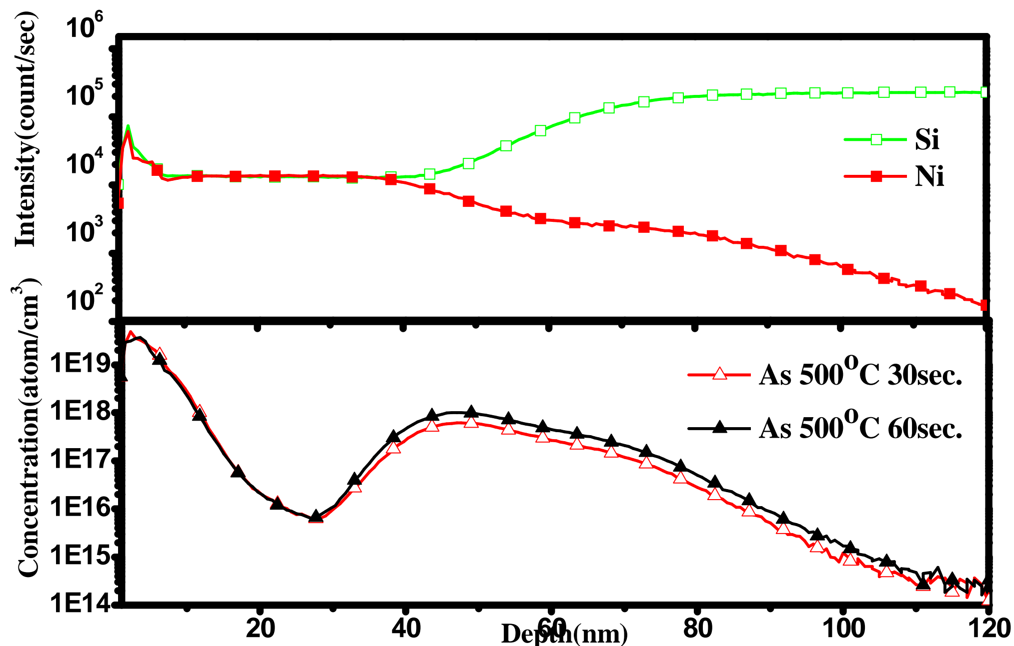


Fig. 5-14 The SIMS depth profile of Ni, Si, and As with 500℃ activation annealing.

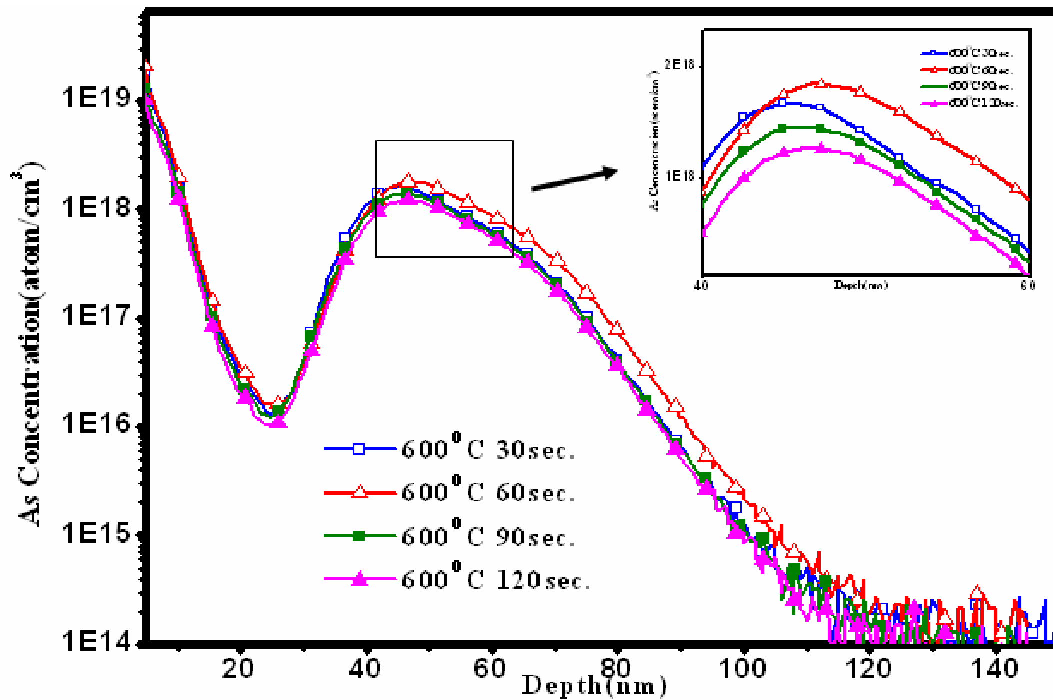


Fig. 5-15 The SIMS depth profile of As with 600℃ activation annealing.

Fig. 5-16 propose the erase speed with V_G=-12V and V_D=5V, it shows that DSSB-SONOS devices have poor erase efficiency, owing to DSSB-SONOS devices minimize hole tunneling to channel, hence the erase speed is slow. And SB-SONOS devices have high erase efficiency, due to ambipolar effect. It is well known that SB-SONOS have large leakage currents, causing hole can easily tunnel to channel furthermore causing large number of hole tunnel to nitride, due to vertical electric field, as shown in Fig. 3-4(b).

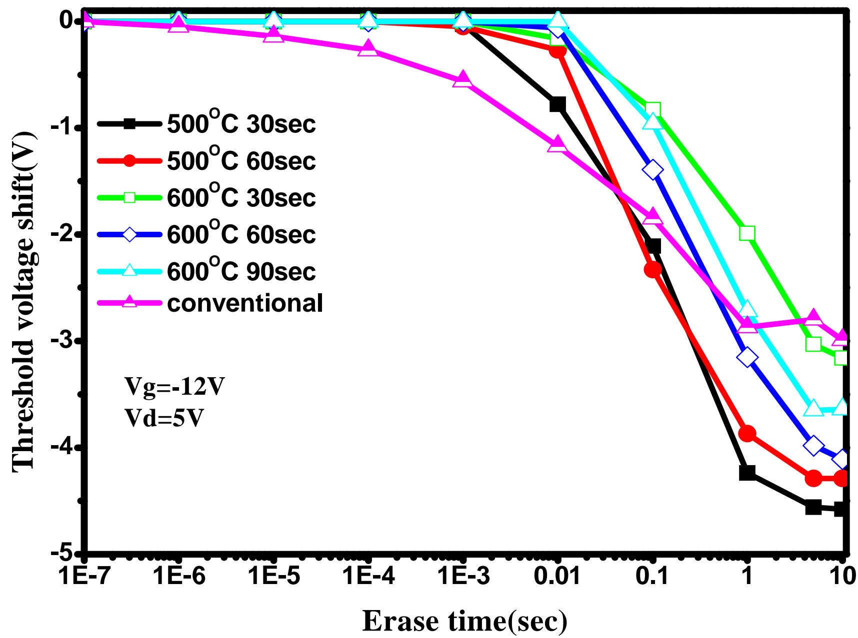


Fig. 5-16 Erasing characteristics of DSSB-SONOS devices with different activation condition.

For activation condition of 700℃ 30seconds and 60 seconds, it shows that devices degrade significantly, owing to NiSi is transforming to $NiSi_2$ phase. It is well known that $NiSi_2$ phase have higher resistivity, moreover the phenomenon for NiSi agglomeration is occurred, causing the broken circuit. Fig. 5-17 shows the top view of source/drain for DSSB-SONOS devices with different activation time and activation temperature. Fig. 5-18 shows the SEM image for annealing 700℃. It can be clearly found that NiSi agglomeration is occurred. And that is the reason why the performance degrades significantly for activation condition of 700℃ 30sec and 60sec DSSB-SONOS devices

[26].

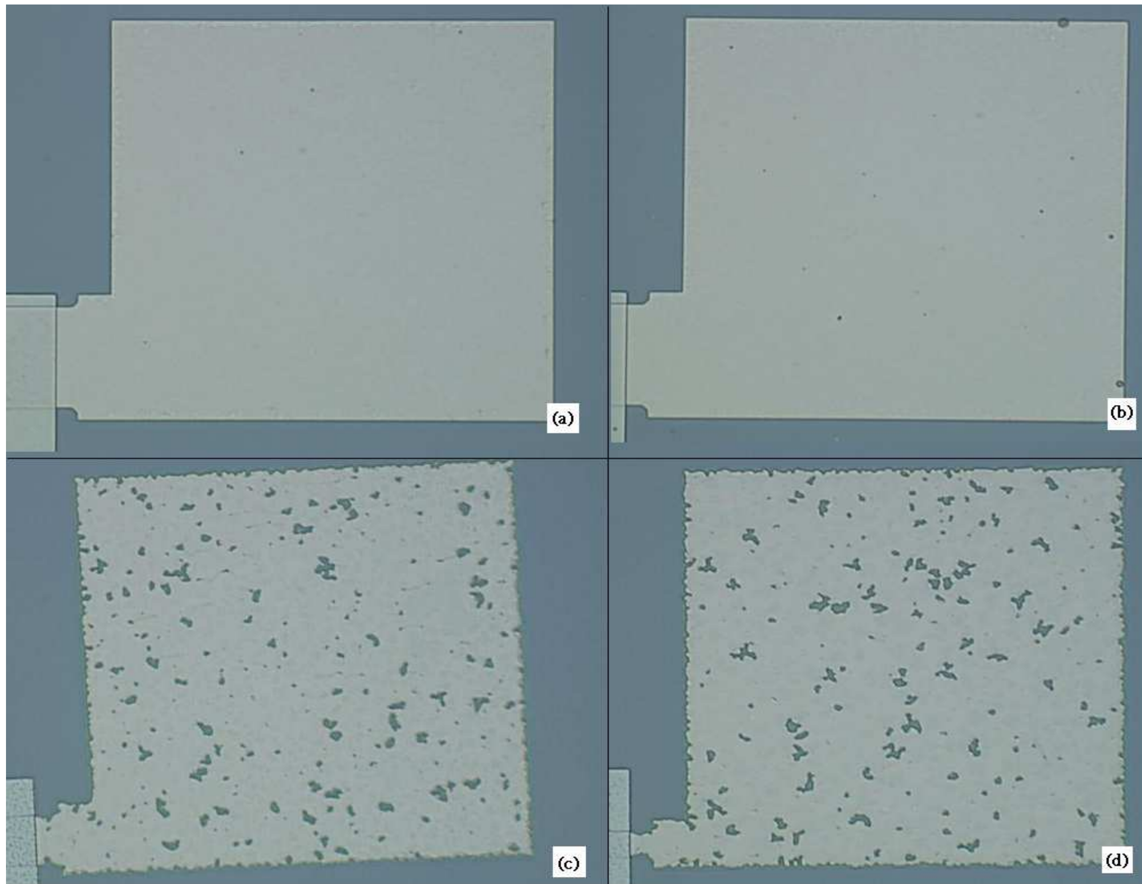


Fig. 5-17 Top view of source/drain for DSSB-SONOS with activation time (a) 600℃ 30seconds (b) 600℃ 120seconds (c) 700℃ 30seconds (d) 700℃ 60seconds.

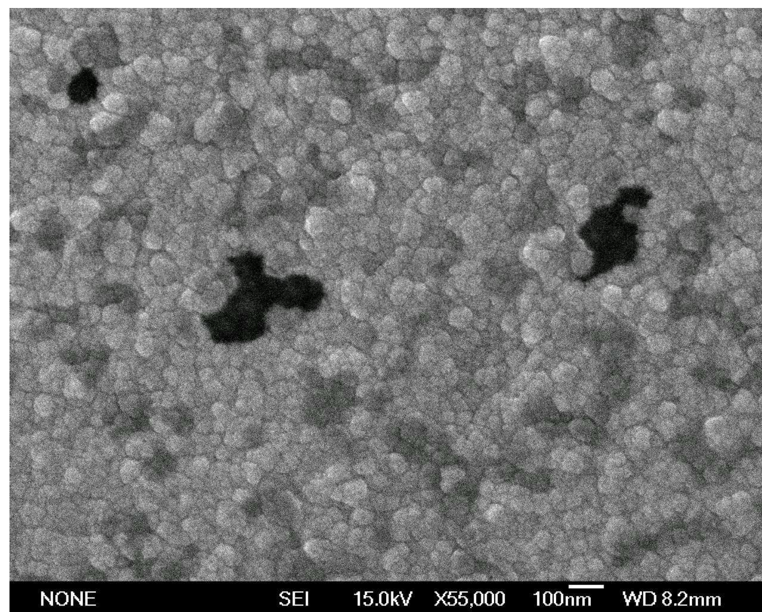
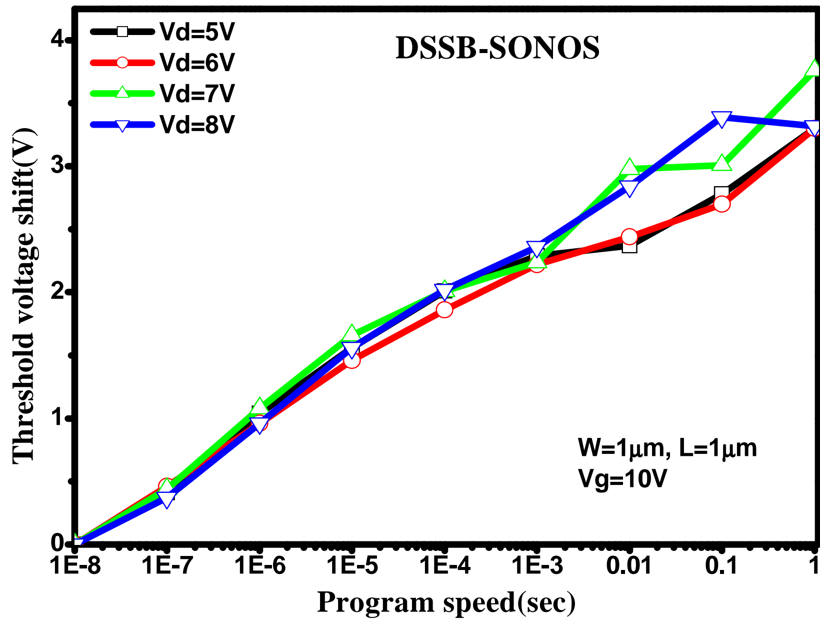


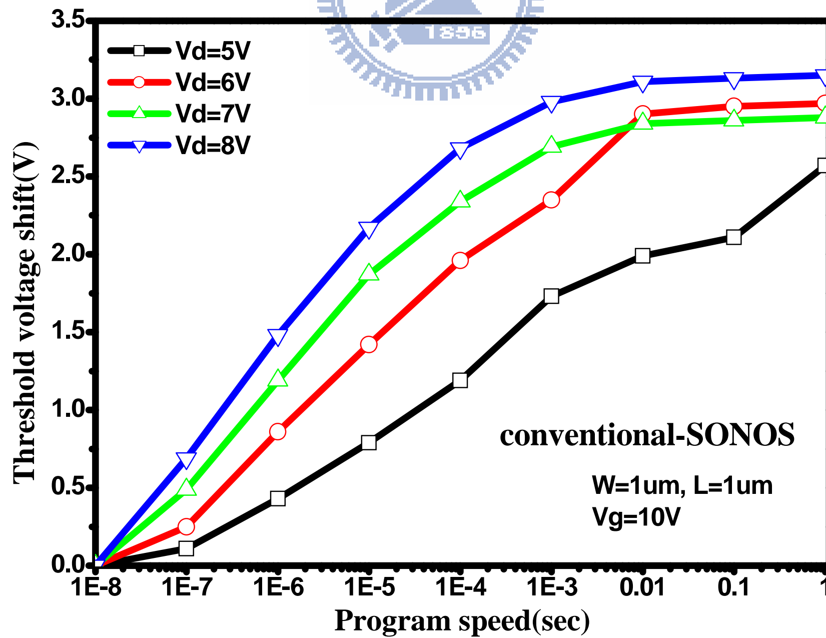
Fig. 5-18 SEM image of NiSi with activation temperature at 700℃.

5-4. The Characteristics of SB-SONOS and DSSB-SONOS Memory Devices by Using Different Method for Programming

In order to prove that SB-SONOS devices demonstrate the source-side injection of hot electrons that achieves high-speed programming. This time try to use F-N tunneling and CHEI mechanism for programming. Fig. 5-19(a) shows the program speed with different drain bias of 5V, 6V, 7V, 8V for DSSB-SONOS devices and Fig. 5-19 (b) are for the conventional SONOS devices. For conventional SONOS devices, the program speed increase when increasing drain bias. Since using CHEI for programming, charges get energy at drain side region. So when increasing drain bias, lateral electric field increase and causing electron gain energy tunneling to nitride at drain side region, as shown in Fig. 2-4 [31]. However the behavior for DSSB-SONOS devices is exactly different to conventional SONOS devices. DSSB-SONOS devices show the same program speed when applying different drain bias. For DSSB-SONOS, it uses source side injection mechanism, which means independent to drain bias, the tendency is similar to F-N tunneling; causing the program speed only depends on gate to source bias. Later, it will use F-N tunneling for programming to prove that source side injection is similar to F-N tunneling.



(a)



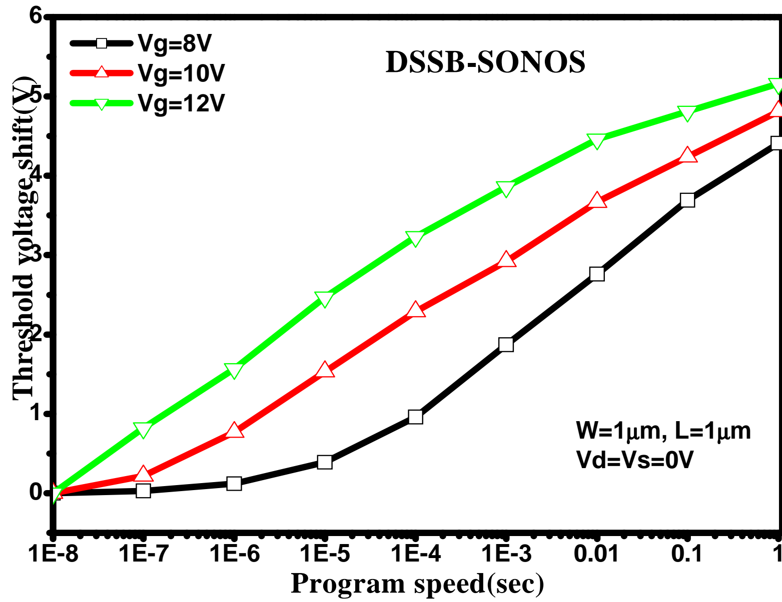
(b)

Fig. 5-19 Programming characteristics of (a) DSSB-SONOS devices (b) conventional SONOS devices with different drain bias for 5V, 6V, 7V, 8V.

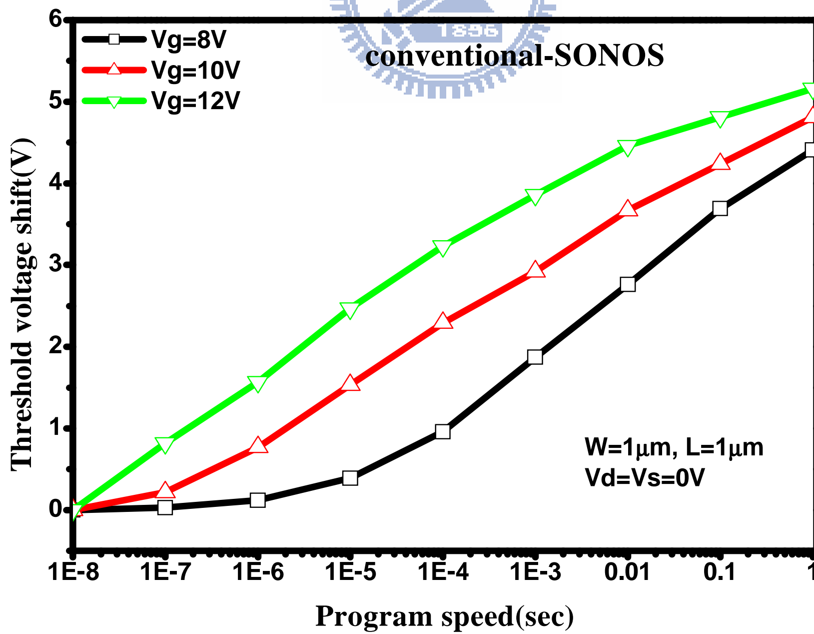
Fig. 5-20(a) shows the program speed with gate bias of 8V, 10V, 12V for DSSB-SONOS devices and Fig. 5-20(b) are for the conventional SONOS devices. When using F-N tunneling for programming, it is found that both conventional SONOS and DSSB-SONOS devices have the tendency for the program speed increases with increasing the gate bias. Moreover it can also be observed that both devices have the same program speed. When programming, both devices exhibit V_{TH} shift about 2V, under the program condition of V_G=10V with program time of 10^{-4} seconds. It is well known that when using F-N mechanism for programming, the program speed is only related to vertical electric field, as shown in formula 2-3 [27-29].

$$T_{F-N} = \exp(-\frac{4\sqrt{2m^*}(q\phi_B)^{1.5}}{3q\hbar\varepsilon_x}), \quad (2\text{-}3)$$

Moreover, Fig. 5-19(a) also shows the threshold voltage shift nearly to 2V when programming with V_G=10V and V_D=5~8V with program time of 10^{-4} seconds. It shows almost the same program speed by using F-N tunneling mechanism and CHEI mechanism. Therefore, it can be concluded that DSSB-SONOS devices use source side injection for programming and the mechanism is close to F-N tunneling mechanism rather than CHEI mechanism.



(a)



(b)

Fig. 5-20 Programming characteristics of (a) DSSB-SONOS (b) conventional SONOS devices with different gate bias for 8V, 10V, 12V.

5-5. The Retention and Endurance Characteristic of SB-SONOS and DSSB-SONOS Memory Devices

The charge retention performance of conventional SONOS and SB-SONOS devices are compared in Fig. 5-21. The programming condition is V_G=10V and V_D=5V with program time one second. And the erasing condition is V_G=-12V and V_D=5V with erase time five seconds. The memory window is expected to have 0.7V and 4.3V respectively for conventional SONOS and SB-SONOS devices after ten years at room temperature. Owing to SB-SONOS has large memory window compared to conventional SONOS.

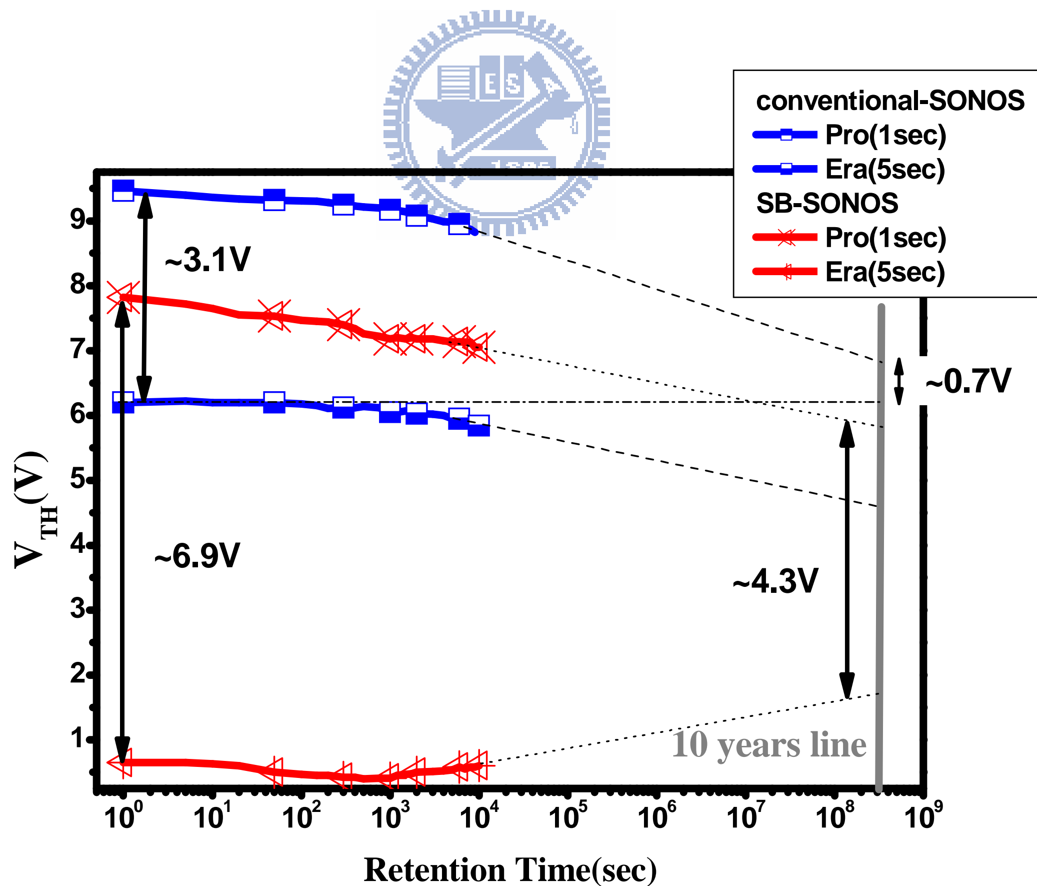


Fig. 5-21 Retention characteristics of conventional SONOS and SB-SONOS devices at room temperature.

Fig. 5-22 shows the fresh state and post cycled retention characteristics of DSSB-SONOS devices. The program condition is V_G=10V and V_D=5V with program time 50ms and the erase condition is V_G=-12V and V_D=5V with erase time 500ms. For DSSB-SONOS devices at fresh state, the memory window decrease from 4V to 3.2V and for devices with 10^4 times P/E cycles, the memory window decrease from 1.9V to 1.2V. Compared with fresh state device, post cycled devices shows V_{TH} increasing in program state and erase state. This is due to interface trapped. For DSSB-SONOS, after 10^4 times P/E stressed, tunneling oxide might be damaged, causing interface states increased. The phenomenon for V_{TH} increasing might be caused by the electrons trapped at tunneling oxide interface. Fig. 5-23 shows the endurance characteristics of DSSB-SONOS devices. It shows the V_{TH} significantly increasing in erased state for device which is stressed for 10^4 times. These characteristics are measured at room temperature. The V_{TH} window is expected to have a value of 1.3 V after 10^4 times P/E cycles.

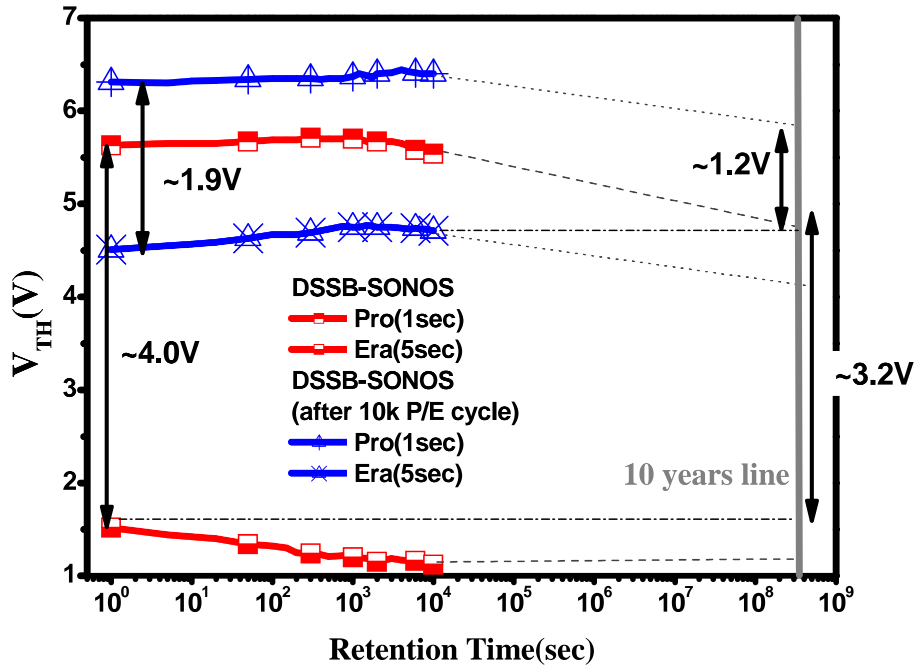


Fig. 5-22 Retention characteristics of DSSB-SONOS devices under fresh state and after 10^4 times P/E cycles.

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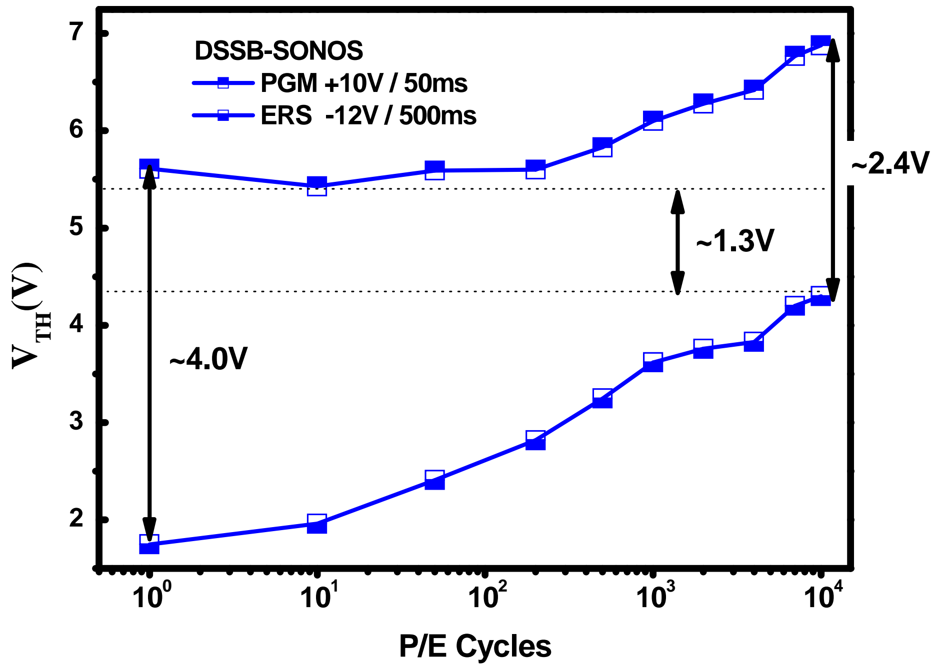

Fig. 5-23 Endurance characteristics of DSSB-SONOS devices.

Fig. 5-24 shows the fresh state and post cycled retention characteristics of SB-SONOS devices. The program condition is V_G=10V and V_D=5V with program time 50ms and the erase condition is V_G=-12V and V_D=5V with erase time 500ms. Fig. 5-25 shows the endurance characteristics of SB-SONOS devices. For SB-SONOS devices at fresh state, the memory window decrease from 6.9V to 4.3V but for device with 10^4 times P/E cycles, the memory window decrease significantly. Moreover, from endurance characteristics, it shows negligible degradation on threshold voltage. That means the gate oxide damaged seriously after 10^4 times P/E cycles, causing carrier can easily tunneling into nitride and easily leak out from nitride.

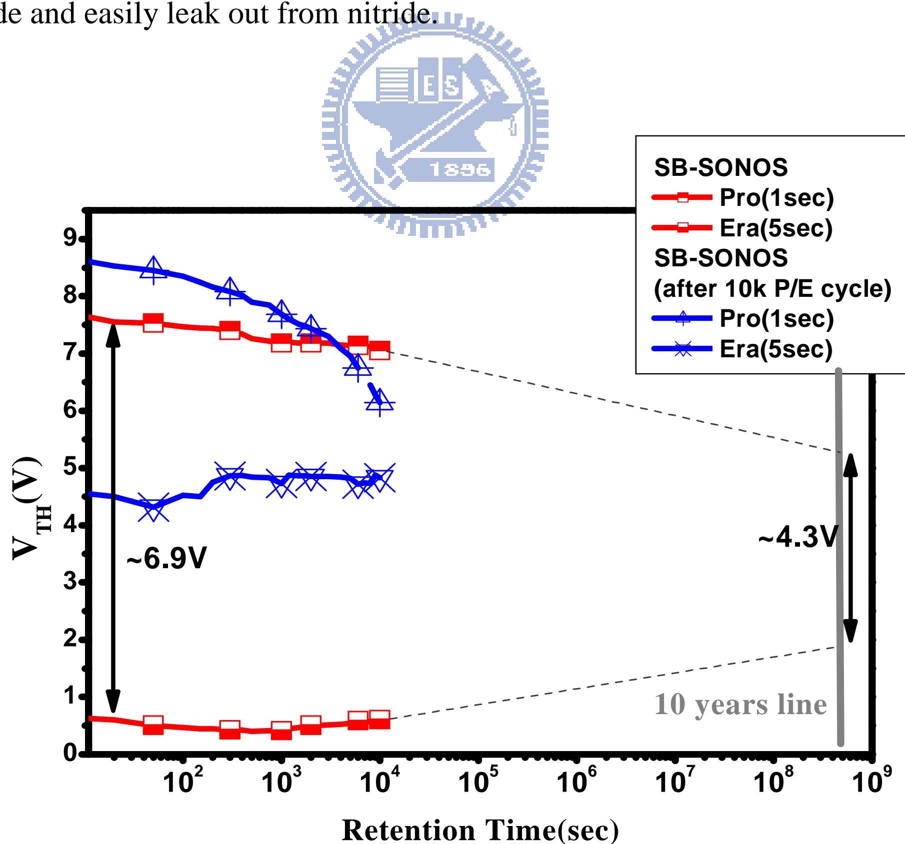

Fig. 5-24 Retention characteristics of SB-SONOS devices for fresh state and after 10^4 times P/E cycles.

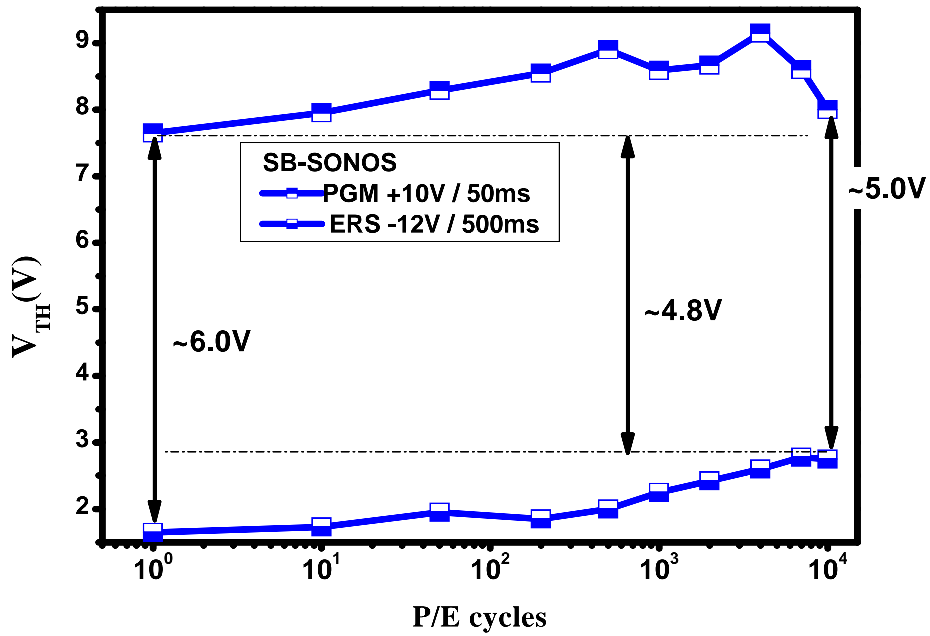

Fig. 5-25 Endurance characteristics of SB-SONOS devices.

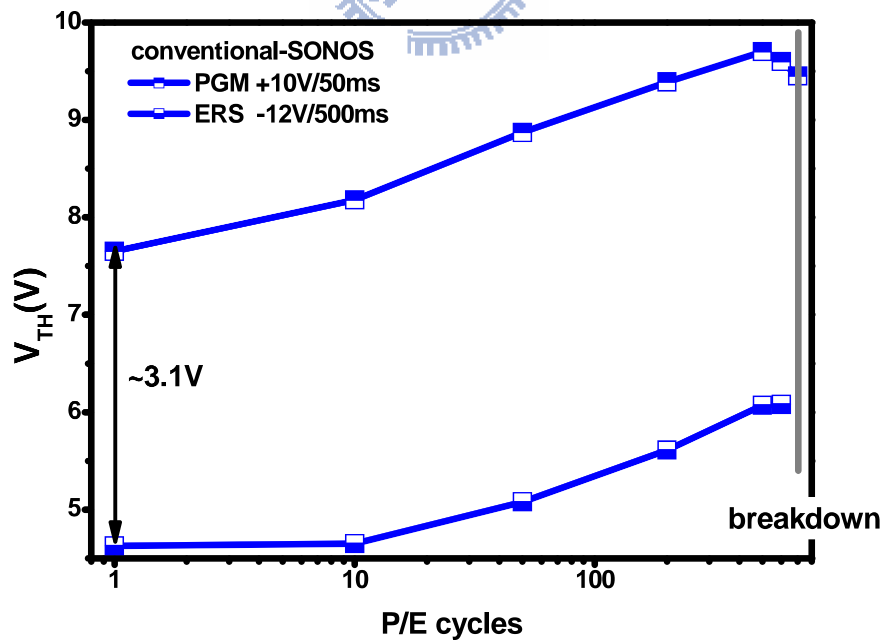

Fig. 5-26 Endurance characteristics of conventional SONOS devices. (When P/E cycles about 700 times, the device breakdown)

For conventional SONOS devices, when applying V_G=10V and V_D=5V, that means CHEI mechanism dominates, as shown in Fig. 2-4. And cause impact-ionization at drain side region, so the devices will breakdown easily, as shown in Fig. 5-26; on the other hand, DSSB-SONOS and SB-SONOS devices do not use CHEI mechanism even though under the same P/E condition. DSSB-SONOS and SB-SONOS devices dominate source side injection, causing program speed is independent to drain bias, and it can be considered that the program mechanism is like F-N tunneling. Hence, after P/E cycles, conventional SONOS shows larger V_{TH} degradation compared to DSSB-SONOS and SB-SONOS devices. SB-SONOS devices show poor retention performance after 10^4 times P/E cycles compared to DSSB-SONOS devices. Owing to SB-SONOS devices have larger injection width compared to DSSB-SONOS devices which have small injection width at source side. Therefore, SB-SONOS after 10^4 times P/E cycles, tunneling oxide may increase plenty of interface states compared to DSSB-SONOS devices which increase a little interface state, causing degrades easily.

5-6. Summary

Table 5-3 shows the performance for conventional SONOS, SB-SONOS, and DSSB-SONOS devices. From the table it is found that although SB-SONOS devices

show fast program speed, erase speed, and large memory window, but the on/off ratio are too small to differentiate between “0” and “1”. Hence, by sacrificing the program speed, erase speed, and memory window to get larger on/off ratio, therefore in my opinion DSSB-SONOS devices are the promising devices for non-volatile flash memory.

	Conventional-SONOS	**SB-SONOS**	**DSSB-SONOS**
On current(A)	6.85×10^{-7} (good)	4.02×10^{-9} (bad)	6.71×10^{-5} (best)
Off current(A)	8.32×10^{-9} (good)	4.88×10^{-7} (bad)	4.59×10^{-9} (best)
Memory-window	3.2V(bad)	6V(best)	4V(good)
Program speed (10^{-4} **second)**	1V(bad)	3V(best)	2V(good)
Erase speed (10^{-1} **second)**	1.7V(good)	2V(best)	0.5V(bad)
Retention (Fresh state)	0.7V(bad)	4.3V(best)	3.2V(good)
Retention (After 10^{4} **times P/E cycles)**	X(Breakdown)	0V	1.2V

Table 5-3 Performance of onventional SONOS, SB-SONOS, and DSSB-SONOS devices.

CHAPTER 6

Conclusions

High performance DSSB-SONOS devices have been demonstrated in this work. Since, approximate constant Schottky barrier potential located at source side region, DSSB-SONOS devices could eliminate the short channel effect and provide fast programming speed. This work also proves that the source side injection of hot electron achieves high speed and low voltage programming by using F-N tunneling and channel hot electron injection mechanism. Because of source side injection, the program speed of the DSSB-SONOS devices is independent to drain bias. DSSB-SONOS devices exhibit V_{TH} shift maintain of 2V under the program condition of V_G=10V and V_D=0~8V with program time of 10^{-4} seconds. It is proven that source side injection is similar to F-N tunneling.

SB-SONOS devices have largest memory window about 6V, compared to DSSB-SONOS and conventional SONOS devices. Memory windows of conventional SONOS and DSSB-SONOS devices are 3V and 4V, respectively. Moreover, SB-SONOS devices provide fast program speed for V_{TH} shift about 3V with programming time of 10^{-4} seconds, compared to DSSB-SONOS for 2V and conventional SONOS for 1V. However the major restriction for SB-SONOS is the small on current that makes it

difficult to differentiate between “0” and “1”. Therefore DSSB-SONOS has been attempted to replace SB-SONOS, due to large on current. Compared to conventional SONOS, DSSB-SONOS indeed improve the device performance. And for SB-SONOS, the on/off ratio is 30.3, but for DSSB-SONOS the on/off ratio improves to 1.9×10^{6}. The experiment shows that an activation annealing at 500℃ for 60seconds is sufficient to produce excellent DSSB-SONOS devices.

Retention characterization for fresh devices, SB-SONOS degrades from 6.9V to 4.3V, DSSB-SONOS degrades from 4.0V to 3.2V, and conventional SONOS degrades from 3.1V to 0.7V. After endurance test, DSSB-SONOS has memory window of 1.2V, but for conventional SONOS, it is breakdown after less than 1000 times P/E cycles. Since conventional SONOS depends on impact-ionization to produce hot carrier, on the contrary SB-SONOS and DSSB-SONOS depends on the high lateral electric field at source side region, no impact-ionization occurred causing better retention and endurance characteristics.

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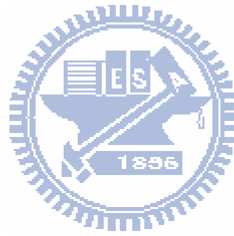

簡歷

姓名：張民尚

生日：民國 75 年 6 月 18 日

地址：台北市和平東路 3 段 269 號 9 樓

學歷：國立交通大學電子工程學系畢

93 年 9 月~97 年 6 月

國立交通大學電子研究所碩士班畢

97 年 9 月~99 年 10 月

碩士論文題目：

具摻雜析離層蕭特基 SONOS 之元件製作與特性分析

Fabrication and Characterization of Dopant Segregated Schottky Barrier SONOS Devices